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BROOKHAVEN FASTBUS ADC's

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ABSTRACT

A high energy physics experiment has been performed at Brookhaven National Laboratory on $K^0_L \to 2\pi^0$ decays employing a large (> 200 element) lead glass array as an electromagnetic calorimeter. To acquire pulse height information from the detector we have constructed ADC modules in the context of the Brookhaven Fastbus data acquisition system. Digitization (8 bits) and encoding, including pedestal subtraction and data sparsing, is achieved for each 16 channel module in 6 μsec.

Introduction

For Brookhaven AGS experiment #749, 256 channels of analog to digital converter (ADC's) have been built in order to acquire pulse height information from a large array of lead glass counters via the BROOKHAVEN FASTBUS[1] data acquisition system. The ADC boards have been constructed as 16 channel devices; hence there are 16 modules available for use in an 130 pin water cooled crate segment. Each board is of hybrid construction consisting of an analog front end (PC layout) and a digital interface (wirewrap kludge card). In what follows we present an overview of the device design and operation and a review of the protocol for accessing data from and controlling the status of the ADC modules.

Analog Front End

The heart of each ADC channel is the LeCroy QT100P hybrid, a high speed charge to time converter, which is used in a Wilkinson run-down analog to digital conversion circuit. An external GATE allows charge from the signal INPUT onto an internal capacitor. A constant current source bleeds the charge off the capacitor and an internal comparator senses the voltage at the capacitor providing an ECL OUTPUT signal whose width is proportional to the injected charge. The trailing edge of the OUTPUT signal is used to latch the contents a clock which was started at a time associated with the GATE. The INPUT signal is assumed to be a fast negative pulse (from a photomultiplier tube) which is accepted via a front panel (50 ohm coax) connection. The run-down current is determined by voltages (V_4,V_5) applied to pins on the QT100P.

Note that even with no INPUT signal a certain amount of charge will be injected into the QT100P. This constitutes the PEDESTAL. Each channel has an adjustable trimmer capacitor to compensate for differences in the various channels, although as is discussed later, there is no need for these trimmers to be adjusted exactly.

From our studies, we have found that there is an appreciable (≈ 20%) amount of pulse height information contained in scintillation light emitted in the lead glass Cerenkov counters. A longer integration period is required to collect the charge associated with this light. Thus we have chosen to use a GATE width of about 100 nsec. In order to retrieve the timing information inherent in the fast Cerenkov light pulse, each ADC channel has additional circuitry, comprised of a fast comparator and a D type flip-flop, which are used as a discriminator and latch. The timing is determined by the coincidence of the comparator output with a STROBE.

The ADC circuitry is such that the integrated pulse height information is digitized with 8-bit resolution. While the QT100Po have an input capacity of 256 pC, we have chosen to use 128 pC as the full scale input value, in order to operate the photomultiplier tubes at lower voltages. The digitization circuitry (described in some detail later) is driven by an 80 MHz ECL crystal oscillator. The run-down time is comprised of 256 time periods of 6.25 nsec in duration, and the run-down current is set at 128 pC/1600 nsec = 0.08 mA, which determines the differential V_5-V_4. This implies that the ADC responds to inputs in a linear fashion with a slope of 0.5 pC/bin. Our arrangement of lead glass Cerenkov counters with Amperex 2212 photomultiplier tubes (modified for high rate environments) give outputs with effective widths of ≈ 15 nsec, so that a translation of the ADC sensitivity into terms of pulse height yields (0.5 pC/bin) * (50Ω)/15 nsec ≈ 1.67 mV/bin.

Digital Interface

The remainder of the ADC electronics consists of the circuitry required for the control of the digitization process, the encoding of the data into a memory STACK, and the SLAVE protocol required for control and readout of the ADC module via FASTBUS. The design is based on ECL series 10,000 logic which is wire wrapped (point to point) on the BROOKHAVEN FASTBUS MULTI-PURPOSE (kludge) card. The digitization, data scan, and STACK filling are all governed by the fundamental CLOCK (80 MHz), so that operations are synchronous; FASTBUS access is handled asynchronously.

Digitization is achieved by using the OUTPUT signal of each QT100P (the width of which is proportional to the INPUT charge) to latch, "on the fly", the contents of an 8 bit Grey coded counter. The starting of the Gray coded counter is determined by synchronizing circuitry triggered by the GATE input. An RC governed monostable multivibrator is used to allow the beginning of digitization time to be adjusted to compensate for major changes in pedestal (common to all channels on the board).

The data is scanned one channel at a time, and the scanning cycle is governed by a 10 MHz clock cycle which allows for data conversion and memory setup times. The 8 bits of Gray code are converted to binary and then enter a subtractor where a 4 bit field representing a predetermined value for the pedestal may be subtracted. Conditionals on the magnitude of the result of the subtraction are tested and valid data is subsequently pushed onto the stack. The time required for complete digitization, including the data sparsing and encoding onto the stack, is less than 6 μsec.

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The pedestals used in the subtraction mentioned above are accessed via the channel pointer from a 16 by 4 bit memory accessable via FASTBUS (as READ/WRITE RAM). The data scan operation can proceed in two modes, in the first the contents of the pedestal memory are ignored, that is no subtraction takes place and the conditionals are then ignored so that each channel always has valid data. This is the mode through which one determines the pedestal. The second mode employs the contents of the pedestal memory and the conditionals from the subtraction of the pedestal from the data to determine if the data is VALID.

The conditionals for subtracted data (determined by wire wrap jumpers) include a test for values larger than a fixed positive threshold and less (more negative) than a fixed negative threshold. Thus inputs which are digitized with pedestal subtracted values which are greater than threshold are considered valid and thus recorded so that the data readout is already sparsed for important "hits".

The STACK, which is READ ONLY FILO from the viewpoint of a FASTBUS MASTER, consists of a 16 by 15 bit memory containing the channel number (4 bits), the data (8 bits with or without pedestal subtraction), the timing bit (on if the leading edge of the pulse was in time with the strobe, the overflow bit (on for error), and the negative bit (on for error). After each FASTBUS READ the STACK pointer is automatically bumped down, and the control circuitry indicates LAST VALID data in the module based on the return of the STACK pointer to the bottom of the STACK. After this final READ, RESET circuitry is activated which drains (via the CLR pin) any charge remaining in the QT100Ps, resets all data and error flag flip-flops, the channel and stack pointers, and the Gray coded counter. The RESET procedure is the same used for FAST CLEAR (initiated by the front panel input), FASTBUS generated CLEAR or ABORT (via broadcast, or via a special control register), or a change of the module's MODE (via FASTBUS through a control register). The RESET period is approximately 500 nsec in duration.

FASTBUS Access and Control

The ADC board performs as a FASTBUS SLAVE following the BROOKHAVEN FASTBUS protocol. Each module has a width of 20_8 in address or control space, which is selected using the four least significant address lines (A/D 0-3). The 16 modules are differentiated by the next 4 address lines, A/D 4-7, as preselected by a 4 bit binary switch.

The ADC module functions in one of three modes: MODE 0 in which pedestal subtracted data is available from the STACK, MODE 1 in which unsubtracted data is available from the STACK, and MODE 2 in which the user may READ and/or WRITE data in the pedestal memory. MODE 0 is the default mode, to which the module returns after FASTBUS initialization has occurred (IT=1). In order to change the mode of the module, the user must access the Control Status Register, CRO, and write the desired mode to this register.

If a module is empty, as it can be in MODE 0 or 1 if no triggering GATE has been received, or in MODE 0 if no VALID data has been stored, a 32 bit word of zeros is returned. In the latter case note that a module still needs to be accessed (i.e., READ) in order to force the data RESET cycle, that is, a triggered but empty MODE 0 module must still be READ once (or otherwise CLEARed) in order to rearm it for the next event.

Valid FASTBUS requests occurring during the digitization period are often ignored (MODE manipulations, data accessing) but acknowledged with a BUSY (BK=1) flag. However FASTBUS initiated (as well as front panel initiated) CLEARs or ABORTs are always obeyed, immediately. Invalid FASTBUS requests (writing pulse heights, block transfers, access of unused CR space, etc.) are ignored and acknowledged with an (NK=1) flag.

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References

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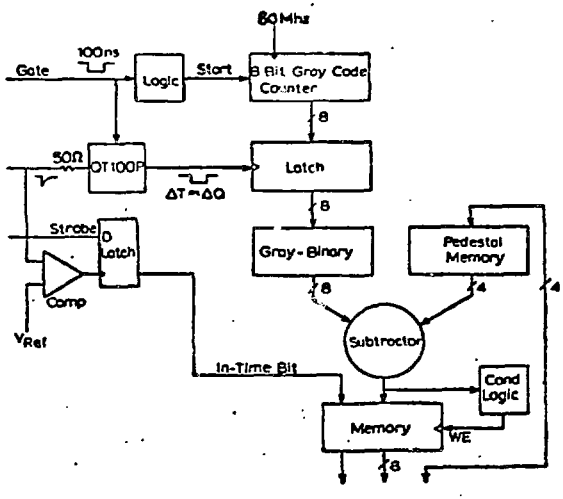

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