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STATISTICAL PROCESS CONTROL FOR QML RADIATION HARDNESS ASSURANCE

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35-word abstract

Key technical issues associated with QML implementation are identified. It is shown that ΔV_{ot} and ΔV_{it} shifts measured on test structures can be correlated with the radiation response of ICs from Sandia's 4/3-μm technology.

DISCLAIMER

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Effective testing of highly-complex VLSI circuits employing ever decreasing feature sizes is becoming extremely difficult. This difficulty arises from the inability to routinely provide 100% fault coverage during testing of these complex functions, as well as by a scarcity of functional parts inherent in low-volume/high-product-mix military-component manufacturing lines. Under the sponsorship of RADC and DESC, the government has proposed a Qualified Manufacturer's List (QML) methodology to qualify ICs for high reliability and radiation hardness. In this approach, a production line is certified on a "one-time" basis, and all product from that line is subsequently qualified per the requirements of MIL-STD-38535. The approach places a large burden on the manufacturer or production source, who is tasked with demonstrating that the quality of the part is "built in," as opposed to being "tested in." This "built-in" quality is assured by the proper control of the IC manufacturing sequence from design through assembly.

A quantitative understanding of two relationships, illustrated in Fig. 1, is essential to QML implementation. The first relationship focuses on the need to *extrapolate* the radiation response of an IC in actual threat scenarios (e.g. weapon and/or space) from simple, practical laboratory measurements. Work in recent years on total-dose "rebound" testing of hardened ICs is an example of performing the required extrapolation [1-4]. In "rebound" testing, an IC is irradiated at a laboratory dose rate (100 to 300 rad(Si)/s) and then annealed for 1 week at 100°C - the measured response following anneal has been shown to approximate hardened part response in space environments without the need for costly, time-consuming irradiations at space-like dose rates (<0.1 rad(Si)/s). A second relationship underscores the fact that QML methodology relies heavily on the evaluation of test structures, whose response to various threats and stresses must be *correlated* with the response of ICs fabricated on the line. These test structures can be macrocells (e.g., 1k SRAMs, random logic, buffers, etc.) on a Technology Characterization Vehicle (TCV) or capacitors from an in-line Process Monitor (PM). It is important that the test structures be designed to account for the radiation threat (total-dose, transient,..), failure mode, and technology. Establishing the two relationships outlined above represents a formidable technical challenge. In this summary, we explore the key technical issues associated with test structure-to-IC correlation. By reviewing data from over 250 lots processed in Sandia's 4/3-μm technology, we will demonstrate that ΔV_{ot} and ΔV_{it} shifts measured on test structures can be correlated with IC total-dose radiation response in weapon and space environments. The concept of "statistical process control (SPC) for radiation hardness assurance" will be introduced, and applied to the 4/3-μm data set.

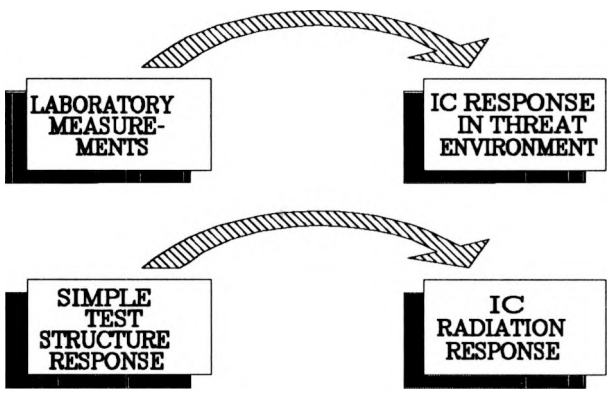

Figure 1. Two relationships are essential to QML implementation The first relationship is extrapolating the radiation response in threat scenarios from laboratory measurements (top) and the second is test structure-to-IC correlation (bottom).

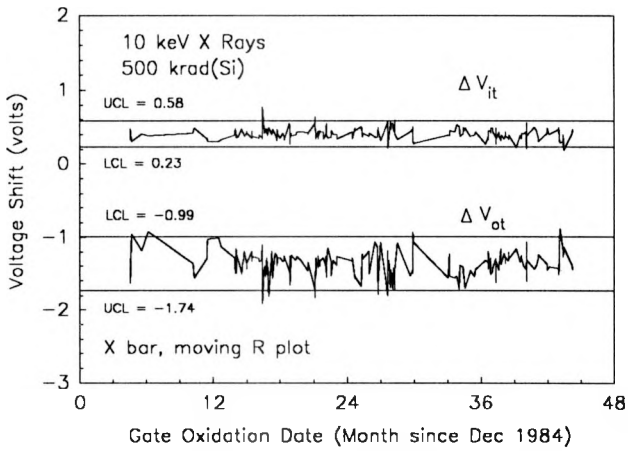

Figure 2. Control chart showing lot-to-lot variation of ΔV_{ot} and ΔV_{it} over a 40 month period for more than 250 lots fabricated in Sandia's 4/3-μm technology.

Figure 2 shows threshold-voltage shifts due to oxide-trapped charge, ΔV_{ot}, and interface traps, ΔV_{it}, following a 500-krad(SiO_2) wafer-level irradiation. The test devices, n-channel transistors with 45 nm gate oxides, were irradiated with +10 V between the gate and substrate. Irradiations were performed using a 10-keV ARACOR x-ray irradiator at a dose rate of 1800 rad(SiO_2)/s. (The x-ray irradiator dose rate of 1800 rad(SiO_2)/s does not fall within 100 to 300 rad(Si)/s dose-rate range specified by MIL-STD-883, method 1019; however, the x-ray irradiator is often used at this dose rate for wafer level testing.) Transistor threshold measurements were made within 3 minutes following irradiation and values of ΔV_{ot} and ΔV_{it} were determined by the method of Winokur and McWhorter [5]. SPC data for lot-to-lot variation of ΔV_{ot} and ΔV_{it} is shown over a 40 month period for more than 250 lots fabricated in Sandia's 4/3-μm technology. (Wafer-to-wafer and within wafer variations have not be included in this analysis, but will be included in the final paper.) Values of Xbar and upper and lower control limits (UCL & LCL) have been derived from the control chart data in Fig. 2; Xbar was -1.36 and +0.46 V for ΔV_{ot} and ΔV_{it}, respectively. The data in Fig. 2 is replotted in Figs. 3 and 4 as ΔV_{ot} and ΔV_{it} distributions, i.e., as the number of lots versus ΔV_{ot} and ΔV_{it} shifts. The data is approximately Gaussian for both distributions, and $\pm 3\sigma$ limits are noted for these 500-krad shifts. For ΔV_{ot}, the -3σ limit is at -1.85 V, while for ΔV_{it}, the $+3\sigma$ limit is at +0.65 V. It is not unreasonable to expect that the maximum ΔV_{ot} shift (given here as the -3σ limit in Fig. 3) will largely determine the tolerance of commercial and hardened CMOS technologies in weapon applications, and commercial CMOS and bipolar technologies in space applications; in both cases, failure is usually determined by large negative threshold-voltage shifts that lead to increases in leakage current. Similarly, the maximum ΔV_{it} shift (given here as the $+3\sigma$ limit in Fig. 4 will control part response in space applications where failure is caused by "rebound" and mobility degradation. Once a "mapping" or correlation between ΔVot and ΔVit shifts and IC radiation response can be demonstrated, the distributions indicate the "capability" (here defined as a radiation level) of the process/technology flow for total-dose radiation hardness. In order for the process to be "robust," 3σ limits for the process/technology must be well within system requirements for a given application. Another way of saying this is that the process/technology needs "margin" to meet its radiation requirements. The concept of "margin" within respect to QML methodology will be discussed further in the final paper.

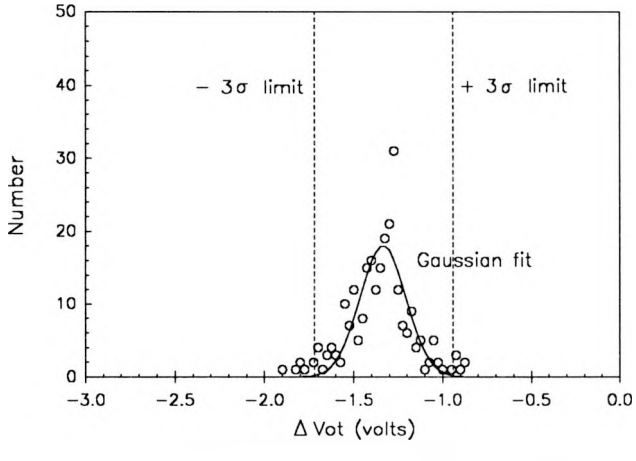

Figure 3. Distribution of ΔV_{ot} shifts following a 500-krad(SiO_2) x-ray irradiation for more than 250 4/3-μm lots processed over nearly 4 years.

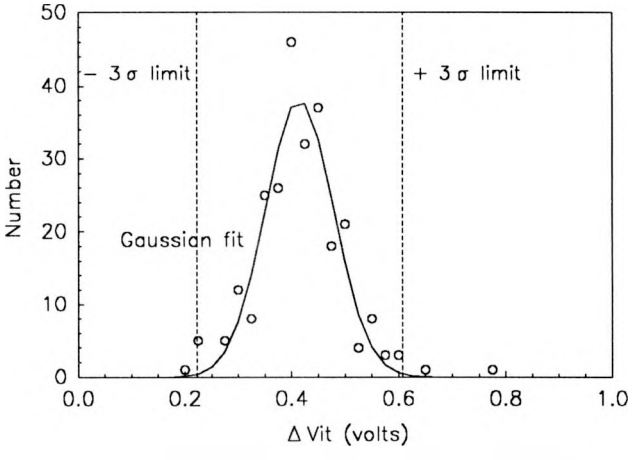

Figure 4. Distribution ΔV_{it} shifts following a 500-krad(SiO_2) x-ray irradiation for more than 250 4/3-μm lots processed over nearly 4 years.

The required demonstration of test-structure to IC correlation can be accomplished by: (1) performing a series of experiments on test structures and ICs, (2) using a set of design tools with appropriate radiation models to simulate or model circuit response from parametric test structure data, or (3) some combination of experiment and modeling. Radiation models might include physical, predictive models that can serve as inputs to SPICE or other design tools. An example would be a model that accounts for circuit "rebound" in space applications by modeling hole annealing [6] and interface-trap buildup for long-term, low dose-rate irradiations. An example of the experimental approach to test-structure to IC correlation is shown in Fig. 5. This figure shows a correlation between the ΔV_{ot} shift measured on an n-channel transistor following x-ray

irradiations at 1800 rad(SiO_2)/s and I_{DD} on an SA3001 2k SRAM following high-dose-rate irradiations. Transistors were irradiated with +10 V between gate and substrate and SRAMs were irradiated with a +10 V static bias applied in a checkerboard pattern. From the figure, I_{DD} appears to depend roughly exponentially on ΔV_{ot} for three different processes with varying radiation hardness. If parametric failure on the IC is chosen as 3 mA following the high-dose-rate irradiation, then ΔV_{ot} shifts less than or equal to -1.5 V are required (as shown by the dashed lines). Based on the data shown in Fig. 2 Sandia's 4/3-μm technology is not "robust" enough to meet the 3-mA specification at 500-krad. Figure 2 shows a measurable population of ΔV_{ot} shifts greater than -1.5 V (i.e., absolute magnitude of shift larger than 1.5 V). This exercise illustrates an experimental approach that can be taken to demonstrate a test structure-to-IC correlation for strategic applications. In similar experiments on 4/3-μm parts, correlations have been demonstrated between ΔV_{it} shifts and increases in circuit timing [7]. These correlations helped form the technical basis for "rebound" tests that are presently recommended for space qualification of ICs [4]. Despite these early demonstrations that correlations can be established, considerably more work needs to be performed to (1) provide a sound technical basis for the correlations and (2) demonstrate them for more advanced technologies, including SOI. One important task on the QML roadmap will be the development of physical, predictive models that can be used by designers to relate test structure measurements to IC parametric/functional response in different radiation environments.

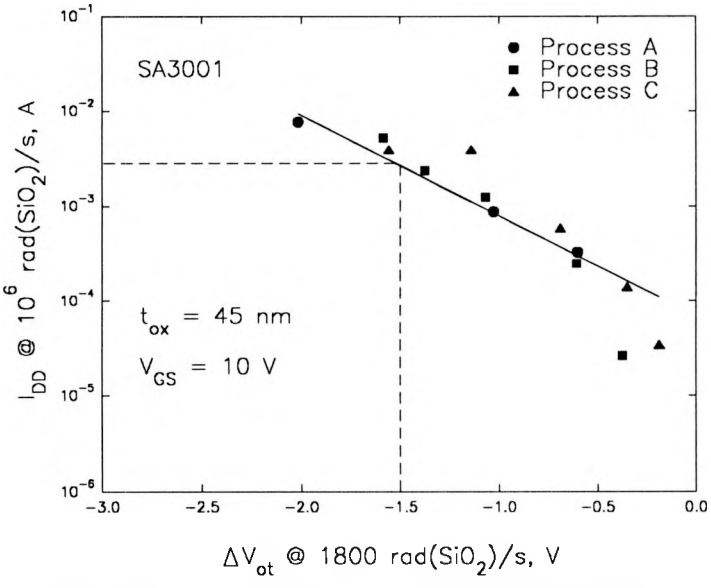

Figure 5. Correlation between ΔV_{ot} measured on n-channel transistors following 10-keV x-ray irradiation at 1800 rad(SiO_2)/s and I_{DD} measured on 2k SRAMs at 10^6 rad(SiO_2)/s.

Although the data shown here was largely taken on transistors from fully processed test die, the data could just as easily have been taken from capacitors pulled at various stages of the process [8]. The use of capacitors as in-process "radiation-hardness" monitors provides the opportunity to monitor the effect, and control the variability, of individual process steps on radiation hardness. After the correlation of key process steps with the radiation hardness of final product is established, their (i.e., the process steps) control assures that process capability will translate into radiation hardness. Consistent with QML methodology, this provides the most cost effective manner of assuring radiation hardness by proper control of the manufacturing sequence. "SPC for radiation hardness assurance" is simply controlling process steps that are known to affect the radiation hardness of the product. Over the years, many process variables which have an important effect on the total-dose radiation hardness of CMOS circuits have been identified [9]. Some examples of process steps important to total-dose hardness include: gate-oxide thickness and growth conditions [8,10,11], high temperature anneals containing hydrogen [8,12], and radiative processing including e-beam metalization [13]. In a similar fashion, process steps important for transient and single-event upset (SEU) immunity can be defined. An example of a process step important to CMOS transient immunity is the thickness of the epitaxial layer on which the circuit is fabricated, while for SEU an appropriate process might be the doping of the high-resistance polysilicon feedback resistor.

In the final paper, representative approaches to test structure-to-IC correlation will be demonstrated for transient and SEU immunity, as well as total-dose radiation hardness. In addition, specific needs for simulators and improved radiation models required for QML implementation will be identified.

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