SLAC-PUB-2652
November 1980
(E/I)

CONF-801103--50

STATUS OF THE FASTBUS STANDARD DATA BUS*

R. S. Larsen†
Stanford Linear Accelerator Center
Stanford University, Stanford, California 94305

Abstract

FASTBUS is a new laboratory standard data bus intended for use in experimental data acquisition and control. The development of FASTBUS began with a feasibility study in 1976 and is presently at the development prototyping stage. The principal aims of the standard are to provide a factor of ten or more improvement in speed of data transfers over present systems, as well as to provide an architecture for systems containing multiple processors. Developmental prototypes now in progress include crates, backplanes, cooling devices, power supplies, test and diagnostic modules, and user modules. A sizeable software development effort is also underway. Several experiments have made commitments to use FASTBUS. A review of current work and potential applications is given.

Introduction

The year 1976 marked the beginning of an inter-laboratory collaboration among high energy physics laboratories to develop a next generation high speed standard data bus. The primary motivation was to prepare for large, future systems where multiple, parallel processors would become commonplace. Since an appraisal of existing systems, including experience with new multiprocessing systems, indicated that the current broadly used standard (CAMAC) had certain architectural restrictions which would become increasingly difficult to circumvent, it was therefore decided to launch a new design. The early history and developments have been reviewed at previous Symposia (Refs. 1, 2, 3) and the goal of this paper is to provide an update.

The FASTBUS development work is being conducted by somewhat loosely coupled groups from several major laboratories and universities, chiefly Fermilab, SLAC, Brookhaven, LASL, LBL, and University of Illinois. There are in addition many collaborators involved from other laboratories and universities, including several European labs, chiefly CERN. The various contributions of some of these labs will be mentioned in the body of this report, although the individual contributions are far too numerous to list. Suffice to say that FASTBUS continues to rely on a combination of formally supported projects and informal contributions from many interested designers and potential users.

Design Goals

The general design goals have been outlined in the previous references and will be only briefly reviewed here. The major design goal is increased speed, or bandwidth. A second major goal is a multiprocessor architecture. A third main goal is flexibility. The main goals, and a host of secondary goals, are being pursued within the overall constraint of achieving a practical, cost-effective system. Some particular implications of the goals and practical constraints will be noted in the further discussion. The basics of FASTBUS can be illustrated with the aid of Fig. 1.

Here is illustrated a system with two crates with backplanes, called segments, or crate segments. The crate itself can function as a stand-alone with a single master and, typically, multiple slaves. Such single crate systems are common in CAMAC as well as other implementations. However, consider the system shown, where each segment can have one or more masters, and each master may be required to read from or write to a master or a slave on the other segment. This is a basic illustration of a generalized multiprocessor system, in which masters may communicate with different parts of the system on demand, within a preassigned priority structure.

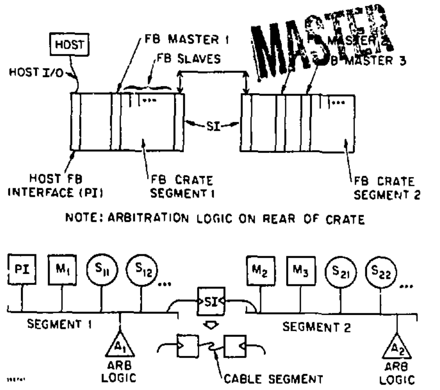

Fig. 1. Basic FASTBUS System.

In Fig. 1, all masters, including the host processor, are given a priority. If master M1 wishes to communicate with slave S12, it first must request (arbitrate for) use of its local segment. Each segment contains arbitration logic which interprets the pending requests and assigns (grants) the bus to the highest priority master. Having achieved mastership of segment 1, M1 must now request via the segment interconnect (SI) mastership of segment 2. To do this, the SI temporarily masquerades as processor M1, accepting its request on one side (its "near side") and translating it into a request for mastership on the other segment (its "far side"). In this case, the SI itself may be assigned a priority vector (local vector) which it passes to segment 2 (and thus would represent all devices on segment *1 with the same priority) and arbitrates for segment 2.* In this event, M1 is put into a wait state while the arbitration takes place. If successful, M1 is given mastership also of segment 2, and can then proceed to address S12 in a normal manner, and eventually complete the transaction.

It should be noted that a variation of the priority arbitration as outlined is possible, namely that a sufficiently high priority master could be assigned a system priority vector, which the SI would pass, which would preempt all other vectors competing for segment 2 with the exception of a higher priority system vector. In this event M1 would in all probability achieve mastership of segment 2 as soon as any current local transaction is completed.

In any event, this generalized mechanism for inter-segment communication is essential to the system, and it is the design of this mechanism together with the attendant control and address logic, and system software,

* Work supported by the Department of Energy, contract DE-AC03-76SF00515.
† Chairman, Fast System Design Group (FSDG).

(Invited paper presented at the 1980 Nuclear Science and Nuclear Power System Symposium, Orlando, Florida, November 5-7, 1980.)

on which the FASTBUS development group has concentrated most of its energies.

Obviously, in a large system the picture of Fig. 1 becomes more complex in terms of the members of autonomous segments which can co-exist, as well as system management of the data paths. Although in practical high energy physics systems, for various reasons, these problems often reduce to simple sub-sets, it is nonetheless necessary at this stage of the FASTBUS development not only to analyze the more general problem but also to provide a demonstration proof in the form of a working multi-segment prototype illustrating a reasonably full set of the potential FASTBUS protocols.

A more general system topology is given in Fig. 2.

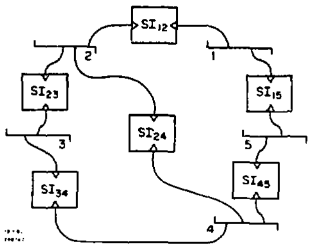

Fig. 2. Generalized Topology.

Here, each segment and SI is given an appropriate label, the SI's shown being full duplex (bidirectional) SI's. In the case shown, there are multiple paths to some segments, which means that some rules must be adopted to eliminate message conflicts due to the multiple physical paths. The general solution is to control message paths by means of a <u>route map</u> stored at each port of each SI, and by prior specification of preferred routes in the system data base. Such a route map is simply a range of addresses allowed to pass by that particular port, which in principle can be programmed via a RAM address or via a more restrictive method such as switches or hard-wire patches. If dynamic reconfiguration is desired, a RAM is needed.

During system initialization, each segment is assigned a unique range of logical addresses, consistent with the address range requirements of the devices to be placed on each segment. Then segment ranges are calculated and route maps generated, and preferred routes established to eliminate potential conflicts due to multiple paths. Further comments on this procedure will be discussed in a companion paper at this conference (Ref. 4).

The remainder of this paper constitutes a progress report on the development of various aspects of the FASTBUS standard.

General Developments

FASTBUS Specification

The most important single task in 1980 has been the development of a complete specification for the standard In July, 1980, after many arduous sessions, an interim 175 page specification was issued, followed in October, 1980 by an edited version with minor technical modifications[1]. Most of the actual writing was performed by an editorial sub-group of the Fast System Design Group (FSDG). This specification is to serve as a working document which can be used to test prototypes during the coming year. The objective is then to incorporate any necessary corrections or modifications within a final specification to be issued in about one year. The interim specification has been issued to all members of the general committee (FSDG) as well as to NIM/CAMAC manufacturers.

The Interim Specification (July 1980, updated September 1980) contains a number of changes from the earlier draft. The most significant of these are the elimination of the so-called T-Bus (32 lines) and subsequent connection of the TP-pins, used for Sparse Data recognition and similar uses, to the AD lines. At the same time, geographic addressing (coded pins at each card slot) was added. Other changes included reordering of the AD lines, addition of two 'Daisy-Chain" lines, DL and DR, and reservation of several lines for special protocols in use at BNL during the prototyping period. Some other fairly minor changes and corrections were made; a complete list of these can be found in the errata sheet[2].

Crates and Backplanes

There are two types of prototype crates being developed, which differ mechanically in order to accommodate different cooling schemes. Figure 3 shows a prototype air-cooled crate (Type A). The main design goals are to provide an open structure for free vertical air flow from a blower or rack air handling system. The backplane (Fig. 4), which includes all power planes, is a staked-pin multilayer "sandwich" using a 130 pin 100 mil 2 row segment connector and a 132-pin 100 mi 3 row auxiliary connector. The FASTBUS segment connector used on the air-cooled design (Fig. 5) is available from 5 manufacturers[3].

An initial order of 50 crate assemblies has been received from the manufacturer[4]. The corresponding backplane order is approximately 25% complete[5]. The plastic parts for the backplane card guides are complete[6]. These units are scheduled for delivery to approximately 13 different laboratories and universities for evaluation and prototype work. A few spare units will be available.

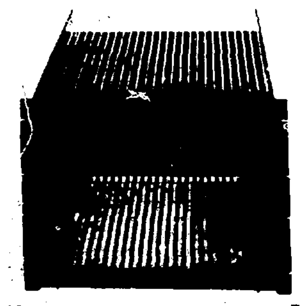

Fig. 3. Prototype Crate - Type A.

[1] FASTBUS Draft Specification, September 1980, available from L. Costrell, Department of Commerce, National Bureau of Standards, Washington, DC 20234.

[2] Memo, L. Costrell, "Tentative FASTBUS Specification, July 1980," September 29, 1980.

[3] Amp, Berg, ITT Cannon, Elco, Philips, Bendix.

[4] Nuclear Specialties, San Leandro, California.

[5] Elfab Corp., Dallas, Texas.

[6] Baumbach Engineering, Mountain View, California.

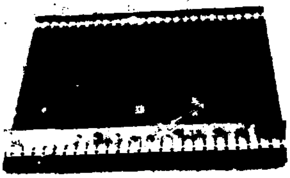

Fig. 4. Prototype Crate Backplane - Type A.

Fig. 5. Segment Connector - Type A.

Figure 6 shows a prototype water-cooled crate (Type W). This unit consists of a water-cooled top and bottom plate with which a vertical "cold plate" holding the module makes thermal contact. The main design objective is to eliminate the need for air movers and their attendant space requirements, noise, and filters. This is achieved with some additional mechanical complexity of the crate itself in terms of thermal contact mechanisms.

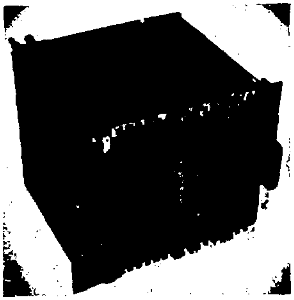

Fig. 6. Prototype Water-Cooled Crate - Type W.

The backplane for this prototype crate differs from the aforementioned model in that it has 20 connector positions (compared with 26) and utilizes a different connector[7]. However, in terms of rack utilization, the water-cooled unit will require less vertical space.

Two of the water-cooled crates have been built[8], and one is operating in an experiment at Brookhaven. Complete details are given in two companion papers in this Conference (Refs. 5, 6).

Note that it is the current goal of the FSDG to achieve a module design which is compatible with either type of system. At the moment, the circuit cards (Type A and Type W) are dimensionally equivalent, differing only in the connector arrangement. However, the conduction cooling mechanisms place dimensional restrictions on component height such that while a Type W may be able to function in an air-cooled environment, the converse may not be possible. The Mechanics Working Group (MWG) is studying this matter.

Modules

Basic module hardware has been developed. For the air-cooled unit, a typical kluge-card module is shown in Fig. 7. The particular kluge card shown was designed at FNAL and is available commercially[9] in both ECL and TTL versions. The card contains artwork for the basic interface to FASTBUS. Figure 7 shows a memory module (PRIMO).

A typical Type W module is shown in Fig. 8. This hardware is also available commercially[10].

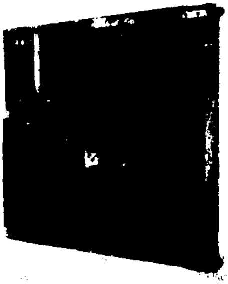

Fig. 7. Kluge Card Module - Type A.

Ancillary Logic and Terminations

Ancillary logic is that logic residing on FASTBUS which performs the arbitration control function, as well as miscellaneous controls such as HALT/RUN (actuated by a crate switch). So as not to consume a crate slot, this logic is mounted on the rear of the staked-pin backplane. Similarly, small termination cards for each end of the bus are placed on the backplane. The nominal impedance of the bus is 100Ω. Design and fabrication of two Ancillary Logic prototypes is complete; testing is in progress. Several terminator cards have been completed.

Prototype Test Program

In order to completely test the specification, a prototype test program has been designed which has two major goals:

(1) To test the various critical sub-components such as crates, backplanes, masters, slaves, ancillary logic, and segment interconnects.

---

7 Bendix.
8 Manufacturer: Industrial Fabricators, Stratford, CT.
9 Vern Kiebler Associates, Wheaton, Illinois.
10 Industrial Fabricators, Stratford, CT.

Fig. 8. Type W Module.

(2) To demonstrate both hardware and software capable of supporting a multi-segment, multi-processing system.

A secondary but equally important goal of the prototype effort is to demonstrate the applicability of FASTBUS to actual physics data acquisition systems and sub-systems.

The initial configuration chosen for the test system (Test Phase I) is shown in Fig. 9. The objective of this system is to allow programming of sequences into test modules which will run at or near maximum speed. The required modules are a master (Sequencer), slave (Memory), load modules ("Dummy's"), an interface to a computer (PI), and a diagnostic module (Snoop). The second configuration (Test Phase 2) is the same as already shown in Fig. 1, where the segment interconnect is used between crate segments.

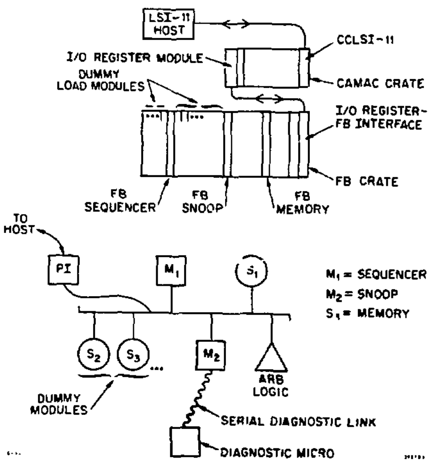

Fig. 9. Prototype Test System.

Prototype Demonstration System Status and Results

The following is a brief summary of the prototype demonstration system and test results.

Crate Backplane

Transmission tests have been performed on a staked-pin backplane which has every position loaded 4 lines at a time, as well as with a partially loaded backplane. In these tests, terminations at each end of 100Ω to -2V were used. Some of the results are summarized in Figs. 10(a) through 10(c).

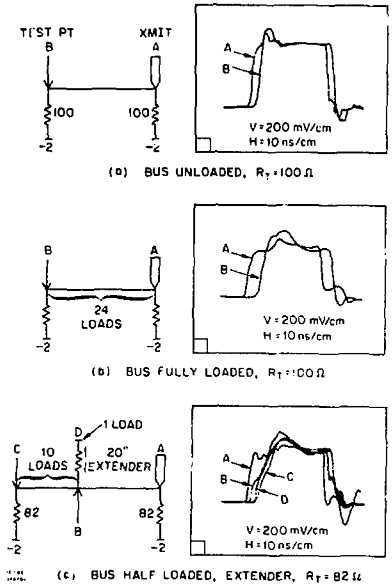

Fig. 10. Backplane Waveforms.

Backplane Power Tests

A test using Dummy load modules, with a load of 11A per module position wired into the -5V pins in each card slot, was performed in order to test (a) backplane voltage drops at high current; and (b) performance of the distributed power pin arrangement in the staked-pin backplane. In this test, voltage drops were measured through backplane power studs and individual pins. The results were as follows:

Number of cards = 25

Total I = 290A @ -5.2V

Total P = 1500W

I/card = 11.6A

I/pin = 1.6A

ΔV_1 (Stud-backplane) = 12 mV max

ΔV_2 (pin-pin on backplane) = ±2 mV max

ΔV_3 (stud-module powerplane) = 24 mV typ.

Note that in actual operation, regulation of each supply will be sensed at one of the backplane connections, and equal length leads must be maintained to assure relatively equal sharing of currents throughout the connected system.

Fast Memory Module

The memory module is configured as a 32 bit by 256 word data memory using the fastest available ECL memories (Fujitsu MB7071H). The module allows all FB slave functions, such as random read-write, block transfer, extended addressing, broadcast, parity generation, etc. The prototype wire-wrap module is operational and has been tested both with a manual tester; tests are being set up using a programmed I/O channel (LSI-11 via CAMAC) over the FASTBUS. Slow-speed tests will be performed with a partially and fully loaded backplane. Maximum speed tests will be made upon completion of the Fast Sequencer.

Dummy Module

The Dummy Modules serve both as bus loads, simulating a Sparse Data Scan module, as well as maximum power and heat loads as described above. The modules contain a simple interface and front-end read/write register. Twenty-six of the units have been fully tested and are being used in a test setup.

I/O Register to FB Interface

The so-called "simple" interface, initially designed and constructed in wire-wrap at LASL, has been extended and the new version is being constructed on a 4-layer printed board. Logic design and pc layout are complete and two units are in fabrication. The unit is designed for reading and writing to FASTBUS via a standard CAMAC I/O module, or other I/O source, under program control. Once loaded, the interface executes standard FASTBUS cycles (single reads and writes, broadcasts, extended addressing). It also contains the standard arbitration logic and a loadable FB address register such that two such devices can accomplish the basic function of an SI. Similarly, two interfaces from two different hosts can perform the multiple master function, although much more slowly than FB maximum speeds.

Fast Sequencer

The Fast Sequencer has both master and slave logic to perform most FB functions. The Fast Sequencer is the vital component needed to execute FB cycles at the fastest possible speeds (within the current limitations of wire-wrap board construction). The module contains a 32 bit, 512 word data memory and a 32 bit, 256 word control memory. (Note that both the memory and sequencer units have all the features needed for fully general purpose operation. Later, expanded printed circuit versions will be designed and built.) The Sequencer is completely designed in its initial configuration, and construction has started. Anticipated completion data of the first unit is late November, 1980.

Snoop

The Snoop is a powerful diagnostic module which is considered to be essential for trouble-shooting on-line in large systems. The unit is described in detail in a companion paper in this conference (Ref. 7). It consists of a very high speed front-end "silo" built as a 100K series ECL FIFO; this section has control logic which can be programmed to insert WAIT cycles into normal FASTBUS operations taking place on the bus. Using its silo, it can store up to 256 words of the most recent activity on all bus data and control lines. The Snoop contains basic master logic to execute simple FB commands, as well as a microprocessor (M68000) together with communication ports for the FB Serial Diagnostic bus.

The Snoop has been completely designed with the exception of some final details of the uP section. Because of its high density and performance, the high speed front-end has been designed immediately onto a 4-layer pc board. Anticipated completion of fabrication of the first unit is December, 1980.

Segment Interconnect (SI)

The primary design goals of the SI are to achieve a fully programmable, full capability unit containing both master and slave logic, programmable address registers and route-map RAM, etc., in order to demonstrate the most powerful architectural configuration and operational features of FASTBUS. Once demonstrated, this SI will serve as a general purpose tool for multi-segment, multiprocessing systems; however, simpler implementations (e.g., simpler or more restrictive address range setting schemes) can be visualized for less general systems.

A secondary design goal is to package the SI on a single-width FASTBUS module. The interconnecting cable is designed as a standard cable segment (single-ended, and therefore restricted in length); this will allow easy extension to tests of several segments.

The SI logical design is essentially complete and initial layout of a 4-layer pc has begun. Anticipated completion of fabrication of the first unit is late January, 1981. After debugging, two SI's will be built and tested as part of an intersegment link involving at least two independent masters (sequencers) capable of operation at or near maximum FASTBUS speeds. (See Fig. 1.)

Test System Software

Software for driving the CAMAC interface from a FORTH system on an LSI-11 microcomputer has been developed and the basic load and test routines are operational. Fully general system software for supporting initialization and route map generation is under development and near completion; as mentioned earlier, this will be described in Ref. 4. (Also see Ref. 10.) Actual multi-segment tests using two crates and SI modules is anticipated sometime in late Spring of 1981.

Prototype Test System Summary

Several of the critical components in FASTBUS have been tested and have performed to specifications. Full speed tests of a single segment are imminent. Shortly thereafter, the first SI's should be available to complete the multi-segment, multi-processor demonstration program. The current goal is to complete the basic Phase I demonstration by March, 1981; and to have Phase II operational by June, 1981.

Experimental Demonstration System

A second important and complementary aspect of the FB prototype effort is the design and implementation of a single-crate (single segment) experimental system at BNL; details are given in the two companion papers cited earlier (Refs. 5 and 6) as well as Ref. 8. Briefly, this system consists of the following components:

- Conduction-cooled crate and module hardware
- Unibus-to-FASTBUS fully bidirectional interface with DMA

-- FASTBUS programmable sequencer for data handling

-- Data Memory Module

-- Fast Coincidence-latch modules

-- Scaler Modules

-- Interrupt Module.

Most of the modules are constructed using wire-wrap technology, but several are pc, including one designed by a commercial supplier[11]. All are conduction cooled. The system has taken data in an on-line experiment and is being expanded for further experiments. Performance has been to specifications; details are provided in the references.

It should be noted that the design of this equipment started before the FB protocol was completely finalized and the protocol used is somewhat different from the current standard. However, the major significance of the development is that the basic bus architecture, speed, multiple master operation, and a number of the protocol features have been demonstrated in a single segment system. Moreover, a variety of practical, experimental data handling modules have been constructed in FASTBUS format and the modular hardware and architecture appear to be well adapted to the high density, high-speed circuitry typical of the newest generation of high energy physics experiments.

Other Significant Developments

A number of other developments are noteworthy. These are briefly summarized as follows:

Unibus-Processor Interface (UPI)

It has been obvious from the beginning of the FASTBUS development that the most important processor interface required is for the DEC Unibus. A major project at FNAL is the hardware and software design of a powerful Unibus Interface. This device is the subject of another companion paper at this conference (Ref. 9). Briefly, the interface consists of four sections: A Unibus-FB window, a FB-Unibus window, a programmable interface including a fast list processor, and an interrupt handler. A complete specification[12] for this unit has been written and detailed hardware and software design is under way. The goal is to construct a first prototype by the end of March, 1981. Operational tests using the aforementioned demonstration hardware and software will commence shortly thereafter.

Q-Bus Interface

An interface for the DEC Q-Bus has been designed and is being used for system development at FNAL. This is part of a large detector[13] development program which will encompass many front-end modules and very fast, distributed preprocessors. This program is in the feasibility study and preliminary design phase.

Drift Chamber Digitzer System

BNL[14] is developing several FASTBUS modules for readout of high density, high resolution drift chamber systems utilizing a custom IC high speed shift-register front end. The FASTBUS system will provide control, data gathering, and preprocessing capabilities. Several prototype modules are in checkout.

[11] Joerger, Inc. (32 bit 8/16 ch. scaler).

[12] Fast System Design Group Note FSDG-084, available from R. S. Larsen, SLAC or E. Barsotti, FNAL.

[13] Colliding Detector Facility (CDF).

[14] E. Platner, Private Communication.

Power Supplies

There are four separate power supply developments under way:

(a) BNL has been developing an on-board regulator scheme utilizing a bulk supply as a primary source. (The experimental prototype modules mentioned earlier are currently using external dc power.)

(b) A commercial manufacturer[15] has developed a prototype bulk supply capable of 2 KW (-5.2 @ 300A, -2 @ 100A, and +5 @ 100A). Further development of this custom unit has been superseded by a new unit which will use a line of standard, high current modules. The manufacturer will provide 2 basic units, but custom units built around the existing mainframe hardware will also be possible. The 2 units currently being developed are:

Model	+5	-5.2	-2	+15	-15
5XS6030	200	200	60	24	16
3XS6031	200	200	60	--	--

Note that the above models use a standard product line of independent modules, and a large variety of different current and voltage units are available. The basic package will be a 5½" high, 24" deep rack mounting chassis.

(c) A packaging effort similar to (b) is underway at SLAC using another manufacturer's modules[16]. These units differ in detail from the above and the objective is simply to offer an alternative source for a standard (or group of standard) supplies. The present unit has the following modules:

+5 @ 220A (AMQ5 - 220)

-5.2 @ 220A (AMQ5 - 220)

-2 @ 45A (AMS2 - 45) .

In addition, space is available for a small amount of ±15V power in a 24" deep chassis. Obviously, a large range of variations are possible. The manufacturer will offer the unit as a package. Both (b) and (c) are packaged in a 24" deep, 5½" height rack mounting chassis. The basic chassis contains a front panel main breaker, ac power indicator, and readout DVM. The rear panel contains the power output studs and two connectors, one for control (e.g., inhibit, margining) and remote monitoring; the other for sense lead outputs. Both units normally operate on 220 VAC.

(d) A development at FNAL[17] is aimed at a modular card power supply system for single (Type A) crate operation. The objective is to combine the supply with the Type A crate and air handler in a compact, self-contained package. Again, a variety of power module cards will allow tailoring of the supply to the intended application, in a similar manner to (b) and (c) above. Power module cards are in the prototype stage. The current program is to determine the feasibility of making the system available from a commercial supplier.

FASTBUS Master Controllers

A project which is in a preliminary design phase is a general purpose master controller using one of the new 16 bit processor chips. The M68000 is the current favorite candidate primarily because of architectural and software considerations; however, other devices are also under consideration.

[15] Todd Engineering, Brentwood, L. I., N. Y.

[16] Acme Electric Corp., Cuba, New York.

[17] T. Droege, Private Communication.

The more specialized subject of high speed bit-slice processors in FASTBUS has also been discussed but no firm decisions have been made. BNL[18] is committed to such a development project in the form of a preprocessor to be used as a programmable filter for physics data pattern recognition. Their goal is to produce a unit with 1/5 to 1/10 the throughput of a 7600 for prefiltering applications.

Another project under discussion is that of a special FB processor, using ECL-LSI, and FORTH as an operating system language. A feasibility study, and discussion with a potential commercial supplier, are under way.

Custom FASTBUS Protocol Chips

Discussions have been held with the vendor concerning a preliminary design of the FB interface using Motorola Gate Array chips. A chip set of 2-3 types would reduce the total interface to about one-quarter of the current chip count. The ECL drivers and receivers, for example, could be packaged as 8 complete transceivers per 4-sided 64-pin package, and 4 such chips would handle the 32 FB address/data lines. Two other chips would handle arbitration and basic master/slave control functions. Evaluation and projected costs are being analyzed.

Miscellaneous

A number of smaller efforts are in various stages of completion. These include a backplane tester, kluge card, test boxes, displays, etc. Completed documentation, when available, can be obtained by contacting the author.

Vendor Support for FASTBUS Components

From the previous description, it is obvious that some vendor support for a number of items has already been developed. However, much more needs to be done before FASTBUS can be widely used.

Over the next year it is estimated that a major effort will be made to persuade manufacturers to evaluate some of the basic FASTBUS hardware. Obviously, major production cannot proceed until the specification is finalized (i.e., about one year from now).

A number of prototype modules now under development are likely candidates for early vendor support. It is proposed to write specifications and place purchase orders in order to expedite this process. Obviously, the specification must remain firm, essentially as presently written, or with very minor modifications, in order to initiate this type of activity.

Manufacturers are being encouraged to evaluate their current CAMAC product lines as candidates for FASTBUS. If distributed processing continues its current trend, the high performance of FASTBUS will make it an attractive standard for all types of physics data acquisition modules. In many cases, it should also be very attractive for modules involved in control applications, especially where these coincide with experimental needs.

Projected FASTBUS Costs

Costs must be somewhat speculative at this time because accurate comparisons are difficult due to the developmental state of the system. In the final analysis, it is the competitive manufacturing community which will establish the "real" costs of system components or sub-systems; and the laboratory systems engineers who will determine total system costs by a consideration of the various tradeoffs in implementing any large system.

However, it is of interest to make at least a rough comparison of what shall be called the "FASTBUS Interface Overhead" versus the "CAMAC Interface Overhead". To do this, it shall be assumed that a CAMAC crate, power supply and crate controller (resulting in X square inches of CAMAC user board area) can be compared with a FASTBUS crate, power supply and Segment Interconnect (resulting in Y square inches of FASTBUS user board area); costs can then be normalized as $/sq. in. of available user board area.

The following represent some fairly well-established numbers for CAMAC and some less well established numbers for FASTBUS:

Interface Cost Estimates

	Item	FASTBUS	CAMAC
a.	Crate & Backplane ÷ No. Slots	$ 40	$ 32
b.	Power for Interface @ $1/watt	30	10
c.	Chips & Other Parts for "full" M-S Interface (80 vs 35)	175	35
d.	Board (4-layer)	130	65
e.	Loading (interface only)	25	10
f.	$SI ÷ 25 or $CC ÷ 23	80	33
	Totals	$480	$185

The result is a FASTBUS board which supports a maximum of approximately 250 chips, and a CAMAC board which supports a maximum of about 100 chips (189 sq. in. vs 74 sq. in., assuming 0.75 in^2 per chip). Subtracting the interface chip counts of 80 and 35 respectively gives:

	Available Board Area (No. Chips)	Cost/Chip Area
FASTBUS	170	$480/170 = $2.82
CAMAC	65	$185/65 = $2.85

This result is obviously close. However, some additional factors should be considered: First of all, the FASTBUS calculation contains a full 32-bit interface compared with 24-bits for CAMAC, so the comparable costs of FASTBUS are 25% less than the above. Secondly, we have not placed any value on the fact that the usable bandwidth of the FASTBUS interface is at least 10 times greater than CAMAC. Thus if one is truly utilizing the bandwidth, the cost per functional area multiplied by bandwidth would be a truer comparison, and FASTBUS wins by an order of magnitude. If special protocol chips become available, FASTBUS costs will be reduced further.

The above assumes full utilization of available board space, and also provides a crude measure of the cost of not utilizing the full board. High density packaging is clearly called for.

Conclusion

The total FASTBUS program has made significant strides in the past year. The specification is close to finalization. Prototype efforts so far indicate that the basic designs are meeting all major goals, and that FASTBUS will provide the adaptability, functionality, and cost effectiveness desired in the new standard. In the coming year, in addition to completing the prototype demonstration program, a major effort will be made to begin to develop vendor support for the FASTBUS standard.

Contact Persons

The following are contacts for available documentation at their respective laboratories:

[18] E. Platner, Private Communication.

National Bureau of Standards	L. Costrell
Stanford Linear Accelerator Center	R. S. Larsen
Fermi National Accelerator Laboratory	E. Barsotti
Brookhaven National Laboratory	W. Sims
Los Alamos Scientific Laboratory	D. Machen
CERN, Geneva, Switzerland	H. Verweij

Acknowledgement

The FASTBUS program has received support from a large contingent of dedicated people from essentially all the major laboratories. Several of the chief contributors to the prototype program deserve special mention: R. Downing of University of Illinois; L. Paffrath, H. Walz, D. Horelick and B. Bertolucci of Stanford Linear Accelerator Center; D. Gustavson and the software team at SLAC (S. Deiss, T. Holmes, J. Steffani and C. Logg); E. Barsotti, M. Larwill, K. Turner and T. Droege of FNAL; R. Brown and the University of Illinois software contingent; the Leipuner and Platner groups at BNL; and D. Machen, K. Dawson and D. Ethridge at LASL. In addition, many others have contributed at the various laboratories, and we especially acknowledge the useful interaction and contributions of the CERN contingent, in particular P. Ponting, E. M. Rimmer and H. Verweij. Finally, the work of the chief editor of the Draft Specification, L. Costrell, and the members of the Draft Specification editorial group, are recognized.

References

1. B. Wadsworth, "A System Overview of FASTBUS," IEEE Trans. Nucl. Sci. NS-27, No. 1 (1980), pp. 612-621.
2. R. S. Larsen, "Status of the Interlaboratory Development of a High Speed Standard Data Bus - FASTBUS," IEEE Trans. Nucl. Sci. NS-26, No. 1 (1979), pp. 679-685.
3. R. S. Larsen, "FASTBUS - Status of Development of a Standard High Speed Data Bus for High Energy Physics," IEEE Trans. Nucl. Sci. NS-25, No. 1 (1978), pp. 735-739.
4. D. B. Gustavson, "FASTBUS Software Status," paper presented at this Symposium.
5. L. Leipuner et al., "A FASTBUS System Used in a High Energy Experiment," paper presented at this Symposium.
6. W. Sims et al., "Conduction Cooling: Multicrate FASTBUS Hardware," paper presented at the Symposium.
7. R. Downing and H. Walz, "FASTBUS Snoop Diagnostic Module," paper presented at this Symposium.
8. M. Campbell et al., "High Speed Processor for FASTBUS," paper presented at this Symposium.
9. M. Larwill et al., "A UNIBUS Processor Interface for a FASTBUS Data Acquisition System," paper presented at this Symposium.
10. D. B. Gustavson et al., "A 'Front Panel' Human Interface for FASTBUS," paper published in this Symposium.