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PHASE 2, AUTOMATED ARRAY ASSEMBLY, TASK IV LOW COST SILICON SOLAR ARRAY PROJECT

Quarterly Report No. 1

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January 1978

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Lockheed Missiles & Space Company, Incorporated
Sunnyvale, California

U.S. Department of Energy

Solar Energy

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QUARTERLY REPORT NO. 1

January 1978

Prepared by

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The JPL Low-Cost Silicon Solar Array Project is sponsored by the U. S. Department of Energy and forms part of the Solar Photovoltaic Conversion Program to initiate a major effort toward the development of low-cost solar arrays. This work was performed for the Jet Propulsion Laboratory California Institute of Technology by agreement between NASA and DoE.

FOREWORD

The results described herein represent the initial work performed from November 1, 1977 to January 27, 1978 by the Manufacturing Research Organization of Lockheed Missiles & Space Company, Inc., in Sunnyvale, California. The project team, headed by Mike Lopez, is staffed with the following key personnel:

> Dean Housholder, Semiconductor and Device Technology
> Jerry Katzeff, Laser Technology (Annealing)
> Bob Casey, Automation Processes
> Harold Weinstein, R&D Staff, Photovoltaic Devices, International Rectifier Corporation

Other principal contributors include John Knudson, Ion Implantation; and Cheryl Bostwick, Screen Printing of Contacts.

The JPL Contract Technical Manager is B. D. Gallagher.

ABSTRACT

This first quarterly report on the Phase 2, Process Development Effort of the Task IV, Low Cost Silicon Solar Array Project, covers the period of November 1, 1977 through January 28, 1978. Technical and economic evaluations are discussed on the selected process sequence consisting of: starting material CZ silicon wafers, as sawn, 3 inch diameter; texture etch with N_aOH; ion implantation of phosphorus for junction formation; laser annealing; screen printing of ohmic contacts; spray-on AR coating; module assembly. Process verifications have commenced on the texturizing and ion implanting processes. Argon, Ruby and YAG lasers were determined to be best suited for laser annealing having wavelengths of .5 μm, .694 μm and 1.06 μm, respectively. Arrangements are being made to utilize appropriate lasers.

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Section 1

SUMMARY

This first quarterly report on the Phase 2, Process Development Effort on the Task IV, Low Cost Silicon Solar Array Project, covers the period of November 1, 1977 through January 28, 1978. The contract is to verify the technological readiness of a selected process sequence from the "as sawn" CZ silicon wafers to the module assembly. This verification work deals principally with the following sequence: (1) starting material of 3" diameter "as sawn" CZ silicon wafers, (2) texture etching of the surfaces using sodium hydroxide, (3) ion implanting of phosphorus for junction formation and boron for back surface field, (4) laser annealing ion implanted wafers, (5) screen printing of ohmic contacts using Ag loaded inks and Ag-Al for back surface field effects (for performance and economic comparisons with the ion implanted boron), (6) spraying of AR coating and (7) assembling fabricated cells into modules.

Literature reviews were conducted along with personal contacts of principal accomplished investigators in industry to reinforce our technology base. Particular emphasis was placed on ion implantation and laser annealing.

Technology and economic reviews were completed on texture etching, ion implanting, screen printing and module assembly as planned.

The Zicon spray-coater was installed and hooked up for power, exhaust, air and plumbing. The equipment operational aspects for the AR coating process are underway.

The texture-etch process was set up by International Rectifier in their facilities, and wafers processed using the JPL supplied procedure. Acceptable texture-etched surfaces were achieved as verified by SEM analysis.

Ion implantation of ^{31}P dopant was performed on 1:0:0 orientation, .5 ohm-cm to 7 ohm-cm, P type wafers by both LMSC and IR with acceleration voltages ranging from 50 KeV to 200 KeV and dosage levels of 1×10^{15} ions/cc. Surface activation measurements (V/I) were made on thermally annealed wafers with resulting V/I values of 10.9 to 19.

Laser annealing equipment and facilities have been reviewed. From the literature, it is apparent that YAG, Ruby and Argon lasers are the most suitable for this application. Sources have been located to accommodate our experimental work.

Section 2

INTRODUCTION

This contract is a process development effort to verify the technological readiness of a selected process sequence from the "as sawn" Czochralski grown silicon wafers to the module assembly. The contract has an effectivity date of 28 October 1977 and is of a 12 month duration.

The process to be investigated consists of the following sequence:

- Starting material: 3 inch "as sawn" CZ silicon wafers.
- Texture etch silicon wafers using sodium hydroxide.
- Form junction by ion implantation of phosphorus/boron (back surface field).
- Laser anneal ion implanted wafers.
- Screen print Ag, Ag-Al for ohmic contact and back surface field. The Ag-Al for back surface field is for cost and performance comparison with ion implanted boron.
- Spray AR coating.
- Assemble module using the LMSC module design, developed under the JPL Contract 954653, as baseline.

This selected process sequence will be evaluated for its technical potential of achieving the economic goals of the Low Cost Silicon Solar Array Project of $.50/watt for 500 megwatt/yr production by 1986.

Specific areas of investigation under this contract consist of the following:

- Performance of detailed technical and economic evaluations of the selected process sequence.

- Preparation of process steps descriptions detailing input-output requirements and characteristics, and identifying materials, supplies and equipment utilized.

- Performance of critical reviews to identify processing areas which require significant development, or proof of operation to reach the Project goals.

- Performance of process verifications of the selected sequence.

- Demonstration of the technological readiness of the selected process by fabrication of cells and assembling into a module.

Solar cells will be fabricated and evaluated for their respective efficiencies and throughput. The Samics format will be utilized in the determination of economic considerations and updated as necessary, as technology advancements are projected in the course of this contract.

International Rectifier, El Segundo, California, will work jointly with us to satisfy the various facets of the contract.

Two process steps of the specified sequence will receive greater emphasis in this contract. These are: laser annealing and sprayed AR coating. Laser annealing offers the potential of reduced energy consumption and improved efficiency at no loss in throughput over conventionally practiced techniques. Automated spray coating of anti-reflective film should improve thickness control and uniformity over large surface areas. The balance of the steps in cells processing will necessarily be performed in the production of modules. It is understood that these have been, or are being, studied in greater detail by other contractors. For these steps, processing of wafers will constitute verification of their respective technological readiness.

The module assembly work will be limited to the assembly of cells fabricated per the selected process sequence. The module configuration will be based on the work performed by LMSC for the Jet Propulsion Laboratory/California Institute of Technology under Contract No. 954653 and documented in the Final Report entitled "Transparent Superstrate Terrestrial Solar Cell Module", dated October 1977. Figure 1 shows the module configuration developed under the aforementioned contract. There are 41 three (3) inch diameter cells connected in series, as shown in the schematic, Figure 2. The copper interconnects are interconnected as shown in Figure 3. Basic materials used in this module design are:

- 3" diameter cells, silver screened contacts.
- 2 oz. copper interconnects.
- Superstrate - Sunadex glass, type B, 1/8" thick.
- Cell to glass bond - Sylgard 184.
- Back surface encapsulant - Dow Corning X1-2577.
- Aluminum frame assembly.

A cross section of the module showing these materials is shown in Figure 4.

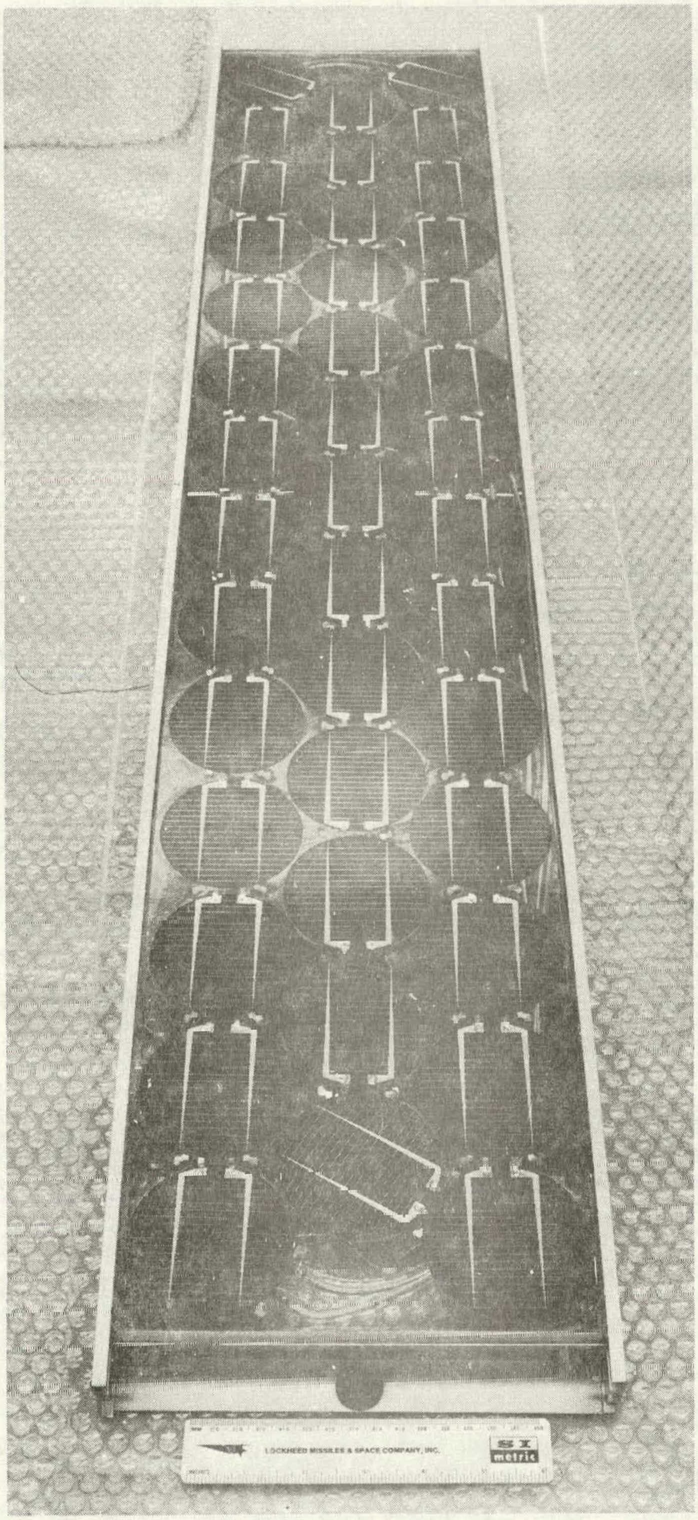
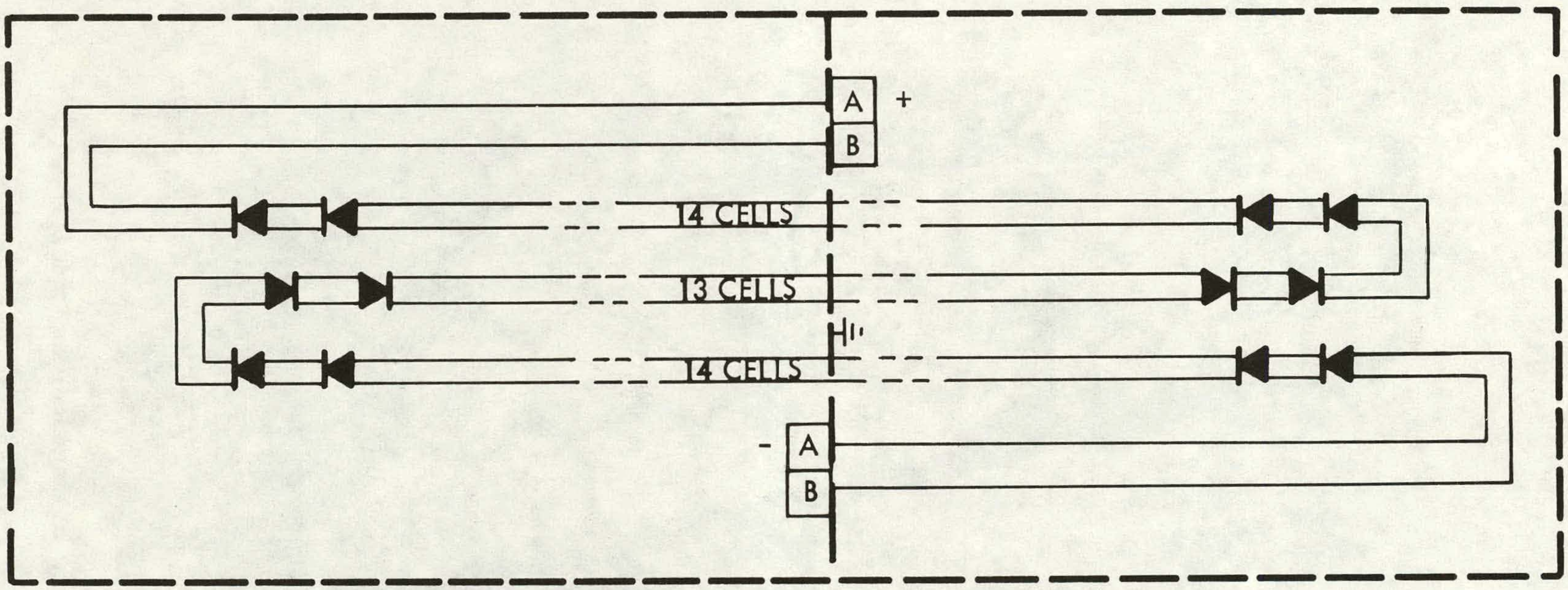


Figure 1. Engineering Module - Spectrolab Cell



(SUN SURFACE REF)

Figure 2. Module Electrical Schematic

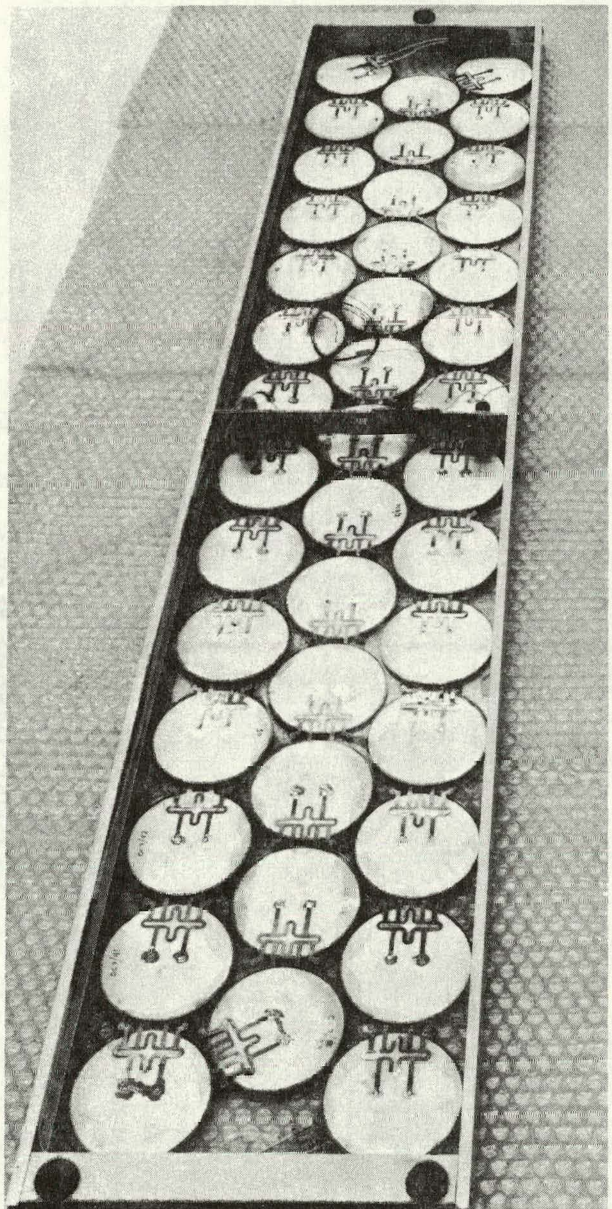


Figure 3. Rear View of Engineering Module Prior to Encapsulation

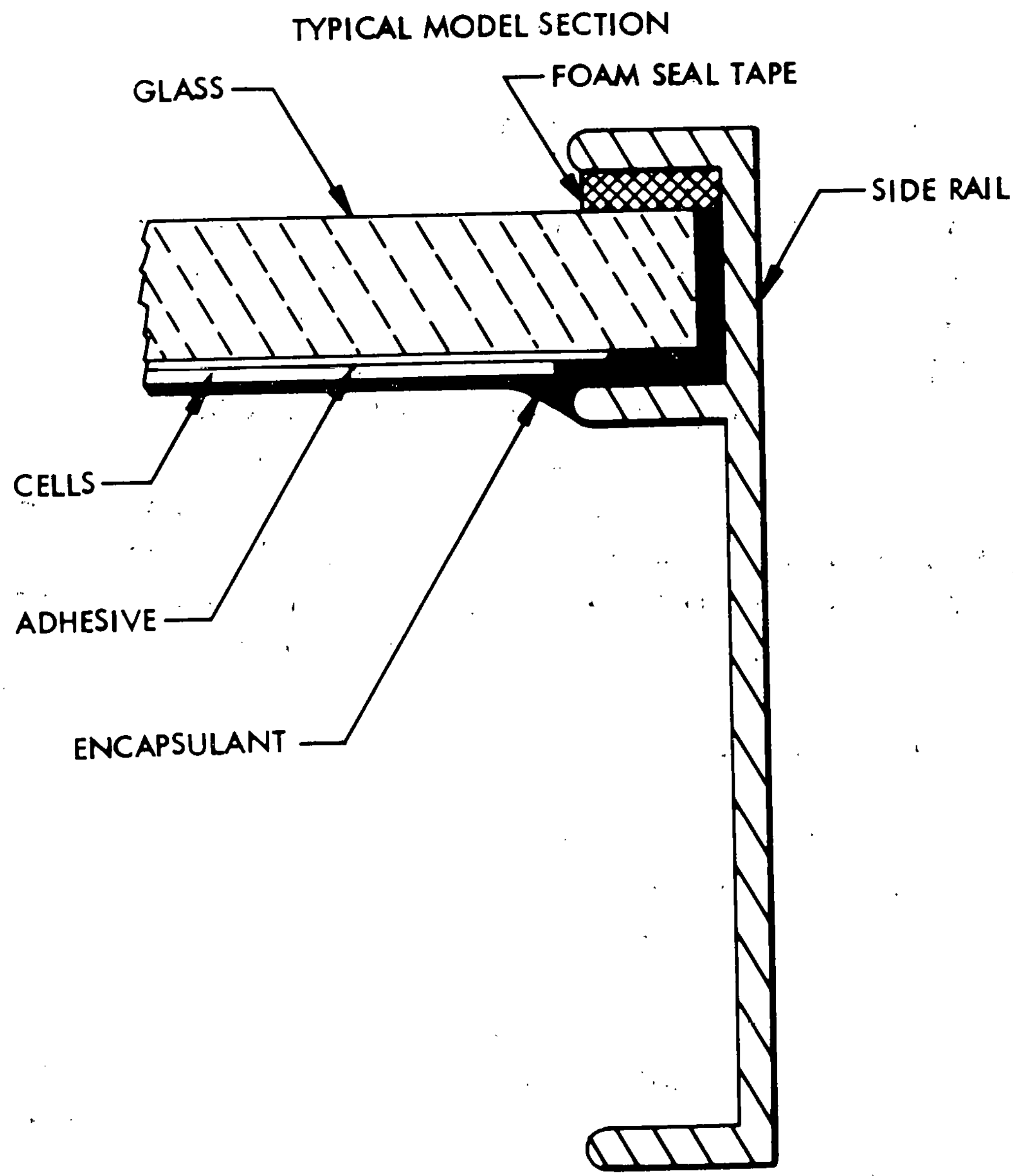


Figure 4. Typical Section Through Module Siderail

Section 3

TECHNICAL DISCUSSION

3.1 TECHNICAL AND ECONOMIC EVALUATION

The following discussion is a general evaluation of the specified process sequences. Most of the process steps have already received extensive analyses in previous work performed by the various participants on the Low Cost Silicon Solar Array Project (LSSA). This evaluation will necessarily cover some of the same ground. Laser annealing is considered state-of-the-art in terms of reduction to practice, and will receive greater emphasis during this contract. There is no module assembly verification work to be performed under this contract; however, an extensive discussion based on prior LMSC work is presented to lay the groundwork for future consideration when this phase of the project will have to be addressed.

3.1.1 Texturize Etching

Considerable work was accomplished by other contractors during Phase I of this program in evaluation of a textured surfaced solar cell. The overwhelming consensus of these investigators (and LMSC/IR as well) is that if single crystal silicon is to be used as the base solar cell material then a texturized surface should be used. Since single crystal silicon appears to be the most viable candidate for meeting the short term goals of the program, the question then resolves to a definition of the texturizing process.

The LMSC contract requires process verification of a sodium hydroxide texture etch process based on contract work done previously. (For more detail see Section 3.2.1). It is our general opinion that while this technique for texturizing represents the most cost-effective process available at present a more careful analysis of the many associated aspects should be made, i.e., prior flash etch, rinse, acid neutralize rinse, solvent rinse, chemical toxicity, chemical disposal, reclamation, etc. Anisotropic plasma etching of 1:0:0 silicon has been reported[1)] as offering several advantages over "wet" chemical etching. The most important of these is the elimination of chemicals which represents savings in both initial cost and cost of disposal/ reclamation and one side etching, saving silicon. The greatest disadvantages, as established by an "in-house" funded research and development program, are those of throughput rate and initial equipment cost. Although equipment costs are not expected to decrease, the production rate has sufficient potential for improvement to make plasma etching a future alternative to wet chemical processing. This improvement should occur in two areas. The first of these is in adaptation of the equipment to automated wafer handling and the second is in the development of new etchants to achieve improvements in both quality and cycle time.

It is our opinion that a closer scrutiny should be made, particularly for the post 1980 period, of plasma etch technology for texturized etching of solar cells.

3.1.2 Ion Implantation

As previously indicated in the process sequence described in Section 2, ion implantation has been chosen as the prime candidate for doping solar cells. The primary disadvantage currently encountered is the formation of an essentially amorphous surface layer due to impurity ion collisions with the single crystal silicon lattice during implantation. Present means for restoring crystallinity in the surface layer is by thermally annealing in a furnace at 900° to 1000°C for 15 to 45 minutes. Although this technique restores the crystal structure to an acceptable level, it also will cause excessive impurity diffusion and introduce bulk dislocation loops in the subsurface silicon due to the high temperature thermal cycling. This causes trapping centers and reduces cell efficiency. This is true to a certain degree for any doping technique requiring a thermal diffusion or redistribution of the desired impurity. It is anticipated that laser annealing (to be discussed later) will obviate this thermal cycle to the bulk silicon by heating only the surface layer, thus, leaving the bulk silicon free of further thermally induced dislocation loops. If the laser annealing proves feasible as an annealing technique, then ion implantation becomes more attractive for its many advantages.

One of the more important advantages is the more precise control of the dopant quality, quantity and doping profile, thus insuring cell uniformity, repeatability and quality. The automation potential of ion implanting is also very high, being limited by mechanical cell handling and the ability to cool cells during implant. New implanters are available from Extrion, and Lintott with 2×10^{-3}A and 4×10^{-3}A beam currents, respectively, lowering implant time per cell to seconds. Both of the above companies have 2×10^{-2}A equipment on the drawing board. A comparison of present and future implant times of 3" diameter wafers is shown in the following calculations:

$$\text{time} = \frac{\text{coulombs x ion dose x area}}{\text{beam current}}$$

Examples:

1. Present: IR Extrion-200 (50 μa beam current)

$$t = \frac{(1.6 \times 10^{-19})\ (1.0 \times 10^{15}\ \text{ions/cm}^2)\ (65.5\ \text{cm}^2)}{5 \times 10^{-5}} = 209.6\ \text{sec.}$$

2. Future: Extrion System (10 ma beam current)

$$t = \frac{(1.6 \times 10^{-19})\ (1.0 \times 10^{15}\ \text{ions/cm}^2)\ (65.5\ \text{cm}^2)}{1 \times 10^{-2}} = 1.048\ \text{sec.}$$

Implanters with beam currents of 0.1A are predicted for the early 1980's, if required. Obviously, with such high power systems cell cooling becomes a critical factor. This is under study and will be treated in more depth in a future report. Ion implantation does not require the backside silicon etch to remove the N+ backside junction formed during a furnace frontside N+ junction formation. In addition, the cost of oxide masking for planar junction formation or the silicon edge etch required to clean the peripheral junction formed during N+ front and P+ back surface field formation is simplified by using a peripheral metal mask during the front N+ ion implantation, thus forming a frontside planar junction.

For purposes of the evaluation (Figure 5) of the ion implantation process, gaseous diffusion using phosphorous oxychloride (POCl) and boron trichloride ($B\ Cl_3$) and polymer (spin-on) dopant technologies were used. It should be understood that the advantages or disadvantages of one process compared to the other two does not necessarily apply to both of the others and when it does they must be weighed to a differing degree. Furthermore, the appearance of a - in the chart in Figure 5 is not intended to imply that the process is not adequate, but rather that another process is considered superior for that particular function.

It has been assumed for this evaluation that laser annealing will be utilized as the annealing technique for the ion implanted cells. Should this assumption prove erroneous items 6 through 9 in Figure 5 must be reevaluated. However, if this were to be the case, ion implantation still appears to be the best choice as a doping technique.

In order to achieve the technological objective of the ion implant—laser anneal program, it is recognized that we must overcome the problem that is associated with using a single energy implant directly into silicon which produces a detrimental bucking drift field extending from the peak ion concentration of the ion implant region, to the silicon surface. This is a

ATTRIBUTE	ION IMPLANT		DIFFUSION FURNACE			
			GAS DOPANT		SPIN-ON DOPANT	
	Present	Future	Present	Future	Present	Future
1. Dopant Application						
a. quality	+	+	-	o	-	o
b. uniformity	+	+	+	+	-	-
c. profile repeatability	+	+	+	+	-	o
d. simultaneous N^+P^+ diffusion/anneal	+	o	-	-	+	+
2. Edge Etch	+	+	-	-	-	-
3. Backside Removal	+	+	-	-	+	+
4. Throughput	-	+	-	-	+	+
5. Anneal Required	-	-	+	+	+	+
6. Chemical Expenditure	+	+	-	-	-	-
7. Oxide Removal Required	+	+	-	-	-	-
8. Rinse and Dry	+	+	-	-	-	-
9. Further AR Coating Required	-	-	+	+	-	o

KEY: Advantage: +

Disadvantage: -

Unknown: o

Figure 5. Evaluation of Advantages and Disadvantages of Junction Formation Techniques

consequence of the inherent nature of the implant impurity profile done at a single beam energy. The approach generally proposed or taken to avoid this undesirable effect is to implant thru an appropriate dielectric such as silicon dioxide or silicon nitride. This can produce the desired impurity profile in the silicon with maximum concentration at the surface, diminishing toward the region of the junction and eliminating the bucking field otherwise present.

This method though technically effective, costs added process steps and is energy wasteful in the implant process. A concept has been suggested that involves adjusting implant beam energy vs. implant time at a maximum constant current so as to produce an optimized impurity profile for the elimination of this drift field. Both mathematical and experimental implant programs should be studied to determine the feasibility and viability of this approach.

The ion implantation process under consideration for use in solar cell manufacture has the potential for high rate production. Assuming that the basic process proves to be acceptable, for this application, at least two other related problems must be overcome. One of these is the dissipation of the heat generated in the wafer by the high energy levels to be employed, and the second is to find a method of presenting the wafers to the ion beam in a high vacuum at a suitable fast throughput rate.

The standard approach for implantation of wafers involves the use of a carrousel which supports a number of cells on individual stations. This system requires that the carrousel be manually loaded and then placed within the vacuum chamber which must then be pumped down. The procedure involves excessive idle time and as presently configured, the carrousel system is not capable of achieving a production level high enough to support this program. It does offer the option of scanning the wafers individually, indexing through each station in sequence; or of scanning all wafers at once as the carrousel rotates at a constant speed. Temperature rise in the wafers is minimized in the latter mode.

The wayflow production wafer handling system* uses vacuum lock chambers to gravity feed individual wafers into the ion implantation chamber and then to receive the processed wafer for return to atmospheric pressure. This system is characterized by a 3 to 4 second dead time between implantation cycles while the cells are being transferred in and out of the vacuum lock chambers. Conveyor belts are used to transport the components to and from the wayflow unit. A maximum throughput of 250 wafers per hour (14.4 seconds per wafer) is reported for this system, which is also short of the production rate necessary to support the LSSA program with a reasonable number of processing units.

Optimized production with the ion implantation process will depend upon maximum utilization of the beam at the highest practical energy levels. The limitations of the presently available wafer handling systems can be mitigated but some idle beam time will always be present in these or any system which must wait upon physical movement of the cells. One possibility is to alternately direct the beam between either of two wafer handling stations. This might be accomplished by a modification as shown in Figure 6 of the X-Y electrostatic scanning system described in Ref *. The addition of a second horizontal axis scanner, positioned a minimal distance down stream from the first scanner and set up to deflect the beam at a different angle, could allow rapid switching from one wafer station to the other. This would allow a loading time at the idle station approximately equal to the implantation processing time at the active station. Two wayflow wafer handling systems, each with a 3 to 4 second dead time should then be more than adequate to support a near 100% utilization of the beam at the fastest implantation rate which can be envisioned.

Temperature control of the wafer under the suggested system would present a problem. The configuration of the wayflow system suggests that it would be possible to circulate cooling water or a liquified gas through passages in the housing and in the wafer holder.

*Ryding, Wittkower and Rose - Features of a High Current Implanter and a Medium Current Implanter, J. Vac. Sc. Technology, Vol. 13, No. 5, Sept/Oct 1976.

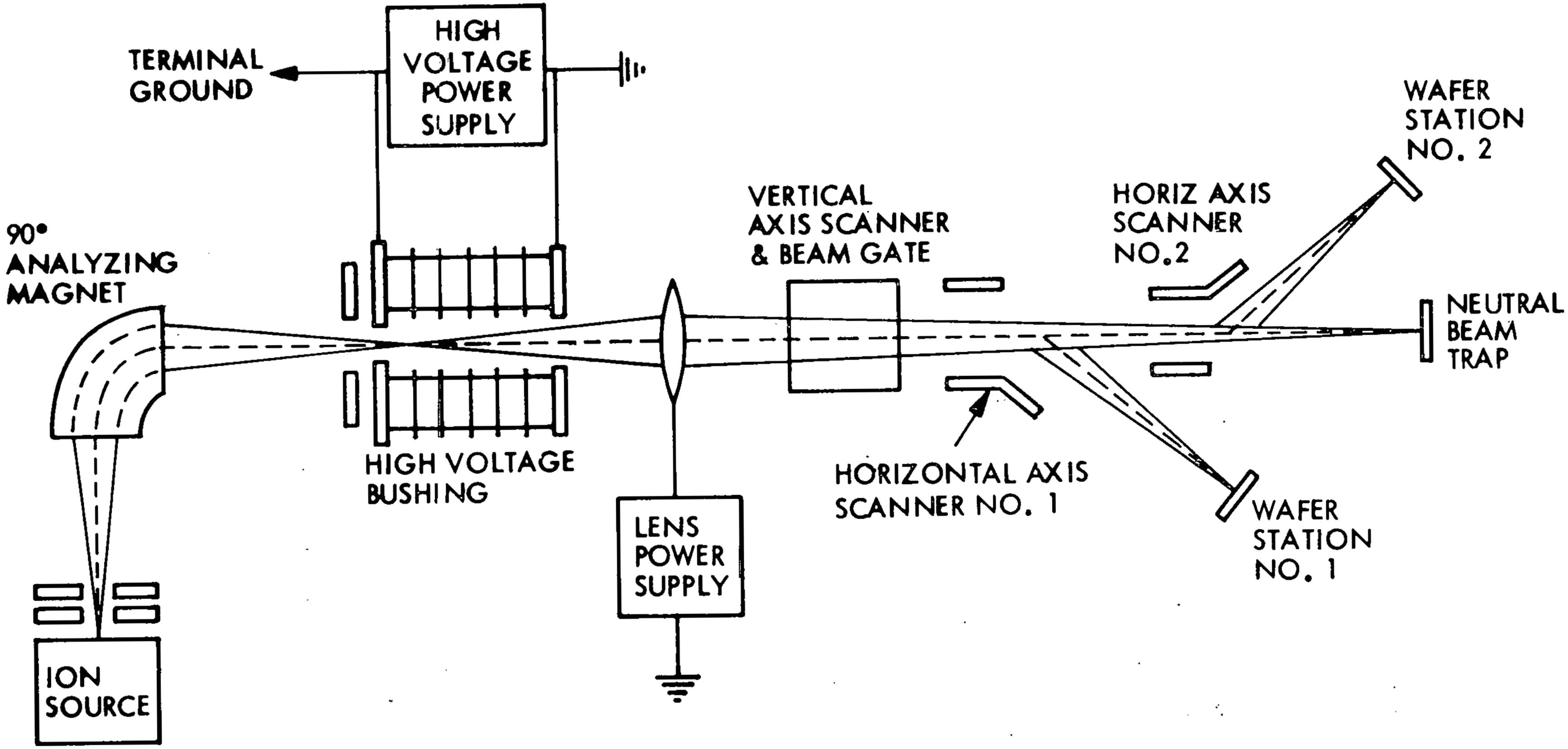


Figure 6. Schematic of the Medium Current Implanter as Described in Reference *and With Suggested Modifications

One suggested approach has been described. At least three others can be visualized. These include:

1. An Expansion of the carrousel system using three vacuum chambers on a large indexing table. One chamber would be at a load/unload station, one at a pump down station and the third would be at the working station. A small volume lock would be used at the interface of the chamber and the ion beam tube at the working station.

2. A system in which cells are nested in flat trays and held in position by a mask which covers the perimeter face of each cell. Trays are then processed through the vacuum chambers in much the same manner as for the previous method, with a mechanical scanning device to position the cells to the beam. This method would be useful if trays were used for cell handling in prior and/or subsequent operations.

3. A three chamber system for processing of individual cells had been defined at LMSC. This is similar in principle to the wayflow system described earlier but differs in that wafers pass through five interlock and three main chambers in their progress through the system. Three levels of vacuum are used and mechanical complexity is reduced by transfer of the wafers on turrets within the chambers. This system promises a higher throughput rate than the wayflow system and would be useful in the event that switching of the beam as described earlier proves to be impractical; or if the implantation process time could be reduced to a two or three second cycle.

We conclude that the decision to use ion implantation can be made on the basis of the quality and speed of the basic process, and that the associated problems of cell handling and cooling can be resolved to achieve an automated process.

3.1.3 Laser Annealing

Evaluation of literature[2-9] concerning laser annealing has revealed that with this process several technical advantages can be attained over the presently utilized furnace annealing technique. The advantages are:

1. Relative immobility of the junction as compared to furnace annealing.

2. Reduction by one to two orders of magnitude of bulk silicon dislocations introduced by present furnace anneal or diffusion processes.

3. More complete regrowth of the implanted surface resulting in fewer dislocation loops and stacking faults associated with higher pulsed anneal temperatures than is practical with furnace annealing.

4. Precision control of annealing depth by choice of laser type can be accomplished since most of the energy expended will be dissipated near the silicon surface and will depend on the wavelength of the particular laser chosen and its absorption coefficient in silicon.

Based on the referenced literature and preliminary calculations it appears that the guiding criteria in selecting a laser system for solar cell annealing applications should be as follows:

1. The laser must be capable of providing sufficient power and energy to allow the required annealing process to take place.

2. The laser must be of suitable wavelength to minimize the depth of beam penetration into the silicon.

3. The laser must be capable of annealing the cells at energies and speeds which would make the system cost compatible within the required contractual goals.

Since the light absorption coefficient (Figure 7) of silicon and consequently the mean absorption length increase considerably with increase in the wavelength of the incident beam, it is concluded that no laser exceeding the wavelength of a YAG laser should be considered. The three lasers which appear to be the best candidates for this evaluation are Argon, Ruby, and YAG with wavelengths of .5 μm, .694μm, and 1.06 μm, respectively. The Argon laser is a continuous wave laser, whereas the Ruby and Yag are pulsed type systems. Two types of pulsing techniques are utilized for the above lasers, namely, "Q-switch" and "Conventional mode". The Q-switched systems TEMoo mode should be capable of discharging a minimum 15 joules of energy into a 10-50 nsec pulse. Conventional mode systems due to their longer pulse duration should provide energies in excess of 15 joules. Utilization of such high power lasers is intentional. With these energies and with proper uniformity the beam can be homogenized to attain full, uniform illumination of the entire cell surface with resultant single pulse annealing.

It is anticipated that the energy requirements and therefore operational costs of laser annealing would be lower than furnace annealing. However, a cost analysis is deferred to the next quarterly report. At that time studies will be completed and data will be available to indicate which laser system should be utilized to attain the required annealing of the solar cell wafers. This is important since the energy requirements of a Q-switched system differ

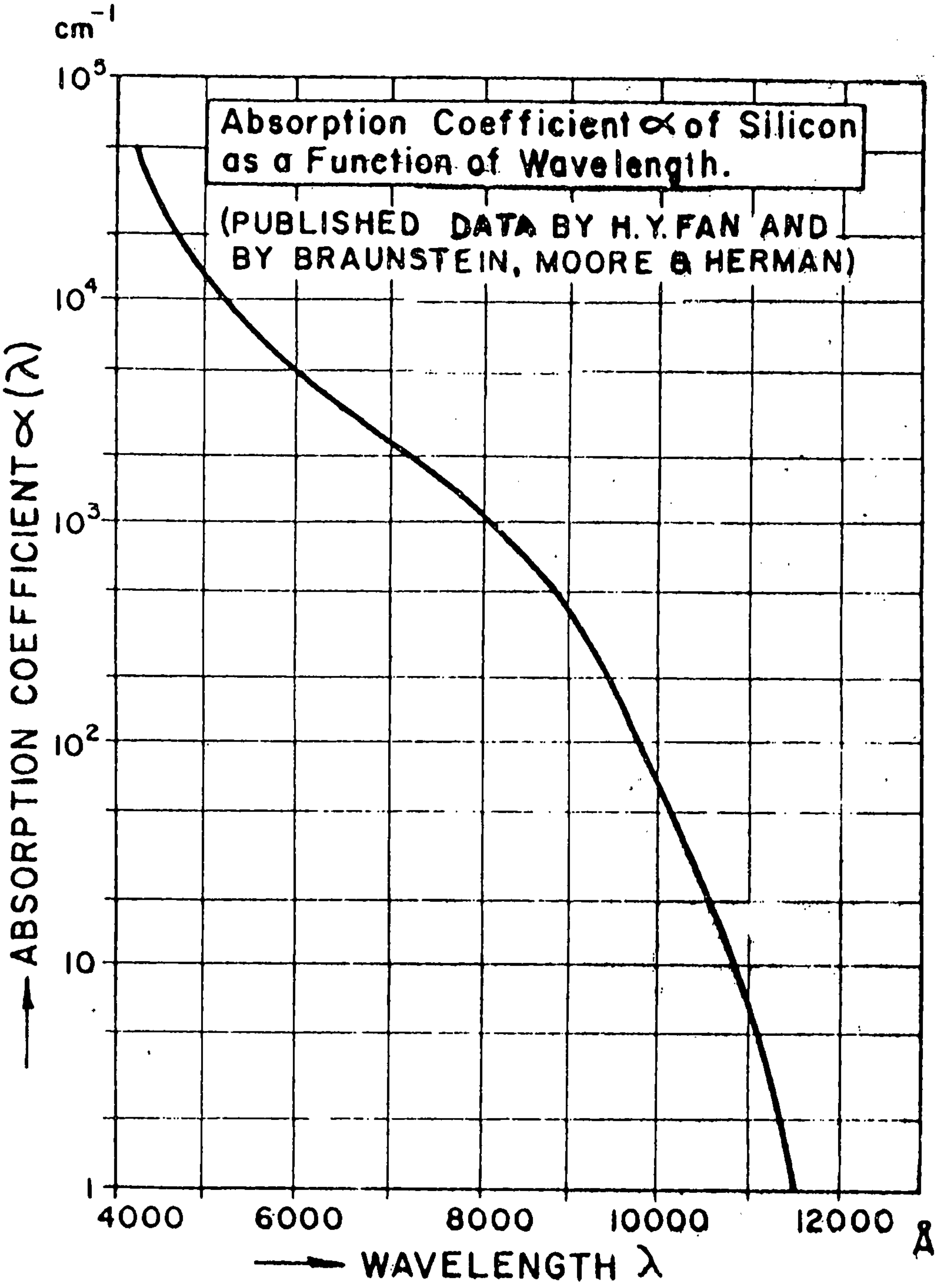


Figure 7. Absorption Coefficient ∝ of Silicon As A Function of Wavelength

substantially from a conventional mode system. Final selection of a laser will be made based upon technical considerations and cost analysis.

3.1.4 Screen Printed Contacts

The merits of screen printed contacts for terrestrial solar cells have, in general, received universal acceptance from the standpoint of low cost manufacturing. Equipment is claimed to be available today which can process in excess of 5,000 parts/hr[10]. At these rates, it is apparent that the Project's high throughput objectives can be satisfied.

Participants in this LSSA Project describe achieving fine line widths of 5 mils as routine, using a 320 mesh screen. This is consistent with our work performed on Hybrid Microcircuits where line widths of 5 mils were also demonstrated[11,12]. With this demonstrated, fine line printing capability, the photoactive area on the top surface can be maximized to achieve areas greater than 90%. The question then, is how repeatable is the screen printing process? Process repeatability is dependent upon many factors including, paste consistency (batch-to-batch), squeegee and screen maintenance and durability, squeegee pressure and speed, and cell flatness. These and other areas still require verification and further refinement.

Silver pastes are, at present, prime candidates for ohmic contacting due to their excellent conductivity properties. They have been in wide use as conductors in thick film circuitry due to their ease of application and electrical stability in varying environments. Of the noble metals in common use for conductors (the others being gold, platinum and palladium), silver is the lowest in cost.

Conductive pastes have been discussed and analyzed under the Phase 1, Automated Array Assembly Task of the LSSA Project, (e.g., RCA Quarterly Reports 2 and 3 of JPL Contract 954352). There is no point in entering into an extensive evaluation on this subject except to state that there is general accord in the relative high material cost/watt of silver bearing pastes. Our preliminary estimates on 0.5 mil thick back contacting with 100% coverage showed greater than $.15/watt cost.

Other candidate metal filled pastes such as copper, nickel and aluminum, although perhaps lower in material cost, have other shortcomings which would preclude their general acceptance for this application without extensive experimentation and testing.

Reduction of the amount of silver screened on the backs followed by solder dipping might lower costs. Pattern screening is another alternative; however, this would also have to be substantiated through experimentation.

Whereas, high throughput of screen printed parts is achievable, performance and long-life of printed hardware is another matter. Such factors as the extent of conductor material penetration into the region of the junction after firing, contact adhesion and resistivity, particularly in a moisture environment, and solderability, still pose serious concerns and need further investigation and testing for life cycle performance.

It is apparent that the contacting process as presently known, warrants further investigation into alternate materials and/or processes.

3.1.5 Sprayed Anti-Reflective Coatings

As has been generally reported by participants in the LSSA Project[13-15], the spray-on techniques for AR coatings offer the best chances for high throughput and acceptable coating thickness and uniformity on large area surfaces. Spray-on applications have particular appeal on cells with irregular shapes and sizes, and having rough surfaces, such as those texture-etched. Throughput in excess of 3000-three inch wafers per hour are considered attainable based on our existing Zicon 10,000 in-line autocoater, and RCA's Process Parameter Description on AR spray coat[16]. Our unit is equipped with automatic overhead spray traverse (front-back) with up to a 17 inch stroke. Traverse speed is 0 to 20 inches/sec, continuously adjustable. Work pieces are incrementally indexed under the gun permitting in-line processing.

The two important application concerns, of course, are in thickness control and uniformity. The vapor-carrier system forms the heart of the Zicon equipment, and is reputedly capable of achieving precise control of coating thickness and uniformity. These aspects will be investigated in the course of this contract.

3.1.6 Module Assembly

Much of the following detailed technical discussion on module assembly reflects information derived from in-house funded activities and is offered to provide our reference technology base in this area.

The LMSC Module Design defined in Section 2 and documented in the final report on Module Development[17] is specified as the baseline for assembly planning. The first consideration in this regard is the determination of the required production rate. An approximation will serve our present purpose by providing a perspective of the general assembly equipment requirements.

Each individual cell must be handled and processed in production of a module, regardless of the method of assembly. We assume that the cycle time per cell will be four seconds, that cells will be processed sequentially and that the module level operations can be accomplished concurrently within the time span represented by the processing of the forty-one cells in our module. The assembly time per module is then 4 seconds x 41 cells = 164 seconds, or

2.7 minutes. On this basis the production rate for each assembly line will be 22 modules per hour, with the number of parallel assembly lines required to meet the scheduled factory output shown in Figure 8. Viewed in this perspective, we believe that the quantity of parallel assembly lines shown is a reasonable number through 1984. The thirty-six lines shown for 1986 can be expected to be reduced in numbers by process improvements and faster throughputs. There is also the ever-present possibility of early obsolescence through a technological breakthrough.

These approximations lead us to conclude that a minimum assembly line production rate of 22 modules per hour is acceptable for at least the first few assembly systems. Since this rate is derived from the processing time per cell, the throughput can also be measured in watts/hour or M^2 of modules/hr, which are not related to module size.

The next important consideration is the selection of a method of assembly capable of meeting the desired production rate. Two basic approaches to module assembly are known. One involves the direct assembly of cells in a module level fixture and the other employs the intermediate step of sub-assembly of cells into series connected strings followed by arrangement of the strings into the module configuration. A preliminary assessment of the relative merits of the two approaches is shown in Figure 9. Both methods have merit and it is probable that either could be developed to the point of satisfying the production requirements of this program. There is also the possibility of combining the two methods by attaching interconnects to individual cells and then positioning these subassemblies in a module level fixture. Other variations may also be considered, but it is simpler to deal with the basic methods first. Both of these will be discussed.

Prior LMSC studies in this area and our current assessment of the requirements of the automated assembly task lead us to the conclusion that the cell string sub-assembly method is best suited to our purpose. There are a number of reasons for this selection.

Year	M^2 of Modules Per Year (1)	Number of LMSC Modules At .25 M^2 Ea.	Req'd Factory Production Rate in Modules per Hour (2)	Number of Assy Lines Req'd to Meet Production Rate (3)	Approximate Number of Assembly Lines @ 10% Extra Capacity
1980	27,000	108,000	13	.59	1
1982	100,000	400,000	48	2.36	3
1984	490,000	1,960,000	237	10.77	12
1986	1,800,000	7,600,000	718	32.64	36

(1) From JPL Document 5101-33 Interim Price Estimation Guideline - Table 2-1 Standardized Production Quantities.

(2) Based on 8,280 Hrs/Yr - From JPL 5101-15 Samics Workbook P32.

(3) Arbitrarily Assigned Production Rate of 22 Modules/Hr.

Figure 8. Approximate Number of Assembly Lines Required for a Module Assembly Factory at 40% of Market

ASSEMBLY METHOD	ADVANTAGES	DISADVANTAGES
Direct Assembly of Cells at Module Level	- Allows interconnect pattern to be cut from one piece - Allows mass soldering technique to be used - Reduced number of operations	- High waste of interconnect material - Probable high energy consumption for mass soldering - Operations are mostly sequential (lower production rate) - Requires quantity of complex fixtures in circulation through most of assembly operations
Sub-Assembly of Cells into strings-assembly of strings into module	- Many simultaneous operations (higher production rate) - Individual spot application of heat to make solder joints (lower energy consumption) - Greater modularity of assembly equipment - downtime reduced by quick replacement of modular units. Lower investment in standby equipment - Easier to modify in accommodation of process and/or design change	- Greater number of operations therefore more process parameters to be controlled - Probable higher equipment investment

Figure 9. Comparison of Candidate Module Assembly Methods

- The LMSC Module Design has the cells series connected in straight line strings for which this method is particularly well suited.

- The process appears easier to modify in accommodation of the changes anticipated in the next several years.

- The processing equipment is easier to configure in separate modular units to permit quick replacement to minimize downtime for maintenance and repair.

- The cell string sub-assembly method appears to have a higher production rate potential.

<u>Assembly at the Module Level</u>

The direct assembly of cells at the module level is of interest because of the smaller number of processing steps involved and because of the potential for making most or all of the reflow solder connections at one time. Three process options for this soldering step were considered. They were conventional oven heating, induction heating and vapor phase heating. The latter method is potentially attractive because it may allow the elimination of solder flux. This has not been tested for solar array assemblies, but successful reflow soldering of circuit boards using solder preforms without flux has been reported by another Lockheed facility.

The direct module assembly process sequence used in our evaluation is as follows:

1. Etch interconnect pattern for entire module, leaving ties to a strip-out pattern which is used for location.

2. Place the interconnect pattern in a fixture, locating on index holes in the strip-out pattern.

3. Place the open structured fixture on a sub base with projections near each cell location which lift each N contact of the interconnect pattern to allow clearance for placement of the cells.

4. Unload cells from cartridge and "clock" using a "Pick and Place" arm with a vacuum chuck, a turntable, and a photodetection device.

   NOTE: Requires micro computer, programmable controller, or similiar unit to count cells and direct the orientation of those to be placed at the end of rows where they must connect to adjacent rows.

5. Place cells in fixture. Requires a second "pick and place" arm to transfer "clocked" cells from operation 4 and place them in the fixture, which is indexed to receive the cells by an NC controlled table. (An alternative would be to use a programmed robot arm with sufficient reach to position all the cells while the fixture remains fixed).

6. Position frames on both upper and lower faces of the fixture to clamp the interconnect contacts to their proper locations on the front and back faces of the cells.

7. Place the loaded fixture in the soldering unit until reflow soldering is completed. (NOTE: It is assumed that the interconnects, the cells, or both, have been pre-tinned).

8. Remove the fixture from the soldering unit, remove the clamp frames, and pick up the entire cell interconnect assembly with a multiple chuck vacuum pick-up device and transfer to the next operation.

9. Cleaning, if necessary, and final assembly is assumed to be the same as for the cell string sub-assembly method.

Cell String Sub-Assembly

The cell string assembly approach has been examined in greater detail. A number of candidate processes have been identified as potentially applicable to the Lockheed design and these are presented in the charts of Figures 10 and 11. It will be noted that the operations are divided into several basic groups. These represent logical divisions of the work in terms of assembly sequences, equipment, and factory arrangement. The specifics of the various operations will be discussed later.

The first group, entitled "Prepare Cells for Assembly", is included on the assumption that in the early production of these arrays it will be necessary to clean and retest cells prior to the assembly operations at the assembly plant. At some later date, it is assumed that these cells will be received, cleaned, tested, and sorted by power output levels in preparation for direct assembly.

The second group of operations, "Preparation of Interconnects", offers a considerable number of variations in method. From the point of view of cost alone, it may be assumed that progressive die stamping of these interconnects in strip form is the most attractive method. However, until the analysis is completed, the other techniques cannot be discarded and must be considered. A number of commercial firms also offer etched patterns in strip form, either on a substrate or unsupported. It may also be desirable to plate and/or to solder coat the interconnects as part of the same continuous process sequence. None of the operations of Group II introduce new art; they are all merely adaptations of existing technology applied to our particular design requirements. One operation of special interest in Group II is operation 80 where it may be necessary to cut access holes in

CANDIDATE ASSEMBLY OPERATIONS				CANDIDATE PROCESSES – USING OPERATIONS NOTED					
GROUP I	PREPARE CELLS FOR ASSEMBLY	TOOLS AND EQUIPMENT		A	B	C	D	E	F
10	TRANSFER CELLS FROM SHIPPING CONTAINER TO WASHING MACHINE	TRANSFER CELLS TO MAGAZINE OR CONVEYOR DEVICE	AUTOMATIC DEVICE TO UNLOAD CONTAINERS	10					
20	MACHINE WASH	STANDARD EQUIPMENT WAFER WASHING MACHINE		20					
30	CLOCK, TEST, AND SORT. TRANSFER CELLS FROM MAGAZINE TO TURNTABLE - (STA. 1) CLOCK (STA. 2), TEST (STA. 3), UNLOAD (STA. 4) AND SORT TO MAGAZINES	1. PICK AND PLACE ARM TO TRANSFER CELLS TO TURNTABLE 2. LIFT, ROTATE, READ, POSITION, AND RETURN TO STATION 2 3. SOLAR SIMULATION TEST 4. UNLOAD AND PLACE IN PROPER MAGAZINE (PICK AND PLACE)	AUTOMATIC MACHINE WITH PROGRAMMED CONTROL. USE WITH SOLAR SIMULATOR – COMPUTER FOR DATA ANALYSIS AND SORT	30					
40	TESTED AND SORTED CELLS TO STORES OR TO ASSEMBLY AREA	PROTECTIVE PACKAGING	PLACE IN MAGAZINE PACKAGING FOR OPERATIONS IN GROUP 3 REQUIRES QUANTITY OF MAGAZINES FOR RECYCLE	40					
GROUP II	PREPARE INTERCONNECTS	TOOLS AND EQUIPMENT		A	B	C	C	E	F
10	PUNCH INTERCONNECTS IN METAL TAPE, LEAVE TIES TO HOLD IN TAPE FORM	PRESS AND PROGRESSIVE DIES – REEL TO REEL – PUNCH PATTERN MAY INCLUDE INDEX HOLES	METAL RECEIVED SLIT TO FINISH WIDTH	10	10				
20	FORM INTERCONNECTS FROM PAIRED WIRES (RETAIN IN CONTINUOUS FORM AT THIS STAGE)	NONE	USE RIBBON WIRE ON SPOOLS AS RECEIVED			20	20		
30	PUNCH INDIVIDUAL IC'S AND STACK IN MAGAZINE	PRESS AND PROGRESSIVE DIES WITH MAGAZINE LOADING PROVISION	REQUIRES QUANTITY OF MAGAZINES FOR RECYCLE						30
40	ETCH INTERCONNECTS FROM METAL CLAD ON PLASTIC TAPE	CONTINUOUS REEL TO REEL PHOTO PROCESS/ETCH/RINSE/DRY/ETC.						40	
50	PLATE OR COAT INTERCONNECTS AS REQUIRED	REEL TO REEL	MAY BE INCLUDED IN OPERATION 50	50	50	50	50	50	
60	CUT ACCESS HOLES IN NONCONDUCTIVE CARRIER TAPE	REEL TO REEL PRESS AND DIES	USE TAPE AS RECEIVED; MAY BE INTERLEAVED CONTROL INDEX SPACING	60			60		
70	BOND IC TO CARRIER TAPE IN REGISTER	REEL TO REEL WITH REGISTER CONTROL		70			70		
80	LASER CUT ACCESS HOLES IN CLAD TAPE	CO_2 LASER AND TEMPLATE REEL TO REEL WITH INDEX						80	
90	PKG REELS FOR STORAGE			90	90	90	90	90	

Figure 10. Preparation of Components for String Assembly

CANDIDATE ASSEMBLY OPERATIONS					CANDIDATE PROCESSES – USING OPERATIONS NOTED					
GROUP III	ASSEMBLE STRINGS AND ARRANGE TO FORM MODULE	TOOLS AND EQUIPMENT		COMMENTS	A	B	C	D	E	F
10	PUNCH OUT IC TIES	ALL OPERATIONS THROUGH 100 ARE PERFORMED BY MODULAR TOOLS ON STRING ASSEMBLY MACHINE. COMPONENTS ARE INDEXED THROUGH OPERATION STATIONS BY A WALKING BEAM TRANSFER UNIT USE PROGRAMMABLE CONTROL FOR ALL OPERATIONS THROUGH 110	MINI PRESS AND DIES TO PUNCH OUT TIES FOR SINGLE IC PATTERN PROVIDE REEL TAKE UP FOR MARGINS	(OPERATION SEQUENCE MAY VARY)	10		10	10		
20	FORM N CONTACT TABS ON ICs		MINI PRESS AND FORMING DIES TO OFFSET 2 TABS ON SINGLE IC PATTERN		20	20	20	20	20	20
30	APPLY FLUX PASTE SOLDER OR CONDUCTIVE EPOXY AS REQUIRED		METERED DISPENSING EQUIPMENT DEPOSIT MATERIAL 4 PLACES ON SINGLE IC – 2 ABOVE, 2 BELOW		30	30	30	30	30	30
40	MATE N CONTACTS AND CELLS IN SEQUENCE. SOLDER, WELD, OR BOND		LASER W/BEAM SPLIT 4 WAYS FOR SOLDER PARALLEL GAP WELDERS W/MONITORS FOR WELD	CLOCK ALL CELLS BEFORE MATING. COUNT CELLS/STRING AND SKIP CELL BETWEEN STRINGS			40			40
50	MATE P CONTACTS AND CELLS IN SEQUENCE. SOLDER, WELD, OR BOND		SIMULTANEOUS ATTACHMENT 2 PLACES OPERATION 40 AND 2 PLACES OPERATION 50	IF REQUIRED BY DESIGN, RECLOCK LAST CELL IN STRING BEFORE ATTACHMENT			50			50
60	MATE BOTH CONTACTS TO CELLS IN SEQUENCE SOLDER, WELD, OR BOND		SAME AS ABOVE EXCEPT ATTACH ALL 4 PLACES IN THIS OPERATION	NOT POSSIBLE TO RECLOCK	60	60		60	60	
70	REMOVE METAL TAPE CARRIER STRIP		SAME TOOLS AS OPERATION 10			70				
80	REMOVE NONCONDUCTIVE CARRIER TAPE (IF DESIRED)		TAKE UP REEL	REQUIRE "LIGHT TACK" ADHESIVE TO PERMIT REMOVAL	80					
90	CUT STRING TO LENGTH		MINI PRESS AND DIES TO CUT IC TO SEPARATE STRINGS		90			90	90	
100	PICK UP ASSEMBLED STRING AND TRANSFER		VAC CHUCKS FOR EACH CELL IN STRING PICK UP, TRANSFER TO SIMILAR CHUCK IN OPERATION 110		100	100	100	100	100	100
110	GROUP STRINGS TO FORM MODULE ASSEMBLY AND TRANSFER TO GROUP IV	PICK UP STRING IN EACH OF 3 CHUCKS – ARRANGE CHUCKS TO SUIT MODULE CONFIGURATION – IMMERSE IN CLEANER – TRANSFER TO ASSEMBLY CHUCK		PART OF ASSEMBLY MACHINE AT END OF WALKING BEAM	110	110	110	110	110	110

GROUP IV	FINAL ASSEMBLY	TOOLS AND EQUIPMENT	
10	CLEAN GLASS PANEL AND FRAME	SOLVENT BATH, SCRUBBER, DRY CHAMBER, APPLY GASKETING AND FRAME	
20	APPLY ADHESIVE AND DEGAS	DOCTOR BLADE – APPLICATION – VACUUM CHAMBER	
30	MATE CELL/IC ASSEMBLY TO GLASS/FRAME ASSEMBLY AND CURE	TRANSFER ON CHUCK FROM OPERATION 110 OR 200 VAC BLADDER AND CURE (FAST)	
40	ADD LEAD WIRES AND MAKE FINAL CONNECTIONS	MANUAL	
50	ADD PROTECTIVE COATING ON BACKSIDE OF ASSEMBLY AND CURE	AUTOMATIC DISPENSE WITH MANUAL ASSIST	

Figure 11. Candidate String Cell Module Operations

nonconductive carrier tape to expose the metal interconnect for the joining operation. Either of two methods can be used for this—one is to prepunch the tape and then join the tape to the metal strip in register, the other is to use a laser to remove the unwanted carrier film. This is being successfully used by Lockheed on a production basis with a CO_2 laser, scanning through a metal mask. It is obvious, of course, that all Group II operations are for the string type interconnect and are applicable to the cell string assembly process.

The Group III operations are those where the cell string assembly is actually made, and these have been the subject of the greatest LMSC attention. It is in this group of candidate operations where the advantages to be derived from the use of modular equipment are the most obvious. The basic structure of this series of equipments is the walking beam, which is used to transfer the interconnects and the cells through the sequence of operations, all of which are performed simultaneously as the parts are indexed through the various stations. (The term "walking beam" is used here to mean any of several methods for indexing cells through the work stations).

The walking beam cited in Figure 11 and typical modular equipment items are shown pictorially in Figure 12. A schematic diagram of this process is shown in Figure 13 as it would be set up for process "C" of Group III operations. A partial definition of the operational functions of the modular units is also noted, as are the locations of the vacuum chucks used to transport cells through the system. It will be evident that capability for rearrangement to accommodate any of the processes can be incorporated in the system design.

Operations 10 through 110 described in Group III are all capable of being configured as individual plug-in equipment modules. Reference to the candidate processes as shown on the chart will indicate that not all of the modules need be developed. Similarly, additional modules may be required as further evaluation is conducted.

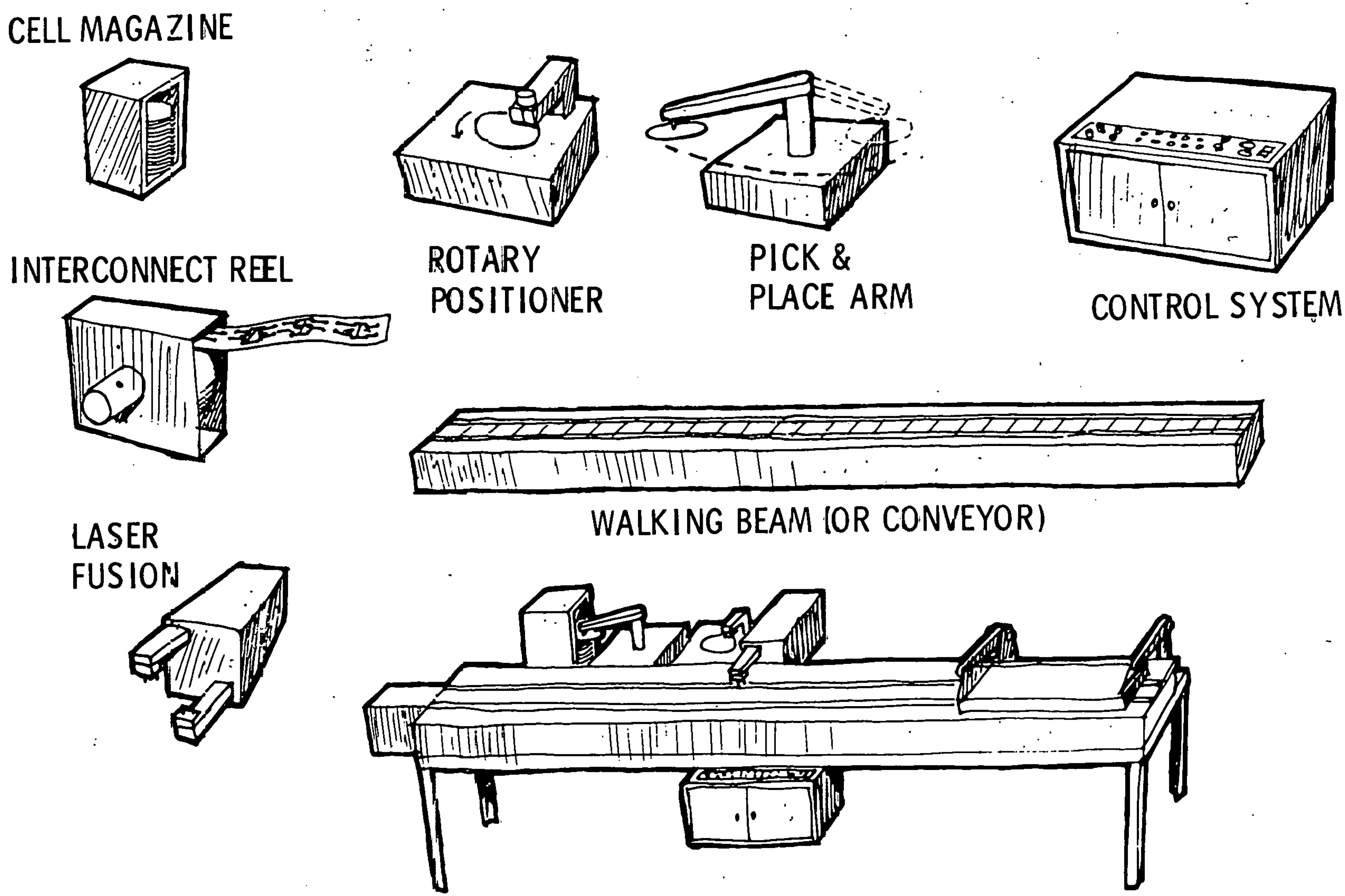
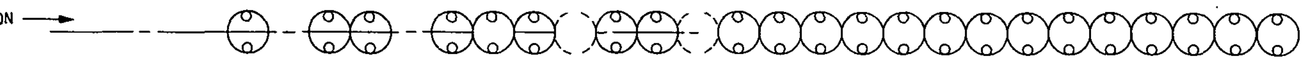


Figure 12. Concept Sketch Modular Equipment and Walking Beam

CELLS IN POSITION →



Operation	Operation of walking beam				"CENTER" CELL AND LOAD	OPEN - CLEARANCE FOR OPERATION AT 4	ROTARY POSITION CELL (CLOCK)	APPLY PASTE TO "N" CONTACTS ON CELL	OPEN - CLEARANCE FOR OPERATION AT 9	POSITION "N" CONTACTS	SOLDER "N"	CUT TIES	OPEN - CLEARANCE FOR OPERATION AT 13	RECLOCK AS REQUIRED	APPLY PASTE AT "P" CONTACTS ON CELL	OPEN - CLEARANCE FOR OPERATION AT 14	SOLDER "P"	BUILD UP TO 13 OR 14 CELL STRING AS REQUIRED AND TRANSFER TO NEXT OPERATION ↕ ↷														
WALKING BEAM STATION NO. (@SPACING 3-IN.)		1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	⑥
TOPSIDE VACUUM CHUCKS (STATIONARY)					⑤		O ③	O		O ①	O	O		O ③	O																	
TOPSIDE CHUCKS – ASSEMBLY PICK-OFF DEVICE																	O	O	O	O	O	O	O	O	O	O	O	O	O	O	O	
WALKING BEAM CHUCKS ON PRIMARY SLIDE				②	O			O			O	O			O			O	O	O	O	O	O	O	O	O	O	O	O	O	O	
WALKING BEAM CHUCKS ON SECONDARY SLIDE							O			O				O			O															
ACTUATORS ④ CYL 1	↓ ↔				→			↕ P		↕	↕ T1	↕↕		T1	↕ P		↕ T															
CYL 2										↕				T2																		
CYL 3														0																		
MOTOR 1							M↻																									
MOTOR 2																																
SENSORS LIGHT SOURCE AND PHOTODIODE							X							X																		
PNEUMATIC PROXIMITY SENSOR					X			X		X	X	X			X		X													X	X	

NOTES:

① TOPSIDE CHUCK RAISES CELL TO ALLOW "N" CONTACTS TO BE MOVED TOPSIDE

② INDICATES POSITION AT RETRACT TO PICK UP CELL FOR INDEX FORWARD
INDICATES POSITION AFTER INDEX AND AT "HOLD" FOR OPERATION
– 2 CHUCKS AT EACH STATION

③ TOPSIDE CHUCK ROTATES AT FIXED SPEED. PHOTO CELL READS CELL PATTERN AND SIGNALS "STOP" AFTER DELAY TIME. STATION 13 PROGRAMMED TO "SKIP", DELAY T1 OR DELAY T2

④ DIRECTION OF ARROW DENOTES POWERED ACTUATION.
SPRING RETURN IS ASSUMED FOR CYLINDERS AS REQUIRED
P = PULSE T = TIME DELAY

⑤ SPECIALLY FITTED STATION – NO TOPSIDE CHUCK

⑥ DESIGN TO ALLOW FOR ADDITION OF STATIONS BY EXTENSION ASSEMBLY

Figure 13. Schematic of Walking Beam Operation

In the first operation, Number 10, the ties that hold the interconnects in the body of the string are separated by a punch and die mounted in a miniature press. This is a standard operation except for its small size and configuration to suit the walking beam assembly.

The equipment module of Operation 20, which would be used to joggle the N contacts on the interconnects, is essentially the same module as in Operation 10, differing only in the die configuration. This operation would be used only in the event that the interconnect material was thick, stiff, or very closely coupled between adjacent cells.

The module for Operation 30 would utilize standard commercial equipment with multiple dispensing tips to meet specific quantities of a paste material at appropriate locations on the interconnects or on the cells. This material would most likely be solder flux or conductive paste as required by the operation. In the single string assembly four dispensing units would be used simultaneously. Lockheed has been using as many as eight tips simultaneously in a similar production operation.

Operations 40, 50, and 60 are all concerned with the attachment of the interconnect to the cell surfaces. This is, of course, the most important operation of the assembly sequence. In the different operations, we are concerned only with the sequence of the attachment steps. A number of candidate methods were considered for these processes. It is anticipated that reflow solder will be the technique used for the terrestrial cells of this program and several candidate methods are available. But any of the other basic attachment methods are capable of being mounted to the module and incorporated into the automatic system.

Operation 70, removing the metal tape carrier strip, is essentially the same as Operation 10, the difference being only that it occurs at a different point in the operation sequence.

Operation 80 is included only in the event that a tack adhesive carrier tape is used to transport the interconnects. This is an unlikely operation, because of its extra cost. The equipment involved is primarily a take-up reel with a tension clutch.

Operation 90 is used when a cell string assembly of appropriate length has been completed. The controlling program has counted the cells that have been processed through the equipment and has skipped a cell at the point of string completion. This leaves an opening where a miniature press with punch and die is free to make the separation and release the string from the other elements that are still remaining in the walking beam assembly.

Operation 100 is the last operation associated with the walking beam. As the string assembly has been processed through previous operations it progressively moves through vacuum chucks of the assembly pick-off device (refer to the schematic of the walking beam assembly, Figure 13). When the appropriate number of cells has been moved into the assembly pick-off device and the string has been cut off from the remainder of the work pieces, this cell string assembly is then ready for removal to the next operation. As presently envisioned, the top side chucks holding this assembly will rise a sufficient distance to permit the chuck assembly to be rotated 180 deg., presenting this assembly with its bottom side up for transfer to the next operation by a second and similar chuck assembly.

Before proceeding to the module assembly level, it should be noted that in a series-connected module, the interconnects at the ends of the strings will necessarily cross over to join with the end cell of the adjacent strings. In the Lockheed terrestrial module, the standard interconnect is used and is set at an angle to make this cross connection. In accommodation of this requirement, one additional process module is required that is not shown in the sequence of the Group III operations. It has been assumed in the previous discussion that the cells have come to the assembly operation already oriented or "clocked" so that the N contacts are in position for attachment to the interconnects. In that event, our additional module would be brought into play only when the controlling program had counted the appropriate number of cells and signaled that the cell then in the module station would need to be rotated to some angle other than the standard setting. At that point the turntable lifts the cell a sufficient distance to clear its normal rest points and begins rotation. A photo-reflective sensor is used to detect an appropriate point on the grid pattern on the upper surface of the cell. This signal is used as a reference point to properly position the cell so that when it is attached to the second-last cell in the string its interconnect is properly oriented for mating with the adjacent string. In the event that none of the cells have been properly oriented prior to presentation for Group III operations, a similar clocking device is used at the beginning of the sequence to process all of the cells that pass down this assembly line.

The final operation in the group is performed by equipment attached to the end of the walking beam, but operating independently of it. A number of string pick-off chucks equal to the number of cell strings in the assembly are mounted in an overhead frame where their motion may be controlled both in lateral travel and in rotation about the chuck vertical center line. This frame is positioned over the chuck on Station 100 of the walking beam assembly and is capable of presenting each of the several pick-off chucks in sequence to the transfer chuck of Station 100. Since, in a series-connected assembly, each alternate cell string assembly is reversed in direction, the appropriate pick-off chucks are also programmed to reverse their position accordingly. When all the chucks of Station 110 have been filled and assembled at the end of their carrier frame, all of the cells and the interconnects of the module are located precisely in the assembly position ready for cleaning, if necessary, or for final assembly. In this type of assembly operation, the final connection between cell strings to complete this series string circuit is made as part of the final assembly process.

The Group IV operations represent the final steps in the completion of a module. The glass face is assumed to be received from the vendor, cut to final size and ready for assembly, except for final cleaning. Standard equipment to wash, scrub and dry glass panels is available and will be employed for this operation.

As the glass leaves the cleaning operation on a conveyor it is ready for assembly to the solar cell module. Adhesive may be applied to the glass as shown on the chart or, alternatively, it may be applied to the individual solar cells by individual metering devices. This second process is presently used on the backside of cells in current LMSC module assembly. The mating operation of module cells to the glass panel requires precise positioning of the glass relative to the cell chucks and involves a degassing operation to eliminate any bubbles from the glass cell interface upon bonding. A special tool to perform this operation was devised by LMSC for use on the terrestrial module program and a modification of this process could be applicable in the production of this module assembly.

This discussion of module assembly methods has been deliberately broad in scope. Certain general directions have been established and within this framework a number of options are identified. The intensity of the current research and development activity in terrestrial photovoltaic arrays argues strongly for an assembly method which offers the greatest flexibility in accommodation of changing design. We consider this a necessary attribute in reducing the risk of premature obsolescence and therefore it assumes economic importance as well.

It has generally been established that the silicon material and the cell processing are the principal contributors to the cost of a module. The present emphasis on developmental work in these areas is well justified. Corollary reasoning would tend to delay commitment to a specific assembly process as long as possible. This position is reinforced by the generally expressed confidence of JPL contractors that automated assembly of these arrays presents relatively minor problems and that when automated, this assembly task represents a small portion of the overall cost. While this is true when compared with the magnitude of the problems inherent in reducing the principal cost items, the development of assembly equipment is still a major task.

Preliminary cost projections as outlined in the module development work[17)] reflect a high module material cost/watt at the 1 megawatt level ($.45/watt) assembly material exclusive of cells). Though cost projections into the 500 megawatt range would show further material cost reductions, we do not feel, at this time, that the reduction would be sufficiently significant to meet the Project cost goals. Indications are that major breakthroughs must yet occur in the assembly material categories (exclusive of cells) for goal realization, particularly in the areas of the glass superstrate and aluminum framing.

3.2 PROCESS VERIFICATION

Progress on the process verification phase of the work is delineated in the following subsections by process sequence.

3.2.1 Surface Texturizing Process (This work was performed at International Rectifier by Harold Weinstein)

The contract cell processing verification phase requires the use and evaluation of a texturizing process using sodium hydroxide based upon preliminary contract work performed by another contractor. The process was supplied by JPL.

The process called for a "flash" etch and rinse, followed by sequential five minute cleanings in hot trichloroethane and methanol, respectively. This portion apparently has not been included in the initial SAMICS evaluation. After, some initial set up problems, some modifications were made on the set up and procedural steps. The small quantities of wafers processed to date appear acceptable.

It is apparent from this texturizing work, however, that the process as outlined is highly dependent upon the wafer loading. Large batch quantities vs. small quantities affect the etch rate due to increased heating of the NaOH solution caused by the increased chemical reaction of the larger batch sizes. It would appear that this characteristic should be better defined to obtain consistent results.

It is felt that the flash etch step could be eliminated, or at least should be more closely related to the method of ingot sawing, which affects the damaged layers and amount of silicon to be removed. Relevant cost factors associated with flash etching could be significant in the overall economies. It is our general opinion that it is desirable to further improve the total texturizing process ("flash" etch included) to develop a more cost and performance effective process.

Due to the time and cost involved in repeated process checks by SEM analysis, required for control of this process, an on-line tester has been constructed. This instrument was constructed as a quick reference to check the reflectance of the texturized surfaces being produced, and is expected to be useful regardless of the texturizing process used. It consists of directing light from a light tower through a hole in a black box, at normal incidence, to the surface of the silicon wafer being measured. Light from the irradiated surface is reflected to silicon photocells mounted on the under surface of the "black box" top, adjacent to the light entrance hole. Short circuit current measurements of these photodetectors give relative reflectance values. A semi-polished chemically etched wafer surface exhibited approximately 4 times the reflectance of the NaOH etched groups. Time has not permitted extended tests; however, it is planned to make this kind of in-process testing (reflectance) a regular feature for Q. A. control of texture etched surfaces and to serve as an adjunct to other generally employed criteria such as SEM analysis. In addition it is anticipated that this reflectance measurement may later be utilized as a means for screening/categorizing cells for laser anneal, where the reflectance may influence power settings on the laser.

3.2.2 Ion Implantation

The LMSC contract requirement for ion implantation is limited to process verification of the technology which has been developed by other contractors, with such modifications as are required to implement the process and determine feasibility of the subsequent process of laser annealing of implant damage. One of the greatest deviations from the accepted "standard" solar cell implant is the initial implantation range. Since it is anticipated that very little, if any, junction movement[3]) (diffusion/redistribution) will occur during laser anneal, relatively higher acceleration voltages were used (100-150 KeV at LMSC, and 50-75 KeV at IR) than is common (20-50 KeV) for solar cell implantation. The reason for targeting[18]) for the deeper implant of 0.8μ to .23μ is to minimize junction shorting due to sintering of the metallization grid for the initial cell evaluation. Further work will be done in the future to optimize (reduce) the junction depth vs. metallization sintering to enhance the cell short wavelength response. Control wafers using the standard lower acceleration voltages for ion implantation are being processed to act as controls for evaluation of the laser anneal samples. Pre-anneal and post-anneal junction depth will be verified by SIMS analysis. None of the test samples were implanted with boron on the back since all will be destroyed during junction evaluation. Results from these tests will be available in the next reporting period along with relative junction movement data.

Prototype metal masks for edge shadowing during ion implantation in the LMSC Acceleration MP-400 have been fabricated to form planar junctions, and removes the need for subsequent edge etch.

Runs are presently in progress at IR using the Extrion-200 to implant ^{31}P at 50 and 75 KeV at a fluence of 1 x 10^{15} ions/cc. These are to be used for laser annealing and cell processing. LSS Range Statistics indicate a projected range for 50 KeV ^{31}P implants of .0795μ. In view of the relative absence of appreciable impurity re-distribution of laser annealed implants, this doping impurity penetration has been considered minimal for this investigation, as compared to normal implantation processing of 25 KeV accompanied by furnace annealing. Parameters recorded to date are shown in Table 1.

Table 1

Parameters of Ion Implanted Wafer Runs

PARAMETERS	RUNS (IR)					
	IR-1	IR-2	IR-3	IR-4	IR-5	IR-6
Species	^{31}P	^{31}P	^{31}P	^{31}P	^{31}P	^{31}P
Ion Fluence (1×10^{15})	1.	1.	1.	1.	1.	1.
Voltage (KeV)	50.	50.	50.	75.	75.	75.
Beam Current (μa)	50.	50.	50.	50.	50.	50.
V/I (anneal)	15.5	17.0	(1)	10.9	19.	(1)

(1) Held for laser anneal

A furnace anneal in nitrogen was performed at 900°C for 15 minutes on samples IR-1 and IR-4 and at 1000°C for 30 minutes on samples IR-2 and IR-5. The 900°C - 15 min. anneal is considered comparable, although slightly high, to a normal solar cell diffusion-time cycle. The 1000°C - 30 min. anneal is considered a generally effective process for 100% ion activation for (100) oriented silicon.

Surface resistivity (V/I) measurements were made on the furnace annealed test wafers and compared to a standard diffused solar cell (V/I=12). As shown in Table 1, the test wafer readings ranged from 10.9 to 19.0 comparing favorably with the standard solar cell. All measurements were made using a standard 4 point probe.

3.2.3 Laser Annealing

Initial work was conducted in the determination of suitable lasers to perform this operation. As reported in Section 3.1.3, the most promising candidates consist of Argon, Ruby or YAG lasers with wavelengths of .5 μm, .694 μm and 1.06 μm, respectively. Q-switched ruby lasers capable of delivering approximately 15 joules of energy are manufactured by Apollo Lasers, Los Angeles, CA, Hadron, Inc., Korad Division, Santa Monica, CA, and Holobeam Laser, Inc., Orlando, Florida. These companies were contacted and program requirements reviewed. Considerable interest, with promise of full cooperation, for this study was given by Korad Management/Engineering personnel. Korad has two ruby lasers, the K2 and K1500, which appear to be well suited for the particular requirements of laser annealing. These lasers will be available to LMSC/IR for evaluation at the Korad application laboratory. In addition, the facilities of HDE Systems, Inc., Mountain View, CA will be utilized to evaluate 15 and 50 joule Sylvania and Raytheon YAG lasers, respectively.

Data has been obtained from Dr. J. F. Gibbons, Professor, Stanford Electronics Lab., relative to his utilization of a Spectra physics Argon Laser for annealing of 100 KeV arsenic implants in silicon. Additional information on high powered Argon lasers from Spectra Physics and Coherent Radiation is forthcoming.

3.2.4 Screen Printing

Activity during this reporting period was limited to the making of screens using a 320 mesh for 2 and 3 inch diameter cells. The front contact pattern selected is similar to that of cells used by Lockheed in previous fabrication of panels. The pattern was so selected to conform to the existing Lockheed Module Assembly System. These screens are now on hand. Other work is underway in the redesign of the front contact pattern to increase the active photo area to greater than 90%.

Silver pastes to be used in the fabrication of cells for our investigation consist of: DuPont 7095 and 4021, Ag and Ag-Al paste, respectively; Owens-Illinois 6105, 6109 and 6150, Ag, Ag-Al and Al, respectively.

3.2.5 AR Spray Coating

The Zicon Autocoater has been installed in the Manufacturing Research Electronics Technology Lab with exhaust, electrical and plumbing hook-ups completed. Only the spray booth module was fully hooked up, and should be adequate to fulfill the requirements of this contract. Figure 14 shows the unit as installed. The spray gun is mounted overhead within the spray chamber, with the spray directed veritically. The spray gun can be automatically traversed over a pattern of approximately 17" x 22", with a traverse speed of -20 inches per second, continuously adjustable.

Contacts by IR with Dow Corning, Midland, Michigan, has revealed the availability of a new coating material known as ARC, which perhaps can be used as a carrier and binder for Ta_2O_5 coatings. Dow developed the ARC coating for its high abrasion resistance properties and when cured, forms a SiO_2 matrix structure which can be applied by the Zicon Spray Coater. Samples of silicon photocells (supplied by I.R.) have been coated by Dow Corning with the ARC film (without Ta_2O_5) and are to arrive in the early part of February for evaluation.

It has been considered that with a superior and reliably reproducible texturized surface, a relatively thick, clear dielectric film, if cost-effective, might be suitable as a total system. It is with this in mind, that the investigation with the Dow Corning ARC material becomes doubly interesting. The presence of small amounts of sodium (as a silicate) in this material, though it is in a stabilized chemical structure, may become a potential problem. This will be considered and investigated. Dow Corning has stated that the basic chemistry of this system can be modified to eliminate the sodium, if it becomes necessary.

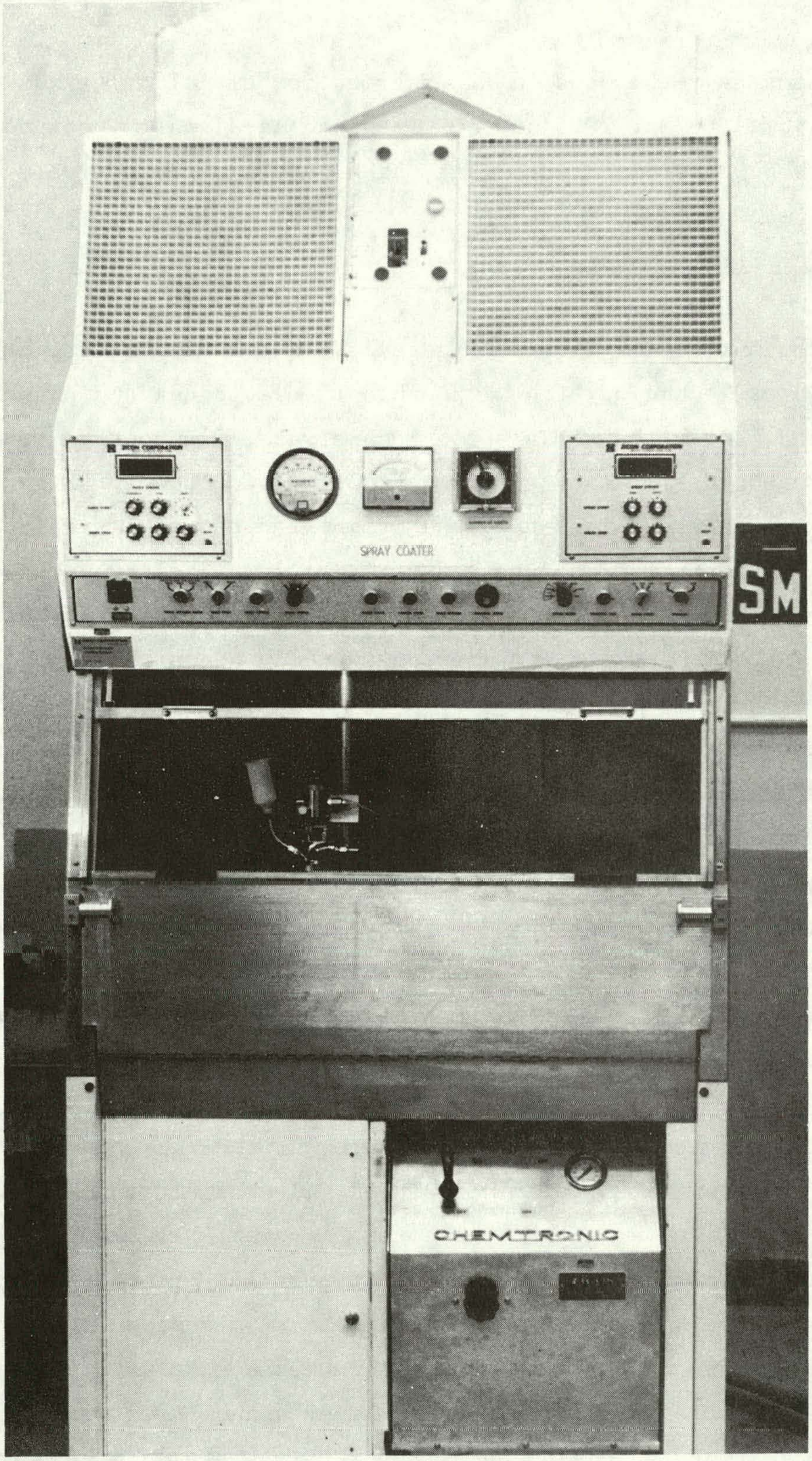


Figure 14. Zicon 10,000 Autocoater - Spray Module

Contacts have been made with Emulsitone Company and Allied Chemical regarding supplying the desired Ta_2O_5 coating material in liquid form.

A one pound quantity of Ta_2O_5 optical grade powder was ordered from Atomergic Chemicals Corporation. This will be evaluated for application in the spray coating.

Section 4
CONCLUSIONS

4.1 Texture etching utilizing a "flash-etch" step to remove saw damage, followed by a 10% NaOH solution produces acceptably etched wafers. However, the cost-effectivity of the flash etching step is in question.

4.2 Candidate methods for improving ion implantation throughput, as an adjunct to increased beam current implant machine design, include: dual beam deflection, expanded carrousel system using multiple vacuum chambers, and increased interlock stations and vacuum chambers used in conjunction with the Varian-Extrion Wayflow System.

4.3 Lasers most suitable for laser annealing are Argon, Ruby and YAG with wavelengths of .5 μm, .694 μm and 1.06 μm, respectively.

4.4 Silver paste material costs for screen printed contacts will not meet the project cost objectives unless techniques are developed which reduce the amounts utilized. Alternate materials and processes could contribute significantly.

4.5 Module assembly material costs based on high transmission glass superstrates and aluminum framing must be reduced significantly in order to meet the Project cost objectives.

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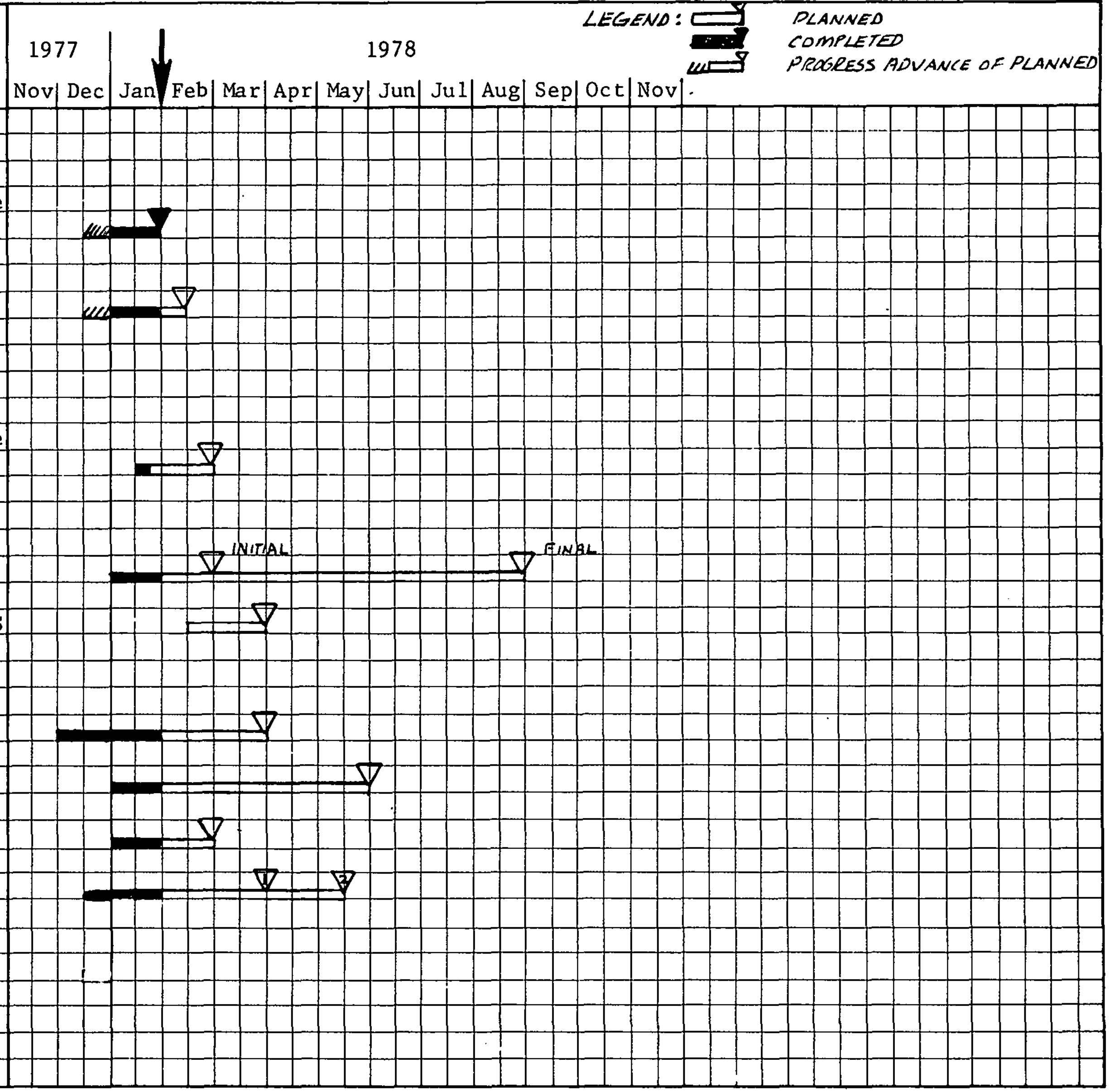
18. LSS Range Statistics for Phosphorus in Silicon

PROGRAM PLAN STATUS

Progress to date is shown in the following Program Plan Chart.

PROGRAM PLAN

MODEL	PLAN	TITLE	PREPARED BY:	DATE
		PH 2, AUTOMATED ARRAY ASSEMBLY - Contract 954898	M. Lopez	12-6-77
ISSUE NO.	REFERENCE		APPROVED BY:	DATE
	CDRL Item 2(a)			



1.0 TECHNICAL & ECONOMIC EVALUATION

a. Review texture etch, ion implant, screen print, module assembly

b. Generate new info for laser anneal & spray-on TA_2O_5 AR

2.0 PROCESS STEP DESCRIPTION

a. Review texture etch, ion implant, screen print, module assy. steps.

b. Prepare and update descriptions for laser anneal and spray-on TA_2O_5.

3.0 CRITICAL REVIEW OF PROCESS STEPS

4.0 PROCESS VERIFICATION

a. Procure materials/supplies

b. Fixtures & process dev tools

c. Texture-etch silicon wafers

d. Ion implant phos/boron

(1) Set-up equipment and determine proc parameters

(2) Process proof

PROGRAM PLAN

MODEL	PLAN	TITLE	PREPARED BY: M. Lopez	DATE 12-6-77
ISSUE NO.	REFERENCE CDRL Item 2(a)	PH 2, AUTOMATED ARRAY ASSEMBLY - Contract 954898	APPROVED BY:	DATE

4.0 PROCESS VERIFICATION (CONT)

e. Laser Anneal
- ① Equip determ and prelim assessment
- ② Preparation & evaluation of annealed cells
- ③ Process refinement

f. Screen Print Contacts
- ① Verify proc
- ② Prepare & evaluate samples

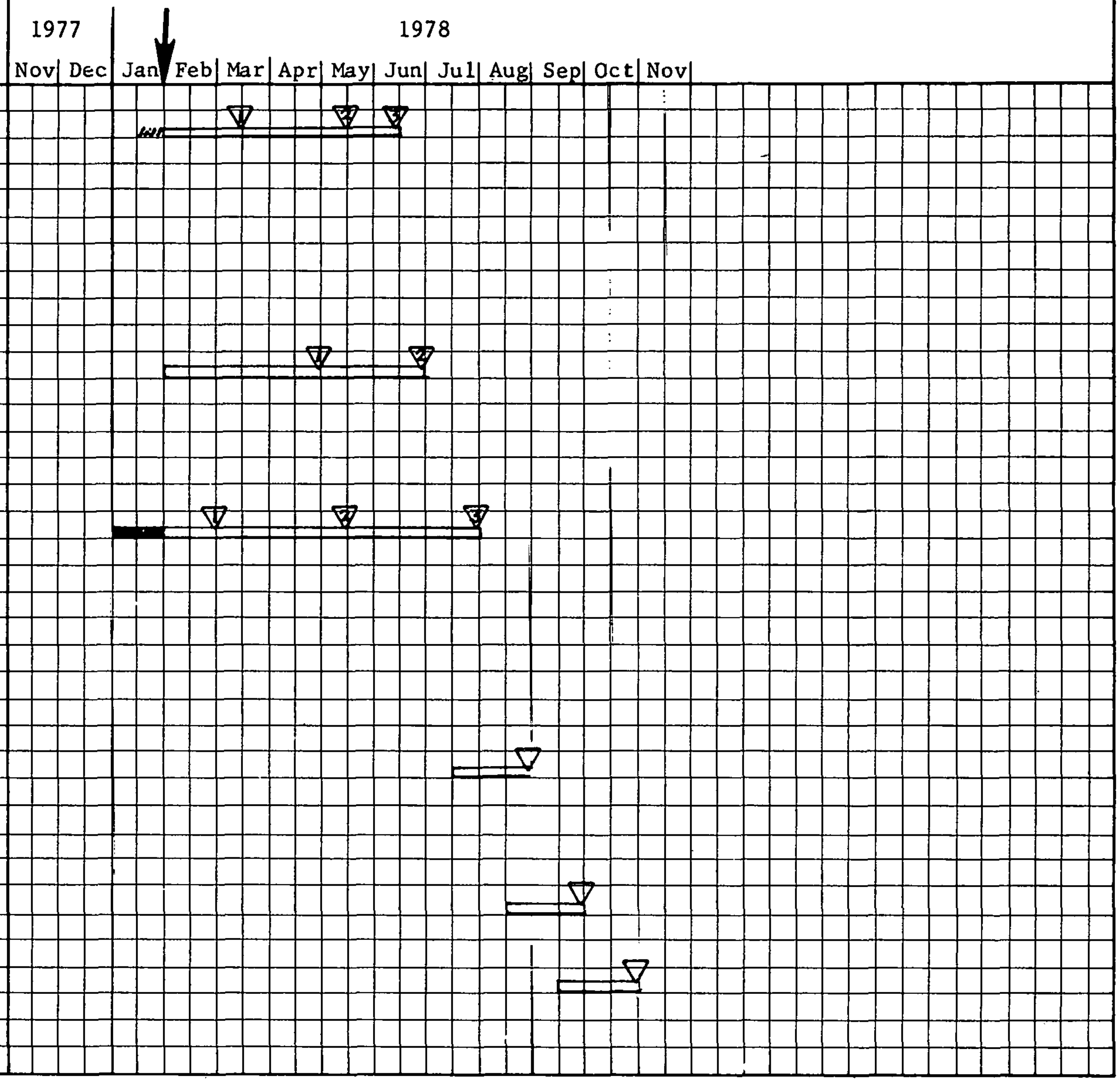
g. Spray TA_2O_5 AR Coat
- ① Equip set-up & operational
- ② Parameters developed
- ③ Process proof

h. Module assembly for process compatibility

5.0 VERIFICATION PERFORMANCE

a. Fab cells using processes verified/developed

b. Fab 2 - 41 cell modules (LMSC design)



PROGRAM PLAN

MODEL	PLAN	TITLE	PREPARED BY:	DATE
			M. Lopez	12-6-77
ISSUE NO.	REFERENCE		APPROVED BY:	DATE
	CDRL Item2(a)	PH 2, AUTOMATED ARRAY ASSEMBLY - Contract 954898		

6.0 ARRAY AUTOMATION PLAN

TECHNICAL DOCUMENTATION

a. Process dev & program plans

b. Matls, supply & process specification & procedures

c. SAMICS

d. Monthly tech progress report

e. Quarterly report

① Abstract

② Report

f. Final report

① Draft

② Approved final

g. New technology

MEETINGS AND WORKSHOPS

a. Program Review (at LMSC)

b. Project Integration (at JPL)

c. Workshop

d. Verification hardware