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PHASE 2 OF THE AUTOMATED ARRAY ASSEMBLY TASK OF THE LOW COST SILICON SOLAR ARRAY PROJECT

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Motorola Report No. 2345/1

By
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Phoenix, Arizona

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Project No. 2345

The JPL Low-Cost Silicon Solar Array Project is sponsored by the U.S. Department of Energy and forms part of the Solar Photovoltaic Conversion Program to initiate a major effort toward the development of low-cost solar arrays. This work was performed for the Jet Propulsion Laboratory, California Institute of Technology by agreement between NASA and DOE.

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1.0 ABSTRACT

A process sequence for manufacturing silicon solar cell modules was chosen for detailed study. This sequence, when automated, is expected to be capable of mass producing modules combining high efficiency, low cost, high reliability, and minimal consumed materials and waste disposal. Specific steps are:

1. Plasma etch of silicon
2. Apply wax etch stop (one side)
3. Texture etch; remove etch stop
4. Silicon nitride deposition (vacuum CVD)
5. Form metallization pattern in Si_3N_4 (contact masked plasma etch)
6. Ion implant back surface field region
7. Ion implant P-N junction
8. Thermal anneal of implant damage
9. Plate metal (front and back); solder coat
10. Test cells; interconnect
11. Encapsulate

A wax which appears to display all the characteristics necessary for use as an etch stop has been selected and tested. Plasma etching of silicon, and contact-masked plasma etching of silicon nitride, have been shown to be feasible. Compatability of simultaneous front and back plated metallization with this process sequence has been shown. Ion implantation studies have been delayed due to a longer-than-anticipated equipment installation time. SAMICS data are presented in a separate report.

2.0 INTRODUCTION

There is a high probability that flat plate solar photovoltaic modules will become a major source of electricity generation throughout most of the world, and that the silicon solar cell will be the preferred generating element. In order to provide a realistic framework on which to build an effective program of R&D and demonstration for silicon solar cell modules, a series of objectives has been established to lead to a 1986 goal of 50¢/peak watt. At this price, solar-generated electricity will be able to compete with electric power generated by any other means, provided the solar cell modules are sufficiently reliable (e.g., have a mean life of 20 years).

To reach the 1986 JPL goal will require several advancements: 1) a cheaper source of pure silicon, 2) a much more economical way of transforming the source of silicon into large, thin, (essentially) single crystal substrates having a controlled geometry, 3) an economical, large module package that will protect the interconnected solar cells it contains for at least 20 years from degradation caused by exposure to the weather, 4) an automated process sequence that produces high efficiency, reliable, cheap solar cells, tests them, interconnects them, and encapsulates them, and 5) a large market, of the order of 500 Mw/year.

When the JPL/ERDA LSSA Project started, the Motorola Solar Energy R&D Department participated in the Phase I of the Automated Array Assembly Task. The Phase I study identified a few potentially powerful process sequences for silicon solar cell production, and experimentally verified the overall consistency of the process sequence. It concluded that no basic technological innovations were necessary for solar cell fabrication or encapsulation in order to meet the long range LSSA Project goals. Detailed economic analyses were performed, based on today's technologies, and showed that it should be possible to meet the JPL cost

projections for solar panels.

The overall conclusion of the Array Automated Assembly Task, Phase I, was one of cautious optimism. The present program, for Phase 2, has as its objective the further development of specific process steps (in a specified, powerful process sequence) leading to a completely specified solar cell (and module) production process sequence. This sequence must be capable of a high degree of automation and control. A detailed economic analysis is a major part of the program to ensure that the most cost-effective approach is taken.

3.0 TECHNICAL DISCUSSION

An advanced process sequence for manufacturing silicon solar cell modules is being developed. This process is expected to be capable of producing cells with the highest cost-effective efficiency possible from any given quality of starting material. It has been concluded that maximum cost-effectiveness is enhanced when a minimum of materials is consumed in the process sequence. As a result, emphasis is placed on the minimization of consumed materials during the development of this process sequence. The two factors, high cell efficiency and minimization of consumed materials, are consistant with the third goal of high process yields achieved through well-defined process controls.
The true cost effectiveness of any product is reflected in its serviceable life, not just in its initial cost. Accordingly, attention will be concentrated on the reliability of the product manufactured by this process sequence. The goal is to maximize cost effectiveness through maximization of module operating life.

3.1 THE PROCESS SEQUENCE

The specific process sequence is outlined below:

1. Etch starting material
    a. Cz to remove saw damage
    b. Sheet, as-grown, to remove surface layer*
2. Apply etch stop - one side
3. Texture etch and remove etch stop
4. Chemical vapor deposition of silicon nitride
5. Form metallization pattern in silicon nitride
6. Ion implant back surface field region (High-low junction)
7. Ion implant front p-n junction

8. Activation anneal of implant
9. Plate metal, and solder coat
10. Cell test and solder reflow interconnect
11. Encapsulate

*(This may not be necessary with sheet produced by some processes.)

The rationale and description of each of the process steps and interactions within the process sequence are presented in this section.

3.1.1 STEP ONE: ETCH STARTING MATERIAL

The input material for this process sequence is assumed to be either 1) sliced Cz material, obtained in the as-sawed condition, or 2) a form of continuously grown silicon sheet material. In either case, the first step in the process sequence will be an etch to remove the surface layer of silicon.

For the case of the as-sawed Cz material, the sawing operation leaves a heavily damaged surface layer. This layer contains microscopic cracks and slipped regions of silicon as a result of the sawing operation. Silicon particles torn away from one region may be mechanically forced into other regions, producing an effect similar to smearing. Material worn from the saw itself, slurry particles, and/or other foreign material (e.g., contaminants) may be forcefully lodged into the silicon surface. Surface damage can propagate deeply into the silicon during subsequent high temperature processing, degrading crystalline perfection and reducing minority carrier lifetime. Also, contaminants trapped in the fine interstices of a damaged surface may diffuse into the silicon

during such high temperature processing steps, degrading lifetime as well. Below the heavily damaged surface layer is found a more lightly damaged layer, containing slip and strain, which can contribute to the formation of dislocations and dislocation networks upon heating. Such damage sites may act as recombination centers and also have an adverse effect upon minority carrier lifetimes. Further, such damage may be interactive with processing steps of junction formation in a non-uniform and uncontrollable manner. Accordingly, major damage from sawing must be removed in order to achieve satisfactory process control, and yield of solar cells with uniform cell efficiency.

Continuously grown silicon sheet material, such as is grown by the edge-defined film-fed growth (EFG) technique or by the ribbon-to-ribbon (RTR) technique, may also require surface etching. Reports, both formal and informal, by several companies with major programs in this area, have indicated that improved solar cell efficiencies were obtained on EFG material which had been surface etched rather than utilized in the as-grown condition. The improvement of solar cell efficiency utilizing EFG ribbon following removal of the surface layer has been postulated to be a result of placing the p-n junction in a region containing a dramatically lower concentration of either oxygen or carbon (or both) than exists in the as-grown surface layer. If the cause is, in fact, removal of an oxygen-rich layer from the surface, any as-grown sheet material may be improved by surface etching. Although evidence from EFG technology indicates that a surface-etching step is desirable for as-grown silicon sheet material, it is not known whether all (or indeed any) of the silicon sheet-growth techniques under investigation need to have such a surface layer removal. If silicon sheet with good surfaces is achieved in the future, then this first step can be eliminated from the process sequence.

A smooth surface on the silicon material after etching is desired for all material in order that the back surface of a solar cell be flat and thus allow utilization of back surface total internal reflection.

Surface etching of silicon can be achieved by wet chemical techniques. Wet chemistry etching is a proven technology that is widely utilized in the semiconductor industry. Wet chemistry, however, consumes volumes of materials such as acids and deionized (DI) water, and thus is inherently limited in cost to the price of these consumed materials. Further, a disposal problem exists for waste acids, adding to the cost of wet chemistry etching.

An alternative to wet chemical etching is plasma etching of the silicon surface. In plasma etching technology, the silicon is placed in a reduced pressure chamber filled with low partial pressures of gases such as CF_4 and O_2. The CF_4 and O_2 are ionized with an RF field, forming an energetic plasma of ionized fluorine and oxygen which will attack and etch silicon. Reaction products follow the gas stream and are swept from the reaction chamber, allowing continuous etching to occur. Consumed materials costs, and waste disposal problems, are minimal compared to wet chemistry etching. The plasma etching process has demonstrated proven feasibility at Motorola, but requires further development for large scale production.

The first step in the solar cell process sequence under development by Motorola, thus, will incorporate plasma technology for etching the starting silicon material. If a technique for growing silicon ribbon with high surface quality is developed, this step may be eliminated.

3.1.2 STEP TWO: APPLY ETCH STOP

Following the formation of smooth surfaces from the first step (silicon etching), one side of the silicon is texture etched while maintaining the smooth

surface on the opposite side of the substrate. In order to achieve this, one side of the silicon must be masked against the texture etchant. A sprayed wax resist is under study for this process step.

Masking of one side of a silicon sheet can be accomplished by a variety of ways, including application of tape; photoresist spinning or spraying; and spinning or spraying other types of resists. Since masking of one side for texture etching requires only blanket coverage, a very simple surface covering technique may be used. Such a masking operation could result in consumption of materials that do not appear in the final solar cell; to minimize costs of materials, energy usage, and waste disposal, it would be desirable to utilize a recyclable masking material. As a result, Motorola is studying the use of a sprayed wax resist. The wax would be dissolved in a solvent, sprayed upon one side of the silicon, and the solvent evaporated from the wax, leaving a wax coating upon one side of the silicon. The evaporated solvent would be reclaimed, at least in part, by condensation. The wax could then be subsequently removed in the solvent. Both the wax and solvent can, thus, be continually recycled, reducing consumed materials to a very samll level.

3.1.3 STEP THREE: TEXTURE ETCH AND REMOVE ETCH STOP

The silicon is now texture etched on one side. Texturing is an anisotropic etching process, which has been developed to the point where it is now a simple, well-developed, and controllable step. The process incorporates a simple bath-etching technique which requires minimal capital investment.

Texture etching of (100) Cz wafers is a proven technology and has been incorporated in production process sequences at Motorola to produce high efficiency solar cells.

As-grown silicon sheet material may be oriented with surfaces other than (100). If the silicon sheet is (large grain) polycrystalline, several crystallographic orientations will be present. Accordingly texture etching will produce different results on these different orientations. If as-grown sheet can be seeded to grow (100) surfaces, processing should be identified to that developed for (100) Cz wafers. Some as-grown sheet has been shown to have a structure of (100) surfaces and <112> axial orientation; texturing of such surfaces has been reported.

Over the next several years, each promising silicon sheet growth technique will be investigated with respect to its capabilities for producing material with a specific surface orientation. It is assumed here that sufficient orientation control will be obtained so that some texture etching can be performed effectively. If this proves not to be the case, then either sheet-grown silicon will suffer an inherent disadvantage, or effective texturing techniques must be found for the grain orientations found on sheet-grown silicon surfaces.

Following texture etching, the wax resist is removed by dissolution in the original solvent carrier as discussed in Section 3.1.2.

To ensure that all wax and solvent residue are removed from the silicon surfaces, the silicon must be cleaned further. Two choices are possible: 1) wet chemistry cleaning or 2) plasma cleaning. Again, plasma cleaning is preferred. This cleaning is performed in an oxygen-rich plasma (air is adequate) and is identical to a process widely utilized throughout the semiconductor industry to remove photoresist. (The accepted terminology for an oxygen plasma removal of films which are primarily organic is "ashing".)

3.1.4 STEP FOUR: CHEMICAL VAPOR DEPOSITION (CVD) OF SILICON NITRIDE

A layer of silicon nitride is deposited on both sides of the silicon sheet simultaneously. This is accomplished in an isothermal chamber at a pressure of less than one atmosphere, and constitutes a well-developed process. Film parameters, such as thickness and index of refraction, are highly reproducible and readily controlled.

The silicon nitride layer is an excellent example of process synergism, serving several functions in the process sequence and in the final cell. The silicon nitride layer acts as a partial ion implantation mask to tailor concentration profiles, and, being amorphous, scatters the ion beam to reduce ion channelling effects. The silicon nitride serves as a plating mask during metallization, and acts as a passivant over the p-n junction. The silicon nitride layer covering the back surface serves as a convenient means for providing a reflecting back surface by masking metal deposition. As has been shown experimentally, palladium silicide, nickel silicide, and perhaps other contacts, if they form ohmic contact to silicon, are light absorbing. Masking the back from metal deposition, thus, leaves a well defined silicon surface for reflection. Total internal reflection will occur due to the large angle of incidence at the back surface resulting from refraction at the textured front surface. Finally, and most important, after serving its process-facilitating role, the silicon nitride layer on the front surface acts as the antireflection coating over the completed cell surface.

Silicon nitride has an index of refraction near 2.0. While this value is lower than optimum for plane front surface cells, it performs as an excellent antireflection coating on textured surfaces. Further, silicon nitride is the best known p-n junction passivant in the semiconductor industry and as a result

is widely used in silicon device and integrated circuit production. Silicon nitride has proven particularly beneficial as a passivating layer for silicon devices and integrated circuits that are encapsulated in non-hermetic (e.g., plastic) packages; in such cases the silicon component is in a package environment that approximates the one in which silicon solar cells appear.

3.1.5 STEP FIVE: FORMATION OF METALLIZATION PATTERN IN SILICON NITRIDE

The next step in the proposed process sequence is to pattern the silicon nitride layers on both front and back surfaces of the silicon substrate with the desired metallization pattern. While this process step may be performed by photolithographic techniques, a novel plasma technique is proposed.

Photolithographic techniques and equipment are now available for sequentially coating photoresist on both sides of a silicon sheet, simultaneously exposing a pattern on both sides of the sheet, and developing these patterns to allow selective etching of the nitride. Photoresist is, however, an expensive consumable material which requires not only the steps mentioned above, but also the steps of removing the hard resist and cleaning the silicon after the dielectric pattern has been etched.

Plasma etching can be utilized to etch silicon nitride. Masking to achieve selective pattern etching can be done through the use of photoresist, but the undesirable features discussed above are still fully applicable.

Gases used in plasma etching of silicon nitride do not attack some metals, such as aluminum. Further, aluminum in contact with, or in close proximity to, a silicon wafer will mask plasma etching behind it. An aluminum mask, containing the desired cell metallization pattern, thus, may be mechanically placed over the wafer, and the desired pattern formed in the silicon nitride by exposure to the

appropriate plasma. The wafer can, in fact, be placed between two such masks, and patterns simultaneously formed in the silicon nitride by plasma etching on both sides of the wafer. Only the etchant gas is consumed, a tremendous advantage in materials usage over photolithography.

3.1.6 STEPS SIX AND SEVEN: ION IMPLANTATION OF FRONT AND BACK JUNCTIONS

Dopants for forming the metallurgical p-n junction in the textured front surface and the back surface field high-low junction in the smooth back surface are ion implanted into the silicon following silicon nitride patterning. There is broad industrial agreement that junction formation in future solar cells will be done by ion implantation, assuming that advanced reliable ion implantation equipment will be developed to supply sufficiently high ion beam currents to allow increased throughput over today's existing equipment. Such advanced equipment appears completely feasible, based on projections of ion implanter manufacturers.

In this process sequence, the front surface dopant used to form the p-n junction is implanted through the silicon nitride under conditions such that the peak as-implanted dopant concentration is very near the dielectric-silicon interface. (The stopping powers of silicon nitride and silicon are similar, but not equal.) The distribution of as-implanted ions into any given material is approximately Gaussian in nature. If the peak concentration of the distribution occurs at the dielectric-silicon interface, approximately one-half of the dopant is situated in the silicon and the other one-half is in the dielectric. Having the peak dopant concentration at the silicon surface is desirable in that the doping decreases monotonically towards the p-n junction, creating an electric field away from the surface and thus aiding in carrier collection at the p-n junction.

Ions implanted along the major crystallographic directions in a crystalline material will penetrate much further than those implanted in other crystallographic directions, since the major directions are more open to ions, i.e., present channels for the ions. The resulting deeper penetration is called channelling. The silicon nitride surface layer, being amorphous, acts as a moderator and scattering medium for implanting ions, minimizing channelling effects and maintaining a uniform shallower junction profile.

Openings in the silicon nitride resulting from the (previous) metal contact patterning step are ion implanted under different conditions than the areas under the silicon nitride. First, since there is no silicon nitride to absorb ions, dopant concentration in the exposed silicon is approximately twice that in the dielectric-covered regions, and the peak concentration is deeper than in the dielectric-covered regions. Second, since there is no dielectric layer to cause scattering, some further penetration due to channelling can be expected. Following implant activation (discussed in the next section) the p-n junction beneath the openings in the silicon ntiride is deeper than the p-n junction under the silicon nitride. This additional junction depth under the metal contact is desirable to allow formation of strongly adherent contacts by reaction with the silicon without penetration to (and thus degradation of) the p-n junction by the metal.

Ion implantation, being a directional doping process (as compared to isotropic doping from a diffusion source) has a unique advantage when applied to textured surfaces. If the ion beam is normal to the plane of the wafer, the beam will be at a large angle to the surfaces of the (microscopic) textured pyramids. The range of an ion into silicon is defined as the (average) linear thickness of silicon through which it passes before coming to rest. Since the ion beam enters a textured silicon surface at an angle to the planes of the

pyramid surfaces it stays closer to the actual silicon surface than its penetration depth, even allowing for the scattering effects of the silicon nitride layer. The resulting junction depth, as measured perpendicular to the faces of the pyramids comprising the textured surface, is less than would be seen for implantation into a plane surface.

Ion implantation into the back surface of a solar cell to form the back surface field has features similar to those characterizing implantation into the front surface. In this case, however, the surface is smooth. Implantation is performed at a different acceleration voltage since a different doping species is being used and since the implant beam incidence is normal to the smooth silicon nitride surface, rather than at a large angle such as for textured pyramids.

It is not known at this time if there is any strong preference as to which implant, the front surface or the back surface, should be performed first. While this can be empirically determined, it has no effect on the fundamental process sequence presented here.

The ion implantation process can be readily used to give either a planar or a passivated p-n junction. The ion beam can be mechanically masked on the first implant to give a planar p-n junction. If the edges of the silicon are protected during the preceding silicon nitride patterning step such that silicon nitride remains around the periphery of the silicon wafer, a passivated p-n junction can be achieved even by implanting completely to the edge of the silicon (i.e., no physical masking). Since the ion beam is collimated, it is virtually impossible to obtain a region implanted from both the front and back directions such that an n+ - p+ junction could be formed. Ion implantation, thus, can allow utilization of the entire silicon front surface for the solar cell p-n junction, while still achieving a silicon nitride passivated p-n junction.

3.1.7 STEP EIGHT: ACTIVATION ANNEAL OF IMPLANT

Following ion implantations, the silicon lattice is heavily damaged and the implanted dopant ions are, for the most part, electrically inactive. An annealing step must be performed in order to both repair the silicon damage and to electrically activate the dopant ions. Annealing can be performed in a standard resistance-heated furnace. This technique is a proven technology utilized effectively throughout the semiconductor industry. It has been utilized in solar cell fabrication.

3.1.8 STEP NINE: PLATE METAL AND SOLDER COAT

Under contract DOE/JPL/954689 the use of a plated metallization system in which palladium silicide, Pd_2Si, is the electrical and mechanical contact to the silicon, is being developed. The palladium silicide is then covered with electroless nickel to form a solderable surface which, at the same time, is strongly adherent to the palladium silicide. Finally, the nickel layer is solder coated to achieve both the desired metallization conductivity and a soldered surface for subsequent reflow during interconnection. Developments under the parallel contract will be incorporated into this program.

This metallization system has proven feasibility and is currently being utilized as metallization on cells in commercially available modules.

It is expected that this metallization system will prove to be extremely reliable in terrestrial service. Palladium silicide has been used in place of platinum silicide as part of the silicon integrated circuit (and device) beam-lead metallization system in order to simplify processing for that system. (The beam-lead metallization system is considered the most reliable of all for hi-rel system applications.) Palladium silicide contacts are, by themselves, moisture

resistant. For example, there is no observable change in any property after a long boil in deionized water. The resistance of these contacts to corrosive ambients and electrochemical reactions in service, (i.e., with nickel cap and solder overcoat), while not yet thoroughly tested, appears very optimistic.

Palladium and nickel metallization layers are deposited from plating baths. A first , an extremely thin layer of palladium is plated from an immersion bath, covering exposed silicon surfaces only; plating does not occur on the silicon nitride. The palladium layer is heat treated to form a very thin layer of Pd_2Si, which may not be completely continuous. This thin Pd_2Si layer, formed by heat treatment of the immersion plating, serves to activate the plated areas so that the subsequent plating will occur in a uniform and controllable manner. A second plating of palladium from an electroless palladium bath is then formed over the Pd_2Si. This layer is thicker than that deposited from the immersion bath. The new layer is now reacted to form a continuous layer of Pd_2Si in the desired contact areas.

Several features of the Pd_2Si layer must be noted at this time. First, when Pd_2Si is formed, it is produced primarily by the solid state diffusion of silicon into the palladium layer, with little or no palladium diffusing into silicon ahead of the Pd_2Si - Si interface. Metallic palladium ions, thus, are limited to approximately the region of the Pd_2Si. This allows the formation of Pd_2Si over very shallow p-n junctions without degradation of the p-n junction characteristics. Second, Pd_2Si has low contact resistance and excellent mechanical adherence to silicon. In addition, the Pd_2Si layer should act as a physical barrier to the migration of other metallic impurities into the p-n junction area. Since a nickel layer is utilized for soldering, this barrier feature is highly important for the very shallow p-n junctions that are utilized in high efficiency solar cells.

Following the second sinter to form Pd_2Si, the cell metallization areas are plated with electroless nickel. This layer has excellent adherence to Pd_2Si and is easily solderable. The entire solar cell is then solder dipped to coat all metallization areas with a thick layer of solder.

The metallization process utilizes only chemical hoods and plating baths for the formation of metal contacts on both sides of the wafer simultaneously. The bulk of the metal conductors is composed of solder, which is relatively inexpensive compared to other conductor metals for solar cells.

3.1.9 STEP TEN: CELL TEST AND SOLDER REFLOW INTERCONNECT

Following solder coating, the solar cells are tested and interconnected. Motorola has developed a flexible circuit interconnection scheme utilizing a laminated conductor and insulating dielectric sheet; presently utilized are laminated copper and kapton. The copper can be patterned to incorporate any series, parallel, or series-parallel cell interconnection scheme desired. Tabs are cut in the laminate for contact to the top surface of the solar cell in such a manner as to obtain multiple contacts to each cell and to insure minimum stress upon the interconnection. The back cell contact is a direct solder contact from the cell back surface metallization to the copper layer. All contacts are made simultaneously by solder reflow, minimizing labor content in interconnection.

3.1.10 STEP ELEVEN: ENCAPSULATION

Encapsulation is necessary to support and protect the interconnected solar cells. Accordingly, it will play a very important role in module reliability as well as in the performance of the interconnected cells.

Major failure modes for modules are expected to be related to the solar cell interconnections. It is probable that, until there is sufficient evidence that an interconnected group of cells can meet a greater than 20 year MTBF reliability criterion without any encapsulation, the cells must be encapsulated in such a way as to offer a considerable degree of protection from the environment if 20 year MTBF is to be achieved. (Indeed, the degree of reliability required for low cost per watt-hour modules is so high that it will probably be best accomplished by incorporation of high reliability concepts in both metallization/interconnect and encapsulation.) Such overall protection requires both front and back protection for the cells with a material impervious to moisture and other contaminants, and, most important, a high quality edge gasket having excellent sealing properties. The front protection must be transparent and have proven terrestrial environment reliability. The back plate may or may not be transparent, must have good thermal conduction, and also have proven terrestrial reliability. Together, the two must provide structural support for module handling and environmental mechanical stress such as wind loading. Glass meets all requirements for both front and back, except for good thermal conductivity for the back. However, sufficient glass thickness to provide structural support is heavy, costly, and thermally inefficient, unnecessarily increasing the operating temperature of the cells within the module. A glass front cover and a steel back plate is the basis of the encapsulation scheme utilized in this study.

Within the protecting glass cover and steel back plate, the solar cells must be effectively coupled optically through the front surface and efficiently connected thermally to the back plate. (Thermal connection to the front surface is also necessary in order to minimize cell operating temperatures.) The volume surrounding the interconnected cells is, thus, filled with a silicone gel which is optically clear, coupling the cells to the front surface both optically and

thermally, while providing a good thermal path from the cell interconnection to the steel back. The silicone also acts as a secondary barrier to moisture and contamination ingression.

Additional structural strength, as well as a seat for location of the primary ingression barrier, is provided by a steel bezel which overlaps both the steel back plate and the glass cover. The regions of overlap provide the primary seal for the module, utilizing a formed-in-place gasket.

The encapsulation, thus, is provided by a glass cover, a steel back and bezel, a silicone gel surrounding the interconnected cells, and a formed-in-place gasket at the module perimeter. Physically, the encapsulation step starts with assembly of the glass cover, cell interconnect, and steel back. This assembly is then back-filled, under vacuum, with silicone gel, and the gel is cured to a pliable consistency. The bezel is then attached with the formed-in-place gasketing being applied around the periphery of the glass cover and steel back plate. The gasket, held in place by the bezel, is then cured to its final condition.

This process is more expensive (in that it utilizes more materials) than a single sided encapsulation system. However, with today's limited reliability experience, this added expense is probably necessary to ensure a 20 year life for solar cell modules. Further, this proposed process step is conservative in that, if it is proven to be excessively wasteful of materials in the future, a less sophisticated encapsulant scheme is easily substituted. Present implementation of a simpler encapsulation technique will neither help ensure future reliability nor establish the necessary manufacturing experience for future reliable encapsulation technology. It should be emphasized that such a sophisticated

encapsulation system is still capable of meeting the 1985 LSSA Project price goal of 50¢/watt for complete modules. Projected prices for encapsulation materials total less than $\$2/ft^2$, and, with automated assembly of 15% solar modules, the encapsulation costs will still be only about 1/3 of the total.

3.1.11 PROCESS SEQUENCE RATIONALE AND INTERRELATIONS BETWEEN PROCESS STEPS

The individual process steps of the process sequence have now been presented. Each individual step is interactive in a positive manner with the other steps to provide an optimally efficient, cost effective solar cell and module. The process sequence has been chosen from processes with proven technical feasibility, which have, at the same time, the potential of meeting the long range cost goals.

Processes have been chosen such that consumed materials are minimized and, in addition, are additive in nature, that is, utilized to build upon the cell structure (and performance) rather than being partially removed and discarded as waste materials. Where feasible, consumed materials are recycled within the process. Waste disposal is also minimized through the use of dry plasma processing where practicable, leaving texture etching as the only wet chemical step (which requires waste disposal) in the entire process sequence.

The process sequence is initiated with a dry plasma etching of the starting material surfaces. This ensures a smooth surface for the back of the cell, and also that any poor quality silicon at the surface of a wafer or ribbon, caused either by contamination or damage, is removed. The smooth back surface, in conjunction with a textured front surface, allows total internal reflection of light. This reflection, in turn, reduces the silicon thickness necessary to assure efficient light absorption within the cell necessary for high solar cell conversion efficiency. Light reflecting back to the front surface will, for the most part, be transmitted out of the cell. Longer infrared wavelengths, to which

silicon is transparent, will thus pass out of the cell without being absorbed, reducing the cell operating temperature compared with absorbing back surfaces of currently produced solar cell structures.

In order to maintain the smooth back surface during texture etching of the front surface, a wax resist is applied. This is done by first dissolving the wax in a solvent, spraying the wax solution on the wafer, and evaporating and reclaiming the solvent. Following texture etching this wax resist is redissolved in the reclaimed solvent to be recycled. Neither the reclaiming of the solvent nor the wax will be 100% efficient, of course, but the costs of consumed materials are minimized and waste disposal virtually eliminated by this process sequence.

The texture etching is a wet chemistry step. This etching is performed in an alkaline solution, with most of the chemicals consumed before bath replacement. The benefits gained from texture etched surfaces make this wet chemistry step extremely cost effective.

The textured surface, in addition to expediting the back surface reflection effects already discussed, has other profound effects on cell operation and on processing. Very shallow p-n junctions are achievable by ion implantation. The general light-trapping nature of a textured surface can increase efficiency appreciably. The textured surface also allows utilization of an antireflection coating with a somewhat lower index of refraction than would be optimum for a smooth front surface. This feature permits the use of silicon nitride with an index of refraction near 2.0 as the antireflection coating.

Silicon nitride serves many functions in addition to its effective use as an antireflection coating. It acts as a surface and p-n junction passivant, as an ion implatation moderator to allow accurate dopant profiling, while its absence

in the contact areas during implantation allows deeper junctions under the metallization. The silicon nitride also serves as a plating mask, for both front and back surfaces, allowing minimum metal consumption for metallizing both surfaces while allowing back surface reflection.

The combination of a textured front surface, and a smooth back surface with reflection occurring from its unmetallized areas, allows the utilization of thinner silicon material than could otherwise be achieved. If, for example, efficient reflection of light can be achieved from the back surface, and accounting for the increased path length of light in the silicon from refraction at the front textured surface, less than one-half of the silicon thickness is required to absorb the same amount of light as is needed for a solar cell with a smooth front surface and having no back reflection. This factor will obviously reduce the cost of input silicon by permitting use of thinner substrates to make high efficiency cells.

Patterning of the silicon nitride dielectric layer is accomplished without the use of photoresist chemicals and solvents. Further, no photoresist removal step is required, further eliminating material consumption while gaining process simplicity. The dry plasma etching technique utilizing mechanical masking also provides edge protection, if desired, allowing total areal usage of the silicon sheet while maintaining a passivated p-n junction. The masked plasma etching allows simultaneous front and back patterning of the silicon sheet, further simplifying the process sequence while optimizing solar cell efficiency and minimizing consumed materials.

Ion implantation, in addition to providing p-n junction advantages already discussed, ensures that only the desired dopant species are put into the silicon, eliminating possible incorporation of undesirable impurities into the area of the illuminated p-n junction. This aspect, as well as other inherent control features

of ion implantation, should result in a process with as excellent a distribution of solar cell outputs as the quality of the input material is capable of providing.

The only high temperature step in the process sequence is the activation anneal, and both the front surface p-n junction and the back surface high-low junction are activated simultaneously. (The silicon nitride step is considered a moderate temperature step, being performed near 725°C.)

Metallization by plating is an additive process in that metal is deposited only where it is ultimately utilized. The metallization system of palladium silicide-nickel-solder also has the potential of being an extremely reliable metallization system, allowing the 20 year reliability goal to be met or surpassed. While this is presently unproven, this metallization system may allow reduced encapsulation requirements and, thus, reduced encapsulation costs.

The interconnection scheme is versatile with respect to solar cell size and shape as well as method of cell interconnection (series, series-parallel, or parallel). Further, it has multiple contact and low electrical loss capability, while also being of low labor content now and capable of full automation in the future.

The module encapsulation approach is conservative for the sake of reliability. Future developments may ease the requirements for encapsulation, simplifying this technique at that time. Being the last step, it is the least interactive with other steps in the process sequence, and will move only in the direction of simplification, not increased complexity.

Each step of the process sequence, thus, contributes to the cell and module in several ways. Consumed materials are intentionally kept low, substituting advanced technologies for traditonally more expensive, (though technically feasible) steps. Further, the process is capable of utilizing as-grown silicon sheet material with no penalty compared to sliced Cz material.

3.2 WAX RESIST TECHNOLOGY FOR TEXTURE ETCHING

This step is designed to permit texture etching of only the front surface of the silicon substrate. While texture etching per se is not part of the technological advancement portion of this contract, the masking of texture etching on the silicon substrate is one of the technology advancement studies.

Manufacturers of waxes have been contacted to identify suitable waxes. Since texture etching is performed in a heated alkaline bath, the foremost requirement on the wax is its resistance to soponification. This greatly limits the list of potentially suitable choices.

One wax which appears suitable for masking one side of a silicon substrate while the opposite side is being texture etched has been identified. The wax is Multiwax 195-M, manufactured by Witco Chemical Company, New York. Multiwax 195-M is a microcrystalline wax which has properties suitable for this application. The melting point of the wax is 195°F (90.6°C), which is above the temperature utilized for the texture etching solution. The wax has a (high) flash point of 550°F (287.8°C) which indicates a low flammability. It has a very low vapor pressure, having no odors or fumes. It has a density of 0.78 g/cm^3 (at 115°C). The wax has shown good adhesion to wafers and has exhibited good protection from the texture etching solution. The wax does not soponify. Prices have been quoted at $0.69/lb. in small quantities and $0.57/lb. in quantities over 500 lbs. Initial tests were performed utilizing toulene as a solvent for convenience, but since toluene is ecologically unsatisfactory, further studies of solvents are underway.

3.3 PLASMA ETCHING OF SILICON AND SILICON NITRIDE

Processing of solar cells can involve a large number and variety of wet chemistry steps. These steps include such items as isotropic silicon etching

to remove saw damage or surface layers, texture (anisotropic) etching of silicon, dielectric etching, metal etching, and metal plating. Wet chemical steps may be the only viable means for achieving the desired result for some cases, such as texture etching and metal plating. In other cases, however, alternatives have been identified which may achieve the desired result while minimizing consumed materials and waste disposal requirements. Two such alternatives are the plasma etching of silicon to remove sawing damage (or other undesirable surface layers), and the plasma etching of patterns in silicon nitride without utilizing photoresist.

Plasma processing utilizes an appropriate gas (or gas mixture) at a reduced pressure, ionized in an RF field. The ions exist at low physical temperatures, but are highly energetic, representative of much higher effective temperatures. Surface processes which would normally require high temperatures can, thus, be performed at or near room temperature.

Etching of silicon in a plasma can be accomplished with a mixture of CF_4 and O_2. The plasma contains ionized fluorine and oxygen which attack and etch silicon, producing volatile reaction products which can be swept from the plasma chamber, allowing continuous etching. Plasma etching of silicon is first being investigated in a parallel plate plasma chamber. Work on this is currently underway.

Patterning of silicon nitride is also being studied utilizing plasma. In this case, only CF_4 is introduced into the plasma chamber. Plasma etching of silicon nitride has been demonstrated utilizing photoresist masking. Photoresist processing, however, utilizes many consumable materials, making it desirable to find an alternative. A new technology has been proposed for development in this study which replaces photoresist with a mechanical mask. The mechanical mask would be exactly analogous to a shadow metallization mask

for evaporation of metal contacts. The opening sizes and proximity of the mask to the solar cell surface during etching are key parameters.

Initial experiments have been performed to pattern silicon nitride by plasma etching through a mechanical mask; their success confirms the feasibility of this technology.

The initial experiments utilized a CF_4 plasma in a parallel plate reactor. A thin metal mask of molybdenum, sometimes used as an evaporation mask for metallization, was placed against a polished silicon wafer coated with silicon nitride. The pattern on the mask was reproduced in the nitride, but the nitride pattern was slightly larger than that on the mask. This is attributed to the fact that the metal mask was warped, and good contact to the wafer did not occur. Further experiments with both aluminum and stainless steel masks are scheduled to be performed.

A concern, not yet founded in fact, however, has arisen for the patterning of silicon nitride on textured substrates. For an accurate pattern replication from the mask to the substrate surface, reasonably close contact must be made. It is known that the peaks on a textured surface are fragile. Concern has arisen, thus, that peaks may be broken through contact with the metal mask. This may be especially true if the peak height on the textured surface is non-uniform.

In order to study this potential problem, a soft coating material for application to the metal mask is being considered. Such a material is intended to act as a cushion between the textured surface and the metal mask. At the same time, such a coating may also produce a better contact between the mask and substrate, reducing undercutting effects during etching. Materials currently being considered are polymer silicones which can be applied to the mask by screening.

3.4 ION IMPLANTATION

Junction formation, both the front P-N junction and the back high-low junction, will be formed by ion implantation and annealing. An Extrion high beam current ion implanter has been purchased for development of this technology. This machine has just finished being completely installed. This will cause a small delay in the experimental work for ion implantation. This delay will be compensated for later in the program with accelerated efforts in this area.

3.5 INCORPORATION OF METALLIZATION ADVANCEMENTS

Choice of the metallization process for solar cells has a major impact upon the rest of the process sequence. The impact is greatest when comparing plating and essentially all other metal application processes. Plating, a selective process of necessity, requires intimate masking of the substrate where no metal is desired. The masking must be in place and the metal pattern defined prior to plating. For other metallization methods, including evaporation and silk screening, the silicon surface is totally bare and the masking is provided mechanically by a metal or screening mask.

For maximum cell efficiency, even on textured surfaces, an antireflection coating is necessary. For such metallization methods as evaporation or silk screening, the antireflection coating is applied following metallization. The antireflection coating, in this case, must be applied at a sufficiently low temperature to avoid cell degradation through excessive metallization heating. The antireflection coating, in addition, may cover the metallization and in such a case must be selectively removed at the points of cell interconnection to assure reliable interconnection joints.

Conversely, the antireflection coating itself can be utilized as the plating mask for a plated metallization. Since no metal is on the cell surface

at the time of the formation of the antireflection coating, the limitations on deposition temperature seen for evaporated or screened metal are eased considerably. This permits the utilization of silicon nitride for this purpose. The silicon nitride also serves as a p-n junction passivant. The process sequence chosen for development, thus, incorporates a silicon nitride layer which serves as a p-n junction passivation, antireflection coating, and as the plating mask.

The metallization system is the Pd_2Si - (Pd) - Ni - solder system and is being developed on contract DOE/JPL/954689. Since this process sequence is so heavily dependent upon the plating contract work, it will, from time to time, be reported on this contract. Interactions between the metallization process step and the overall process sequence will be closely monitored and reported.

3.6 PROCESS SEQUENCE ENHANCEMENT

The process sequence under development here contains many innovative process steps. It is anticipated that some modifications to individual process steps will have interactive effects throughout the process sequence. This study is designed to present a means of identifying and reporting such modifications when they occur. No such modifications have been performed during this first quarterly report period.

3.7 VERIFICATION OF PERFORMANCE

The process sequence studied in this contract is comprised of a number of critical individual steps. Each step must be operating satisfactorily in order for the entire sequence to perform successfully. Accordingly, control

points must be identified at each process step to verify that the particular step is working properly. These in-process measurement points are presently being studied for detailed specifications.

3.8 ECONOMIC ANALYSIS

An economic analysis of the process sequence being developed is being performed by two parallel methods. The first method is to utilize the JPL Solar Array Manufacturing Industry Costing Standards (SAMICS). Accordingly, Format A data sheets have been supplied to JPL. This will, of course, be updated as new information is available. The second method is to perform a detailed process step and process sequence analysis in the same format as Motorola presented in its cost analysis study for Phase I of the Automated Array Assembly Task contract. (1)

Some of the individual process steps incorporated into the Phase II process sequence were specified in the Phase I study. The data and assumptions generated in the Phase I study are being utilized as the basis for the present cost analysis. The Phase II process sequence contains several innovative process steps which were not analyzed in Phase I. These new process steps are enumerated below:

1. Plasma Silicon Etch
2. Wax Resist Apply
3. Wax Resist Remove
4. Mechanically Masked Plasma Patterning of Si_3N_4

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(1) L. A. Grenon and M. G. Coleman, Phase I of the Automated Array Assembly Task of the Low Cost Silicon Solar Array Project, Technical Quarterly Report No. 6, DOE/JPL/954363-7, October, 1977.

Assumptions for these process steps, along with modification of previously defined process steps, are being specified in the same format as previously utilized in the Phase I cost analysis. Results of the Motorola format cost analysis will be presented in later reports.

4.0 CONCLUSIONS

Due to the early stage of the contract, few conclusions may be drawn. It does appear, however, that a wax suitable for masking texture etching has been identified.

5.0 RECOMMENDATIONS

No specific recommendations can be made at this time.

6.0 CURRENT PROBLEMS

No specific problems have occured during this report period.

7.0 WORK PLAN STATUS

The work plan is on schedule with the exception of the experimental portion of the ion implantation studies which, because of its interaction with other planned work, has resulted in the expenditure of fewer hours than planned.

8.0 LIST OF ACTION ITEMS

No items requiring unusual action have come to light during this report period.

9.0 MILESTONES

Status of the program is shown in the Milestone Chart, Figure 1.

	1	2	3	4	5	6	7	8	9	10	11	12	13
	O	N	D	J	F	M	A	M	J	J	A	S	O
STUDY I													
TECHNOLOGY ADVANCEMENT													
A. Wax Resist Technology Advancement													
B. Plasma Silicon Etching													
C. Plasma Silicon Nitride Etching													
D. Ion Implanation Technology													
E. Incorporation of Metallization Advancements from Parallel Study													
F. Process Sequence Enhancement													
STUDY II													
VERIFICATION OF PERFORMANCE													
A. Establish Verification Points													
B. Correlation of Verification Measurements													
C. Solar Cell and Module Fabrication													
D. Verification of Process Sequence Performance													
STUDY III													
ECONOMIC ANALYSIS													

Figure I - MILESTONE CHART

	1	2	3	4	5	6	7	8	9	10	11	12	13
	O	N	D	J	F	M	A	M	J	J	A	S	O
STUDY IV													
DOCUMENTATION													
1. Process Development Plan	▲												
2. Program Plan and Milestone Schedule	▲												
3. Program Review Meetings*	▲			▲			△			△			
4. Project Integration Meetings			▲				△				△		
5. JPL Workshops*										△			
6. Material, Supply & Process Specifications and Process Procedures													
7. Samics Cost Analysis				▲			△			△			△
8. Monthly Technical Progress		▲	▲		△	△		△	△		△		
9. Contractor Financial Management Report		▲	▲	▲	△	△	△	△	△	△	△	△	△
10. Status and Cost Report Summary		▲	▲	▲	△	△	△	△	△	△	△	△	△
11. Status and Cost Report		▲	▲	▲	△	△	△	△	△	△	△	△	△
12. Abstract of Quarterly Technical Report				▲			△			△			
13. Quarterly Technical Report				▲			△			△			
14. Final Report Draft												△	
15. Final Report													△
16. Baseline Cost Estimate	▲												

MILESTONE CHART (continued)

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