L. H. GOLDSTEIN
SANDIA LABS
ALBUQUERQUE,
NEW MEXICO
87115

20th MIDWEST SYMPOSIUM ON CIRCUITS AND SYSTEMS

AUGUST 15-17, 1977

Lubbock, Texas

Edited by
K.S. CHAO/R. SAEKS

TEXAS TECH UNIVERSITY

DISCLAIMER

SAND 77-6709 #C

MULTIPLE FAULT ANALYSIS IN SYNCHRONOUS SEQUENTIAL CIRCUITS BY MEANS OF VECTOR BOOLEAN DIFFERENCE

Lawrence H. Goldstein
Sandia Laboratories
Division 2142
Albuquerque, New Mexico 87115

Abstract

The Boolean difference is an elegant mathematical concept which has found significant application in the study of single faults of a stuck-at nature in combinational logic circuits. Recently, several authors have extended this technique to the analysis of multiple faults in combinational circuits. In this paper, the concept of vector Boolean difference is further extended to the analysis of multiple stuck-at faults in synchronous sequential circuits.

1. INTRODUCTION

Fault analysis in digital circuits has emerged as one of the principal research areas in fault-tolerant computing. As LSI realization of digital circuits has increased in popularity, the problem of generating fault-detection test sets for complex sequential circuits has increased in importance. Significant results have been achieved in generating tests for combinational logic circuits under the assumption that only single-fault situations can occur. However, there are cases where multiple-fault situations must be considered. Several authors[1],[2] have recently extended the Boolean difference technique to the multiple fault case. In this paper, the concept of vector Boolean difference is further extended to the analysis of multiple stuck-at faults in synchronous sequential circuits.

Treating the current state of the circuit as a pseudo-input vector and the next state as a pseudo-output vector, a vector Boolean difference technique is utilized to determine the set of input/state pairs that will produce a difference in either output or next-state between the fault-free and faulty circuits. Assuming that the fault-free and faulty circuits start in the same initial state, they must be driven by applying a sequence of input vectors to a state in which either a difference in output or next-state is evidenced. If a difference in output cannot be achieved immediately, a second sequence of input vectors must be applied in order to propagate the state difference to the output. The Boolean difference analysis can be combined with a successor tree approach to derive the required input vector sequences.

2. CIRCUIT DESCRIPTION

Consider a synchronous sequential circuit with input vector $\underline{X}(k) = [X_1(k), X_2(k),\ldots,X_m(k)]$, output vector $\underline{Y}(k) = [Y_1(k), Y_2(k),\ldots,Y_n(k)]$, and state vector $\underline{S}(k) = [S_1(k), S_2(k),\ldots,S_b(k)]$, where k is the time parameter. Each line of the circuit is labeled with a unique integer, a line numbered j having a logical value $I_j[\underline{X}(k), \underline{S}(k)]$. Assume that the initial state of the circuit is a known $\underline{S}(0)$. Then the behavior of the circuit can be described by two vector-valued Boolean functions,

$$\underline{Y}(k) = \underline{G}[\underline{X}(k), \underline{S}(k), \underline{I}(k)] \quad (1)$$

$$\underline{S}(k+1) = \underline{F}[\underline{X}(k), \underline{S}(k), \underline{I}(k)] \quad (2)$$

where the dependence of the output and next-state functions on a subset of the internal lines $\underline{I}(k) = [I_{j1}(k), I_{j2}(k),\ldots,I_{jp}(k)]$ is explicitly indicated in Equations (1) and (2).

3. FAULTY CIRCUITS

The type of fault under consideration is representable as the logical values of a group of lines in the circuit permanently stuck at one (s-a-1) or permanently stuck at zero (s-a-0). Fault situations in which lines $I_{j1}, I_{j2},\ldots,I_{jp}$ are stuck at $a_{j1}, a_{j2},\ldots,a_{jp}$, respectively, $a_{ji} \in \{0,1\}$, $i = 1, 2,\ldots,p$ are denoted $I_{j1}(s\text{-a-}a_{j1})$, $I_{j2}(s\text{-a-}a_{j2}),\ldots,I_{jp}(s\text{-a-}a_{jp})$.

Two faults, α and β, in a synchronous sequential circuit starting in an initial state $\underline{S}(0)$ are said to be "strongly equivalent" if the output and next-state functions of the circuit with fault α, $\underline{G}_\alpha$ and $\underline{F}_\alpha$, respectively, are identical to those of the circuit with fault β, $\underline{G}_\beta$ and $\underline{F}_\beta$. Strong equivalence of faults in a synchronous sequential circuit resettable to $\underline{S}(0)$ is identical to equivalence of faults in the combinational circuit derived from the synchronous sequential circuit by breaking feedback loops and considering the current state vector as a pseudo-input and the next state vector as a pseudo-output.

If faults α and β are strongly equivalent, then the tests for faults α and β are identical. Moreover, for some multiple faults, a subset of the faults may dominate the others in the set under consideration. For example, if a multiple fault $I_{j1}(s\text{-a-}a_{j1})$, $I_{j2}(s\text{-a-}a_{j2})$, $I_{j3}(s\text{-a-}a_{j3})$ is strongly equivalent to $I_{j1}(s\text{-a-}a_{j1})$, then it is necessary to test only for the presence of $I_{j1}(s\text{-a-}a_{j1})$, which is called the dominating fault. A multiple fault which contains only dominating faults is called a reduced multiple fault. From each set of strongly equivalent faults in a synchronous sequential circuit, only one reduced multiple fault need be considered for the purpose of test sequence generation.

4. BOOLEAN DIFFERENCE EXPRESSIONS FOR MULTIPLE FAULTS IN SEQUENTIAL CIRCUITS

Consider a fault involving the p internal variables $\underline{I} = [I_{j1}, I_{j2},\ldots,I_{jp}]$ simultaneously. The vector Boolean differences of output $\underline{Y}$ and next state $\underline{S}^+$ with respect to $\underline{I}$ can be defined as

$$\Omega_{j1j2\ldots jp}\,\underline{Y} = \sum_{\ell=1}^{n} {}^{\ell}G[\underline{X},\underline{S},\underline{I}] \oplus {}^{\ell}G[\underline{X},\underline{S},\overline{\underline{I}}] \quad (3)$$

and

$$\Omega_{j1j2\ldots jp}\,\underline{S}^+ = \sum_{\ell=1}^{b} {}^{\ell}F[\underline{X},\underline{S},\underline{I}] \oplus {}^{\ell}F[\underline{X},\underline{S},\overline{\underline{I}}] \quad (4)$$

where ${}^{\ell}G$ and ${}^{\ell}F$ are the ℓ^{th} components of the output and next-state vectors, respectively, and $\overline{\underline{I}} = [\overline{I}_{j1}, \overline{I}_{j2},\ldots,\overline{I}_{jp}]$. Define the residual functions of ${}^{\ell}G[\underline{X},\underline{S},\underline{I}]$ as

$${}^{\ell}G_0[\underline{X},\underline{S}] = {}^{\ell}G[\underline{X},\underline{S},0,0,\ldots,0],\ {}^{\ell}G_1[\underline{X},\underline{S}]$$

$$= {}^{\ell}G[\underline{X},\underline{S},0,0,\ldots,1],\ldots,{}^{\ell}G_\alpha[\underline{X},\underline{S}] =$$

${}^{\ell}G[\underline{X},\underline{S}]$, p-bit binary number with decimal equivalent $\alpha],\ldots,{}^{\ell}G_{2^p-1}[\underline{X},\underline{S}] = {}^{\ell}G[X,S,1,1,\ldots,1]$.

Defining the residual functions of ${}^{\ell}F[\underline{X},\underline{S},\underline{I}]$ in an analogous manner, we obtain[2]

$$\Omega_{j1j2\ldots jp}\,\underline{Y} = \sum_{i=0}^{2^{p-1}-1} \left(m_i + m_{2^p-1-i}\right) \sum_{\ell=1}^{n} \left({}^{\ell}G_i \oplus {}^{\ell}G_{2^p-1-i}\right)$$

and

$$\Omega_{j1j2\ldots jp}\,\underline{S}^+ = \sum_{i=0}^{2^{p-1}-1} \left(m_i + m_{2^p-1-i}\right) \sum_{\ell=1}^{b} \left({}^{\ell}F_i \oplus {}^{\ell}F_{2^p-1-i}\right)$$

where $m_0 = \overline{I}_{j1}\overline{I}_{j2}\cdots\overline{I}_{jp}$, $m_1 = \overline{I}_{j1}\overline{I}_{j2}\cdots I_{jp},\ldots,$ $m_{2^p-1} = I_{j1}I_{j2}\cdots I_{jp}$. Define a combinational test as an input/state vector which, when applied to the combinational circuit derived from the sequential circuit as indicated in Section 3, produces a difference in output or next-state between the fault-free and faulty circuits. To compute the complete set of combinational tests, single through p^{th}-order on the p lines $j1j2\ldots jp$, we must

compute the vector Boolean differences of the output and next-state functions with respect to all 2^p different combinations of the p variables $I_{j1}I_{j2}\cdots I_{jp}$.

Theorem[2]: Consider the combinational logic circuit which results from a given synchronous sequential circuit by regarding the current state as a pseudo-input and the next-state as a pseudo-output. The vector Boolean functions which describe the output and next state in terms of input, current state, and internal line values are $\underline{Y} = \underline{G}[\underline{X},\underline{S},\underline{I}]$ and $\underline{S}^+ = \underline{F}[\underline{X},\underline{S},\underline{I}]$, where $\underline{I} = [I_{j1},I_{j2},\ldots,I_{jp}]$. The complete set of combinational test vectors, t, to detect all possible fault situations from single through p^{th} - order on the p lines j1j2...jp is

$$\begin{aligned}\alpha[I_{j1},I_{j2},\ldots,I_{jp}] = \{t|&\Omega_{j1}\underline{Y} + \Omega_{j1}\underline{S}^+ + \Omega_{j2}\underline{Y}\\ &+ \Omega_{j2}\underline{S}^+ + \ldots + \Omega_{jp}\underline{Y}\\ &+ \Omega_{jp}\underline{S}^+ + \Omega_{j1j2}\underline{Y} + \Omega_{j1j2}\underline{S}^+\\ &+ \ldots + \Omega_{j1j2\ldots jp}\underline{Y}\\ &+ \Omega_{j1j2\ldots jp}\underline{S}^+ = 1\}\ .\end{aligned}$$

Corollary: The complete set of combinational test vectors to detect the specified multiple fault $I_{j1}(\text{s-a-}a_{j1})$, $I_{j2}(\text{s-a-}a_{j2}),\ldots,I_{jp}(\text{s-a-}a_{jp})$ on the p lines j1, j2,...,jp is

$$\begin{aligned}\alpha[&I_{j1}(\text{s-a-}a_{j1}),\ I_{j2}(\text{s-a-}a_{j2}),\ldots,I_{jp}(\text{s-a-}a_{jp})]\\ &= \{t|\ I_{j1}(\bar{a}_{j1})\ [\Omega_{j1}\underline{Y} + \Omega_{j1}\underline{S}^+]\\ &\quad + I_{j2}(\bar{a}_{j2})\ [\Omega_{j2}\underline{Y} + \Omega_{j2}\underline{S}^+]\\ &\quad +\ldots+ I_{jp}(\bar{a}_{jp})\ [\Omega_{jp}\underline{Y} + \Omega_{jp}\underline{S}^+]\\ &\quad + I_{j1}(\bar{a}_{j1})\ I_{j2}(\bar{a}_{j2})\ [\Omega_{j1j2}\underline{Y} + \Omega_{j1j2}\underline{S}^+]\\ &\quad +\ldots+ I_{j1}(\bar{a}_{j1})\ I_{j2}(\bar{a}_{j2})\ldots I_{jp}(\bar{a}_{jp})\\ &\quad [\Omega_{j1j2\ldots jp}\underline{Y} + \Omega_{j1j2\ldots jp}\underline{S}^+] = 1\}\end{aligned}$$

where

$$I_{jk}(a_{jk}) = \begin{cases} I_{jk} & \text{if } a_{jk} = 1\\ \bar{I}_{jk} & \text{if } a_{jk} = 0\end{cases}$$

Consider the fault on the p lines j1j2...jp of decimal equivalent π. That is, $(a_{j1}a_{j2}\cdots a_{jp})_2 = \pi_{10}$. If the circuit is in a detecting state for fault π, an input can be applied that will produce a difference in output between the fault-free and fault-π circuits. Let Σ_π^* be the set of detecting states for fault π. If $\Sigma_\pi^* = \phi$, input/state pairs may exist that will cause a difference in next state between fault-free and faulty circuits. States belonging to these pairs are called diverging states for fault π and form the set Σ_π^+. The difference in state must be propagated to an output in order for the fault to be detected.

5. DETECTING FAULT π

Given that the initial state of both fault-free and faulty circuits is $\underline{S}(0)$, the problem is to generate a sequence of input vectors that will detect fault π. If $\underline{S}(0) \in \Sigma_\pi^*$, we are guaranteed that a sequence of length 1 exists. If $\underline{S}(0) \notin \Sigma_\pi^*$, we must either drive the circuit to a state in Σ_π^* or drive the circuit to a state in Σ_π^+ and propagate the resulting difference in state between the fault-free and faulty circuits to an output. A successor tree with root $\underline{S}(0)$ in which are recorded the outputs and states of both fault-free and faulty machines produced by various sequences of input vectors, when combined with the results of a Boolean difference analysis of the form presented in Section 4, will yield an efficient means for generating test sequences for faults in a given synchronous sequential circuit.

6. CONCLUSIONS

It has been demonstrated that the Boolean difference method can be effectively utilized in the synthesis of test sequences for multi-output synchronous sequential circuits. Boolean difference equations provide complete sets of combinational tests for the circuit derived from a given sequential circuit by treating the current state as a pseudo-input vector and the next-state as a pseudo-output vector. When this information is combined with a successor tree technique for treating the sequentiality of the circuit, it becomes a straightforward procedure to derive test

sequences for synchronous sequential circuits.

REFERENCES

(1) C. T. Ku and G. M. Masson, "The Boolean Difference and Multiple Fault Analysis," IEEE Trans. on Comput., Vol. C-24, No. 1, Jan. 1975, pp. 62-71.

(2) S. R. Das, P. K. Srimani, and C. R. Datta, "On Multiple Fault Analysis in Combinational Circuits by Means of Boolean Difference," Proc. IEEE, Sept. 1976, pp. 1447-1449.

BIOGRAPHY

Lawrence H. Goldstein

He received the B.E. degree from Cooper Union, New York, in 1973, and the M.S.E., M.A., and Ph.D. degrees in electrical engineering from Princeton University, Princeton, New Jersey, in 1974, 1975, and 1976, respectively. He is currently a Member of the Technical Staff in the Computer-Aided Design Division of Sandia Laboratories, Albuquerque, New Mexico.

During the summers of 1970 and 1971, he was employed in the Instrumentation Division of Brookhaven National Laboratory, and during the summer of 1972, he worked on solid state devices at the Health and Safety Laboratory, New York, New York.

Dr. Goldstein is a member of Tau Beta Pi and Eta Kappa Nu.