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AUTOMATED ARRAY ASSEMBLY

Phase 2

Quarterly Technical Progress Report, Fourth Quarter 1977

By
Bernard G. Carbajal

MASTER

January 1978

Work Performed Under Contract No. NAS-7-100-954881

Texas Instruments Incorporated
Dallas, Texas

U.S. Department of Energy

Solar Energy

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AUTOMATED ARRAY ASSEMBLY
PHASE 2

Texas Instruments Report No. 03-77-56

Quarterly Technical Progress Report
Fourth Quarter 1977

Bernard G. Carbajal

January 1978

JPL Contract No. 954881

Texas Instruments Incorporated
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The JPL Low-Cost Silicon Solar Array Project is funded by DOE and forms part of the DOE Photovoltaic Conversion Program to initiate a major effort toward the development of low-cost solar arrays.

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TABLE OF CONTENTS

LIST OF ILLUSTRATIONS

LIST OF TABLES

SECTION I
INTRODUCTION

The Automated Array Assembly Task, Phase 2 of the Low Cost Silicon Solar Array (LSSA) Project is a process development task. This contract includes solar cell module process development activities in the areas of Surface Preparation, Plasma Processing, Diffusion, Cell Processing and Module Fabrication. In addition, a High Efficiency Cell Development Activity is included. The overall goal is to advance solar cell module process technology to meet the 1986 goal of a production capacity of 500 megawatts per year at a cost of less than $500 per kilowatt. This contract will focus on the process element developments stated above and will propose an overall module process.

During this quarter, effort was concentrated on wafer etching for saw damage removal, establishing a standard phosphorous diffusion process and a baseline solar cell process as a test bed, designing a large area square cell including test sites, analyzing module layouts for optimum packing efficiency and fabricating the first Tandem Junction Cells (TJC) for this contract. A TJC with backside contacts gave 15.1% efficiency at AM1.

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SECTION II
TECHNICAL DISCUSSION

All major task areas that were scheduled to start in this quarter have begun. A brief description of each area follows.

A. SURFACE PREPARATION

Surface texturing studies on 100 silicon surfaces has begun. Aqueous NaOH has been selected as the etchant. Hydrazine, an alternate selective etchant, has been relegated to a very low priority choice due to cost and potential disposal problems.

A standard surface removal technique is being used to thin wafers for the High Efficiency Cell activity and to remove saw damage. Aqueous 40% NaOH is used at a temperature of 100-105°C. This is not the fastest etching condition but it appears to give a more uniform surface. The damaged material at the original sawed surface etches faster than the undamaged material. A total of 0.003-0.0035 inch (0.0076-0.0089 cm) is removed from both sides. The etch rate decreases slowly with use. The starting etch rate was 0.00034 inch/minute (0.00086 cm/minute) and after 133 wafers the rate decreased to 0.00028 inch/minute (0.00071 cm/minute).

Etch rate and conditions studies will continue.

B. PLASMA ETCHING

This activity is just being initiated. There are no results to report at this time.

C. DIFFUSION

A standard phosphorous diffusion ($POCl_3$ source) procedure is being established for comparison purposes. Results from the sensitivity study in Phase I are being used to establish the phosphorous diffusion procedure. A baseline cell fabrication process has been defined (see following section) using a $POCl_3$ deposition and diffusion at 850°C.

Solar cell fabrication runs have been started using As as the N^+ dopant. Both polymer dopant and ion implant are being processed. These runs are also discussed in the following section. A standard $POCl_3$ process has been completed. Electrical evaluation will begin shortly.

D. CELL PROCESSING

All process lots being run at this time except the High Efficiency Cell Development activity will use the hexagonal cell with the fishbone metallization that was designed during the prior contract. This cell features a number of test sites that can be used for evaluation. A square cell, compatible with high module packing efficiency is in design and will become the standard large-area test cell as soon as the patterns are available.

1. Cell Design

A revised large-area cell is being designed to be used on this contract as a vehicle for process development and to provide cells for assembly of modules. This cell will be a truncated square scribed from 7.62 cm (3 inch) circular slices. Based on module optimization studies, the cell will be 6.2 centimeters on a side. The cell will also contain some of the test patterns developed on the previous contract for evaluation of processes.

Design of the cell and test patterns has started. A layout of the cell is shown in Figure 1. Number of metal stripes and spacing will be determined by design techniques developed on the previous contract. Test patterns to be included on the cell are indicated by letters. The test patterns are variations of designs from the previous contract and will include:

A) Concentric Ring Pattern – (4 variations)

B) 4-Point metal pattern – on stripe

C) 4-Point metal pattern – on oxide

D) Diodes (2 each)

E) Spreading resistance contact to base region on backside (3 each)

F) Test cell with AR coating

G) Test cell without AR coating.

Layouts will be submitted for masks in early December.

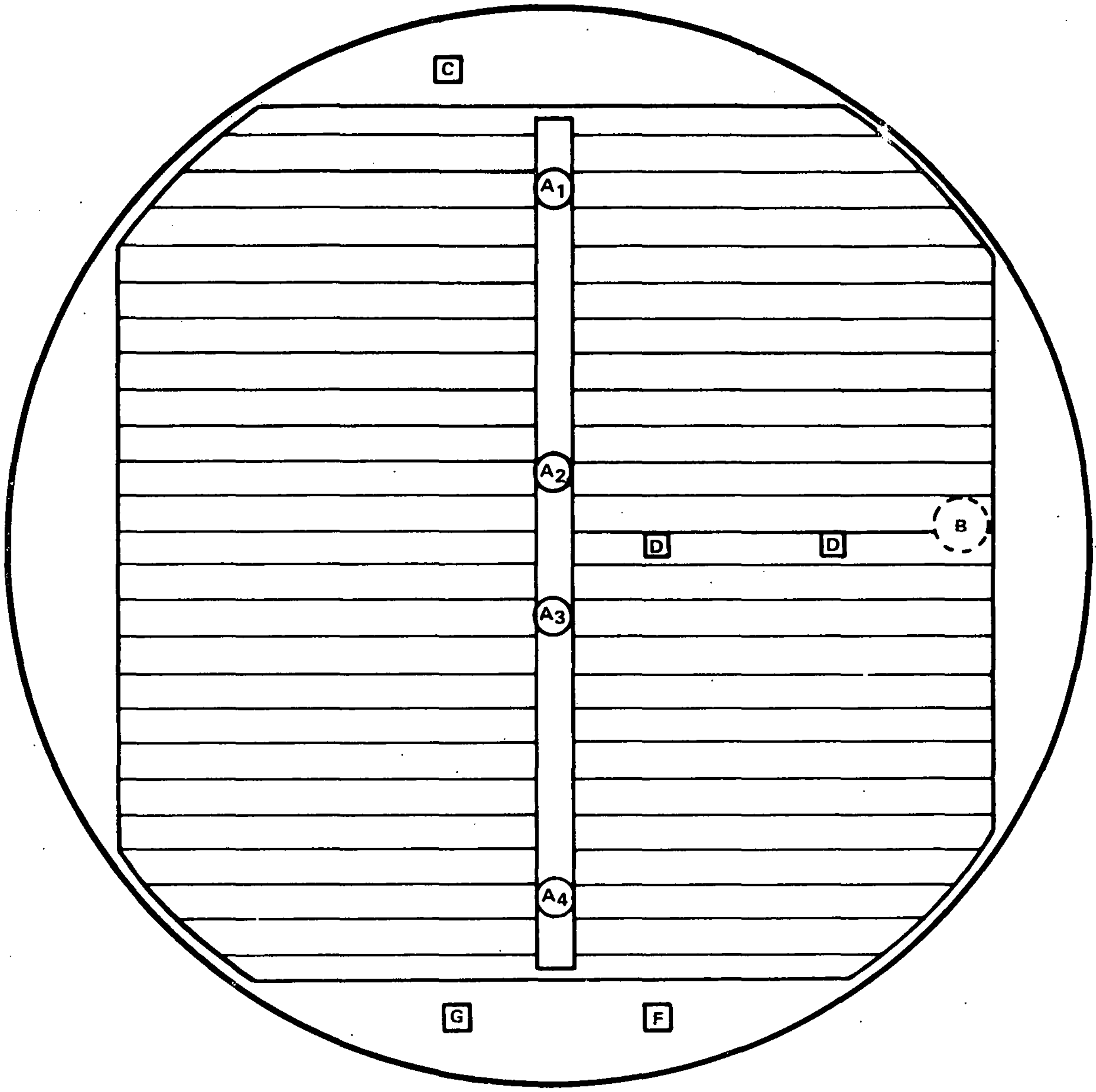

Figure 1. Layout of Cell and Test Patterns

2. Processing

A standard process has been defined. Process steps are shown in Figure 2.

A baseline lot of cells was completed. Electrical testing will begin in the next report period.

Runs have also been started using arsenic for the front surface N^+ region. Several cells were fabricated with planar arsenic implanted N^+ regions. These cells exhibited high NKT currents as previously observed in mesa cells fabricated with arsenic polymer doping. Additional polymer doped cells have been fabricated. These cells have planar junctions and were processed as a split lot with and without phosphorous gettering.

Starting Material
P-type
⟨100⟩
0.3-2.0 Ω-cm
$\tau > 50\ \mu s$
Cleanup
Oxidize – 2 KÅ
Pattern Oxide – Front side
Diffuse N^+
Deposit Silane (1200Å) – front side
Remove Oxide – back side
Evaporate Aluminum – back side
Sinter
Cut Contacts – front side
Evaporate Metal – front side
Pattern Metal – front side
Test

Figure 2. Standard Baseline Process

One lot of thin tandem junction cells (TJC), 110-μm thick, that was started before this program began, was completed. Test results are reported under High Efficiency Cell Development. A second lot of TJC, AAAP-II-3, was also fabricated. Results are reported in a following section of this report.

E. MODULE FABRICATION

Two development efforts will be pursued in module fabrication. First, a detailed module design versus cost review will be made to identify all potential cost reductions in this cost-intensive operation. Second, sample quantities of modules representing the optimized module design will be fabricated to evaluate the fabrication process and allow sample modules to be subjected to accelerated life testing as JPL identifies meaningful module tests.

Overall module efficiency is expressed by the following equations:

$$\text{Module Efficiency} = \frac{\text{module power}}{\text{module area X 1000 watt/M}^2}$$

$$\eta_M = \overbrace{[\eta_C\ \eta_{MIS}\ \eta_\tau\ \eta_{NOCT}]}^{\eta_{EC}} \text{ X } \overbrace{[\eta_{BR}\ \eta_{BS}\ \eta_{IC}\ \eta_N]}^{\eta_P}$$

where

η_{EC} = Encapsulated cell efficiency

η_C = Cell efficiency at 28°C, 100 mW/cm^2

η_{MIS} = Cell mismatch efficiency

η_T = Optical transmission efficiency

η_{NOCT} = Cell operating temperature efficiency

η_P = Packing efficiency

η_{BR} = Border area efficiency

η_{BS} = Bus area efficiency

η_{IC} = Interconnect area efficiency

η_N = Cell nesting efficiency

Theoretical packing efficiencies were calculated using the following constraints:

6.16 cm and 6.20 cm square silicon cells

0.10 cm spacing between cells

1.00 cm allowance for bus and interconnect

1.00 cm border

Module width = 0.750 (N) – 0.12 inch

Where "N" is an integer value from 13 to 64 (obtained from JPL Drawing J10082854 Rev. A, Note 7) Refer to Table 1.

Tables 2 and 3 display packing efficiency calculations based on various module widths with a constant module length. Excess width generated by cumulative mismatch between overall cell width and JPL module width was included in the "border efficiency" calculation.

As expected with rectangular or square cells, the nesting efficiency is 100%. At this time square cells with rounded corners were not taken into account. The interconnect area efficiency remained constant at 96.8% because it is assumed that there will be all back side connections and the spacing between the cells remains constant. As the module area increases so does the bus area efficiency, because the bus area is independent of module size. In Table 3 cell efficiency is assumed to be 20%. Optical transmission is based on water-white crystal glass with a transmittance value of

Table 1. Allowable Module Widths

Module Width = 0.750 (N) – 0.12 inch
Where N = 13 to 64 (integer value)

N	Inches	cm	N	Inches	cm
13	9.63	24.46	39	29.13	73.99
14	10.38	26.37	40	29.88	75.90
15	11.13	28.27	41	30.63	77.80
16	11.88	30.18	42	31.38	79.71
17	12.63	32.08	43	32.13	81.61
18	13.38	33.99	44	32.88	83.52
19	14.13	35.89	45	33.63	85.42
20	14.88	37.80	46	34.38	87.33
21	15.63	39.70	47	35.13	89.23
22	16.38	41.61	48	35.88	91.14
23	17.13	43.51	49	36.63	93.04
24	17.88	45.42	50	37.38	94.95
25	18.63	47.32	51	38.13	96.85
26	19.38	49.23	52	38.88	98.76
27	20.13	51.15	53	39.63	100.66
28	20.88	53.04	54	40.38	102.57
29	21.63	54.94	55	41.13	104.47
30	22.38	56.85	56	41.88	106.38
31	23.13	58.75	57	42.63	108.28
32	23.88	60.66	58	43.38	110.19
33	24.63	62.56	59	44.13	112.09
34	25.38	64.47	60	44.88	114.00
35	26.13	66.37	61	45.63	115.90
36	26.88	68.28	62	46.38	117.81
37	27.63	70.18	63	47.13	119.71
38	28.38	72.09	64	47.88	121.62

91%. Transmittance of 95% and 98% are also used to demonstrate the effect of antireflecting coatings. PRO (Pessimistic, Realistic, Optimistic) calculations were made for module efficiencies based on existing information. These calculations do not include cell mismatch or NOCT efficiencies since these values are not yet defined for the tandem junction cell.

The module length constraints listed on Table 2 show an excess of 0.78 cm on the overall length of the module. This excess length was proportionately added to each cell to arrive at a 6.2 cm by 6.2 cm cell. Efficiencies were recalculated using a 6.2 X 6.2 cm cell and the new values are shown in Tables 4 and 5.

Table 2. Module Design Efficiency Calculations – 6.16-cm Cell

Module Length 47.88 inches	=	**121.62 cm**
Cell Length (19 @ 6.16 cm)	=	**117.04 cm**
Cell Spacing (18 @ 0.1 cm)	=	**1.80 cm**
Border (2 @ 1.0 cm)	=	**2.00 cm**
Excess Length	=	**0.78 cm**

19 Cells/Column (fixed) 6.16 cm x 6.16 cm each

		Numbers of Cells Per Row															
		3	**4**	**5**	**6**	**7**	**8**	**9**	**10**	**11**	**12**	**13**	**14**	**15**	**16**	**17**	**18**
Total Cell Width (cm)		18.48	24.64	30.80	36.96	43.12	49.28	55.44	61.6	67.76	73.92	80.08	86.24	92.40	98.56	104.72	110.88
Cell Space Width Total (cm)		0.20	0.30	0.40	0.50	0.60	0.70	0.80	0.90	1.0	1.10	1.20	1.30	1.40	1.50	1.60	1.70
Border Width (cm)		2.00	2.00	2.00	2.00	2.00	2.00	2.00	2.00	2.00	2.00	2.00	2.00	2.00	2.00	2.00	2.00
Bus Allowance Width (cm)		1.20	1.20	1.20	1.20	1.20	1.20	1.20	1.20	1.20	1.20	1.20	1.20	1.20	1.20	1.20	1.20
Total Module Width (cm)		21.88	28.14	34.40	40.66	46.92	53.18	59.44	65.70	71.96	78.22	84.48	90.74	97.00	103.26	109.52	115.78
Recommended JPL Width (cm)		24.46	28.27	35.89	41.61	47.32	54.94	60.66	66.37	72.09	79.71	85.42	91.14	98.76	104.47	110.19	115.90
Excess Area (cm)		323.70	37.30	203.90	144.60	84.10	250.70	191.40	130.80	71.50	238.10	177.60	118.30	284.90	224.30	165.00	104.60
Module Area (cm^2)	A	2974.8	3438.2	4364.9	5060.6	5755.1	6681.8	7377.5	8071.9	8767.6	9694.3	10388.8	11084.4	12011.2	12705.6	13401.3	14095.8
Planned Border Plus Excess Area (cm^2)	B	611.9	333.1	514.9	467.1	418.0	599.8	552.0	502.8	454.9	636.8	587.7	539.8	721.7	672.5	624.6	575.6
Bus Area (cm^2)	C	143.5	143.5	143.5	143.5	143.5	143.5	143.5	143.5	143.5	143.5	143.5	143.5	143.5	143.5	143.5	143.5
Interconnect Area (cm^2)	D	70.2	93.6	117.0	140.4	163.9	187.3	210.7	234.1	257.5	280.9	304.3	327.7	351.1	374.5	397.9	421.3
Cell Area (cm^2)	E	2162.9	2833.9	3604.8	4325.8	5046.8	5767.7	6488.7	7209.7	7930.6	8651.6	9372.6	10093.5	10814.5	11535.5	12256.4	12977.4
Efficiency (%)																	
Border	η_{BR}	79.4	90.3	88.2	90.8	92.7	91.0	92.5	93.8	94.8	93.4	94.3	95.1	94.0	94.7	95.3	95.9
Bus	η_{BS}	93.9	95.4	96.3	96.9	97.3	97.6	97.9	98.1	98.3	98.4	98.5	98.6	98.7	98.8	98.9	98.9
Interconnect	η_{IC}	96.8	96.8	96.8	96.8	96.8	96.8	96.8	96.8	96.8	96.8	96.8	96.8	96.8	96.9	96.9	96.9
Nesting	η_N	100.0	100.0	100.0	100.0	100.0	100.0	100.0	100.0	100.0	100.0	100.0	100.0	100.0	100.0	100.0	100.0
Packing	η_P	7.27	83.9	82.6	85.5	87.7	86.3	88.0	89.3	90.5	89.2	90.2	91.1	90.0	90.8	91.5	92.1

Table 3. Module Design Efficiency Calculations – 6.16-cm Cell

Efficiency (%)		Number of Cells Per Row: 3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18
Border Area		79.4	90.3	88.2	90.8	92.7	91.0	92.5	93.8	94.8	93.4	94.3	95.1	94.0	94.7	95.3	95.9
Bus Area		93.9	95.4	96.3	96.9	97.3	97.6	97.9	98.1	98.3	98.4	98.5	98.6	98.7	98.8	98.9	98.9
Interconnect Area		96.8	96.8	96.8	96.8	96.8	96.8	96.8	96.8	96.8	96.8	96.8	96.8	96.8	96.9	96.9	96.9
Cell Nesting		100.0	100.0	100.0	100.0	100.0	100.0	100.0	100.0	100.0	100.0	100.0	100.0	100.0	100.0	100.0	100.0
Packing		**72.7**	**83.9**	**82.6**	**85.5**	**87.7**	**86.3**	**88.0**	**89.3**	**90.5**	**89.2**	**90.2**	**91.1**	**90.0**	**90.8**	**91.5**	**92.0**
Cell @ 28°C, 100 mW/cm^2	AM1	20.0	20.0	20.0	20.0	20.0	20.0	20.0	20.0	20.0	20.0	20.0	20.0	20.0	20.0	20.0	20.0
Cell Mismatch																	
Optical Transmission	P 91.0 R 95.0 O 98.0	95.0	95.0	95.0	95.0	95.0	95.0	95.0	95.0	95.0	95.0	95.0	95.0	95.0	95.0	95.0	95.0
NOCT																	
Encapsulated	**R (95.0)**	**19.0**	**19.0**	**19.0**	**19.0**	**19.0**	**19.0**	**19.0**	**19.0**	**19.0**	**19.0**	**19.0**	**19.0**	**19.0**	**19.0**	**19.0**	**19.0**
	Pessimistic	13.2	15.3	15.0	15.6	16.0	15.7	16.0	16.3	16.5	16.2	16.4	16.6	16.4	16.5	16.7	16.7
Module	Realistic	13.8	15.9	15.7	16.2	16.7	16.4	16.7	17.0	17.2	16.9	17.1	17.3	17.1	17.3	17.4	17.5
	Optimistic	14.2	16.4	16.2	16.8	17.2	16.9	17.2	17.5	17.7	17.5	17.7	17.9	17.6	17.8	17.9	18.0

Table 4. Module Design Efficiency Calculations – 6.2-cm Cell

Module Length 47.88 inches = 121.62 cm
Cell Length (19 @ 6.20 cm) = 117.80 cm
Cell Spacing (18 @ 0.1 cm) = 1.80 cm
Border (2 @ 1.0 cm) = 2.00 cm
19 Cells/Column (fixed) 6.2 cm x 6.2 cm each

	Number of Cells Per Row															
	3	**4**	**5**	**6**	**7**	**8**	**9**	**10**	**11**	**12**	**13**	**14**	**15**	**16**	**17**	**18**
Total Cell Width (cm)	18.60	24.80	31.00	37.20	43.40	49.60	55.80	62.00	68.20	74.40	80.60	86.80	93.00	99.20	105.40	111.60
Total Cell Space Width (cm)	0.20	0.30	0.40	0.50	0.60	0.70	0.80	0.90	1.00	1.10	1.20	1.30	1.40	1.50	1.60	1.70
Border Width (cm)	2.00	2.00	2.00	2.00	2.00	2.00	2.00	2.00	2.00	2.00	2.00	2.00	2.00	2.00	2.00	2.00
Bus Allowance Width (cm)	1.20	1.20	1.20	1.20	1.20	1.20	1.20	1.20	1.20	1.20	1.20	1.20	1.20	1.20	1.20	1.20
Total Module Width (cm)	22.00	28.30	34.60	40.90	47.20	53.50	59.80	66.10	72.40	78.70	85.00	91.30	97.60	103.90	110.20	116.50
Recommended JPL Width (cm)	24.46	28.27	35.89	41.61	47.32	54.94	60.66	66.37	73.99	79.71	85.42	93.04	98.76	104.47	110.19	117.81
Excess Area (cm^2)	294.27	– 0 –	154.31	84.93	14.35	172.25	102.87	32.30	190.20	120.82	50.24	208.14	138.76	68.18	– 0 –	156.70
Module Area (cm^2)	2974.8	3438.2	4364.9	5060.6	5755.1	6681.8	7377.5	8071.9	8998.7	9694.3	10388.8	11315.5	12011.2	12705.6	13401.3	14328.1
Planned Border Plus Excess Area (cm^2)	582.47	295.8	465.31	407.43	348.25	521.35	463.47	404.30	573.60	519.52	460.34	629.64	575.56	516.38	459.6	627.70
Bus Area (cm^2)	143.5	143.5	143.5	143.5	143.5	143.5	143.5	143.5	143.5	143.5	143.5	143.5	143.5	143.5	143.5	143.5
Interconnect Area (cm^2)	70.6	94.2	117.8	141.3	164.9	188.4	212.0	235.6	259.1	282.7	306.2	329.8	353.4	376.9	400.5	424.0
Cell Area (cm^2)	2191.1	2921.4	3651.8	4382.2	5112.5	5842.9	6573.2	7303.6	8034.0	8764.3	9494.7	10225.0	10955.4	11685.8	12416.1	13146.5
Efficiency (%)																
Border	80.4	91.4	89.3	91.9	93.9	92.2	93.7	95.0	93.6	94.6	95.5	94.4	95.2	95.9	96.6	95.6
Bus	94.0	95.4	96.3	96.9	97.3	97.7	97.9	98.1	98.3	98.4	98.6	98.7	98.7	98.8	98.9	99.0
Interconnect	96.9	96.9	96.9	96.9	96.9	96.9	96.9	96.9	96.9	96.9	96.9	96.9	96.9	96.9	96.9	96.9
Nesting	100.0	100.0	100.0	100.0	100.0	100.0	100.0	100.0	100.0	100.0	100.0	100.0	100.0	100.0	100.0	100.0
Packing	73.7	85.0	83.7	86.6	88.8	87.4	89.1	90.5	89.3	90.4	91.4	90.4	91.2	92.0	92.6	91.8

Table 5. Module Design Efficiency Calculations – 6.2-cm Cell

		Number of Cells Per Row															
Efficiency (%)		**3**	**4**	**5**	**6**	**7**	**8**	**9**	**10**	**11**	**12**	**13**	**14**	**15**	**16**	**17**	**18**
Border Area		80.4	91.4	89.3	91.9	93.9	92.2	93.7	95.0	93.5	94.6	95.6	94.4	95.2	95.9	96.6	95.6
Bus Area		94.0	95.4	96.3	96.9	97.3	97.7	97.9	98.1	98.3	98.4	98.6	98.7	98.7	98.8	98.9	99.0
Interconnect Area		96.9	96.9	96.9	96.9	96.9	96.9	96.9	96.9	96.9	96.9	96.9	96.9	96.9	96.9	96.9	96.9
Cell Nesting		100.0	100.0	100.0	100.0	100.0	100.0	100.0	100.0	100.0	100.0	100.0	100.0	100.0	100.0	100.0	100.0
Packing		**73.7**	**85.0**	**83.7**	**86.6**	**88.8**	**87.4**	**89.1**	**90.5**	**89.3**	**90.4**	**91.4**	**90.4**	**91.2**	**92.0**	**92.6**	**91.8**
Cell @ 28°C, 100 mW/cm^2	AM1	20.0	20.0	20.0	20.0	20.0	20.0	20.0	20.0	20.0	20.0	20.0	20.0	20.0	20.0	20.0	20.0
Cell Mismatch																	
Optical Transmission	P 91.0 R 95.0 O 98.0	95.0	95.0	95.0	95.0	95.0	95.0	95.0	95.0	95.0	95.0	95.0	95.0	95.0	95.0	95.0	95.0
NOCT																	
Encapsulated	**R (95.0)**	**19.0**	**19.0**	**19.0**	**19.0**	**19.0**	**19.0**	**19.0**	**19.0**	**19.0**	**19.0**	**19.0**	**19.0**	**19.0**	**19.0**	**19.0**	**19.0**
Module	Pessimistic	13.4	15.5	15.2	15.8	16.2	15.9	16.2	16.5	16.3	16.5	16.6	16.5	16.6	16.7	16.9	16.7
Module	Realistic	14.0	16.2	15.9	16.5	16.9	16.6	16.9	17.2	17.0	17.2	17.4	17.2	17.3	17.5	17.6	17.4
Module	Optimistic	14.4	16.7	16.4	17.0	17.4	17.1	17.5	17.7	17.5	17.7	17.9	17.7	17.9	18.0	18.1	18.0

It should be clarified at this point that the recommended JPL dimensions were used in all calculations to maintain continuity with JPL. In other than JPL test stations, modules would be designed using an optimized cell manufacturing process, and then, the encapsulation would be optimized to fit the cells. Similarly, an optimum cell size can be calculated for a given module. Silicon sheet material could be specified as a function of module dimensions.

Figures 3, 4 and 5 are a graphical presentation of packing efficiencies using 6.16 cm cells, 6.20 cm cells, and a comparison of the two respectively.

A 1.3% increase in unit cell area results in a 1.3% decrease in the number of modules required for a given power output. For example, a 0.807-m^2 module with 17% efficiency will supply 124.16 watts with a 6.2-cm cell against 122.56 watts with a 6.16-cm cell and result in an annual requirement of 80,542 modules versus 81,593 modules for a 10 MW facility; a reduction of 1051 modules annually. Some annual savings would be as follows:

	Pounds	**Dollars**
Steel	24,990	5372.25
Glass	17,182	4030.44

Plus related manufacturing costs.

More work will be done in this area over the next several months. An evaluation will also be completed on the effect of packing efficiency versus rounded corners on cells.

The smaller the module, the higher the ratio of bus and border to total module area. This shows up dramatically in the plots where bus and border efficiencies drop significantly as the number of columns is decreased. Consequently, desired packing efficiencies can only be achieved with 2′ X 4′ modules or larger.

Emphasis was also placed on tooling up for manufacturing of sample quantities of substrate and lock frame. The 75-ton press, which is used to form our substrates, is being modified to meet OSHA standards. Submodule sizes of 34.60 cm X 40.34 will be manufactured to incorporate a 6 X 5 matrix of 6.20 cm square cells. Three submodules could be mounted on a rack to form a 121.62 cm long module. The rack will increase the overall module width to the JPL dimension of 35.89 cm. Machining of homemade dies for the substrate has begun.

Design decisions on full size substrates have begun. Not only must the substrate be sufficiently designed to meet handling and environmental conditions, it must also be designed to survive processing conditions. Porcelainizing, for example, is the application of an inorganic finish at temperatures ranging from 800 to 1800°F. Consequently, a determining factor in using ferrous

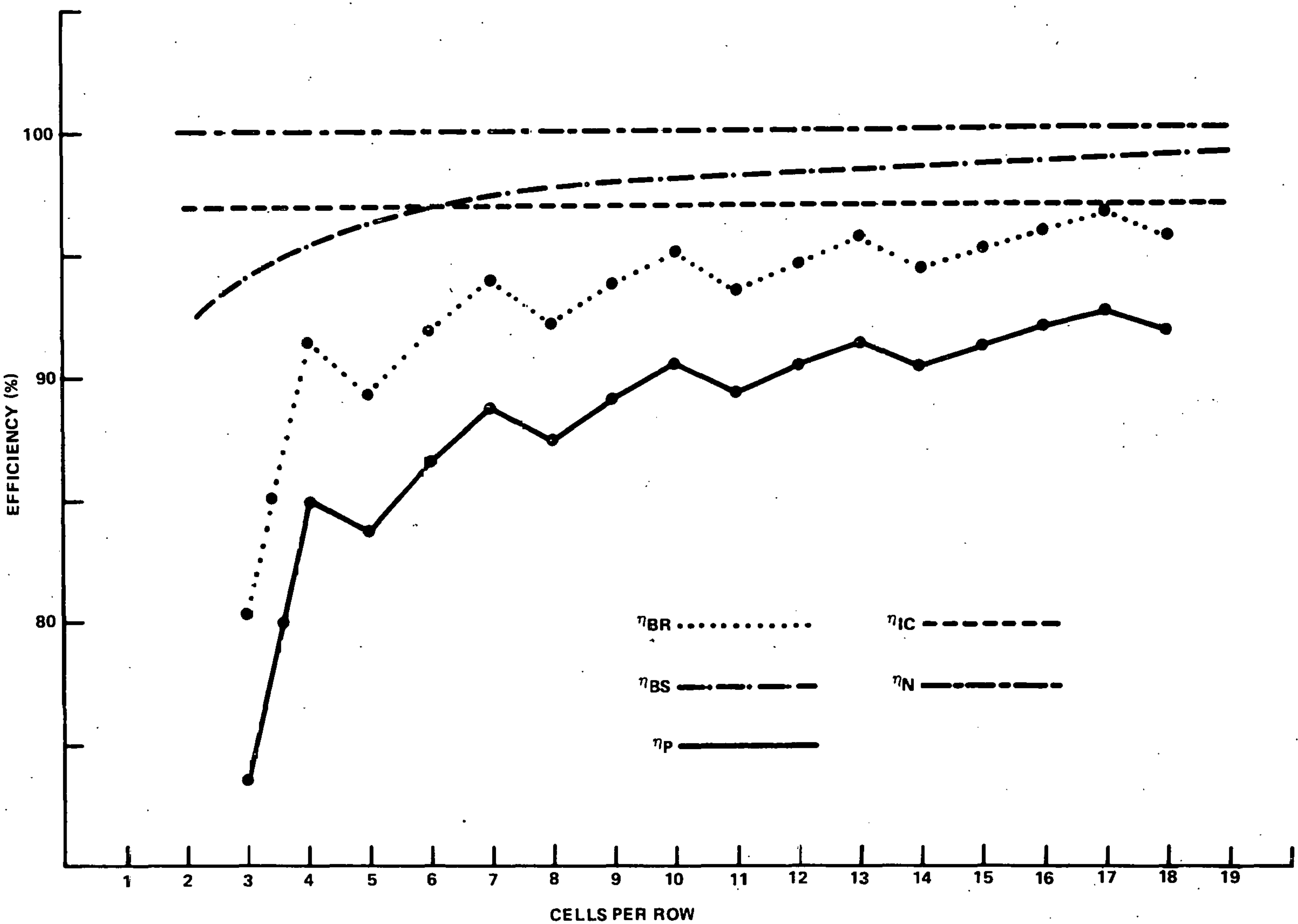

Figure 3. Packing Efficiency – 6.16-cm Cell

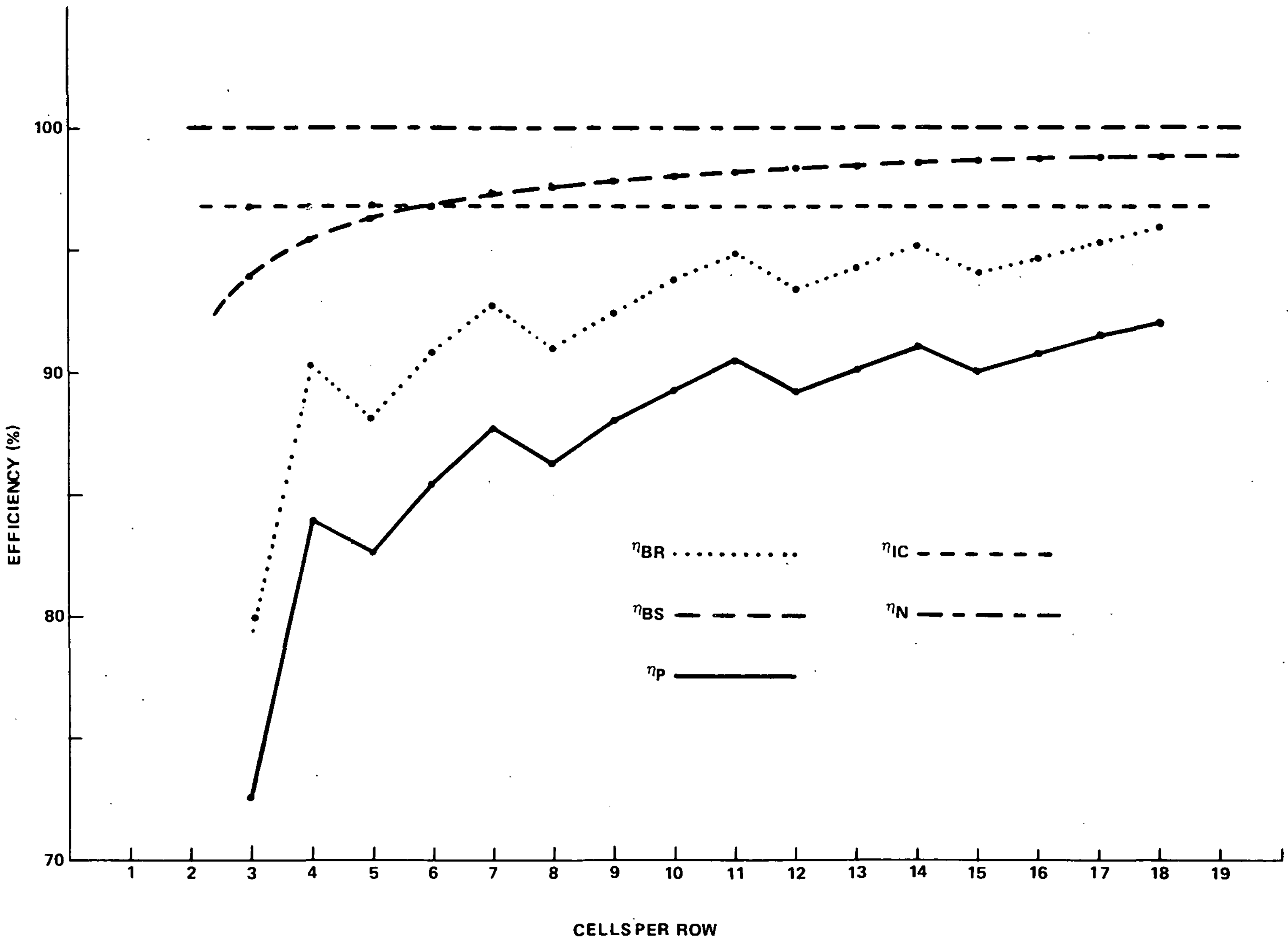

Figure 4. Packing Efficiency – 6.2-cm Cell

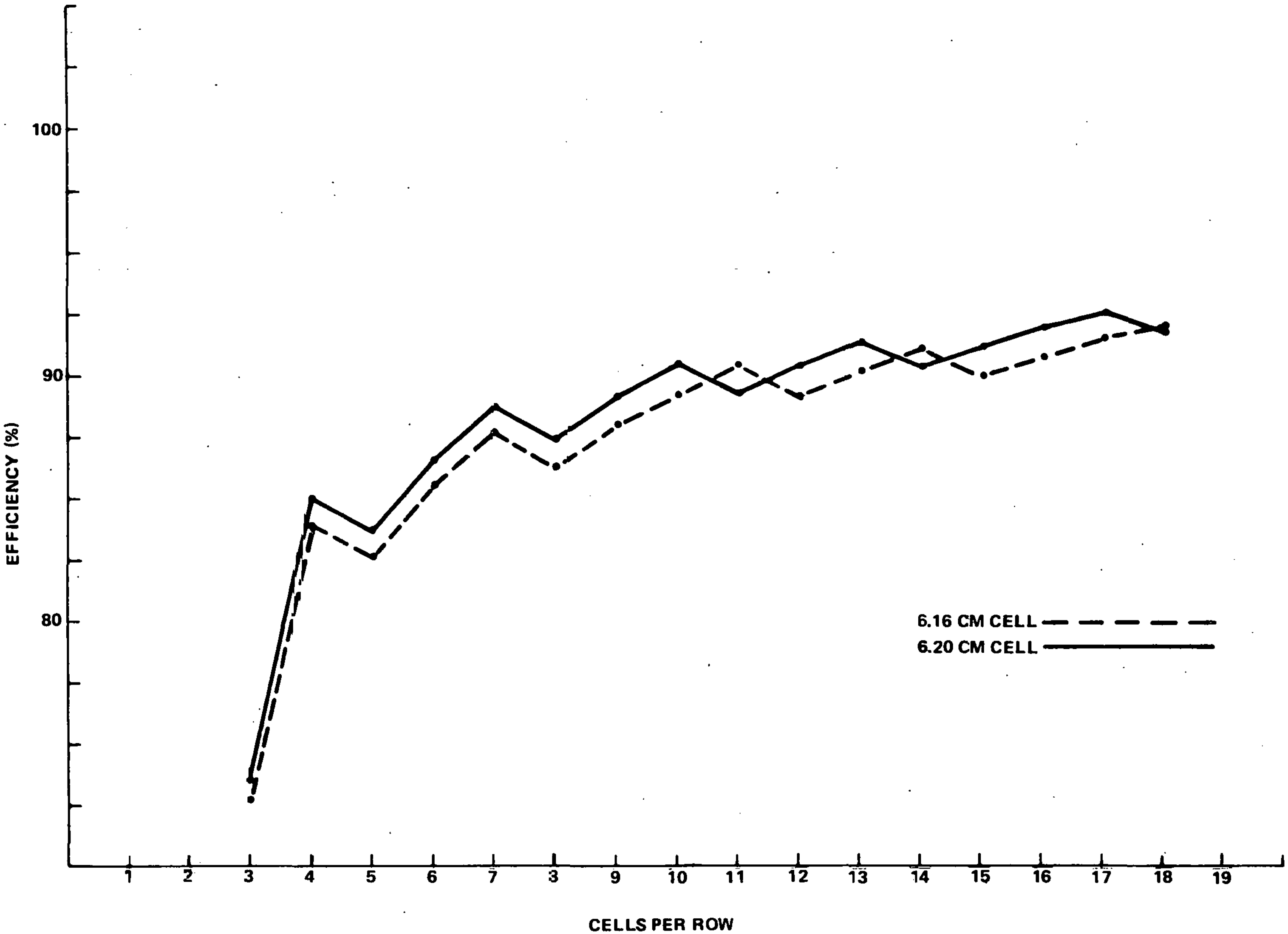

Figure 5. Packing Efficiency Comparison – 6.16 and 6.2-cm Cells

metal sheet as a base for porcelain enameling is the high temperature involved in firing the porcelain enamel. Ferrous metal sheets have a tendency to sag, warp or deform. In addition, gas may be evolved, resulting in blisters and fish scaling per PEI (Porcelain Enamel Institute) Bulletin P-306. As a result, enameling grade steels must be used.

The PEI guide for proper metal thickness indicates that the minimum gage for a 2 by 4 foot substrate would be 0.0359. Minimum bend radii on the substrate and lock frame would be 3/16 inch. PEI also recommends that reinforcement gussets be two gages lighter than the substrate itself. This will reduce the danger of under-firing at points where attachments are welded. A 0.050 inch clearance will be allowed for the mating of the substrate and lock frame prior to porcelain enameling. An additional overall design consideration will be to keep the 2 X 4 foot module weight below 50 pounds.

F. HIGH EFFICIENCY CELL DEVELOPMENT

Two 5.0-cm Czochralski crystals have been grown for use on this activity. Both crystals are ⟨100⟩ orientation. One crystal has a target resistivity of 0.2 ohm-cm and the other has a target resistivity of 1.0 ohm-cm. Wafers are being prepared for processing. All cell development will be performed on wafers from these two crystals, as soon as they are ready. Preliminary processing is being performed on available 5.0-cm wafers from other crystals.

Thin TJCs (110 μm) with backside contact only were submitted to JPL and to NASA-Lewis for photoresponse measurements. These cells have phosphorous N^+ diffused layers on both sides, junction depth $\approx$0.3 μm and a textured front surface coated with a SiO_2 antireflection coating. The back contacts have 8 fingers per cell (the 1 X 1 cm cell is a shrink of the 2 X 2 cell). Several features are nonoptimum, the cells are thicker than ideal, the front N^+ layer is thicker than ideal, the AR coating has a low refractive index and the finger spacing is too wide for the 3 Ω-cm material. Photoresponse measurements are shown in Table 6.

Table 6. Photoresponse for TJC with Back Contact Only

Cell No.	Area (cm^2)	Measured by	Isolation	I_{SC} (mA)	V_{OC} (V)	F.F.	η (%)
20-6	0.975	NASA-Lewis	AM0	36.4	0.593	0.758	12.4
			AM1	33.3	0.586	0.753	15.1
20-2	0.975	NASA-Lewis	AM0	34.0	0.590	0.762	11.6
			AM1	31.0	0.584	0.756	14.1
20-1	3.90	JPL	AM1	115.2	0.595	0.65	11.8
20-8	0.975	JPL	AM1	30.0	0.595	0.766	14.1

The effect of the wider finger spacing on the 2 X 2 cm cell, 20-1, is obvious in the lowered fill factor. Figures 6 and 7 are the measured AM1 photoresponse for cells 20-6 and 20-2. The effect of the other nonideal features, thickness, deeper front N^+ layer and low refractive index cannot be measured at this time.

A second lot, AAAP-II-3, was fabricated on the same material with thickness from 65 to 90 μm. Front surface texture was very poor with less than 50% of the surface showing good texture. The front N^+ layer was diffused from an As doped CVD silicon oxide and the back N^+ layer was diffused from $POCl_3$ (850°C, 60 minutes versus standard 15 minutes). Unfortunately the CVD silicon oxide did not block the P diffusion and the front layer resistivity was $\approx$ 120 Ω/□. A SiO_2 AR coating was used. These cells with back contact only gave $J_{SC} \approx$ 25 to 30 mA/cm^2 at AM1 (sunlight) due to the poor surface texture and deeper than planned front junction. More samples are in process.

The two crystals grown for experimental work have been characterized. Resistivity and surface photovoltage (SPV) lifetime measurements are reported below.

Crystal Characterization

Crystal No.	**277**	**278**
Orientation	⟨100⟩	⟨100⟩
Resistivity (Ω-cm)	0.23-0.33	0.73-0.93
SPV lifetime (μs)	0.82	9
SPV lifetime after Oxidation (μs)	0.16	0.73
Comments	Swirl and haze, resistivity striations	No swirl or haze clear surface.

Sample wafers are being sawed from both crystals to fabricate test cells. Crystal No. 277, the low resistivity crystal, shows low SPV lifetime and may not be acceptable. Solar cell fabrication will be used to qualify the crystal. Crystal No. 278 appears to be satisfactory. Both crystals exhibit a fairly severe lifetime degradation after oxidation.

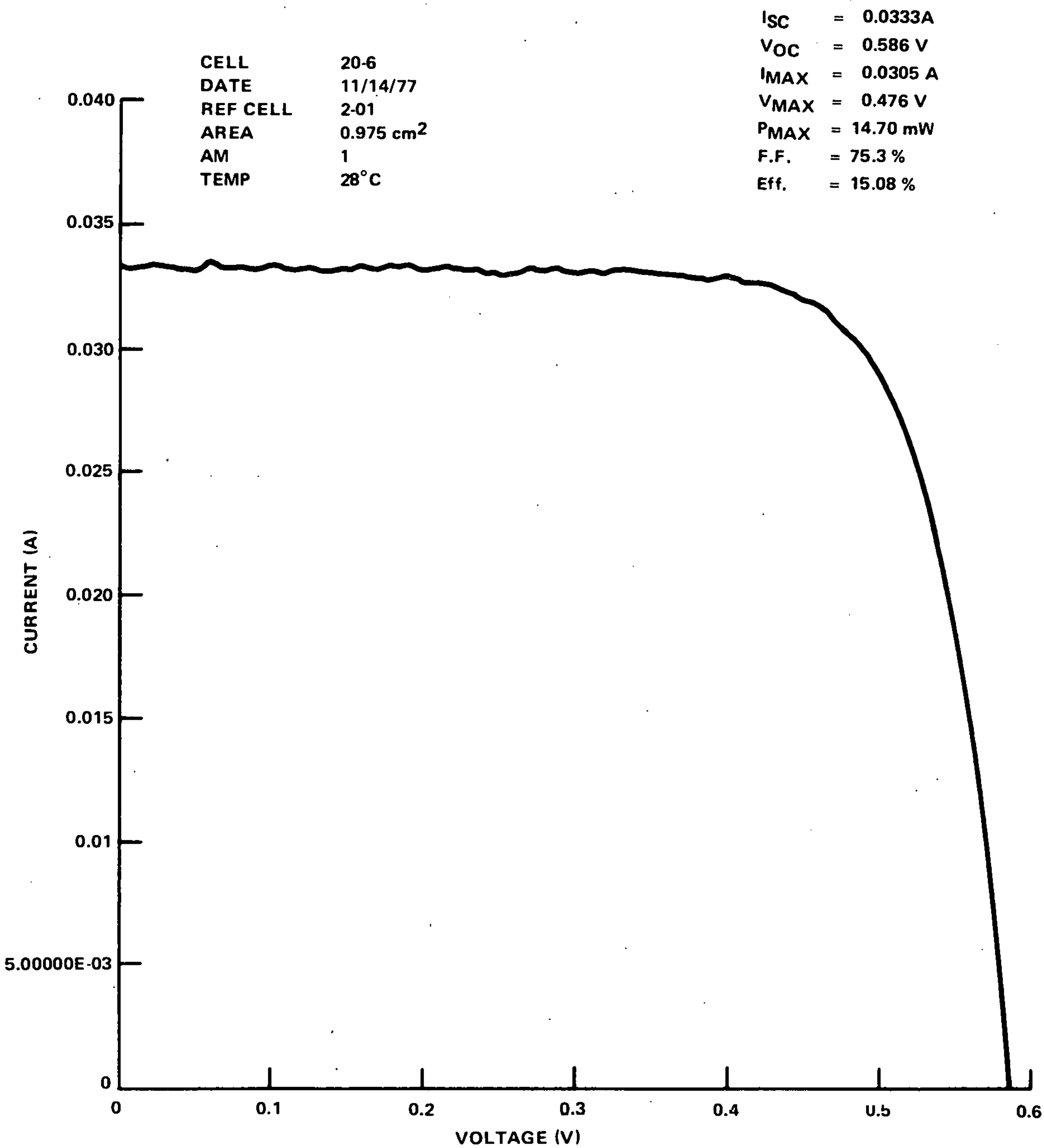

Figure 6. Tandem Junction Cell Photoresponse

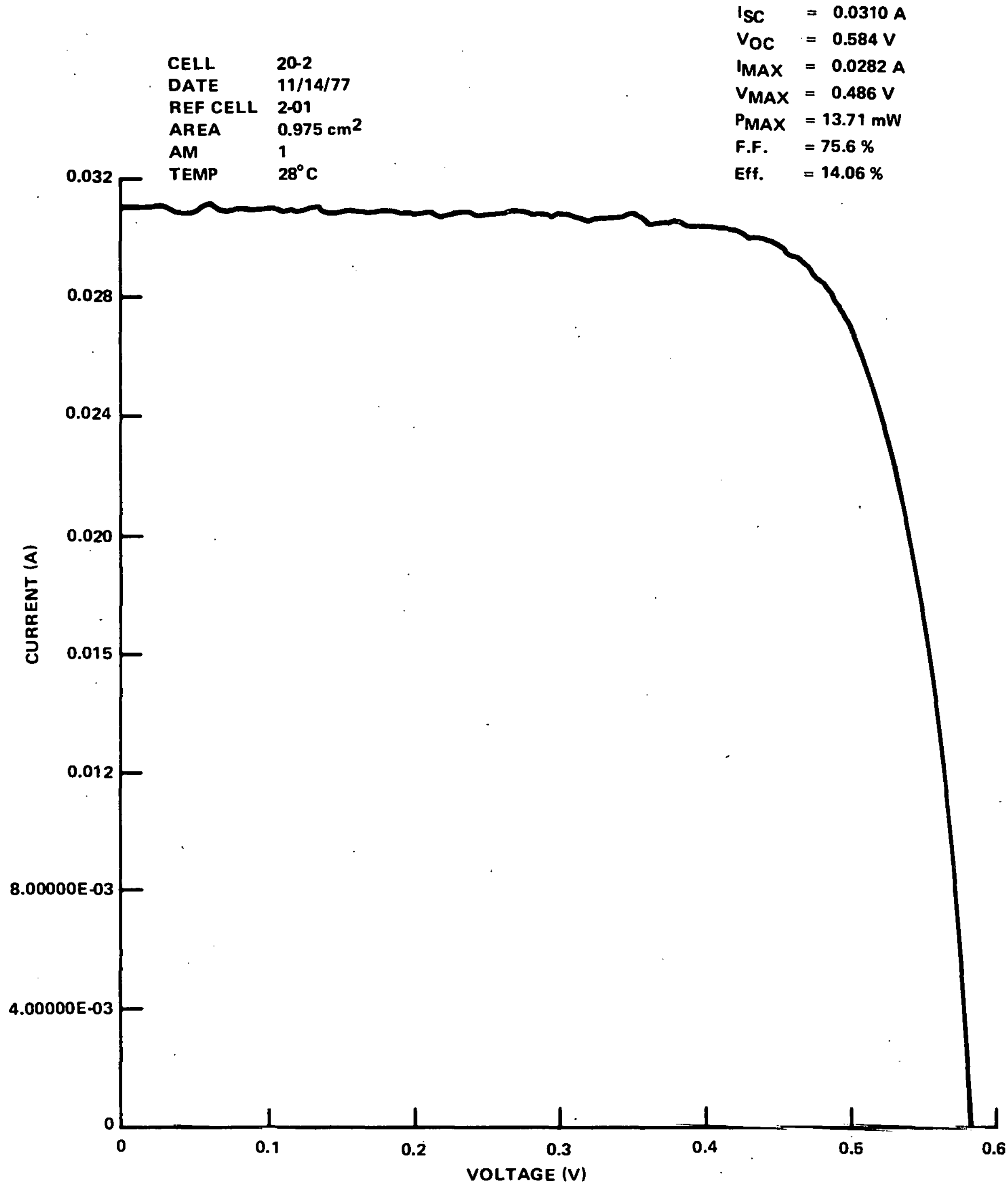

Figure 7. Tandem Junction Cell Photoresponse

SECTION III
CONCLUSIONS AND RECOMMENDATIONS

Aqueous NaOH etchant is useful for surface damage removal and for surface texturing.

Maximum module packing efficiency can be achieved by using rectangular solar cells. A square cell has been chosen for this work.

The TJC structure has been demonstrated to give up to 15.1% efficiency at AM1 on small cells using only back contacts. An improved metal pattern is being designed.

SECTION IV
NEW TECHNOLOGY

No new technology has been disclosed this quarter.

SECTION V
PROGRAM SUMMARY

Figure 8 shows the current work plan status. All scheduled activities are in process. No problems are apparent at present that will prevent attaining the indicated milestones.

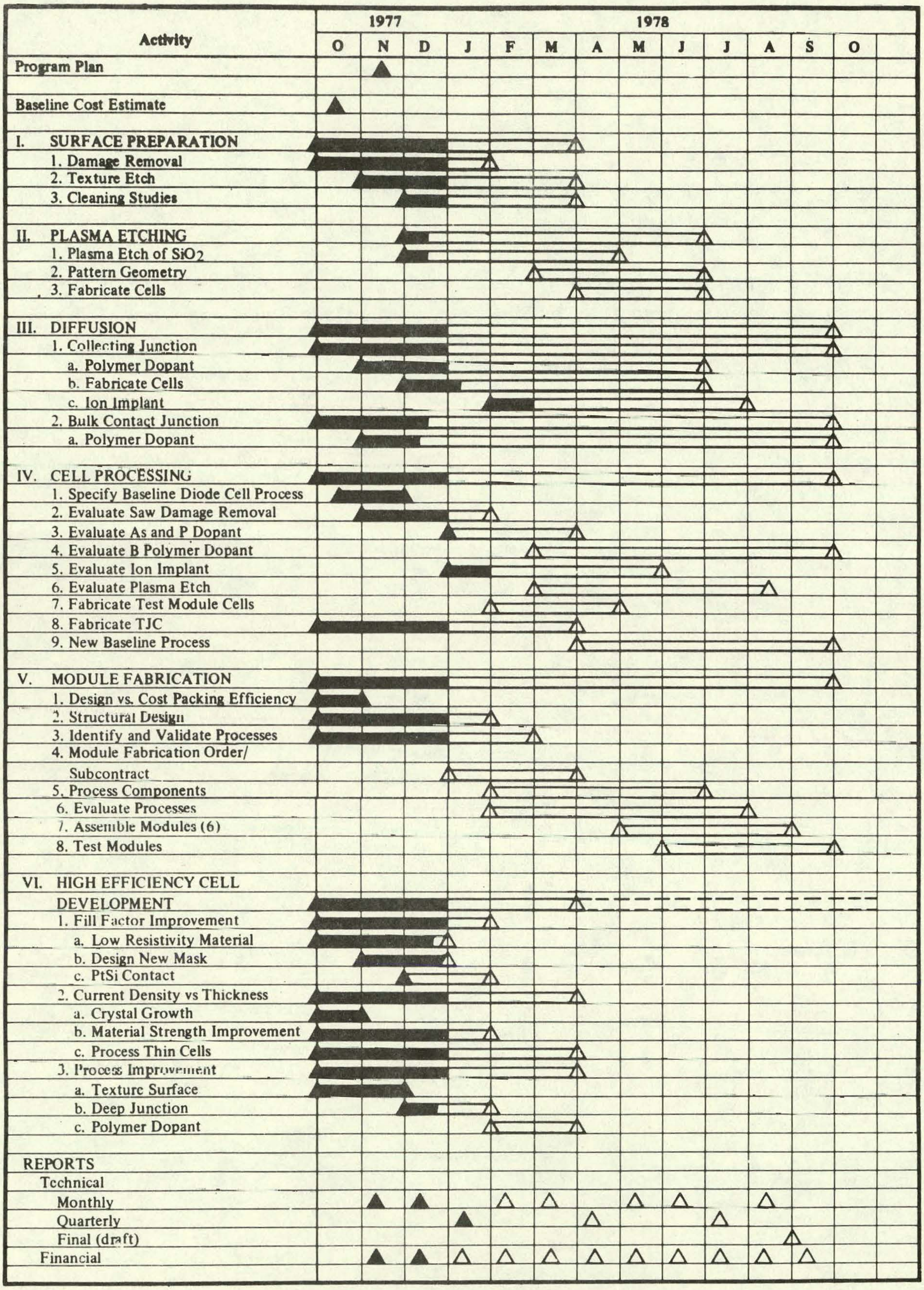

Figure 8. Work Plan

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