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# AUTOMATED ARRAY ASSEMBLY, PHASE 2

Texas Instruments Report No. 03-78-12

Quarterly Technical Progress Report. First Quarter 1978

By
Bernard G. Carbajal

April 1978

Work Performed Under Contract No. NAS-7-100-954881

Texas Instruments Incorporated
Dallas, Texas



U.S. Department of Energy

Solar Energy

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# AUTOMATED ARRAY ASSEMBLY
# PHASE 2

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Quarterly Technical Progress Report
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Bernard G. Carbajal

April 1978

JPL Contract No. 954881

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The JPL Low-Cost Silicon Solar Array Project is funded by DOE and forms part of the DOE Photovoltaic Conversion Program to initiate a major effort toward the development of low-cost solar arrays.

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## TABLE OF CONTENTS

## LIST OF ILLUSTRATIONS



## LIST OF TABLES

# SECTION I
# INTRODUCTION

The Automated Array Assembly Task, Phase 2 of the Low Cost Silicon Solar Array (LSSA) Project is a process development task. This contract includes solar cell module process development activities in the areas of Surface Preparation, Plasma Processing, Diffusion, Cell Processing and Module Fabrication. In addition, a High Efficiency Cell Development Activity is included. The overall goal is to advance solar cell module process technology to meet the 1986 goal of a production capacity of 500 megawatts per year at a cost of less than $500 per kilowatt. This contract will focus on the process element developments stated above and will propose an overall module process.

During the first quarter of 1978, effort was focused on understanding the texture etch process, improving the phosphorus diffusion process, fabricating large-area square cells, refining module costing and identifying cost problem areas, initiating module piece part fabrication, and establishing current density – thickness relationships for Tandem Junction Cells. A mechanism is proposed that explains the texturing process and accounts for the various methods of accelerating the pyramid formation process. The first large-area square cells have been fabricated for use in test sample module assembly. Cu-Invar clad metal bus bars have been fabricated and two material cost areas have been identified as cost problem areas.

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## SECTION II
## TECHNICAL DISCUSSION

All major task areas are in progress. A brief description of the activities in each area follows.

### A. SURFACE PREPARATION

Surface texturing experiments have proceeded to a point where some definite conclusions can be drawn and the direction of future work is more obvious. This report will summarize the most significant observations and postulate a mechanism that is consistent with the available data.

All texturing work was done with sodium hydroxide (NaOH) solutions. Hydrazine hydrate also is reported to be useful, but due to cost and safety factors, it has not been included in this study. All texturing work has been done on ⟨100⟩ silicon wafers. The surface texture is the result of preferential etching to form pyramids, whose faces are ⟨111⟩, on the prior ⟨100⟩ surface.

The following factors have been observed in aqueous NaOH systems. (Many of these have been reported by others in earlier studies.)

#### 1. Alcohol Additions

Addition of 1 to 35% isopropyl alcohol (IPA) to dilute NaOH solutions enhances the formation of pyramids. Typically aqueous NaOH with added IPA gives a high density of small pyramids. Optimum conditions have been reported[1,2] to be a 35% IPA-water solvent, 2% NaOH, at 80°C for 50 minutes.

#### 2. Proximity Effect

It has been observed earlier at Texas Instruments that the presence of another surface, essentially parallel to and in close proximity (0.4-1.0 mm) to the etching surface promotes surface texturing even at NaOH concentrations that normally do not favor pyramid formation, (≥4%). The

1. P. Stella and J. Scott-Monck, JPL Contract 954600, First Quarterly Report, January 1977.
2. *High Efficiency Solar Panels*, AFAPL-77-36, Spectralab, 1 June 1975 to 15 June 1977.

controlling factor appears to be the entrapment of hydrogen ($H_2$) bubbles between the two surfaces. This effect allows one to texture one surface selectively. Since the effect is dependent on $H_2$ bubble entrapment; viscosity, flow and position of the parallel surfaces are all factors.

### 3. Water-Glass ($Na_2SiO_3 \cdot X H_2O$) Additions

It has been observed that "used" NaOH solutions were more effective in surface texturing than "fresh" NaOH solutions. Therefore, it is reasonable to assume that small amounts of the reaction product, $Na_2SiO_3$, would promote the desired selective etching to produce the textured surface. The expected enhancement of selective etching was observed for NaOH solutions containing 0.5-2.0% (vol) $Na_2SiO_3 \cdot X H_2O$.

### 4. Surface Roughness and Damage

Sawed surfaces subjected to concentrated (40%) aqueous NaOH etching to remove damage can exhibit deep pits at damage locations. The walls of these pits initiate pyramid formation more readily than the rest of the surface. To eliminate this effect, chem-mechanically polished surfaces may be used.

### 5. Greases and Organic Contaminants

Long chain carboxylic acids have been reported to promote texturing.[2] We have observed that greases, even finger prints, have the same effect. Some organic materials, such as polyvinyl chloride cement, seriously inhibit pyramid formation. In our studies, plastic containers were avoided and each wafer was etched for 3 minutes in 30 to 40% aqueous NaOH at 100°C prior to texture etching.

From the foregoing data, the following conclusions were drawn. First, on a <100> surface, all surface atoms are equivalent in their bonding to the crystal lattice. Each atom has an equal chance to become the tip of a pyramid. Therefore, some external influence selects the preferred sites for pyramid formation. Second, since pyramid formation is enhanced in dilute (<4%) aqueous NaOH solutions and not in concentrated (40%) aqueous NaOH solutions, the external factor is related to either solubility in the etchant or dissolution rate. Third, the presence of certain insoluble or slightly soluble materials, greases or fingerprints, enhances pyramid formation, therefore a reaction product is probably a key factor in clean experiments. Fourth, the addition of small amounts of $Na_2SiO_3 \cdot XH_2O$ enhances pyramid formation. $Na_2SiO_3$ is the main reaction product, along with $H_2$, of the NaOH-Si reaction. $Na_2SiO_3$ has limited solubility in aqueous NaOH solutions and even lower solubility in water-IPA mixtures. Fifth, bringing another surface close to the etching one forces the $H_2$ bubbles to flatten against both surfaces and effectively screens the boundary layer from the remainder of the solution. (This action is intermittent because the bubbles grow, escape, and reform.) Thus, silicate concentration can build up near the surface and promote silicate nucleus formation.

It has been proposed[3] that pyramid formation in the KOH/IPA/$H_2O$ system is caused by silicate precipitation on the surface. These random precipitates protect the top of the pyramid during formation. A similar scheme is envisioned here, except that the protection may be by silicate nuclei growing on the silicon surface rather than by random precipitation in the solution. Figure 1 shows the stages from the formation of protective nuclei to the completion of texturing. The effectiveness or uniformity of the pyramid formation is related to the formation and density of these protected sites.

## 6. Experimental

In order to quantify the various effects, pyramid formation was measured for the various additives and conditions. This was done by using texturing times that gave only a small fraction of coverage of the surface by pyramids, which allowed them to be counted separately. Texturing was done at 90°C. Data were taken at two NaOH concentrations: 4% and 1%. Chem-mechanically polished surfaces were used to eliminate the roughness effect.

Figure 2 compares the results of:

1) 4% aqueous NaOH for 10 minutes.
2) 4% aqueous NaOH for 10 minutes, with 1% IPA (by volume) added.
3) 4% aqueous NaOH for 10 minutes, with 1% $Na_2SiO_3$ solution added.
4) 4% aqueous NaOH for 10 minutes, with 0.51 mm proximate surface.

Pyramids were counted from 1/2 to full size. Figure 2 shows that each additive or promoting condition causes a 2-10X increase in pyramid density for this set of conditions.

Figure 3 compares the results of:

1) 1% NaOH for 5 minutes.
2) 1% NaOH for 5 minutes, with 1% IPA added.
3) 1% NaOH for 5 minutes, with 2% IPA added.
4) 1% NaOH for 5 minutes, with 1% $Na_2SiO_3$ solution added.
5) 1% NaOH for 5 minutes, with 2% $Na_2SiO_3$ solution added.
6) 1% NaOH for 5 minutes, with 0.51 mm proximate surface, vertical.
7) 1% NaOH for 5 minutes, with 0.51 mm proximate surface, 6° off horizontal.

3. A. Fissore, B. Waldman and G. M. Oleszek, *J. Electrochem. Soc.* **124**, 216C (1977).

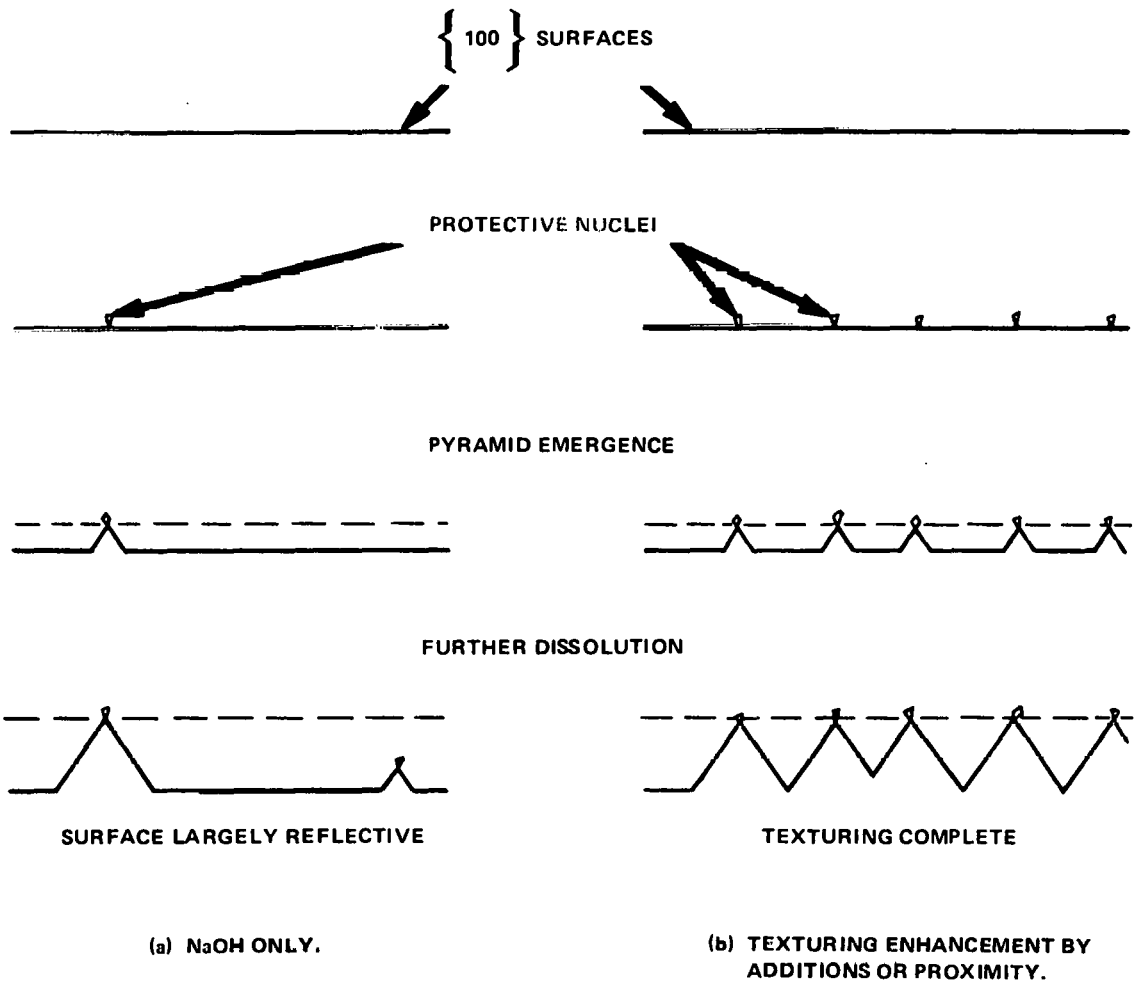


Figure 1. Pictorial Representation of Texturing Process and Enhancement Effects

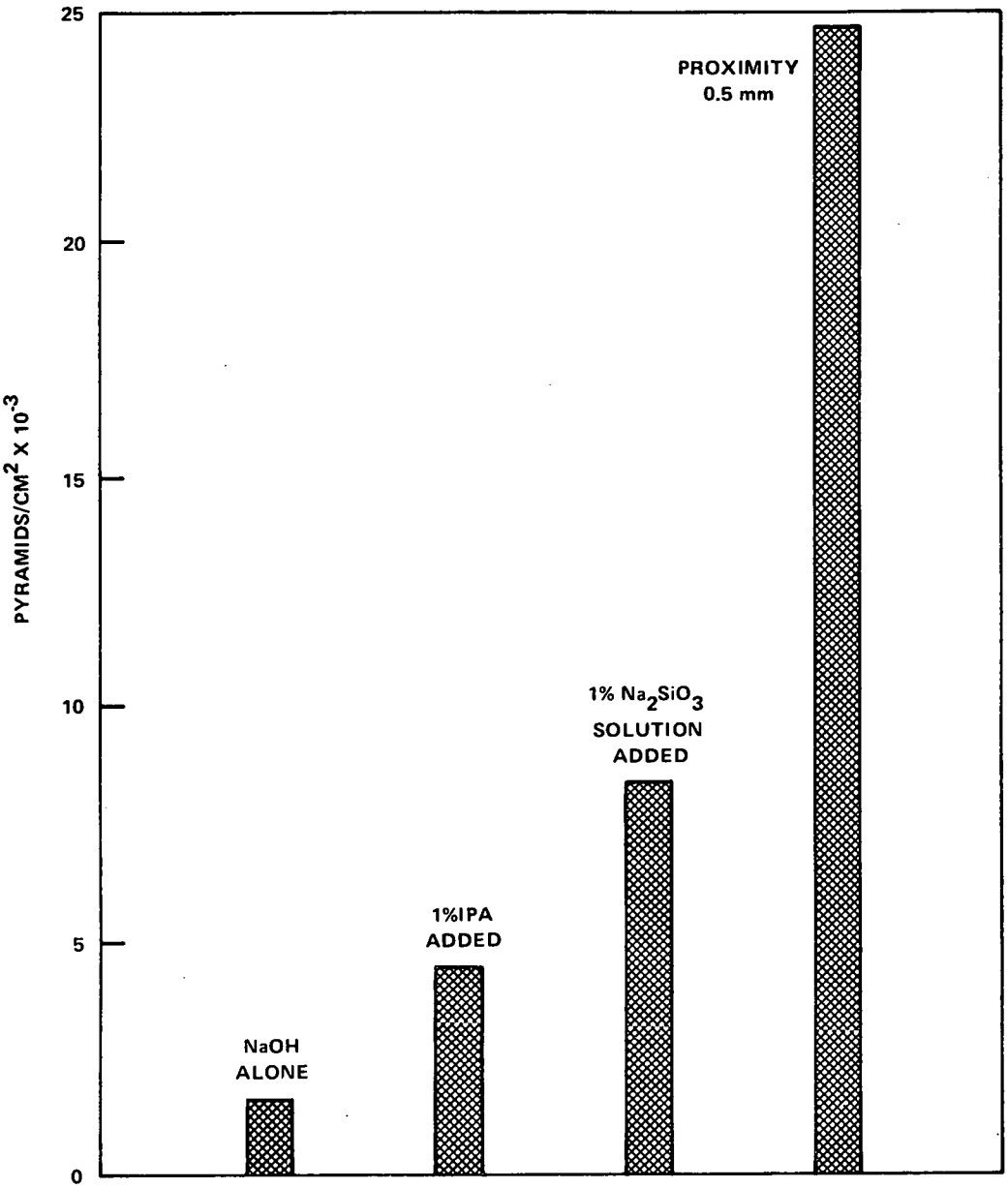


Figure 2. Effects of Various Enhancement Conditions of Pyramid Density in 4% NaOH for 10 Minutes at 90°C

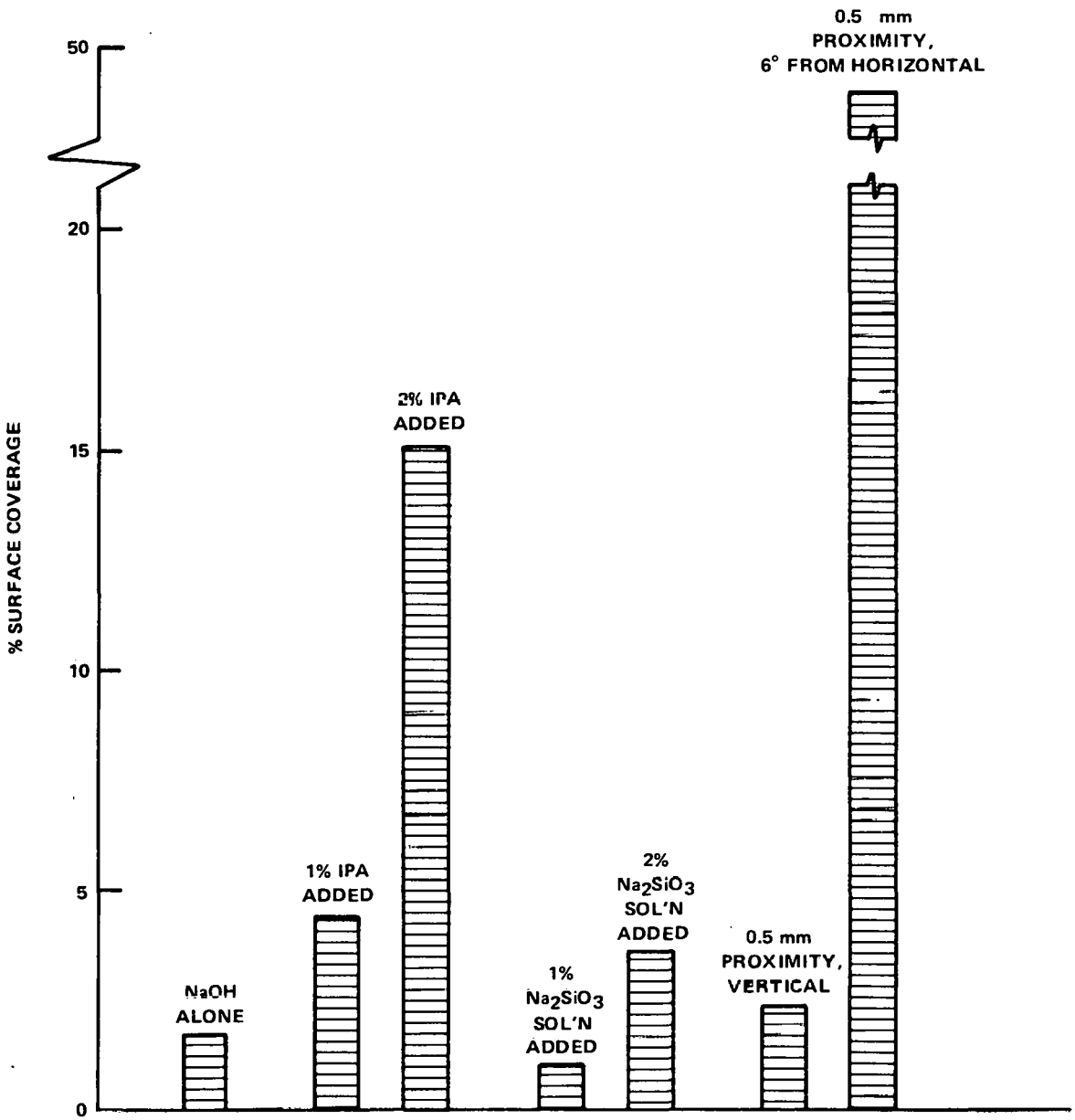


Figure 3. Effects of Various Enhancement Conditions of Pyramid Density in 1% NaOH for 5 Minutes at 90°C

In this case, total areas covered by the pyramids were measured and plotted. This study shows similar results to the foregoing one and that a threshold concentration exists for some additives.

Microscopic examination of the pyramidized surfaces showed a definite connection between silicate growth nuclei and pyramid formation. Such nuclei were present after any pre-etching in concentrated sodium hydroxide and probably accounted for a fraction of the pyramids seen from the unenhanced texturing solution. Often the growth nuclei could still be seen connected to the pyramids even after water rinsing and drying. Figure 4 shows an example as seen by the scanning electron microscope.

Combined use of additives or proximity greatly enhances pyramid formation – complete texturing can be achieved at reasonable etch times using any two of the additives or conditions noted in the foregoing.

At this stage, texturing appears to be controlled by the formation of $Na_2SiO_3$ growths on the ⟨100⟩ surface and texturing efficiency can be enhanced by any of the several techniques or combinations of the techniques discussed above.

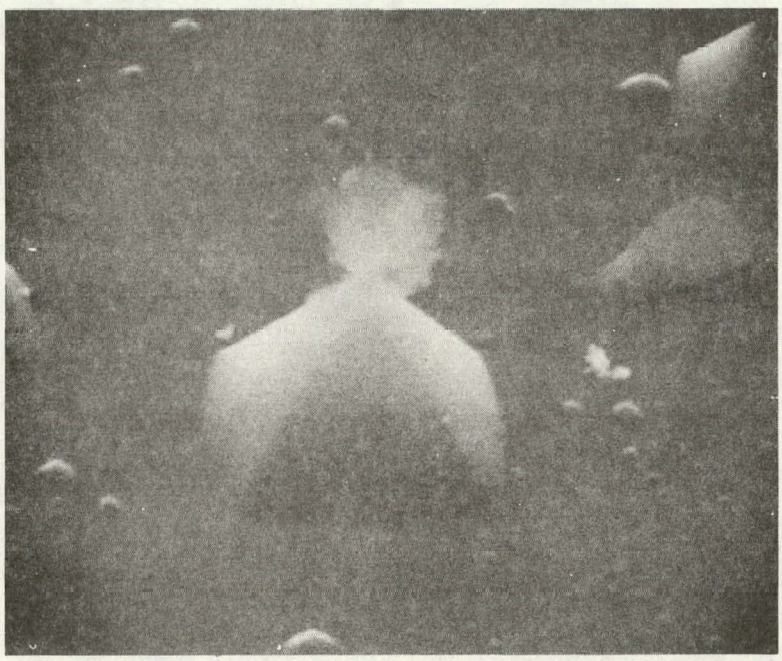

Figure 4. Silicate Growth Nucleus at Top of Texturing Pyramid

## B. PLASMA ETCHING

No results to report at this time.

## C. DIFFUSION

A diffusion sensitivity experiment containing a matrix of temperatures from 800°C-950°C at times ranging from 7 minutes to 140 minutes was run during the Phase I contract. Further analysis of the minority carrier lifetime, measured by the Surface Photovoltage (SPV) technique, before and after processing as a function of processing temperature and time show the following trends:

1) Diffusion temperature >950°C causes substantial degradation in lifetime (9 $\mu$s → 5 $\mu$s).

2) Long diffusion time with phosphorus is beneficial to lifetime (9 $\mu$s → 11 $\mu$s).

3) Long diffusion time without phosphorus degrades lifetime (9 $\mu$s → 7 $\mu$s).

These trends are being evaluated in this study.

Based on the above observations on the effect of high temperature, ≥950°C, processing steps on base minority carrier lifetime, it appears desirable to minimize time at high temperatures and eliminate temperatures greater than 900°C. On the further observation that dark current density for test diodes fabricated on the wafer with hexagon cells was significantly higher for the diodes than it was for the solar cells, a further hypothesis was made. Test diode dark current density is lower for diodes with deeper junctions. Base resistivity of these test devices was 0.6 Ω-cm, therefore dark current is dominated by current injected into the diffused region. The diodes have a high percentage of the surface area (51%) covered by metal and the solar cells have a low percentage of the surface area (<10%) covered by metal, therefore:

1) Dark current for the solar cell may be controlled by current injection in the diffused layer area covered by the contact metallization

2) Deeper diffusion under the contact metal area should reduce dark current (and raise $V_{OC}$) in the solar cell.

A series of test runs have been made to test these hypotheses, using several base resistivities, lower temperature oxide formation steps and a deep $N^+$ diffusion under the metal contact regions. In all cases the collecting junction diffusion is ≈0.3 $\mu$m deep and formed by an 850°C, $POCl_3$ diffusion. The steam oxidation step was run at 950°C and 900°C and in some cases a low-temperature chemical vapor deposition from silane was used to form the first oxidation. The deep $N^+$ diffusion, ≈1.0 $\mu$m, was formed by a masked two-step 850°C, $POCl_3$ diffusion. The data is summarized in Table 1.

Table 1. Process Lot Data – $POCl_3$ Diffusion

| Lot No. AAAP-II- | Base Resistivity Ω-cm | Oxide Type (°C) | Deep $N^+$ | Avg* $V_{OC}$ (V) | Avg* $I_{SC}$ (A) |
|---|---|---|---|---|---|
| 4 | 1.5 | 950 | No | 0.589 | 1.207 |
| 10 | 1.5 | 950 | No | 0.589 | 1.190 |
| 11 | 1.5 | 950 | Yes | 0.598 | 1.163 |
| 24 | 1.5 | 900 | No | 0.535† | 0.710† |
| 18 | 1.5 | Silane | No | 0.594 | 1.257 |
| 26** | 1.5 | Silane | No | 0.588 | 1.247 |
| 24 | 0.9 | 900 | No | 0.595 | 1.243 |
| 26** | 0.9 | Silane | No | 0.595 | 1.283 |
| 4 | 0.6 | 950 | No | 0.591 | 1.160 |
| 16 | 0.6 | 950 | Yes | 0.608 | 1.203 |
| 25 | 0.6 | Silane | Yes | 0.605 | 1.247 |
| 25 | 0.2 | Silane | Yes | 0.606 | 1.083 |

*Averages based on best 3 of 4 solar cells.

**Square cell design – cell area = 37.2 $cm^2$, all other data is for hexagonal cell area = 37.7 $cm^2$.

†This lot may have been contaminated, see Cell Processing.

Lots AAAP-II-4 and -10 are representative of hexagonal cells produced by the standard baseline process using 1.5 Ω-cm material. Lots AAAP-24, -18 and -26 represent the baseline process using a 900°C oxidation step or CVD silane oxide. (The data from lot AAAP-II-24 is questionable due to a probable Cu contamination during February, see Cell Processing.) Note that lots AAAP-II-18 and -26 using silane oxide give $I_{SC} \approx 4\%$ higher than the baseline. Lot AAAP-II-11 uses the baseline process with the deep $N^+$ diffusion under the contact metallization. $V_{OC}$ is ≈9-10 mV higher for this configuration. The increase in $V_{OC}$ is limited by the base resistivity in this case. The increase in $I_{SC}$ for the silane oxide lots implies an improvement in base minority carrier lifetime as predicted.

Lots AAAP-II-24 and -26 were run on 0.9 Ω-cm material using a 900°C steam oxidation and a silane oxide, respectively. Both lots give very good $V_{OC}$ and $I_{SC}$ values with the silane oxide lot ≈3% higher than the 900°C oxidation lot. $V_{OC}$ for the 0.9 Ω-cm materials is ≈6 mV higher than for the 1.5 Ω-cm material, as expected.

Lots AAAP-II-4, -16 and -25 were run on 0.6 Ω-cm material, using the 950°C oxidation (baseline) and silane oxide. The deep $N^+$ diffusion was used on lots AAAP-II-16 and -25. Lot AAAP-II-16 using the deep $N^+$ shows an improvement in both $V_{OC}$ and $I_{SC}$ over the baseline process (AAAP-II-4). The $V_{OC} = 0.608$ V is the best we have seen for large area cells, the increase in $I_{SC}$, ≈2%, is unexpected and may not be significant. The silane oxide lot with a deep $N^+$, AAAP-II-25, gave excellent $V_{OC}$ and $I_{SC}$ values, as expected.

Lot AAAP-II-25 run on 0.2 Ω-cm material using silane oxide and deep $N^+$ diffusion gives high $V_{OC}$, 0.606 V, but lower $I_{SC}$. The lower $I_{SC}$ is due to the reduced minority carrier lifetime in the low resistivity base material.

In summary, the hypotheses that lower processing temperatures (<900°C) would improve current collection, $I_{SC}$, and that a deeper $N^+$ diffusion under the contact metallization would improve $V_{OC}$, appear to be valid. Under optimum conditions, an improvement of 5% to 10% in $V_{OC}$ might be realizable.

Results on As ion implant (II) and As polymer dopant are summarized in Tables 2 and 3. Lots AAA-II-5, -9 and -19, all use the baseline process with the As II operation in place of the $POCl_3$ diffusion. Solar cells were fabricated with and without a 1000°C, 10-minute anneal after implant and with and without a 850°C $POCl_3$, 5-minute gettering step. Both $V_{OC}$ and $I_{SC}$ are lower than with the baseline process (compare to lots AAAP-II-4 and -10, Table 1). Lot AAAP-II-19 appears to have a cell number identity problem (C-6 and C-8 are reversed?). Ion implant has not yielded results equivalent to the baseline process in this work. Further work will continue.

Lots AAAP-5 and -9 were run on 1.5 Ω-cm material using the baseline process with As polymer dopant diffusion in place of the $POCl_3$ diffusion. A 1000°C, 100-minute diffusion cycle is used to obtain a 60 to 80-Ω/□, 0.3-μm diffusion. Cells were fabricated with and without a $POCl_3$, 850°C, 5-minute gettering step. Both $V_{OC}$ and $I_{SC}$ are lower than with the baseline process (compare to lots AAAP-II-4 and -10, Table 1). The $POCl_3$ gettering step offers no improvement. Further work will continue.

Table 2. Results of Arsenic Ion Implanted Lots

| Lot No. AAAP-II- | Cell No. | Base Resistivity Ω-cm | Oxide Type (°C) | Anneal Temp (°C) | Getter Temp (°C) | $V_{OC}$ (V) | $I_{SC}$ (A) |
|---|---|---|---|---|---|---|---|
| 5 | 13 | 1.5 | 950 | – | 850 | 0.534 | 0.84 |
| | 14 | 1.5 | 950 | – | 850 | 0.539 | 0.89 |
| | 15 | 1.5 | 950 | – | | 0.490 | 1.1 |
| | 16 | 1.5 | 950 | – | – | 0.495 | 1.1 |
| 9 | A-9 | 1.5 | 950 | 1000 | 850 | 0.552 | 0.80 |
| | A-10 | 1.5 | 950 | 1000 | 850 | 0.563 | 0.89 |
| | A-11 | 1.5 | 950 | 1000 | 850 | 0.556 | 0.84 |
| | A-12 | 1.5 | 950 | 1000 | – | 0.567 | 0.89 |
| 19 | C-6 | 1.5 | 950 | 1000 | – | 0.575 | 1.0 |
| | C-7 | 1.5 | 950 | 1000 | 850 | 0.579 | 1.1 |
| | C-8 | 1.5 | 950 | 1000 | 850 | 0.526 | 0.72 |

Table 3. Results of Arsenic Doped Polymer Lots

| Lot No. AAAP-II- | Cell No. | Base Resistivity Ω-cm | Oxide Type (°C) | Diffusion Temp (°C) | Getter Temp (°C) | $V_{OC}$ (V) | $I_{SC}$ (A) |
|---|---|---|---|---|---|---|---|
| 5 | 6 | 1.5 | 950 | 1000 | – | 0.523 | 0.68 |
| | 9 | 1.5 | 950 | 1000 | – | 0.528 | 0.71 |
| | 11 | 1.5 | 950 | 1000 | 850 | 0.532 | 0.72 |
| 9 | A-1 | 1.5 | 950 | 1000 | 850 | 0.551 | 0.91 |
| | A-2 | 1.5 | 950 | 1000 | 850 | 0.536 | 0.65 |
| | A-8 | 1.5 | 950 | 1000 | 850 | 0.527 | 0.60 |
| | A-5 | 1.5 | 950 | 1000 | – | 0.536 | 0.75 |
| | A-6 | 1.5 | 950 | 1000 | – | 0.538 | 0.80 |
| | A-7 | 1.5 | 950 | 1000 | – | 0.529 | 0.74 |

## D. CELL PROCESSING

### 1. Cell Design

The truncated square cell design has been completed through processing (see Table 1, lot AAAP-II-26). Process results were very good. This cell will be used for module fabrication.

### 2. Processing

Results from processing large-area hexagonal cells (37.7 $cm^2$) are reported in Tables 1, 2 and 3 for $POCl_3$, As II and As polymer dopant, respectively. Lot-to-lot reproducibility is excellent.

A contamination problem was encountered in early February that appears to be due to a Cu contaminant in the Al evaporation source. Several lots appear to have suffered from severe lifetime degradation after the Al alloy operation. The results from these lots are at best questionable. The Al evaporation source has been changed, the Al alloy furnace tube has been cleaned. Several process lots that were questionable have been scrapped. Several process lots that were questionable were completed and evaluated. All questionable lots are identified. For example, lot AAAP-II-24, Table 1 is questionable. The low $V_{OC}$ and $I_{SC}$ are apparently the result of very low minority carrier lifetime in the base region. No explanation other than the Cu contamination is apparent at this time.

Lot AAAP-II-8 was run using a 3.7-cm hexagonal pattern on 0.375 mm thick wafers to characterize crystal 278 for Tandem Junction Cell (TJC) fabrication. The standard baseline process was used. Diode cells with no surface texture and $SiO_2$ AR coating gave good photoresponse, $V_{OC}$ = 0.59 V, $J_{SC}$ = 30 mA/$cm^2$. Lifetime after processing was ≈11 μs as measured by the short circuit current method. This crystal, 0.8 to 1.0 Ω-cm, will be used for TJC fabrication.

Four lots of TJC cells using the original mask set (8 fingers/2 cm on the 2 X 2-cm cells) were completed. These results are reported under High Efficiency Cell Development. Several TJC lots are in process, including As polymer dopant using the redesigned pattern with 12 and 16 fingers/2 cm on the 2 X 2-cm cells.

The Cu contamination problem severely impacted several TJC lots completed in February. Some results are reported in the High Efficiency Cell Development section of this report.

All questionable results are being repeated where the data is significant.

## E. MODULE FABRICATION

Detailed module design versus cost reviews are continuing to identify areas of cost reduction in the module fabrication area. Prior analysis points to a packing efficiency in excess of 90% for module sizes 0.664 m by 1.216 m or greater. Using this module size, Table 4 was generated for a 10 MW facility. The data is plotted in Figure 5 to show the cumulative effect of material, labor (including OH), depreciation and factory OH. At all module efficiencies, material is the dominant cost factor in the present design. No material substitutions are available at this time that can provide the 20-year lifetime goal. Unique design characteristics are being continuously evaluated to identify areas for material cost reductions. The present projection of $0.229 to 0.279 per watt for model efficiencies of 19 to 16% are too high.

Table 4. $/W As A Function Of Various Efficiencies

| Module Efficiency | Watts per Module | Modules per 10 MW | Material | Labor | Depreciation | Factory OH | Total |
|---|---|---|---|---|---|---|---|
| 10 | 80.7 | 126,445 | 0.245 | 0.111 | 0.028 | 0.022 | 0.406 |
| 13 | 105 | 96,689 | 0.189 | 0.090 | 0.028 | 0.018 | 0.325 |
| 16 | 129 | 78,579 | 0.154 | 0.073 | 0.028 | 0.015 | 0.270 |
| 19 | 153 | 66,607 | 0.129 | 0.059 | 0.028 | 0.013 | 0.229 |
| 22 | 177 | 57,651 | 0.112 | 0.048 | 0.028 | 0.011 | 0.199 |

Module Size = 0.664 m X 1.216 m
Module Area = 0.807 $m^2$
Total Module Cost = $19.80 (excluding cells)

Six substrates and lock frames have been fabricated to evaluate design, handling, and potential problems associated with processing. Previous substrates had been formed with 18-gauge (0.0478-inch, 1.21-mm) steel using a soft die. The surface of the substrate designed to accept the cells row mounting was convexed (bowed) by 0.040 inch to 0.050 inch (1.02-1.27 mm). After

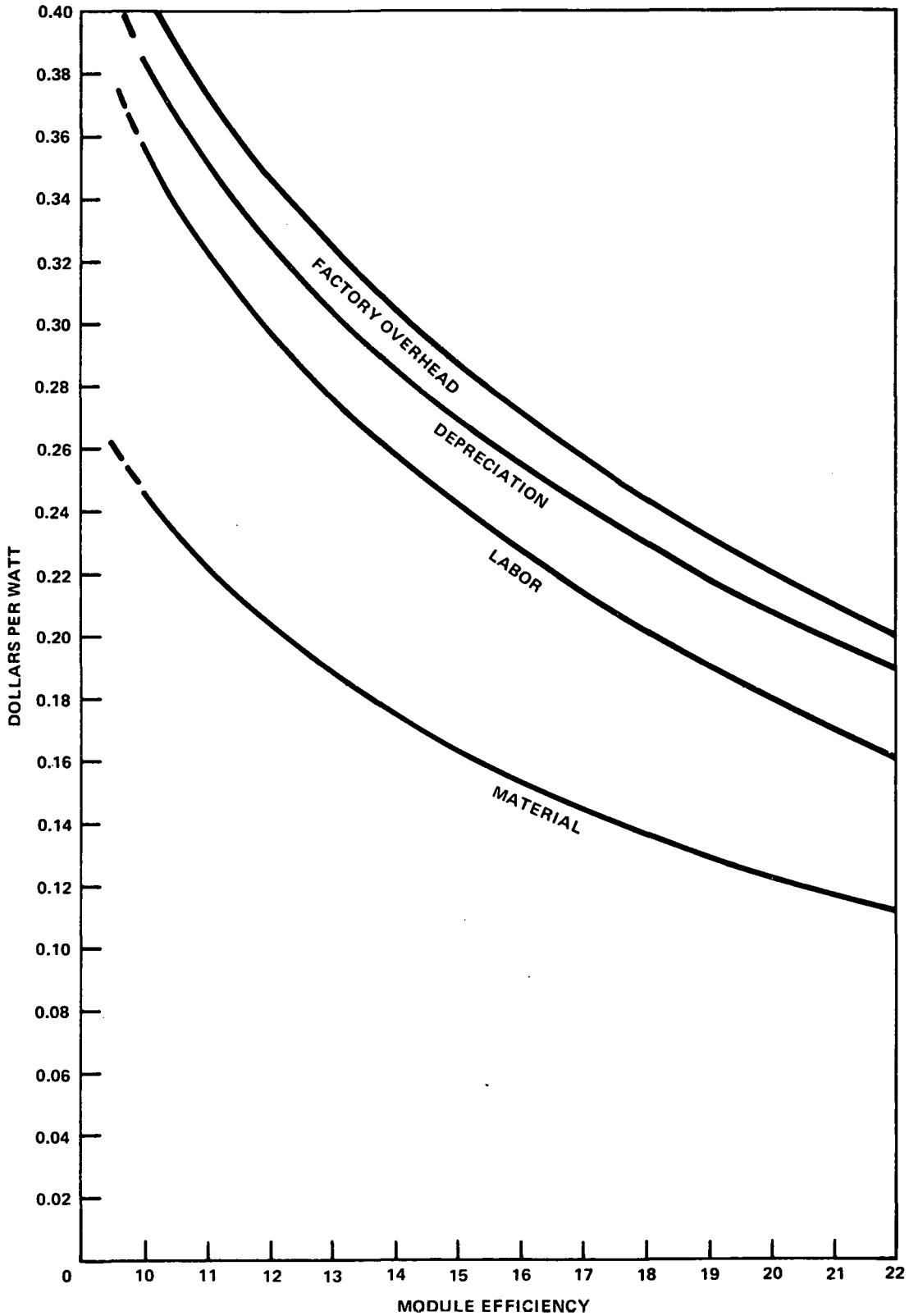


Figure 5. Module Costs as a Function of Module Efficiency

porcelainizing, convexity increased to 0.0938 inch (2.38 mm), making the substrates useless for cell mounting. With properly designed hardened dies, the substrates could have been made at this gauge. Design reviews, however, concluded that 18-gauge material was heavier than required for a substrate. Six substrates were formed from 20 gauge (0.0359 inch, 0.91 mm) using a soft die. Coarse measurements indicate that there is an increase in the depth of the substrate recess area from 0.150 inch (3.81 mm) at the peripheral boss area to 0.200 inch (5.08 mm) approximately one to 1.5 inches into the recess area. The remainder of the recess area is flat at 0.200 inch (5.08 mm). More precise measurements are now being taken prior to porcelainizing. The same measurements will be repeated after porcelainizing. A substrate and lock frame assembly has been sent to Alpha Metals Inc., and to Ervite Corporation for porcelainizing and subsequent evaluation. The review is intended to evaluate product design and process compatibility.

Front and back bus bars were fabricated. By design, the front bus will be copper clad Invar with an equilateral triangular cross section. The Invar is used to more closely match the thermal expansion coefficients of the bus with the silicon cell. The process for triangular cross section involves bonding copper to a rod and then drawing it into the desired form through a turks head. Invar wire is not available in-house but has been ordered and is expected in during the middle of March. To evaluate the manufacturing process, copper clad alloy 42 wire was used. Process review concluded that a 20% reduction would be incurred during the forming process. Consequently, a 0.162-inch diameter starting wire would be required to result in an equilateral triangle with 0.118 inch (3.00 mm) per side. However, this proved to be false. Very little reduction in cross-sectional area was incurred so starting wire size was decreased to 0.134 inch (3.40 mm). Good fill was achieved at this diameter but it required six passes through the rolls and some finning resulted at each apex. Finning was easily removed with steel wool. Starting wire cross-sectional areas will be obtained which closely match the desired triangular cross-sectional area. This closer matching should eliminate finning and will reduce the number of passes required to form the triangular cross section.

Back bus bars of copper clad Invar have also been made with a 0.0029-inch/0.0176-inch/0.0029-inch (0.074-mm/0.45-mm/0.074-mm) thickness combination or a 12.5%/75%/12.5% ratio. The Cu/Invar/Cu was bonded and rolled to 0.0235 inch (0.60 mm) and then sheared to the desired width. Present Invar (alloy 10) price structure is

| | |
|---|---|
| $4.16/lb | small quantities (samples) |
| $3.24/lb | large quantities (10,000 lbs) |

| | Annealed | Tempered | |
|---|---|---|---|
| Flatness | Good | Fair | |
| Thickness | 1/8" | 1/8" | |
| Sample orders or small lots | $1.00/ft$^2$ | $2.00/ft$^2$ | |
| Standard Size (34" X 76") | 0.50/ft$^2$ | 0.69/ft$^2$ | truck load |
| Cut Size (module size) | 0.68/ft$^2$ | 0.94/ft$^2$ | |

Silicon sealants, adhesives, and potting mediums are presently in-house.

Two items in our module clearly need very serious evaluation. First is the glass cover. Economic justification must be evaluated in terms of transmittance, mechanical strength, efficiency and cost. Second is the bus bars. The largest single cost of the module is the bus bars. Total bus bar costs approach $7.00 per module. This represents approximately 30% of the total module cost. This cost will have to be justified in terms of thermal expansion, mechanical integrity, resistance to corrosion and electrical characteristics. Other modes of bus barring will be explored and evaluated.

Process validation experiments using condensation soldering were successful. Triangular front bus bars (Cu-Alloy 10) were soldered to the plated Ag cell metallization using eutectic Pb/Sn solder. Mechanical adhesion was very good.

From the data in Table 4 relating module add-on cost ($/W) as a function of various module efficiencies a correlation can be drawn between cell efficiency, packing efficiency and module add-on cost. Figure 6 is a plot of module efficiency versus packing efficiency for various cell efficiencies and versus module add-on cost ($/W). This particular figure is drawn for a module add-on cost of $19.80 for a 0.664 m X 1.216 m module. The figure demonstrates the need for high efficiency in both cells and module to achieve low module add-on cost. The figure can be used as a nomograph. From the packing efficiency of the module, proceed vertically to the line for a given cell efficiency, dotted line A for 90% packing efficiency and 15% cell efficiency, to determine module efficiency, 13.5% in this case. Then proceed horizontally to the module add-on cost curve, dotted line B. From this intersection, proceed vertically to determine the module add-on cost, dotted line C, $0.314/W in this case. For this module configuration, maximum packing efficiencies for round and square cells are shown on the bottom ordinate in the figure. As the module cost changes, the module add-on cost curve will move but the general shape of the curves is the same.

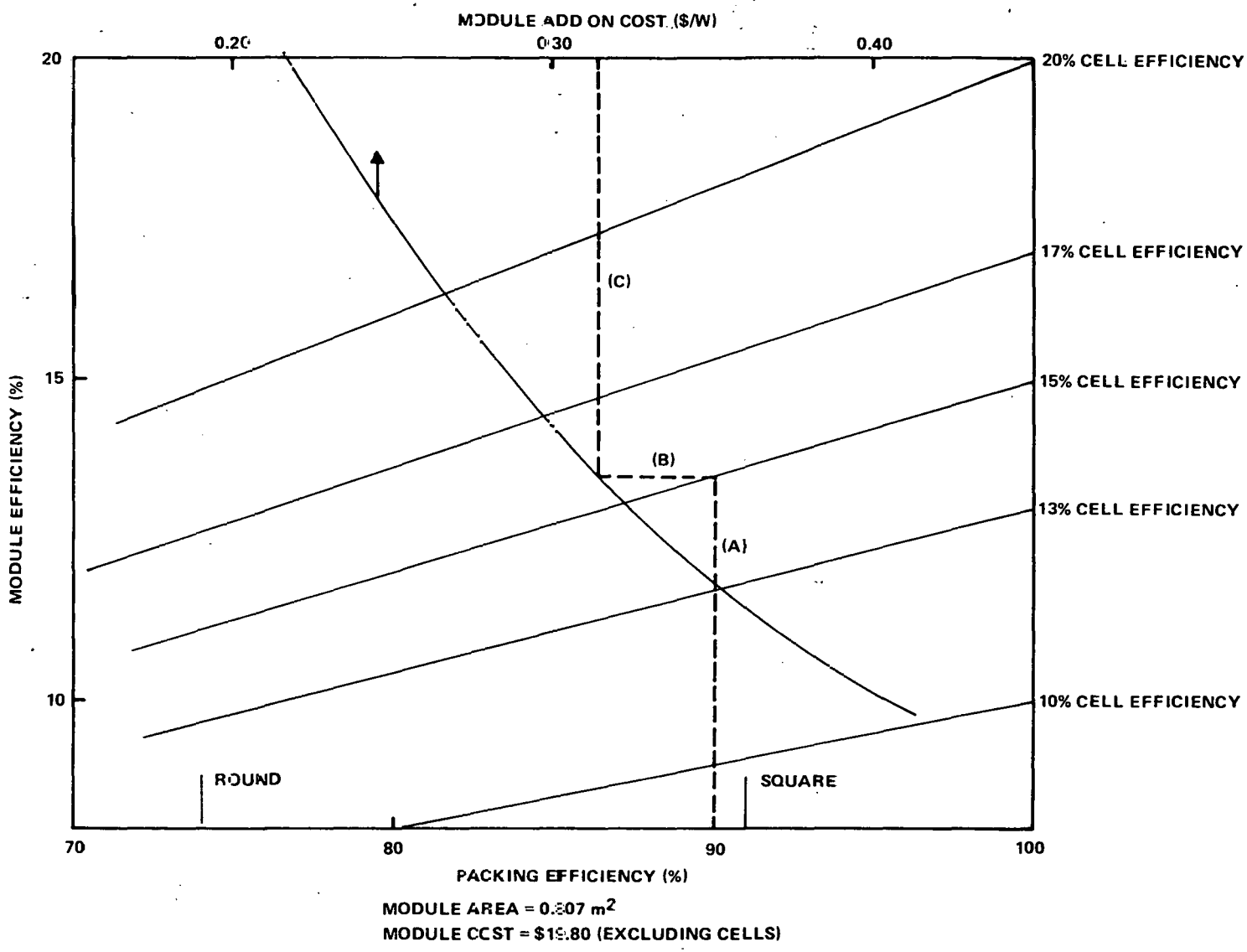


Figure 6. Module Add-On Cost Nomograph

This approach can be used to analyze the impact of cell efficiency on module add-on costs and for given module designs and costs, establish lower limits for acceptable cell efficiency. In this particular case, module cost is too high to meet the 1986 goal but the magnitude of the needed cost reduction can be readily established.

## F. HIGH EFFICIENCY CELL DEVELOPMENT

A number of lots of thin TJCs were processed this quarter. The first comparison was by base material resistivity. Lot AAAP-II-7 was run on crystal 370, 0.2-0.3 Ω-cm, $\tau_{SPV} < 1\ \mu s$; lot AAAP-II-12 was run on crystal 278, 0.8-1.0 Ω-cm, $\tau_{SPV}$ = 8-10 μs. Both lots were run using the standard process ($POCl_3$, 850°C diffusion). The data is summarized in Table 5.

Table 5. TJC Resistivity Data

| Lot Number | Thickness (μm) | $\tau_{SPV}$ (μs) | $\tau^1$ (μs) | $J_{SC}$ (mA/cm$^2$) |
|---|---|---|---|---|
| AAAP-II-7 | 110 | <1 | 1.2[2] | 12 |
| AAAP-II-7 | 90 | <1 | 1.2[2] | 16 |
| AAAP-II-12 | 75 | 8-10 | 11[3] | 31 |

1. Lifetime after processing.
2. Measured by diode recovery (3 to 4 X greater than SPV).
3. Measured by short circuit current method.

Two conclusions can be drawn from this data. First, $J_{SC}$ for back side only collection is strongly dependent on minority carrier lifetime at thicknesses near 100 μm. Lot AAAP-II-12 gives $J_{SC}$ approximately twice that of AAAP-II-7. Second, for low lifetime, $J_{SC}$ is strongly dependent on thickness. This $J_{SC}$-thickness relationship is even more strongly supported by the following experiments.

Four lots of thin TJCs were completed on crystal 278 material (including lot AAAP-II-12 above). Lots AAAP-II-12 and -23 represent a baseline process, lots AAAP-13 and -14 use As polymer dopant and As ion implant, respectively, to achieve a very shallow, ≈500 Å, front $N^+$ layer on the TJC. Lot AAAP-II-23 was subjected to Cu contamination and lots AAAP-II-13 and -14 may have been contaminated. All lots featured a textured front surface and back contacts only. Cell thickness ranged from 67 to 110 μm.

Table 6 lists the lifetime after processing, measured by the short circuit current method, $J_{SC}$ range for all thicknesses and $V_{OC}$ for each of these lots run on crystal 278. The only difference between lots AAAP-II-12 and -23 is the back side contact pattern and the apparent Cu contamination on lot AAAP-II-23. Note the very severe impact on cell performance and lifetime

Table 6. TJC Evaluation

| Lot No. | $\tau$ ($\mu$s) | $J_{SC}$ (mA/cm$^2$) | $V_{OC}$ (V) |
|---|---|---|---|
| AAAP-II-12 | 11 | 24-31 | 0.58-0.59 |
| AAAP-II-13 | 2 | 13-23 | 0.55-0.57 |
| AAAP-II-14 | ≈0.03 | 1-11 | 0.39-0.53 |
| AAAP-II-23 | ≈0.03 | 1-8 | 0.4 -0.5 |

due to Cu contamination. Log current density versus thickness is plotted in Figure 7 for lots AAAP-II-12, -13 and -14. The trend to higher $J_{SC}$ for thinner cells is evident for all samples, even with the low lifetime observed on lots AAAP-II-13 and -14. Only the data on lot AAAP-II-12 can be taken at face value at this time. The expected higher $J_{SC}$ for thinner $N^+$ layers was not observed due to the severe lifetime degradation problem. Thin TJC lots are in process to repeat the conditions that are in question due to the Cu contamination problem.

The improved back contact pattern, with 12 and 16 fingers/2 cm, were completed. Lot AAAP-II-23 used this improved contact pattern. Although low lifetime degraded solar cell performance, the improved pattern masks were verified. All future processing will use this denser contact pattern.

Spectral response was measured* on two 110-$\mu$m thick TJCs. Measurement using low-intensity chopped monochromatic light gives a response significantly lower than anticipated for a conversion efficiency of 12% (AM0). When the cell was flooded with a white light (intensity ≈0.5 sun) and the low intensity chopped monochromatic light was superimposed, a significantly higher spectral response was observed at all wavelengths. The data for one cell is shown in Figure 8. Several features are worthy of note: the peak spectral response for the TJC occurs at a longer wavelength, ≈1.0 $\mu$m, than is typical of conventional solar cells, the thin TJC exhibits significant response at 1.1 $\mu$m, the upper limit of the measurement, and significant enhancement of the blue response occurs when the cell is flooded with white light. The longer wavelength peak response is expected for a thin TJC using back contacts. The high spectral response at 1.1 $\mu$m is probably related to the long wavelength peak response. Both the response at short wavelengths (0.4 $\mu$m) and the enhancement in this region were not expected since these cells have no contacts on the front (illuminated) junction.

Present TJCs are fabricated from Czochralski grown Si. This represents an inefficient use of the Si crystal since a large fraction of the Si crystal is wasted in the preparation of thin, 50-100 $\mu$m, substrates or conventional, 200-300 $\mu$m, substrates. However, if one ignores the present day Si sheet fabrication and looks at photovoltaic power as a function of Si volume (or mass) used, the TJC with

*Measurements were performed by B. Anspaugh, JPL.

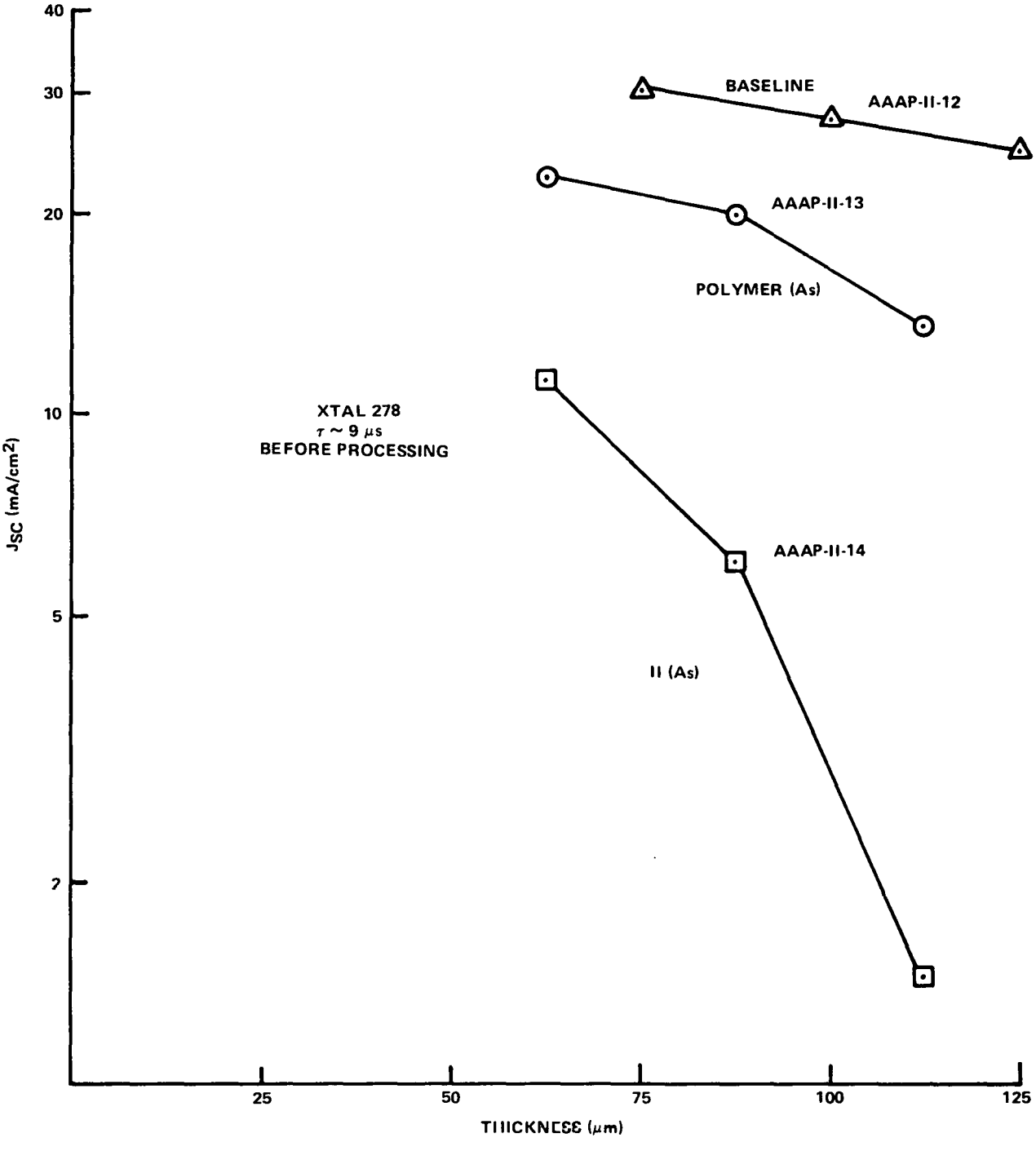


Figure 7. Current Density versus Thickness for TJC Structures

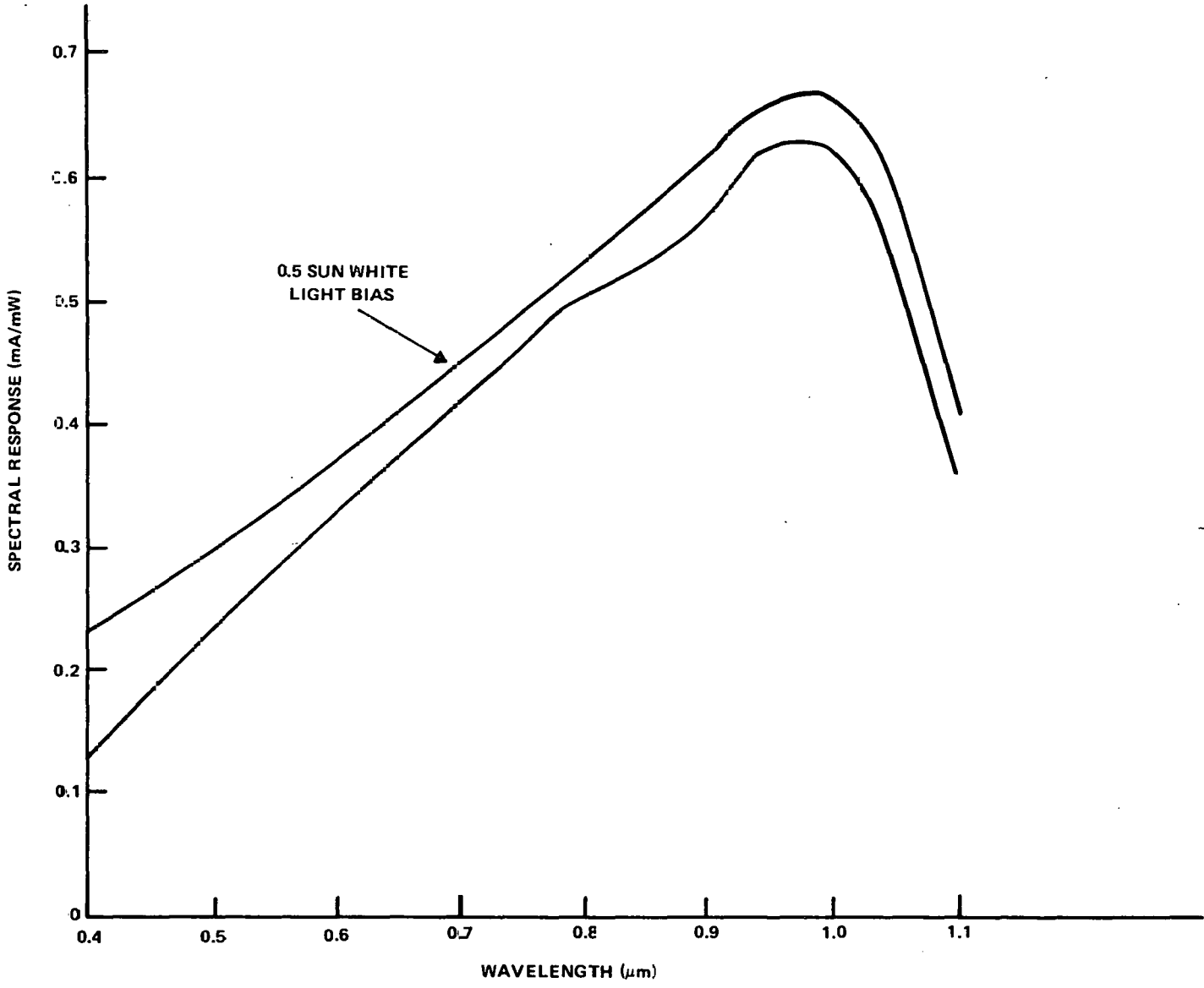


Figure 8. Spectral Response of TJC

15% efficiency at a 100 $\mu$m thickness is at least a factor of 2-3 better than a conventional solar cell with 15% efficiency at a 200-300 $\mu$m thickness. At a thickness of 50 $\mu$m with an efficiency of only 15%, the TJC would be at least a factor of 4-6 better than a conventional solar cell with 15% efficiency. Considering the high cost content of Si sheet, this represents a significant area for cost improvement in module fabrication. Direct conversion of polycrystalline Si to Si sheet of 50-100 $\mu$m thickness would eliminate the present-day inefficiencies of converting Cz crystal to thin wafers. It must be remembered that the TJC uses a textured surface and suitable Si sheet (or ribbon) must be amenable to a texturing process. This type of step function cost improvement must be pursued if the 1986 LSSA goals are to be met.

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## SECTION III
## CONCLUSIONS AND RECOMMENDATIONS

The texture etch process is controlled by the formation of $Na_2SiO_3$ growths on the ⟨100⟩ surface. The proximity texturing effect is a special example of the general texturing phenomena on ⟨100⟩ surfaces.

High-temperature operations, at temperatures >900°C, cause a reduction in $J_{SC}$.

$V_{OC}$ is limited by the shallow junction under the contact metallization. Deeper junctions under the contact metallization yield higher $V_{OC}$.

For the TJC structure using back contacts, $J_{SC}$ shows a significant increase as cell thickness decreases down to at least 67 $\mu$m. The magnitude of $J_{SC}$, is strongly dependent on base minority carrier lifetime. Further work must be continued on this high-efficiency structure as an efficient use of Si to generate photovoltaic power.

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## SECTION IV
## NEW TECHNOLOGY

No new technology has been disclosed this quarter.

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## SECTION V
## PROGRAM SUMMARY

Figure 9 shows the current work plan status. All scheduled activities are in process. No problems are apparent at present that will prevent attaining the indicated milestones.

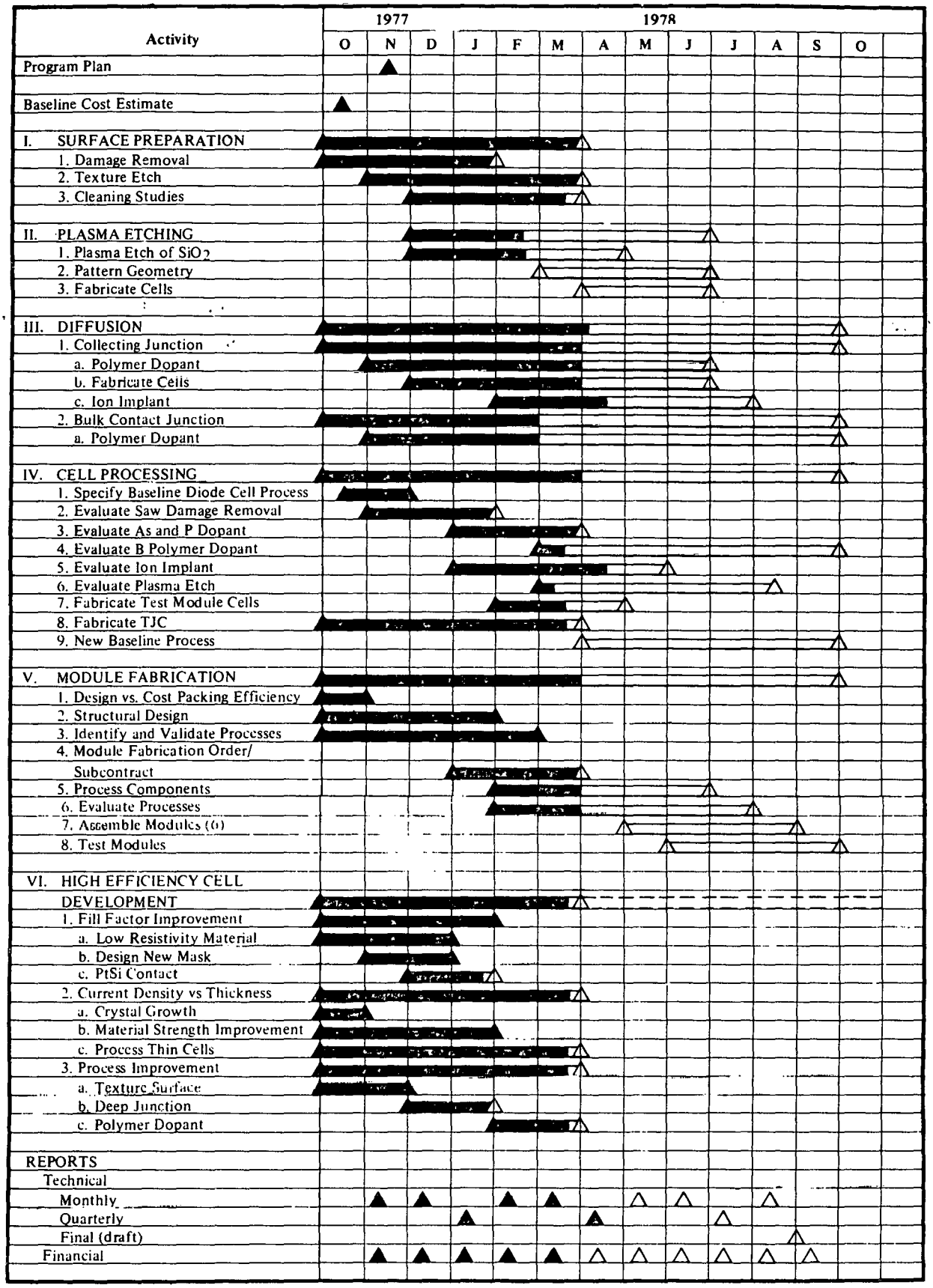


Figure 9. Work Plan



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