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A Monolithically Integrated Detector-Preamplifier on High-Resistivity Silicon

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Abstract- A monolithically integrated detector-preamplifier on high-resistivity silicon has been designed, fabricated and characterized. The detector is a fully depleted p-i-n diode and the preamplifier is implemented in a depletion-mode PMOS process which is compatible with detector processing. The amplifier is internally compensated and the measured gain-bandwidth product is 30 MHz with an input-referred noise of 15 nV/$\sqrt{\text{Hz}}$ in the white noise regime. Measurements with an Am^{241} radiation source yield an equivalent input noise charge of 800 electrons at 200 ns shaping time for a 1.4 mm^2 detector with on-chip amplifier in an experimental setup with substantial external pickup.

1. Introduction

Recently there has been much interest in the integration of radiation detectors and preamplifiers on the same silicon substrate [1-6]. The ability to perform electronic signal processing on the same chip as the detector offers significant advantages in certain applications, especially in large-scale tracking detectors proposed for the Superconducting Super Collider. The two main advantages are enhanced electronic performance and simplified mechanical assembly. The former comes about because of the fact that it is possible to minimize the stray capacitance resulting from the detector-preamplifier connection when the devices are fabricated on the same substrate. Minimization of this capacitance improves both equivalent input noise charge and amplifier closed-loop frequency response. This advantage is only realized for low-capacitance detectors such as the silicon drift chamber [7] or small area pixel and strip detectors where the stray capacitance due to conventional detector-preamplifier bonding is a significant portion of the total input capacitance.

Even in applications where this is not the case, monolithic integration of detectors and readout electronics could greatly simplify the packaging considerations for complex detector systems which require many detecting elements, such as the strip-detector systems in use for particle physics applications. Monolithic integration of readout electronics with on-chip multiplexing of output signals would reduce the number of external connections by one or two orders of magnitude, thus greatly simplifying the mechanical assembly of such a system.

In this work we describe the design and experimental performance of a detector-preamplifier fabricated on a high-resistivity silicon substrate with fully-depleted p-i-n radiation detectors. Although the realization of active devices on high-resistivity silicon was demonstrated over 20 years ago [8], special care is needed in the design of both the process and the circuitry in order to develop a low-noise preamplifier with characteristics suitable for radiation detection. One key to the fabrication process is a backside gettering layer that allows the use of a conventional MOS process to realize the amplifier [5-6]. However, even though the gettering allows the use of a fairly standard technology, several key steps in the process had to be optimized in order to fabricate an amplifier with acceptable performance. This is discussed in the next section.

2. Process design considerations

The most important consideration for the monolithic integration of detectors and readout circuitry is the development of a robust process that yields both high-performance circuitry and high-quality detectors. Ideally the processing technology would be as conventional as possible in order to draw on the vast body of process development in the integrated-circuits industry, while making the fabrication amenable to high-volume manufacturing for any applications requiring large numbers of devices.

In previously published work much emphasis has been placed on the special processing techniques necessary to develop detectors with low reverse-bias leakage currents [1-4]. In particular, the minimization in the number of high-temperature thermal cycles during fabrication has been stressed. As a result the processing used for the circuitry in the previous work is somewhat restricted in comparison to modern integrated-circuit processes [1-4]. In contrast, we have developed a detector process that overcomes the high-temperature processing limitations and allows the use of standard MOS technology to realize the readout circuitry [5-6]. The ability to fabricate circuitry at relatively high temperatures is due to the presence of a backside layer of in-situ doped n^+ polysilicon which acts as a gettering layer. This layer is a sink for fast-diffusing metallic impurities, which increase the detector reverse-bias leakage current when their

concentration in the detector depletion region exceeds levels well below one part per billion. With this gettering layer in place it is possible to fabricate detectors and transistors on the same substrate with annealing temperatures in the 900C range while still maintaining low reverse-bias leakage currents in the detector [5-6]. The use of gettering also yields a very robust and reliable process.

The advantages of fabricating transistors on high-resistivity silicon were initially pointed out by Richman [8-9]. These include minimal junction capacitance to the substrate due to the large depletion regions, very small variation of the transistor threshold voltage with substrate bias (body effect), and the ability to suppress punchthrough currents with the application of a substrate bias. The latter two advantages make it possible to fabricate transistors on high-resistivity silicon that can operate satisfactorily with the relatively large substrate biases that are necessary to deplete the detector volume [3-6].

For the sake of simplicity in this first demonstration device we chose a PMOS technology on high-resistivity n-type substrates. In order to develop an amplifier with acceptable performance, it was necessary to design the transistors carefully in order to maximize key parameters within the constraints of the technology. In particular, the minimum channel length in any process is usually constrained by lithographic considerations. In the technology developed here, a conservative value of 5 μm was chosen. For a fixed channel length, the effect of the gate oxide thickness on the device performance was investigated with the goal of achieving sufficient gain in the transistors in order to allow an amplifier with only one gain stage. Single-stage amplifiers are much easier to design for unconditional stability in fed-back configurations and require minimal area for implementation, both of which are important considerations in systems with many detector elements.

Figure 1 shows the effect of gate oxide thickness on transistor output resistance at a fixed channel length of 5 μm. Transistor output resistance is plotted versus drain current for devices biased in the saturation region. Data are shown for p-channel MOSFETs fabricated on 10,000 Ω-cm silicon. As can be seen, a dramatic improvement in output resistance is observed as the oxide thickness is reduced from 37 nm to 17 nm.

Figure 2 shows a plot of the product of transistor transconductance and output resistance versus drain current for the same devices. The product $g_m r_{out}$ is the maximum voltage gain available in a common source amplifier with an ideal current-source load [10]. At an oxide thickness of 37 nm the maximum gain is approximately 20. However, at a gate oxide thickness of 17 nm the maximum gain is approximately 100, which is much more suitable for a single-stage amplifier design. Given the significant improvement in gain when thin gate oxides are used, a value of 20 nm was chosen for this process. An added benefit resulting from the use of a thin gate oxide is an increase in the transistor's radiation hardness [11]. Similar effects to those presented in Figures 1 and 2 have been

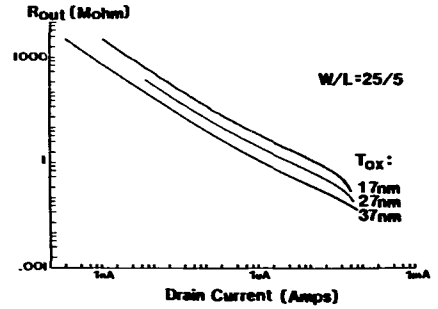

Figure 1. Measured transistor output resistance versus drain current for gate oxide thicknesses of 17, 27, and 37 nm. The devices were fabricated on 10,000 Ω-cm silicon.

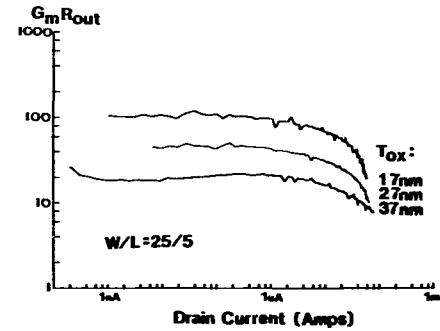

Figure 2. Measured transistor gain $g_m r_{out}$ versus drain current for gate oxide thicknesses of 17, 27, and 37 nm. The devices were fabricated on 10,000 Ω-cm silicon.

reported in the literature for MOSFETs fabricated on low-resistivity substrates [12].

Another key aspect of the technology is the choice of a load device. In this process the load consists of a depletion-mode transistor with the gate terminal connected to the source. Resistors tend to be impractical in a standard MOS process because of the relatively low sheet resistance of the conductive layers, which implies the need for large areas to realize high-value resistors. Even if an additional step is added to implement high-value resistors, the voltage drop across the resistors is usually much larger than the voltage drop across a transistor used as an active load with the equivalent resistance. An enhancement load, which requires only one type of transistor in the process, is incapable of yielding large voltage gain in a single stage because the load impedance is the inverse transconductance of the device and hence large values of resistance require large area devices. In contrast, the depletion-mode device load resistance is simply the output

resistance of the transistor provided the body effect is negligible, as is the case in this technology. Hence a large load impedance is possible in a relatively small area [10].

Given these requirements a process has been developed which includes three types of transistors, namely enhancement, depletion, and unimplanted devices [6]. Shallow implants are used for the enhancement and depletion devices in order to minimize the body effect. Thus the technology combines a thin gate oxide with a depletion load device to achieve acceptable performance with a simple single-stage amplifier. CMOS circuits are capable of much larger gain per stage but at the expense of additional processing complexity. An NMOS technology would be expected to result in improved performance because of the higher mobility of electrons when compared to holes. However, p-type silicon is not in widespread use for detectors and some additional process development is likely needed in order to develop low-leakage detectors and transistors on a p-type substrate.

Finally, in order to implement a low-noise charge-sensitive preamplifier, a high-quality capacitor must be included in the process. Capacitors are needed for the feedback element and test input. The capacitor in this process is a p^+ polysilicon – gate oxide – p^+ substrate capacitor which requires one additional mask to define the p^+ region. The p^+ region in the substrate is formed by a high-dose implant of boron.

In summary, the process developed for this work is the simplest possible which nonetheless yields acceptable performance in a single-stage amplifier. In order for this to be possible, the process does require a thin gate oxide, depletion-mode load devices, and on-chip capacitors. The next section describes the design of an amplifier on high-resistivity silicon.

3. Amplifier design

Figure 3 shows a simplified schematic of the amplifier. The amplifier consists of a cascode gain stage followed by a unity-gain level-shifting source follower. The input device is biased at a nominal current level of 20 μA and the overall nominal power dissipation is 200 μW. Figure 4 shows the actual implementation which includes a bias circuit (M7-M10) and off-chip driver (M11-16).

The small-signal gain for the cascode stage formed by transistors M1-M4 is given by

$$A_v = -g_{m1} R_{eff} \qquad (1)$$

where R_{eff} is

$$R_{eff} = r_{o3} \,||\, r_{o2}\left[1 + g_{m2} r_{o1} \,||\, r_{o4}\right] \qquad (2)$$

The g_m's are the small-signal device transconductances and the r_o's are the small-signal output resistances. Depletion-mode transistors M3 and M4 function as the current sources of the cascode stage. The current source M4 shunts current away from M2 and M3. This allows a high current through M1 to increase its transconductance g_{m1} and reduces the current through M2 and M3 to increase their output resistances r_{o2} and r_{o3} (Figure 1), with the cumulative effect of increasing the voltage gain [13]. M3 is a long-channel device (L = 25 μm) which is necessary for high output resistance.

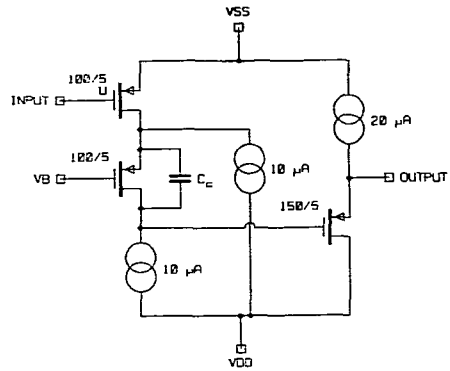

Figure 3. Simplified schematic of the amplifier considered in this work. $V_{SS} = 0V$ and $V_{DD} = -5V$.

In the charge-sensitive configuration an on-chip capacitor is fed back from the output of the source follower stage M5-M6 to the input of the amplifier. Thus the circuit must be designed to ensure that oscillation does not occur when the amplifier is used in a fed-back configuration. The 4 pF capacitor between the source and drain of M2 accomplishes the frequency compensation. The function of this capacitor is to give a transmission zero in the overall transfer function which approximately cancels the excess phase shift from the non-dominant pole of the circuit [14]. This is preferable to simply adding capacitance at the high-impedance node of the cascode which causes an unacceptable reduction in the amplifier bandwidth. Since the capacitors used in this process have a thin dielectric layer (the gate oxide) it is possible to integrate the 4 pF compensation capacitor on chip in a modest area (≈45 by 50 μm^2). The transmission zero frequency is simply g_{m2} / C_c where C_c is the value of the compensation capacitor.

The output stage is a broadband unity-gain stage which consists of a transconductance amplifier (M11-13) of gain g_{m11} followed by a transresistance stage (M14-16) of gain g_{m14}^{-1} [13]. Transistors M11 and M14 are sized to be identical and hence a voltage gain of unity is achieved. This circuit also offers lower output impedance than a single source follower [13]. Actual measured performance of the amplifier is presented in the next section.

4. Experimental results

An experimental detector integrated circuit was designed and fabricated. The starting material was 10,000 Ω-cm n-type, and the crystalline orientation was <100>. The chip contains arrays of MOS transistors and capacitors, amplifiers with varying design rules, radiation detectors, and two structures which consist of radiation detec-

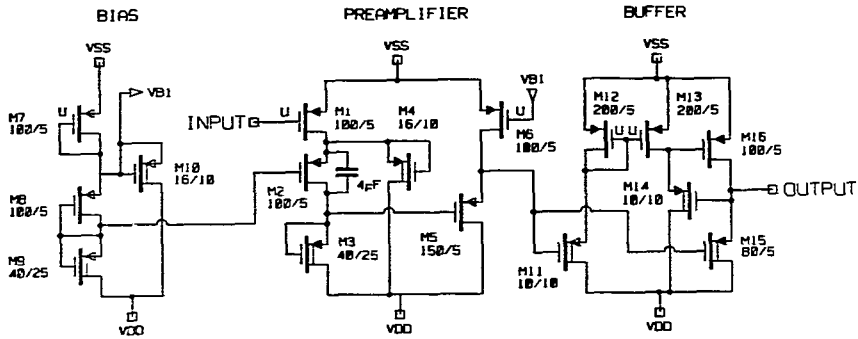

Figure 4. Implementation of the amplifier including bias circuitry and an off-chip driver. U denotes an unimplanted transistor. $V_{SS} = 0V$ and $V_{DD} = -5V$.

tors dc-coupled to on-chip amplifiers. The latter are a 1.4 mm^2 rectangular detector with on-chip amplifier, and a strip detector on a 60 μm pitch layout with amplifiers connected to four adjacent strips. In the portion of the chip containing only amplifiers, various configurations were included to facilitate testing, i.e. combinations of amplifiers with and without biasing circuitry, feedback capacitors, and output buffers.

Figure 5 shows the measured open-loop frequency response of an amplifier including on-chip biasing circuitry (M1-M10 of Figure 4). An active probe was used at the output in order to minimize the capacitive loading and the measurements were performed using a Hewlett-Packard 4195A Network/Spectrum analyzer. The low-frequency voltage gain is ≈250 and the -3dB bandwidth is ≈115 kHz yielding a gain-bandwidth product of nearly 30 MHz. The measured phase margin is 45 degrees and hence the amplifier is stable in a unity-gain feedback configuration. The roll-off is slightly greater than 20 dB/decade and therefore the unity-gain frequency is somewhat less than the gain-bandwidth product of the amplifier. These measurements were performed at a substrate bias of 20V which fully depletes the ≈250 μm thick substrates used in this work.

Figure 6 shows the input-referred noise voltage for the full (open loop) circuit shown in Figure 4. The measurement bandwidth was 3 Hz and the measurements were also performed with the Hewlett-Packard 4195A. The input-referred noise in the white-noise regime is ≈ 15 nV/√Hz which is in rough agreement with what is expected given the transconductance of the input device M1. Hence the open-loop measurements yield a gain-bandwidth product and input-referred noise acceptable for applications using low-capacitance detectors.

Figures 7 and 8 show the results of measurements of the amplifier in a charge-sensitive configuration using the device consisting of the 1.4 mm^2 detector directly connected to the amplifier of Figure 4. The amplifier feedback capacitor is 100 fF and a 100 fF capacitor is connected to the amplifier input in order to allow for charge injection into the amplifier from an external voltage pulser. Both capacitors are included on chip. A small geometry MOSFET is used to provide resistive discharge of the feedback capacitor. The output of the amplifier drives an external buffer amplifier to minimize loading on the on-chip amplifier, and is then fed into the input of a single CR-RC shaper/filter. Figure 7 shows the output of the

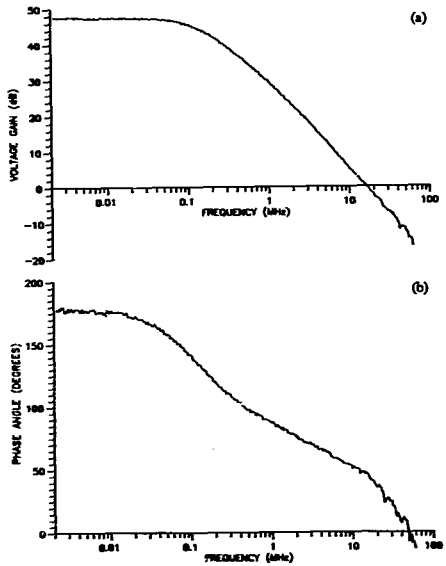

Figure 5. Measured open-loop frequency response of an amplifier fabricated on 10,000 Ω-cm silicon. The substrate bias was 20V.

(a) Voltage gain versus frequency.

(b) Phase versus frequency.

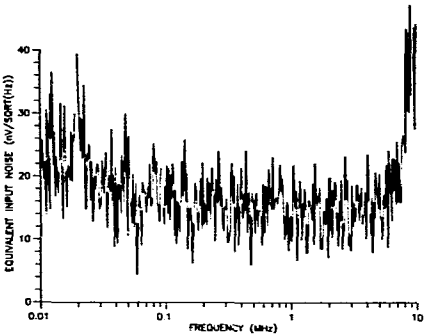

Figure 6. Measured input-referred noise of an amplifier fabricated on 10,000 Ω-cm silicon. The measurement bandwidth was 3 Hz.

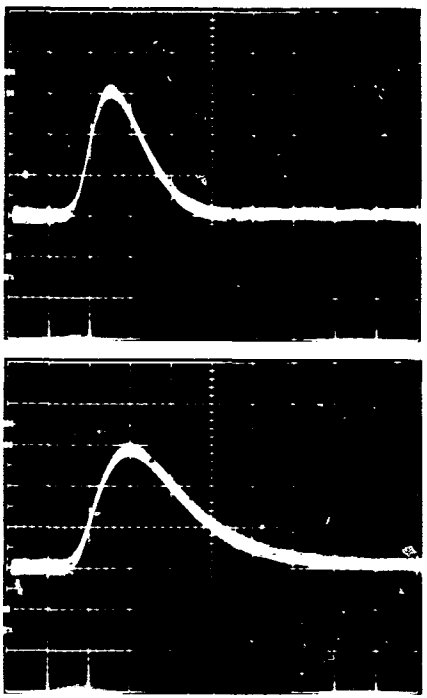

Figure 7. Oscilloscope trace of the output of a single CR-RC shaper driven by an amplifier on high-resistivity silicon. The amplifier input is a voltage pulse applied across a 100 fF injection capacitor yielding an input charge of = 4 fC. 1 V/div : 200 ns/div.

Upper photograph: Shaper time constant of 100 ns.

Lower photograph: Shaper time constant of 200 ns.

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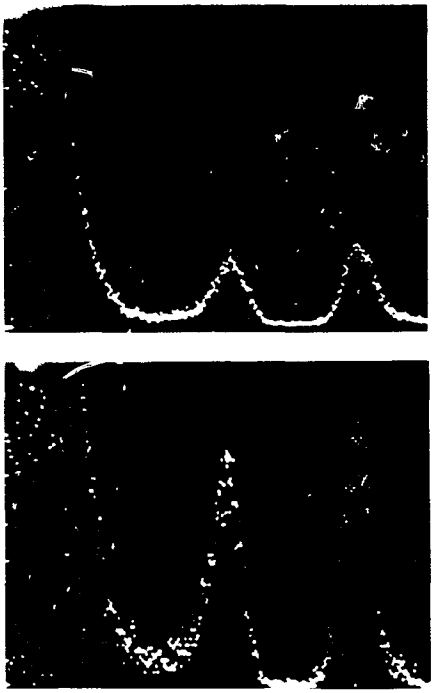

Figure 8. Measured radiation spectrum for a 1.4 mm^2 detector with on-chip amplifier. The shaper time constant was 200 ns. The lower peak is the 60 keV gamma ray from an Am^{241} radiation source, and the upper peak is a voltage pulser set to inject 4 fC. The FWHM is = 6.8 keV, equivalent to an input noise charge of 800 electrons r.m.s. The lower photograph shows an expanded view.

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CR-RC shaper when the shaper time constant is set to 100 ns and 200 ns. The voltage pulser was adjusted to inject the charge equivalent to minimum ionizing particles traversing = 300 μm of silicon (= 4 fC). The total capacitance at the amplifier input due to the detector, input transistor and injection capacitor is estimated to be = 1.4 pF. The measured amplifier risetime in this configuration is about 100 ns.

Figure 8 shows the response of the 1.4 mm^2 detector with on-chip amplifier to an Am^{241} radiation source. The capacitance of this detector is approximately equal to that of one strip in the strip detector. The radiation spectrum shows the Am^{241} 60 keV gamma peak in addition to a voltage pulser set to inject an amount of charge equivalent to a minimum ionizing particle. The measured resolution is 6.8 keV FWHM corresponding to an input noise charge of 800 electrons r.m.s.

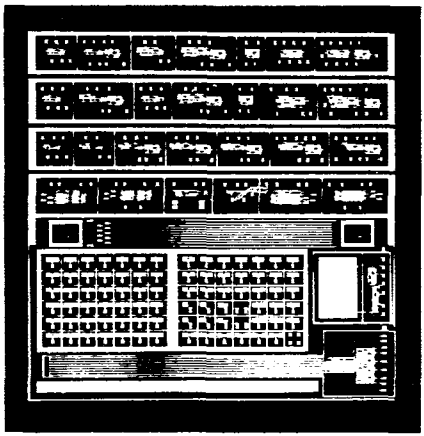

Figure 9. Die photograph of the experimental detector integrated circuit.

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with a shaper time constant of 200 ns. It should be noted that all the measurements reported here were performed on a probe station at the wafer level where the noise is significantly affected by external electronic pickup. The measurement of equivalent input noise voltage was less sensitive to pick-up and indicates significant improvements in the noise figures with better electronic shielding. Even so, the signal to noise ratio for minimum ionizing particles is greater than 30 for the measurement setup used here.

Figure 9 shows a die photograph of the fabricated device. The 1.4 mm^2 detector with on-chip amplifier is located in the lower right portion of the photograph. The detector is the large rectangular structure. The die size is 9 mm by 9 mm.

5. Summary

A process capable of integrating silicon p-i-n radiation detectors and low-noise readout electronics on the same monolithic substrate has been demonstrated. Preamplifiers have been designed and realized on high-resistivity silicon. The amplifiers have acceptable performance for many radiation-detection applications, especially in high-energy physics, and the viability of monolithic integration of detectors and readout electronics has been demonstrated by the detection of 60 keV gamma rays with on-chip amplification. The technology chosen for this work is a very simple one but nonetheless has yielded a usable proof-of-principle device. By including effective gettering in the process standard fabrication techniques can be used to integrate detectors and readout electronics with more sophisticated technologies, e.g. CMOS. This opens the path toward highly-integrated detector systems with high-performance circuitry in the foreseeable future.

6. Acknowledgements

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7. References

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