Optical Timing Receiver for the NASA Spaceborne Ranging System
Part I: Dual Peak-Sensing Timing Discriminator

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Abstract

Position-resolution capabilities of the NASA Spaceborne Laser Ranging System are essentially determined by the time-resolution capabilities of its optical timing receiver. The optical timing receiver consists of a fast photoelectric device;(e.g., photomultiplier or an avalanche photodiode detector), a timing discriminator, a high-precision event-timing digitizer, and a signal-processing system. The time-resolution capabilities of the receiver are determined by the photoelectron time spread of the photoelectric device, the time walk and resolution characteristics of the timing discriminator, and the resolution of the event-timing digitizer. It is thus necessary to evaluate available fast photoelectronic devices with respect to their time-resolution capabilities, to design a very low time walk timing discriminator and to develop a high-resolution event-timing digitizer which will be used in the high-resolution spaceborne laser ranging system receiver.

This report describes the development of a new dual-peak sensing timing discriminator. The amplitude dependent time walk is less than $\pm$ 150 psec for a 100:1 dynamic range of Gaussian-shaped input signals having pulse widths between 11 and 17 nsec. The unit produces 800 mV negative output pulses, each 10 nsec wide, and 3V positive pulses with widths of 15 nsec. The time delay through the discriminator is approximately 37 nsec. In

this discriminator the input signal is processed by a peak-crossing circuit which produces a bipolar pulse having its zero-crossing point at the peak of the input signal. All essential functions in the discriminator are performed by means of tunnel diodes with backward diodes as nonlinear loads. The discriminator is designed to be CAMAC compatible to a conventional time-interval unit or a high-precision event timing digitizer. The adjustment procedure for obtaining minimum time walk is also given.

1. Introduction

Satellite laser ranging methods have been used successfully for precise satellite orbit determination, polar motion determination, the measurement of earth tidal parameters, high precision distance measurements between laser sites, and for the calibration of spaceborne radar altimeters (1). More recently, it has been proposed that a high precision laser ranging system be applied to geophysical studies, particularly those concerned with solid earth dynamics measurements and earthquake prediction, using a Laser Geodetic Satellite (LAGEOS) (2), and the Space Shuttle (3). Since the pulsed laser ranging system determines the distance to a target by measuring the time of flight of a short light pulse to a target and back, its position-resolution capabilities are essentially determined by the time-resolution capabilities of its optical timing receiver. The optical timing receiver consists of a fast photoelectric device, primarily a standard or crossed-field photomultiplier or an avalanche photodiode detector, a timing discriminator, a high-precision event-timing digitizer, and a signal processing system. The time resolution capabilities of the receiver are determined by the time spread of the photoelectric device, the time walk and resolution characteristics of the timing discriminator, and the time resolution of the event timing digitizer. Consequently, to achieve optimum results, it was necessary to evaluate fast photoelectric devices with respect to their time resolution capabilities in order to select the best available, to design a very low time walk high resolution timing discriminator and to develop a high-precision event timing digitizer to be used in this High Resolution Spaceborne Laser Ranging System Receiver. An evaluation of timing characteristics of the very fast classically designed and static crossed-field photomultipliers was carried out and was reported in Ref. (7)-(10). A high-precision event-timing digitizer with an incremental resolution of 20 psec will be developed in the Electronics Research and Development Group of the Lawrence Berkeley Laboratory as the next step in this project. As a further step in the development of the spaceborne optical timing receiver it was necessary to design a high resolution dual peak-sensing timing discriminator with a time walk of $\pm$ 150 psec or less capable of processing signals from the tapped delay line correlator of the receiver. The design is based on experience acquired by the Electronics Research and Development Group developing high precision timing discriminators and time interval digitizers for atomic and molecular subnanosecond fluorescence decay time measurements over a period of many years, (5), (11), (12).

One of the problems of high resolution time of-flight measuring instruments is that of matching discriminators to the photon detectors used for generating the start and stop signals. State-of-the-art discriminator designs permit timing resolution in the 25-100 psec range when dealing with detector signals having 1-2 nsec risetimes and amplitude ranges of 0.1-2V, (4)-(6). Here the ambient temperature is assumed not to vary more than a few degrees Celsius. However, there is need for a very low time walk discriminator which will accept and process input pulses with greater dynamic ranges and much longer risetimes. Also, such a discriminator must not exceed certain limits of electrical power requirements.

The discriminator herein described accepts detector pulses with risetimes in the 8-13 nsec range which is a very slow rate of rise for signal pulses. It also has a timing resolution within a fraction of a nanosecond over an amplitude range of 50mV-5V. To achieve this resolution, the signal rise rate must be increased before the output timing pulse is generated. For this it has been found that a linear amplification of at least 30 dB is required. Signal level of the peaks must be clipped to prevent excessive overloading of the amplifiers. However, even with maximum practical clipping certain overloading occurs with input signals above 2V, and this in turn limits the maximum acceptable operating pulse rate to below 100 kHz due to the time required for the amplifiers to recover.

The input amplifiers increase the rise rate (typically from 1.5mV/nsec to 100mV/nsec in the most severe case) before a tunnel diode triggers at the zero-crossing point. A tunnel diode, in this mode of operation will behave like a leading edge discriminator which is undesirable for producing amplitude-independent timing signals. To overcome this the zero-crossing point is made to occur at the peak of the signal by means of a processing circuit at the input. A pedestal is generated and applied to the diode before the zero-crossing point is reached which increases the diode bias right up to its threshold point. As soon as the signal crosses over the base line, the diode triggers producing the detector timing pulse.

Since the timing error occurring in the tunnel diode circuit as a result of a threshold change with temperature is unacceptable, the tunnel diode is placed in a temperature controlled environment. Ideally, the whole discriminator should be temperature controlled; however, the heater power required would be unacceptably high. Driver and buffer stages are used to bring the output signals up to the required levels. Adjustable threshold and gating circuits are built into the discriminators.

2. Description of the Dual-Peak Sensing Timing Discriminator Circuit

A schematic diagram of the dual-peak sensing timing discriminator is shown in Fig. 1. Pertinent waveforms at the specified points in the circuit and the sequence of operation of the discriminator are given in Fig. 2. Referring to these figures simultaneously, the negative unipolar input signal, having an amplitude anywhere from 50mV to 5V enters the discriminator at Point A. The signal is immediately attenuated, by a factor of 2, by means of an attenuator consisting of resistors R1 and R2, Point C. The input signal is also inverted and delayed for a time T1 by means of a wideband transformer T1 and delay line DL1, respectively, (Point B). The attenuated signal and the inverted-delayed signal are added together, creating the bipolar wave shape at Point C. The zero-crossing point of the bipolar pulse occurs within the 95% of the input pulse amplitude over a pulse width of 11-17 nsec. An amplitude-limiting network, consisting of the hot carrier diodes CR1 and CR2, limits the amplitudes of the bipolar signal to a maximum of 350mV. After being limited, the clipped bipolar signal is amplified by amplifier M5. With an input signal amplitude of 50mV, the rise rate of the zero-crossing point of the clipped bipolar pulse is increased from 1.5mV/nsec to 7.5mV/nsec. The bipolar output signal from the first amplification stage is again amplitude-limited by means of diodes CR3 and CR4, (this is seen in the wave shape at Point E). The amplitude-limiting network limits the bipolar signal amplitudes to within a maximum of 350mV before they are amplified by the second amplifier M6. After the second amplification the rise rate of the crossing of the bipolar signal becomes 100mV/nsec. The bipolar output signal from the second amplification stage is again amplitude-limited by means of diodes CR5 and CR6. The resultant clipped bipolar signals are delayed, Point F, and applied to the threshold tunnel-diode zero-crossing discriminator.

The positive portion of the bipolar signal serves as a trigger pulse for the tunnel diode CR7 threshold detector. The peak current of this diode is 10mA. The variable resistor R26 provides a threshold adjustment for diode CR7. The inductor L7 and the backward diode CR8 serves as the nonlinear load for tunnel diode CR7. Detector timing signal is shown at Point H. Operating a tunnel diode in this mode improves the sensitivity of the circuit and reduces its standby power dissipation. As the input signal is being processed, a pedestal is generated as explained below and is used to shift the bias of the zero-crossing detector to compensate for the time walk resulting from differences in amplitude of the input signals. In order to avoid the degradation of the time-walk characteristics of the discriminator as a whole, one of the comparator in M4 is used as a lower-level discriminator which inhibits output pulses when the input signal is below a certain level. In this way the threshold level of the tunnel diode CR7 can be adjusted to obtain the best possible time walk characteristic throughout the entire input pulse amplitude dynamic range, and it stays fixed at that level.

The variable resistor R64 is used to set the threshold level of the first element of the dual comparator, M4, through a voltage range from 50mV to 5V. The output of the comparator is differentiated by the capacitor C46 and the resistor R66. The pedestal mentioned above is generated when the first element in comparator M4 recognizes an input pulse and generate a trigger pulse for tunnel diode CR9. This diode generates a pulse with a width of approximately 50 nsec which is further shaped by the second element of M4 before it is used as the bias pedestal, Point G. Variable resistor R70 provides the bias adjustment for diode CR9. Inductor L6 and the backward diode CR10 serve as the nonlinear load for tunnel diode CR9. The other output of the comparator M4, at the Point I, provides the enable pulse for the output driver M7. The bias provided by the voltage divider formed by R76 and R77 prohibits comparator M7 from operating except when it receives a recognized signal. The recognized signal causes the comparator M7 to yield an output pulse at the MECL logic levels, "0" being -1.9V, "1" being -0.8V. Transistors Q4, Q5 and Q6 are used to convert the signal from the MECL logic levels to the Nuclear Instrument Module (NIM) Standard levels (i.e., -0.8V across 50Ω). Transistors Q10, Q11 and Q12 are used to provide an alternative positive output pulse. Transistors Q7-Q9 and Q13-Q15 are used to provide one more NIM and positive output pulse, respectively.

The system described will generate an output pulse as long as the input signal amplitude exceeds the preset threshold level of the threshold detector. This means a spurious pulse with a high enough amplitude from the high gain photon detector of the optical timing receiver can yield a spurious output timing pulse. Therefore, an external gating function is incorporated to ensure that an input signal will be processed only when an external gating pulse is present. The external gating of the discriminator is achieved through the circuit comprised of transistors Q1-Q3. The "Gate In" and "Gate Out" function is selected by a toggle switch on the discriminator front panel. In the "Gate In" position a positive gating pulse with a minimum width of 50 nsec starting from the expected arrival time of the input signal must be present at the gate input to enable the discriminator to operate in its normal mode. At the "Gate Out" position the discriminator will produce an output pulse whenever the input signal amplitude exceeds the threshold level.

Because the threshold level of the zero-crossing tunnel diode detector is temperature sensitive and this affects the time walk of the discriminator, it is necessary to keep its temperature constant. This is achieved by putting the tunnel diode in a temperature controlled oven. Since the area of the discriminator printed circuit board is limited, the temperature control device will be of reasonable size and its power consumption will be low. The small size oven is made from a 10Ω, 8 watt wire wound resistor (R106). The resistor itself is used as the heating element while the hallow center of the ceramic form serves as the oven cavity for the tunnel diode and the thermistor, RT. The thermistor is used as the temperature sensor which provides feedback thru the operational amplifier M8, which controls the power applied to the heating element. This control system operates in a proportional mode. Variable resistor R99 adjusts the oven temperature. A section of fiber-glass tubing contains the oven and the inside of the resistor where the tunnel diode and thermistor are located is filled with a heat sink compound. A high temperature silicon rubber is used to seal off both ends.

When the power is turned on, the full voltage is applied across the heating element. As the temperature approaches 75°C and the voltage decreases gradually until just enough power is provided to maintain the 75°C level inside the oven. The steady-state power consumption is less than 1 watt while the startup power required is close to 2.5 watts.

3. Measurement of the Time Walk and Resolution Characteristics of the Discriminator

The time walk of the dual peak-sensing timing discriminator, as a function of the input pulse amplitude and ambient temperature were measured with the input pulse rise time and width as parameters. Measurements were made using the system illustrated in Fig. 3. The source of the discriminator input pulses with Gaussian waveshapes was a Hewlett-Packard pulse generator 8007B with adjustable risetimes and falltimes. A fast reference pulse, displayed on the oscilloscope, was generated by means of a discriminator. The main signal went through a wideband attenuator HP8496B, which could be adjusted over a range of 110 dB, before entering the discriminator under test. The output of the discriminator was displayed on the oscilloscope together with the leading edge of the reference pulse, and the two pulses were adjusted to be 1-2 nsec apart so that the amount of walk could be easily observed. This eliminates the drift of the pulse generator as well as that of the oscilloscope from interfering with the measurement.

The measured time-walk characteristics are shown in Figs. 4 and 5 for a top and bottom discriminator, respectively. It should be pointed out that in these two sets of characteristics the discriminator operating conditions were optimally adjusted to yield the smallest time walk for each curve for the particular input signal waveshape. The characteristics shown in the figures indicate that, at a repetition frequency of 10kHz the time walk at any given pulse width is approximately equal $\pm$ 100 psec for an input pulse amplitude variation from 50mV to 5V. Fig. 6 and 7 show another two sets of time-walk characteristics where the discriminator operating conditions were optimized for input pulse width of 14 nsec only. It should be pointed out that in these two figures, each characteristic was individually taken and had no time relationship to other characteristic in the same plot. From Figs. 6 and 7 it can be seen that a time walk of $\pm$ 150 psec can be obtained for input pulses having width from 11 to 17 nsec, FWHM, for input signal amplitudes below 1.2V.

An increase of the input pulse amplitude from 5V to 10V adds approximately 200 psec to the measured walk values given above. The discriminator time resolution was also measured as a function of the input pulse amplitude. The time resolution was better than 100 psec, FWHM, in the worst case.

If the detector signal is a sequence of Gaussian shape pulses with different widths, the peaks of these pulses will occur at different times (the peaks of pulses with a larger width will occur later). Since the timing pulse occurs at the pulse peaks, the time walk will be very well in the nanosecond region as the peak of a 11 nsec pulse would occur 5 nsec before that of a 17 nsec pulse assuming the starting point of both pulses are the same. Under such conditions the zero-crossing point should be extracted at a low fractional point rather than at the peak to minimize the time walk.

Despite the temperature controlled zero-crossing detector, the ambient temperature affects the time walk of the discriminator. The propagation delay of the discriminator was measured as a function of ambient temperature. In this measurement, the whole discriminator was placed in an oven whose temperature could be controlled. The propagation delay of 50mV, 500mV and 5V input pulses were measured as a function of temperature. The results are shown in Figs. 8 and 9. The top and bottom discriminators show similar change pattern. The temperature related change is mainly due to propagation delay changes of the amplifiers especially at large input pulse amplitudes. In this case the amplifiers operate close to saturation level. The threshold level changes because ambient temperature sensitivity of the comparators used as output buffer-drivers contributes to the time walk.

The changes in propagation delay at various input signal amplitude through a temperature range of 20°C-50°C were measured to be from 200 psec to 400 psec for 50mV to 500mV pulses for the top discriminator. For input signal amplitudes of 5V the propagation delay change was 800 psec. The changes in propagation delay is obviously due to components other than the zero-crossing detector tunnel diode which was maintained at 75°C through the 20°C-50°C ambient temperature range. The time walk through this temperature range is close to 800 psec in the worst case, but if two similar channels are used side by side, the differential time walk would become acceptable.

The differential progagation delay of the two discriminators was also measured as a function of temperature. Fig. 10 shows that the delay differential is within 120 psec over the temperature range 5°C-55°C. The signal propagation time of the discriminator is 37 nsec.

4. Operation Instructions

The discriminator should be turned on for approximately an hour before being tested, adjusted or used for any measurement. This time is required to stabilize the temperature of critical components. If possible, the discriminator should be left on at all times. The voltage of +6V (1A when switched on and decreasing shortly to 0.6A-0.8A depending on ambient temperature). The voltages -6V(0.6A), +24V(0.2A) and -24V(0.06A) required by the discriminator should be within 5% or better.

5. Discriminator Adjustments

Operating conditions of the discriminators have been optimized for a 14 nsec FWHM input pulse width. As Fig. 6 and 7 suggested, this adjustment allows 13-15 nsec FWHM pulses to operate within specifications. For pulses with width beyond this range, some adjustment of the discriminators' operating conditions must be made to bring the time walk back within the specified range.

With reference to the measuring system block diagram, the attenuator following the pulse generator is set for input pulse amplitudes of 50mV, 158mV, 500mV, 1.58V or 5V with the settings of 40 dB, 30 dB, 20 dB, 10 dB and 0 dB, respectively. The three adjustments at the rear panel of the discriminator, i.e., zero-crossing, Bias 1 and Bias 2 are used to minimize the time walk. The zero-crossing adjustment is mainly used to bring the 50mV pulse within the ± 150 psec range. Bias 1 and Bias 2 are mainly for adjsted 1.58V and 5V pulses, respectively. However, Bias 1 and Bias 2 adjustments do affect the walk of both pulses and hence must be optimized by going back and forth, if necessary, to obtain the best possible walk for pulses having amplitudes above 1.5V. The normal sequence is to use the 500mV pulse as the reference point and adjust the three controls to achieve time walk within ± 150 psec range centering around the 500mV point.

The input signal pulse shapes used for these measurements, having a width of 11, 14 and 17 nsec, are shown in Figs. 11, 13 and 15, respectively. Zero-crossing signals of the test pulse are shown in Figs. 12, 14 and 16 (Point C in the circuit diagram). The zero-crossing point does not change with amplitude, but it does shift with the shifting of the pulse peaks.

6. Conclusions

A dual discriminator detecting the peaks of signal pulses has been designed and constructed for precision timing measurements. The pulses should be Gaussian in shape with widths in the 11-17 nsec FWHM range. The discriminator has small time walk and time resolution in the range of 100-200 psec.

Diode clippers are used to limit the peak amplitude to avoid excessively overloading the amplifiers which follow the tunnel diode detector. The most critical detector timing element, tunnel diode CR7, was found to require temperature controlling to avoid excessive walk due to temperature change. While this helped to eliminate the time error due to this stage, other components in the circuit contribute certain amount of error over a temperature range of 23-50 degree Celsius. An obvious solution is to temperature control all critical points in the circuit although power consumption would be higher than permitted by the application for which the circuit was designed.

The discriminator circuit can also be used to process signals with zero-crossing point at fractional points other than the peak. For this only the front end signal processing circuit needs to be slightly modifield.

7. Acknowledgments

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8. References

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9. Figure Captions

Fig. 1 Schematic Diagram of the dual peak sensing discriminator.

Fig. 2 Waveforms at the particular points in the schematic of the discriminator.

Fig. 3 Block diagram of the measuring system.

Fig. 4 Time-walk characteristics of the top peak-sensing discriminator as a function of input pulse amplitude with pulse width as parameter.

Fig. 5 Time-walk characteristics of the bottom discriminator as a function of input pulse width as parameter.

Fig. 6 Time-walk characteristics of the top discriminator as a function of input pulse amplitude with adjustment optimized for input pulse width of 14 nsec, FWHM.

Fig. 7 Time-walk characteristics of the bottom discriminator as a function of input pulse amplitude with adjustment optimized for input pulse width of 14 nsec, FWHM.

Fig. 8 Time-walk characteristics of the top discriminator as a function of ambient temperature.

Fig. 9 Time-walk characteristics of the bottom discriminator as a function of ambient temperature.

Fig. 10 Propagation time differential of top and bottom discriminators as a function of ambient temperature.

Fig. 11 Input test pulse having a width of 11 nsec, FWHM.

Fig. 12 Zero-crossing signal of the test pulse given in Fig.11.

Fig. 13 Input test pulse having a width of 14 nsec, FWHM.

Fig. 14 Zero-crossing signal of the test pulse given in Fig. 13.

Fig. 15 Input test pulse having a width of 17 nsec, FWHM.

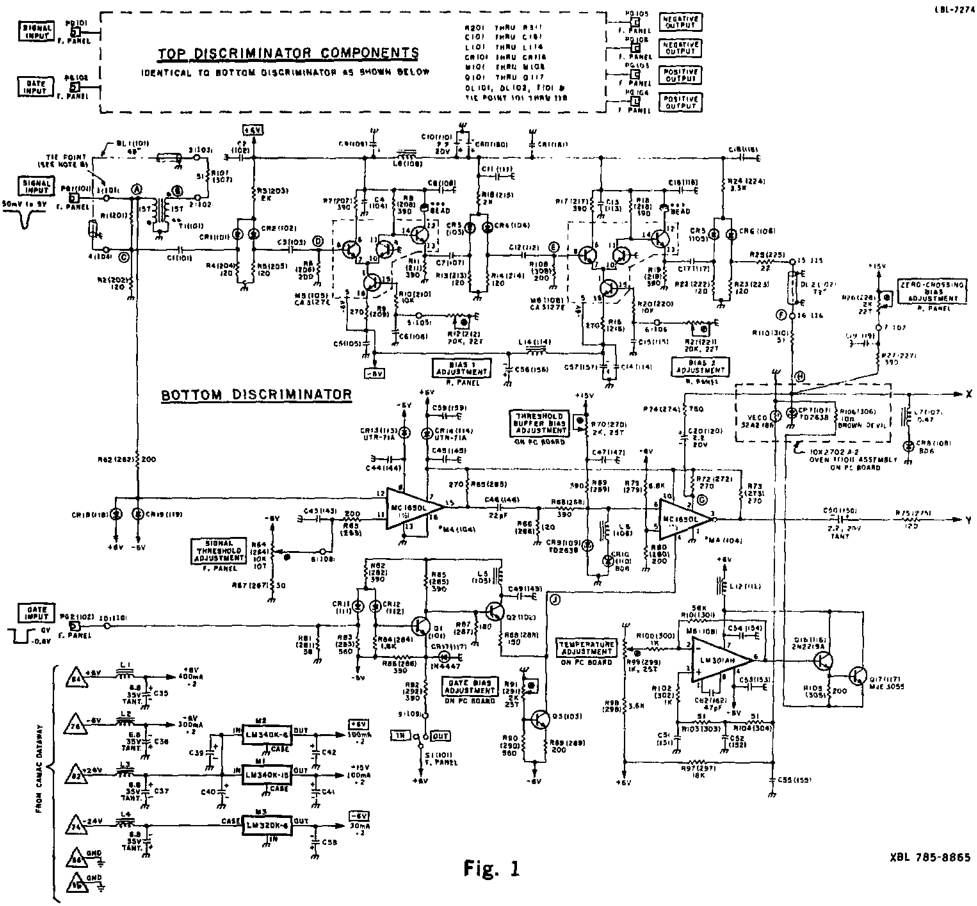
Fig. 16 Zero-crossing signal of the test pulse given in Fig. 15.

Fig. 17 Front panel of the dual peak-sensing discriminator.

Fig. 18 Rear panel of the discriminator.

Fig. 19 Left side view of the discriminator.

Fig. 20 Right side view of the discriminator.


LBL-7274
TOP DISCRIMINATOR COMPONENTS
IDENTICAL TO BOTTOM DISCRIMINATOR AS SHOWN BELOW
SIGNAL INPUT
GATE INPUT
NEGATIVE OUTPUT
NEGATIVE OUTPUT
POSITIVE OUTPUT
POSITIVE OUTPUT
BOTTOM DISCRIMINATOR
BIAS 1 ADJUSTMENT
BIAS 2 ADJUSTMENT
ZERO-CROSSING BIAS ADJUSTMENT
THRESHOLD BUFFER BIAS ADJUSTMENT
SIGNAL THRESHOLD ADJUSTMENT
GATE BIAS ADJUSTMENT
TEMPERATURE ADJUSTMENT
FROM CAMAC DATAWAY
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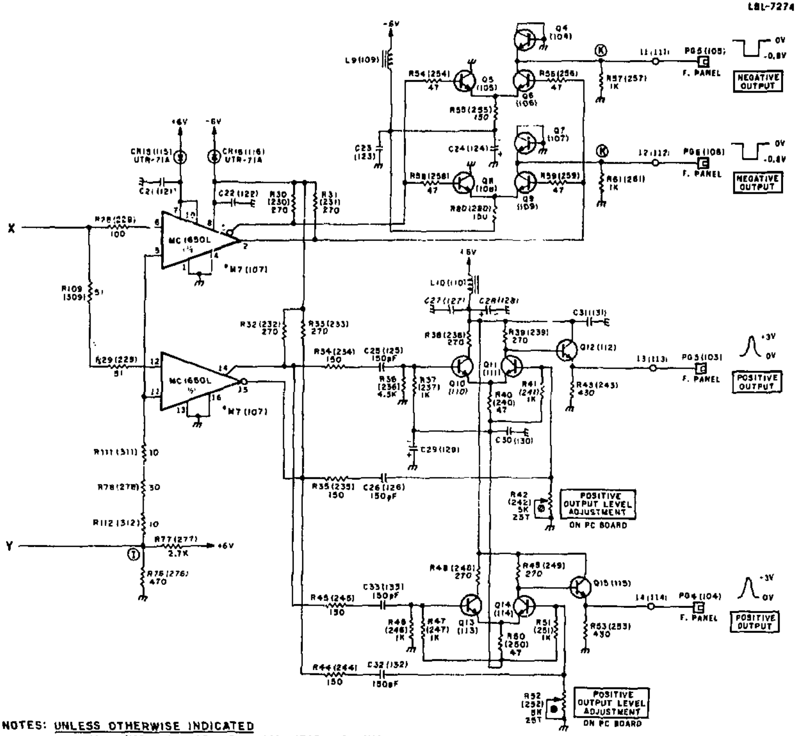
LM340K-15
LM320K-6
MC1650L
LM301AH
XBL 785-8865

Fig. 1



NOTES: UNLESS OTHERWISE INDICATED

1. CAPACITANCE IN MICROFARADS & CAPACITORS CERAMIC.
   a. —||+ ARE 10μF 20V TANTALUM.
   b. —||— ARE 0.1μF 100V CERAMIC CK05BX103M.
2. CONNECTORS OSM 211.
3. DIODES HPA 5082-2303.
4. INDUCTANCE IN MICROHENRIES & CHOKES 2.2μH 1100mA.
5. RESISTANCE IN OHMS & RESISTORS 1/4W 5% CARBON COMPOSITION.
6. TRANSISTORS 2N2857.
7. COMPONENTS WITH TWO DESIGNATED NUMBERS ARE IDENTICAL FOR TOP & BOTTOM DISCRIMINATOR ON PC BOARD 7U2802.
8. NUMBER OUTSIDE O—— ARE TIE POINTS ON PC BOARD 7U2802.
*9. HEAT SINKS WAKEFIELD TYPE 650-B EXPOXY BONDED ON TOP OF M4(104) & M7(107).
**10. TI TOROIDAL CORE INDIANA GENERAL CF121 TYPE Q-2.
***11. FERRITE BEADS FERROXCUBE NO. 56-590-65.
12. △— CAMAC FINGERS ON PC BOARD 7U2802.

XBL 785-8865A

Fig. 1

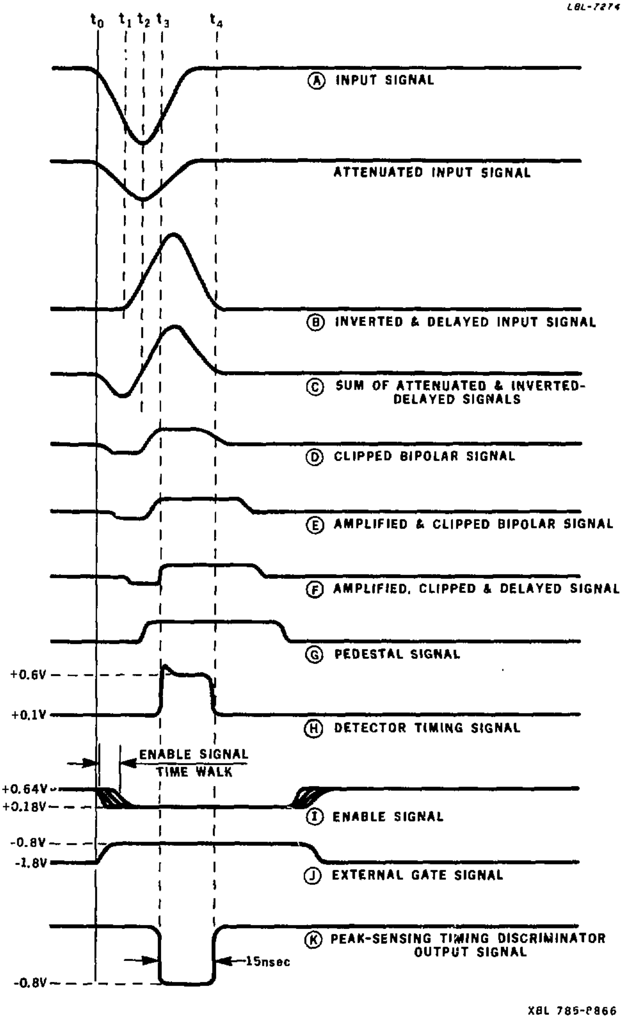

LBL-7274
t_0 t_1 t_2 t_3 t_4
(A) INPUT SIGNAL
ATTENUATED INPUT SIGNAL
(B) INVERTED & DELAYED INPUT SIGNAL
(C) SUM OF ATTENUATED & INVERTED-DELAYED SIGNALS
(D) CLIPPED BIPOLAR SIGNAL
(E) AMPLIFIED & CLIPPED BIPOLAR SIGNAL
(F) AMPLIFIED, CLIPPED & DELAYED SIGNAL
(G) PEDESTAL SIGNAL
+0.6V
+0.1V
(H) DETECTOR TIMING SIGNAL
ENABLE SIGNAL TIME WALK
+0.64V
+0.18V
(I) ENABLE SIGNAL
-0.8V
-1.8V
(J) EXTERNAL GATE SIGNAL
(K) PEAK-SENSING TIMING DISCRIMINATOR OUTPUT SIGNAL
15nsec
-0.8V
XBL 785-8866

Fig. 2

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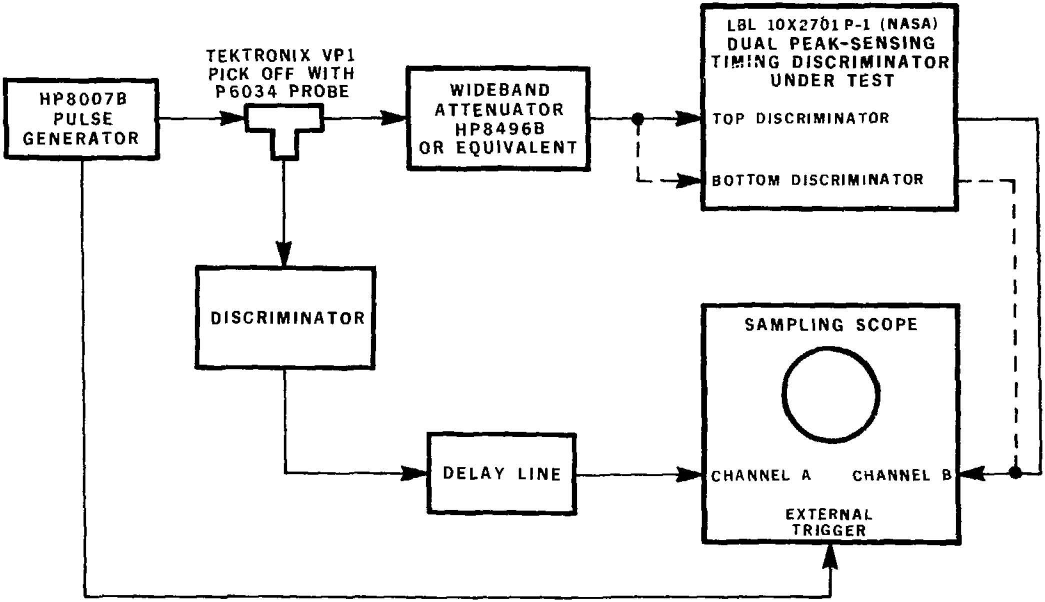

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Fig. 3

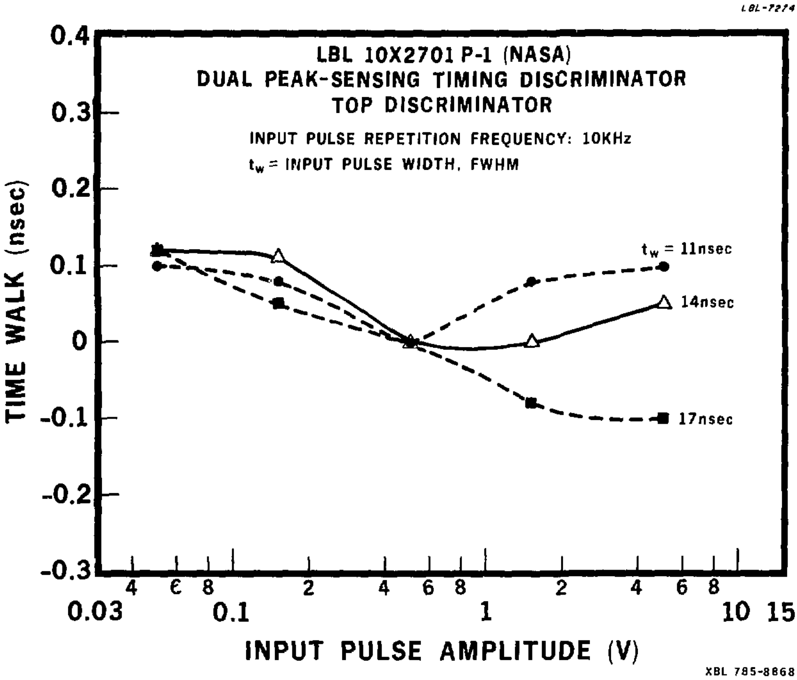
LBL-7274
LBL 10X2701 P-1 (NASA)
DUAL PEAK-SENSING TIMING DISCRIMINATOR
TOP DISCRIMINATOR
INPUT PULSE REPETITION FREQUENCY: 10KHz
t_w = INPUT PULSE WIDTH, FWHM
t_w = 11nsec
14nsec
17nsec
TIME WALK (nsec)
0.4
0.3
0.2
0.1
0
-0.1
-0.2
-0.3
4
6
8
2
4
6
8
2
4
6
8
0.03
0.1
1
10
15
INPUT PULSE AMPLITUDE (V)
XBL 785-8868

Fig. 4

LBL-7274

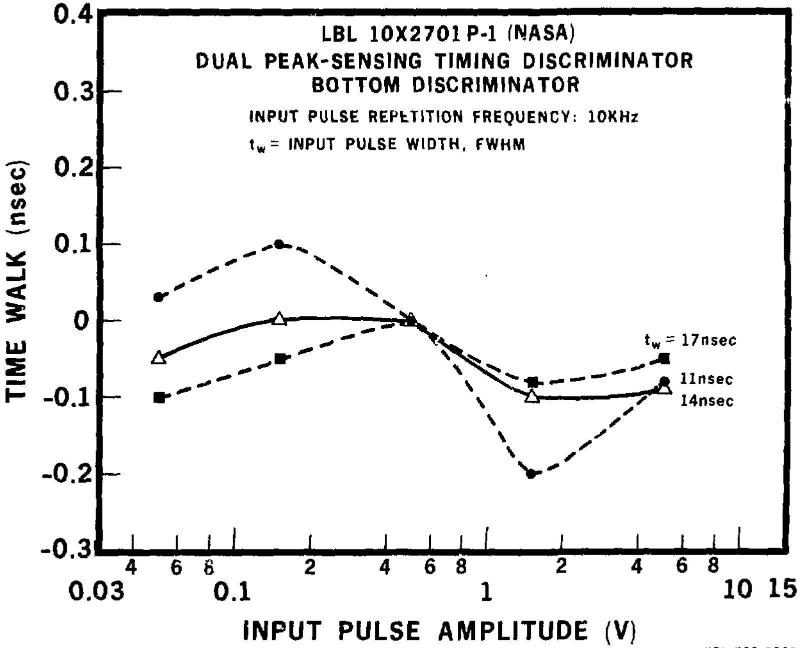

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Fig. 5

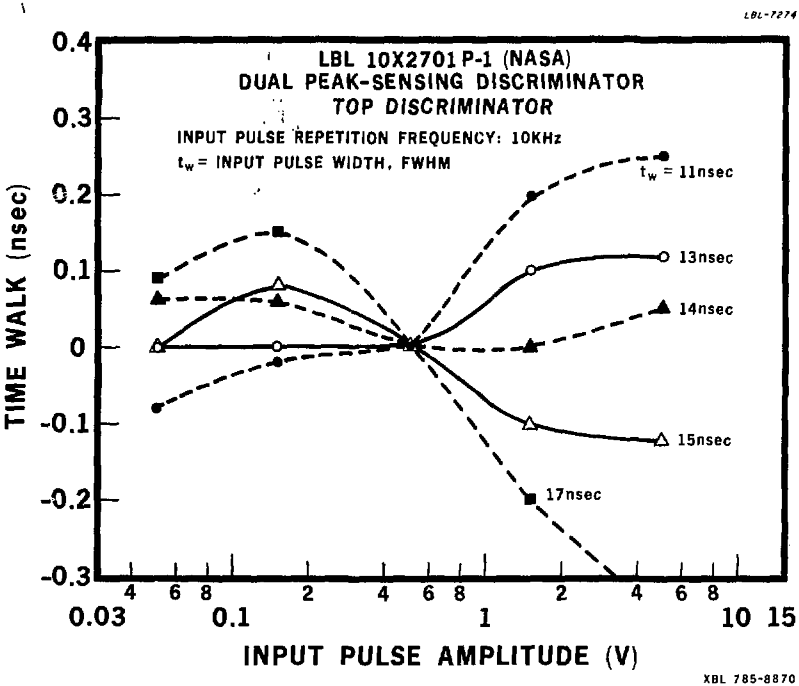
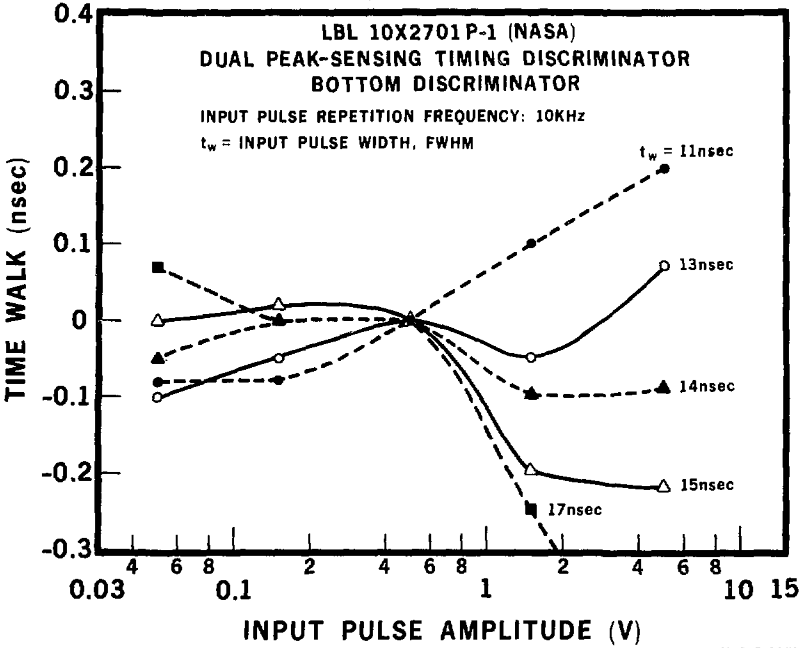

LBL-7274
LBL 10X2701 P-1 (NASA)
DUAL PEAK-SENSING DISCRIMINATOR
TOP DISCRIMINATOR
INPUT PULSE REPETITION FREQUENCY: 10KHz
t_w = INPUT PULSE WIDTH, FWHM
t_w = 11nsec
13nsec
14nsec
15nsec
17nsec
TIME WALK (nsec)
0.4
0.3
0.2
0.1
0
-0.1
-0.2
-0.3
4
6
8
2
4
6
8
2
4
6
8
0.03
0.1
1
10
15
INPUT PULSE AMPLITUDE (V)
XBL 785-8870

Fig. 6

LBL-7274



XBL 785-8871

Fig. 7

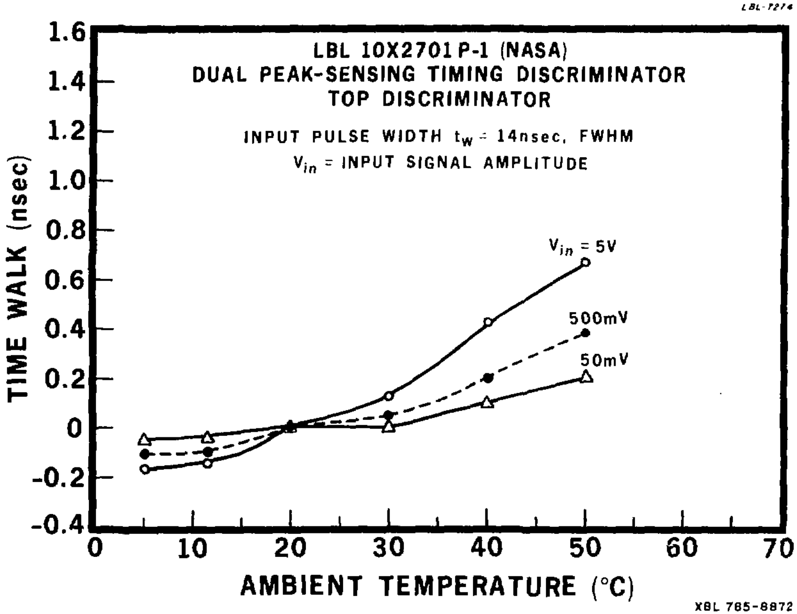

LBL-7274
LBL 10X2701 P-1 (NASA)
DUAL PEAK-SENSING TIMING DISCRIMINATOR
TOP DISCRIMINATOR
INPUT PULSE WIDTH t_W = 14nsec, FWHM
V_{in} = INPUT SIGNAL AMPLITUDE
V_{in} = 5V
500mV
50mV
TIME WALK (nsec)
1.6
1.4
1.2
1.0
0.8
0.6
0.4
0.2
0
-0.2
-0.4
0
10
20
30
40
50
60
70
AMBIENT TEMPERATURE (°C)
XBL 765-8872

Fig. 8

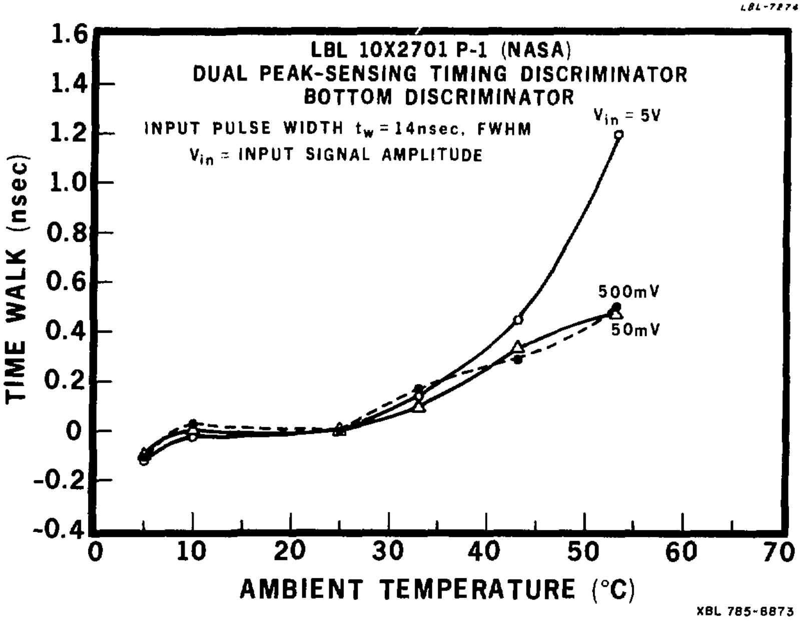

LBL-7274
LBL 10X2701 P-1 (NASA)
DUAL PEAK-SENSING TIMING DISCRIMINATOR
BOTTOM DISCRIMINATOR
INPUT PULSE WIDTH t_w = 14nsec, FWHM
V_{in} = INPUT SIGNAL AMPLITUDE
V_{in} = 5V
500mV
50mV
TIME WALK (nsec)
1.6
1.4
1.2
1.0
0.8
0.6
0.4
0.2
0
-0.2
-0.4
0
10
20
30
40
50
60
70
AMBIENT TEMPERATURE (°C)
XBL 785-8873

Fig. 9

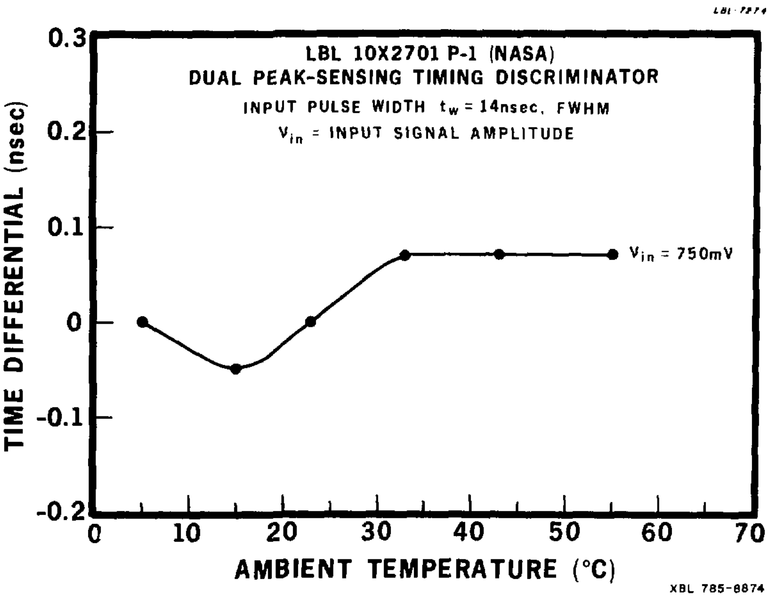
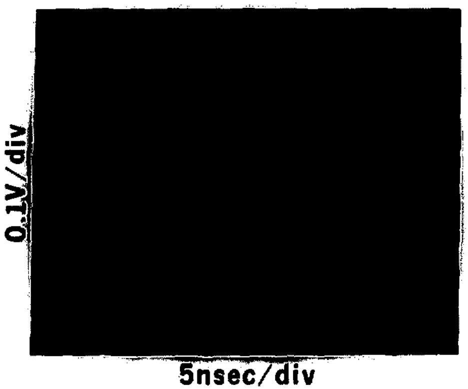

LBL-7874
LBL 10X2701 P-1 (NASA)
DUAL PEAK-SENSING TIMING DISCRIMINATOR
INPUT PULSE WIDTH t_w = 14nsec, FWHM
V_{in} = INPUT SIGNAL AMPLITUDE
V_{in} = 750mV
TIME DIFFERENTIAL (nsec)
0.3
0.2
0.1
0
-0.1
-0.2
0
10
20
30
40
50
60
70
AMBIENT TEMPERATURE (°C)
XBL 785-8874

Fig. 10

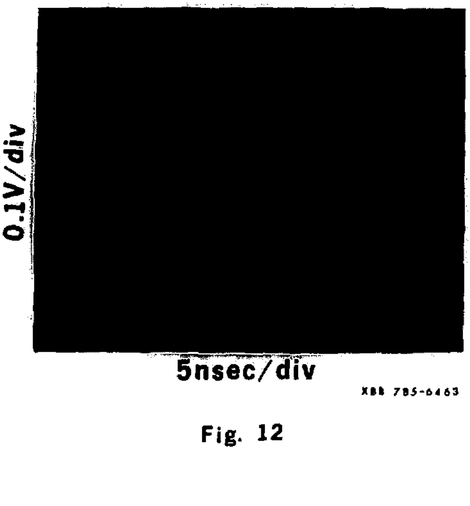
LBL-7274



XBB 785-6462

Fig. 11

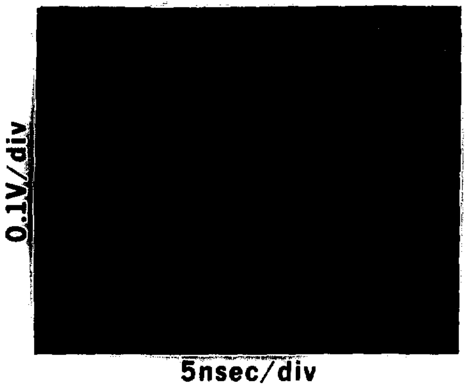
LBL-7274



XBB 785-6463

Fig. 12

LBL-7274



XBB 785-6464

Fig. 13

LBL-7274

XBB 785-6465

Fig. 14

XBB 785-6466

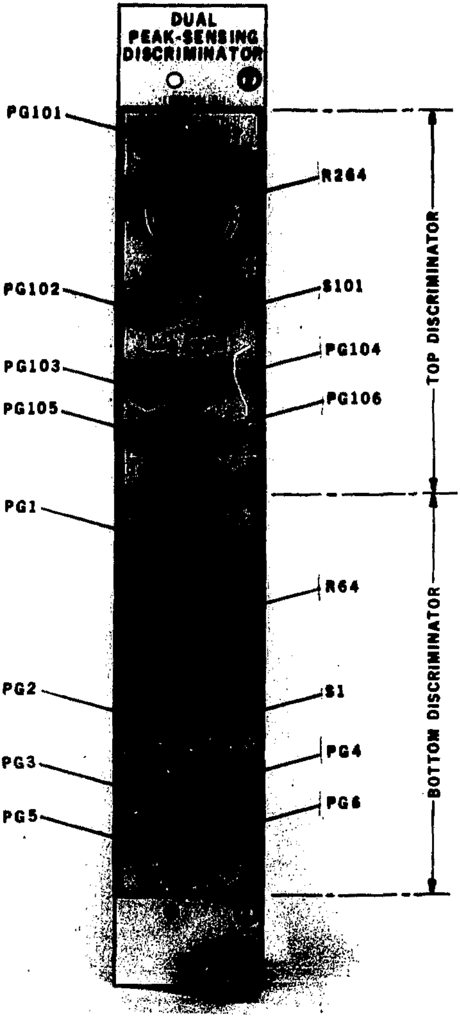
Fig. 15

LBL-7274

XBB 785-6467

Fig. 16

LBL-7874

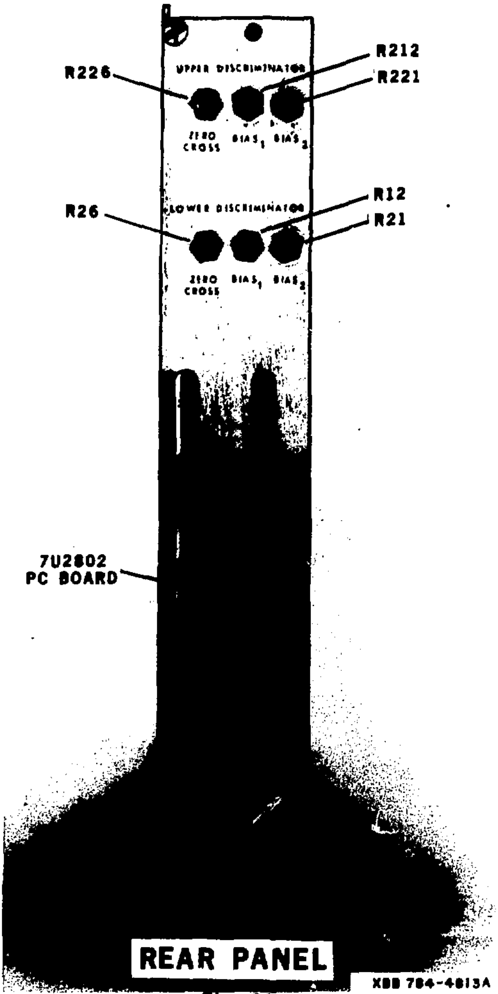


FRONT PANEL

XBB 784-4811A

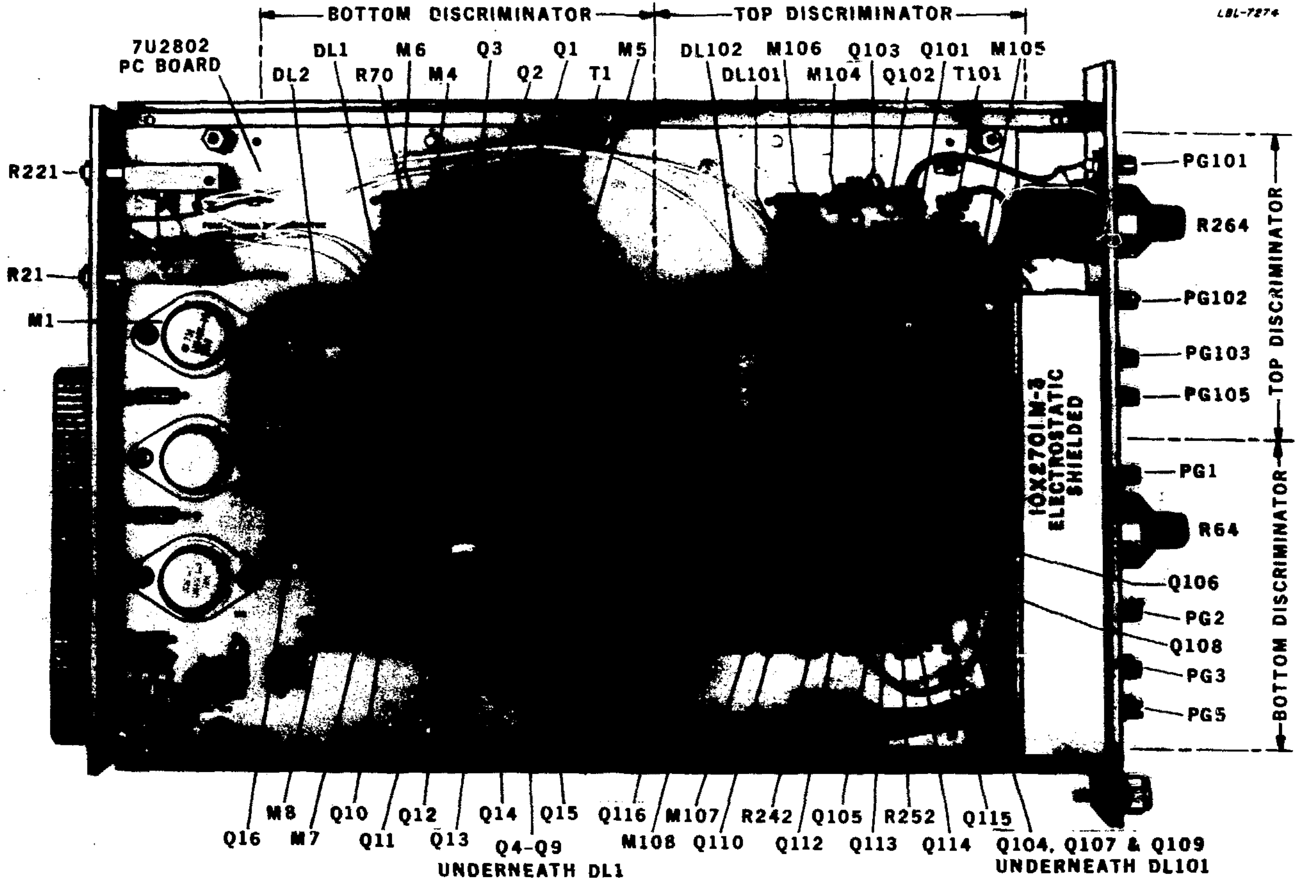
Fig. 17

LBL-7274



XBB 784-4813A

Fig. 18



LEFT SIDE VIEW

Fig. 19

XBB 784-4816A

RIGHT SIDE VIEW

XBB 784-4817A

Fig. 20