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Analysis of Multiple Faults in Synchronous Sequential Circuits by Boolean Difference Techniques

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ANALYSIS OF MULTIPLE FAULTS IN SYNCHRONOUS SEQUENTIAL CIRCUITS BY BOOLEAN DIFFERENCE TECHNIQUES

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ABSTRACT

The Boolean difference is a mathematical concept which has found significant application in the study of single and multiple "stuck at" faults in combinational logic circuits. In this paper, the concept of vector Boolean difference is extended to the analysis of multiple stuck-at faults in synchronous sequential circuits. A vector Boolean difference technique is utilized to determine the set of input/state pairs that will produce a difference in either output or next-state between the fault-free and faulty circuits. Assuming that the fault-free and faulty circuits start in the same initial state, they must be driven by applying a sequence of input vectors to a state in which either a difference in output or next-state is evidenced. If a difference in output cannot be achieved immediately, a second sequence of input vectors must be applied in order to propagate the state difference to the output. Methods for combining the Boolean difference analysis with techniques for deriving the required input vector sequence are discussed.

INTRODUCTION

Fault analysis in digital circuits has emerged as one of the principal research areas in fault-tolerant computing. As LSI realizations of digital circuits have increased in popularity, the problem of generating fault-detection test sets for complex sequential circuits has increased in importance. Significant results have been achieved in generating tests for combinational logic circuits under the assumption that only single-fault situations can occur. However, there are cases where multiple-fault situations must be considered. Several authors [1], [2] have recently extended the Boolean difference technique to the multiple fault case. In this paper, the concept of vector Boolean difference is further extended to the analysis of multiple stuck-at faults in synchronous sequential circuits.

Treating the current state of the circuit as a pseudo-input vector and the next-state as a pseudo-output vector, a vector Boolean difference technique is utilized to determine the set of input/state pairs that will produce a difference in either output or next-state between the fault-free and faulty circuits. Assuming that the fault-free and faulty circuits start in the same initial state, they must be driven by applying a sequence of input vectors to a state in which either a difference in output or next-state is evidenced. If a difference in output cannot be achieved immediately, a second sequence of input vectors must be applied in order to propagate the state difference to the output. Methods for combining the Boolean difference analysis with techniques for deriving the required input vector sequences are discussed.

CIRCUIT DESCRIPTION

Consider a synchronous sequential circuit with m inputs, n outputs, and b-bits of memory, Figure 1. These quantities are described by the three vectors

$$\text{Input Vector} = \underline{X}(k) = \left[X_1(k),\ X_2(k),\ldots,X_m(k)\right]$$

$$\text{Output Vector} = \underline{Y}(k) = \left[Y_1(k),\ Y_2(k),\ldots,Y_n(k)\right]$$

$$\text{State Vector} = \underline{S}(k) = \left[S_1(k),\ S_2(k),\ldots,S_b(k)\right]$$

where k is the time parameter, and $X_i(k)$, $1 \leq i \leq m$, $Y_i(k)$, $1 \leq i \leq n$, and $S_i(k)$, $1 \leq i \leq b$, $k \geq 0$ are Boolean variables. Assume that the initial state of the circuit is a known $\underline{S}(0)$. Then the behavior of the circuit can be described by two vector-valued Boolean functions

$$\underline{Y}(k) = g[\underline{X}(k),\ \underline{S}(k)]\ ,\quad k \geq 0\ , \tag{1}$$

and

$$\underline{S}(k+1) = \underline{f}[\underline{X}(k),\ \underline{S}(k)]\ ,\quad k \geq 0\ . \tag{2}$$

Equation (1) for the output function can be decomposed as

$$Y_i(k) = {}^{i}g[\underline{X}(k),\ \underline{S}(k)]\ ,\quad 1 \leq i \leq n\ , \tag{3}$$

and the next-state function in Equation (2) is equivalent to

$$S_i(k+1) = {}^{i}f[\underline{X}(k),\ \underline{S}(k)],\quad 1 \leq i \leq b\ . \tag{4}$$

Each line of the circuit is labeled with a unique integer. In addition, the primary inputs are denoted by vector $\underline{X}(k)$ as indicated above. A line numbered j has a logical value $I_j[\underline{X}(k),\ \underline{S}(k)]$ dependent upon the current values of the input and state vectors. The output and next-state functions in Equations (1) and (2) can be modified to explicitly indicate their dependence upon the logical values of internal lines as follows:

$$\underline{Y}(k) = \underline{G}[\underline{X}(k), \underline{S}(k), \underline{I}(k)] \tag{5}$$

and

$$\underline{S}(k + 1) = \underline{F}[\underline{X}(k), \underline{S}(k), \underline{I}(k)] \tag{6}$$

where vector $\underline{I}(k)$ has the form

$$\underline{I}(k) = \left[I_{j1}(k), I_{j2}(k), \ldots, I_{jp}(k)\right] \quad . \tag{7}$$

These concepts can be illustrated by the logic circuit in Figure 2. It is assumed that the T flip-flops are properly clocked and possess the state equation

$$S(k + 1) = \overline{T}\, S(k) + T\, \overline{S}(k) = T \oplus S(k) \quad . \tag{8}$$

The primary outputs can be expressed in terms of the inputs and flip-flop states as

$$\begin{aligned} Y_1(k) &= S_1(k)\, S_2(k) \\ Y_2(k) &= \overline{X}_2(k) \quad . \end{aligned} \tag{9}$$

The next-state function is described by

$$\begin{aligned} S_1(k + 1) &= \overline{X}_1(k)\, S_1(k) + X_1(k)\, \overline{S}_1(k) = X_1(k) \oplus S_1(k) \\ S_2(k + 1) &= \overline{I}_{14}(k)\, S_2(k) + I_{14}(k)\, \overline{S}_2(k) = I_{14}(k) \oplus S_2(k) \end{aligned} \tag{10}$$

where

$$I_{14}(k) = X_2(k)\, S_1(k) + \overline{X}_2(k)\, \overline{S}_1(k) \quad . \tag{11}$$

If we are specifically interested in lines 10 and 12, we can rewrite Equation (11) to indicate this, result in

$$I_{14}(k) = I_{12}(k) + \bar{S}_1(k)\, I_{10}(k) \quad . \tag{12}$$

When we are concerned with a specific subset of lines, j1, j2,...,jp, we will denote the output and next-state functions resulting from setting $I_{j1} = a_{j1}$, $I_{j2} = a_{j2},\ldots,I_{jp} = a_{jp}$, where $a_{ji} \epsilon \{0,1\}$, $i = 1, 2,\ldots,p$, as $\underline{G}[\underline{X}(k), \underline{S}(k), a_{j1}, a_{j2},\ldots,a_{jp}]$ and $\underline{F}[\underline{X}(k), \underline{S}(k), a_{j1}, a_{j2},\ldots,a_{jp}]$, respectively. For example, in Figure 2, if

$$I_{12}(k) = 0 \quad \text{and} \quad I_{10}(k) = 1 \quad ,$$

then $I_{14}(k) = \bar{S}_1(k)$ and $S_2(k + 1) = S_1(k)\, S_2(k) + \bar{S}_1(k)\, \bar{S}_2(k)$.

FAULTY CIRCUITS

The type of fault under consideration in this paper is representable as the logical values of a group of lines in the circuit being permanently stuck at the logical value one (s-a-1) or permanently stuck at the logical value zero (s-a-0). Fault situations in which lines $I_{j1}, I_{j2},\ldots,I_{jp}$ are stuck at $a_{j1}, a_{j2},\ldots,a_{jp}$, respectively, $a_{ji} \epsilon \{0,1\}$, $i = 1, 2,\ldots,p$, will be denoted $I_{j1}(\text{s-a-}a_{j1}), I_{j2}(\text{s-a-}a_{j2}),\ldots,I_{jp}(\text{s-a-}a_{jp})$. In Figure 2 the multiple fault consisting of line 12 stuck at 0 and line 10 stuck at 1 is written $I_{12}(\text{s-a-0}), I_{10}(\text{s-a-1})$.

Assume both the fault-free and faulty machines start in the same initial state $\underline{S}(0)$. A test, $t[\underline{S}(0)]$, for a multiple fault in a sequential circuit with initial state $\underline{S}(0)$ is defined as a finite sequence of input vectors, the application of which will cause the output of the fault-free circuit to differ from that of the faulty circuit. A complete test set for the multiple fault $I_{j1}(\text{s-a-}a_{j1}), I_{j2}(\text{s-a-}a_{j2}),\ldots,I_{jp}(\text{s-a-}a_{jp})$,

denoted $T_{\underline{S}(0)}[I_{j1}(s\text{-}a\text{-}a_{j1}),\ldots,I_{jp}(s\text{-}a\text{-}a_{jp})]$, contains every sequence of input vectors which will detect this fault. A minimal test sequence for a given collection of faults is the shortest sequence of input vectors which will determine the presence or absence of any fault in the collection. The minimal test sequence is not necessarily unique.

In considering multiple faults, we must determine the dominating faults and discuss equivalent faults. Two faults, α and β, in a synchronous sequential circuit starting in an initial state $\underline{S}(0)$ are said to be "strongly equivalent" if the output and next-state function of the circuit with fault α, are identical to those of the circuit with fault β. That is

$$\underline{g}_{\alpha} = \underline{g}_{\beta} \tag{13}$$

and

$$\underline{f}_{\alpha} = \underline{f}_{\beta} \quad . \tag{14}$$

"Strong equivalence" (of faults in a synchronous sequential circuit resettable to an initial state $\underline{S}(0)$) is identical to the concept of equivalence of faults in the combinational circuit derived from the synchronous sequential circuit by breaking all feedback loops and considering the current state vector as a pseudo-input and the next-state vector as a pseudo output.

As an example, consider the combinational circuit in Figure 3. This circuit was obtained from the sequential circuit in Figure 2 by breaking the feedback loops. Line numbers in Figure 3 are consistent with those in Figure 2. The input and state vectors (X_1,X_2) and (S_1,S_2) form the new input vector to the combinational circuit, and the output and next-state vectors (Y_1,Y_2) and (S_1^+,S_2^+) form the new output vector.

If faults α and β are strongly equivalent, the tests for faults α and β are identical. Moreover, for some multiple faults, a subset of the faults may dominate the others in the set under consideration. In

Figure 3, the triple fault I_{14}(s-a-1), I_5(s-a-0), I_9(s-a-1) is equivalent to the single fault I_{14}(s-a-1). Therefore, it is necessary to test only for the presence of the dominating fault I_{14}(s-a-1). A multiple fault which contains only dominating faults is called a reduced multiple fault. Only reduced multiple faults will be considered in the following.

In a combinational circuit, any multiple fault with dominating faults has an equivalent reduced multiple fault, and this reduced multiple fault is unique [1]. Furthermore, only one fault from each set of strongly equivalent faults needs to be considered in the process of test sequence generation, since tests for strongly equivalent faults are identical. Thus, from each set of strongly equivalent faults in a synchronous sequential circuit, only one reduced multiple fault need be considered.

BOOLEAN DIFFERENCE EXPRESSIONS FOR MULTIPLE FAULTS IN SEQUENTIAL CIRCUITS

Consider a fault involving the p internal variables

$$\underline{I} = \left[I_{j1}, I_{j2}, \ldots, I_{jp}\right]$$

simultaneously. The vector Boolean difference of the output $\underline{Y}$ with respect to $\underline{I}$ can be defined as

$$\Omega_{j1j2\ldots jp}\,\underline{Y} = \sum_{\ell=1}^{n} {}^{\ell}G[\underline{X},\underline{S},\underline{I}] \oplus {}^{\ell}G[\underline{X},\underline{S},\overline{\underline{I}}] \quad . \tag{15}$$

Similarly, the vector Boolean difference of the next state $\underline{S}^{+}$ with respect to $\underline{I}$ is

$$\Omega_{j1j2\ldots jp}\,\underline{S}^{+} = \sum_{\ell=1}^{b} {}^{\ell}F[\underline{X},\underline{S},\underline{I}] \oplus {}^{\ell}F[\underline{X},\underline{S},\overline{\underline{I}}] \quad . \tag{16}$$

In Equations (15) and (16), $\underline{\bar{I}} = [\bar{I}_{j1}, \bar{I}_{j2}, \ldots, \bar{I}_{jp}]$, a super-bar means logical complement, + represents the logical OR operation, and $\oplus$ is the exclusive OR. The vector Boolean differences in Equations(15) and (16) equal one if any term in the sum equals one and equal zero only if every term in the sum equals zero. The primary objective is to solve Equation (15) for the input/state pairs that will sensitize the output to differences in the specified internal variables. However, if the output functions do not depend on the selected internal variables, then Equation (16) must be solved for the input/state pairs that sensitize the next state to differences in the internal variables under consideration. If an internal variable affects neither the output nor the next state of a sequential circuit, it is unobservable and may be eliminated without altering the behavior of the circuit.

Define the residual functions of ${}^{\ell}G[\underline{X},\underline{S},\underline{I}]$ and ${}^{\ell}F[\underline{X},\underline{S},\underline{I}]$ as

$$ {}^{\ell}G_o[\underline{X},\underline{S}] = {}^{\ell}G[\underline{X},\underline{S},0,0,\ldots,0] \; ; \quad {}^{\ell}F_o[\underline{X},\underline{S}] = {}^{\ell}F[\underline{X},\underline{S},0,0,\ldots,0] \qquad (17) $$

$$ {}^{\ell}G_1[\underline{X},\underline{S}] = {}^{\ell}G[\underline{X},\underline{S},0,0,\ldots,1] \; ; \quad {}^{\ell}F_1[\underline{X},\underline{S}] = {}^{\ell}F[\underline{X},\underline{S},0,0,\ldots,1] $$

$$ \vdots \qquad\qquad\qquad\qquad \vdots $$

$$ {}^{\ell}G_\alpha[\underline{X},\underline{S}] = {}^{\ell}G[\underline{X},\underline{S}, \text{ p-bit binary number with decimal equivalent } \alpha] \quad {}^{\ell}F_\alpha[\underline{X},\underline{S}] = {}^{\ell}F[\underline{X},\underline{S}, \text{ p-bit binary number with decimal equivalent } \alpha] $$

$$ \vdots \qquad\qquad\qquad\qquad \vdots $$

$$ {}^{\ell}G_{2^p-1}[\underline{X},\underline{S}] = {}^{\ell}G[\underline{X},\underline{S},1,1,\ldots,1] \; ; \quad {}^{\ell}F_{2^p-1}[\underline{X},\underline{S},1,1,\ldots,1] \; . $$

Using the residual functions defined in Equation (17), Equations (15) (16) can be written [2]

$$\Omega_{j1j2\ldots jp}\,\underline{Y} = \sum_{\ell=1}^{n}\sum_{i=0}^{2^{p-1}-1}\left(m_i + m_{2^p-1-i}\right)\left({}^{\ell}G_i \oplus {}^{\ell}G_{2^p-1-i}\right) \tag{18}$$

$$\Omega_{j1j2\ldots jp}\,\underline{S}^{+} = \sum_{\ell=1}^{b}\sum_{i=0}^{2^{p-1}-1}\left(m_i + m_{2^p-1-i}\right)\left({}^{\ell}F_i \oplus {}^{\ell}F_{2^p-1-i}\right) \tag{19}$$

where

$$\begin{aligned} m_o &= \overline{I}_{j1}\,\overline{I}_{j2}\cdots\overline{I}_{jp} \\ m_1 &= \overline{I}_{j1}\,\overline{I}_{j2}\cdots I_{jp} \\ m_{2^p-1} &= I_{j1}\,I_{j2}\cdots I_{jp} \end{aligned} \tag{20}$$

Reversing the order of summation and regrouping terms in Equations (18) and (19), we obtain

$$\Omega_{j1j2\ldots jp}\,\underline{Y} = \sum_{i=0}^{2^{p-1}-1}\left(m_i + m_{2^p-1-i}\right)\sum_{\ell=1}^{n}\left({}^{\ell}G_i \oplus {}^{\ell}G_{2^p-1-i}\right) \tag{21}$$

$$\Omega_{j1j2\ldots jp}\,\underline{S}^{+} = \sum_{i=0}^{2^{p-1}-1}\left(m_i + m_{2^p-1-i}\right)\sum_{\ell=1}^{b}\left({}^{\ell}F_i \oplus {}^{\ell}F_{2^p-1-i}\right) . \tag{22}$$

Consider the specific fault

$$I_{j1}(\text{s-a-}a_{j1}),\ I_{j2}(\text{s-a-}a_{j2}),\ldots,I_{jp}(\text{s-a-}a_{jp}) . \tag{23}$$

Define

$$I_{jk}(a_{jk}) = \begin{cases} I_{jk} & \text{if } a_{jk} = 1 \\ \\ \overline{I}_{jk} & \text{if } a_{jk} = 0 \end{cases} \quad . \tag{24}$$

The complete set of tests for this particular fault situation can be considered to consist of two disjoint subsets of tests [1]. Note that in this section a test, or combinational test, is defined as an input/state vector which when applied to the combinational circuit derived from the given sequential circuit produces a difference in output or next-state between the fault-free and faulty circuits. Tests in the first subset, called Type I, attempt to drive the logical values of all of the lines j1, j2,...,jp to $\overline{a}_{j1}, \overline{a}_{j2},\ldots,\overline{a}_{jp}$, respectively. For example, the Type I tests for the double fault I_{10}(s-a-1), I_{12}(s-a-0) in Figure 3 attempt to set $I_{10} = 0$ and $I_{12} = 1$ simultaneously. Examination of the circuit in Figure 3 shows that $I_{10} = 0$, $I_{12} = 1$ can be achieved by setting $X_2 = S_1 = 1$. The remaining subset of tests, identified as Type II tests, consists of those tests which attempt to drive only a proper subset of the lines to logical values which are complements of the faulty values. In Figure 3, one Type II test for the fault I_{10}(s-a-1), I_{12}(s-a-0) attempts to set $I_{10} = 0$, $I_{12} = 0$. This is accomplished by making the assignments: $X_2 = 1$, $S_1 = 0$.

For any p lines of a circuit, j1,j2,...,jp, there can be 2^p possible stuck-at faults considering p single faults occurring simultaneously. The complete combinational test set, consisting of Type I tests, for these p^{th} - order multiple faults will be denoted as

$$\beta\left(I_{j1}, I_{j2},\ldots,I_{jp}\right) = \left\{t \,\middle|\, \Omega_{j1j2\ldots jp}\, \underline{Y} + \Omega_{j1j2\ldots jp}\, \underline{S}^{+} = 1\right\} \quad . \tag{25}$$

Every input/state vector resulting from Equation (25) is a combinational test vector for at least one of the 2^p faults on these p lines. The complete set of Type I combinational test vectors for the multiple fault specified in Equation (23) will be denoted by

$$\beta\left[I_{j1}\left(s\text{-}a\text{-}a_{j1}\right),\ I_{j2}\left(s\text{-}a\text{-}a_{j2}\right),\ldots,I_{jp}\left(s\text{-}a\text{-}a_{jp}\right)\right] .$$

Theorem 1 [2]: Consider the combinational logic circuit which results from a given synchronous sequential circuit by regarding the current state as a pseudo-input and the next state as a pseudo-output. The vector Boolean functions which describe the output and next state in terms of input, current state, and relevant internal line values are $\underline{Y} = \underline{G}[\underline{X},\underline{S},\underline{I}]$ and $\underline{S}^{+} = \underline{F}[\underline{X},\underline{S},\underline{I}]$, where $\underline{I} = \left(I_{j1}, I_{j2},\ldots,I_{jp}\right)$. The complete set of combinational test vectors of Type I to detect 2^p possible simultaneous p^{th} - order multiple faults on these p lines is

$$\beta\left(I_{j1}, I_{j2},\ldots,I_{jp}\right) = \left\{t \mid \Omega_{j1j2\ldots jp}\,\underline{Y} + \Omega_{j1j2\ldots jp}\,\underline{S}^{+} = 1\right\}$$

$$= \left\{t \mid \sum_{i=0}^{2^{p-1}-1} \left(m_i + m_{2^p-1-i}\right)\left[\sum_{\ell=1}^{n}\left(\ell_{G_i} \oplus \ell_{G_{2^p-1-i}}\right)\right.\right.$$

$$\left.\left. + \sum_{\ell=1}^{b}\left(\ell_{F_i} \oplus \ell_{F_{2^p-1-i}}\right)\right] = 1\right\} .$$

Corollary 1.1: The complete set of Type I combinational tests to detect the specified multiple fault $I_{j1}\left(s\text{-}a\text{-}a_{j1}\right)$, $I_{j2}\left(s\text{-}a\text{-}a_{j2}\right),\ldots,I_{jp}\left(s\text{-}a\text{-}a_{jp}\right)$ on the p lines j1, j2,...,jp is

$$\beta\left[I_{j1}\left(s\text{-}a\text{-}a_{j1}\right),\ I_{j2}\left(s\text{-}a\text{-}a_{j2}\right),\ldots,I_{jp}\left(s\text{-}a\text{-}a_{jp}\right)\right]$$

$$= \left\{t \mid I_{j1}\left(\bar{a}_{j1}\right)\ I_{j2}\left(\bar{a}_{j2}\right)\ldots I_{jp}\left(\bar{a}_{jp}\right)\left[\Omega_{j1j2\ldots jp}\underline{Y} + \Omega_{j1j2\ldots jp}\underline{S}^{+}\right] = 1\right\}$$

$$= \left\{t \mid m_{2^p-1-\pi}\left[\sum_{\ell=1}^{n}\left(\ell_{G_\pi} \oplus \ell_{G_{2^p-1-\pi}}\right) + \sum_{\ell=1}^{b}\left(\ell_{F_\pi} \oplus \ell_{F_{2^p-1-\pi}}\right)\right] = 1\right\}$$

where the notation defined in Equation (24) is used in Cor. 1.1 and $a_{j1}a_{j2}\ldots a_{jp}$ is a p-tuple of decimal equivalent π.

Once again consider the fault I_{10}(s-a-1), I_{12}(s-a-0) in the combinational circuit of Figure 3. $a_{10}\, a_{12} = 10_2 = 2_{10}$. That is, $\pi = 2$ and $2^p - 1 - \pi = 1$ since $p = 2$. $m_1 = \bar{I}_{10}\, I_{12}$. Relevant values of the output and next-state functions are, using Equations (9) and (10)

$$ {}^1G_1 = {}^1G_2 = S_1\, S_2 \qquad (26) $$

$$ {}^2G_1 = {}^2G_2 = \bar{X}_2 \qquad (27) $$

$$ {}^1F_1 = {}^1F_2 = X_1 \oplus S_1 \qquad (28) $$

$$ {}^2F_1 = 1 \oplus S_2 = \bar{S}_2 \;\; ; \;\; {}^2F_2 = \bar{S}_1 \oplus S_2 = S_1\, S_2 + \bar{S}_1\, \bar{S}_2 \;\; . \qquad (29) $$

From Cor. 1.1, the equation to be solved for the combinational test vectors is

$$ \bar{I}_{10}\, I_{12} \left[\bar{S}_2 \oplus \left(S_1\, S_2 + \bar{S}_1\, \bar{S}_2 \right) \right] = 1 \;\; . \qquad (30) $$

As discussed previously, $I_{10} = 0$, $I_{12} = 1$ implies $X_2 = S_1 = 1$. Since $S_1 = 1$, the exclusive-or term in Equation (30) reduces to $\bar{S}_2 \oplus S_2$ which is identically equal to 1. Therefore, by Corollary (1.1), the complete set of Type I combinational tests to detect fault I_{10}(s-a-1), I_{12}(s-a-0) is generated by setting $X_2 = S_1 = 1$. X_1 and S_2 are unspecified. Equations (26) through (29) imply that the fault will be detected by a difference in S_2^+ between the fault-free and faulty circuits. In the fault-free circuit, $S_2^+ = \bar{S}_2$, while in the faulty circuit $S_2^+ = S_2$.

To compute the complete set of Type I and Type II combinational tests for all possible faults, single through $p^{\underline{th}}$ - order on the p lines $j_1 j_2 \ldots j_p$, we must compute the vector Boolean differences of the output and next-state functions with respect to all 2^p different combinations of the p variables $I_{j1}\, I_{j2} \ldots I_{jp}$.

Theorem 2[2]: Consider the combinational logic circuit which results from a given synchronous sequential circuit by regarding the current state as a pseudo-input and the next-state as a pseudo-output. The vector Boolean functions which describe the output and next state in terms of input, current state, and relevant internal line values are $\underline{Y} = \underline{G}[\underline{X},\underline{S},\underline{I}]$ and $\underline{S}^+ = \underline{F}[\underline{X},\underline{S},\underline{I}]$, where $\underline{I} = \left(I_{j1}, I_{j2},\ldots,I_{jp}\right)$. The complete set of Type I and Type II combinational test vectors to detect all possible fault situations from single through $p^{\underline{th}}$ - order on the p lines $j1j2\ldots jp$ is

$$\alpha\left[I_{j1}, I_{j2},\ldots,I_{jp}\right] = \Big\{t \,\Big|\, \Omega_{j1}\,\underline{Y} + \Omega_{j1}\,\underline{S}^+ + \Omega_{j2}\,\underline{Y} + \Omega_{j2}\,\underline{S}^+ \ldots + \Omega_{jp}\,\underline{Y} + \Omega_{jp}\,\underline{S}^+ + \Omega_{j1j2}\,\underline{Y} + \Omega_{j1j2}\,\underline{S}^+ \ldots + \Omega_{j1j2\ldots jp}\,\underline{Y} + \Omega_{j1j2\ldots jp}\,\underline{S}^+ = 1\Big\} \quad .$$

Corollary 2.1: The complete set of Type I and Type II combinational tests to detect the specified multiple fault $I_{j1}\left(s\text{-a-}a_{j1}\right)$, $I_{j2}\left(s\text{-a-}a_{j2}\right),\ldots,$ $I_{jp}\left(s\text{-a-}a_{jp}\right)$ on the p lines j1, j2,...,jp is

$$\begin{aligned}\alpha\Big[I_{j1}\left(s\text{-a-}a_{j1}\right), I_{j2}\left(s\text{-a-}a_{j2}\right),\ldots,I_{jp}\left(s\text{-a-}a_{jp}\right)\Big] = \Big\{t \,\Big|\, & I_{j1}\left(\bar{a}_{j1}\right)\left[\Omega_{j1}\,\underline{Y} + \Omega_{j1}\,\underline{S}^+\right] \\ & + I_{j2}\left(\bar{a}_{j2}\right)\left[\Omega_{j2}\,\underline{Y} + \Omega_{j2}\,\underline{S}^+\right] + \ldots + I_{jp}\left(\bar{a}_{jp}\right)\left[\Omega_{jp}\,\underline{Y} + \Omega_{jp}\,\underline{S}^+\right] \\ & + I_{j1}\left(\bar{a}_{j1}\right)\, I_{j2}\left(\bar{a}_{j2}\right)\left[\Omega_{j1j2}\,\underline{Y} + \Omega_{j1j2}\,\underline{S}^+\right] + \ldots \\ & + I_{j1}\left(\bar{a}_{j1}\right)\, I_{j2}\left(\bar{a}_{j2}\right)\ldots I_{jp}\left(\bar{a}_{jp}\right)\left[\Omega_{j1j2\ldots jp}\,\underline{Y} + \Omega_{j1j2\ldots jp}\,\underline{S}^+\right] = 1\Big\} .\end{aligned}$$

Again considering the fault I_{10}(s-a-1), I_{12}(s-a-0) in Figure 3, the equation in Cor. 2.1 becomes

$$\begin{aligned} & I_{10}(0)\left[\Omega_{10}\,\underline{Y} + \Omega_{10}\,\underline{S}^+\right] + I_{12}(1)\left[\Omega_{12}\,\underline{Y} + \Omega_{12}\,\underline{S}^+\right] \\ & \quad + I_{10}(0)\, I_{12}(1)\left[\Omega_{10,12}\,\underline{Y} + \Omega_{10,12}\,\underline{S}^+\right] = 1 \quad . \end{aligned} \tag{31}$$

Referring once again to Equations (9) and (10), we see that only S_2^+ is a function of I_{10} and I_{12}. Equation (31), therefore, becomes

$$\bar{I}_{10}\,\Omega_{10}\,S_2^+ + I_{12}\,\Omega_{12}\,S_2^+ + \bar{I}_{10}\,I_{12}\,\Omega_{10,12}\,S_2^+ = 1 \quad . \qquad (32)$$

Equation (32) implies that

$$\bar{I}_{10}\,\Omega_{10}\,S_2^+ = 1 \quad \text{or} \quad I_{12}\,\Omega_{12}\,S_2^+ = 1 \quad \text{or} \quad \bar{I}_{10}\,I_{12}\,\Omega_{10,12}\,S_2^+ = 1 \; . \qquad (33)$$

Since $\Omega_{10}S_2^+ = \bar{S}_1$, we must have $S_1 = 0$, $I_{10} = 0$ for the first term in Equation (32) to equal 1. Thus, $X_2 = 1$, $S_1 = 0$ is one Type II test for the fault I_{10}(s-a-1), I_{12}(s-a-0). If this test is used, the fault-free circuit will have a next-state function for S_2 of the form $S_2^+ = S_2$. The faulty circuit will have $S_2^+ = \bar{S}_2$.

Another possibility occurs when $I_{12}\,\Omega_{12}\,S_2^+ = 1$. $\Omega_{12}\,S_2^+ = S_1 + X_2$. Therefore, since $I_{12} = S_1X_2$,

$$I_{12}\,\Omega_{12}\,S_2^+ = X_2\,S_1 \quad . \qquad (34)$$

Setting Equation (34) equal to 1 implies $X_2 = 1$, $S_1 = 1$. In this case, the fault-free circuit will have $S_2^+ = \bar{S}_2$ and the faulty circuit will have $S_2^+ = S_2$.

The third term of Equation (32) equal to 1 results in the condition $X_2 = S_1 = 1$ as discussed in the section on Type I tests. Thus, the complete set of Type I and Type II combinational tests for the specified fault I_{10}(s-a-1), I_{12}(s-a-0) is $\left\{\left(X_2 = 1,\ S_1 = 0\right),\ \left(X_2 = 1,\ S_1 = 1\right)\right\}$. Or, reducing the test set by noticing that setting $X_2 = 1$ produces a combinational test for the specified double fault regardless of the value of S_1, we conclude that the desired test set is $\left\{X_2 = 1\right\}$.

DETECTING AND DIVERGING STATES

If the circuit is in a detecting state for fault π, an input can be applied that will produce a difference in output between the fault-free and fault-π circuits. Let Σ_π^* be the set of detecting states for fault π. Then for any state $\underline{\sigma} \in \Sigma_\pi^*$, there exists an input vector $\underline{x}$ such that the pair $(\underline{x}, \underline{\sigma})$ is a solution to the equation

$$I_{j1}(\bar{a}_{j1})\,\Omega_{j1}\,\underline{Y} + I_{j2}(\bar{a}_{j2})\,\Omega_{j2}\,\underline{Y} + \ldots + I_{jp}(\bar{a}_{jp})\,\Omega_{jp}\,\underline{Y}$$

$$+ I_{j1}(\bar{a}_{j1})\,I_{j2}(\bar{a}_{j2})\,\Omega_{j1j2}\,\underline{Y} + \ldots \qquad (35)$$

$$+ I_{j1}(\bar{a}_{j1})\,I_{j2}(\bar{a}_{j2})\ldots I_{jp}(\bar{a}_{jp})\,\Omega_{j1j2\ldots jp}\,\underline{Y} = 1$$

where

$$(a_{j1}a_{j2}\ldots a_{jp})_2 = \pi_{10} \quad . \qquad (36)$$

It may happen that no detecting states exist for fault π; i.e., $\Sigma_\pi^* = \phi$. For example, this is the case in Figure 2 for the fault I_{10}(s-a-1), I_{12}(s-a-0). Since neither output is a function of the faulty lines, no input/state pair can be applied that will cause a difference in output between the fault-free and faulty circuits. However, input/state pairs exist that will cause a difference in next-state between the fault-free and faulty circuits. Specifically, for the fault I_{10}(s-a-1), I_{12}(s-a-0) as discussed in the previous section, setting $X_2 = 1$ will cause a difference in next state between the fault-free and faulty circuits in Figure 2 for any initial state.

If Σ_π^* is the empty set, we must consider Σ_π^+, the set of diverging states for fault π. When the circuit is in a diverging state for fault π, an input can be applied that will cause the next state of the fault-free circuit to differ from the next-state of the faulty circuit. The input/state pair is a solution to the equation

$$I_{j1}(\bar{a}_{j1})\,\Omega_{j1}\,\underline{S}^{+} + I_{j2}(\bar{a}_{j2})\,\Omega_{j2}\,\underline{S}^{+} + \ldots + I_{jp}(\bar{a}_{jp})\,\Omega_{jp}\,\underline{S}^{+}$$

$$+ I_{j1}(\bar{a}_{j1})\,I_{j2}(\bar{a}_{j2})\,\Omega_{j1j2}\,\underline{S}^{+} + \ldots \qquad (37)$$

$$+ I_{j1}(\bar{a}_{j1})\,I_{j2}(\bar{a}_{j2})\ldots I_{jp}(\bar{a}_{jp})\,\Omega_{j1j2\ldots jp}\,\underline{S}^{+} = 1 \quad .$$

The difference in state must then be propagated to an output in order for the fault to be detected. As mentioned earlier, every state is a diverging state for the fault I_{10}(s-a-1), I_{12}(s-a-0) in Figure 2.

DETECTING FAULT π

Given that the initial state of the circuit is $\underline{S}(0)$ for both fault-free and faulty circuits, the problem is to generate a sequence of input vectors that will detect fault π. This can be accomplished by a modification of the successor tree technique.

If the initial state $\underline{S}(0) \in \Sigma_{\pi}^{*}$, we are guaranteed that a sequence of length 1 exists. That is, we can find an input vector that will immediately detect fault π. However, if $\underline{S}(0) \notin \Sigma_{\pi}^{*}$, we must either drive the circuit to a state in Σ_{π}^{x} or drive the circuit to a state in Σ_{π}^{+} and propagate the resulting difference in state between the fault-free and faulty circuits to an output. In either case, the successor tree is a useful technique for keeping track of the states reached and the outputs generated by the fault-free and faulty circuits. When combined with the Boolean difference method applied to the combinational circuit resulting from the original sequential circuit, efficient test sequences can be generated.

Define $\underline{g}_{\pi}[\underline{X},\underline{S}]$ and $\underline{f}_{\pi}[\underline{X},\underline{S}]$ to be the output and next-state functions respectively of the faulty circuit. For the fault I_{10}(s-a-1), I_{12}(s-a-0) in Figure 2,

$$ {}^{1}g_{\pi}[\underline{X},\underline{S}] = {}_{\pi}Y_1 = S_1 S_2 \tag{38} $$

$$ {}^{2}g_{\pi}[\underline{X},\underline{S}] = {}_{\pi}Y_2 = \bar{X}_2 \tag{39} $$

$$ {}^{1}f_{\pi}[\underline{X},\underline{S}] = {}_{\pi}S_1^{+} = X_1 \oplus S_1 \tag{40} $$

$$ {}^{2}f_{\pi}[X,S] = {}_{\pi}S_2^{+} = \bar{S}_1 \oplus S_2 \tag{41} $$

These equations correspond to Equations (9) and (10) for the fault-free circuit.

Consider now the generation of a test sequence for the fault I_{10}(s-a-1), I_{12}(s-a-0) in the circuit of Figure 2 starting in state $S_1 = 0$, $S_2 = 0$. The example following Cor. 2 .1 shows that no detecting states exist for this fault, but that all states are diverging states; i.e., $\Sigma_{\pi}^{*} = \phi$ and $\Sigma_{\pi}^{+} = U$, where U is the universal set. Furthermore, the Boolean difference procedure produces the result that setting $X_2 = 1$ will cause a difference in S_2^{+} between the fault-free and faulty circuits. This information is entered in the successor tree as indicated in Figure 4. Only one entry is made in each position because the results for the fault-free and faulty circuits are identical. Note that the elements of the input, output, and state vectors are written horizontally, and $X_1(0)$ is left unspecified. The alternative possible input, $X_1(0)$ 0, is not followed up immediately. However, all alternatives are saved for future reference.

The next state for the fault-free circuit (Equation 10) is $S_1^{+} = X_1 \oplus 0 = X_1$, $S_2^{+} = S_1 \oplus S_2 = 0$. Equations (40) and (41) imply that ${}_{\pi}S_1^{+} = X_1$, ${}_{\pi}S_2^{+} = 1$ in the faulty circuit. This information is entered in the successor tree as indicated in Figure 5, where the fault-free circuit information is entered to the left of the faulty circuit information, and the two vectors are separated by a comma.

Equations can now be written to ascertain the input required to cause a difference in output at t = 1.

$$1 = Y_1(1) \oplus {}_{\pi}Y_1(1) = S_1(1)\, S_2(1) \oplus {}_{\pi}S_1(1)\, {}_{\pi}S_2(1)$$

$$= X_1(0) \cdot 0 \oplus X_1(0) \cdot 1 \qquad (42)$$

$$= X_1(0) \quad .$$

Therefore, if $X_1(0) = 1$, a difference in output will appear at time 1 for any input at time 1. This information is entered into the next refinement of the successor tree in Figure 6. Thus, the desired test sequence is 11, $X_1(1)\, X_2(1)$ where $X_1(1)$ and $X_2(1)$ are left unspecified.

CONCLUSIONS

It has been shown that the Boolean difference method, a powerful tool for the generation of test sets for combinational circuitry, can be effectively utilized in the synthesis of test sequences for multi-output synchronous sequential circuits. Boolean difference equations provide complete sets of combinational tests for the circuit derived from a given sequential circuit by treating the current state as a pseudo-input vector and the next state as a pseudo-output vector. When this information is combined with a successor tree technique for treating the sequentiality of the circuit, it becomes a straightforward procedure to derive test sequences for synchronous sequential circuits.

REFERENCES

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[2] S. R. Das, P. K. Srimani, and C. R. Datta, "On Multiple Fault Analysis in Combinational Circuits by Means of Boolean Difference," Proc. IEEE, Sept. 1976, pp. 1447-1449.

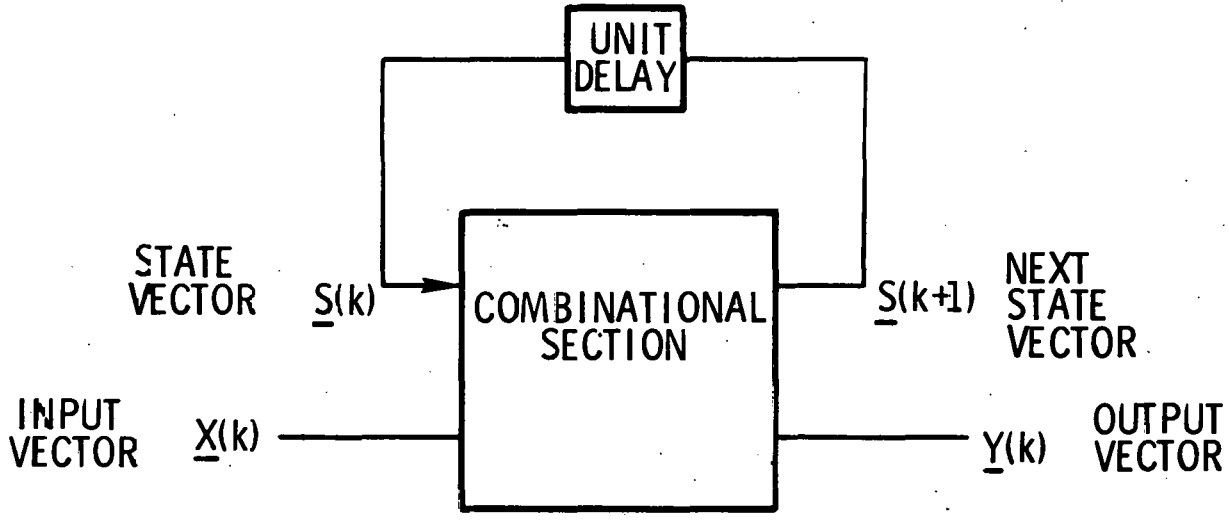

Figure 1. Synchronous Sequential Circuit

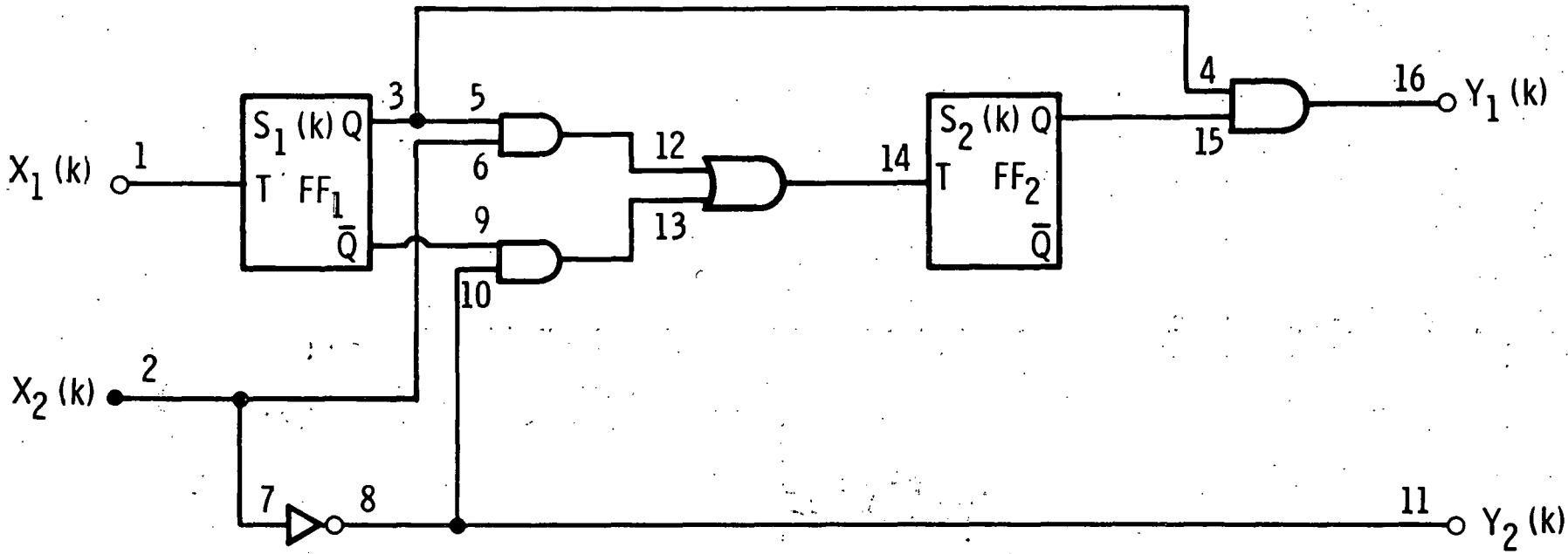

Figure 2. Synchronous Sequential Circuit

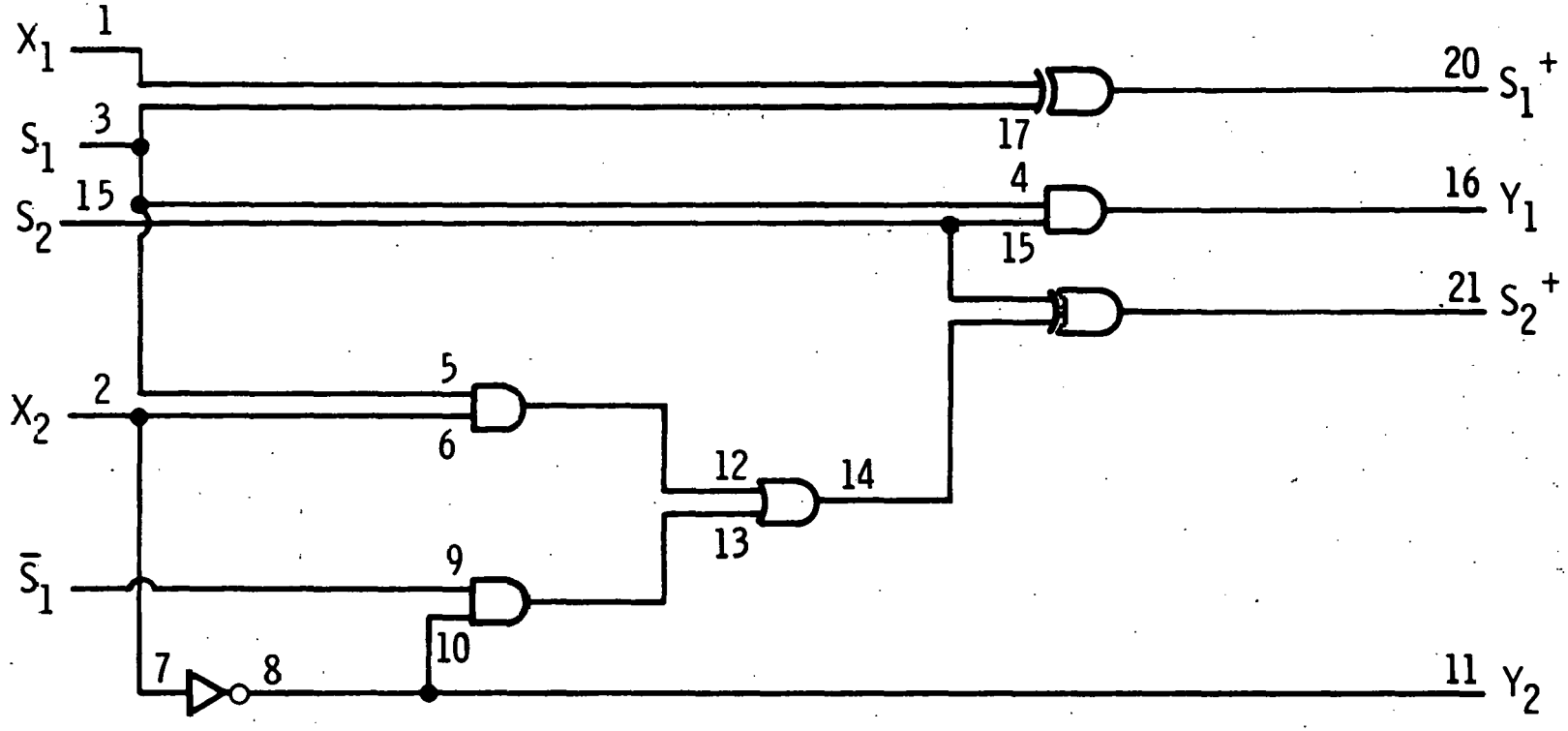

Figure 3. Combinational circuit obtained from synchronous sequential circuit in Figure 2.

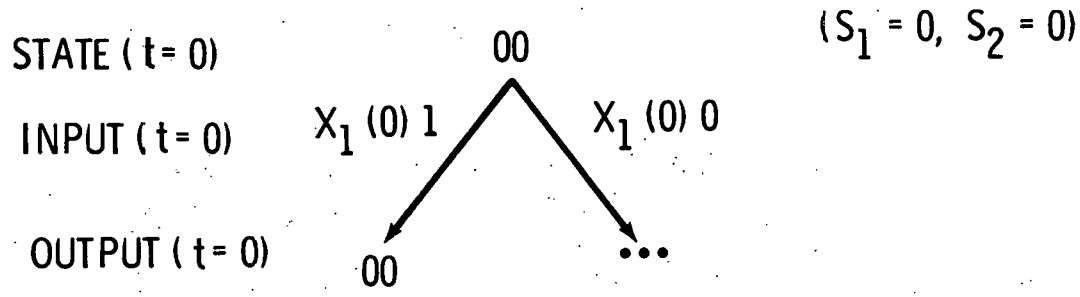

Figure 4. Start of successor tree

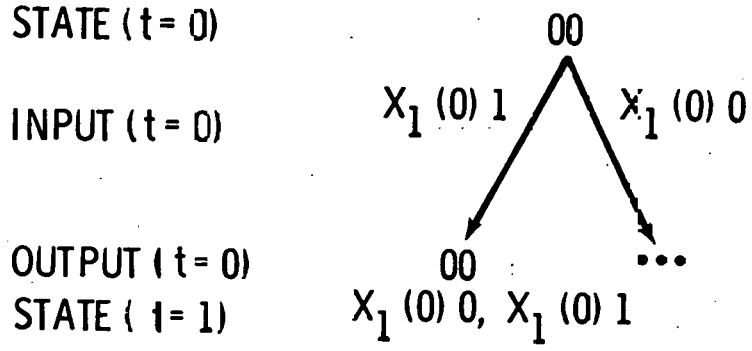

Figure 5. Successor tree at t = 0

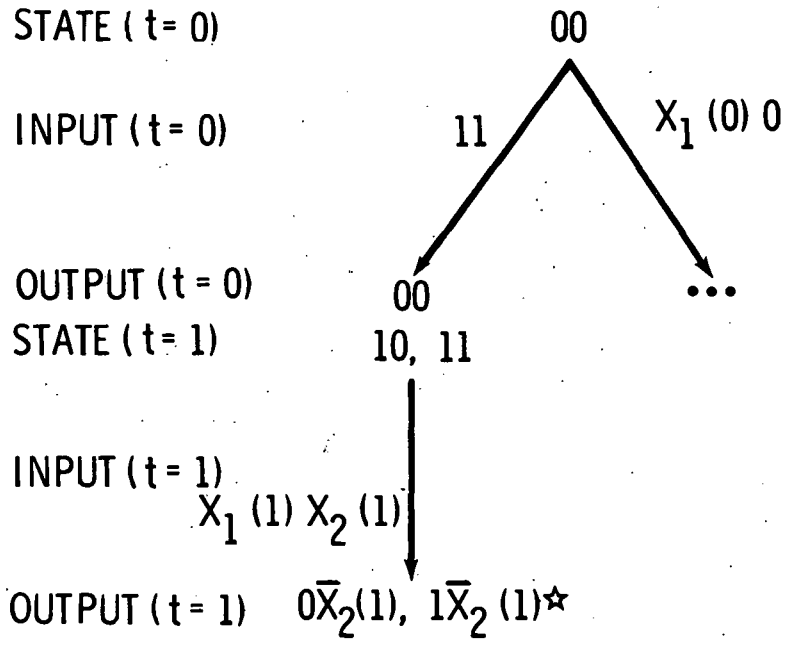

Figure 6. Successor tree with fault detected (indicated by star)

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