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SANDIA REPORT

SAND90—0283 • UC—706
Unlimited Release
Printed May 1990

Standardized Communication Symbols to Facilitate Circuit Design

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Prepared by
Sandia National Laboratories
Albuquerque, New Mexico 87185 and Livermore, California 94550
for the United States Department of Energy
under Contract DE-AC04-76DP00789

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SAND90-0283

Unlimited Release
Distribution Category UC-706
Printed May 1990

SAND--90-0283

DE90 012011

Standardized Communication Symbols to Facilitate Circuit Design

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ABSTRACT

Communication circuit design requires the consideration of many factors such as the specification, configuration, and location of all equipment and media involved. To aid the design process, a set of communication symbols was developed. The symbols not only simplify design, but provide standardization to minimize interpretation problems among circuit designers.

This report describes this set of symbols and how to use them.

ACKNOWLEDGEMENT

Overall design of the communication symbols was a joint effort by the authors of this report and Mark E. Wilkins (formerly Division 2648). Doug L. Bickel, Division 2346, contributed to the design of the Local Area Network symbols. In addition, Edward L. Witzke (BDM International, Inc.) contributed ideas for the presentation of this material.

CONTENTS

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Standardized Communication Symbols to Facilitate Circuit Design

I. Management Summary

Today, data communication engineers are able to treat most circuit elements or segments as black boxes, but they may have to string many segments together to form a useful communication pipeline. In addition, the interaction of digital signals at the interfaces of these segments is not well documented. For these and other reasons, the communication circuit design process is not standardized.

In the course of communication circuit design at Sandia National Laboratories, a set of communication symbols was created to aid, and hopefully standardize, the design process. These symbols, which allow the designer to build a circuit using black boxes, simplify circuit design and documentation. They also provide a standard set to help minimize interpretation problems among circuit designers.

The symbols can be used to represent various devices in a circuit, such as modems, computers, terminals, encryption devices, converters, etc. When using these symbols to design communication circuits, the contours of each symbol show which devices interface together. Mismatched device contours indicate the need for another element (such as a null modem) between the two devices. In addition, the propagation of clock, data, and control signals through the circuit can be represented. Clocking modes on synchronous components (modems, multiplexers, etc.) and signal line crossovers can also be determined from the drawings during the design process.

By designing with these symbols, drawings can be kept up-to-date, thus providing detailed circuit documentation as a circuit evolves. This set of symbols, along with the rules of their use, comprise a very efficient design and documentation tool. To encourage the use of the symbols, plastic templates of the symbol set have been manufactured and distributed to circuit designers at various national laboratories.

Chapters II through V of this paper deal with the construction of the symbols; including basic shape, individual symbol design, and the symbol templates. Chapters VI, VII, and the Appendix illustrate the use of these symbols; including a data communication primer and actual design methodology. It is suggested that readers unfamiliar with data communication (and associated terminology) scan Chapter VI before proceeding.

This report mainly deals with what is termed standard digital data communication. This includes communication devices using the EIA (Electronic Industries Association) RS232 and RS449 standards and the CCITT (Consultative Committee in International Telegraphy and Telephony) V.35 standard. For expediency, EIA RS449 signal names will be used throughout this report.

Additional symbols have been designed for AT&T (American Telephone & Telegraph) DS-1 communication components. Symbols for Ethernet/Local Area Network data communication components have been compiled from various texts and, in some instances, modified. These symbol sets are discussed in Chapter IV and templates appear in Chapter V.

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II. Introduction

A. Definition of DTE and DCE

The basic symbol shapes were designed to differentiate between the two major classes of communication equipment; DTEs and DCEs. Typical examples of DTEs are computers and terminals and examples of DCEs are modems and multiplexers. Following are definitions of DTE and DCE taken from FED-STD 1037, Glossary of Telecommunication Terms.

DATA TERMINAL EQUIPMENT (DTE). 1. Equipment consisting of digital end instruments that convert the user information into data signals for transmission, or reconvert the received data signals into user information. 2. The functional unit of a data station that serves as a data source or a data sink and provides for the data communication control function to be performed in accordance with the link protocol.

DATA CIRCUIT-TERMINATING EQUIPMENT (DCE). The interfacing equipment sometimes required to couple the DTE (data terminal equipment) into a transmission circuit or channel and from a transmission circuit or channel into the DTE. Synonym: DATA COMMUNICATIONS EQUIPMENT.

Alternate definitions are provided for clarification.

DTE: 1. Any circuit interface that sends out the signal Send Data (SD) and receives the signal Receive Data (RD). 2. A data source or a data sink (the origin or destination of data to be communicated).

DCE: 1. Any circuit interface that receives the signal Send Data and sends out the signal Receive Data. 2. Equipment that takes data from a data source and delivers it to a data sink.

B. Development of the Symbols

Traditionally, data communication circuits are designed on paper using square boxes to represent the various circuit elements, such as terminals and modems. These boxes, when connected by simple lines, become the working design drawing. Relatively little information is contained in these drawings except for the designers' (usually sporadic) annotations. This limits the drawing's usefulness as a design tool and also compounds interpretation problems among the designers. Circuit troubleshooting also suffers from the lack of adequate documentation. In addition, these drawings usually span several pages; further hindering understanding and fault isolation.

A method was needed to standardize communication circuit design in order to try to avoid these documentation and interpretation problems. To do this, symbols were created to replace the square boxes and a drawing methodology was created to manipulate these symbols.

The symbols include various polygon designs to differentiate their function from one another. This allows instant identification of a DTE or DCE interface. In addition, symbol shapes are compounded to form devices with more than one interface, eg., a multiplexer, and to depict paired devices, eg., a modem pair. In this way, information about devices in a circuit is conveyed simply by the shape of their respective symbols.

Additional graphics are used within the symbols to depict important circuit information such as data and clock signal paths, clocking modes, and internal device processes (such as data buffering). This combination of symbol shape and graphics conveys device settings and operation to the designers and troubleshooters.

The method for drawing with these symbols is, in part, based on general circuit design methods. The major circuit components are determined first and then drawn in their respective positions. Usually, terminals and computers are placed at the ends and communications devices are placed in the middle. Since the interface between any two devices is the joining of a DTE to a DCE, the shapes of adjacent symbols must fit together. When two adjacent symbols do not match up, it is immediately apparent that an additional device of some kind is needed between the two symbols. As the data, clock, and control signal paths are drawn propagating through the circuit, modem clocking modes and the necessity of signal loopbacks can be determined. (See Chapter VII for detailed information on circuit design.)

Using the symbols with the drawing design methodology leads to accurate and consistent circuit designs. Accuracy improves the communication circuit design process and consistency reduces misinterpretation.

C. Basic DTE and DCE Building Blocks

The DTE shape has its bottom slope in under the top half, as shown in Figure 1a. Since this shape uniquely identifies a DTE, confusion about signal direction is avoided. The upper section of the symbol is used for control signals while the bottom section is used for clock and data signals. When a DTE Pair (Figure 1b.) is used to perform signal crossover between two DCEs (two tail circuits), the pair is drawn as one symbol. This device is also known as a null DTE.

The DCE shape has its bottom slope out away from the top half as shown in Figure 1c. Like the DTE symbols, the DCE symbols use the upper section for control signals and the bottom section for clock and data signals. A DCE Pair, or modem link, is used to connect two DTEs. This modem pair can be drawn as one symbol (Figure 1d.). This symbol is also used to represent a null DCE (or null modem); a device used to interface two co-located DTEs (when a modem link is not needed).

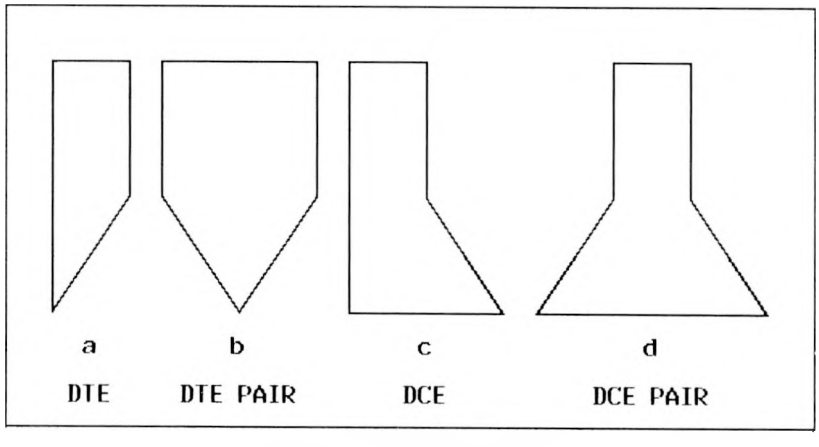

Figure 1. Basic Symbol Shapes

D. Symbol Shape and Dimensions

Figure 2 shows a larger view of a DCE Pair symbol in order to display the symbol proportions and measurements. Each division represents one tenth of an inch for standard digital symbol drawing.

The symbols, after they are drawn with a template or by a computer printer, should be as close as possible to 13 units high. The top of a DTE, DCE, or DCE Pair should be four units wide, the top of a DTE Pair should be eight units wide, and the bottom of a DCE Pair should be 12 units wide. Other standard digital symbols are shown in Chapter III and in the template drawings in Chapter V. Adherence to these proportions assures that later modifications to a drawing can be made accurately.

EIA RS449 signal name abbreviations are shown at their respective locations on the symbol. From the top down, the first five lines are control signals: TR (Terminal Ready), DM (Data Mode), RS (Request to Send), CS (Clear to Send), and RR (Receiver Ready). The remaining five lines are clock and data signals: TT (Terminal Timing), ST (Send Timing), SD (Send Data), RT (Receive Timing), and RD (Receive Data). The function of these signals is covered in detail in Chapter VI., Sections A, B, and C.

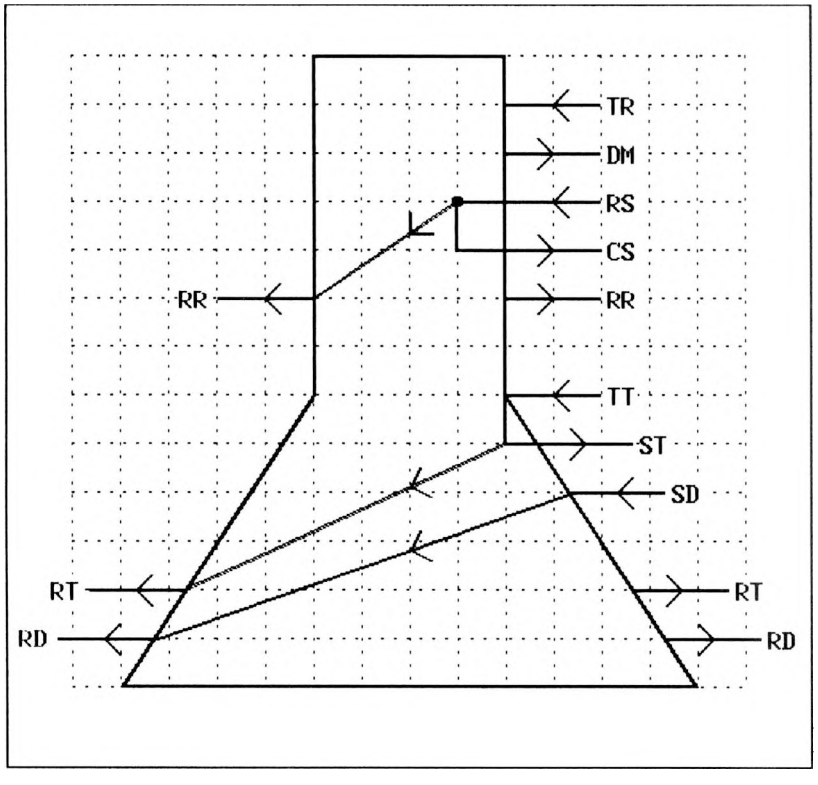

Figure 2. Symbol Proportions

Signal lines that are not required may be left off; eg., when a modem is not being externally clocked, the TT line does not need to be shown. Signal line designations should be used sparingly so as not to clutter up the drawing. Arrows can and should be drawn on the signal lines to indicate signal flow.

Data lines are not shown on synchronous circuit drawings when only the clock signals are of concern. This is done by the circuit designer for expediency. For asynchronous circuits, only the data lines (and sometimes control signals) are shown since there are no explicit clocks in a circuit of this type (data generation and sampling clocks are implicitly regenerated at each piece of equipment).

Ground leads, such as SG (Signal Ground), SC (Send Common), RC (Receive Common), and Shield, can be drawn below a symbol to show their presence in a circuit. Other information, such as equipment location, interface protocols, etc., can be written in or around the symbols. See the circuits in the Appendix for examples of this.

III. Standard Digital Symbols

This chapter will discuss, in detail, the various symbols that make up the standard digital symbol set. DS-1 Standard and Local Area Network symbols will be briefly discussed in Chapter IV.

A. DTEs, Null DTEs, and Null DTE Fifos

By DTE Alternate Definition 2, a DTE is a device that is a data source or sink. Common examples of DTEs are computers and terminals. The DTE shape, whether drawn right or left, always has its bottom half slope in under its top half as shown in Figure 3.

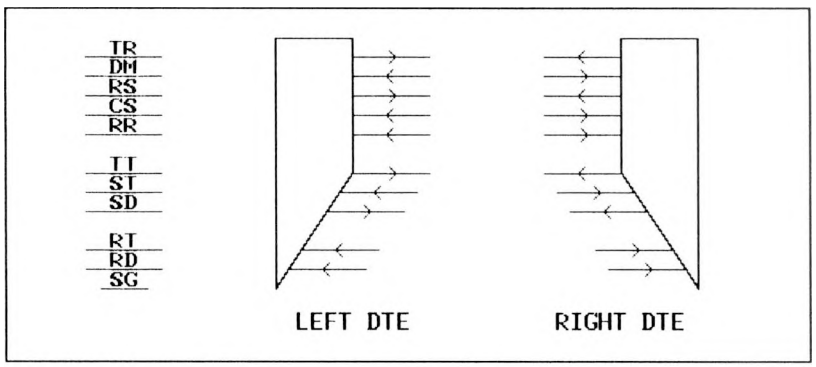

Figure 3. DTE Symbols

DTE Alternate Definition 1 states that a DTE sends out the signal Send Data and receives Receive Data. In Figure 3, it can be seen that on both the right and left DTE, SD is an output (note the arrow direction) and RD is an input. This will be true for any DTE interface on any of the symbols.

When back-to-back DTEs are required, they can be drawn as one symbol. This is commonly referred to as a null DTE. Figure 4a. shows the null DTE with its signal crossovers.

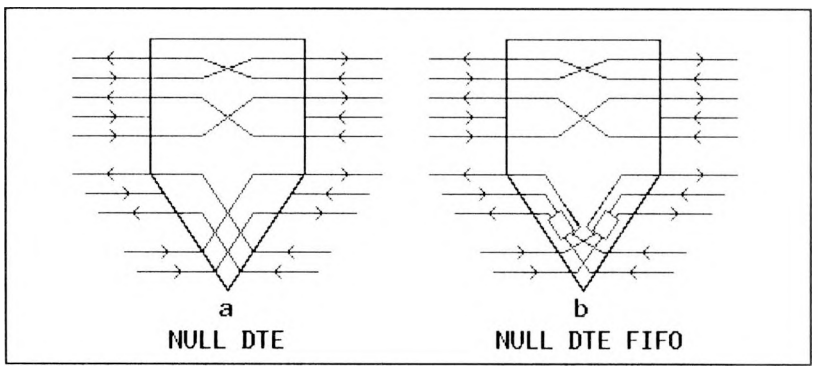

Figure 4. Null DTE Symbols

The null DTE is commonly used where a DCE interface needs to interface directly to another DCE. This "interface conversion" is accomplished by crossing over a pair of data lines, a pair of clock lines, and two pairs of control lines. In multi-segment communication circuits (with multiple modem pairs), a null DTE is used to perform signal crossover between modems of different segments. (See DTE/DCE Interfacing in Section C.)

Often, a null DTE is sufficient to perform signal crossover between two DCEs. But when the clock phase difference between the two DCEs is near 180 degrees, data errors will occur. The null DTE fifo (Figure 4b.) is designed to absorb this phase error. (See Chapter VI, Section D. in this report and SAND88-0175, Null DTE Fifo Buffer for Multi-Segment Communications Circuits for additional details.)

A null DTE fifo is a null DTE with the addition of first-in-first-out (FIFO) buffers along the data paths through the device. Since this device is symmetrical (with bi-directional data paths), only one path, left to right, will be examined closely.

Referring to Figure 5, it can be seen that RD from the left side is clocked into the buffer with the left side RT. The same data, delayed less than one bit time, is clocked out of the buffer as the right side SD by the right side ST. By buffering data in this manner, phase differences between RT on one side and ST on the other are ignored. The SD data will always be valid as it is clocked out of the fifo buffer, provided that the RT and ST signals are of the same frequency differing only in phase (having traveled different paths). Additionally, the left side RT is crossed over to the right side TT for use as an external clock source for the DCE that would be on the right side. In the multi-segment circuit case, the left side RT is timing out of a modem in one segment and the right side ST is timing out of a modem in a different segment. This entire operation takes place independently for the data path in the other direction (right to left).

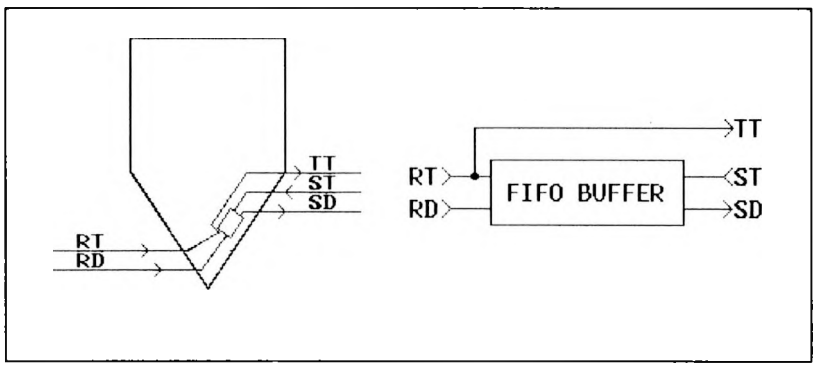

Figure 5. Null DTE Fifo Operation

B. DCEs, Null DCEs, and Modem Pairs

By DCE Alternate Definition 2, a DCE is a device that takes data from a data source and delivers it to a data sink. Common examples of DCEs are modems and multiplexers. The DCE shape, whether drawn right or left, always has its bottom half slope out away from its top half as shown in Figure 6.

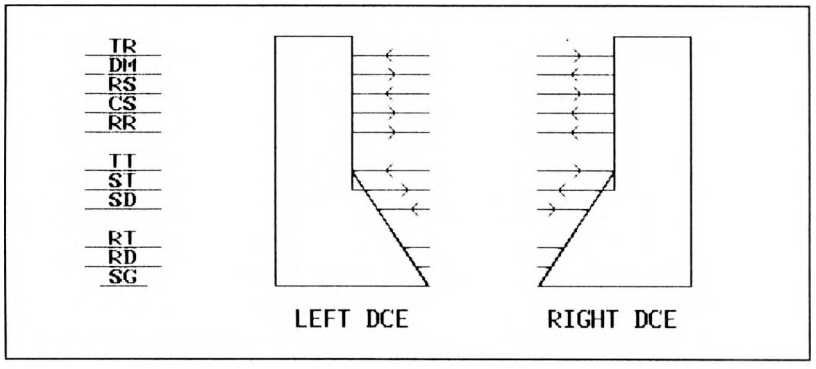

Figure 6. DCE Symbols

DCE Alternate Definition 1 states that a DCE sends out the signal Receive Data and receives Send Data. In Figure 6, it can be seen that on both the right and left DCE, SD is an input (note the arrow direction) and RD is an output. This will be true for any DCE interface on any of the symbols.

When back-to-back DCEs are required, they can be drawn as one symbol. This symbol can represent a null DCE (or null modem). The symbol in Figure 7b. shows the null DCE with its signal crossovers.

The null DCE is commonly used where a DTE interface needs to interface directly with another DTE. This interface conversion is accomplished by crossing over a pair of data lines, a pair of clock lines, and a pair of control lines. Additionally, some signals are looped back to satisfy certain clock and control signal requirements. A null DCE is also used to interface between two co-located DTEs (when a modem link is not needed). (See DTE/DCE Interfacing in Section C.)

A modem link always consists of a pair of modems. The analog side can be shown between the two DCE symbols as in Figure 7a. Normally, the analog side detail is not needed during digital design, and the DCE Pair (modem pair) is drawn as one symbol (Figure 7b.). Since data must enter the local modem as SD and appear at the remote modem as RD, a data signal crossover must take place as shown. (Additional information on modem clocking and control signals can be found in Chapter VI., Sections B. and C.).

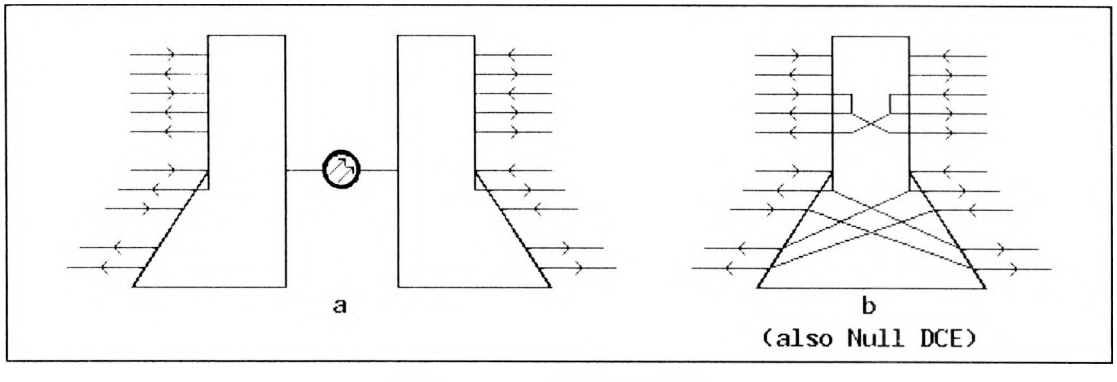

Figure 7. DCE Pair Symbols

C. DTE/DCE Interfacing

The following example will illustrate the way in which DTEs interface to DCEs. Consider the simple computer-to-computer link over one pair of modems in Figure 8.

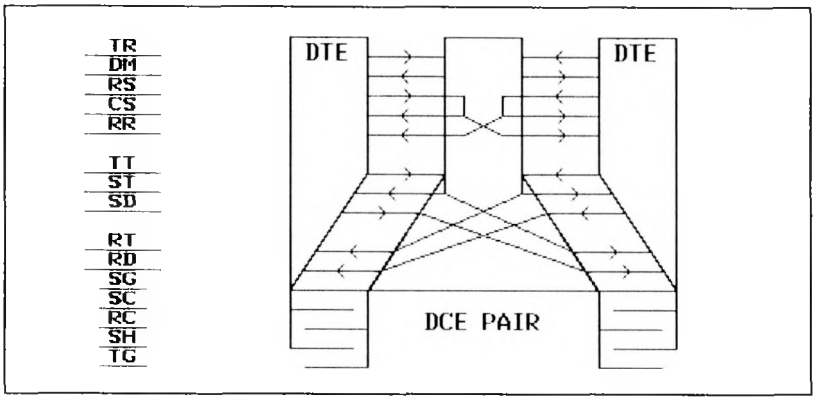

Figure 8. Computer-to-Computer Example

The computers are represented by the DTE symbols at the ends and the modem pair is represented by the DCE Pair symbol in the middle. The DTE/DCE interfacing is correct since the symbol edges match up. Clock, data, and control lines are drawn in to show the signal flow and crossovers. Note that SD on one end becomes RD on the other, and vice versa. It is necessary that modem pairs perform this crossover of data signals in order to conform to the DTE/DCE definitions. The control signal crossovers shown are typical.

Frame ground (FG), also called "Green Wire Ground", is connected to SG at each DTE or DCE via a 1/2 watt, 100 ohm resistor. The purpose of FG is to bleed off potentially dangerous currents which may develop within the equipment or which may be conducted onto the equipment frame. The 100 ohm resistor attenuates loop currents which may arise from the ground loop formed by SG and FG interaction. This resistor may be shorted if the ground loop can be tolerated. FG is not normally shown on these design drawings.

Up to five ground and common signals may be provided on these drawings for purposes of signalling, references, and shielding. Signal Ground (SG), drawn at the base of the DTE/DCE symbol, provides a common voltage reference between adjacent equipment. Send Common (SC), drawn below SG, connects to SG only at the DTE to sink signalling currents back to the DTE from receivers in the DCE. Receive Common (RC), drawn below SC, connects to SG only at the DCE to sink signalling currents back to the DCE from receivers in the DTE. Shield (SH), is typically connected from the DTE's FG to a braided shield conductor in the cable between the DTE and DCE. SH is left open at the DCE end to prevent ground loops. The purpose of SH is to keep external electromagnetic fields from inducing noise on the cable conductors (to keep unwanted signals out). Tempest Ground (TG), drawn below SH, is used to keep desired signals within the cable from emanating out to eavesdropping receivers (placed by unauthorized persons to intercept sensitive data). TG is left open at one cable end to prevent ground loops and sinks current to a single ground reference in as direct a manner as possible (usually to the building counterpoise ground point).

These ground and common signal, though important, will be omitted from most of the drawings in this paper in order to focus on the interaction of the other signals.

If the circuit is more complex, eg., two modem pair links, the drawing might appear as shown in Figure 9. Since a DTE and a DCE must match up, a DTE Pair (or null DTE) is needed between the two modem pairs for correct signal flow. The null DTE crosses the signals over for the two opposing modems since RD out of one modem must become SD into the other.

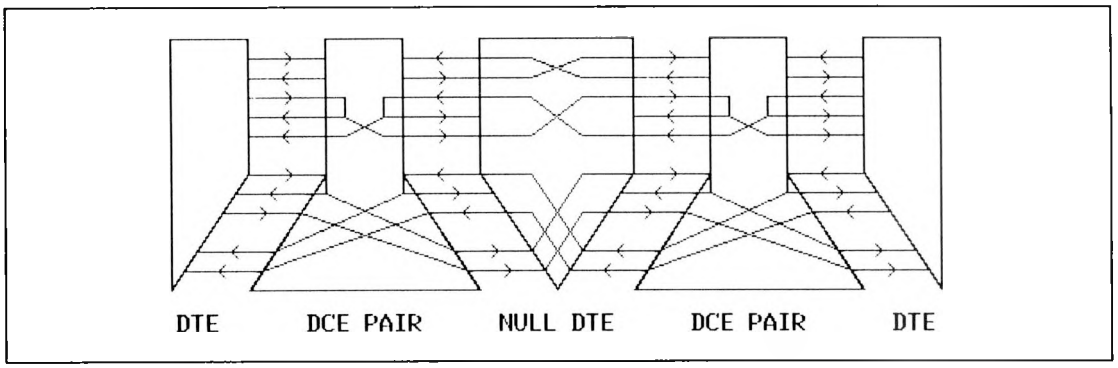

Figure 9. Multi-Segment Circuit Example

D. Multiplexers

Multiplexers are communication devices that take one or more data circuit inputs, concentrate them onto one aggregate communication line, and then split them back into individual data circuits at the other end. This is done to combine many low speed circuits and transmit them on one high speed link. Economic and diagnostic benefits result. However, single-point-of-failure considerations become important.

The input side of the multiplexer is typically composed of DCE interfaces. Each individual data circuit (DTE interface) sees a DCE just as it would if it were using an individual modem to transmit its data. The aggregate output of the multiplexer is a DTE interface since it must talk to the DCE interface of the high speed modem into which it will transmit multiplexed data.

A multiplexer symbol is drawn using single DTE and DCE symbols with an intervening rectangle to represent internal function. Two of these symbols appear in Figure 10. The symbol can be drawn right or left; depending on which end of the circuit you are drawing.

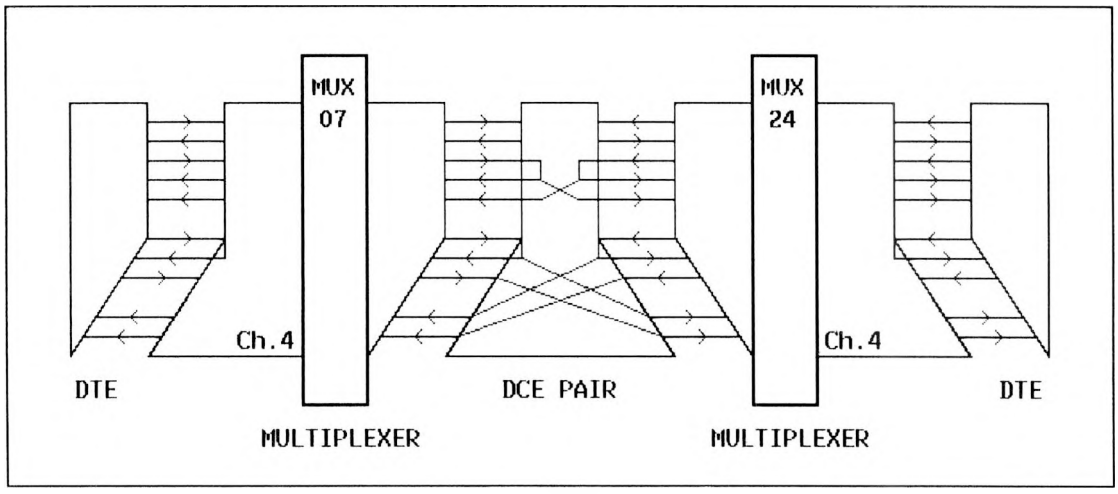

Figure 10. Multiplexer Symbols

Notice that even though a multiplexer may take many data circuit inputs, only one is shown. Extra inputs may be shown for effect but are not required if the symbol is understood by the designer. The intervening rectangle, with one DCE and one DTE, is usually enough to depict a multiplexer. On a multi-circuit drawing, a multiplexer may be drawn along with all input data channels.

It is good practice to note multiplexer information in the rectangle or input DCE. This information might include multiplexer identification, input channel number, line speed, etc.

E. Protocol Converters and Encryption Devices

Often in data communication circuits, physical and logical link protocols need to be converted from one form to another. Protocol converters are designed to perform this function. Logical link protocol converters change the data format and physical link protocol converters change the electrical and physical characteristics of the interface. Neither converter, however, alters the type of interface: type being DTE or DCE.

In order to keep the interface type the same, a protocol converter must have a DTE interface on one side and a DCE interface on the other. For example, SD out of a DTE enters the converter's DCE interface (as it should), is operated on by the converter, and exits out of the converter's DTE interface. Although the data is now either in a different format or has different electrical characteristics, it still appears as originating from a DTE interface.

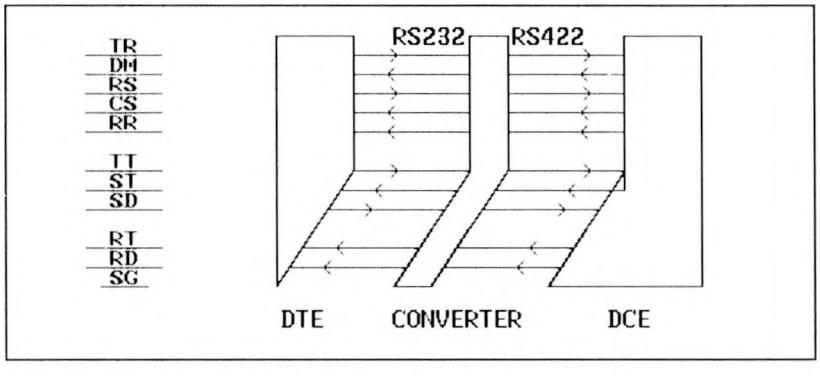

Figure 11. Protocol Converter Symbols

Figure 11 shows a computer (DTE) interfacing to a modem (DCE) with a protocol converter inserted between. Since the converter has one DTE and one DCE interface, it fits between the computer and modem without the need for null DTEs or null DCEs. This is a convenience designed into the converters. If, for instance, the computer had an RS232 interface and the only modems available were RS422, the converter in Figure 11 would be an RS232 DCE to RS422 DTE physical link protocol converter. Note that an RS232 DTE to RS422 DCE converter would not operate properly in Figure 11.

Encryption devices are much like protocol converters, in that, they modify the data stream without altering the interface type. In the case of encryption devices, though, not only is the data format changed, but the actual data bits are changed. This is done using an encryption algorithm.

Encryption devices operate in pairs: one to encrypt the data and another to decrypt the data. Figure 12 shows a circuit consisting of two computers (DTEs) communicating over a pair of modems (DCE Pair) with encryption devices inserted at each computer/modem interface. Since an encryptor has one DTE and one DCE interface, it can be inserted between a DTE and DCE without the need for null devices. The input/output on the DCE side of the encryptor is referred to as the plaintext and the input/output on the DTE side is referred to as the cyphertext.

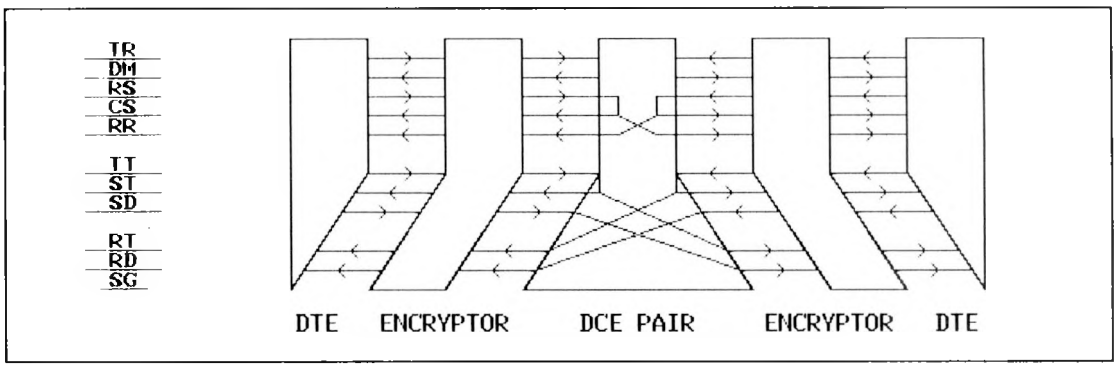

Figure 12. Encryptor Symbols

Following Figure 12 from left to right, SD leaves the DTE, going right, and enters the encryptor. The data is then encrypted and leaves the encryptor, still as SD. This data is then transmitted through the modem pair and emerges as RD. RD continues to the right, into the other encryptor. The data is decrypted and leaves the encryptor, still as RD. The DTE receives RD and the data transmission is complete. The same operation takes place for the data path in the other direction.

F. Switches and Patch Panels

Some circuits employ switches; either manual or electronic. Manual switches are used often during circuit test phases. This is done to allow various communication devices to be switched in and out of a circuit with ease. In test bed circuits, these switches usually become permanent. Electronic switches, or digital circuit switches, are common in asynchronous terminal applications. This type of switch allows a terminal user to access many computer resources. These switches are also used for computer-to-computer circuits when the circuit switch has the capacity to assign dedicated channels.

Figure 13 shows manual switches in a test bed circuit. The switch on the left is being used to switch the computer between two different kinds of modems. The switch on the right is used to switch the line from either modem into the remote computer. This circuit set up might be used to test the quality of various pairs of modems by manually switching each pair into the circuit and comparing circuit performance. Manual switches are also used to switch vital production circuits between redundant communication channels. This is done to allow a ready backup channel to be switched in should the main channel fail.

In Figure 13, only a single switch element is depicted (RD on the left switch). This switching function occurs for each signal (except possibly for SG which may be connected in common to all switch interfaces), but is not explicitly drawn to reduce the clutter and complexity of the diagram.

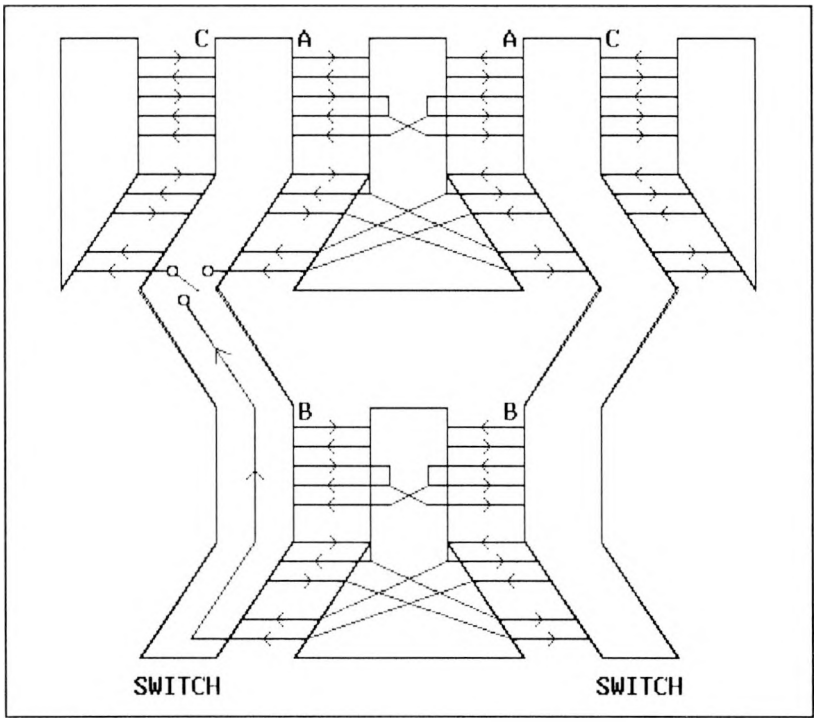

Figure 13. Manual Switch Symbols

Figure 14 shows a simple terminal connected through an electronic switch channel to a remote computer. Since many computer resources might be available to the terminal, it would be impractical to show all possible connections (hundreds or thousands in modern data PBX switches). The switch is drawn with a single channel since only the active connection, or most common connection, needs to be shown. The intervening rectangle represents the internal function of the switch, and the two DCEs represent the modems used to connect to the switch.

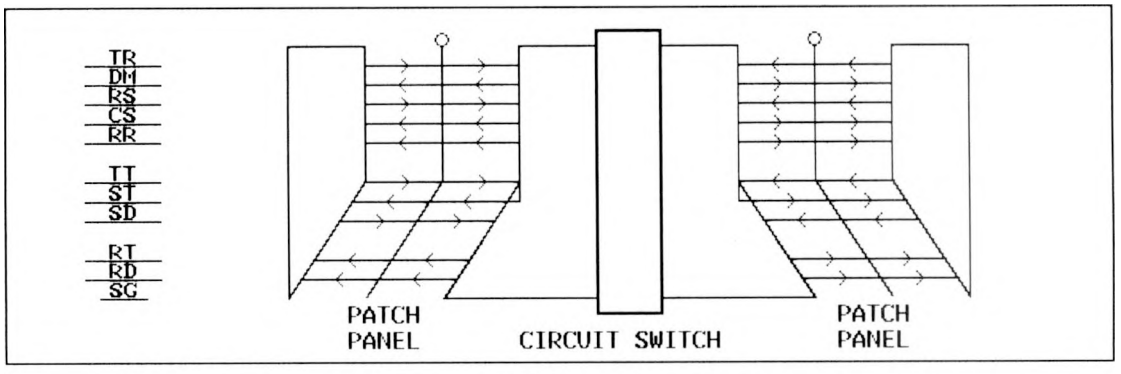

Figure 14. Circuit Switch and Patch Panel Symbols

Patch panels are used in circuits to allow troubleshooters easy access to the digital communication line. The line passes through the patch panel where it can be monitored and/or interrupted. The monitor function taps the digital signals off of a "T" connection and usually provides indicator lights for the more common signals. Connectors and patch cords allow the troubleshooter to patch, or switch, circuit components around during circuit testing.

Figure 14 also shows patch panels at each computer/modem interface. Since many circuits usually come through a single patch panel, the troubleshooter can check the digital signals of different circuits (with the indicator lights) at the same physical location.

G. Analog-Side Symbols (Communications Media)

Analog communication design, for the purpose of this report, involves the media over which modems, multiplexers, and other DCE Pairs exchange data. This includes the layout of cable plants and line termination. Since this paper deals with the digital design aspect of communications, analog design methodology will not be covered.

Since different troubleshooting techniques are employed, depending on the media used, the designer should indicate the type of media. Optical fibers are not treated the same as twisted pair. Satellite channels are not treated the same as terrestrial lines. Figure 15 shows various media, including the optical fiber symbol and the satellite/earth station symbol. The standard DCE Pair symbol, with media noted, can be used for expediency.

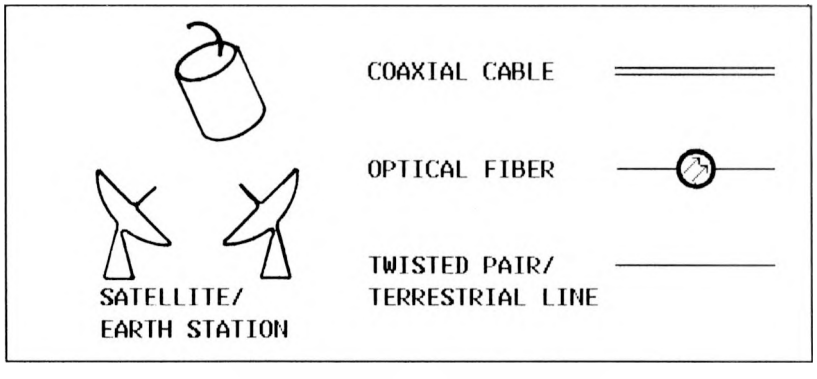

Figure 15. Analog-Side Symbols

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IV. Other Communication Symbols

Due to the increasing use of DS-1 (or T1) communications and Local Area Networks (LANs) at Sandia National Laboratories, two additional sets of symbols were recently developed. These symbols, like the standard digital set, have polygon shapes and assignment of signal line positions to assist the designer.

In this chapter it is assumed that the reader is familiar with the theory of operation and terminology of DS-1 and LANs. It is suggested that the uninitiated reader refer to AT&T publications for further information on the DS-1 Standard and to IEEE publications for further information on the 802.3/Ethernet Standard.

A. DS-1 Standard Symbols

Although not totally synonymous, the terms DS-1 and T1 will be used interchangeably throughout this section.

To keep the symbol set relatively simple, a DTE/DCE (two types of interfaces) approach is used. Although T1 interfaces are not referred to as DTEs or DCEs, two distinct types exist. The first type of interface transmits on signal pair 1 and 9 and receives on pair 3 and 11. The second type transmits on pair 3 and 11 and receives on pair 1 and 9. Since these two types interface to each other, the first type is drawn similar to a DTE shape and the second to a DCE shape. Figure 16 shows the left and right "DTE" and the left and right "DCE". Also shown is the signal convention. The small triangles indicate clock generation activity.)

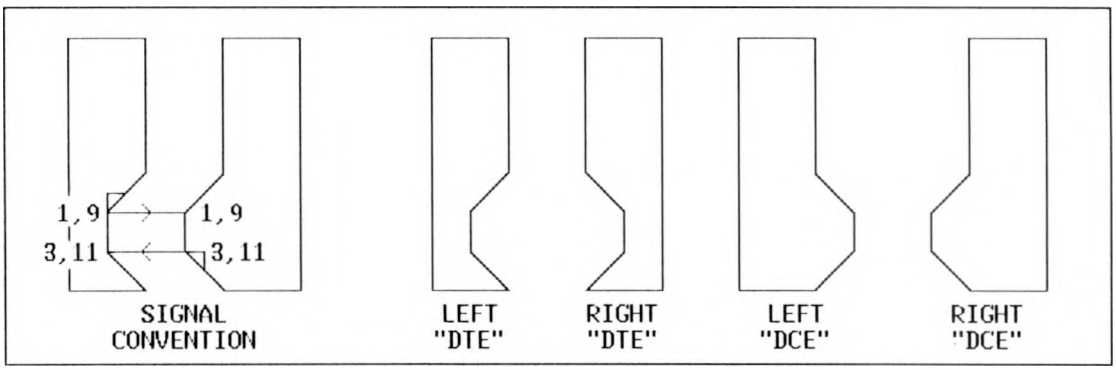


Figure 16. Basic DS-1 Symbols

Unlike standard digital communication, end equipment (data sources or sinks) is not necessarily of the first interface type and transmission equipment is not necessarily of the second interface type. As a result, drawings will not always have the familiar DTE shapes on the ends and DCE shapes in the middle.

Devices found in the circuit path, such as modems and multiplexers, may have one or both types of interfaces. Which lines a particular side of the device transmits on is at the discretion of the equipment manufacturer. Therefore, as in standard digital communications, a null type device may be necessary to allow correct signalling. Figure 17 shows what a T1 circuit might look like.

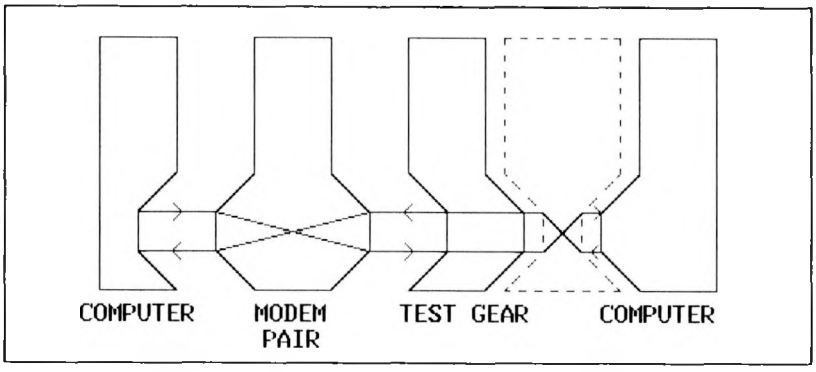


Figure 17. DS-1 Circuit Example

The signalling structure of T1 is a simple one. Since only one pair of lines is used to transmit and only one pair to receive, the signalling can be represented with only two lines on the drawing; TX (Transmit) and RX (Receive). As such, null devices are now reduced to simple wire crossovers. This is shown in Figure 17. Since the right and second-from-right devices both transmit on lines 3 and 11, a simple wire crossover is used as a null device to allow the interfaces to communicate.

Various T1 operating parameters can be indicated in and around the symbols. The left side of Figure 18 shows a key for displaying this data. The options for speed are 1.544, 1.536, and 1.344 Mbps; the options for framing are D4, ESF, and none; and the options for data coding are AMI and B8ZS. (Changes in T1 communication in the future will modify these parameter options.) Since the devices in a circuit must have the same operating parameters to communicate properly, the speed, framing, and coding need only be shown on one device. This is done in Figure 18.

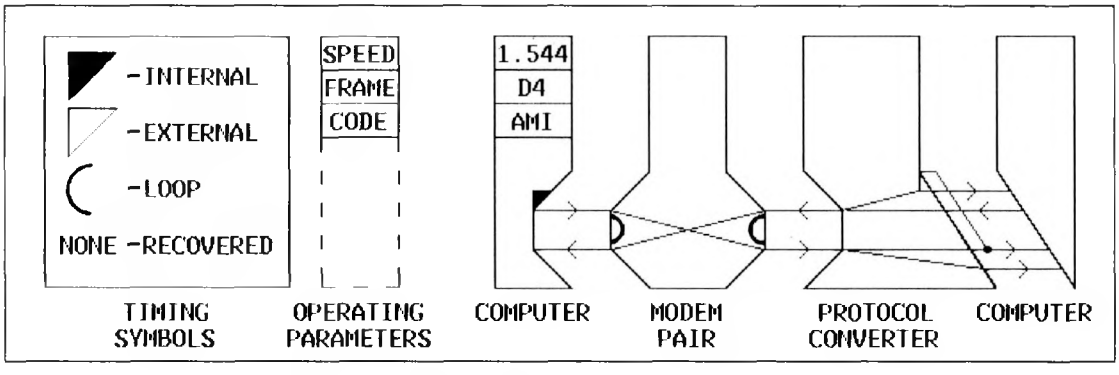


Figure 18. DS-1 Timing and Operating Parameters

As is often the case, communication circuits have some DS-1 components and some standard digital components. This arises because modems, multiplexers, and physical link protocol converters with both kinds of interfaces are used in a circuit. A multiplexer, for example, might take 24 independent 64 Kbps channels on RS422 interfaces and combine them onto one T1 aggregate output channel. Symbols for these devices are created by using parts of symbols from both templates. One such device, a protocol converter, appears in Figure 18.

The timing out of a T1 device can be derived from four sources: internal oscillator, external reference, input timing (loop), and recovered from the incoming signal from the other modem (remote recovered). In Figure 18, the left computer is used to master time (internal) the whole circuit. The modem pair uses loop timing at each modem in order to talk to the computer and the protocol converter. Although loop timing at each modem interface would seem to cause errors due to phase differences, this does not occur in modems that internally buffer the data. These modems can also be operated in remote recovered mode if so desired. The T1 interface of the protocol converter transmits based on recovered timing from the RS422 side of the converter. As a result, one clock frequency is used throughout the circuit. The timing key appears on the left side of Figure 18.

B. Local Area Network Symbols

Although these symbols can be used for various LAN topologies, they were developed while primarily using Ethernet (or IEEE 802.3) LANs.

These symbols are similar to the standard digital symbols insofar as having two distinctive interface types. Ethernet terminals (data sources and sinks) are called Data Terminal Equipment (DTEs) and transmission devices are called Medium Attachment Units (MAUs). MAUs are usually referred to as transceivers. The cables that connect the two types of interfaces are called Attachment Unit Interfaces (AUIs), or simply, transceiver cables.

Unlike the standard digital symbols, the shape of these symbols only distinguishes the device type; eg., terminal, transceiver, repeater, or bridge. The shapes do not indicate how the devices interface to each other. Instead, triangles, or arrows, appear inside the device to depict a DTE or an MAU.

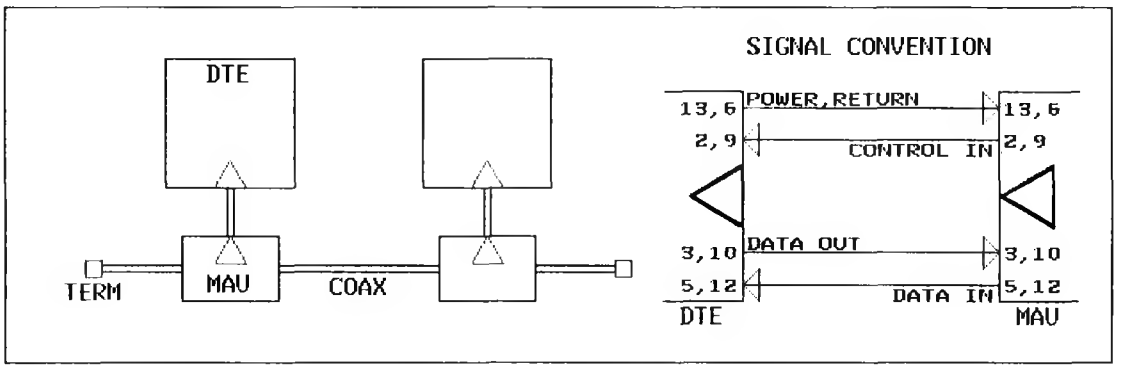


Figure 19. Basic Ethernet (LAN) Symbols

Figure 19 shows a simple LAN with two DTEs connected to a common coaxial cable via two transceivers. The DTE squares have triangles pointing in (to represent female connectors). The transceivers have triangles pointing out (to represent male connectors). Transceiver cables connect the DTEs to the MAUs. The MAUs are shown with the coaxial cable running through them. (The MAUs act as taps on the line.) The small squares on either end of the coax are terminators to provide impedance matching on the cable. The right side of Figure 19 shows the signal convention key. The number pairs are connector pin assignments.

In the case of optical fiber Ethernet cable (instead of coax), the MAU is drawn with an optical fiber line attached to it instead of a coaxial cable running through it.

Figure 20 is a drawing of an Ethernet LAN including various components. The DELNI is a Digital Equipment Corporation device that simulates an Ethernet LAN for eight local terminals.

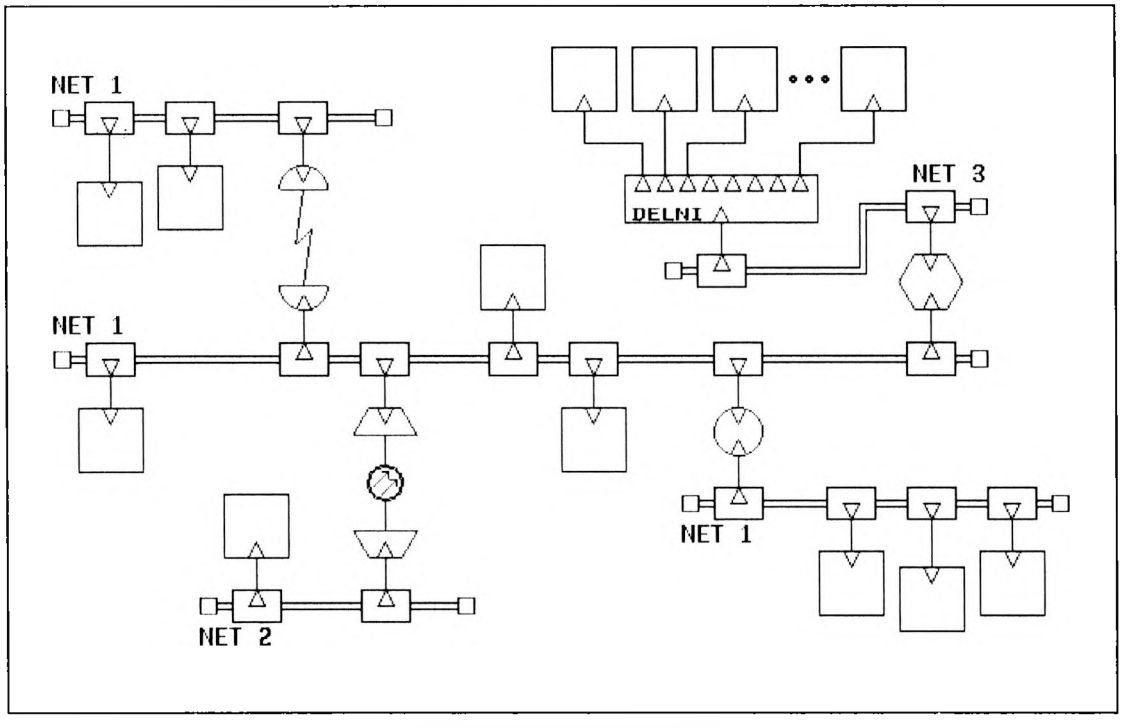


Figure 20. Ethernet Networks

All terminals on the same coax can communicate with each other as well as with those coax cables connected to it through repeaters. While a repeater simply extends a LAN to two or more coaxial cables, a bridge buffers and re-times the transmissions from one Ethernet segment to another, allowing interconnection of short sections over great distances.

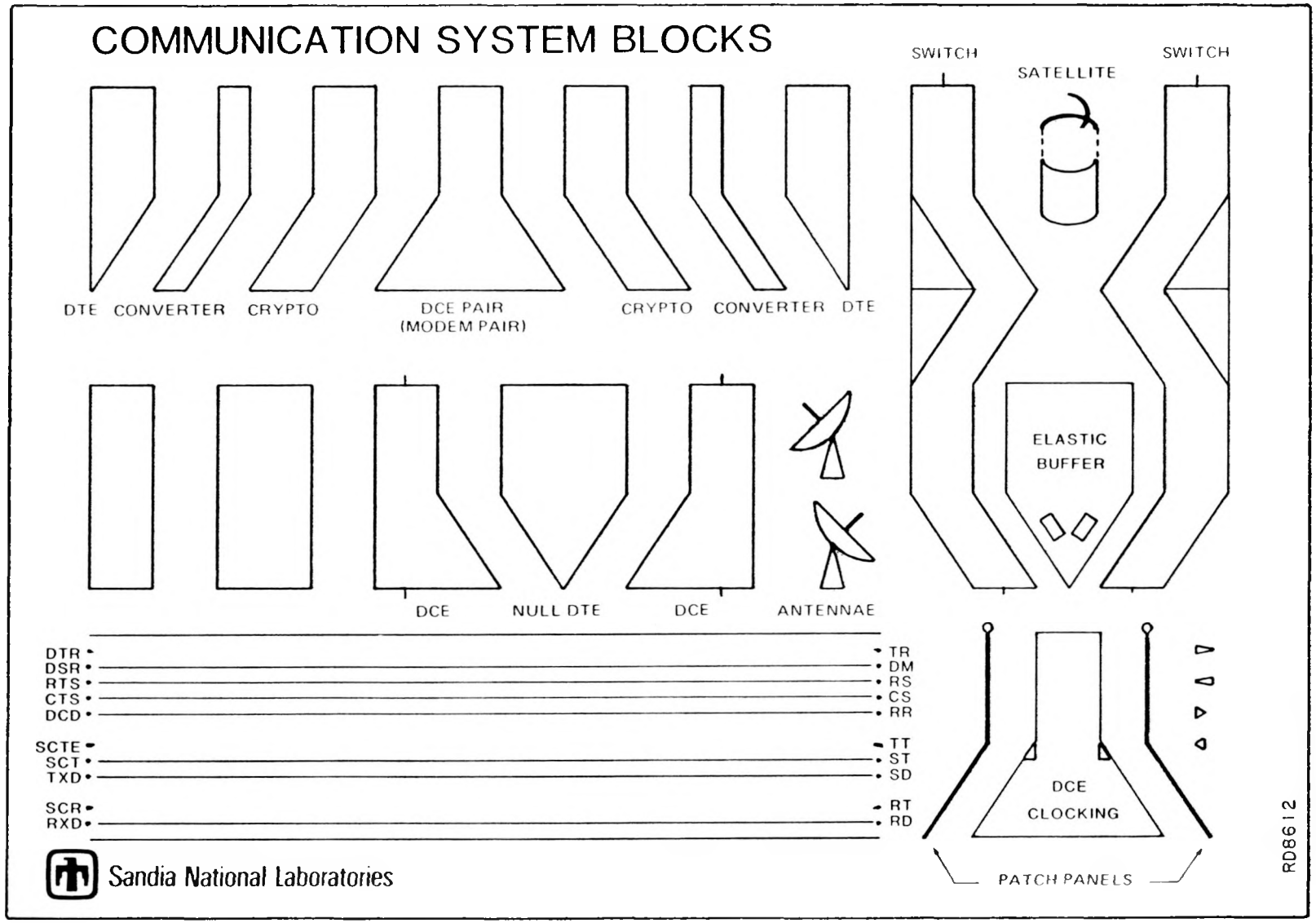
The half repeaters and half bridges are separated by either wire or optical fiber to allow greater distance between LANs. The optical fibers also provide greater data security and noise immunity.

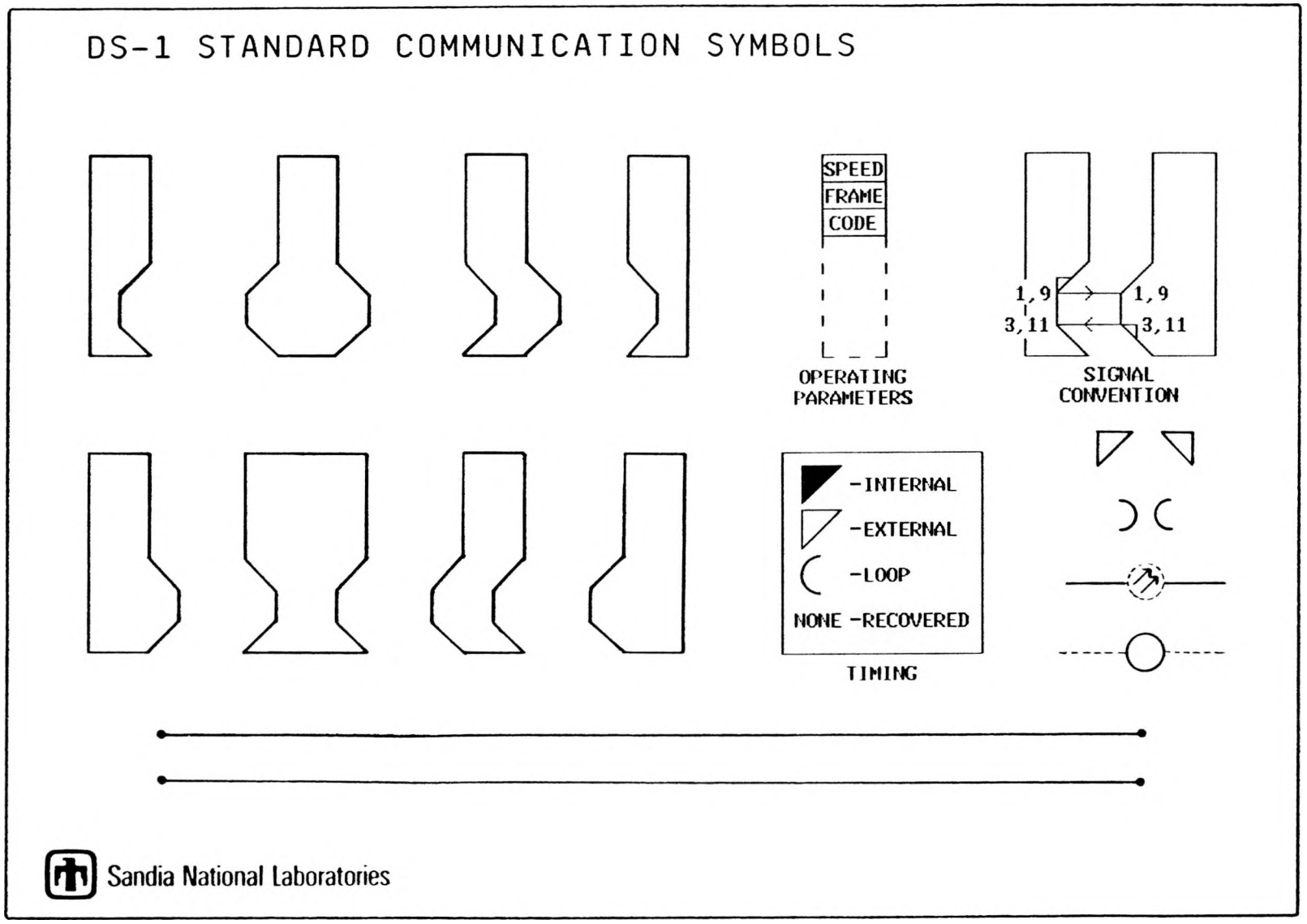
V. Symbol Templates

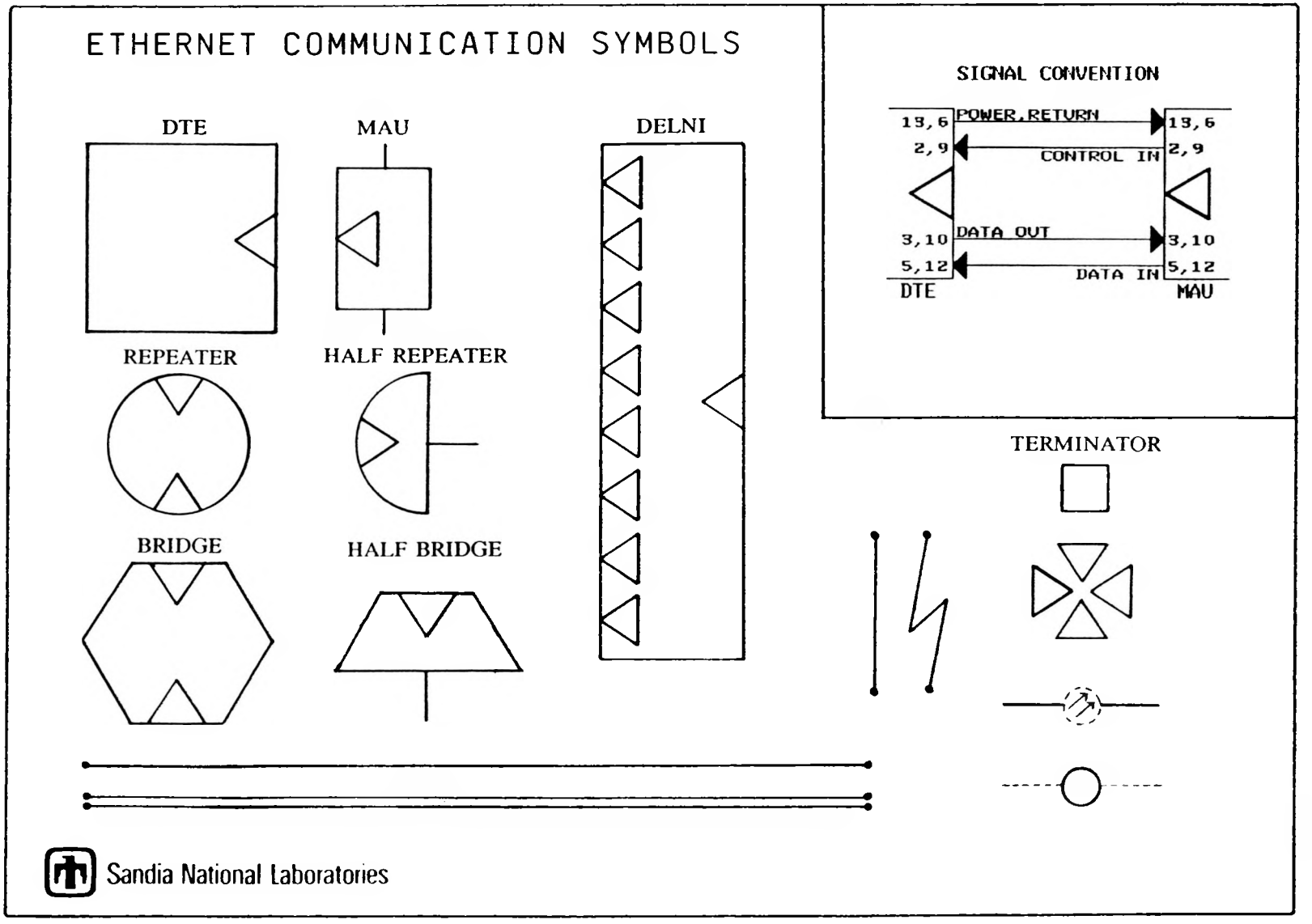
On the following three pages are the templates for the three sets of communication symbols now in use.

Refer to Chapter III for individual standard digital symbol dimensions and details. Refer to Chapter IV for general DS-1 and LAN symbol design.

The DS-1 Standard and Local Area Network templates have not been mass produced at the time of this writing. As such, the design of these symbols may change at any time.


COMMUNICATION SYSTEM BLOCKS
SWITCH
SATELLITE
SWITCH
DTE
CONVERTER
CRYPTO
DCE PAIR
(MODEM PAIR)
CRYPTO
CONVERTER
DTE
ELASTIC
BUFFER
DCE
NULL DTE
DCE
ANTENNAE
DTR
DSR
RTS
CTS
DCD
SCTE
SCT
TXD
SCR
RXD
TR
DM
RS
CS
RR
TT
ST
SD
RT
RD
DCE
CLOCKING
PATCH PANELS
Sandia National Laboratories
RD8612


DS-1 STANDARD COMMUNICATION SYMBOLS
SPEED
FRAME
CODE
OPERATING
PARAMETERS
1, 9
3, 11
1, 9
3, 11
SIGNAL
CONVENTION
-INTERNAL
-EXTERNAL
-LOOP
NONE -RECOVERED
TIMING
Sandia National Laboratories


ETHERNET COMMUNICATION SYMBOLS
DTE
MAU
DELNI
REPEATER
HALF REPEATER
BRIDGE
HALF BRIDGE
SIGNAL CONVENTION
13,6
POWER,RETURN
13,6
2,9
CONTROL IN
2,9
3,10
DATA OUT
3,10
5,12
DATA IN
5,12
DTE
MAU
TERMINATOR
Sandia National Laboratories

VI. Multi-Segment Communication Circuits, A Primer

A. Introduction

There are three basic clocking modes that modems use; asynchronous, isochronous, and synchronous.

Asynchronous communication does not use clocks sent along in synchronism with the data. Instead, when data is ready at the DTE, it is simply sent to the modem; not waiting for clock transitions (an implied clock is regenerated within each equipment, synchronized to the start bit). This data is preceded and trailed by start bits and stop bits respectively. The start bit signals the modem to prepare to sample the incoming data. When no data is being transmitted, the signal lines are at a DC level.

Isochronous communication is similar to asynchronous, in that, data is transmitted from the DTE in an asynchronous fashion. The modem, on the other hand, does not wait for a start bit. Instead, the modem samples incoming data at approximately four times the expected asynchronous speed. In effect, for every four bits that the modem transmits, one bit of asynchronous data is represented.

In synchronous communication, the DTE will wait for a rising ST clock edge from the modem before placing valid data on the SD data line. The data, in turn, is clocked into the modem with the falling edge of the very same ST clock. In this way, rising clock edges and data transitions are propagated through the circuit in synchronism. SD, clocked into the modem with ST, is sent to the remote modem and appears as RD data with the RT clock. RT is then used to clock RD into the remote DTE. The remote DTE samples RD on the falling edge of RT.

Although asynchronous and isochronous communication are widely used, they will not be discussed further. The remainder of this report will deal exclusively with synchronous communication.

B. Modem Clocking Modes

A modem in a modem pair will use one of three clocking modes; internal (master), external, or slave. These clocking modes are usually switch selectable options on modems. Before discussing the individual modes themselves, a few words about signal paths is in order.

A modem normally sends out a clock signal on the ST pin to clock data in on the SD pin. This clock is also sent along with the clocked in SD to the remote modem where they appear on the RT pin and RD pin, respectively. This represents one data path of the communication circuit. The other path, originating at the remote modem, uses the clock on its ST pin to clock in data on its SD pin and sends them both back to the local modem where they appear on the RT pin and RD pin, respectively.

Internal timing is used when the modem is chosen as the master clock source for a synchronous circuit. One modem must be the master clock source unless a common carrier (with its own master clock) is part of the circuit. Two master clocks (one for each path) may be used in the same circuit providing that intervening equipment allows it. Errors associated with multiple master clocks are covered in Section E. Internal timing is generated in the modem using a crystal oscillator. This clock is used as ST on the local modem and propagated to the remote modem as RT. The symbol of such a modem shows a solid TT/ST triangle and no Terminal Timing (TT) signal as shown in Figure 21a.

External timing is used when either the master clock from another modem pair or from a DTE must be used to clock the circuit. Most modems accept an input clock on their TT input and use it to generate ST on the local modem as well as RT on the remote modem. Some modems, however, do not generate ST from TT. They simply use TT to clock SD in and pass them both to the remote modem as RD and RT. ST is left free running (at the modem's crystal frequency). The symbol for the external clocking mode in Figure 21b. shows an open TT/ST triangle with a TT signal line presented to the modem.

Slave timing is similar to external timing, in that, the generated clock is slaved to some other clock. Slave timing is usually used by one modem when the other in the pair is using internal or external timing. The RT clock, sent by the other modem in the pair, is recovered out of the analog signal between the two modems. This clock is then used by the modem to generate ST locally. As before, this ST is used to clock in SD from the DTE and both signals are sent to the remote modem where they appear as RT and RD. The symbol for this clocking mode in Figure 21c. shows an open TT/ST triangle, no external TT signal line, and a line connection from RT to TT (to represent the internal clock recovery of this mode).

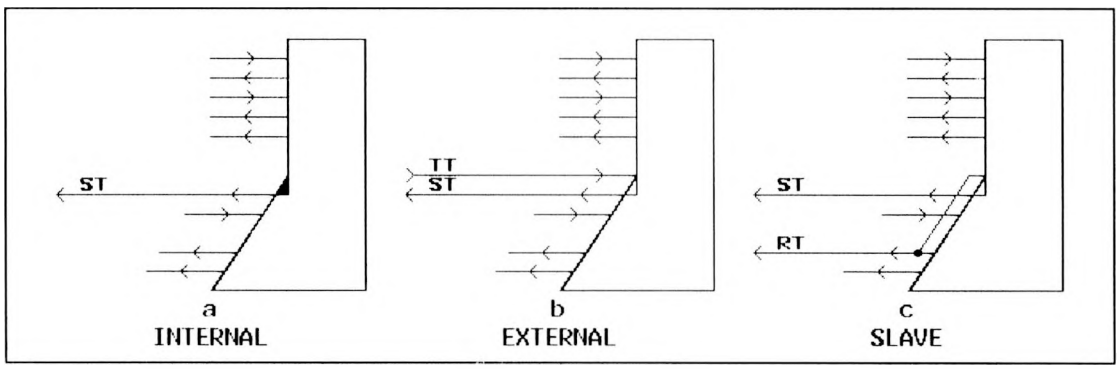


Figure 21. Synchronous Clocking Modes

The clocking mode example in Figure 22, shows a modem pair between two DTEs. One modem is using internal clock mode and the other modem is using slave mode. Note the crossover of clock and data signals through the modem pair. In this configuration, one modem provides the clocking for the entire circuit.

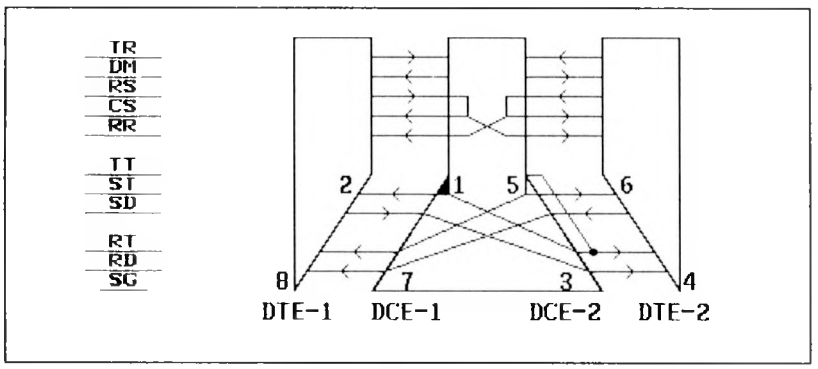


Figure 22. Clocking Mode Example

The clock and data flow begins with the internal clock (ST) generated at point 1. ST from DCE-1 causes SD to be clocked out (on the rising edge of ST) of DTE-1 at point 2. The falling edge of ST at point 1 is then used to clock SD into DCE-1. (Note that a potential clocking error exists at point 1, depending on the cable distance between point 2 and point 1 and on the clock frequency.) ST and SD are propagated through to DCE-2 and appear as RT and RD at point 3. DCE-2 presents RD at point 3 with the rising edge of RT. On DTE-2, at point 4, the falling edge of RT is used to clock in RD. This completes one path of the communications circuit. Since DCE-2 is in slave mode, its ST is generated by recovering RT. To follow the communications path in the other direction, understand that points 5, 6, 7, and 8 represent the same operations as points 1, 2, 3, and 4.

The five examples in Figure 23 show the various combinations of clocking modes. Note that slave/slave is not an option since the circuit must have at least one master clock source. External clocking of a DCE implies that the DTE provides a valid clock on its TT line, although this is not always the case.

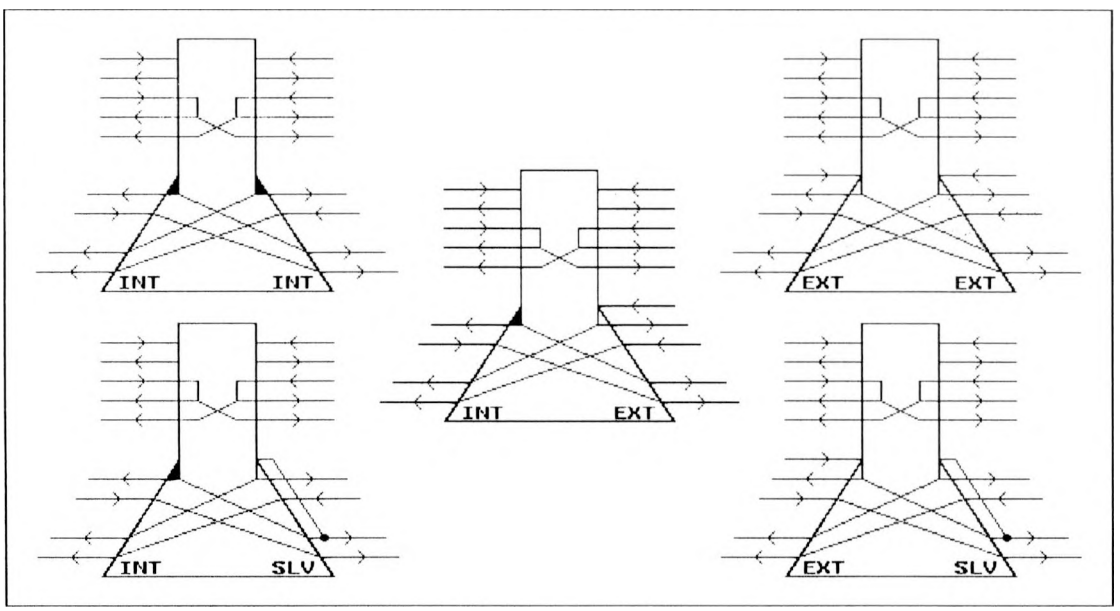


Figure 23. Clocking Mode Combinations

C. Control Signals

In Figure 23, the control signals can be seen to crossover as well as the data and clock signals. A brief explanation of control signals is now in order.

The communications symbols can depict five major control signals used in digital communications. Some, but not all, DTEs and DCEs use these control signals in the manner to be discussed below.

TR,	Terminal Ready	: From DTE to declare operational status to DCE
DM,	Data Mode	: From DCE to declare operational status to DTE
RS,	Request To Send	: From DTE to indicate it is ready to transmit data
CS,	Clear To Send	: From DCE to indicate it is ready to receive data
RR,	Receiver Ready	: From DCE to indicate connectivity to its remote modem

When power is applied to the DTE and DCE devices, TR and DM are usually asserted and remain so. Many devices require this condition before communications can proceed. When the DTE wants to transmit data, it asserts RS. In response, the DCE asserts CS to indicate that is is ready to accept data for transmission. As is often the case, the DCE also asserts RR to indicate that its remote modem is sending an analog carrier, of some sort, which indicates that the remote modem detects RS from the remote DTE. Thus, the presence of CS and RR at the local DCE indicates to the local DTE that a complete and valid communications path exists to the remote DTE. These control signals present on the remote DCE also indicate to the remote DTE that a complete and valid communications path exists back to the local DTE.

Some equipment does not always support this type of control signal handshaking. In this case, control signals are usually ignored at the noncompliant equipment and looped back at the compliant equipment. Loopback is used to "fake" handshaking. For example, if a DCE does not support control signals, they are "faked out" at the DTE. DM and RR are tied high to TR, and CS is tied high to RS. Whenever the DTE wishes to transmit data, it always appears as if the DCEs are ready. The loopback can be accomplished by using a breakout box at each DTE as shown in Figure 24.

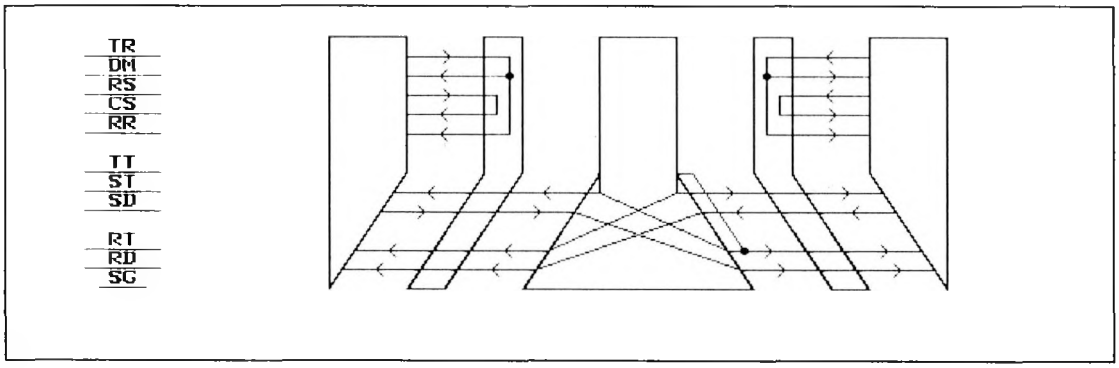


Figure 24. Control Signal Loopbacks

When a null DCE (null modem) is used between two DTEs, the control signals can either be looped back for each DTE or crossed over so that each DTE provides the control signals for the other. If signal indicators are present on the local equipment, the crossover method will allow the local equipment to display the control status of the remote DTE. Examples of both methods are depicted in Figure 25.

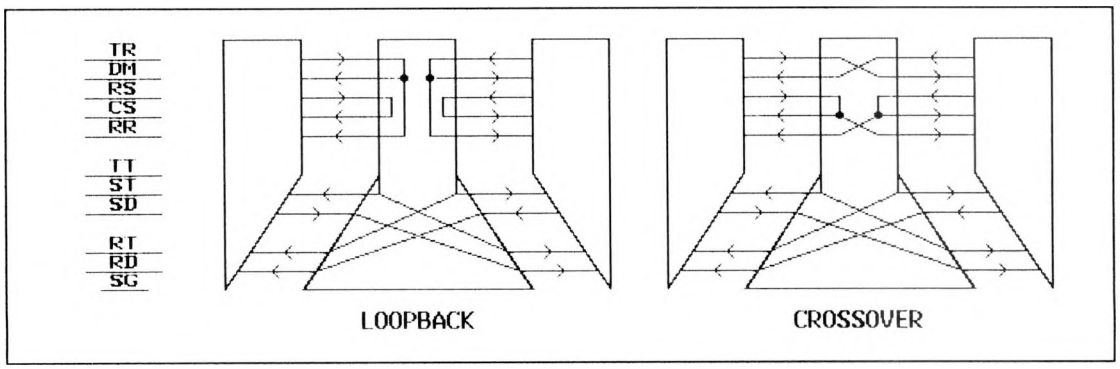


Figure 25. Null DCE Control Signals

D. CONSTANT PHASE ERRORS

In a circuit being clocked with one master clock (master/slave modem operation), it is possible to have a condition at one of the interfaces called constant phase error. This condition frequently occurs in multi-segment circuits. Consider the example circuit in Figure 26.

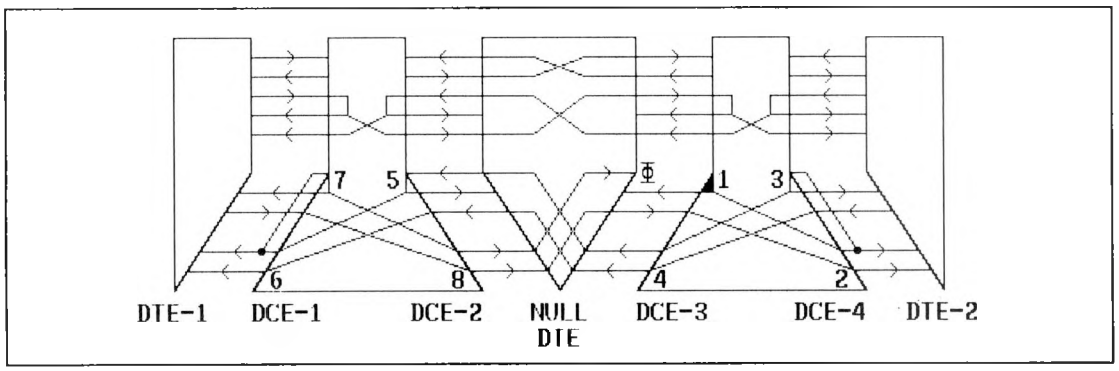


Figure 26. Constant Phase Error at Null DTE

As mentioned previously, the null DTE in the middle of Figure 26 is necessary to perform the signal crossovers to allow the two inside modems to communicate. The internal clock of DCE-3, at point 1, is propagated to its remote modem, DCE-4, as RT (point 2). Since the remote DCE is in slave mode, this RT is used to generate ST at point 3. ST clocks SD out of DTE-2, propagates to point 4 as RT (with RD), and is crossed over to externally clock DCE-2 as TT, at point 5. Here, TT is used by DCE-2 to generate its ST. RD from point 4 is also crossed over to become SD at point 5. Since DCE-2 ST in in phase with TT (and with SD), valid data will always be clocked in at this point. From here, ST and SD are propagated to DCE-1 as RT and RD at point 6 and clocked into DTE-1. This completes the left-to-right path.

Since DCE-1 is also in slave mode, RT at point 6 is used to generate ST at point 7. ST clocks in SD from DTE-1 and they propagate to DCE-2 as RT and RD; point 8. As in the other path, the null DTE crosses over RT and RD as TT and SD, respectively. Here, at point 1, TT can not be used to externally clock DCE-3 because DCE-3 is using internal timing. TT is simply ignored. Even though TT is the same frequency as ST on DCE-3 (since TT, through a long chain, actually originated from this modem), it is possible that they are out of phase with one another. This phase difference is due to propagation delay, both in the equipment and in the communications media. Figure 27 shows SD in phase with (being set up by) TT. If the DCE-3 ST clock is 180 degrees out of phase with TT, DCE-3 will always try to sample data when it is invalid (in transition).

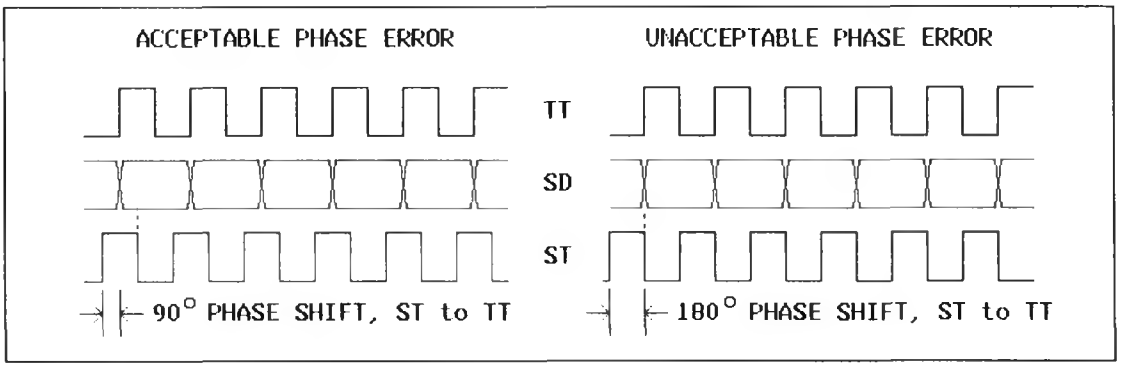


Figure 27. Phase Error Waveforms

Since both clocks are the same frequency and the propagation path is constant, this phase error should also remain constant (subject to clock regeneration jitter). To correct the constant phase error condition, the path length can be changed (to change the propagation delay and thus the phase error). If the phase error can be made to fall out of the 150-to-210 degree range, clocking errors should not occur. The closer the phase error is to 180 degrees, the greater the chance of clocking data errors.

In the event that changing the length of the signal path (propagation delay) is not practical, a buffering scheme must be used. By inserting a null DTE fifo in place of the passive null DTE, this buffering can be achieved. The null DTE fifo symbol is discussed in Chapter III. The previous multi-segment circuit in Figure 26 is redrawn in Figure 28 with a null DTE fifo in place of the Null DTE.

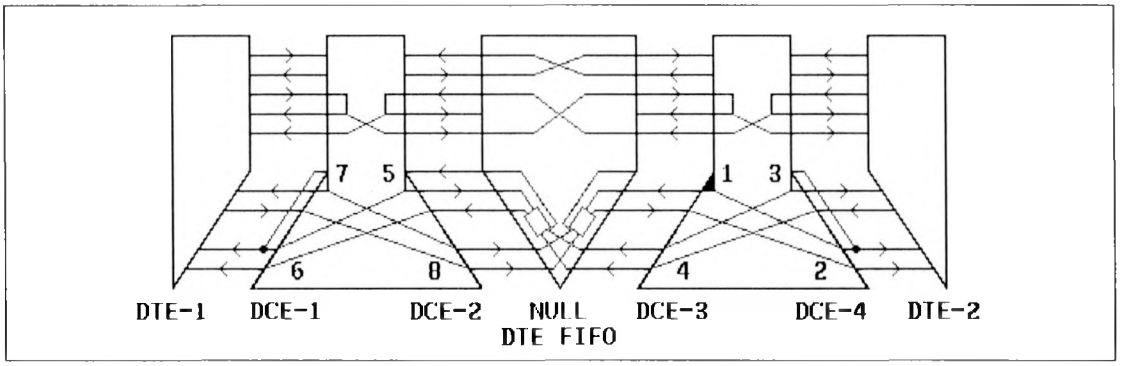


Figure 28. Null DTE Fifo in Circuit

E. Phase Drift (Frequency Error)

Multiple clocks can be used in simple communications circuits. Such a circuit might be one modem pair between two computers. If each computer (DTE) provides its own output clock on the TT line to externally clock each modem (DCE), or if each modem is using its own independent internal clock, the two transmission paths are independent of each other. Since the two clocks are likely to be of slightly different frequencies, each DTE will receive and transmit data at slightly different frequencies. Some DTEs are unable to handle this difference, and as a result, will not operate over a multiple clock circuit.

Examples of the circuit operation just described are given in Figure 29.

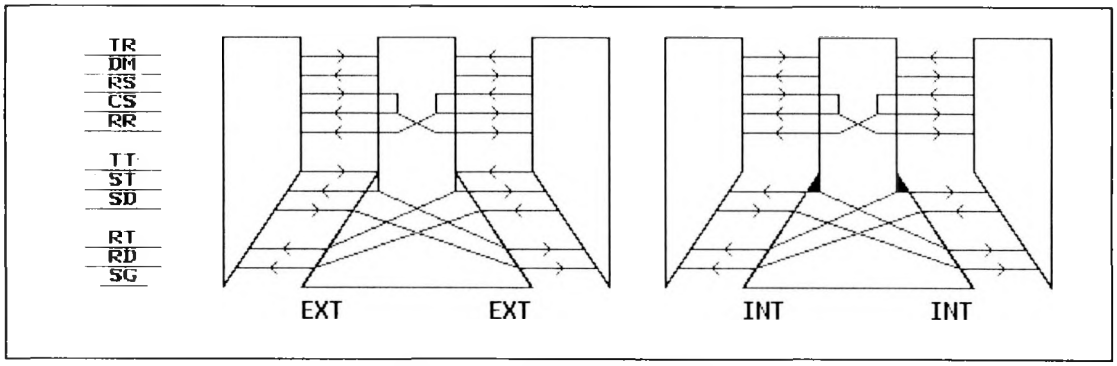


Figure 29. Multi-Clock Examples

If the DTEs will not operate over such a circuit, alternate clocking modes (like those discussed in the previous section) must be used. Running the modem pair as master/slave is the preferred choice.

An exception to this problem of multiple master clocks is when some form of common carrier is used; such as a commercial terrestrial line. In this case, each DCE is using internal timing. But since both DCE clocks are slaved from one common clock source, the matter of different clock frequencies does not apply.

A more serious problem exists in multi-segment communications circuits when the only choice is to use two master clocks in the circuit. Consider the following multi-segment circuit in Figure 30.

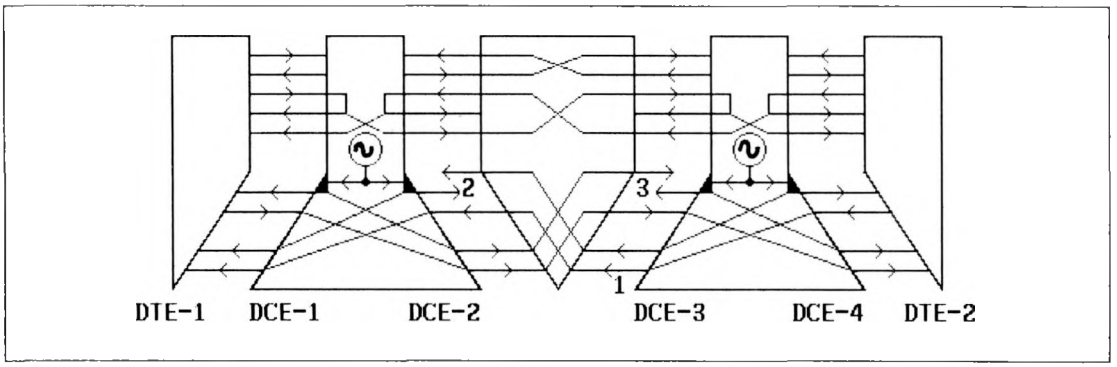


Figure 30. Multi-Segment Example

In this circuit, the DCE-1/DCE-2 pair represents a satellite channel. The DCE-3/DCE-4 pair represents a commercial terrestrial leased line. Both DCE Pairs will only operate with their own clocks. As can be seen, at point 1, RT and RD are crossed over by the null DTE to become TT and ST at point 2. Clocking problems occur at point 2 (and at point 3 on the other path) similar to the constant phase problems described in the last section. The problem here, however, is worse. Because the two frequencies, TT and ST, are different, the phase error between them is not constant. Therefore, some SD bits will be clocked into DCE-3 as valid and others as invalid. Additionally, since the two frequencies are different, some SD bits might be clocked into DCE-3 twice or not at all.

This problem can not be fixed by adjusting propagation delay because the phase error is not constant. To eliminate the problem, data bit buffering must be used (or the circuit must be redesigned to use a single clock source). The null DTE fifo discussed in the last section would only delay the inevitable double or missed clocking of SD bits. For frequencies differing by only a few Hertz on a high speed line, a buffer only two bits long would not be able to hold off errors for more than fraction of a second. A buffer for this type of circuit would have to be hundreds, if not thousands, of bits long to hold off clocking errors. Usually a long buffer will be designed to fill with data bits to the middle and then allow data to be clocked out. Depending on which clock (input or output) is faster, the buffer will either overflow or underflow. When this happens, the buffer will usually signal an alarm and then reset the buffer to half full and start over again. This scheme can be used to hold off data errors in a multiple master clock circuit for minutes, or even hours.

VII. General Circuit Design Using the Symbols

This chapter presumes that the reader is familiar with the material in Chapter IV, Multi-Segment Communication Circuits, and in particular, Section B., Modem Clocking Modes. Refer to Figure A2 in the Appendix during the following discussion. (Not all of the suggested equipment information appears in the drawing.)

A. Major Components

Position and draw major circuit components, listed below, and indicate circuit requirements at each symbol on the drawing.

1. End Equipment: Position at both sides of drawing. Indicate physical location (site/building/room/rack/bay) and nature of equipment (model number, logical unit reference, interface standard, data rate, etc.).

2. Fixed Location Equipment: Position between end equipment allowing space for possible intervening equipment such as modem links, encryptors, etc. Indicate physical location and nature of equipment (satellite earth station, common carrier demarcation points, encryption vaults, etc. and channel identification where applicable).

3. Encryption Equipment: If required, position units between end equipment in such a manner as to enclose the required encrypted portion of the circuit. Indicate physical location and nature of encryptors (DES, Government Supplied, or other and encryption mode if pertinent).

B. Modem Segments

Position and draw in modem segments required to span distances which cannot/will not be spanned by digital DTE/DCE interface cables. Make sure that the allowable signal attenuation (loss budget) is not exceeded by the distance, media, and modulation techniques intended to be used. Indicate physical location and nature of modem segments (model, optical or electrical interface, interface standards if both modems in the pair are not the same, control signal crossovers, etc.).

C. Null Devices

Position and draw in null devices required to fill gaps between major components and modem segments (not shown in Figure A2). The physical location need not be indicated as a null device is usually associated with an adjacent component. Control signal crossovers should be drawn in if nonstandard wiring is used.

D. Signal Paths

Trace signal paths between endpoints of circuit taking care to account for signal crossovers and loopbacks. Drawing the signal paths is not necessary, however, if null devices are properly located in the design drawing and detailed clocking information is not essential. At this point in the design process, the signal path is completely determined and can be deduced at any point on the drawing by examining the DTE/DCE symbol boundaries.

E. Clocking Modes

Use the following steps to determine and draw in correct circuit clocking.

1. Identify any special clocking requirements of the circuit components (such as common carriers which do not accept customer clocking, encryption units which pass clocks only from the cyphertext side to the plaintext side, etc.).

2. Identify the independent clock sources in the circuit.

3. Reduce the independent clock sources to a single clock source (resulting in simpler clocking modes and paths). Redundancy of clock sources may be considered, but introduction of only one clock source at a time is preferred.

4. Trace the clock distribution path through the circuit, looping clocks where required (especially at the cyphertext side of encryption equipment or at demarcation points of common carriers which do not accept customer clocking). Assure that each portion of the data signal paths are accompanied by a portion of the clock distribution paths.

5. Identify clock phase errors (points at which clocks travelling different directions converge). Make sure that clock signal drivers are only connected to appropriate clock signal receivers.

F. Elastic Buffering

Identify for each clock phase error, whether the phase error is due to 1) the same clock source signal arriving via different paths (constant phase error), or 2) independent clock sources (frequency error). See Chapter VI. for more information.

1. This phase error is determined by the clock frequency, clock distribution path length, and modem clock circuit characteristics. If these parameters will be constant for the circuit, the phase error at this point may be able to be ignored (if the phase error produces clocking at a stable portion of the data cycle).

If these parameters may change for the circuit, or if the phase error produces clocking at unstable portions of the data cycle (during transitions), then a short FIFO buffer may be used to overcome the clocking error. Other tricks may be used to shift clocking phase at certain points, but these techniques, in general, defy documentation and debugging.

2. If the clock phase error is due to frequency difference between independent clock sources, the magnitude of the maximum frequency difference must be estimated. A longer FIFO buffer is then introduced to hold off the clocking error for a time sufficient to allow passage of complete data packets (in this context, a packet is the information between line idle periods). Assure that the length of this buffer will not increase end-to-end communication delay beyond acceptable limits.

G. Interface Converters

Examine each identified DTE and DCE interface to assure interoperability with adjacent DTE/DCE interfaces (for example, V.35 interfaces do not interoperate with RS422). Insert interface converters into the design drawing to provide for compatibility between adjacent interfaces.

H. Installation

Mark off each element of the design drawing as it is installed. Be prepared to alter the design as other newfound requirements force design changes.

I. Initial Debugging

Use the following steps to test and document the installed circuit prior to on-line operation.

1. Establish the clock distribution path and measure any uncompensated phase errors to assure that these errors can be ignored (because data is being clocked at a stable portion of the data transmission cycle).

2. Starting from one end, test each component serially for signal continuity and loopback integrity. (Loopback cannot always be easily achieved at all points in the circuit due to clock path difficulties.) Note on the design drawing all valid loopback points for future diagnostics.

3. From the other end of the circuit, test each component serially for signal continuity and loopback integrity. Label on the design drawing all valid loopback points.

4. Remember to check for esoteric errors such as single data inversions (which become double inversions during loopback, such that the circuit works looped back but not end-to-end), or for cryptographic circuits mis-keyed (which can also cause circuits to work in loopback but not end-to-end).

5. Record bit error rates (and data transfer throughputs, if available) for the working circuit for future diagnostic reference.

J. Maintenance

From a suitable initial starting point in the middle of the circuit, presume that the circuit has a single point of failure, and use a bi-section diagnostic technique. Loop in the middle, if good, divide the circuit in half and loop in the middle of each half, etc.

As this design methodology is applied, document variations to this procedure as experience is gained or as repetitive requirements (for certain environments) are discovered.

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APPENDIX Example Circuit Designs

A. Simple Asynchronous Circuit

The asynchronous circuit example in Figure A1 represents a very simple circuit. This might be a link such as a dumb terminal connected to a computer.

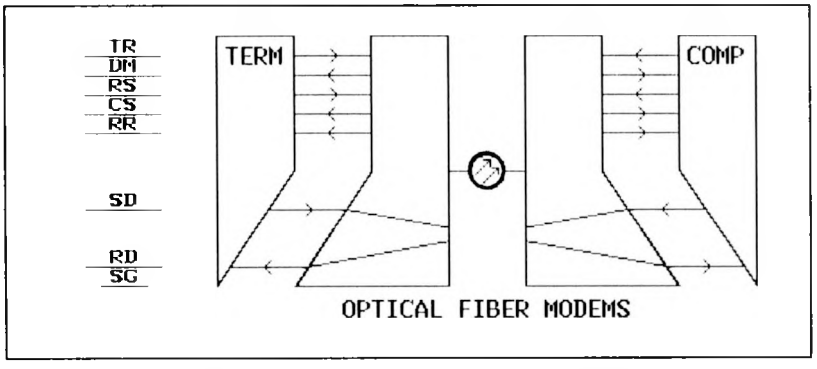

Figure A1. Simple Asynchronous Circuit

Since there are no separate clocks in the circuit (implied clocks are regenerated at each equipment, synchronized with the start bit), only the data lines need be shown. Clock lines and clock mode triangles on the DCEs are not needed. The control signal lines are shown, however, since they are typically used for the transmission of asynchronous data.

The DCEs were drawn as separate symbols but could just as easily have been drawn as a DCE Pair. In some cases, the designer might want to show what media is being used between modems, eg., optical fiber, twisted pair, or even a satellite channel. In Figure A1, optical fiber media is indicated by the symbol between the two modems. If the modems are drawn as a DCE Pair, media information can be noted under the symbol.

Looking from left to right in Figure A1, it can be seen that the modem pair reverses the data lines. SD on the left becomes RD on the right and vice versa in the other direction. When the distance between the terminal and the computer is short, a modem pair may not be needed. Instead, a null DCE, or null modem, can be used. This is usually a small box or cable with wires crosses inside it to perform the same crossover (of data, clocks, control signals, and grounds) as the modem pair. The symbol for the null modem is the same as that for the modem pair except that the word "NULL" is written in or about the symbol.

B. Multi-Segment Encrypted Synchronous Circuit

The synchronous example in Figure A2 is more complex than the previous one. This might be a link such as two computers communicating over an encrypted, multi-segment channel.

Since this is a synchronous circuit, the data lines, as well as the clock and control signal lines, are shown. Refer to Figure A2 during the following discussion of all circuit components. Additional information on synchronous communication is covered in Chapter VI.

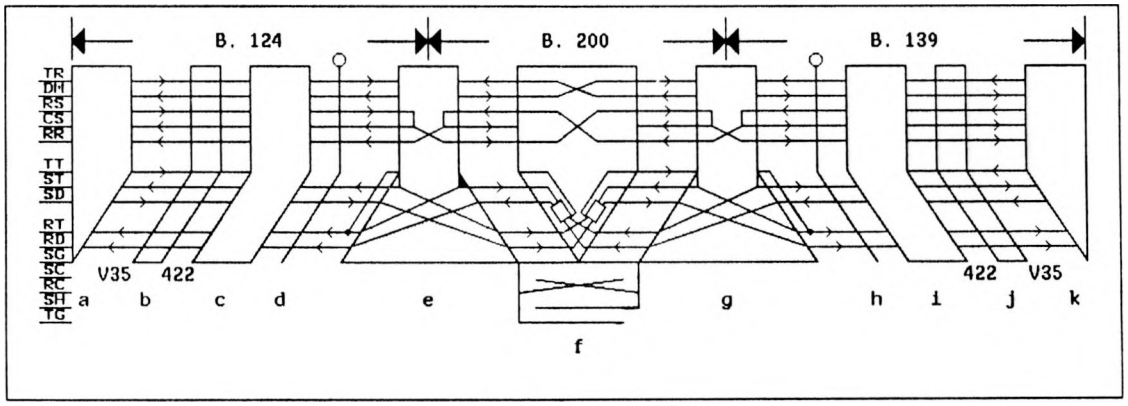

Figure A2. Multi-Segment Encrypted Synchronous Circuit

Devices a. and k. are DTEs that represent two computers remotely located. Note that the information written above the circuit shows the locations of all components.

Devices b. and j. represent physical link protocol converters. These convert the CCITT V.35 protocol electrical signals (from the computers) to EIA RS422 signals (for the rest of the circuit). The converter shape has a DTE on one side and a DCE on the other in order to keep the computer interface looking like a DTE. Only the signals' electrical characteristics are altered.

Devices c. and i. are encryption devices. Once again, the DTE/DCE shape combination is used and therefore the signal lines are not crossed. Unlike the protocol converters, the encryption devices do not change the electrical characteristics of the signals. They do, however, alter the the data bits during encryption/decryption. These devices typically do not pass TT from the end DTEs; therefore all modems must be clocked from a source in the middle of the circuit. If this restriction did not exist, each DTE would be able to clock its own path through the circuit.

Devices d. and h. are patch panels that are usually used in locations where troubleshooting might take place. Patch panels on either side of an encryptor and/or at each modem interface are common. A single line suffices for this symbol as it is just a passive device.

Device e. is a modem pair (segment) spanning Buildings 124 and 200. The modem represented by the right side of the symbol has the master clock for the entire circuit. This is indicated by the solid clock triangle. The left side modem is in slave mode and is shown with an open triangle and RT looped back to TT. This is a common arrangement for this type of circuit. Note the signal crossovers that take place through the modem pair.

Device g. is another modem pair segment which spans Buildings 200 and 139. The reason for this second modem pair might be that only twisted pair was available from Buildings 124 to 200 and only optical fiber was available from Buildings 200 to 139. For design purposes, this difference might have been irrelevant, and as such, was not indicated. The left side modem is being externally clocked; as evidenced by the open triangle and TT from the null DTE in the middle. The right modem (like the left modem of pair e.) is configured for slave timing.

Device f., in the middle, is a null DTE fifo buffer. It is a null DTE in order to fit between the two DCE interfaces in Building 200. Since there is only one clock frequency in the entire circuit, a frequency error can not occur. A phase error, however, can occur where SD is clocked into the right modem of pair e. (the master modem). The phase error will normally occur between TT and ST at this interface. To prevent data errors due to a constant phase error near 180 degrees, this null DTE also buffers the data bits through a fifo buffer. Since the right modem of pair g. is externally clocked, the fifo buffer in this path is not necessary. The buffer can be left in the circuit or bypassed.

The lines under the null DTE fifo represent various grounds in the circuit. These are usually left out of the circuit drawing. For reference, the five lines (from the top down) are: Signal Ground, Send Common, Receive Common (SC and RC cross as they should in a null device), Shield, and Tempest Ground.

These communication symbols have been in use to design, document, and troubleshoot complex circuits as Sandia National Laboratories since 1984. This paper provides a framework for visualization and documentation of these circuits. As such, these symbols form a valuable tool for the circuit designer who is familiar with the complex data communication circuit design constraints and issues. Using this tool, the designer may concisely convey his design to those who are responsible for circuit installation and maintenance.

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