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PHASE 2 OF THE AUTOMATED ARRAY ASSEMBLY TASK OF THE LOW-COST SILICON SOLAR ARRAY PROJECT

Final Report for the Period April 1, 1979—March 31, 1980

By
M. G. Coleman
R. A. Pryor
T. G. Sparks
R. M. Legge
D. L. Saltzman

Work Performed Under Contract No. NAS-7-100-954847

Motorola Inc.
Semiconductor Group
Phoenix, Arizona

U.S. Department of Energy

Solar Energy

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PHASE 2 OF THE AUTOMATED ARRAY ASSEMBLY TASK OF THE LOW-COST SILICON SOLAR ARRAY PROJECT

FINAL REPORT

1 APRIL 1979 - 31 MARCH 1980

MOTOROLA REPORT NO. 2345/8

JPL CONTRACT NO. 954847

PREPARED BY

MOTOROLA INC. SEMICONDUCTOR GROUP
5005 EAST MCDOWELL ROAD
PHOENIX, ARIZONA 85005

M.G. COLEMAN, R.A. PRYOR, T.G. SPARKS
R.M. LEGGE, D.L. SALTZMAN

THE JPL LOW-COST SOLAR ARRAY PROJECT IS SPONSORED BY THE U. S. DEPARTMENT OF ENERGY AND FORMS PART OF THE SOLAR PHOTOVOLTAIC CONVERSION PROGRAM TO INITIATE A MAJOR EFFORT TOWARD THE DEVELOPMENT OF LOW-COST SOLAR ARRAYS. THIS WORK WAS PERFORMED FOR THE JET PROPULSION LABORATORY, CALIFORNIA INSTITUTE OF TECHNOLOGY BY AGREEMENT BETWEEN NASA AND DOE.

PROJECT NO. 2345

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1.0 SUMMARY

Several specific processing steps, as part of a total process sequence for manufacturing silicon solar cells, were studied during this contract.

Ion implantation has been identified as the Motorola preferred process step for impurity doping. Unanalyzed beam ion implantation has been shown to have major cost advantages over analyzed beam implantation. Further, high quality cells have been fabricated using a high current unanalyzed beam.

Mechanically masked plasma patterning of silicon nitride has been shown to be capable of forming fine lines on silicon surfaces with spacings between mask and substrate as great as 250 μm (10 mils).

Extensive work was performed on advances in plated metallization. The need for the thick electroless palladium layer has been eliminated. Further, copper has been successfully utilized as a conductor layer, utilizing nickel as a barrier to copper diffusion into the silicon.

Plasma etching of silicon for texturing and saw damage removal has been shown technically feasible, but not cost-effective compared to wet chemical etching techniques.

2.0 INTRODUCTION

There is a high probability that flat plate solar photovoltaic modules will become a major source of electricity generation throughout most of the world, and that the silicon solar cell will be the preferred generating element. In order to provide a realistic framework on which to build an effective program of R&D and demonstration for silicon solar cell modules, a series of objectives has been established to lead to a 1986 goal of 70¢/peak watt (1980 $). At this price, solar-generated electricity will be able to compete with electric power generated by any other means, provided the solar cell modules are sufficiently reliable (e.g., have a mean life of 20 years).

To reach the 1986 JPL goal will require several advancements: 1) a cheaper source of pure silicon, 2) a much more economical way of transforming the source silicon into large, thin, (essentially) single crystal substrates having a controlled geometry, 3) an economical, large module package that will protect the interconnected solar cells it contains for at least 20 years from degradation caused by exposure to the weather, 4) an automated process sequence that produces high efficiency, reliable, cheap solar cells, tests them, interconnects them, and encapsulates them, and 5) a large market, of the order of 500 Mw/year.

When the JPL/ERDA Low-Cost Solar Array (LSA) Project started, the Motorola Solar Energy R&D Department participated in the Phase I of the Automated Array Assembly Task. The Phase I study identified a few potentially powerful process sequences for silicon solar cell production, and experimentally verified the overall consistency of the process sequence. It concluded that no basic technological innovations were necessary for solar cell fabrication or encapsulation in order to meet the long range LSA Project goals. Detailed

economic analyses were performed, based on today's technologies, and showed that it should be possible to meet the JPL cost projections for solar panels.

The overall conclusion of the Array Automated Assembly Task, Phase 1, was one of cautious optimism. The present program, for Phase 2, has as its objective the further development of specific process steps (in a particular, powerful process sequence) leading to a completely specified solar cell (and module) production process sequence. This sequence must be capable of a high degree of automation and control. A detailed economic analysis is a major part of the program to ensure that the most cost-effective approach is taken.

During the first part of the Phase II program, feasibility of the process sequence and its individual process steps were confirmed. This, the second part of the Phase II program, is concerned with specification of process control parameters and limits which will allow progress toward automation of the process sequence. The main objective of this contract is sufficient process control limit definition to permit advanced equipment prototypes to be designed for incorporation into an advanced pilot line facility.

3.0 TECHNICAL DISCUSSION

3.1 ION IMPLANTATION

Studies on ion implantation for impurity doping in solar cell structures have emphasized the areas of process control and high current unanalyzed beams.

3.1.1 SILICON SURFACE LAYER CONTAMINATION DURING ION IMPLANTATION

It has been noted in the literature (1) that the ion implantation process can, in itself, be a source of surface contamination. Although the process is done in vacuum, residual partial pressures of hydrocarbons from diffusion pump oil can result in polymerized hydrocarbon films because of bombardment by the ion beam. Such films may change the etching properties of the silicon surface and, ultimately, may affect the quality and integrity of metal-semiconductor electrical contacts. Ion implantation using large ion beam currents (in the milliamp range) may be especially susceptible to this surface contamination effect.

A clean, film-free silicon is hydrophobic, i.e., water does not wet the silicon surface. Alternatively, such surface films as silicon dioxide (SiO_2), silicon nitride (Si_3N_4), and photoresist are hydrophilic, being completely wet by water. These properties are useful for control in wet chemistry processing steps, allowing definitive end-point detection when removing surface films from silicon.

In using the Varian/Extrion model 200-1000 high current machine to form solar cell junction and back surface enhancement layers, an etch resistance phenomenon has been repeatedly observed. Wafers implanted with high doses in this high current machine could not be made hydrophobic in hydroflouric acid solutions, implying that some surface contamination is present.

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(1) K. A. Pikar, "Ion Implantation in Silicon" Applied Solid State Science, Volume 5, R. Wolfe, ed., Academic Press, N. Y., 1975.

Such surface contamination may present production control problems, and a clean silicon surface in the ohmic contact areas is imperative if consistent metal-semiconductor contacts are to be produced. A recent paper in the literature (2) has addressed this problem. It has found that ion-induced carbonaceous layers could be removed from the silicon surface by anodic oxidation with subsequent stripping in HF solution. This technique appears to satisfactorily restore the silicon surface cleanliness. (As long as the carbonaceous layer and subsequent oxide growth are at most a few hundred Angstroms thick, the properties of the original silicon surface may not be altered significantly.)

Alternatively, investigations were performed at Motorola using both thermal and plasma oxidation, followed by oxide stripping, to achieve the same cleaning effect. Oxide layers grown in the range from 250Å to 1000Å thick have been effective in restoring the hydrophobic nature of the silicon surface after stripping that oxide in dilute HF solutions. For a thermal oxide, growth can be accomplished during or after a thermal activation anneal cycle. This can be done in the same furnace tube or in a separate furnace tube. As for a plasma process, the only plasma oxidation cycle considered to date provides about 40Å of SiO_2 at most. Therefore, this cycle must be repeated several times, stripping the oxide after each cycle, to effectively remove the carbonaceous layer.

The fact that a polymerized hydrocarbon film or carbonaceous layer is responsible for the unusual etching/cleaning characteristics of high dose, ion implanted wafers is assumed (but not proven) from the cited reports in the literature and the observation that the oxidation/strip technique sucessfully restores the surface. If this assumption is correct, the best processing response is to eliminate the effect in the first place, rather than to try to cure it afterwards.

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(2) M. Y. Tsai, et. al., "Study of Surface Contamination Produced During High Dose Ion Implantation, "J. Electrochem. Soc.; Sol-St. Sci. and Tech., Vo. 126, No. 1, Jan. 1979, pp 98 - 102.

As recommended in Reference 2, the hydrocarbon vacuum pump oils used in the ion implanter vacuum system were removed and replaced with prefluorinated polyether pump oil. Examination of implanted surfaces then showed an improved ability to become hydrophobic, but not to the extent deemed desirable. Subsequent examination of the pump oils showed the presence of some residual hydrocarbons from the original pump oils. Apparently, sufficient quantities of these oils are still present in the system to cause difficulties. A thorough dismantling and cleaning of all vacuum components appears necessary to eliminate this residue. The results, while somewhat inconclusive, indicate the desirability of the perfluorinated polyether oils. Future vacuum systems for ion implanters should incorporate these oils from the start to eliminate subsequent contamination from the hydrocarbon oils.

3.1.2 COMPARISON OF STARTING MATERIALS THROUGH ION IMPLANTATION

A comparison of different ingot-grown starting wafers for ion implanted solar cells has been initiated. Wafers cut from both float zone and Czochralski ingots have been ion implanted and activation annealed for comparison. Early experiments indicated the possibility that float zone material was superior to Czochralski material. Accordingly, a more defined experiment has been performed to study the validity of the early results.

To minimize possible processing variables, bare, smooth, non-texture etched wafers have been utilized for the comparison. While a number of lots have been run, three representative groups are reported here. Each of the three groups consisted of 24 wafers. In each lot, one half (12) of the wafers were float zone wafers purchased from Wacker. These wafers were utilized as controls for comparison between lots. The other half of each lot was comprised of Czochralski wafers from Wacker, Monsanto, and

Motorola, respectively. All substrates were p-type, but various resistivity ranges were utilized.

Wafers were front ion implanted at 35 KeV with phosphorus at a dose of $2 \times 10^{15}/cm^2$. Back surface ion implants of 4×10^{15} boron were also performed. All wafers were then given a furnace activation anneal of 16 minutes at 850°C in a nitrogen ambient, followed by a 120 minute anneal in nitrogen at 550°C.

Open circuit voltage readings were recorded for each wafer under both room (fluorescent) lighting and a tungsten (ELH) simulation of 1-sun. The room light open circuit voltage gives an indication of the cell fill factor -- high values of room light V_{OC} indicate good fill factor. For these wafers, short circuit current readings were identified by measurement of the illuminated cells in reverse saturation. The results of these tests are shown in Table 1 as an average for each half lot.

These measurements indicate that, within experimental variations, all materials give comparable values of 1-sun parameters. A statistical difference is seen for the Czochralski material for room light open circuit voltage. Further processing of these cells through a silicon nitride antireflection coating and pre-metal patterning shows that the variation disappears at this stage of cell fabrication. For all practical purposes, thus, no basic differences have been observed between the various ion implanted materials.

3.1.3 UNANALYZED BEAM ION IMPLANTATION

Ion implantation equipment which is commercially available today is not capable of being incorporated into a process sequence which can meet the 1986 DOE goal of $0.70/peak watt (1980 dollars). There are several factors which limit today's implanters. First, the throughput of cells in today's machines is too low.

TABLE 1

COMPARISON OF ION IMPLANTED, SMOOTH-SURFACED MATERIALS

		BEFORE AR			WITH AR
		OPEN CIRCUIT VOLTAGE (VOLTS)		SHORT CIRCUIT CURRENT (milliamps)	OPEN CIRCUIT VOLTAGE (VOLTS)
LOT	MATERIAL	ROOM LIGHT V_{RL}	1-SUN V_{OC}	1-SUN I_{SC}	ROOM LIGHT V_{RL}
SD019	Wacker FZ 1.3 - 3.0 Ω-cm	.308	.564	1050	.391
	Wacker CZ 1.9 - 2.6 Ω-cm	.276	.563	1050	.423
SD020	Wacker FZ 1.8 - 3.0 Ω-cm	.310	.573	1085	.420
	Monsanto CZ 0.2 - 0.5 Ω-cm	.283	.573	1055	.440
SD021	Wacker FZ 1.8 - 3.0 Ω-cm	.338	.579	1115	.432
	Motorola CZ 0.8 - 2.0 Ω-cm	.145	.564	1125	.386

being limited both by low ion beam currents and by mechanical tranport mechanisms. Second, today's machines are very complex, resulting in three specific problems: (1) high cost, (2) large size, and (3) extensive maintenance. Restated, the cost per machine is far too high for the throughput rate of the equipment, while the large size and low throughput require significant additional capital investment for building floorspace.

Two major areas of cost reduction are available for ion implantation. First, major increases in ion beam current levels are necessary to make ion implantation a viable long range solar cell manufacturing technology. (Increases of more than an order of magnitude, to at least 100 mA, are required.) In addition, reduction of equipment cost is required to ensure that ion implantation is a preferred technology for future solar cell high volume manufacturing. If successful, these innovations would ensure that ion implantation will be the favored long range process for both p-n junction and BSF formation. A new machine design philosophy, however, is required to achieve these objectives.

One of the major factors now limiting ion beam current (and throughput) is the requirement of mass analysis of the ion beam. In general, any ion beam will contain all of the possible molecular and atomic species which can be formed from the source material. In addition, the ion beam may have foreign species from the source chamber, vacuum walls, or pump oil. In order to implant only one atomic or molecular specie, the beam is mass analyzed to eliminate all the undesired species.

Mass analysis is commonly performed by accelerating the ion beam, and then changing the direction of the beam by passing it through a magnetic field. Ions which are too heavy are not bent enough, while ions which are too light are bent beyond the desired direction. Only ions with the specifically desired mass can pass through the analyzer. By changing the field strength

of the analyzing magnet, the desired specie can be chosen. Mass analyzed spectra for three source gases, phosphine (PH_3), arsine (AsH_3), and boron trifluoride (BF_3), are presented in Figures 1 through 3, respectively.

The mass analysis process creates a non-focused diverging ion beam. Following analysis, thus, the beam is normally focused by magnetic fields to the desired beam geometry. While this is suitable for small beam currents, at high beam currents the beam becomes self-shielding from the magnetic fields, requiring greater complexity of equipment.

The equipment components for mass analysis and beam focusing are both large and expensive, major factors in the total cost and floorspace requirements of present equipment. If mass analysis is not, in fact, required for ion implanted solar cells, the equipment can be greatly simplified. Such a simplification would be highly desirable from a cost stand-point.

3.1.3.1 SIMULATED UNANALYZED BEAMS

A series of experiments to investigate the feasibility of utilizing a simulated unanalyzed beam were performed. For these experiments, all of the major components of the ion beam, as identified in the spectra of Figures 1 through 3, are implanted into the cell in proportion to their relative intensities in the spectra. This, in effect, simulates an unanalyzed beam implantation from the gaseous sources. It is not a full simulation, however, since trace components of the beam are ignored. However, if high quality solar cells can be fabricated from the present experiments, the potential feasibility of an unanalyzed beam machine utilizing gaseous sources can be established. The experiments, thus, while not sufficient, provide necessary information for the utilization of unanalyzed ion beams for solar cell fabrication.

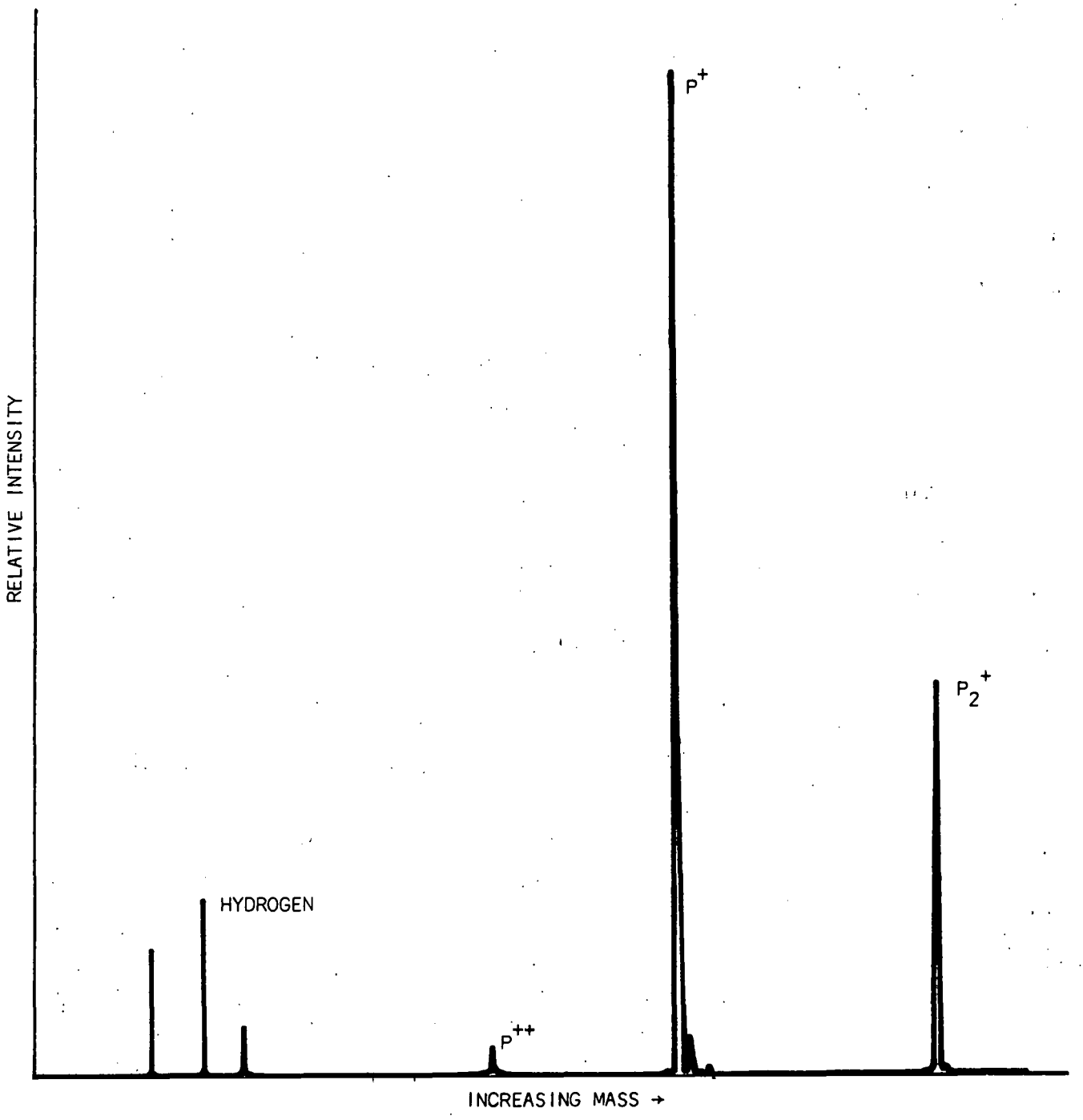


FIGURE 1
MAJOR PEAKS OF PH_3 SOURCE ION SPECTRUM

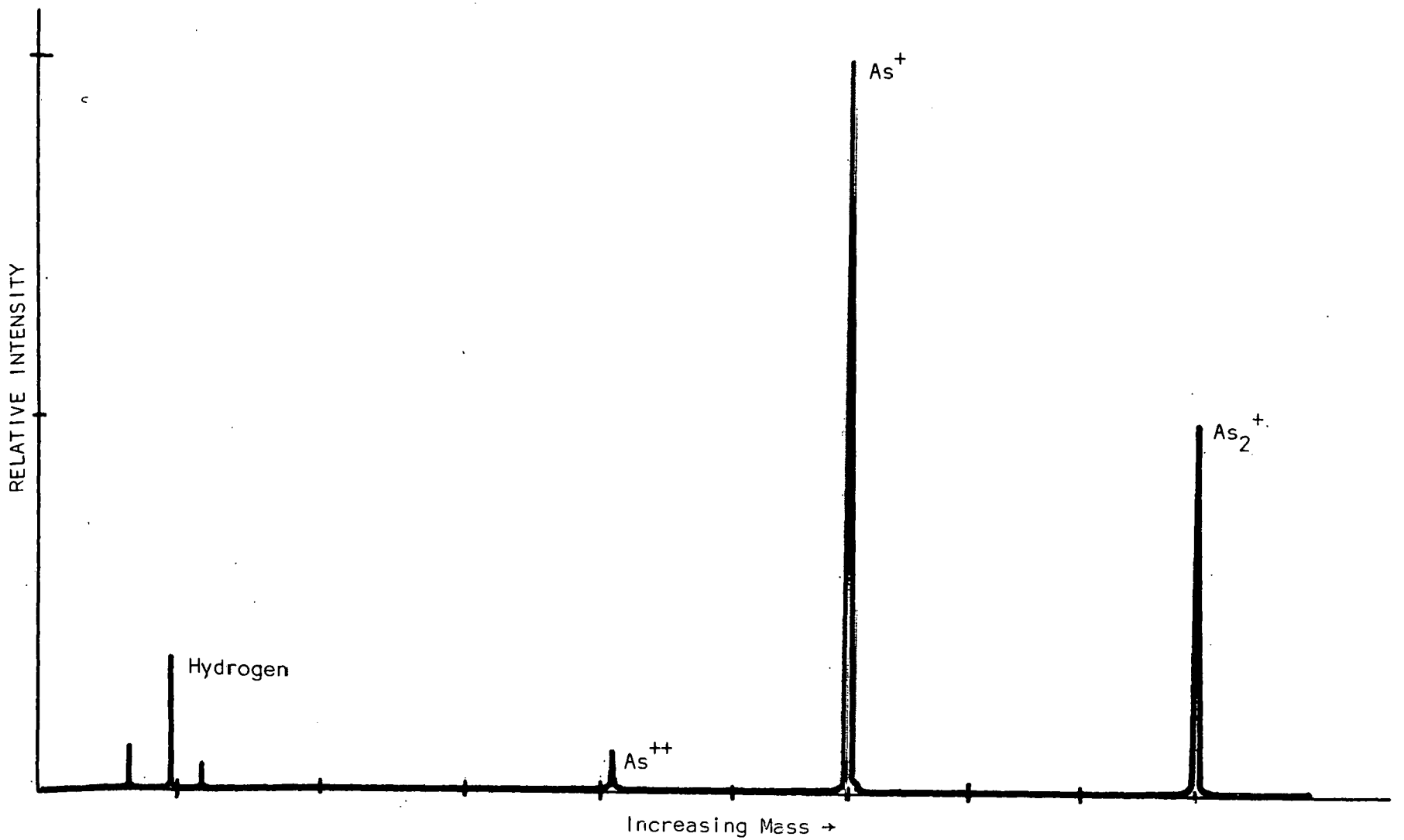


FIGURE 2
MAJOR PEAKS OF AsH_3 SOURCE ION SPECTRUM

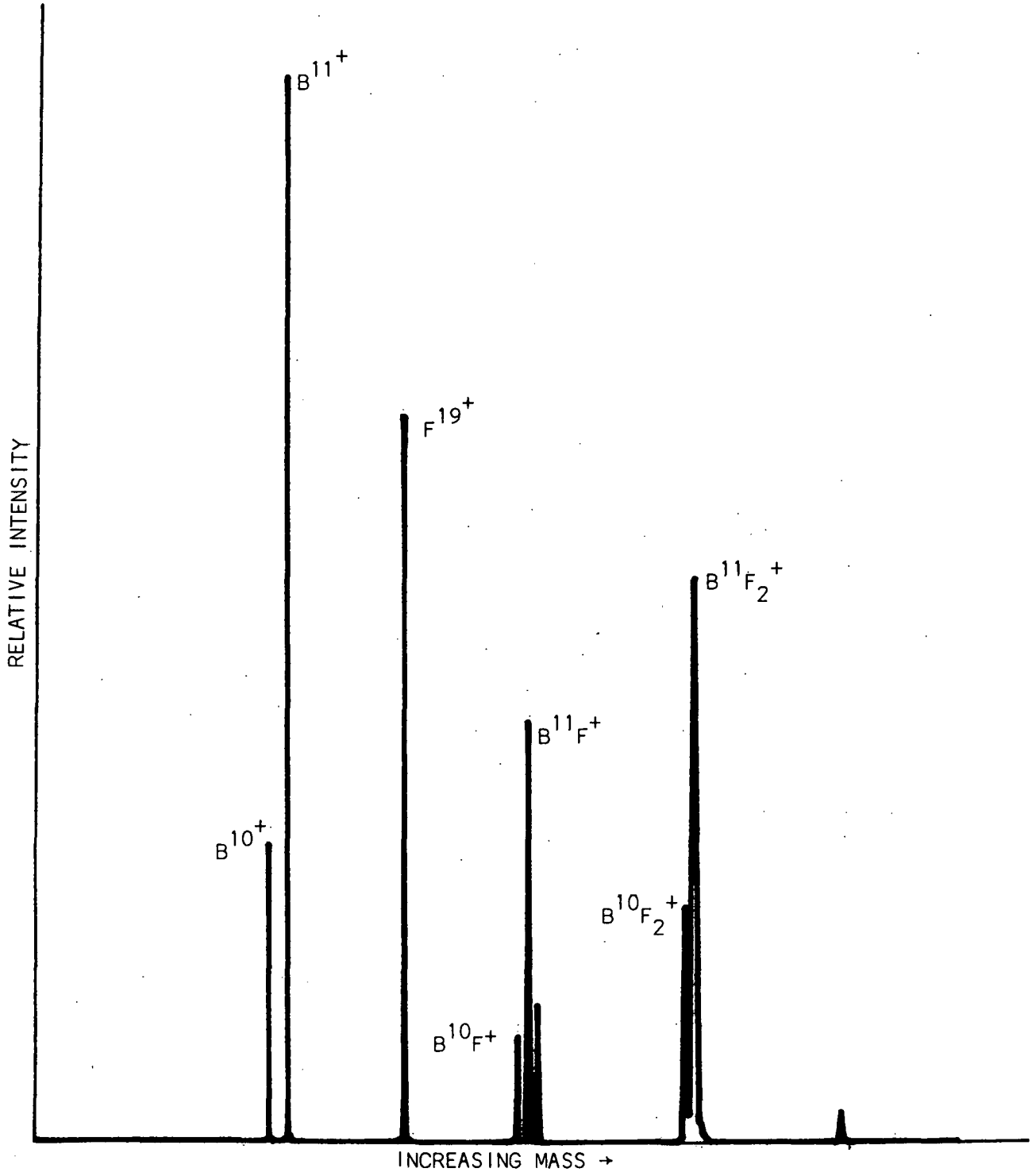


FIGURE 3
MAJOR PEAKS OF BF_3 SOURCE ION SPECTRUM

In these simulations, the major ionic species present in the ion source are implanted in proportion to their relative concentrations in the source mass spectrum. Different isotopes of the same species are not implanted. The species implanted are identified in Table 2 for each source. Groups of wafers for fabricating solar cells are divided such that one half of each lot received the simulated unanalyzed implant.

Cells were completed for both the arsine and phosphine sources. Data for the specific cells made from the analyzed and simulated unanalyzed implants are shown in Table 3. For these two types of implants, no statistical difference can be observed for the arsine and phosphine sources. For arsenic and phosphorus doping, thus, no deleterious effects can be seen from the implantation of hydrogenated ions.

While cells were not completed, ion implantation using all of the major beam peaks in a BF_3 ion spectrum has been shown to produce high quality photoresponse in silicon p-on-n solar cells. Substrates of 7 mil thickness, nominally 0.1 Ω-cm arsenic doping, and smooth surfaces, have shown open circuit voltages in excess of 600 mV and very high fill factors. In all cases, the BF_2 component of the ion spectrum was implanted first, followed by other boron and fluorine components. The results show, in fact, the fluorine is performing some "gettering" effect.

The use of a simulated unanalyzed beam certainly appears feasible based on these experiments. The potential problem of implanting trace impurities, however, remains unaddressed by these simulated techniques.

3.1.3.2 UNANALYZED BEAMS

In order to address the possible implantation of trace impurities in an unanalyzed beam, implantation with a totally unanalyzed beam is necessary.

TABLE 2

SIMULATED UNANALYZED ION BEAM IMPLANTS

GAS SOURCE	PH_3	AsH_3	BF_3
Primary Species (Control)	P^{31} (+1)	As^{75} (+1)	B^{11} (+1)
"Unanalyzed" Species	P^{31} (+1)	As^{75} (+1)	B^{11} (+1)
	P^{31} (+2)	As^{75} (+2)	F^{19} (+1)
	P_2^{31} (+1)	As_2^{75} (+1)	BF^{30} (+1)
	H_2 (+1)	H_2 (+1)	BF_2^{49} (+1)

TABLE 3

CHARACTERISTICS OF SELECTED ION IMPLANTED SOLAR CELLS FABRICATED UTILIZING ANALYZED AND SIMULATED UNANALYZED ION BEAMS. (NON-OPTIMIZED PROCESS)

	I_{SC} (A)	V_{OC} (V)	F.F. (%)
Arsine (AsH_3) Source			
As^{75} (+1)	1.335	0.575	71.2
Unanalyzed	1.375	0.585	73.7
Phosphine (PH_3) Source			
P^{31} (+1)	1.325	0.582	74.7
Unanalyzed	1.350	0.580	73.6

In addition to eliminating mass analysis, a second change in implanter design is desirable to accommodate a very high ion beam current. The change is to utilize a large area beam rather than a small area focused beam. If very high beam currents are focused to a small area, current densities would be very high. These high current densities are capable of causing significant localized substrate heating effects, thought now to be deleterious to device performance. Such localized heating effects, caused by the very high local dose rate, can be reduced or eliminated through the use of lower localized dose rates available through a large area, high current ion beam.

Both features of a totally non-analyzed ion beam and a large area beam are available through the modification of commercially available ion milling equipment. Modifications for safety, since phosphorus, arsenic, and some boron compounds are highly toxic, are necessary.

Ion milling equipment has many features desired for mass production of low cost solar cells. A comparison of similarities and differences between conventional ion implanters and ion millers is shown in Table 4. The ion miller has the desirable features identified for future implantation equipment.

The Solar Energy R&D Department at Motorola does not now posess an ion milling unit. Arrangements were made, however, to modify a unit in another area for preliminary experiments.

In an attempt to fabricate n-on-p junctions for solar cell devices with low energy, hi beam current, unanalyzed ion implantation means, an experiment was organized to use a Commonwealth Scientific Ion Milling machine. This machine has a 4" diameter ion gun, 2.0 keV and 0.4 mA cm^{-2} capabilities. It was modified to accept the dopant gas, 15% PH_3 in 85% H_2 and to exhaust the waste gases in a safe manner.

TABLE 4

A COMPARISON OF CONVENTIONAL ION IMPLANTATION
AND ION MILLING EQUIPMENT

SIMILARITIES:

HIGH VACUUM

AREA DEPENDENT

UTILIZE ACCELERATED IONS

DIRECTIONAL

DIFFERENCES:

CHARACTERISTIC	IMPLANTER	MILLER
IONS	DOPANT SPECIES	MOSTLY ARGON
ANALYSIS	ANALYZED	UNANALYZED
ENERGY	5 - 200 keV	0.3 - 1.0 keV
CURRENT	1 - 10 mA	200 - 4000 mA
AREA	<10 cm^2	>200 cm^2
VACUUM	10^{-6} - 10^{-5} TORR	$2 - 5 \times 10^{-4}$ TORR

Substrate material chosen for this first experiment was Wacker float zone 1.8 - 3.0 Ω-cm, chemically etched, nontextured. In order to establish useful ranges for the first attempt, various process parameters were given wide limits. The p+ back surface enhancement layer was fabricated by several means. Fifty percent of the wafers were ion implanted with B^{11} at a concentration of 4×10^{15} cm^{-2}, 25% were diffused with "standard" BCl_3, and 25% undoped. Both of these process steps were completed before the p-n junction was formed and both saw the anneal cycle that followed the non-mass-analyzed ion implantation (ion milling) process step. The last 25% were ion implanted and annealed with 4×10^{15} atoms cm^{-2} of B^{11} just before metallization. No appreciable differences were seen between groups with ion implanted and diffused methods of back enhancement fabrication.

The n+ front surface was formed by utilizing the $PH_3 + H_2$ mixture in the ion miller. This was the first occasion that this species and mixture of gas had been used to achieve an ion beam in this machine; however, no difficulty was experienced at all.

The substrate stage has 8 ea. 3" diameter wafer capability and 4 ion milling runs were done at different accelerating voltages and exposure times. All the runs were done at about 0.10 to 0.15 mA cm^{-2} of beam current. The first group was implanted in the milling machine with 1.5 keV of energy and with each wafer passed in front of an aperature in a shield which allowed about 3 - 4 seconds of beam exposure on each wafer in turn corresponding to near 3×10^{15} ions cm^{-2}. The second group was implanted in the miller with 2.0 keV of energy with each wafer passing twice in front of the aperature for about 6 - 8 seconds of exposure, or approximately 6×10^{15} cm^{-2}. The third group was not shielded at all and all 8 wafers saw about 2 - 3 seconds of beam. The fourth group was not shielded and saw about 20 seconds of beam. or about 6×10^{16} ions cm^{-2}.

The anneal cycle was 15 min. at 850°C in N_2 followed by 120 min. at 550°C in N_2.

A mesa configuration on the cells (junction edge-etched structure) was achieved by stacking all wafers in direct contact and plasma etching the edges of all wafers.

The AR coating was performed by first forming a thin silicon dioxide (SiO_2) layer on the wafers followed by vacuum deposition of 700Å of Si_3N_4 and a further anneal of 120 min. at 550°C in N_2. The thin oxide layer was grown by a plasma oxidation step for 10 minutes. In the plasma process, a plasma of oxygen ions is formed from O_2 in a standard plasma cleaning system widely used in the semiconductor industry. The energetic oxygen ions from the plasma are capable of uniformly oxidizing silicon surfaces to form thin SiO_2 layers at temperatures near room temperatures.

The preohmic pattern was accomplished with standard photoresist methods.

The pre-metal probe of electrical parameters showed group #4 (20 sec. of beam) to be the only group worth metallization.

Metallization was done by immersion, electroless and electrolytic methods to form a Pd-Ni-Cu-Ni layering.

Testing before metallization gave the parameter estimates for the eight cells of group #4, shown in Table 5.

V-I characteristics (AM1) following metal of 4 of the cells are shown in Figures 4 - 7.

The results of this experiment show that solar cells can be made with totally unanalyzed beam high current ion sources. The potential cost benefits of this technique demand that future efforts be expended in this area.

3.2 PLASMA ETCHING STUDIES

The use of plasma processing as a replacement for wet chemistry steps has been studied during this contract. Specifically, plasma replacement of three steps has been investigated: (1) Mechanically masked plasma patterning of silicon nitride layers, (2) plasma etching of silicon to remove either surface layers or sawing damage, and (3) plasma texture etching.

TABLE 5

PARAMETER ESTIMATES OF UNANAYLZED BEAM
ION IMPLANTED CELLS PRIOR TO METALLIZATION

LOT NO.	WAFER NO.	OPEN CIRCUIT VOLTAGE	SHORT CIRCUIT CURRENT
SC018	5	594 mV	1135 mA
	6	563	1110
	17	523	780
	18	593	1380
SC024	8	560	1080
	9	578	1200
	10	570	1230
	11	561	1080

FIGURE 4: ILLUMINATED, ONE SUN, (AM1, TUNGSTEN SIMULATION) VOLTAGE-CURRENT CHARACTERISTIC FOR NON-MASS-ANALYZED, ION IMPLANTED SOLAR CELL. IMPLANT WAS PERFORMED AT LOW ENERGY WITH AN ION MILLING APPARATUS. BACK SURFACE FIELD: BCl_3 DIFFUSION.

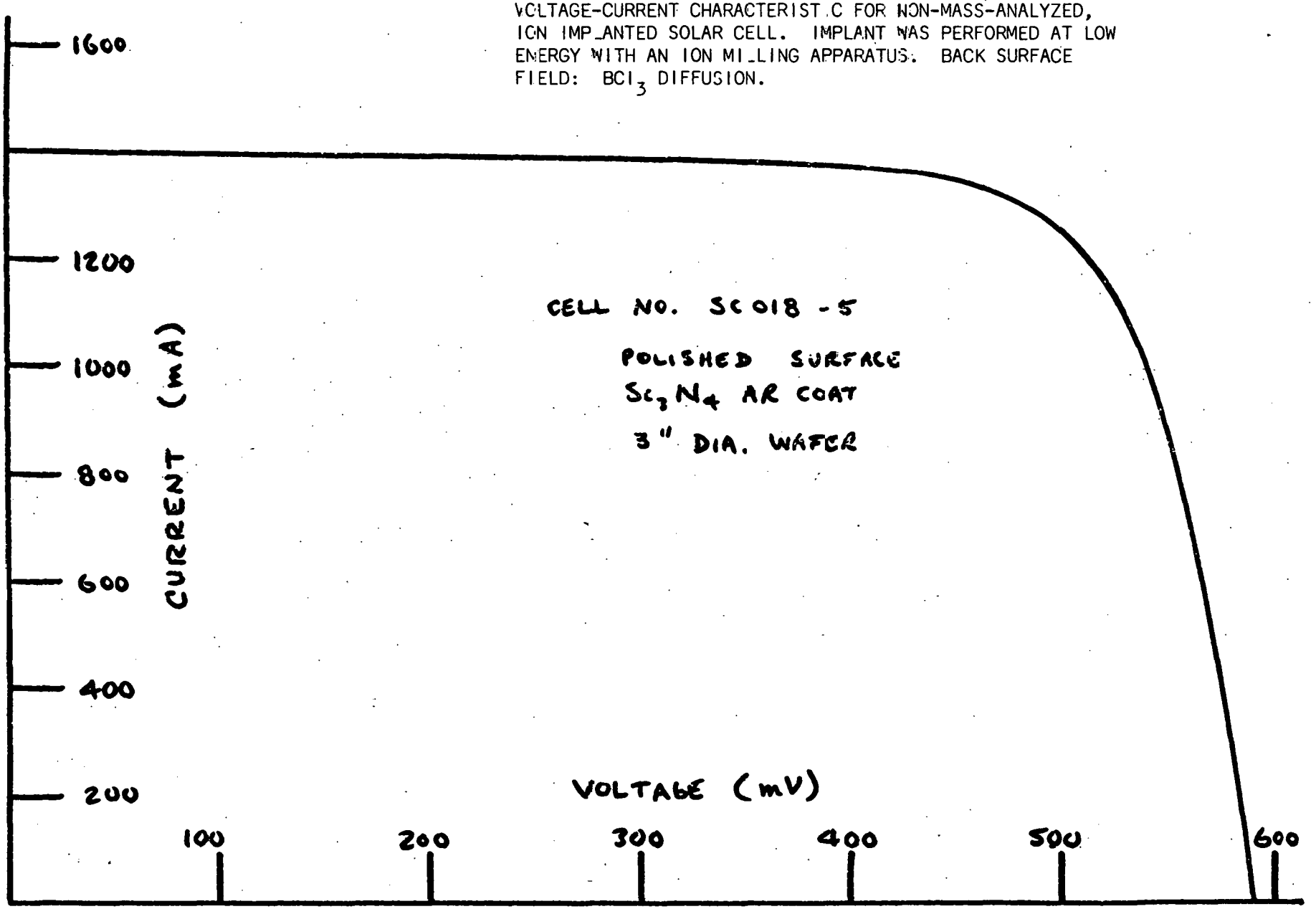


FIGURE 5: ILLUMINATED, ONE SUN, (AM1, TUNGSTEN SIMULATION) VOLTAGE-CURRENT CHARACTERISTIC FOR NON-MASS-ANALYZED, ION IMPLANTED SOLAR CELL. IMPLANT WAS PERFORMED AT LOW ENERGY WITH AN ION MILLING APPARATUS. BACK SURFACE FIELD: BCl_3 DIFFUSION.

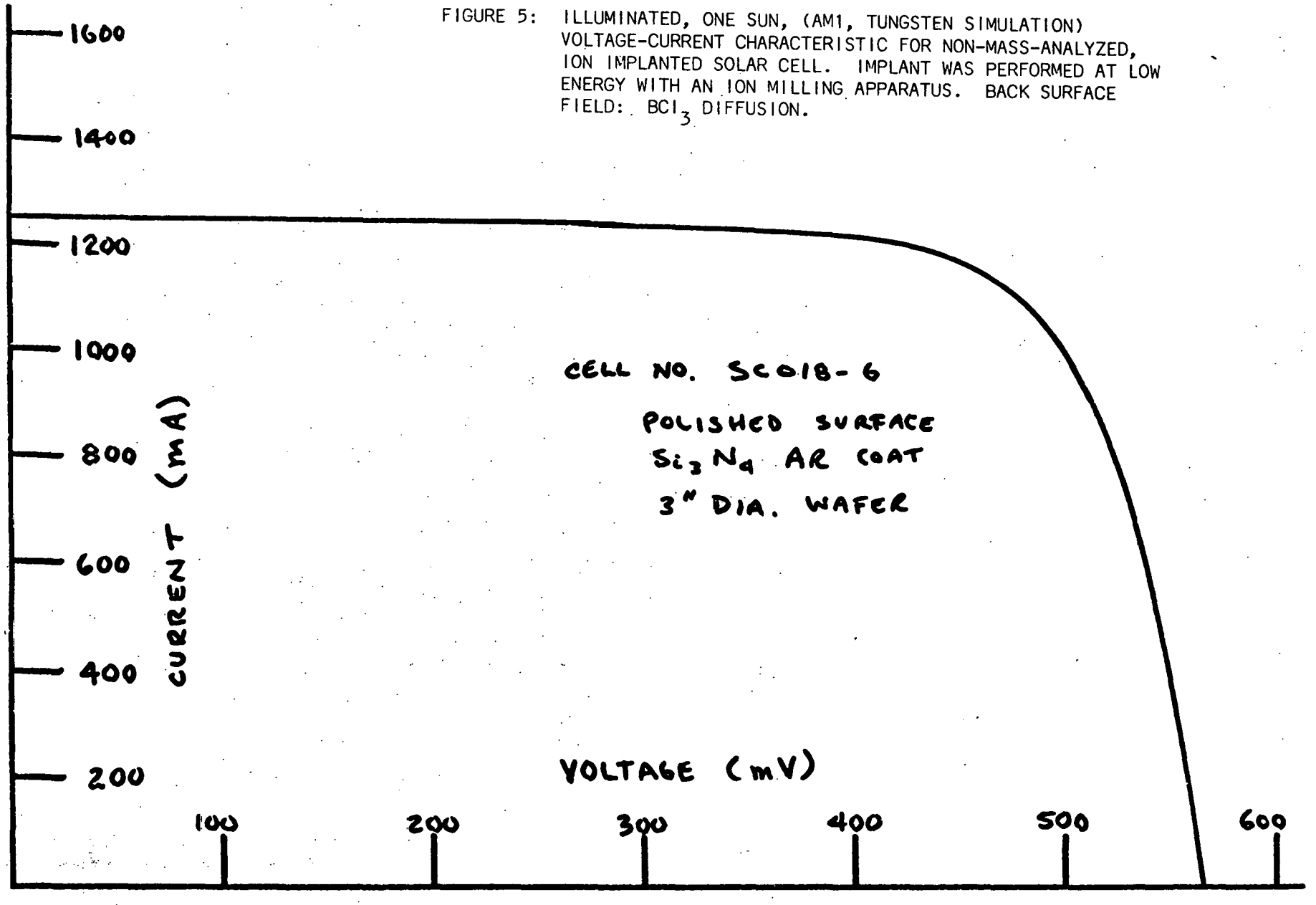
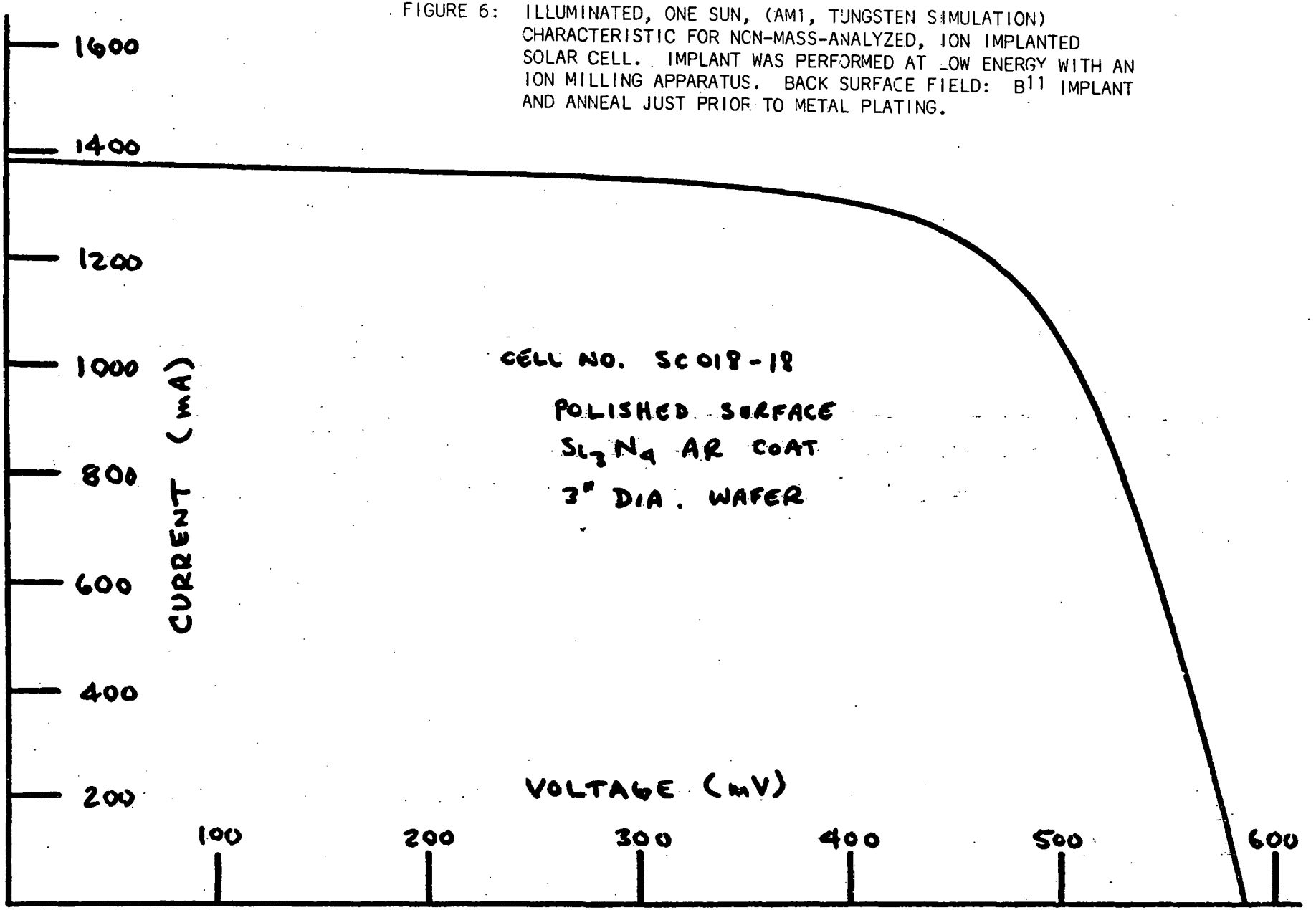


FIGURE 6: ILLUMINATED, ONE SUN, (AM1, TUNGSTEN SIMULATION) CHARACTERISTIC FOR NON-MASS-ANALYZED, ION IMPLANTED SOLAR CELL. IMPLANT WAS PERFORMED AT LOW ENERGY WITH AN ION MILLING APPARATUS. BACK SURFACE FIELD: B^{11} IMPLANT AND ANNEAL JUST PRIOR TO METAL PLATING.



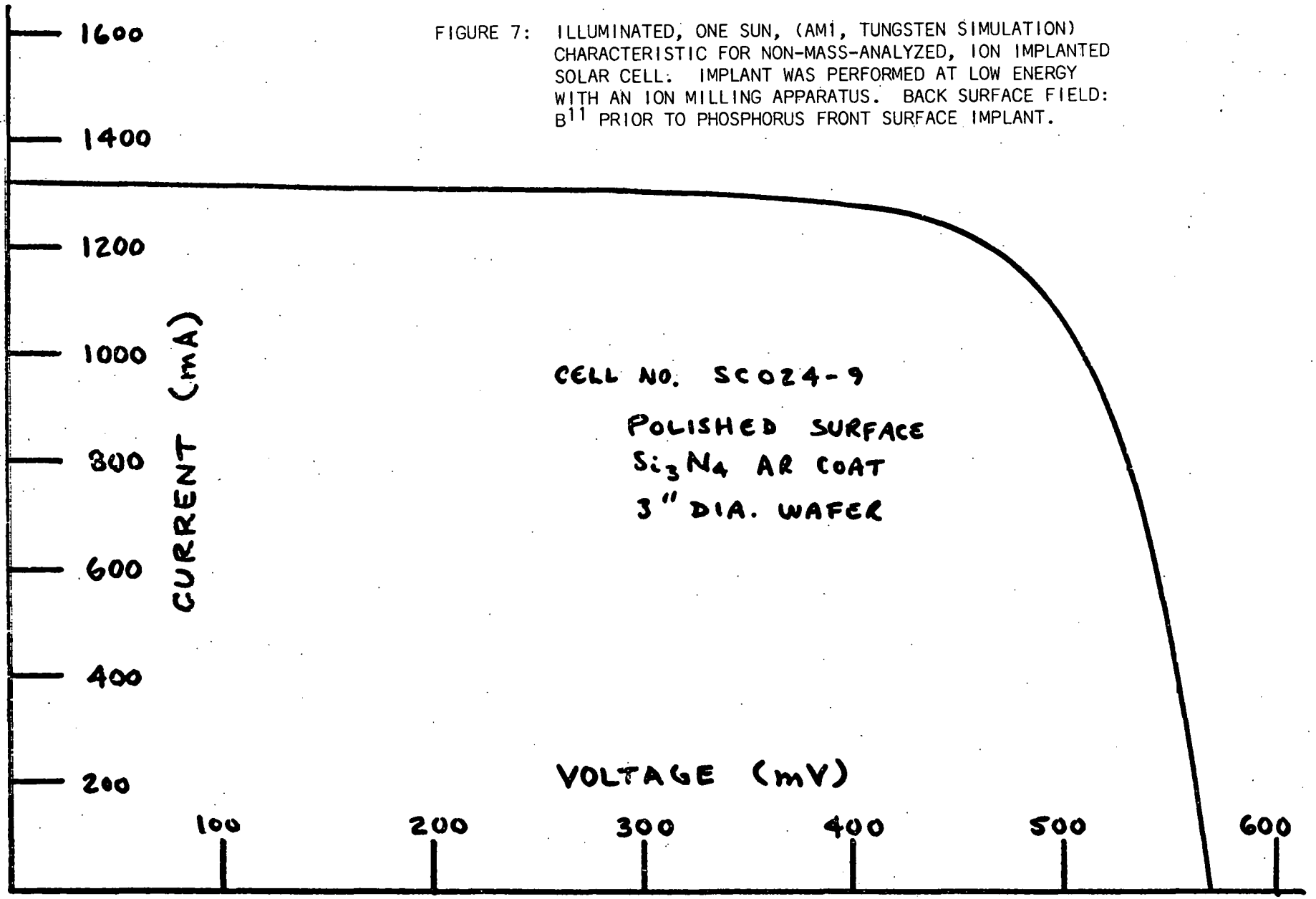


FIGURE 7: ILLUMINATED, ONE SUN, (AM1, TUNGSTEN SIMULATION) CHARACTERISTIC FOR NON-MASS-ANALYZED, ION IMPLANTED SOLAR CELL. IMPLANT WAS PERFORMED AT LOW ENERGY WITH AN ION MILLING APPARATUS. BACK SURFACE FIELD: B^{11} PRIOR TO PHOSPHORUS FRONT SURFACE IMPLANT.

3.2.1 PLASMA PATTERNING

In the solar cell fabrication process sequence under development at Motorola, a silicon nitride layer deposited on the surface of the solar cell must be etched away in the configuration of the desired metal contact pattern. This patterning of the silicon nitride has been achieved by use of a plasma etching technique.

A baseline process sequence was established early in the contract extension period for the plasma patterning process, and applied to textured surfaces. From this baseline, variations were performed to improve manufacturability, reproducibility, and control of the plasma patterning technology. The technology is aimed at selectively and simultaneously etching ohmic contact patterns into the silicon nitride on both sides of a silicon substrate without significantly etching the silicon surface beneath those ohmic areas.

3.2.1.1 THE BASELINE PROCESS

The best pattern definition and selectivity have been achieved by etching in what is referred to as the "reactive ion etching" mode. In this mode, the water to be patterned is placed on top of the same electrode to which RF energy is applied. A plasma is struck between that electrode and the surrounding walls of the vacuum chamber, which is at ground potential. The plasma is established at low pressure, less than 0.1 Torr. The RF electrode is capacitively coupled to the RF power supply and will float to a negative DC bias with respect to the plasma potential. This establishes an electric field which can accelerate ions from the plasma to the surface of the wafer supported on the RF electrode. This effect enhances the anisotropy of the plasma etching reaction and helps promote good line definition and mask opening replication without etching beneath the masked areas.

The baseline plasma patterning process sequence is described in the following paragraphs.

A steel shadow mask with openings where the silicon nitride is to be etched away is mechanically aligned to the front surface of a silicon nitride coated solar cell. The cell and mask are placed on a sheet of flat ceramic magnets which serve to hold the steel mask in registration with the cell surface.

The magnetic plate, cell, and mask assembly is positioned in a vacuum chamber on the RF electrode plate. (Plate area is 196 cm^2.) The electrode and chamber are preset at a temperature of 50°C.

The chamber is closed and pumped down to below 0.05 Torr. This requires about 30 seconds.

When pump-down is complete, RF power (100 watts at 13.56 MHz) and etchant gas flow (approximately 1 cm^3/min.) are started simultaneously to generate the plasma. In work to date, a gas mixture of 8% oxygen in Freon 14 (CF_4) has been used. The plasma is maintained for four minutes.

At the completion of the etch cycle, the RF power and etchant gas flow are stopped, the chamber is vented with nitrogen, and the wafer removed.

This process yields excellent replication of the etch mask openings. In fact, due to the nature of the reactive ion plasma and the metal mask, the line openings etched in the silicon nitride are typically a few tenths mil smaller than the line openings in the steel mask. The masks used for the experiments have approximately 5 mil line openings.

This process can be performed without degrading solar cell electrical characteristics. This has been shown by direct comparison of solar cells whose only difference in processing was the ohmic patterning step. Plasma patterned cells have been compared with those patterned by conventional photolithographic techniques using photoresist to protect against buffered HF etching. Both patterning processes can yield high quality solar cells.

This must imply that even though the CF_4-O_2 gas mixture is capable of etching silicon as well as silicon nitride, any silicon etching which occurs while clearing (patterning) the silicon nitride is not significant.

This implication is confirmed by the etch rate data presented in Figure 8. These data were from a series of samples run at the same pressure, and flow rate as the baseline process. (Some electrode heating during the runs was possible in these cases, however.) Both etch time and RF power were varied. Bare silicon wafers were protected with photoresist so as to expose silicon areas in the shape of a metal grid pattern. After plasma etching, etch depths into the silicon were measured with a mechanical instrument similar to a profilometer. While it is obvious from the data in Figure 8 that the etching process is complex. silicon etching is not a serious problem. For example, silicon etch rates at 100 W RF power are small enough so that even for the case of 100% overetching (etching to clear Si_3N_4 in 4 min., then etching Si for an additional 4 min.), only 0.08 μ of silicon surface would be lost. Note that these data imply that the etch rates for Si and for Si_3N_4 were nearly equal for this particular process. Of course, such a large amount of overetching is not required in the actual process.

3.2.1.2 ADVANCED PROCESSES

Advanced solar cell structures will probably have patterned both front and back metallization contacts. For such cell geometries, it is desirable to pattern both sides of the cell simultaneously in order to minimize the number of process steps and to maximize equipment throughput. In this way, front and back symmetry of the patterns can be readily achieved without the necessity of realignment to an existing pattern on one side.

Advancements in ion-enhanced plasma etching of the silicon nitride layer have been demonstrated. These advancements are the result of modifications in equipment configuration.

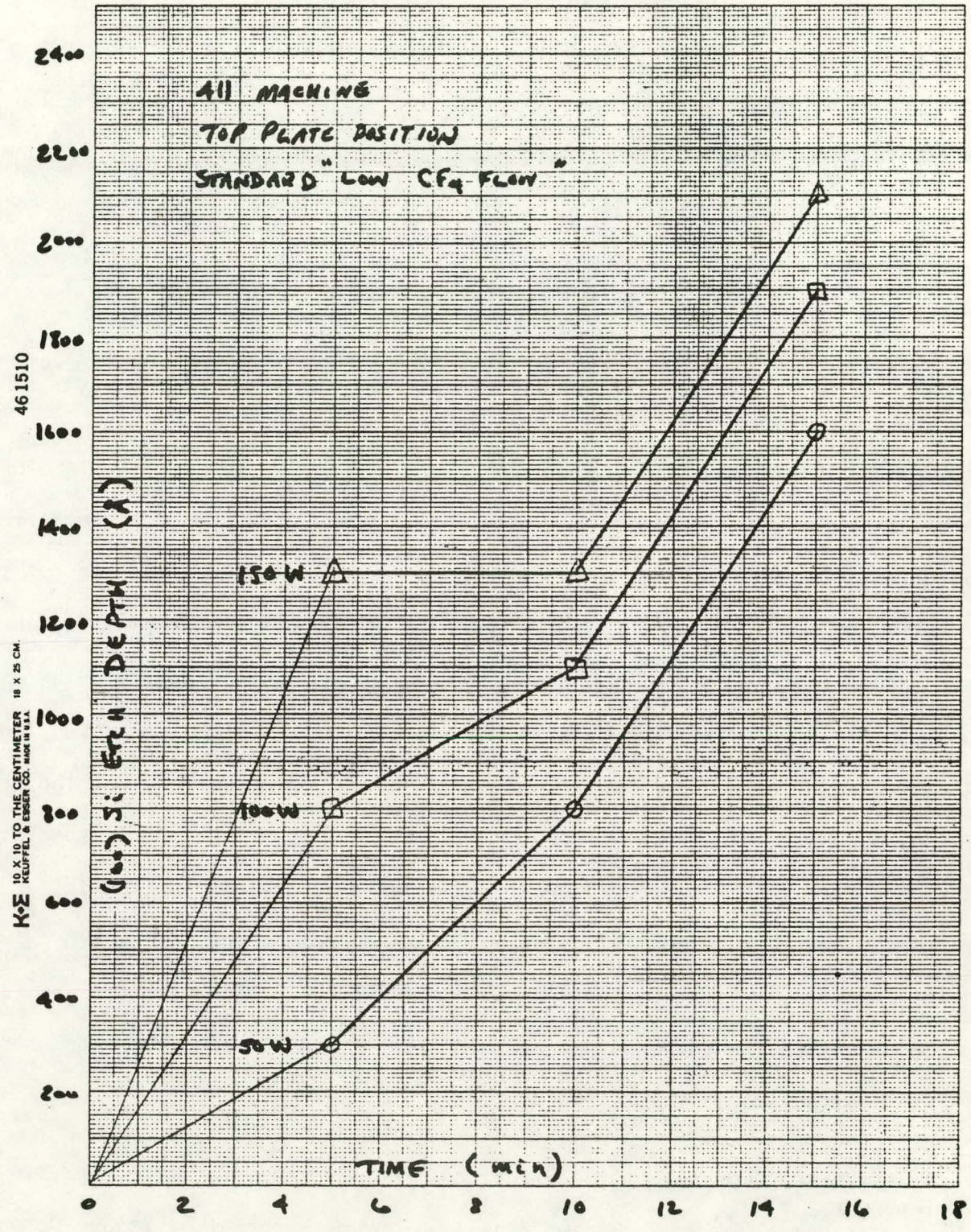


FIGURE 8: SILICON ETCH RATE DATA FOR BASELINE REACTIVE ION ETCHING MODE.

The baseline equipment configuration, figure 9A, has the cell on the RF powered electrode with the vacuum chamber walls as the ground electrode. This equipment has been mofified to have a grounded electrode parallel to the power electrode, figure 9B. This is similar to the arrangement used for RF sputter etching, and in general increases the plasma potential and ion density (3). As expected, an increase in etch rate was observed; unexpectedly (but fortunately) a significant improvement in etch anisotropy also occurred. This etch anisotropy is evidenced by better dimensional replication of the mask in the nitride pattern.

To evaluate the improved etch anisotropy, a metal mask was placed over the cell separated from the surface by a spacer ring as in figure 10. The nitride was then etched with plasma conditions similar to these ulilities for the baseline process. Various thicknesses of spacers were used with resulting separations of 0.005 to 0.020 inches. The maximum line definition lost (width increase) was 10% for the 0.020 inch separation. To obtain such results, an ion-enhanced etching mechanism (reactive ion etching) must predominate the process. As illustrated in Figure 11, random gas motion of unaccelerated ions and neutral species would cause etched lines several times larger than the mask opening, even without surface migration of absorbed neutral and ionic species. The accelerated ions, as assumed, would have paths essentially normal to the power electrode and possibly have a fousing effect at the narrow line opening in the mask. This effect has been observed in various ion sources (4), and could explain the etched lines being narrower than the mask openings when the mask is in direct contact with the surface.

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(3) J. L. Vossen, Journal of the Electrochemical Society, Vol. 126, pg. 319 (February 1979).

(4) H. R. Kaufman, J. M. E. Harper, and J. J. Cuomo, Journal of Vacuum Science and Technology, Vol. 16, pg. 899 (May/June 1979).

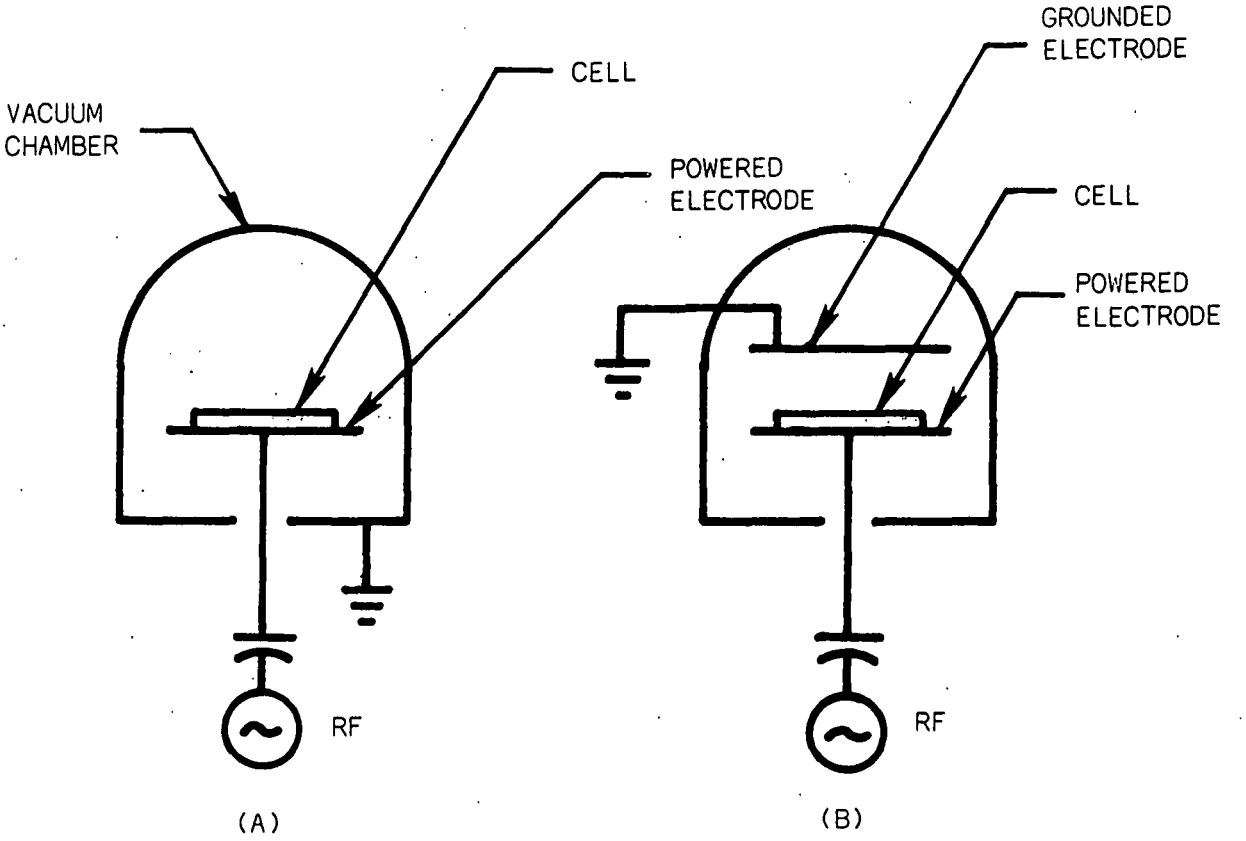


FIGURE 9

PLASMA ETCH EQUIPMENT CONFIGURATIONS (A) BASELINE PROCESS, (B) PARALLEL PLATE MODIFICATION.

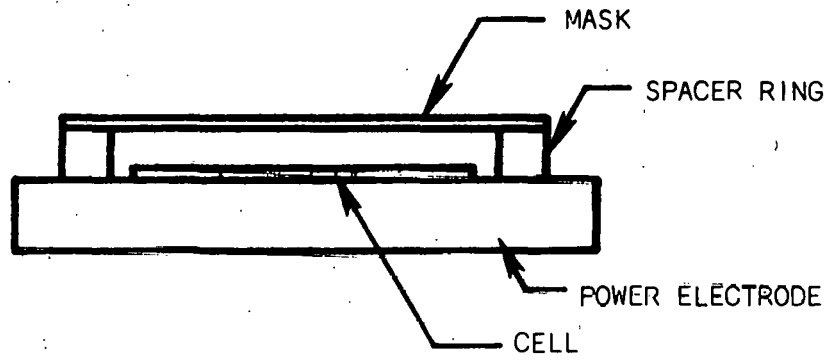


FIGURE 10
ETCH MASK CONFIGURATION

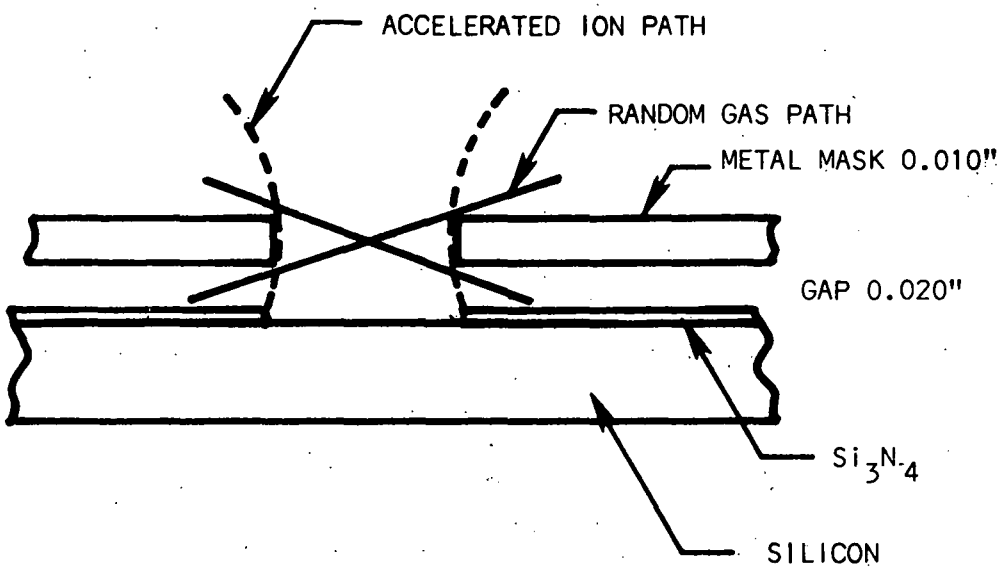


FIGURE 11

LINE DEFINITION FROM RANDOM GAS COLLISIONS AND ACCELERATED IONS.

Of major significance is the fact that the required pattern can be etched without intimate contact between the mask and cell surface. This implies that a double sided process is feasible and may be easily implimented. Also, the process can now be applied successfully to sheet substrates which may be less flat (and more fragile) than as-sawed, single crystal material.

The plasma reactor was further modified by adding another grounded electrode, and changing the power electrode to allow the substrate to be held between two metal masks, as illustrated in Figure 12. Using this new configuration, the silicon nitride layer is etched in CF_4 with 8.5% O_2, at 100 watts of RF power, and at a pressure of 0.1 Torr. The front side of the cell is placed face down on the bottom mask to obtain better resolution for the front pattern, while the back side has an approximately 0.010 inch spacing between the substrate and mask. The results were excellent, generating simultaneous patterns with sharp geometries equal to those previously generated one side at a time. Solar cells with efficiencies in excess of 14% (AM1) were fabricated using these simultaneously formed front and back ohmic patterns.

The masks used during these experiments were thicker than those used in the reported single side baseline process, i.e. 12 mils versus about 5 mils. Thicker masks are required to support the substrate, but have a limitation in the line width which can be formed using common etching techniques. Line-width on the 12 mil masks are 7 - 8 mils. At present this represents a major requirement in developing of a production-ready process, and efforts must be directed toward mask development technology.

A constraint of the equipment design used to demonstrate the advanced process was the low gas flow rate, when operating in the ion-enhanced pressure region near 0.1 Torr. This flow rate was difficult to control, causing some process control variations. Accordingly, the equipment required additional changes to increase vacuum pumping speed. After some modification,

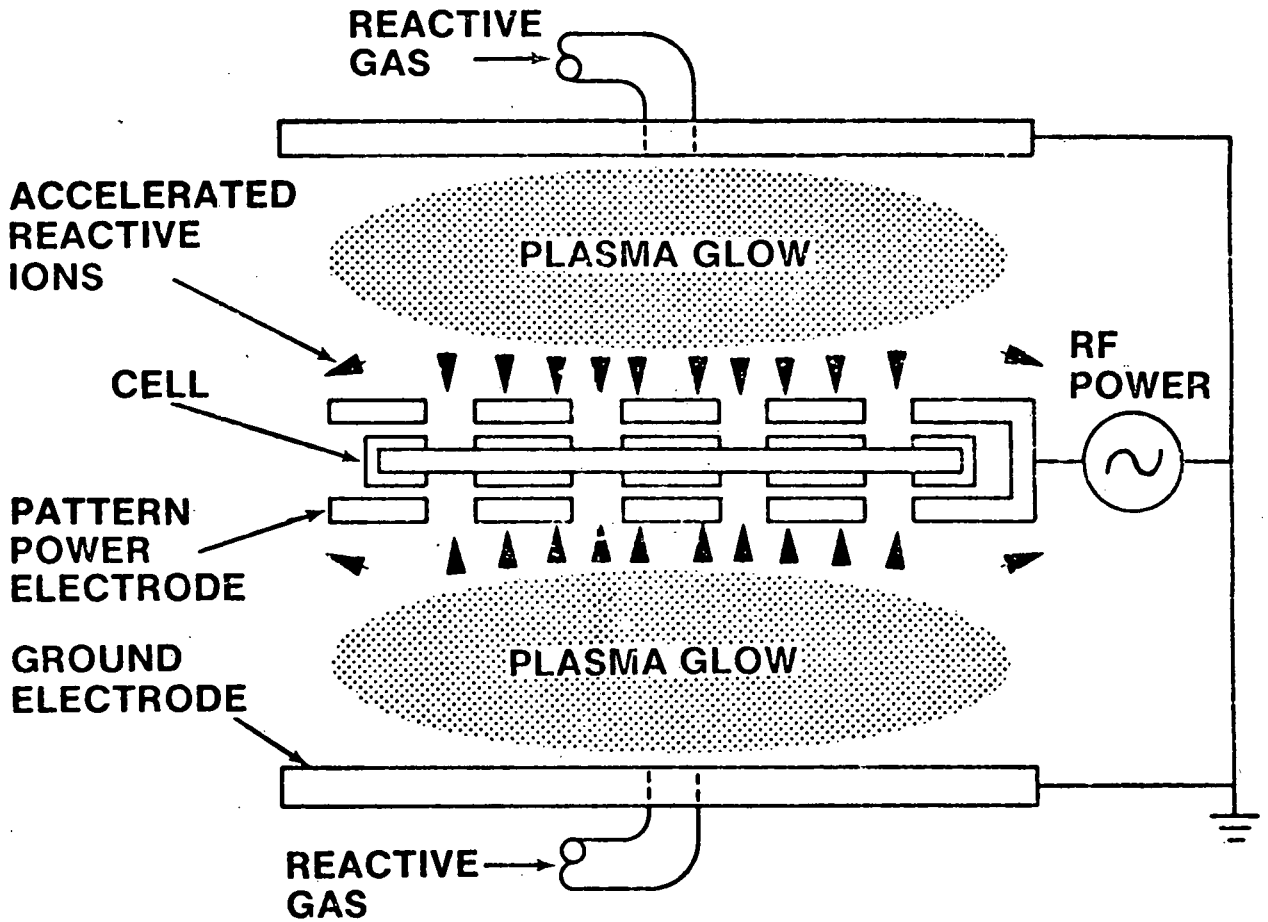


FIGURE 12: PLASMA ETCHING EQUIPMENT CONFIGURATION FOR THE SIMULTANEOUS ETCHING OF BOTH SIDES OF A SUBSTRATE.

an improvement was noted in maintaing stable gas flows in the 3 cm^3/minute range. However, this was still not totally adequate for a reproducible, efficient process.

Another limitation of that equipment is what can be generically called "wall effects". These include both vacuum variations and ion recombination effects due to the chamber's size and electrical interactions, since the chamber was itself an electrode at ground potential. "Wall effects" of that equipment physically limit the size of substrates that can be uniformily etched, the usable pressure range, and the etch rate. These effects were reduced by utilizing a more suitable equipment configuration; to this end, a unit designed as a parallel-plate development system was obtained as a replacement for the unit used for experiments to date. This unit is shown schematically in Figure 13.

The new unit uses a glass bell jar for the vacuum chamber; this eliminates the conductive ground surface near the electrodes. It also has a triple electrode configuration - an RF power electrode between two ground electrode plates, with gas inlets in all three. This is easily adaptable to simultaneous front and back pattern etching. The system's design allows higher pumping speeds of reactive gases and a lower residual gas level of 10^{-4} Torr. Also, larger rectangular electrodes, 4" x 10", offer the capability of handling ribbon substrates.

Tests were initiated in this new system. The results seemed more consistent with some improvement in uniformity. However, somewhat lower etch rates were experienced due to lower power density from increased electrode size.

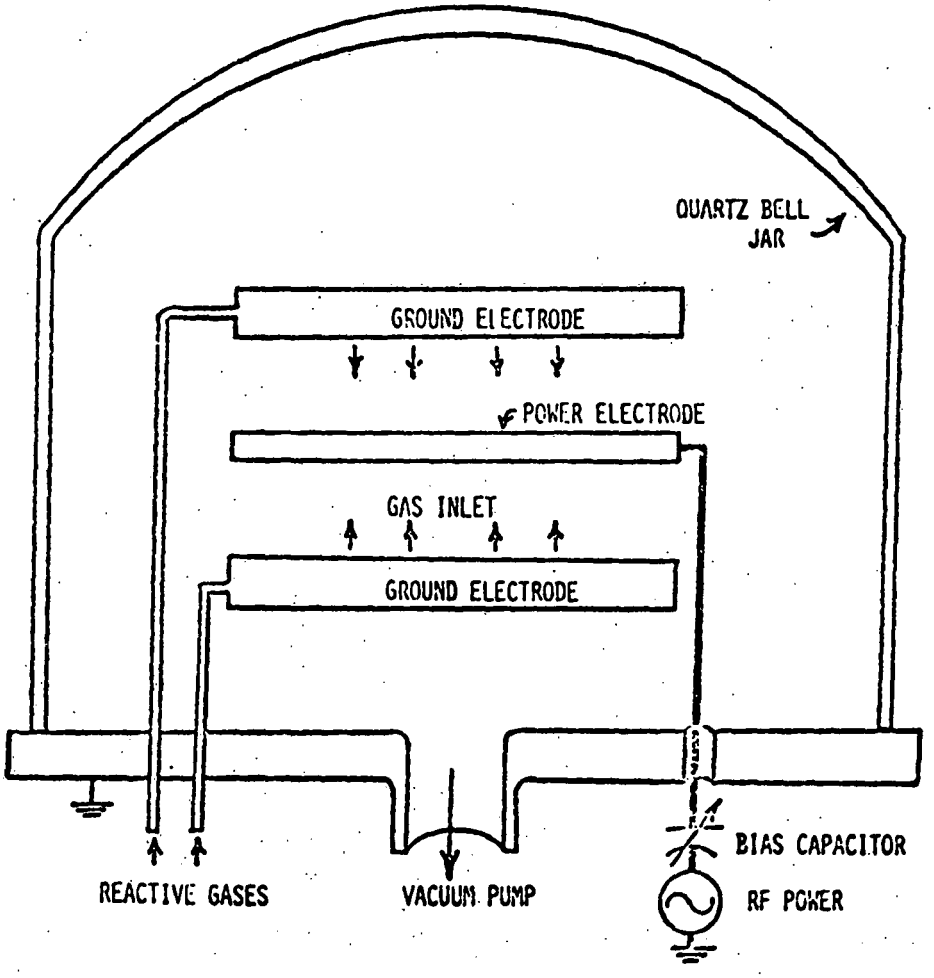


FIGURE 13

PARALLEL PLATE PLASMA CHAMBER

After preliminary evaluation of the new plasma equipment, however, a major and persistent problem developed. There is a mechanism whereby polymerization of the fluorocarbon ions competes with the etching silicon nitride. The polymerization effect varies from a slight reduction in the nitride etch rate to causing a secondary etch mechanism under the etch mask in areas which should not be etched. Under certain conditions, polymerization of the reactant gases totally replaced all etching. Although it had been observed on occasion in the previous equipment, it is more prevalent at the lower pressures. The gas phase effects are also easier to observe with the glass bell chamber. The polymerization phenomenon is believed to be related to the low flow rate or long residence time of the gases in the RF field and to the selection of reactor materials. Increasing the pumping conductance of the vacuum system and increasing the oxygen concentration significantly reduced the polymerization. Also, the electrode spacing was increased to reduce the confinement of the plasma dark space sheath at the lower pressure required for ion enhanced etching. Plasma confinement increases the reaction of the plasma with the electrode surfaces and concentrates the field within the plasma resulting in increased polymerization. These steps basically eliminated the gas phase reaction but nickel and molybdenum components such as used for etch masks were found to also cause surface polymerization. It is thought that since nickel and molybdenum form volatile fluorides that these may act to initiate polymerization. However aluminum and copper form nonvolatile fluorides and do not promote fluorocarbon polymerization. A recent published study (5) verifies these assumptions and gives a qualitative theory of the polymerization mechanism that is found in low-pressure, long-residence-time plasma systems used for ion enhanced etching. Polymerization no longer presents a significant control problem.

(5) J. W. Coburn and Eric Kay, "Some Chemical Aspect of Fluorocarbon Plasma Etching of Silicon and its Compounds", IBM Journal of Research and Development, Vol. 23, No. 1, January 1979.

Mechanically masked plasma patterning of silicon nitride layers on silicon solar cell substrates can now be considered to be a well established process. What can be considered fine linewidths for solar cell processing, i.e., 1 mil, has been demonstrated. Photomicrographs of specific etched examples are shown in Figures 14 through 16. Figure 14 is a photomicrograph of an exposed silicon grid line etched in silicon nitride AR film on a polished silicon surface. This is a portion of the preohmic plating mask routinely etched on 3 inch solar cells. Figure 15 is a photo of a sharp 1 mil line delineated using a resolution test pattern mask. An example of the resolution on textured silicon surface is shown in figure 16.

It must be noted that while the process is proven, extensive efforts are still required in both mask fabrication techniques and in automated equipment design.

3.2.2 PLASMA SILICON ETCHING

The sawing of large silicon cyrstals or ingots into thin substrates leaves the surface extensively damaged. This damage consists of chips, deep microcracks, and dislocation clusters. Recently, (6) the damage resulting from a Hamco ID saw has been described as 1 - 2 μm chips with large microcracks extending 10 to 15 μm below the surface. A somewhat thinner damage layer of 5 to 7 μm has been observed with Motorola's wire saw technique (7). A solar cell cannot be fabricated directly in such a loose, fractured surface layer. Usually a considerable amount of material is removed (20 - 30 μm) before fabrication. Even though the texture etch processes used in the Motorola

(6) T. S. Kalan, K. K. Shih, J. A. Van Vechten, and W. A. Westdorp, "Effect of Lubricant Environments on Saw Damage in Si Wafers," Journal of Electrochemical Society, Vol. 127, June 1980.

(7) B. L. Sopori, "A Rapid Non-Destructive Technique for Monitoring Polishing Damage in Semiconductor Wafers," To be published in Journal of Applied Physics: Doe Contract No. AC-02-79ET-23104.

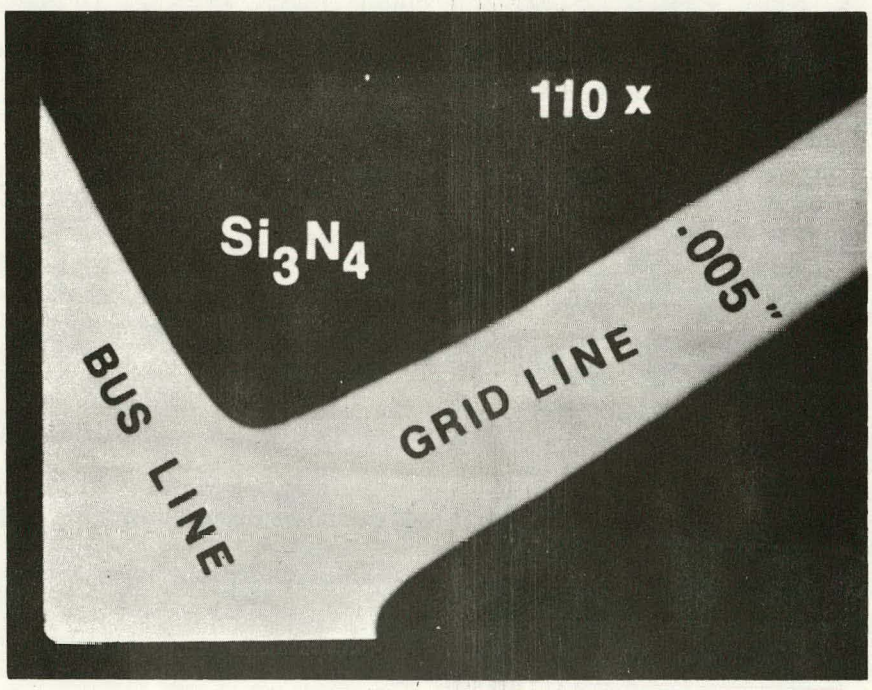


FIGURE 14: PHOTOMICROGRAPH OF 5 MIL ETCHED GRID LINE AT 110X.

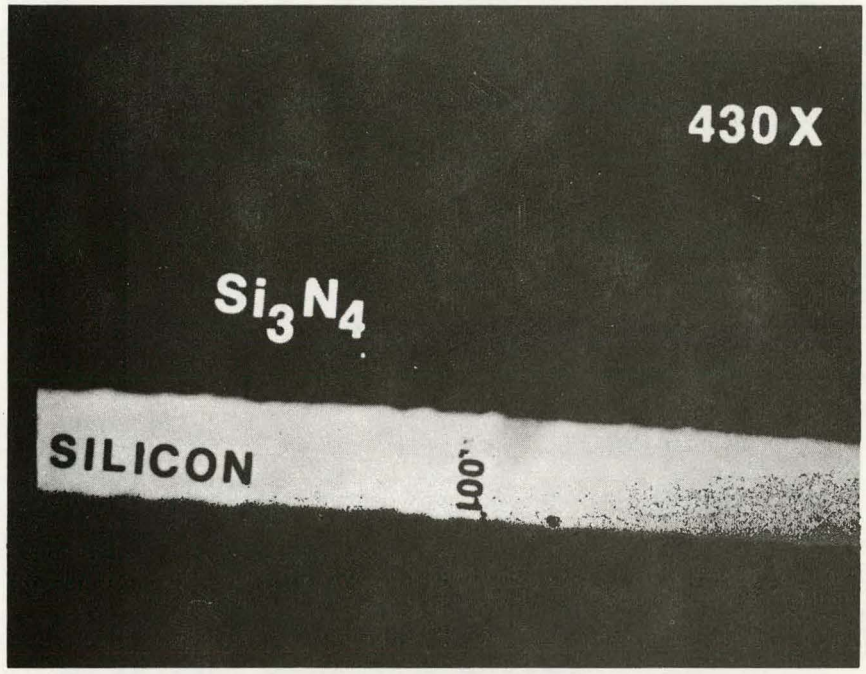


FIGURE 15: PHOTOMICROGRAPH OF A 1 MIL ETCHED GRID LINE AT 430X.

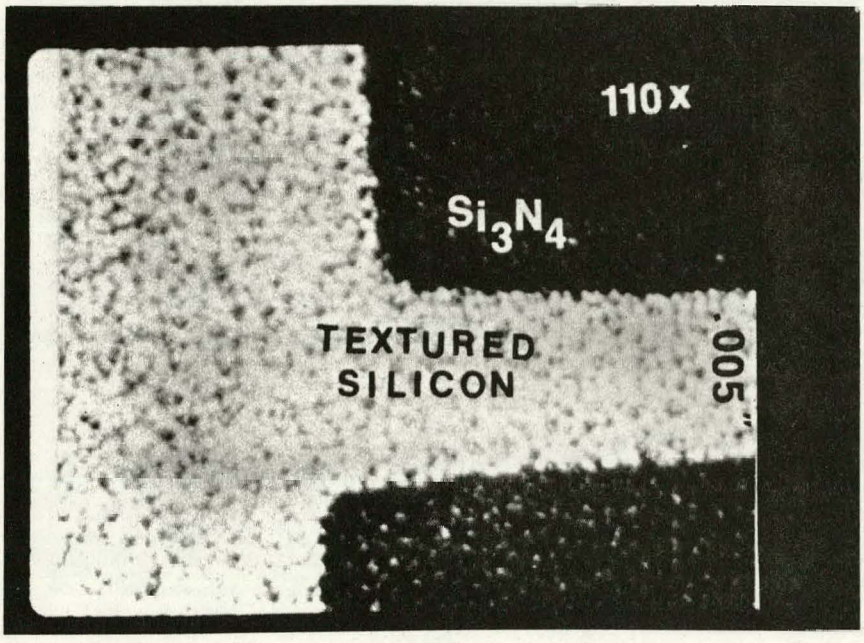


FIGURE 16: PHOTOMICROGRAPH OF A 6 MIL ETCHED GRID LINE ON TEXTURED SURFACE AT 110X.

sequence removes a considerable amount of silicon, most of the worst damaged layer must still be removed. If not removed, the damaged layer can result in texture non-uniformities in peak heights, increases the time required to obtain desired texturing and effects etch bath control and life. More importantly, some electrical degradation may be contributed to not removing some saw damage before texture etching.

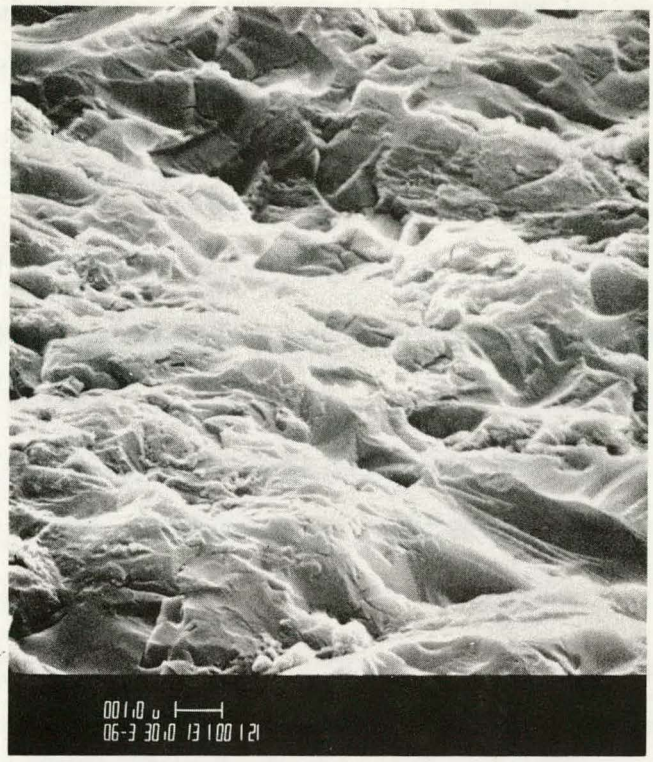
Plasma chemical etching of silicon can be divided into two major processing categories whose different properties are determined by the equipment configuration. These are a volume loading process and a surface loading process. The volume loading process uses a barrel type reactor in which the plasma is formed around the chamber wall and the etchant species diffuse into the substrates at the core. Thus, the silicon is etched by a gas containing active species, usually atomic fluorine. In the surface loading process, the substrates lie on one of two electrodes between which a plasma glow is generated. This provides etching from active atomic species and ions but only on the exposed surface. (Both processes were investigated to determine operational and cost effectiveness for plasma etching of silicon saw damage.)

The barrel type reactor was evaluated first since its large batch substrate processing and relatively low equipment cost made it a likely cost effective choice. The equipment used was a Tegal Model 421, typical of the type used extensively in semiconductor processing. Using CF_4 and O_2 reactant gas mixture, etch rates of over 3,000 Å/min. were attainable. However, attempting to remove silicon from both sides of a large number of substrates greatly reduced the achievable etch rate due to the volume loading effects on the reactant species concentration. As the silicon area increases the etch rate decreases since the species production rate remains fixed with constant pressure and RF power. There is a finite limit of reactant species generation due to the

power limit of the system design, and reactant species lifetime decreases as the pressure is increased. Besides reducing the etch rate, the closer substrate spacing with large batch carriers introduced etch non-uniformity across the substrates. Since the reactant gas diffuses from the edge to the center of the substrate, there can be a substantial decrease in etch rate near the center due again to reactant depletion. This can be improved by increasing the spacing (reduced loading) and by lowering the pressure. An additional observation of concern was that the plasma chemistry preferentially etches the larger microcracks as shown in the SEM micrographs in Figure 17. These can adversely effect the texture etch peak height uniformity or cause additional problems even if a texture etch is not used.

The maximum etch rates obtained were 600 to 800 Å/min. using a reduced wafer loading of 50 - 3" wafers at a pressure of slightly less than 1 Torr and 250 watts of RF power. This is higher than has been reported for integrated circuit etching applications. This improvement was due to vacuum pumping changes and increased temperature. This rate is far too slow to make this technique economical for bulk silicon etching. For example, at 800Å/min., it requires over 60 minutes to etch the minimum of 5 μm on 50 - 3" wafers. The volume flow nature of this process also requires considerable amounts of carbon tetrafluoride gas.

The parallel plate or planar reactor configuration was evaluated next. This process is surface area dependent since the substrates lie on one of the RF electrode plates. There is not the etch rate reduction due to reactant species due to recombination before reaching the substrates since they are in the plasma discharge. Both neutral and ionic species can effect the etching rate within the discharge. The etch rate is therefore much higher in the planar reactor. Gas usage is more efficient and the equipment is more easily automated than the barrel configuration.



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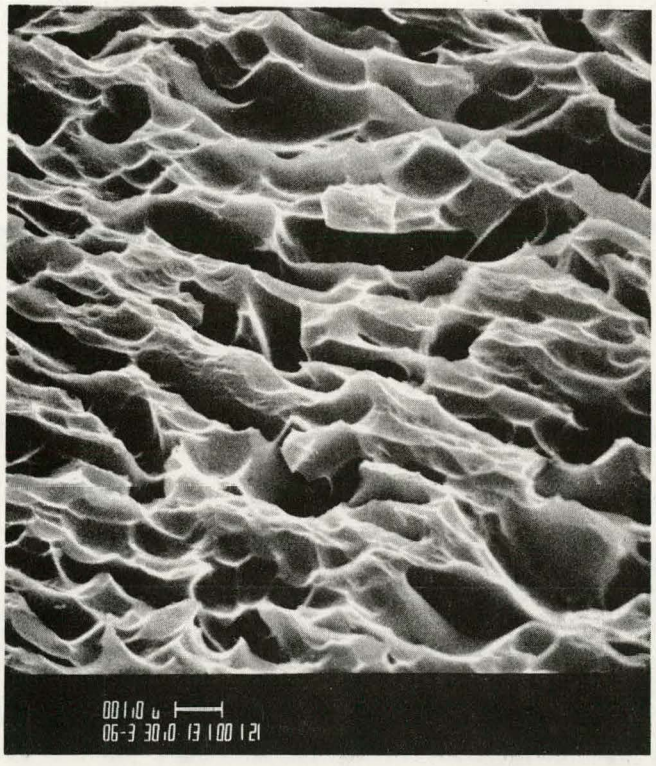

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FIGURE 17: SEM MICROGRAPHS OF (A) WIRE SAW DAMAGED SURFACE AND (B) CF_4 PLASMA ETCHED SURFACE IN A BARREL TYPE REACTOR. NOTE DEEP ETCH GROOVES.

The equipment used in the evaluation was a modified barrel system equipped with parallel plate electrodes which was also used for the initial plasma patterning work. The etch rates were determined by weight loss and substrate thickness measurement. Etch rates of 5,000 Å/min. were obtained at 1 Torr and 300 watts of RF power. Using the small electrode, there was good etch uniformity across the substrate. There was, further, no preferential etching of larger microcracks as seen in the barrel reactor probably because the reaction mechanism is controlled by surface collisions. In fact, the surface appears to be very similar to those obtained using wet chemistry etching except for smaller features.

To evaluate loading effects and operational scale equipment, multiple wafers were etched on a larger parallel plate reactor. This unit was also equipped with an atomic fluorine emission detector. Since silicon etch rate is determined by atomic fluorine, the emission intensity of the plasma can be used to optimize the reactor parameters. The loading effects were found to be less complex (two dimensional) and less severe due to reduced wall effects with this process. The results were very good with etch rates over 1.2 µm/min. for small axial loading to 0.8 µm/min. for fully loaded conditions. Uniformity was more than adequate for this process (>5%) with no apparent difficulties. Consistent etch rates of 1 µm/min. should be a reasonable performance limit using slightly higher power density and recent developments in gas distribution to compensate for loading effects by several equipment suppliers.

Based on a 1 µm/min. etch rate, this process is of questionable cost-effectiveness for saw damage removal. Assuming that a 10 µm must be removed to ensure all damage removal, the throughput, equipment cost, and gas consumption be approximated to cost about 0.75 cents per watt per side. This is not competitive with alkaline wet chemical etching to remove a

comperable thickness. If a greater thickness of damage removal is required, plasma etching becomes even less attractive. This method does, however, appear to be cost-effective for removing thin (less than 1.0 μm) on direct grown sheet material such as RTR or EFG ribbons, if this proves to be necessary.

3.2.3 TEXTURE ETCHING AND BACK SURFACE TRANSMISSION

In the process of wet chemical texture etching, both the front and back side of the substrate will texture unless an effort is made to mask the back side with either a dielectric (SiO_2, Si_3N_4) or a screened wax. This mask must then be removed before further processing. Plasma texturing, with mechanical masking of one side, can be envisioned as a technique for texturing only one side of the substrate. The advantage of texturing the front side only is that as the light which is refracted at the textured front surface reaches a non-textured back, total internal reflection will take place. The increase in short circuit current that this affords (for a patterned back cell) must be weighted against that additional processing expense of the back protection and stripping steps or the cost of plasma texturing.

An experiment was performed to measure the actual amount of increase in transmission through Si wafers which were given wet texturing of both front and back as compared to only front texturing. In the experiment, a high efficiency silicon solar cell was used as an optical detector. The edges of the detector were covered with a mask to prevent stray light or scattered room light from striking the cell. The experimental wafer was then placed directly over the detector. An ENH quartzline lamp was then used as a light source. The geometry of this appratus is shown in Figure 18. By using a high efficiency silicon solar cell as the detector of light

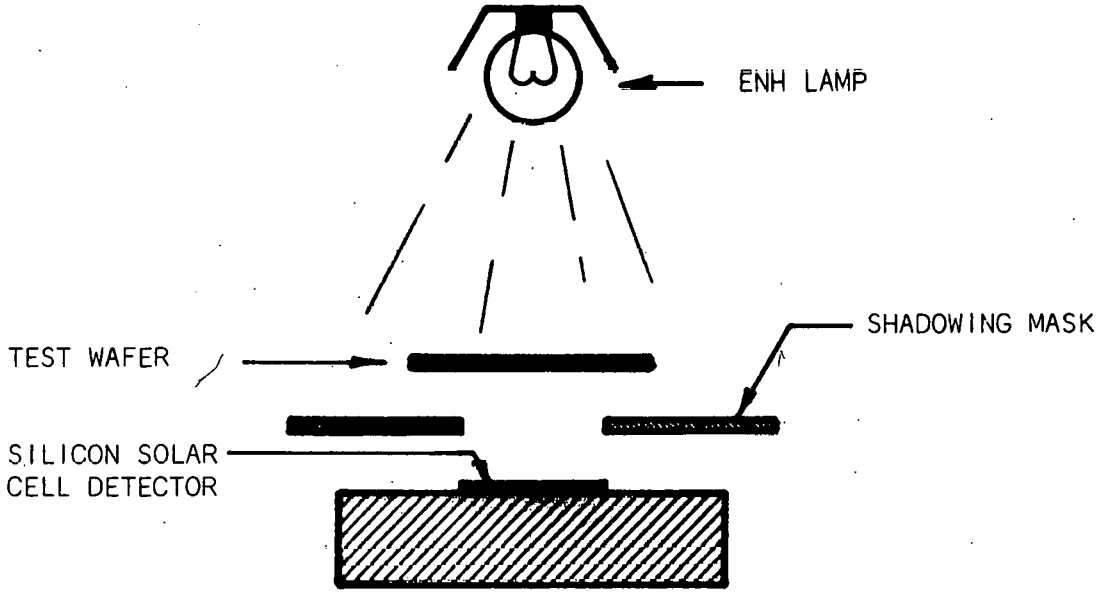

FIGURE 18: SCHEMATIC DRAWING OF TEST APPARATUS FOR TRANSMISSION EXPERIMENTS.

transmitted through two wafers, one textured front and back and one textured on the front only, an accurate measure of useful transmitted light (i.e. .400μm $\leq \lambda \leq$ 1.1μm) can be obtained.

It was found that for 20 mil (500μm) thick wafers, the wafer that was textured front and back transmitted more than 3 (3.24) times the useable incident light, but the actual magnitude of the transmission would result in only 0.175% loss in J_{SC}, compared to a loss of 0.054% for the polished back case. For the thinner, more practical case of 7.6 (190μm) mil wafers, the ratio of transmitted light is, to first order, the same, but the magnitude is much larger because, of course, more light remains to be absorbed after 7.6 mil (190μm) penetration than after 20 mils (500μm). Empirically, the loss in J_{SC} increases from 0.054% (for 20 mil, front textured, back polished) to 0.18% for 7.6 mil. The loss for the textured front and back increases from 0.17% (20 mil) to 0.65% (7.6 mil). In all cases, no front or back metal was on the test wafer, making the observed amount of transmitted light greater than for an actual cell.

Thus, for the thinner wafer, the much simpler texturing of both sides of the wafer results in a reduction of J_{SC} of 0.65%. Since such a small change in J_{SC} will have no measurable effect on V_{OC} or the fill factor, the overall reduction in conversion efficiency will be by the same factor, essentially reducing a 15.00% cell to a 14.90% cell. At a cost of $0.70/watt, this amounts to an increase in cost of 0.46 cents/watt. The cost of protecting the back side from texturing, either by masking or by plasma texturing must not exceed this cost.

The above analysis is a worst case condition. This is because of two assumptions made, namely; all of the light that is totally internally reflected by the one sided textured sample will be fully absorbed; and that none

of the light transmitted through the two sided textured sample is reflected back into the cell by the back of the module.

The second assumption deserves further comment. Because the back side has a patterned metallization, a patterned Si_3N_4 coating is present as a plating mask. The Si_3N_4 thickness is the same as that on the front, textured surface where it serves as an antireflective coating. It will serve exactly the same way for light which, having been transmitted through the cell, is now redirected onto the back surface from any reflective backing utilized in the module. This implies that the above discussion of losses is overestimated, and that the actual reduction in efficiency due to front and back texturing may be negligible once the cell is properly encapsulated.

3.2.4 PLASMA TEXTURE ETCHING

Texture-etched like surfaces on silicon have been achieved in a conventional plasma etching system. Demonstration of this process was performed on ribbon-to-ribbon (RTR) material grown internally at Motorola.

Texture etching of polycrystalline silicon materials occurs readily. In the case of polycrystalline materials, as in the case of single crystal wafers, the (111) crystal surfaces are left, forming pyramidial shapes. In the case of polycrystalline materials, however, these pyramids are not normal to the surface, as they would be on a (100) single crystal substrate, but are rotated to one side depending on the orientation of the grain in which they exist. A SEM photomicrograph of a texture etched RTR sample, etched by conventional wet chemistry techniques is shown in Figure 19.

In contrast, SEM photomicrographs of a plasma "texture etched" sample are shown in Figures 20 and 21. These were etched in a CF_4-O_2 (8%) plasma in a barrel type reactor. The total etch time was about 30 minutes.

FIGURE 19: SEM PHOTOMICROGRAPH OF A TEXTURED RTR SAMPLE ETCHED BY WET CHEMISTRY AND SHOWING A GRAIN BOUNDARY.

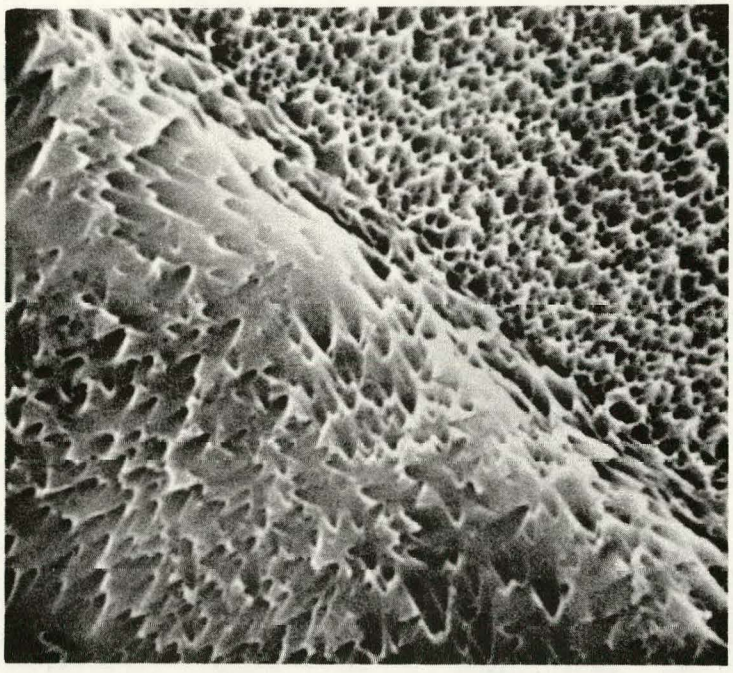

FIGURE 20: SEM PHOTOMICROGRAPH OF A PLASMA TEXTURED RTR POLYCRYSTALLINE AREA.

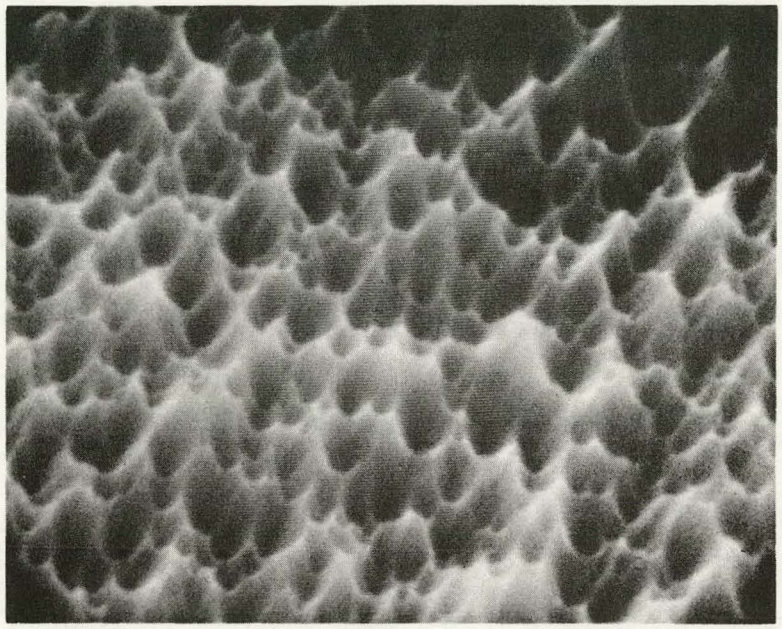

FIGURE 21: SEM PHOTOMICROGRAPH AT GREATER MAGNIFICATION OF ONE AREA SHOWN IN PREVIOUS FIGURE.

The geometrical shape of the plasma textured surfaces is not as sharp as that formed by wet chemistry and can be described more accurately as an egg-carton type geometry. This shape is extremely attractive as an effective light trap, but appears to be much more fragile and susceptible to peak breakage. Further, the geometry may present problems in ion implantation, perhaps causing localized shadowing.

In order to achieve the anisotropic etching, the etch conditions were changed from attempts at plasma etching saw damage removal. The gas flow and pressure must be reduced to allow a much slower etch rate. These conditions would be necessary regardless of the reactor geometry or type. It is concluded, thus, that the low throughput and high equipment cost preclude the use of plasma texture etching. Further, based on the discussion in the previous section, one sided texturing is not critical from a cell (module) efficiency standpoint.

3.3 METALLIZATION

At the present time, two techniques for forming metal contact on solar cells remain potentially viable from both cost and technical considerations: plating and printing (silk screening). The plated metal process has now shown distinct advantages over the printed process.

The Pd_2Si - (Pd) - Ni - solder metallization system for silicon solar cells has been developed at Motorola. This system can be considered the baseline system which all other competing systems must strive to outperform. A full description of the Pd_2Si-(Pd)-Ni-solder metallization is available in another report (8).

(8) R. A. Pryor, DOE/JPL Report No. 954689-78/4, "Metallization of Large Silicon Wafers, Final Report for JPL Contract No. 954689 (1978).

Several developments in plated metallization were studied simultaneously for this contract. Using the palladium-nickel-solder metal system developed under JPL Contract No. 954689 as a baseline process, new procedures were generated to substitute copper for solder as the conductive layer and to eliminate the use of the relatively thick and expensive electroless palladium for the silicon contact layer. The thin immersion palladium, however, may be retained.

3.3.1 NICKEL PLATING

In the past, experiments attempting to plate electroless nickel directly to silicon using the usual ammonia-based nickel chloride bath have yielded inconsistent, and therefore unsuccessful, results. In some instances, excellent bond strength and contact resistance would be obtained, while in some others, contact strength would be totally inadequate. The primary reason for inconsistent contact performance was a tendency for the plating bath to produce an oxide interface layer on the silicon surface faster than it produced a plated nickel layer. This oxide interfacial layer prevented the effective (and controllable) nickel silicide formation needed for adherence.

The interfacial oxide problem was solved in the baseline (PNS) process by using immersion and electroless plated palladium layers, but the electroless palladium layer contributes a significant cost to the process. Experiments have been initiated to eliminate the electroless palladium plating step in the PNS process, using only an immersion palladium silicon surface preparation followed by the electroless nickel deposition. While this has been readily performed with the original nickel bath, it has not yet resulted in consistently satisfactory nickel layer adhesion. It seems that the same oxidizing effects may be present whether the specified nickel solution is

used on bare silicon or on silicon sparsely coated with palladium from an immersion solution.

The direct use of nickel and nickel-silicide ohmic contact layers have been re-evaluated. In fact, it has been discovered that consistently strong nickel contacts can be obtained after heat treatment of nickel layers formed directly on the silicon surface by electroplating. Apparently this is possible because of the differences between the behavior of the alkaline electroless nickel bath specified in the PNS process and the acid electrolytic nickel bath used in the present experiments. The nickel layer produced by the alkaline electroless bath is the nickel-phosphorus mixture, containing a few percent phosphorus, while the layer produced by the acid electrolytic bath is essentially pure nickel with no component of phosphorus. Moreover, in directly plating the nickel layer onto silicon with the electrolytic nickel process, there appears to be no tendency to form an interfacial oxide. Thus, the nickel is in intimate contact with the silicon surface. The result is to allow the controllable formation of a very adherent nickel-silicide layer (Ni_2Si) at very low temperatures (250 - 300°C) and in time intervals of 15 - 60 minutes.

Experiments were conducted using a commercial electrolytic nickel bath. A formulation based on nickel sulfamate was chosen because this chemistry is widely recognized as providing nickel deposits with very low internal stress. Low stress is important for building reasonable deposit thickness without generating adhesion problems before nickel silicide formation and for not imparting stress to the silicon crystal lattice near the junction (which could degrade current-voltage characteristics of a solar cell).

The electrolytic nickel plating solutions were prepared from nickel sulfamate solutions manufactured by Allied-Kelite of Des Plaines, Illinois. Instructions for preparing and using the plating solutions were obtained from

technical data sheets for the "Barrett Sulfamate Nickel Plating Process, Type SN'. The basic formula for the Barrett SN solution is 76.5 g/ℓ of nickel metal in the form of nickel sulfamate plus 30 g/ℓ of boric acid. The nickel metal content is supplied by Barrett Sulfamate Nickel Replensiher Solution, Type SNR-24, which contains 180 g/ℓ of nickel metal. Other solution additives such as an anode corrosion chemical (Barrett Additive "A" , 3 g/ℓ) and an anti-pit agent (Barrett SNAP, 0.4 g/ℓ) may be used (but were not used for most of the experimental studies). Optimum operating parameters given for the Barrett SN process include a bath temperature of 49°C, solution pH of 4.0, tank voltage between 6 and 12 volts, and cathode current density between 10 and 20 mA/cm^2. Typical 3 inch diameter solar cells with patterned front metal and solid back metal have an exposed area of about 50 cm^2. Therefore, cathode currents of about 0.5 to 1.0A were actually used.

Experiments with electrolytic nickel were performed with the plating solution contained in quartz beakers on top of magnetic stirring hotplates. A sulfur depolarized nickel anode was used. Plating voltage and current were supplied with a standard regulated power supply, and typical plating times ranged between 1 and 10 minutes.

It was determined that for at least some solar cell structures, nickel plating could be initiated directly on the exposed silicon front and back surfaces with no pretreatment other than a dilute hydrofluoric acid (e.g., 10:1 H_2O:HF or 50:1 H_2O:HF) rinse to ensure oxide-free silicon surfaces. In performing the electrolytic nickel plating process, no tendency to form oxide interfaces between the silicon and nickel was observed. This is probably the major reason for the excellent adhesion obtained with nickel layers which have been deposited with this bath (and subsequently heat-treated). Such layers, after treatments of as little as 15 minutes at 300°C, have passed the requirement that vertical pull-test failure occur by silicon substrate fracture. Moreover,

the process of applying the nickel layer and forming the nickel silicide contact does not degrade solar cell electrical performance.

There are, however, some precautions to be noted before the successful production-ready development of electrolytically plated nickel contacts is completed. First, the plating process is dependent on solar cell structure since electrolytic plating performance depends very much on silicon surface conductivity. Therefore, cells with both a front surface diffusion and a back surface enhancement will adapt more readily to the electrolytic process than cells with no back surface layer. Secondly, electrolytic processing requires electrical contact to the solar cell so that it may be made cathodic. The proper fixturing required to make effective electrical contact to the bare silicon of the solar cell, and yet not shadow the cell or rob current from the cell, is not a trivial design problem and may require a fair amound of engineering development.

A potential drawback, thus, of electrolytic nickel plating to bare silicon may be the requirement of careful attention to the fixturing and jigging arrangements which provide electrical contact to the cathodic solar cell. Because of the fixturing complexity (especially associated with the electroplating of bare silicon), it would be desirable to use an electroless nickel bath to form the silicon contact layer. Thus, a re-evaluation of electroless nickel solutions was undertaken.

Electroless nickel solutions routinely used by the semiconductor industry for plating silicon usually consist of nickel chloride and a sodium hypophosphite reducing agent in an ammonical bath maintained at proper pH by excess amounts of ammonium hydroxide. A complexer such as sodium citrate is also used. From past investigation of electroless nickel solutions, it appears that a basic, high pH solution is required to effectively plate silicon. Therefore, in

re-evaluating the direct use of electroless nickel, chemistries were considered which were alkaline in nature but which used substantially different solution components. Baths using nickel sulfate rather than nickel chloride were prepared. The amount of ammonium hydroxide required for pH control was reduced. Sodium pyrophosphate was used as a complexing agent. Both sodium hypophosphite and dimethylamine borane were considered for reducing agents. In general, no substantial difference was noted between the phosphorus reducing agent and the boron reducing agent with respect to plating silicon solar cells. Hence the less expensive sodium hypophosphite was chosen for further experimentation. The formula used for further experiments is given in Table 6.

The performance of this electroless nickel chemistry has been studied by Schwartz (9) and Feldstein (10) for applications other than silicon plating. However, this solution has proven to give excellent performance when used at moderate temperatures (50°C - 70°C) to plate silicon. Direct plating can be initiated in a matter of seconds on clean, heavily or lightly doped n-type silicon, or on lightly doped p-type silicon. Some difficulty which has not yet been resolved occurs when trying to plate heavily doped p-type silicon, such as a BSF layer for an n+pp+ solar cell.

To circumvent such difficulties, and to introduce a uniform, repetitive plating situation, a surface pre-treatment has been employed to prepare the p+ and n+ silicon surfaces for simultaneous nickel plating. The pre-treatment consists of a short (2-4 min.) immersion in a dilute palladium chloride solution which deposits a very thin and adherent palladium film on all exposed silicon. This film need not be continuous but is dense enough to effectively catalyze the subsequent electroless nickel deposition. The

(9) M. Schwartz, Proc. Am. Electroplat. Soc., 47, 176 (1969).

(10) N. Feldstein, RCA Review, 31, (2), 317 (1970).

TABLE 6

ELECTROLESS NICKEL FORMULATION USING NICKEL SULFATE

REAGENT	CONCENTRATION
Nickel Sulfate ($NiSO_4 \cdot 6H_2O$)	25 g/ℓ
Sodium Pyrophosphate ($Na_4P_2O_7 \cdot 10H_2O$)	50 g/ℓ
Ammonium Hydroxide (58% NH_4OH)	22 ml/ℓ
Sodium Hypophosphite ($NaH_2PO_2 \cdot H_2O$)	25 g/ℓ

immersion palladium solution has been described in other Motorola reports and consists of palladium chloride in a dilute, aqueous ammonium fluoride solution.

After palladium sensitization and water rinsing, the solar cell is plated in the sulfate electroless nickel solution for about 4 minutes. This is sufficient to obtain a nickel contact layer on the order of 5000 Å thick. With this electroless nickel chemistry, no tendancy to oxidize the silicon surface has ever been observed. The result is a nickel layer (with a very small percentage of palladium) which is in intimate contact with the silicon surface. This assertion is born out by the fact that very low temperatures (250°C) are sufficient to react the nickel-silicon interface to form nickel silicide (Ni_2Si), thus obtaining strong metal contact adherence. Such rapid silicide formation at low temperatures is in agreement with studies found in the technical literature where vacuum deposited nickel layers are formed on freshly cleaned silicon surfaces. As much as 400 - 500 Å of nickel silicide can be expected after heat treatment at 250°C for 60 minutes (11).

3.3.2 COPPER AS AN ECONOMICAL CONDUCTOR LAYER

The minimum cost achievable for any metallization system is limited by the cost of component materials. All printed metallization systems which have been satisfactorily utilized with solar cell structures (for contact to the shallow junction areas) are based on silver as the primary conductor. No printable base metal system has been reported to be satisfactory for utilization on solar cells. The Motorola plated metal system, discussed above, utilizes solder as the primary conductor. While solder can be broadly classed as a base-metal, it is relatively expensive. A conductor layer material such as copper would be much cheaper.

(11) K. N. Tu, W. K. Chu, and J. W. Mayer, Thin Solid Films, 25, 403 (1975).

Some pertinent properties of potential conductor layer materials are presented in Table 7. Two important observations can be made. First, the conductivities of silver and copper are comparable, while solder is a relatively poor conductor. Second, in order to achieve a given conductivity for any given conductor geometry, 11% more silver, and over 800% more solder, (by weight), would be required compared to copper.

The cost of metals varies significantly as a function of time in a manner determined more by supply and demand factors than by inflation. For the basis of this discussion, the prices for the three metals were identified on March 29, 1979 and are presented in Table 8. On a weight basis, copper is significantly cheaper than solder and less than 1% of the cost of silver.

When the cost per pound of a metal is correlated with the weight requirement for a unit conductivity, the cost of a metal as a conductor can be determined. Utilizing the 3-29-79 prices, solder is about 40 times as expensive as copper, while silver is about 115 times as expensive as copper. During 1979 and 1980, metals prices varied wildly. Silver prices rose by an order of magnitude, while copper prices rose less than 50%. Subsequently, prices have decreased but copper has held even greater cost advantages over silver and solder than indicated by the prices above. On a cost basis, thus, copper is extremely attractive as the primary conductor metal on solar cells.

3.3.3 COPPER-SILICON INTERDIFFUSION

Any solar cell metallization for terrestrial applications must, in addition to being sufficiently economical, provide both excellent electrical performance and ensure reliability under actual operating conditions. Numerous candidates exist which will provide suitable electrical performance, but which fail the reliability criterion. In order to perform reliably, the solar cell

TABLE 7

COMPARISON OF SELECTED PROPERTIES OF METAL CONDUCTOR LAYERS

	SOLDER (60SN-40PB)	COPPER	SILVER
RESISTIVITY (Micro Ohm-cm)	14.5	1.673	1.59
DENSITY (g/cm^3)	8.53	8.96	10.49
RELATIVE WEIGHT PER UNIT CONDUCTIVITY	8.26	1.0	1.11

TABLE 8

COST* OF CONDUCTOR METALS ON MARCH 29, 1979

	SOLDER** (60SN-40PB)	COPPER	SILVER
COST PER POUND	4.67	1.00	104.22

*BASED ON PURE METAL COMPONENT COSTS

**DOES NOT INCLUDE ALLOY FORMATION COSTS

metallization must both maintain excellent adherence to the solar cell and, at the same time, not contribute to degradation of the electrical characteristics.

A severe criterion would be that the only satisfactory adherence test of a metallization system for solar cells is a mechanical pull-test which shows no separation of metal layers and which guarantees that separation of the metal from the cell is accomplished by silicon fracture. (Motorola's palladium silicide-nickel-solder metallization system satisfies this criterion.)

During operation, for a minimum of a 20 year life, the metallization must not contribute to a significant loss in output power from the solar cells. Such a loss could occur either from an increased series resistance, due to such phoenomenona as corrosion or metal migration, or from degradation of the silicon cell behavior, such as could occur by diffusion of the metal into the silicon. Diffusion of metal into the silicon could cause degradation of minority carrier lifetime in the silicon, decreasing cell efficiency. From all tests performed to date, the Pd_2Si-(Pd)-Ni-solder system appears suitable from these standpoints.

The substitution of copper for solder as the primary conductor layer in the metallization system would result in substantial materials cost savings. Substitution of copper for solder should have no impact on metal adhesion, but copper can have a degrading effect on cell electrical performance if it accumulates near the p-n junction.

The diffusion of copper in silicon is extremely rapid at low temperatures. While copper present in silicon before device processing can be gettered or precipitated (12) copper penetration following any high temperature processing,

(12) A. M. Salama, "The Effects of Copper and Titanium on Silicon Solar Cells," The Conference REdord of the Thirteenth IEEE Photovoltaic Specialists Conference - 1978, p. 496, 1978.

such as from cell metallization, can significantly degrade cell efficiency (13).

Diffusion kinetics can generally be described by an Arrhenius type relation,

$$D = D_o e^{-\frac{Q}{RT}}$$

where D is the diffusion coefficient, D_o is the pre-exponential or frequency factor, Q is the activation energy, T is absolute temperature, and R is the gas constant. The penetration of a limited amount of impurity into another species at one temperature can be approximated by a gaussian distribution

$$C = C_o e^{-\frac{x^2}{nDt}}$$

where C is the concentration of the impurity at distance x, C_o is the surface concentration, D is the diffusion coefficient, t is the time of the diffusion, and n is a constant determined by the diffusion geometry. On the other hand, if the source of impurity is infinite, penetration is described by

$$C = C_o \text{ erf } \frac{x}{\sqrt{nDt}} .$$

A measure of impurity penetration for either case can be taken as the distance $\sqrt{Dt}$. Further, at a distance of 10 $\sqrt{Dt}$, vanishingly small amounts of the impurity will be found. A suitable diffusion barrier, thus, has a thickness of at least 10 $\sqrt{Dt}$.

In operation, the solar cell will be subjected only to maximum temperatures near 100°C. Unfortunately, no diffusion data exist for copper in silicon for this temperature range, requiring extrapolation from higher temperature data. Such an extrapolation, however, does not appear unreasonable.

(13) T. Daud and K. M. Koliwad, "Effect of Copper Impurity on Polycrystalline Silicon Solar Cells," Ibid, p. 503.

Diffusion of copper in silicon has been studied for the temperature range of 400°C (14). These data are approximately reproduced in Figure 22 and extrapolated to the lower temperatures of interest. From this figure, diffusion coefficients for copper in silicon in the range of 50°C to 120°C have been determined and are shown in Table 9. These data have been utilized to calculate the distance $\sqrt{Dt}$ for copper in silicon at these temperatures for a time of 20 years, Table 10 for copper in silicon at these temperatures for a time of 20 years, Table 10. These distances are on the order of 1 cm in this time-frame, a distance which virtually ensures copper throughout a silicon solar cell operating for 20 years. Thus, cell degradation is virtually ensured during the required operating life if copper is allowed direct contact to silicon.

It is apparent, thus, that a barrier to copper diffusion into silicon is required to ensure cell reliability. Nickel appears to be ideal for this purpose. Diffusion data for copper and nickel have been compiled (15), and representative data are presented in Table 11. Again, extrapolation of high temperature diffusion data is required. Both copper and nickel exhibit complete mutual solid solubility, and both have face-centered-cubic crystal structures. Extrapolation of diffusion data for face-centered-cubic materials over large temperature ranges has proven satisfactory due to the extreme dominance of diffusion by a single vacancy mechanism in these materials. The extrapolation is primarily dependent upon the accuracy of the high temperature data.

The diffusion data for copper and nickel, shown in Table 11, are reasonably self-consistent. There is, however, sufficient scatter to make precise extrapolations unreliable. Precise diffusion distances are not

(14) R. M. Hall, et. al., Final Report, AFCRL Report 62-533, Contract AF 19 (604)-6623, May, 1962, as quoted in Fundamentals of Silicon Integrated Device Technology, Volume 1, Oxidation, Diffusion, and Epitaxy, Edited by R. M. Burger and R. P. Donovan, p. 235, 1967.

(15) John Askill, Tracer DiffusionData for Metals, Alloys, and Simple Oxides, 1979.

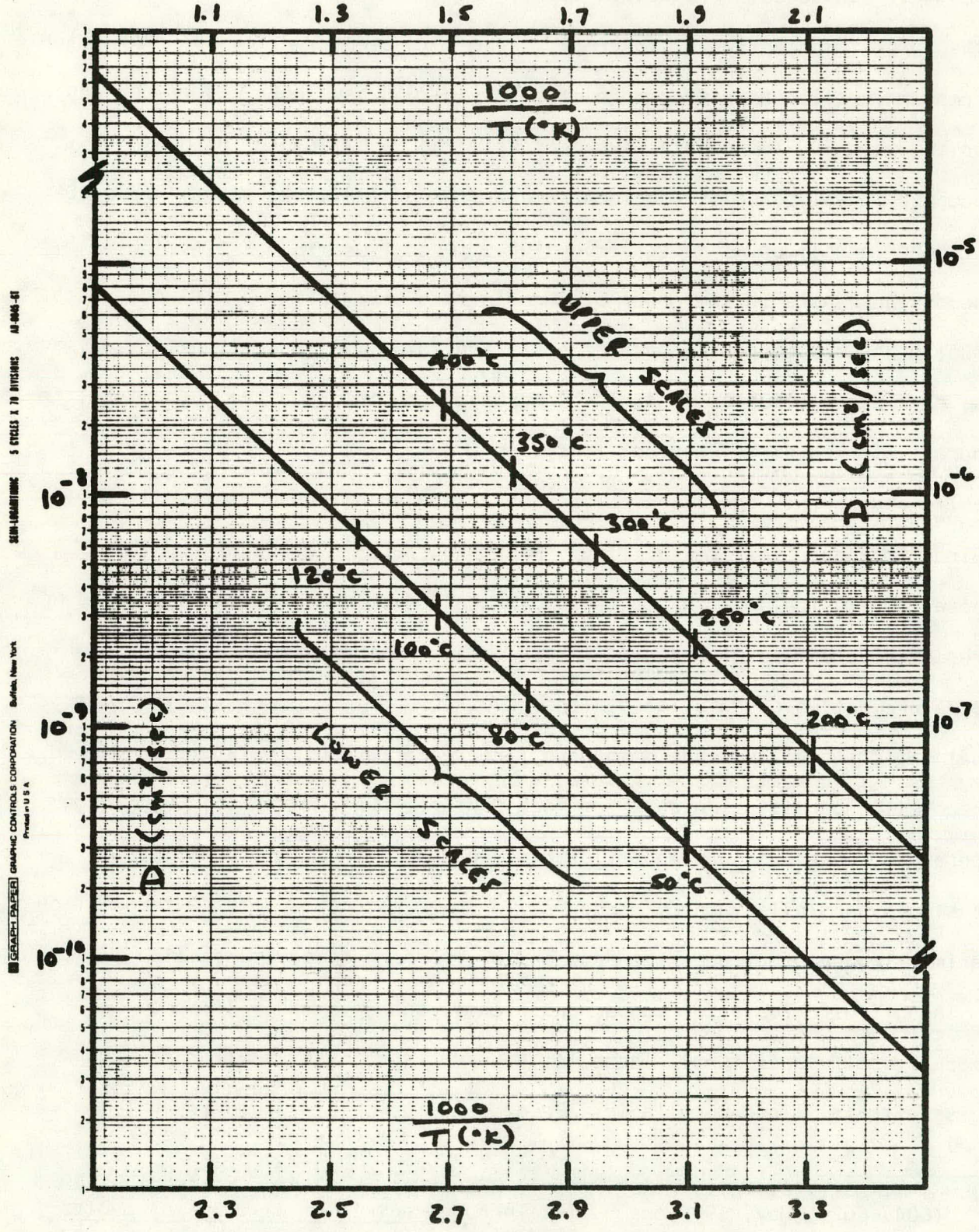

FIGURE 22: EXTRAPOLATION OF DIFFUSION DATA FOR COPPER IN SILICON.

TABLE 9

EXTRAPOLATED DIFFUSION DATA FOR COPPER IN SILICON [14]

TEMPERATURE T (^{o}C)	DIFFUSION COEFFICIENT D (cm^2/sec)
50	3.0×10^{-10}
80	1.35×10^{-9}
100	3.15×10^{-9}
120	6.7×10^{-9}

TABLE 10

PENETRATION OF COPPER IN SILICON FOR A PERIOD OF 20 YEARS

TEMPERATURE T (^{o}C)	DISTANCE $\sqrt{Dt}$ (cm)
50	0.44
80	0.92
100	1.4
120	2.1

TABLE 11

REPRESENTATIVE DIFFUSION DATA FOR COPPER AND NICKEL [15]

BULK MATERIAL	DIFFUSING SPECIES	ACTIVATION ENERGY Q (kcal/g.atom)	FREQUENCY FACTOR D_o (cm^2/sec)	TEMPERATURE RANGE (°C)
Copper	Cu^{64}	48.2	0.33	863 - 1057
Copper + 1 wt% Ni	Cu^{64}	48.9	1.86	780 - 890
Copper + 21.5 at % Ni	Cu^{64}	55.3	1.9	863 - 1112
Nickel + 45.4 at % Cu	Cu^{64}	60.3	2.3	985 - 1210
Nickel + 13 at % Cu	Cu^{64}	63.0	1.5	1054 - 1360
Nickel	Cu^{64}	61.3	0.65	850 - 1360
Copper	Ni^{63}	69.2	2.22	900 - 1200
Copper + 21.5 at % Ni	Ni^{63}	49.7	0.063	930 - 1113
Nickel + 45.4 at % Cu	Ni^{63}	60.3	2.3	985 - 1210
Nickel + 13 at % Cu	Ni^{63}	74.9	35	1054 - 1360
Nickel	Ni^{63}	60.5	9.96	1000 - 1400

necessary to determine the suitability of nickel as a diffusion barrier for copper; a general range is satisfactory. Accordingly, typical data, rather than specific high accuracy data, will be utilized.

Typical data for diffusion of copper into nickel and nickel rich alloys of copper and nickel can be approximated from the data in Table 11. For this purpose, values have been chosen as follows:

$$Q = 60 \text{ K cal/g. atom}$$

$$D_o = 1.5 \text{ cm}^2/\text{sec.}$$

Utilizing these numbers, values for diffusion coefficients, D, and diffusion distances, $\sqrt{Dt}$, have been calculated, Table 12. From these calculations, it can be seen that $\sqrt{Dt}$ is vanishingly small at 100°C. If 20 years storage occurred at 300°C, $\sqrt{Dt}$ would be 10^{-7} cm or 10^{-3} micrometer. This means that at 300°C, $10\sqrt{Dt}$ would be only 100 angstroms in 20 years. Nickel is, thus, an extremely effective diffusion barrier to copper. If processing interconnection or encapsulation requires times as long as 30 minutes at a temperature near 300°C, the nickel is still an extremely effective barrier. Copper substitution for solder in the Motorola plated metal system can be both technically and economically possible.

3.3.4 COPPER PLATING

Copper plating is a widely utilized technology. Adaptation to plating of copper on solar cells, however, required development. Due to the requirement of a nickel barrier to copper diffusion into silicon, plating of copper on solar cells is realy always plating of copper on nickel.

In addition to being necessary as a barrier to copper, nickel serves an additional function for copper plating of solar cell metallizations. The

TABLE 12

CALCULATED DIFFUSION DATA FOR COPPER INTO NICKEL, UTILIZING ASSUMED VALUES OF Q = 60 k cal/g.atom AND D_o = 1.5 cm /sec

T (°C)	D (cm^2/sec)	$\sqrt{Dt}$ (cm)
t = 20 years		
100	7.8×10^{-36}	7×10^{-14}
200	2.2×10^{-28}	3.7×10^{-10}
300	1.6×10^{-23}	1×10^{-7}
t = 30 min		
300	1.6×10^{-23}	1.7×10^{-10}

nickel layer increases surface conductivity of the cell contact areas, so that, once a nickel layer is present, even though it has only moderate conductivity itself, it expedites the subsequent uniform electroplating of additional layers of metal. Major requirements for obtaining a satisfactory copper layer are design of the fixturing for making electrical contact to the cell while plating, and the choice of the electrolytic copper plating solution chemistry.

In preliminary experiments, electrical connections to the external power supply (providing electrolytic bias) for copper plating were made in the same fashion as those described for electrolytic nickel plating. That is, fixturing was employed which was as simple as an alligator clip, or as elaborate as specially constructed holders consisting of copper rings and contacts mounted in teflon handles. Of course, making electrical contact to the nickel for copper plating is much easier than making contact to the silicon to plate the nickel layer. The nickel layer guarantees more uniform current distribution across the surface of the cell and hence more uniform plating. In addition, the plating bath contact itself is more consistent because it is metal (fixture) to metal (solar cell nickel layer) rather than metal to silicon. Optimization of a plating contact fixture has not yet been attempted but should be a straightforward exercise in engineering design.

Choice of an electrolytic copper plating solution is less obvious. Initial copper plating experiments utilized a cyanide solution, such as for the Lea-Ronal* Q-Level Copper Plating Process. Such solutions are known to provide highly efficient copper depositions with good throwing power. Throwing power is a measure of the degree of uniformity with which metal is deposited on an irregularly shaped electrode. By providing good throwing power (uniformity of deposit), effects of the actual electrical contact fixturing, and position of the cell in the plating tank with respect to the anode, are subordinated.

*Lea-Ronal Inc., Freeport, New York 11520

There are, however, several difficulties with cyanide copper processes. One immediate problem is the safety requirement of a cyanide plating hood and drain which are separate from all other acid facilities. This means that the plating tanks and rinse baths must be separate from any pre-plating, acid cleaning facilities or any pre-copper plating solutions such as acid electrolytic nickel plating baths. Another problem with cyanide copper plated layers is the inherently high internal stress in the metal layer. Of the four widely used types of electrolytic copper solutions (sulfate, fluoborate, pyrophosphate, and cyanide), the cyanide solutions deposit layers with significantly more internal stress. Such stress can promote future delamination of plated copper layers as well as impart strain to the silicon lattice in the vicinity of the metallurgical p-n junction, and thus introduce fill factor degradations.

To circumvent cyanide problems, subsequent experiments were initiated with acid copper sulfate solutions. The first tests were made using the Lea-Ronal Copper Gleam PC bath which is advertised to provide a bright ductile copper deposit particularly suited to the needs of the printed circuit industry. This bath consists of copper sulfate (8-12 oz. gal.), sulfuric acid (22-28 oz./gal.), chloride ion (30-60 ppm), and a proprietary brightener (Lea-Ronal Copper Gleam PC, 0.4 - 0.6% vol.). The operating temperature range for this bath is 70 - 90°F. It was used at room temperature (within this range), proving successful in that it was capable of plating to the nickel layer on the solar cell, and of being operated in the same hood along side the electrolytic nickel plating solution.

Anticipating that it may be desirable to reduce internal stress to a minimum in thickly plated copper layers, experiments were initiated to study

low stress copper plating solutions. An excellent refernece (16) was found which gives detailed measurements of the properties, such as stress, of deposits from numerous copper solutions. Two low stress copper sultafe/ sulfuric acid solutions suggested by (16) have been evaluated. Two formulas are listed in Table 13.

Formula 1 provides a plating bath which has low internal tensile stress. Formula 2 provides an internal stress which can range from very low tensile to low compressive. These simple formulas have proven to give satisfactory plated copper layers over electroless nickel base layers. Copper layers as thick as ten micrometers can be plated in 5 to 10 minutes. Adhesion is excellent and stress appears to be no problem. Plating can be accomplished at room temperature.

Formula 2 has been adopted for routine use in evaluating the nickel copper solar cell metallization system. Results of cell tests will be reported later. One addition to the copper solution which may prove to be desirable is a brightening agent. Addition of a brightener can lower stress and improve ductility. A commercial brightener has been ordered and will be tested.

3.3.5 CELL FABRICATION STUDIES

To test the ability of a plated nickel layer to serve as a diffusion barrier for an electroplated copper conductor layer, several heat stress experiments have been performed. Various samples have been heated in nitrogen to temperatures of 300°C and 400°C for times of 15 to 60 minutes. In all cases, no degradation of solar cell performance was noted when a plated nickel barrier was present, but catastrophic degradation, usually in the form of a total electrical shunt of the solar diode, occurred when no nickel was present.

(16) V. A. Lamb, C. E. Johnson, and D. R. Valentine, Journal of the Electrochemical Society, 117, 291C, 1970.

TABLE 13

LOW STRESS ACID COPPER ELECTROPLATING SOLUTION FORMULATIONS

FORMULA 1:

Distilled or Deionized Water, H_2O	to desired volume
Cupric Sulfate, $CuSO_4 \cdot 5H_2O$	87 g/ℓ
Sulfuric Acid, H_2SO_4	14 ml/ℓ

FORMULA 2

Distilled or Deionized Water, H_2O	to desired volume
Cupric Sulfate, $CuSO_4 \cdot 5H_2O$	187 g/ℓ
Sulfuric Acid, H_2SO_4	21 ml/ℓ

As an example of stress tests, two cells were prepared with electroless nickel layers approximately 5000Å thick. These were nominally three inch diameter cells with complete metal coverage on the back and about 8% coverage for the metal grid on the cell front. The front grid pattern was formed by etching the ohmic pattern into an existing silicon nitride antireflection coating using photoresist techniques. Thus, the silicon nitride also serves as a plating mask for the selective plating of electroless nickel.

After nickel deposition the cells were heated at 250°C in nitrogen for 30 minutes in order to form an adherent contact by nickel silicide formation. When pull tested, similar cells prepared at the same time as the two test cells failed only through concoidal fracture of the silicon under the pull test tab.

One of the two test cells was then etched in an aqua regia solution (3:1 $HCl:HNO_3$) to remove all of the nickel layer. This cell, and the cell with nickel still intact, were then both plated with copper in an acid electrolytic copper solution. The copper was plated to a thickness of about 8 microns.

At this point, current-voltage characteristic curves were measured for both cells. Measurements were made with no illumination and with simulated (tungsten quartz-halogen lamps) one sun illumination. In the dark, sufficient data were taken to plot the logarithmic current versus voltage curves. These curves conveniently display the behavior of low-level excess currents which directly influence solar cell fill factor. Under illumination, the standard solar cell characteristic curve was plotted to obtain values for open circuit voltage, short circuit current, efficiency, and fill factor. Before heat stress, both test devices are excellent solar cells, each with fill factors just exceeding 80%. Both cells were then heated to 300°C for 15 minutes.

Current-voltage characteristic curves for the two test cells for measurements taken both before and after heat stress are given in Figures 23 and 24 for the cell with the nickel barrier removed and in Figures 24 and 25 for the cell with the nickel barrier intact. The results are dramatic. The cell without the nickel layer is thoroughly destroyed. The cell with the nickel retains its excellent characteristics.

As indicated in Figure 26, the illuminated characteristic curve remains unchanges after heat stress for the cell protected with nickel. The only change occurs for very low level currents, as seen in the log I versus V curves of Figure 25. In contrast, the log I versus V curve for the cell with nickel removed, Figure 23, shows an enormous increase in excess current -- so much so that the cell characteristics are totally dominated by this current. The effect, as seen in Figure 24, is to lower the cell output voltage to less than one fourth of its original value.

The failure of the cell without the nickel barrier layer after just 15 minutes at 300°C is no surprise. It is expected that copper will easily diffuse on the order of 200 microns through silicon for this level of thermal stress. This is, in fact, about the same as the wafer thickness (7 mils) used for the test cells.

The test cell with the nickel barrier layer that suffered no ill effects after 15 minutes at 300°C was given an additional 45 minutes to effectively equal a total stress time of 60 minutes, four times longer than the first treatment. As observed in Figures 25 and 26, the additional time at temperature had no effect on the solar cell operating characteristic and had only minimal effect on the diode low level excess current. In fact, the cell fill factor was still maintained at 80%. Although improbable, the slight changes observed in the low

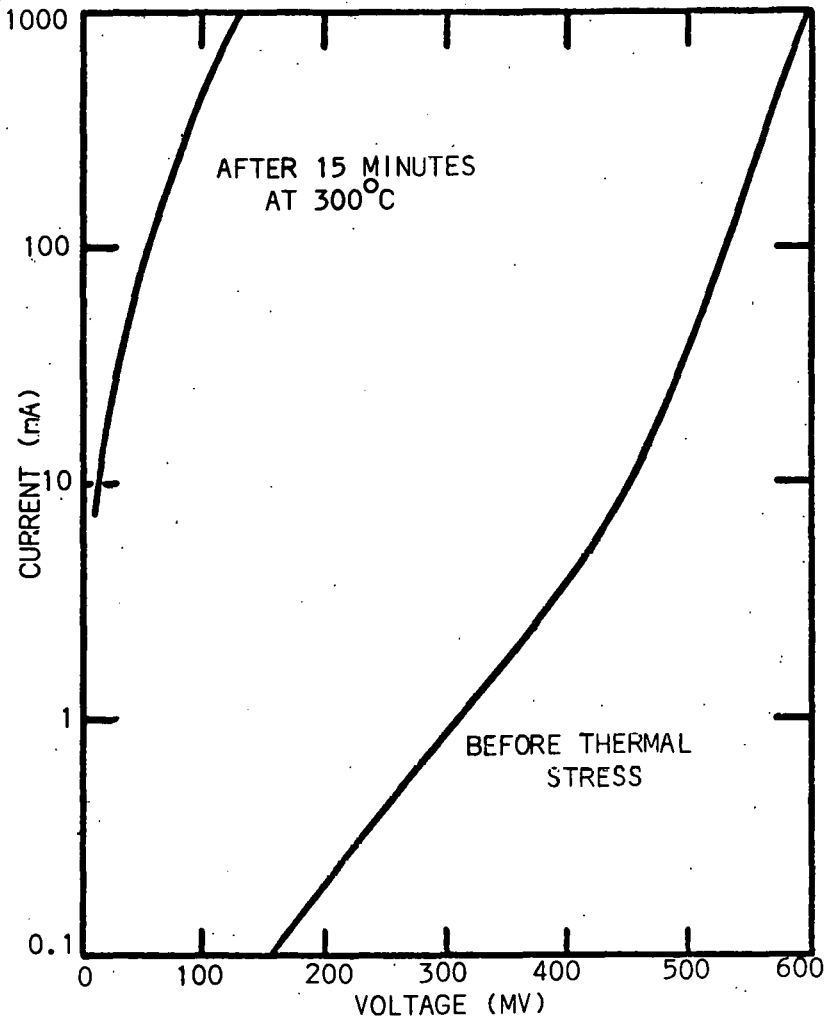

FIGURE 23: Logarithmic current versus voltage curves for solar cell plated with copper but with no nickel barrier layer. Severe degradation occurs after heat treatment.

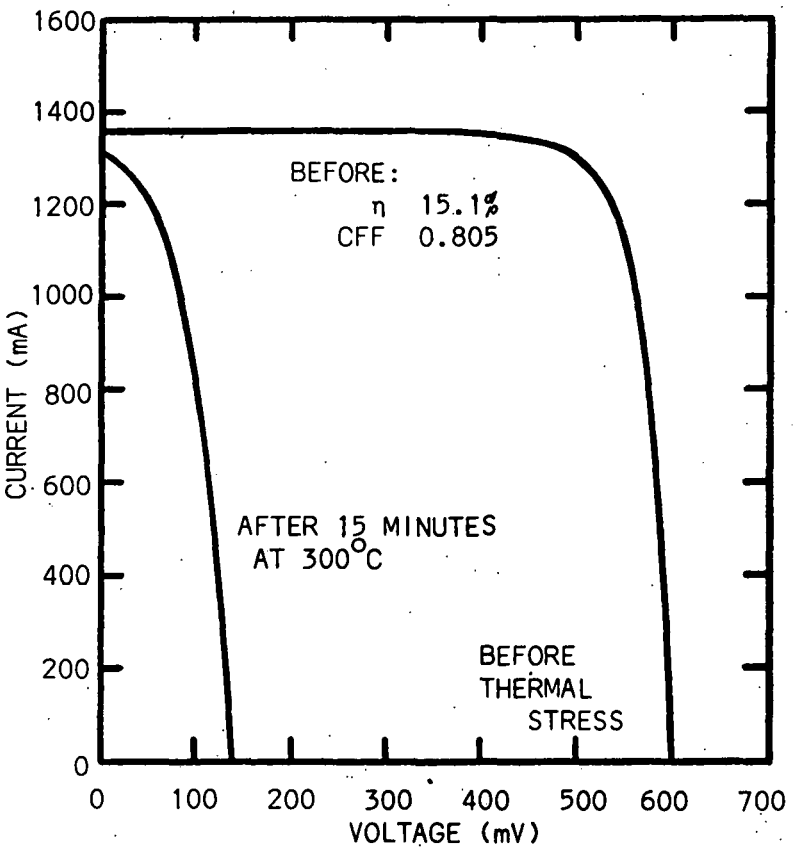

FIGURE 24: One sun, illuminated characteristic curves for solar cell plated with copper but with no nickel barrier layer. Performance is thoroughly destroyed after heat treatment.

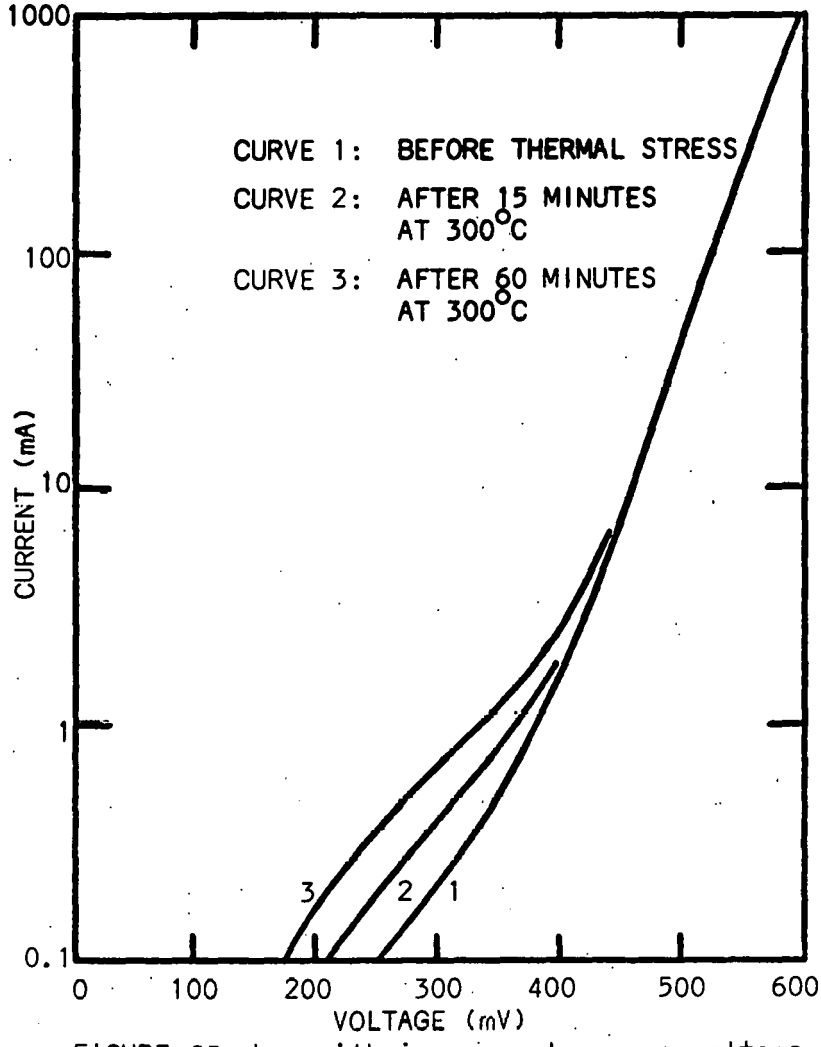

FIGURE 25: Logarithmic current versus voltage curves for solar cell plated with copper on top of a nickel barrier layer. No important changes occur after heat treatment.

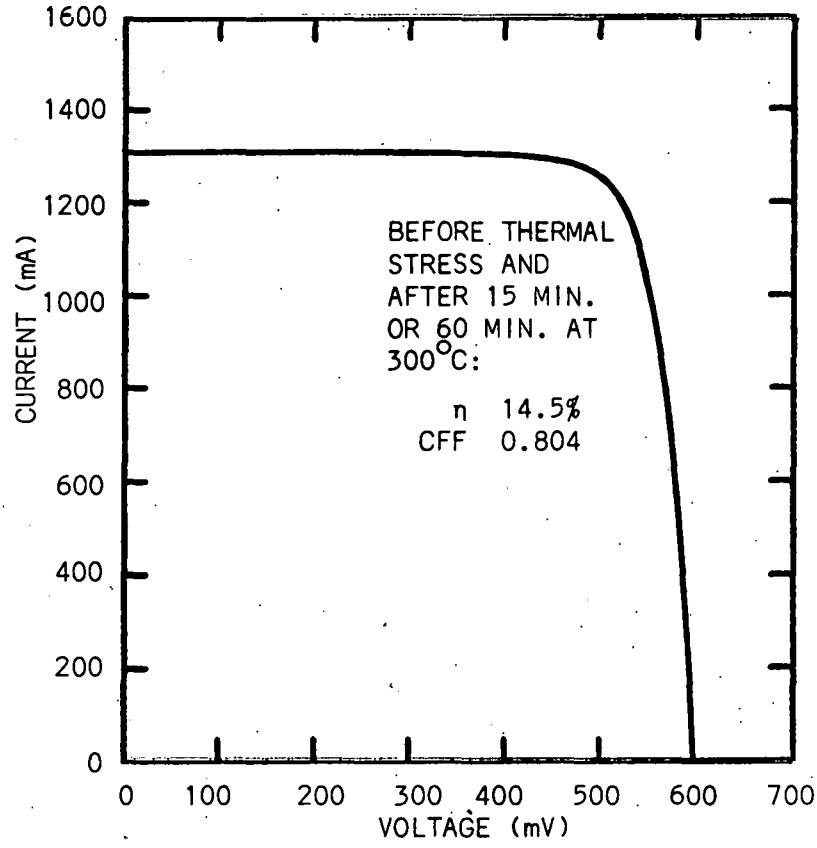

FIGURE 26: One sun, illuminated characteristic curve for solar cell plated with copper on top of a nickel barrier layer. No perceptible change occurs after heat treatments.

current portions of the log I versus V plots of Figure 25 may be due to very small and localized pinholes in the nickel layer through which copper has penetrated. On the other hand, the slight increases may be due to nickel itself diffusing to the junction in localized areas, may be due to other impurities from the plating operation, or may be due to stress.

These results indicate that the plated nickel-copper metallization system is truly viable as a solar cell metallization system.

3.3.6 METAL TOP SURFACE PROTECTION

The nickel-copper metallization system has the desirable qualities of high performance and low cost. As previously discussed, nickel serves as a good ohmic contact (through nickel silicide formation) and as a barrier to copper diffusion. Copper is the best low cost conductor available. It is also readily solderable in solder reflow interconnection schemes.

Copper, however, may be subject to oxidation during any thermal cycles at interconnection. Moreover, the amount of copper surface oxidation, sulfation or other corrosion during solar cell field service will depend on the extent and type of cell encapsulation. Copper sulfation and oxidation are assumed to be undesirable, since the reacted copper will be less conductive than pure copper, causing ohmic losses. Such ohmic losses may lead to solar cell degradation and eventual failure.

There are two ways to prevent copper surface reactions. The possibility of oxidation during interconnection can be eliminated by choosing the proper soldering technique, such as soldering under an inert ambient like argon. The possibility of reaction during field service can be minimized with an effective encapsulation system. However, there is little knowledge of the

effects of 20 years service life on today's encapsulation systems. Therefore, it would be prudent to seek an extra degree of insurance against copper degradation.

Additional protection of the copper surface against oxidation can be provided by using a third metal layer as a protective cap on top of the nickel-copper metallization. Such a protective cap could consist of tin, a nickel-tin alloy, a lead-tin alloy, nickel or nickel compounds, palladium, gold, chrome, etc. All these layers could minimize or prevent copper oxidation. Obviously gold or palladium could be very costly and are to be avoided.

The layer which is most easily achieved is tin. A protective tin cap can be formed in a simple immersion tin solution. There are numerous commercial baths available, all developed to plate tin to copper. A tin layer of reasonable thickness, say 50 microinches (1.25 micrometers) will provide excellent corrosion protection and maintain surface solderability. However, there are some potential disadvantages with tin. Tin is a low melting point metal ($232^{o}C$). It's use would preclude any heat stress tests after it was applied to the copper. Potential stress tests would include metal sintering or testing the integrity of the nickel contact copper barrier. Furthermore, if the entire cell is heated during solder interconnection, the total tin surface may be melted. The potential danger of melting the tin surface is that the molten tin will readily dissolve into the copper, forming an alloy and negating the protective surface coating.

Another potential difficulty with a proective tin layer as well as with bare copper itself is that copper can readily dissolve into the solder during interconnection. This can be troublesome if fine grid lines are used for the metal grid pattern and if the conductive copper is dissolved away just at the

point where the grid lines join the buss. This could introduce further ohmic losses.

The next most easily applied metal cap is probably nickel from an electroless nickel bath. The proper choice of electroless nickel could be plated directly to the copper surface. Nickel solutions using boron reducing agents are known to plate copper without any special sensitization. The small percentage of boron incorporated in such a nickel layer encourages an additional degree of solderability compared to pure nickel or phosphorus-nickel. However, minimizing nickel oxidation before solder interconnection remains the principal concern. Once interconnected, nickel oxidation is self-passivating and the nickel layer can provide excellent long term protection to the copper. In addition, a nickel-copper-nickel metallization system should be capable of withstanding thermal stress without degrading its beneficial properties. A protective top layer of nickel would remain virtually unaffected by a solder interconnection process, since the nickel will not interdiffuse with the copper and since the dissolution rate of nickel into lead-tin solder is much slower than any other metal under consideration.

Other possible protective top layer choices are nickel-tin or lead-tin alloys. These combine some of the individual advantages and disadvantages of tin and nickel. One processing difference is that such alloy layers are formed by electrolytic plating, which requires special jigging and fixturing.

Whichever metal is chosen as a top layer protectant, it is believed important to use such a layer for the additional margin of insurance it provides toward extending the service life of photovoltaic cells. Many of the combinations listed above have been investigated during the course of this contract. Two that have been studied in some detail are tin and nickel. An

electroless tin solution (Cu Tech ST 240) manufactured by Coppertech, Inc., of Allentown, Pennsylvania was used to provide an experimental tin layer. This proved to be readily solderable, even after weeks of storage. However, the low temperature melting point problems discussed earlier were evident. Experiments with nickel top surface layers were performed using an electroless nickel solution consisting of nickel sulfate, 25 g/ℓ, sodium pyrophosphate, 50 g/ℓ, ammonium hydroxide, 25 ml/ℓ, and dimethylamine borane, approximately 2 g/ℓ. The resulting nickel deposit contains on the order of 1% or less boron. It has been noted that this composition seems to maintain solderability even after 15 minutes exposure to air at 325°C on a hot plate. This was not the case for electroless nickel-phosphorus compounds that were studied. The phosphorus-nickel layers are most difficult to solder after short exposures to elevated temperatures in air.

In summary, an electroless nickel top surface protective layer over the copper conductor layer of the solar cell metallization seems to make the right compromise and provide both processing compatibility and long term protection when produced with an electroless nickel solution using a boron compound reducing agent.

4.0 CONCLUSIONS

While numerous conclusions can be drawn from the work performed on this contract, there are several significant conclusions which overshadow the others.

1. The thick electroless palladium layer in the Motorola PNS metallization system can be eliminated through the use of suitable nickel plating bath compositions for both electrolytic and electroless techniques.
2. Copper can be successfully used as the primary conductor layer for silicon solar cells. Nickel is a suitable silicon contact and barrier to copper diffusion. Further, electroless nickel, utilizing a boron compound as the bath reducing agent, provides a good top surface protection to the copper.
3. Mechanically masked plasma patterning of silicon nitride on a silicon surface is capable of opening lines with widths of one mil (25 μm). Excellent mask reproduction of five mil (125 μm) lines occurs even with spaces as great as ten mils (250 μ) between the the mask and substrate.
4. Plasma etching of thick surface layers to remove saw damage or to perform surface texturing is not cost-effective due to the long etch times and resulting slow throughput.
5. Ion implantation using high current unanalyzed beams can be used to fabricate high quality solar cells. This can significantly reduce the capital cost of equipment and floorspace required for ion implantation.
6. A SAMICS analysis of the Motorola process sequence was performed. Including formation of the initial silicon sheet, ribbon-to-ribbon (RTR) regrowth, cell processing, and encapsulation, the SAMICS calculations show a price of $0.6609 $ (1980)/watt (for a 100 megawatt factory) with an energy payback time of 0.767 years.

5.0 RECOMMENDATIONS

No specific recommendations can be made at this time.

6.0 CURRENT PROBLEMS

No current problems have been identified.

7.0 WORK PLAN STATUS

The work plan is complete.

8.0 LIST OF ACTION ITEMS

No items requiring unusual action have come to light during this report period.

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