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AUTOMATED ARRAY ASSEMBLY, PHASE II

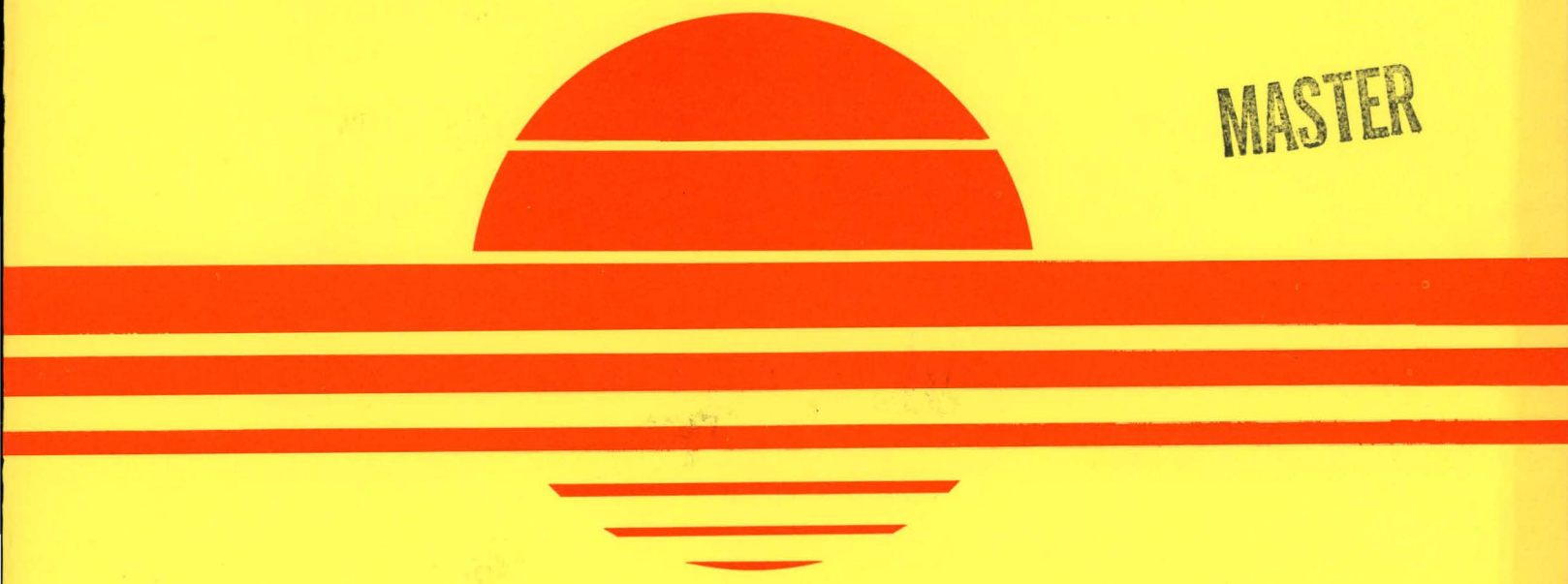
Quarterly Report No. 1

By
R. V. D'Aiello

December 1977

Work Performed Under Contract No. NAS-7-100-954868

RCA Laboratories
Princeton, New Jersey



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Prepared Under Contract No. 954868 For

JET PROPULSION LABORATORY
CALIFORNIA INSTITUTE OF TECHNOLOGY
Pasadena, California 91103

REA

PREFACE

This Quarterly Report, prepared by RCA Laboratories, Princeton, NJ 08540, describes the results of work performed from October 1, 1977 to December 31, 1977 in the Energy Systems Research Laboratory, B. F. Williams, Director; Materials and Process Laboratory, Solid State Division, H. Veloric, Manager; and at the Advanced Technology Laboratory, Government and Commercial Systems, Camden, NJ, P. Wright, Director. The Project Scientist is R. V. D'Aiello and the Project Supervisor is D. Richman, Head, Semiconductor Materials Research. Others who participated in the research and writing of this report are:

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SECTION I

SUMMARY

During the first quarter, a detailed process plan for the Automated Array Assembly - Phase II program to be conducted at RCA was developed. The elements of that plan are outlined in this report including a description of the individual processing steps in our manufacturing sequence. The progress made in each process step is then described. Highlights of the progress reported here are improved efficiency in ion-implanted solar cells by the introduction of a gettering step into the process and successful screen printing of a silver contact grid pattern on 3-in.-diam cells. In addition, initial tests of an aqueous spin-on dopant source are described including the possibility of applying this source by roll-on or screen-on techniques. Process steps needing further development include spray-on AR coating and back surface doping and contacting of cells. Plans for these developments and the verifications of working process steps are described.

SECTION II

INTRODUCTION

The purpose of our overall program is to establish technological readiness and provide verification for the elements of a manufacturing sequence which would ultimately be suitable for the large-scale production of silicon solar array modules at a selling price of less than $500/kW. A program and process plan for accomplishing this objective was developed and put into operation during the first quarter. This plan (described in Section III) is centered around the processing sequence shown in Fig. 1. Three junction-formation processes are shown; since our cost analysis shows that they do not differ greatly in cost, each should be considered for technical merits and possible future cost reduction. In Section IV the progress made in these processes is described, and plans for the next quarter are summarized in Section V.

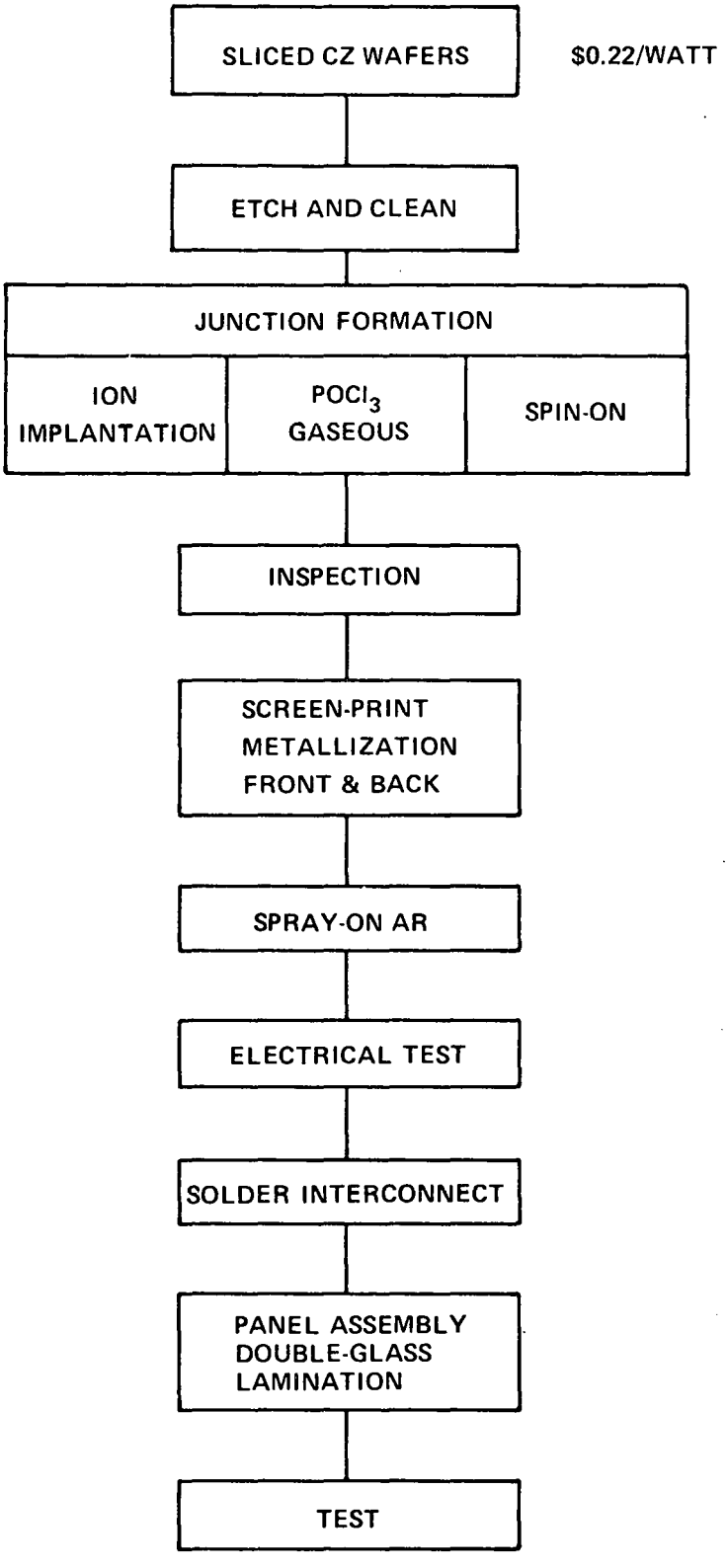

Figure 1. Major steps of process sequence.

SECTION III

PROGRAM AND PROCESS PLAN

A. INTRODUCTION

Our overall process plan is shown in Fig. 2. The philosophy of this plan is to establish an experimental production line starting with 3-in.-diam silicon wafers and consisting of junction formation using $POCl_3$ gaseous diffusion, screen-printed thick-film metallization, reflow solder interconnect, and double-glass lamination panel assembly. This pilot line will produce a sufficient number (approximately 2000) of solar cells in order to demonstrate the technological readiness of each of those process steps. Variations (of each process) will be made in order to set limits on the usable range of each process step and to determine the interaction with adjoining steps. Inspections, measurements, and tests are included in order to determine the output requirement characteristics of each step, obtain statistical variations, and evaluate the performance of the solar cells and panels.

Additional development and studies will be conducted in junction-formation and interconnect technology. Specifically, ion implantation will be studied in detail since this junction-formation process promises the lowest long-range cost but has been disappointing in terms of cell efficiency. Our objective is to first establish the starting material requirements, implant and anneal parameters necessary to fabricate high-efficiency cells, and then to verify this process in experimental production. Studies of spin-on dopants for both front and back cell surfaces will also be followed by an experimental production phase.

The technique of forming interconnects by parallel gap welding will be examined. If feasibility is established, the limits of this technology will be set.

B. DETAILED PLAN

The details of the major process steps of Fig. 2 are given below.

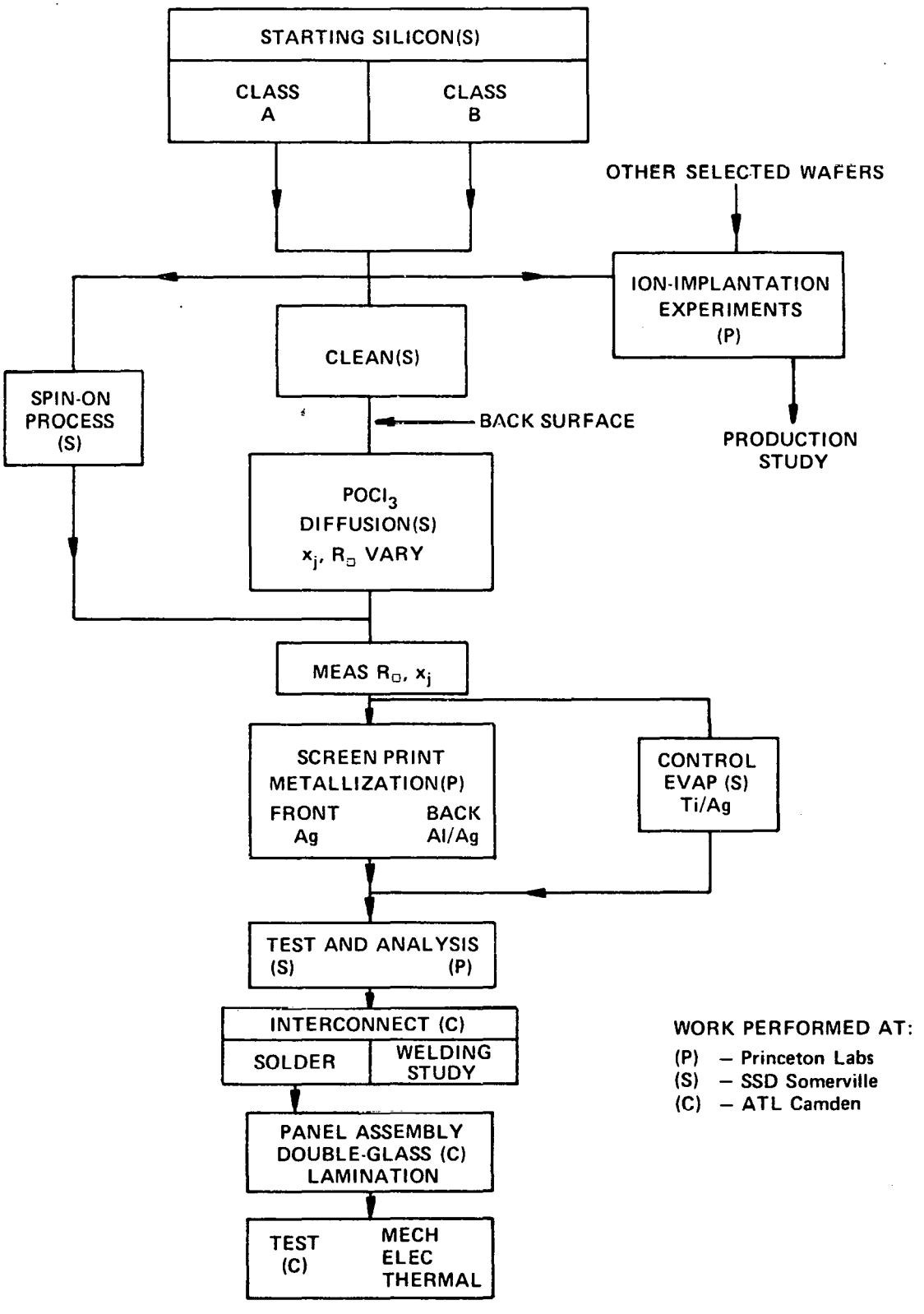

Figure 2. Block diagram of process sequence.

1. Starting Silicon - Selection and Preparation

For inventory and batching, Class A wafers are 3-in.-diam <100> wafers 1 to 3 ohm-cm or 5 to 10 ohm-cm with mechanically-chemically polished front and deep-etched back surfaces. Fifteen-mil-thick wafers are individually inspected under oblique light at X2 for surface defects and cleanliness and are scribed with a serial number on the backside. Each wafer is measured for thickness and resistivity by four-point probe. Twenty-five such wafers form one lot and these are logged into the travel log sheet which is used to enter information at each stage of processing and finally for statistical summary.

Class B wafers differ from the Class A samples only in the surface preparation. For economic reasons, elimination of surface polisning and minimizing surface etching is desirable. Class B wafers will be prepared by saw/etching from a 3-in.-diam boule. Sample lots of Class B wafers with the different etching conditions described below will be run along with Class A wafer lots.

Present data indicate that wafers from all approved vendors show little variation in critical parameters, i.e., grouping into resistivity ranges, physical dimensions, surface finish to specification, so that statistical sampling can be introduced. During the process verification work the initial sampling rate will be one wafer/lot and lot traceability will be maintained. Toward the end of this program it is expected that sampling can be reduced to 1/10 lots.

The present standard surface preparation process based on a polished front and deep-etched back surface is known to produce cells with a certain distribution of parameters. To reduce costs, six engineering lots will be fabricated on wafers with a front surface prepared by etching of the sawed surface. Our data indicate that good surfaces, i.e., with little residual damage, can be obtained by removing 1.5 mil by etching. Three of these wafer lots will have a deep-etched back surface and the other three will address the question of whether a sawed and flash etched (less than 0.2 mil) back surface with a sawed and deep-etched front surface can be used economically. It is unlikely that a sawed flash etched front surface can produce solar cells with acceptably high efficiencies. If these tests indicate feasibility, Class B wafers will be introduced into the experimental production lots along with Class A

wafers in a 60:40 proportion. Experiments will be conducted to determine the minimum silicon removal required from the front surface.

In separate tests described in Section IV, processing of 3-in.-diam wafers of 1- to 3-ohm-cm resistivity resulted in clearly better solar cell performance than 8- to 12-ohm-cm wafers obtained from the same vendor with the same specification except for resistivity. Thus, 1- to 3-ohm-cm wafers will be used throughout our work.

2. Junction Formation

a. $POCl_3$ Diffusion - Diffusion from a $POCl_3$ source is a standard industrial method and has been used extensively for fabricating solar cell junctions. Our data indicate that high performance cells with conventional evaporated Ti/Ag contacts can be made from $POCl_3$ junction diffusions 0.3 μm deep having a sheet resistance in the range of 30 to 200 ohm/square. In the present work, experimental production lots will be made to determine the range of sheet resistance and junction depth which are consistent with both the requirements for screen-printed contact metallization and good performance. Phosphorus surface concentration and junction depth will be varied by controlling the temperature of the $POCl_3$ liquid source and by adjusting the diffusion schedule.

b. Spin-On Sources - Experimental studies will be conducted on both n(P,As) and p(B)-type spin-on sources. Up to now, we have used only alcohol-based spin-on sources to fabricate solar cells, and these compared favorably with standard $POCl_3$ diffused cells. However, wide variations in sheet resistance within lots were observed, and, moreover, alcohol-based sources have a limited and somewhat variable shelf-life. Aqueous sources have become available recently, and are thought to have better reproducibility and longer shelf-life than the alcohol-based sources.

We plan to test both sources for the individual and simultaneous formation of both the n^+/p junction and the p^+/p back contact. In each case, evaluations and comparisons will be made of: required wafer cleaning and preparation; liquid source application techniques (i.e., spin-on vs roll-on or screening); diffusion schedule; uniformity and reproducibility of resultant sheet resistance and junction depth. After an acceptable procedure has been established, experimental production lots of 3-in. solar cells will be run in order to verify the process.

c. Ion Implantation - Our experience has shown that the ion-implantation process for junction formation requires significant design and development effort. Accordingly, we plan a separate and intensive study of the implant process and its interaction with water quality and subsequent contact metallization. The details of that study are listed in Table 1.

An experimental production phase will constitute verification of the best process selected during the study phase by generating statistical data on the performance of 3-in.-diam cells.

3. Metallization - Screen Print - Thick Film

Eighty percent of the wafer lots will be screen printed; the metallization for the remaining wafers will be evaporated Ti/Ag and will constitute a control for the screen-printing process.

A commercial silver ink with phosphate-bearing frit, Owens-Illinois* 6105, will be used to metallize the front side of the cell. A commercial aluminum ink, Engelhard** A-3484, will be used to metallize the backside. To improve solderability on the back, a second printing with silver ink OI-6105 will be used. Internally synthesized Ag, Al, or Ag-Al alloy inks will be developed with specific dopants as cell performance tests dictate the need.

After screen printing and drying both sides, the wafers will be sintered for varying times, peak temperatures and heating up rates to optimize cell efficiency consistent with other metallization properties, i.e., adhesion, solderability, and sheet resistance. Following potential wafer cracking during printing, ink firing conditions will require the most development effort. Limits must be determined for the heating-up rate, which is in turn dependent upon polymer burn-out behavior. Total dwell time and peak temperature will determine the critical penetration depth, specific contact resistance, sheet resistance, adhesion, and solderability. Each specific property will be checked on small 1- by 1-in. test patterns of appropriate configuration. For example, the dot-to-dot electrical resistance measurement will be used to determine specific contact resistance. Another pattern will be used to determine sheet resistance, adhesion via soldered wire tensile

*Owens-Illinois, Inc., Toledo, OH.
**Engelhard Industries, East Newark, NJ.

TABLE 1. ION-IMPLANTED SOLAR CELL EXPERIMENTS

Wafer Parameters to be Tested

Orientation <100> vs <111>
Background Doping Level
Starting Defect Level
n-Type Wafers vs p-Type Wafers

Implant Parameters to be Tested

Implant Voltage
Dose Level
Dose Rate
Species (^{11}B, ^{35}P, ^{75}As)

Process Parameters to be Tested

Anneal Temp
Anneal Time
Type of Cap
Gettering
Contact Problems (Screen Print to Implanted Layers)

Measurements to be Made

Illuminated I-V Curves → { Conversion Efficiency; Fill Factor; V_{oc} vs J_{sc} → J_o
Quantum Efficiency
Dark I-V Curves
Forward-biased Recovery Lifetime in Diodes
Reverse-biased Recovery Lifetime in Capacitors
Diffusion Length Measurements

test, and solderability via contact angle measurement. Device measurements on 3-in.-diam wafers with appropriate front and back fired patterns will be used to test cell efficiency and other electrical properties.

In order to determine intrinsically critical ink constituent properties, and to meet performance goals, new inks will be synthesized, in addition to using the commercial inks for prototype cells. Several Ag and Al powders and frits will be evaluated. Inks of varying particle size distribution, morphology, frit composition, and frit content will be formulated with appropriate organic vehicles. The frit compostion will be selected to match the specific dopant used on the n- and p-sides of the wafer. The test procedures outlined in the paragraph directly above will be employed to evaluate the influence of ink composition and morphology upon metallization and solar cell performance.

The extent of metallization penetration will be measured metallographically on the <100> and <111> plane of Si to assess metallization capabilities on both materials.

4. Antireflection Coating

We plan to use a spray-on process for the application of the antireflection film. The base material is a commercially available titanumsilicafilm* which will be modified for a spray process. Use will be made of Zicon** spray equipment at their facility in conjunction with experimental development at RCA as shown in Fig. 3.

5. Test and Analysis

The cell electrical testing and data analysis will form an important part of the verification of the preceding process steps. The test step will consist of:

(1) AM-1 simulated illumination measurement to determine the cell parameters (J_{sc}, V_{oc}, F.F.), 100% testing of all lots.
(2) Measurement of spectral response on selected cells representing the extremes of performance.

*Emulsitone Co., Whippany, NJ.
**Zicon Corp., Mt Vernon, NY.

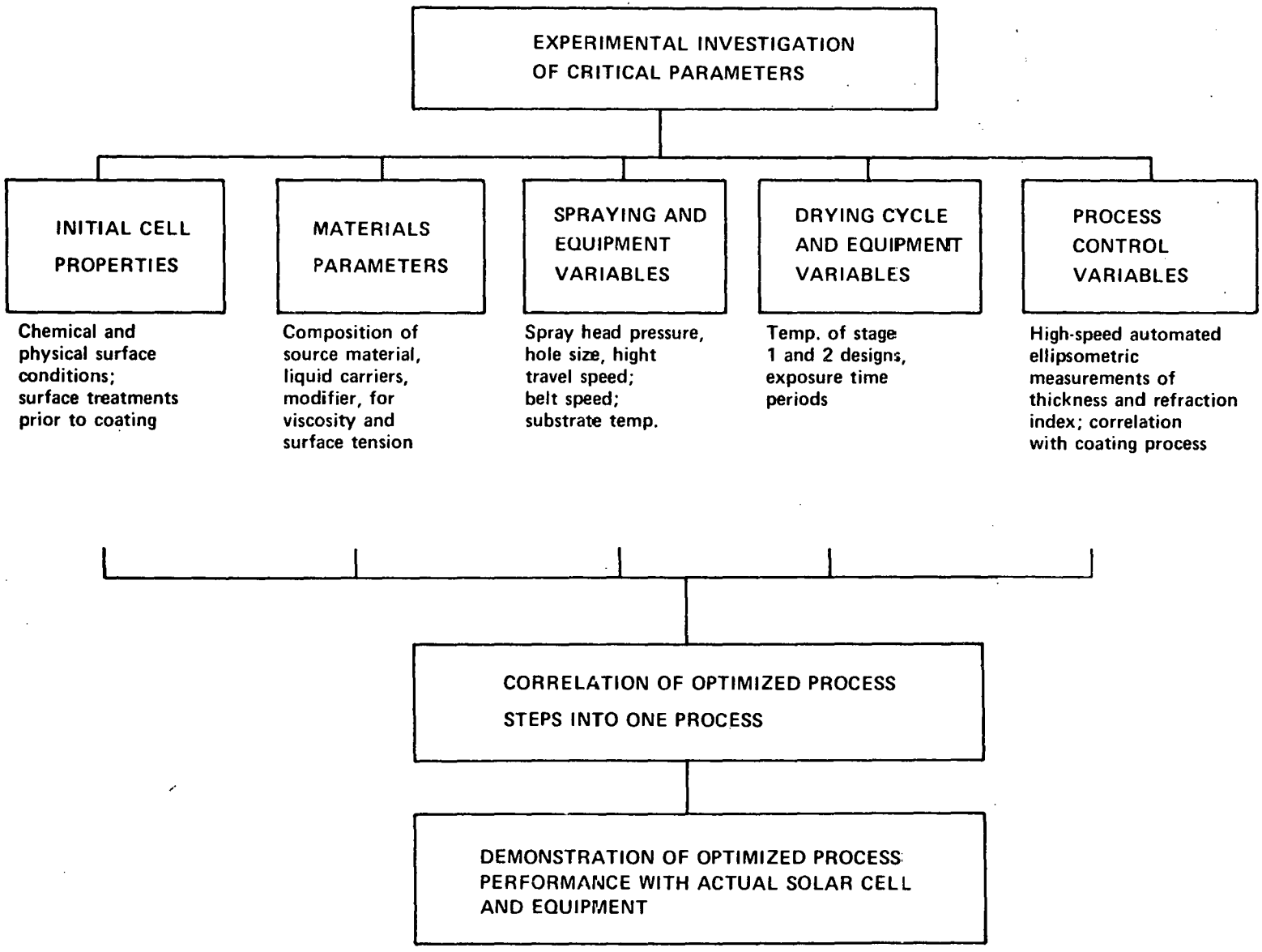

Figure 3. Process development plan for solar cell AR coating.

(3) Measurement of minority carrier lifetime by diode pulsed diode recovery on sample wafers from each lot.

(4) I-V measurements to assure junction quality and to evaluate parasitic resistance.

6. Interconnect and Panel Assembly

Interconnect technologies to be studied are reflow soldering and gap welding. Reflow soldering will be the primary method used to form strings for panel assembly. Welding studies will be performed in an attempt to establish feasibility and, if successful, to set limits on this process.

Our double-glass laminated panel design has been fully described in Quarterly Report No. 5 [1].

Laminations will be conducted at a vendor* location. Experiment will be conducted on small, ∿2- by 2-ft panels, first to assess the lamination conductions required for the fabrication of larger panels.

1. R. V. D'Aiello, *Automated Array Assembly*, ERDA/JPL-954352-77/3, Quarterly Report No. 5 prepared for Jet Propulsion Laboratory under Contract No. 954352, October 1977.

*Chromalloy-Saftee Glass Div, King of Prussia, PA.

SECTION IV

PROGRESS

The progress made during this quarter in the individual process steps is described below.

A. WAFER SELECTION AND PREPARATION

The major question to be resolved is the resistivity of the starting crystal. An initial test was conducted by mixing (1:1) p-type, 1 to 3 ohm-cm ($\bar{\rho}$ = 1.6 ohm-cm) and 8 to 15 ohm-cm ($\bar{\rho}$ = 10 ohm-cm) wafers purchased under identical specifications, except for resistivity, to form a process lot, and fabricating cells. $POCl_3$ junction formation, and conventional evaporated Ti/Ag contacts were used. The average cell parameters for this lot are listed in Table 2; it can be seen that the lower resistivity wafers yielded clearly better performance.

TABLE 2. SUMMARY OF ELECTRICAL TEST DATA ON CELLS MADE FOR RESISTIVITY SELECTION

	Average AM-1 Parameters		
Bulk $\bar{\rho}$ (ohm-cm)	I_{sc} (A)	V_{oc} (mV)	η (%)
1.6	1.32	585	11.0
10	1.28	510	9.3

Based upon the results of this test, three silicon boules of 1- to 3-ohm-cm resistivity, p-type, <100> orientation, 3-in.-diam wafers were purchased. These boules will be saw-cut and the surfaces prepared as described in Section II. These wafers will be used in the junction-formation studies and for experimental cell production.

B. JUNCTION FORMATION

1. $POCl_3$ Diffusion

This process is the most advanced and will be used to fabricate junctions for the majority of screen-printed metallization tests and for the fabrication of cells to be used in interconnect and panel assembly. For these purposes, during this quarter, 150 completed and electrically tested solar cells were supplied to the interconnect and panel group, and two lots of cells were prepared and used in screen printing tests as described below.

The major problem encounted thus far with the $POCl_3$ junction process is related to a lack of p^+ doping and some n^+ cross doping on the back of the wafers. At the temperature of diffusion (850°C), virtually no diffusion occurs from the boron source spun onto the back of the wafers, and this film does not completely protect against n^+ diffusion into the back.

2. Spin-On Dopant Sources

a. Background - Up to now only alcoholic spin-on sources had been used to fabricate solar cells, and these compared quite well with standard phosphorus oxychloride diffused cells in efficiency, even though wide variations in sheet resistance within each batch and on a wafer had been observed. This applied to the n-type diffusions, especially in the range of 30 to 100 ohm/square. Aqueous sources became available recently and are thought to have a better chance to give reproducible and uniform results because they tend to hydrolyze less readily and also because it seemed possible to use techniques other than spinning to apply the coating, such as roll-on or silk screening. Other questions to be investigated was whether boron diffused sufficiently at 850°C, the normal temperature for $POCl_3$, to form a back contact and whether high-temperature processing destroys the ability of lifetime recovery altogether. If arsenic could be used to form the junction and the necessary high-temperature processing did not destroy the lifetime irretrievably, the back contact boron diffusion could perhaps be made simultaneously. Again, conditions for diffusing these species from preferrably aqueous sources are of interest.

b. Experimental - All tests were made on chemically-mechanically polished wafers with deep-etched backsides in two resistivity groups, 1 to 3 ohm-cm and 5 to 10 ohm-cm, <100> p-type. For comparison of solutions and techniques, the 3-in.-diam wafers were processed in pairs. Caro's acid was used to prepare the hydrophobic surfaces deemed desirable for the alcoholic sources and ammonia-hydrogen peroxide for the hydrophylic surface found best for aqueous solutions.

Diffusions were made either at 850°C for 50 to 60 min for P and B or at 1000°C for boron followed by slow cooling to 600°C which required about 100 min or a fairly slow pull that required about 10 min.

The initial heat-up period was 10 min in nitrogen ambient, and the diffusion was carried out at first in 10% O_2 90% N_2 and later in a 50% mixture of the two gases in an effort to promote compete stripping of the glass in hydrofluoric acid. Although the situation improved in the 50-50 mixture, a supplementary wet oxidation step was necessary, using ammonia-hydrogen peroxide, to competely strip the glasses.

Sheet resistance was measured on blunt four-point probes, and the junction depth was determined by the groove and stain method.

c. Results - The alcoholic P spin-on source gave a sheet resistance of 228 $\pm$130 ohm/square and a standard deviation (SD) of 36% compared with the aqueous source of 50 $\pm$5 for set no. 1, 51 $\pm$6.5 on set no. 2 with SD of 6.5 and 7%, respectively. A third set made by diffusing longer at 850°C gave 32 $\pm$1.6 ohm/square and a standard deviation of 4.4%. A roll-on test under similar conditions gave 35 $\pm$10 ohm/square and a SD of 21%. All junction depths were 0.1 to 0.16 um and not further optimized. It is concluded that the aqueous source for phosphorus diffusion gives more uniform and reproducible results in terms of sheet resistance whether it is spun or rolled on. It was also found that the sheet resistance did not vary significantly with thickness of the film which was deliberately varied from 100 to 410 nm by varying the spin speed from 1500 to 3000 rpm and also by dilution of the film. We also found that the addition of glycerol was better as a diluent than water.

No penetration of boron was observed during any of the 850°C diffusions from alcoholic or aqueous, spin-on or roll-on sources. The detection limit was about 0.02 um on the high resistivity n-type mechanically-chemically polished samples used in this test.

The aqueous and alcoholic sources gave the same reproducibilities, 21% SD, in diffusions at 1000°C for 60 min, giving sheet resistivities of 25 to 40 ohm/square and a penetration of about 0.13 um.

The aqueous boron source can be used to provide the back contact diffusion at 1000°C when evaluated in terms of sheet resistance, reproducibility, and convenience.

Preliminary data were obtained by SEM techniques after developing a relatively simple procedure. These indicated wide variations of diffusion length but with no clear cut relationship to annealing. A systematic test has been started that will permit us to measure diode lifetime and cell efficiency on the same wafers used for the diffusion length measurement.

3. Ion Implantation

From our previous experience [2] in the fabrication of experimental and production-quantity ion-implanted solar cells, we have found that the low efficiencies (8 to 10%) generally obtained were directly related to low lifetimes (short diffusion length) measured after processing. This condition is believed related to unannealed implant damage and, to some extent, to the thermal cycle used to form the junction. It is also suspected that the defect density existing in the starting wafers is of importance in its interaction with the ion-implantation and annealing processes.

Our study of ion implantation was started by examining the crystallographic defect density in a variety of potentially useful silicon wafers. This was done by oxidation and chemical preferential (Wright-etch) etching of the wafer surfaces. A large variation in defect density was found from lot to lot and within a given lot, with high defect density occurring even in some wafers which were supposedly of "high-quality."

With this information as a background, a gettering step was incorporated into our ion-implantation and anneal process. The major purpose of the gettering is to improve the resultant lifetime after processing. The first gettering process selected involves the deposition of a highly doped boron source on the back

2. R. V. D'Aiello, *Automated Array Assembly*, DOE/JPL-954352-77/4, Final Report prepared for Jet Propulsion Laboratory under Contract No. 954352, December 1977 (Draft).

surface of the wafers. This is a low temperature process (600 to 800°C) and can be done either before or after implanting the top surface. The gettering action is then accomplished during the normal furnace anneal of the top junction.

Initial experiments were conducted on six p-type, 1- to 2-ohm-cm wafers, with three wafers receiving the gettering step. The junction side was formed by a phosphorus implant with a dose of 1.5×10^{15} A cm^{-2} at an energy of 5 keV. The average AM-1 cell parameters and the range of lifetime measured by pulsed recovery of the gettered and control samples are listed in Table 3. The data show that gettering results in longer lifetime resulting in considerably higher short-circuit current density and much improved overall cell performance.

TABLE 3. SUMMARY OF SOLAR CELL PARAMETERS FOR ION-IMPLANTED CELLS

Gettered	$\overline{J_{sc}}$ (mA/cm^2)	$\overline{V_{oc}}$ (mV)	$\overline{F.F.}$ -	$\overline{\eta}$ (%)	Lifetime τ (μs)
Yes	31.6	542	0.764	13.3	3-5
No	27.5	512	0.733	10.5	∿0.3

C. SCREEN-PRINTED METALLIZATION

Preliminary investigation involed chemical analysis and qualification tests of commercial inks. These tests resulted in the selection of Owens Illinois No. 6105 phosphated silver ink on the basis of low contact and sheet resistance. A satisfactory printing and firing schedule (675°C, 10 min in air) was also found.

During this quarter, one lot (12 wafers) of 3-in.-diam solar cells were screen-printed with OI-6105 Ag ink. Only the front surface grid pattern was printed; evaporated and sintered aluminum was applied to the back after printing and firing. The wafers were prepared by the $POCl_3$ junction-formation process with a resultant average sheet resistance of 33 ohm/square. A 20-wafer lot was split, twelve for screen printing and eight for conventional evaporated Ti/Ag metallization (designated as controls).

A summary of the cell parameters measured on this lot is given in Table 4. Independent measurements of the junction I-V characteristics on the screen-printed cells showed reasonably low leakage current and a diode n-factor

TABLE 4. SUMMARY OF SOLAR CELL PARAMETERS FOR 3-in.-DIAM CELLS WITH SCREEN-PRINTED METALLIZATION

	$\overline{I_{sc}}$ (A)	S_I (A)	$\overline{V_{oc}}$ (mV)	S_V (mV)	$\overline{F.F.}$ -	S_F -	$\overline{\eta}$* %	S_η (%)	R_s (ohm)
Best Screen Printed	0.762	-	570	-	0.712	-	7.1	-	0.045
Average Screen Printed	0.730	0.036	560	10	0.680	0.06	6.4	0.82	
Average Control	0.828	0.060	533	12	0.610	0.02	6.7	0.80	

*No AR coating

between 1.15 and 1.30. These results are encouraging, but data on larger lot sizes are required before definitive conclusions can be drawn.

D. SPRAY-ON AR COATING

Several attempts were made to spray the "as-received" titiumsilicafilm liquid onto solar cells and polished silicon wafers. An extensive test was conducted at Zicon Corp. using their Autocoater. Experiments were conducted with the objective of spraying a film which when baked would be 700 $\pm$35 Å thick. All attempts to spray the liquid resulted in continuous films, but very nonuniform in thickness. These tests indicate that the viscosity of the liquid should be adjusted for the spraying apparatus and conditions. Experiments are in progress to determine the required liquid and spraying parameters.

SECTION V

PLANS FOR NEXT QUARTER

A. JUNCTION FORMATION

1. $POCl_3$ Diffusion

We will process 10 lots (250 wafers) having ∿30-ohm/square sheet resistance and junction depth of ∿0.3 μm with 200 wafers designated for screen-printed contacts; of these, 150 wafers will be fabricated on saw/etched wafers.

We will begin tests of the effect of variation of diffusion parameters (furnance temperature, time, and gas flow) on resultant cell properties and ability to successfully form screen-printed contacts.

2. Spin-On Dopant Sources

We will prepare solar cell and diode structures with both alcohol based and aqueous sources to compare junction properties and solar cell performance. Structures will be $n^+/p/p^+$, prepared with phosphorus and boron spin-on dopants. Feasibility of roll-on and silk-screen application of aqueous sources will be tested. We will determine whether high-temperature diffusion of arsenic/boron impairs lifetime irretrievably.

3. Ion Implantation

Work on gettering will be continued to determine the optimum gettering and anneal cycle. Similar experiments will be performed on several ranges of starting wafer parameters. The cost of the gettering process will be determined, and exploration of implant parameters will begin with primary emphasis on dose level and energy. We will prepare samples for screen-printed contact tests.

B. SCREEN-PRINTED METALLIZATION

The screen-printing process will be evaluated for both back and front sides of solar cells. Aluminum and silver inks will be used on the back and silver on the front. We will screen print 200 wafers to determine statistical information on this process. Work will be continued on in-house ink development. Initial tests will be conducted to determine printing and firing schedules and resultant electrical properties on silicon.

C. SPRAY-ON ANTIREFLECTION COATING

Experiments will continue in an effort to determine the parameters required of the liquid and spray apparatus to obtain a uniform film.

D. INTERCONNECT AND PANEL ASSEMBLY

Welding experiments will continue on 3-in.-diam cells having both conventional Ti/Ag contacts and screen-printed silver metallization. Weld-bond strength and cell degradation over a range of welding parameters will be studied.

Reflow soldering will be used to form series strings which will then be paralleled to form arrays for lamination experiments.

Twelve panels will be laminated by the safety glass technique. Ten panels will be approximately 2 ft^2 and two will be larger, the size dependent upon the results with the smaller panels. All panels will contain active cells.

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