

HOLE-TRAPPING/HYDROGEN TRANSPORT (HT)² MODEL FOR INTERFACE-TRAP BUILDUP IN MOS DEVICES

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The electric field dependence of radiation-induced interface-trap formation has been reported to be different for metal-gate capacitors and polysilicon-gate capacitors and transistors. For metal-gate capacitors, interface-trap formation steadily increases with increasing positive field [1]. On the other hand, for polysilicon-gate capacitors and transistors, interface-trap buildup peaks near fields of 1 MV/cm to 2 MV/cm and decreases with an approximate $E^{-1/2}$ dependence at higher fields [2]. The previously reported field dependence for interface-trap generation for Al-gate capacitors is consistent at all fields with McLean's physical explanation of the two-stage process [3], which depends on hydrogen ion (H^+) release in the bulk of the oxide as radiation-induced holes transport to either interface via polaron hopping. Above 1 MV/cm to 2 MV/cm, the field dependence of interface-trap buildup for polysilicon-gate devices is inconsistent with this model. Instead, it is similar to the field dependence for hole-trapping in SiO_2 [2], suggesting that hole trapping may play a key role in interface-trap generation in Si-gate devices. However, recent studies of the time-dependence of interface-trap buildup by Boesch [4] and Saks et al. [5] have shown that hole trapping cannot be the rate-limiting step in interface-trap buildup in polysilicon gate devices. Consistent with McLean's [3] physical explanation of the two-stage process, the rate-limiting step in interface-trap formation appears to be H^+ transport to the Si/ SiO_2 interface [4,5].

At the SISC we will show that the electric field dependence of radiation-induced oxide- and interface-trap charge buildup for both polysilicon and metal-gate transistors follows an approximate $E^{-1/2}$ field dependence over a wide range of electric fields ($E_{ox} > 0.2$ MV/cm) when electron-hole recombination effects are included. This field dependence provides further support that hole trapping is involved in the interface-trap buildup process in MOS devices. Based on these results a hole trapping/hydrogen transport (HT)² model for interface-trap buildup is proposed.

Irradiations were performed using a 10-keV ARACOR x-ray source at a dose rate of 4170 rad(SiO_2)/s, and at Boeing Physical Science Center's 10-MeV electron linear accelerator (LINAC). Threshold voltage shifts due to oxide- and interface-trap charge, ΔV_{ox} and ΔV_{it} , were determined via the dual-transistor charge separation technique [6]. Charge-pumping measurements [7] were also used to determine ΔV_{it} . Our observed field dependence for ΔV_{ox} is consistent with previous results at comparable fields [2]. ΔV_{ox} increases with increasing positive field up to approximately 1 MV/cm to 2 MV/cm and decreases with an approximate $E^{-1/2}$ dependence at higher fields. The $E^{-1/2}$ field dependence for ΔV_{ox} at fields above ~ 2 MV/cm has been attributed to a reduction in effective hole-capture cross-section with increasing electric field [8,9]. The departure from an $E^{-1/2}$ dependence for ΔV_{ox} below ~ 2 MV/cm is caused by electron-hole recombination. As the electric field decreases, fewer holes escape electron-hole recombination [8,9], resulting in fewer holes trapped at the Si/ SiO_2 interface. If we adjust ΔV_{ox} for electron-hole recombination, we can correct for the effect of the loss of these holes on the field dependence of the observed hole trapping. To adjust the data, we use the empirical equation for electron-hole recombination for x-ray irradiation given by Dozier et al. [9]. At the SISC, the adjusted ΔV_{ox} data for both metal- and polysilicon-gate transistors will be shown to follow an $E^{-1/2}$ dependence at fields above 0.2 MV/cm.

We now examine the field dependence of interface-trap generation for positive fields during irradiation. Under positive bias, holes transport to the Si/ SiO_2 interface. In Fig. 1, ΔV_{it} data is shown for polysilicon-gate transistors irradiated to 500 krad(SiO_2) at fields (E_{ox}) from +0.2 MV/cm to +5 MV/cm, and annealed for 1-week at +3 MV/cm at room temperature. This anneal was sufficient for the interface trap buildup to saturate. Also shown in Figure 1 are adjusted ΔV_{it} data, in which the values of ΔV_{it} were corrected for charge yield in the same manner as ΔV_{ox} . With this procedure, we are attempting to correct for the effect of electron-hole recombination on the field dependence of interface-trap buildup. We have drawn a best-fit line showing an $E^{-0.6}$ field dependence through the adjusted ΔV_{it} data, though to within the experimental uncertainty the data are also quite consistent with an $E^{-1/2}$ field dependence.

Next, we explore the field dependence of interface-trap generation for negative bias during irradiation, followed by anneal at constant +3 MV/cm. For this case hole transport during irradiation is to the polysilicon/ SiO_2 interface. In Fig. 2 we plot both the measured and adjusted ΔV_{it} data for polysilicon-gate transistors irradiated to 1 Mrad(SiO_2) at negative electric field. The bias was then switched to +3 MV/cm for a 1-week anneal at room temperature, so the dependence of the saturated ΔV_{it} on electric field during irradiation could be determined. While the magnitude of ΔV_{it} after anneal is less for the 1 Mrad(SiO_2) irradiation in Fig. 2 than for the 500 krad(SiO_2) positive-bias irradiation in Fig. 1, the adjusted ΔV_{it} data in Fig. 2 also show an $E^{-1/2}$ field dependence (illustrated by the dashed line). Thus, interface traps in polysilicon gate devices build up with an $E^{-1/2}$ field dependence whether holes are transported during irradiation to the Si/ SiO_2 or to the gate/ SiO_2 interface.

The observed $E^{-1/2}$ field dependence of ΔV_{it} strongly suggests that McLean's physical explanation of the two-stage process [3] does not account for the interface-trap buildup in these metal- and polysilicon-gate transistors. Instead, this field dependence is strongly reminiscent of the decrease in effective hole capture cross section with increasing oxide electric field [8,9], suggesting that hole trapping may be intimately involved in the interface-trap buildup process for these transistors. This point must be reconciled with recent evidence from time-dependent studies of interface-trap buildup, which show that hole-trapping cannot be

the rate-limiting step in the interface-trap buildup process [4,5].

To reconcile previous results with our data, we suggest a hole-trapping/hydrogen transport (HT)² model for interface-trap buildup. In this model, for positive bias during irradiation, holes transport to the Si/SiO₂ interface. We propose that, during their capture (and/or neutralization), H⁺ is released [10]. This H⁺ then transports to the Si/SiO₂ interface and there may react to form an interface trap [11]. Under negative bias, hole trapping events near the gate/SiO₂ interface liberate H⁺, which may then drift to the Si/SiO₂ interface and form interface traps during a subsequent positive-bias anneal.

In the (HT)² model, we propose that the number of holes trapped (and/or neutralized) determines the total number of interface traps (i.e., the saturated value) that build up at a given electric field. Because the number of holes trapped scales with E^{-1/2} (after recombination effects are accounted for), the E^{-1/2} dependence of interface-trap buildup is therefore naturally explained with the (HT)² model. This model is consistent with previous observations on similar devices that, under positive bias, the protons that lead to interface-trap buildup are predominantly released near the Si/SiO₂ interface [12]. Furthermore, this model also seems to be consistent with the experimental work of others [13-15], although with a different interpretation of the results. Yet, we emphasize that, based on the work of Boesch and Saks et al. [4,5], the rate-limiting step in the interface trap formation process must be the time required for the H⁺ to transport from its point of release, at or near the hole trap site, to a suitable site at the Si/SiO₂ interface at which it may react to form an interface trap.

At the SISC, we will show interface-trap buildup for metal-gate transistors with similar gate oxides, which also followed an E^{-1/2} field dependence. This field dependence differs from that observed previously for metal-gate capacitors [1]. This suggests that the way that hydrogen is incorporated in the oxide during device processing may play a key role in determining whether H⁺ release in the bulk of the oxide [3], or near an interface [12], leads to the interface-trap buildup.

Based on the proposed (HT)² model for interface-trap buildup, we would expect to see a clear difference in the time dependence of interface-trap buildup for these devices under positive and negative bias. We are currently conducting experiments to address this issue, and the results will be presented at the conference. Also, experiments to distinguish between hole trapping and neutralization as the process that is responsible for the release of the H⁺ will be discussed at the SISC, as will the thickness dependence.

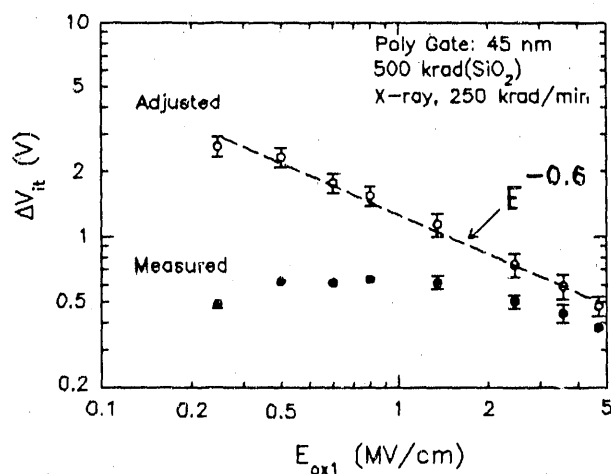


Figure 1: ΔV_t for positive bias irradiation and a 1-week, +3 MV/cm anneal.

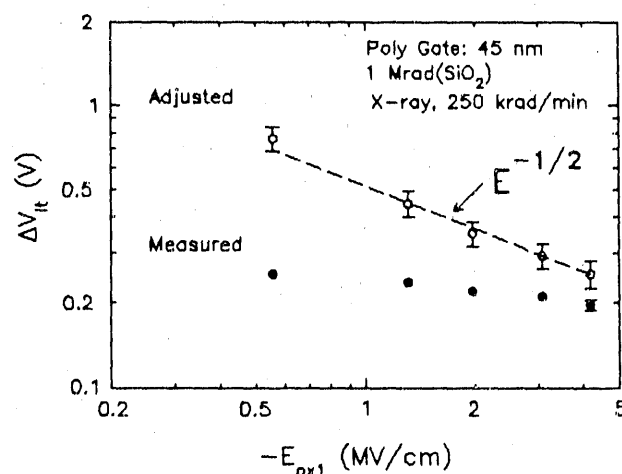


Figure 2: ΔV_t for negative bias irradiation and a 1-week, +3 MV/cm anneal.

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