BIPOLAR MONOLITHIC PREAMPLIFIERS FOR SSC SILICON CALORIMETRY*

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Abstract

This paper describes preamplifiers designed specifically to address the requirements of silicon calorimetry for the Superconducting Super Collider (SSC). Eight different preamplifiers designed for detector capacitances ranging from 20 pF to 500 pF and operating temperatures from 25° C to -20° C are discussed. The preamplifiers were fabricated with two different high-frequency processes (one with the VTC, Inc. VJ900 process, seven with the Harris Semiconductor VHF Process). The different topologies and their features are discussed in addition to the design methodologies employed. The results for noise, power consumption, speed, and radiation damage effects as well as data for post-damage annealing are presented for the VTC process preamplifier. Simulations for the VHF Process circuits are presented. This work was funded through SSC Generic Detector funding, SSC Detector Subsystem funding, and the Oak Ridge National Laboratory (ORNL) Detector Center.

Introduction

Preamplifiers for SSC silicon calorimetry involve requirements that are common to other forms of calorimetry and some that are unique. Among the requirements are a need for low charge sensitivity, fast rise times, high slew rate, low noise, radiation hardness to > 5 Mrad, allowance for increasing detector leakage, low power consumption, and the fewest number of power supply connections possible. Developments undertaken at ORNL attempted to address these requirements with several preamplifier designs fabricated by two silicon foundries - VTC, Inc. and Harris Semiconductor. Both processes were dielectrically isolated complementary bipolar processes with transition frequencies in excess of 1 GHz. This paper describes the circuit topologies chosen, measured results of the circuit fabricated through VTC, and simulated results of the circuits being fabricated through Harris. All circuits presented have either been fabricated or are currently in fabrication. Both pre- and post-radiation measurements of the devices used in both the VTC and Harris processes are presented elsewhere in this conference[1].

Circuit Fabricated Through VTC

The initial design philosophy of this preamplifier was to develop a circuit for use with a silicon detector of ~ 100 pF capacitance and exhibit a noise of < 7500 rms electrons (erms) for a CR-RC peaking time of ~ 100 ns. The rise time was to be < 10 ns to allow the use of shorter peaking times if desired. The power dissipation was required to be < 10 mW, charge sensitivity was to be ~ 0.2 V/pC, and maximum charge input was to be 17 pC which corresponds to a 3000 MIP event. The power supply rails were chosen to be ± 3.5 V for reduced power dissipation.

Current Feedback Preamplifier Topology

The topology chosen for the first preamplifier development was that of current feedback (CF) described by Comlinear Corporation[2] and Kennedy[3]. Current feedback has many advantages when compared to more traditional topologies such as differential input[4] or grounded source (grounded emitter)[5,6,7]. Among the advantages are short settling time, excellent loop stability at low closed-loop gain, and high bidirectional slew rate for low static power dissipation. The major drawback is that the noise due to input bias current is larger than either of the other topologies by approximately the β of the input device. With the short peaking times necessary for the SSC, the current noise should be acceptable.

One of the design goals of this project was to allow the detector to be directly coupled to the preamplifier, thus precluding the need for a bulky external coupling capacitor. The current flowing from the detector into the input and, subsequently, the feedback resistor of the preamplifier shifts the preamplifier dc bias point as the detector current increases with progressive detector radiation damage. The shift in bias point causes two problems. The first and most apparent is that the output of the preamplifier will move closer to the negative supply rail. This reduces the

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maximum output signal amplitude and, therefore, the dynamic range that can be tolerated prior to overload. The lower supply voltages required for low power dissipation only compound the problem. The second and less obvious is that as bias point changes, the preamplifier gain changes slightly because of the nonlinear nature of the transistors, resistors, and capacitors comprising the circuit. This condition is normally described as differential nonlinearity[8]. One desirable feature of a preamplifier would be to provide a method of restoring the dc operating point with minimal effect upon the impulse response, noise, or power dissipation of the circuit. The complete circuit, a block diagram of which is shown in Fig. 1, employs a gated rebalance amplifier (error amp) that samples the output for 10 μs to 50 μs every 40 ms and restores the preamplifier output to a value equal to the bandgap reference voltage allowing the preamplifier to continue to operate within its optimum range of performance, despite increases in detector leakage current. The particular implementation shown here will correct for up to 25 μA of detector leakage current. Table 1 summarizes the pre- and post-radiation performance results.

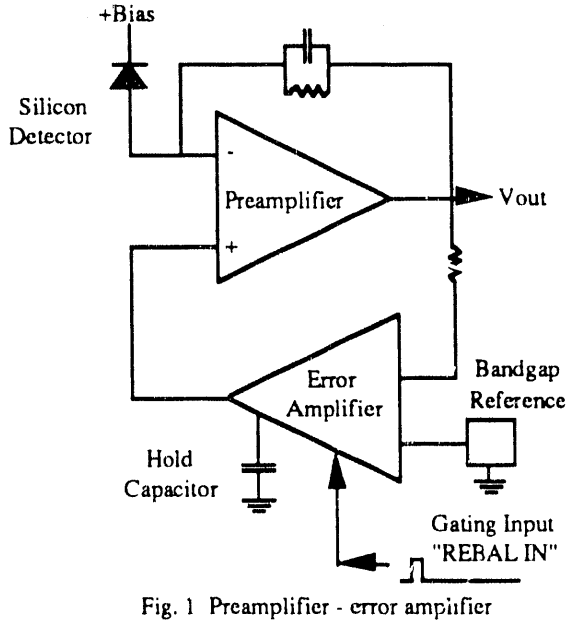

Fig. 1 Preamplifier - error amplifier Block Diagram

Table 1. Results of Tests (C_d=100pF)

Condition	Risetime	Power (+/-3.5 V)	ENC_e (60 ns Peaking)
Pre-rad	6.3 ns	7.5 mW	6300 erms
5.3 Mrad	20 ns	2.1 mW	6600 erms
5.3 Mrad 4 hrs. 100°C anneal	9 ns	5 mW	6800 erms

Circuits Fabricated Through Harris

Seven preamplifier designs for silicon calorimetry were implemented in a dielectrically isolated bipolar VHF Process using the Harris Semiconductor FASTRACK design system. The process used 1.2 GHz npns and 1.0 GHz pnps with breakdown voltages of ~ 20 V. All preamplifiers were charge-sensitive designs with feedback components on the chip. Each packaged chip housed four identical preamplifiers in a 16-pin, ceramic, leadless chip carrier. Three topologies were implemented with designs tailored for detector capacitances ranging from 20 pF to 500 pF. Power dissipation on all designs was typically < 20 mW for ±5 V power supplies. The designs featured low noise performance, radiation hardness, low power dissipation, wide dynamic range, minimum external parts count, and direct-coupled input connections. The dimensions and pad placements of all chips were physically and functionally identical to streamline wafer probe testing on the multi - project wafers.

Folded Cascode topology

Three quad preamplifier circuits were designed with a folded cascode input topology, having been optimized for detector sizes of 1 x 1, 2 x 2, and 3 x 3 cm^2 fully-depleted 400 μm silicon. The folded cascode topology exhibits the lowest input noise for given input device size and collector current of the three topologies. The output dc voltage was offset toward the positive supply voltage, V_{cc}, to maximize the useable dynamic range of the negative-going pulses using high-valued pinch resistors in the feedback network. A resistor was connected in series with the emitter of the input transistor in the case of the lowest detector capacitance (the 1 x 1 cm^2 design) to stabilize the circuit at the expense of additional noise. A feedforward path using a p-channel JFET was added from the input node to the dominant node to improve large signal response and to establish the amplifier's dc bias currents. The JFET was preferred over a pnp device because of its low gate leakage current when compared with the base current of the pnp after radiation exposure.

Current Feedback Topology

Two quad preamplifier circuits were designed with a current feedback topology, having been optimized for detector sizes of 1 x 1 and 2 x 2 cm^2 fully-depleted 400 μm silicon. The circuit was similar to the VTC chip without the bandgap reference circuit; the positive input node was connected to an internal bias voltage. Input device emitter currents were established using a p-channel JFET based current source with improved current mirrors to stabilize bias currents under post-radiation, low-beta conditions. Again, the output dc voltage was offset toward the positive supply voltage, V_{cc}, to maximize the useable dynamic range of the negative-going pulses. All feedback components are implemented on the chip with only external bypass capacitors at the positive input nodes required.

Differential Topology

Two quad preamplifier chip designs using the differential topology were implemented for detector sizes of 3 x 3 and 4 x 4 cm^2. For 400 μm detector thickness, these sizes correspond to 243 pF and 432 pF detector capacitances. Among the advantages of the differential topology are the

Table 2. Simulation results for the charge-sensitive bipolar preamplifiers using Harris' VHF process. C_d is detector capacitance for 400 um thickness, fully-depleted silicon; ENC_e (equivalent noise charge) is given in rms electrons at -20° C including ballistic deficit effects for a CR-RC peaking time of 50 ns; P_d (power dissipation) is given for ±5 V supplies; t_r (rise time) given for 10 mV output signal.

Preamp Type	Folded Cascode			Current Feedback		Differential	
Detector Size	1x1	2x2	3x3	1x1	2x2	3x3	4x4
C_d (pF)	27	108	243	27	108	243	432
ENC_e	4152	5001	7868	7619	9023	13,750	19,200
P_d (mW)	18.2	19.5	19	15	15	23.5	23.5
t_r (ns)	3.5	3.3	5.4	2.4	6.7	5.6	4.2
Ext. Cap. ?	NO	NO	NO	YES	YES	YES	YES

excellent dc bias resulting from a symmetrical design, and the high loop transmission possible with large detector capacitances. The series noise performance is dominated by the two input devices and as such is higher than in the folded cascode case for equivalent device sizes and emitter currents. Emitter resistors were added in the 3 x 3 cm^2 case for stability without degrading the large signal slew rate. The positive input node reference voltage is established from an internal bias network with an external 0.01 µF bypass capacitor to ground. The collectors of the input differential npns connect to pnp folded cascode stages with an improved current mirror in one path for bias stability under post-radiation conditions.

Performance Comparisons

Based on simulations using device models provided by Harris Semiconductor, Table 2 lists noise performance, transient response, and power dissipation results for the three circuit types as applied to the various detector sizes. The folded cascode topology is clearly the design of choice: the noise performance is superior, no external reference bypass capacitors are required, power dissipation and output dynamic range are comparable to the other designs, and component count (thereby required chip area) is lower indicating more circuits will be produced per wafer. While the speed of the current feedback design is superior, the response of the folded cascode design is more than adequate for the 7 ns and 22 ns respective electron and hole collection times anticipated for the 400 µm thick silicon detectors when operated at -20° C.

Conclusion

Eight preamplifiers were developed for silicon calorimetry in two different high-frequency bipolar processes. Three different topologies were implemented to evaluate the performance of each under the target conditions. The preamplifier fabricated through VTC was tested, while the preamplifiers currently being fabricated through Harris have been thoroughly simulated.

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