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MICROFABRICATION OF MEMBRANE-BASED DEVICES BY DEEP-REACTIVE ION ETCHING (DRIE) OF SILICON

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ABSTRACT

Deep reactive ion etching (DRIE) of silicon was utilized to fabricate dielectric membrane-based devices such as microhotplates, valves and flexural plate wave (FPW) devices. Through-wafer DRIE is characterized by fast etch rates (~3 μm/min), crystal orientation independence, vertical sidewall profiles and CMOS compatibility. Low-stress silicon nitride, a popular membrane material, has an appreciable DRI etch rate. To overcome this limitation DRIE can be accompanied by a brief wet chemical etch. This approach has been demonstrated using KOH or HF/Nitric/Acetic etchants, both of which have significantly lower etch rates on silicon nitride than does DRIE. The DRIE etch properties of composite membranes consisting of silicon dioxide and silicon nitride layers are also under evaluation due to the higher DRIE selectivity to silicon dioxide.

INTRODUCTION

Microfabricated membranes serve many applications in sensing and actuation. Microhotplates fabricated on thin dielectric membranes benefit from the low heat capacity and thermal conductivity of the membrane (1) and have been used for sub-atmosphere pressure sensing (2), flow sensing (3), calorimetric (4) and conductometric (5) gas sensing and uncooled IR sensing (6). Membranes are also remarkably robust and have been used in pressure sensing (7) and in micromachined valves and pumps (8).

Typically, membrane-based devices are microfabricated by front or reverse side wet chemical etching, a process characterized by relatively slow etch rates, crystallographic dependence, consumption of precious wafer real estate and potential CMOS incompatibility. Surface micromachined membranes overcome these limitations, but have small underlying air gaps, usually no greater than 2 μm, which can be restrictive for certain applications. For instance, significant heat transfer by air conduction occurs between surface micromachined heaters and the underlying substrate, limiting the thermal efficiency of these devices (9).

DISCLAIMER

We have used through-wafer DRIE to fabricate membrane-based devices such as microhotplates, flow and temperature sensors, and FPWs. Fabrication steps, as well as characteristics and limitations of this method are described.

BASIC FABRICATION

The basic process flow for fabricating dielectric membrane devices by DRIE is outlined in Figure 1. Processing commences with a silicon substrate coated with a suitable membrane material (Figure 1a). Although any number of membrane materials can be used, low-stress silicon nitride was initially chosen for its good mechanical properties, chemical resistance and low thermal conductivity.

For FPWs and microhotplates, the front side of the wafer is metallized, patterned, and annealed if necessary (Figure 1b). At this point, a thin layer of photoresist should be deposited over the metal for protection during subsequent processing.

In step (c) the membrane etch mask is patterned in thick photoresist (such as AZ4903) on the reverse side of the wafer using back-side aligning . After dry etching the SiN, the silicon is etched via DRIE using the Bosch process. Etching is halted once the membrane material is reached.

Microhotplates produced by this method are shown in Figures 2 and 3. In Figure 3 a packaged die containing three DRI etched microhotplates is illustrated. At the left and right hand sides of the die are two small microhotplates 0.5 mm on a side; in the center of the die is a large microhotplate 2.75 mm on a side. These three microhotplates could be used in conjunction for three-wire hot anemometry. If only one membrane had been used, thermal cross talk by conduction between the three devices would limit flow sensitivity. However, by placing the three heater/thermometers in on their own membranes, cross talk is virtually eliminated. It should be observed that DRIE has permitted the close spacing of the membranes. Such proximity is not possible via wet etching of {100} silicon with wet anisotropic etches like KOH due to the shallow angle (54.74°) formed between the exposed {111} planes and the wafer surface.

COMBINED DRI/WET ETCHING

A thin layer of silicon often remains near the edges of a membrane after DRIE (Figure 4). This residual silicon, often referred to as the silicon "foot", is problematic for microhotplates and FPW devices. In the former case, the efficiency and speed of the hotplate is compromised by the heat conduction and heat capacity of the silicon. In the latter, the edge boundary condition of the membrane is poorly defined, and the acoustic modes are affected. Simple overetching to remove the foot is not an option due to the finite silicon nitride etch rate.

DRIE can be followed by a brief wet chemical etch to remove the residual silicon. After DRI etching to the membrane, the wafer is briefly inserted into a wet etch bath containing a common silicon etchant like aqueous KOH or HF/Nitric/Acetic mixtures. Since these solutions have superior etch selectivity of silicon over silicon nitride, it is possible to remove the foot without significantly etching the membrane.

The shape and orientation of the membrane can be a concern during KOH etching if

there is a significant amount of silicon remaining. One side of square membranes should be roughly aligned to the {100} wafer flat to avoid unwanted widening of the etch pit as {111} planes are exposed (Figures 5 and 6). Of course, circular membranes etched by DRIE will begin to take on a polygonal shape in KOH etching. If only a small foot remains, this shape modification may not be a problem depending on the intended application of the membrane device.

HF/Nitric/Acetic etches, sometimes called CP-4 or CP-8 depending on the relative concentration of the acids, can also be used to remove the silicon foot. Since they are isotropic etchants for silicon, the orientation problems noted above for KOH are not present with CP-x. However, CP-x also aggressively attacks many metals, including the common Ti sticking layer. Thus, steps must be taken to protect metals from this etchant and this can be a serious limitation of this approach.

COMPOSITE MEMBRANES

The DRI etch rate of SiO_2 is roughly one third that of silicon nitride (Table 1). At first glance, then, silicon dioxide would appear to be a superior membrane material for DRI etched membranes, since overetching could be used to remove the silicon foot without significant danger of etching through the membrane. Unfortunately, residual stress in oxide films is compressive, and silicon dioxide membranes tend to buckle.

A composite membrane material consisting of nitride on top of oxide should be useful as a DRI etched membrane material. The tensile stress of the silicon nitride compensates the compressive stress in the silicon dioxide. Furthermore, the oxide layer serves as an etch stop for the DRIE and overetching can be safely performed to clear any remaining silicon. Composite films of 1000Å of thermally grown silicon dioxide and 5000 Å of PECVD silicon nitride are currently under investigation. Also being studied are etch rates of oxynitride films.

MICROHOTPLATE PERFORMANCE

Two essential characteristics of microhotplates are time response and steady-state power consumption. The time response of a DRIE etched membrane to a square voltage pulse is shown in Figure 7. The device reaches 200 °C in less than 8 ms. Only 54 mW of applied power is required in the steady state.

CONCLUSIONS

DRIE is a promising technique for the fabrication of membrane based devices on silicon. The rapid etch rate, crystal orientation independence, vertical side walls, and CMOS compatibility of this technique lend it significant advantages over front or reverse side wet chemical etching. Vertical sidewalls and orientation independence, for instance, allow for closer proximity of membranes and a reduction in consumed wafer area. The large, wafer-thick air gaps beneath DRIE etched membranes give them two main advantages over surface micromachined membranes: enhanced thermal efficiency for microhotplates and increased deflection distance for pressure sensors and valves. Finally, both dielectric membranes and silicon membranes can be fabricated by this technique.

Poor etch selectivity of DRIE to silicon nitride, a popular membrane material, is an

apparent disadvantage to this technique. Combined DRI/wet etching overcomes this limitation while maintaining most the advantages of DRIE. Composite oxide/nitride layers as well as oxynitride films are currently under investigation for fabrication of membranes using DRIE.

ACKNOWLEDGMENTS

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FIGURES

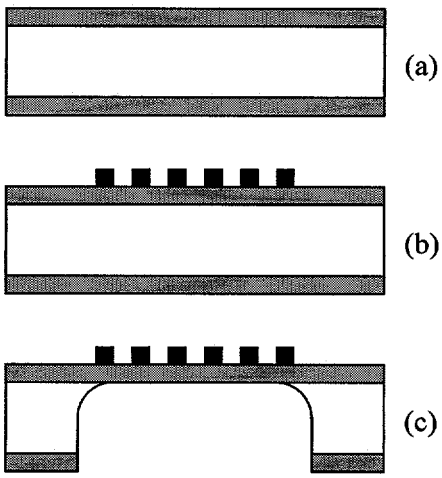

Figure 1: DRIE processing sequence for dielectric membrane devices.

Table I

Material	Etch Rate
Silicon {100}	3 μm/min
Thermal SiO_2	91 Å/min
LPCVD SiN	295 Å/min
PECVD SiC	180 Å/min

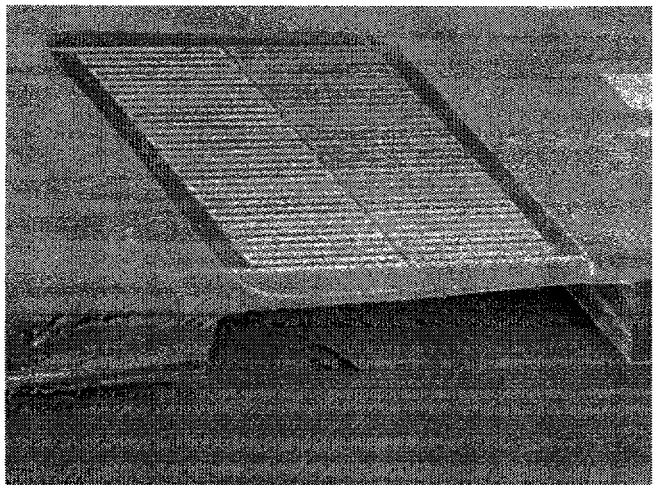

Figure 2: SEM cross section of a DRIE dielectric membrane microhotplate with a Pt heater. The membrane is 2.75 mm on a side.

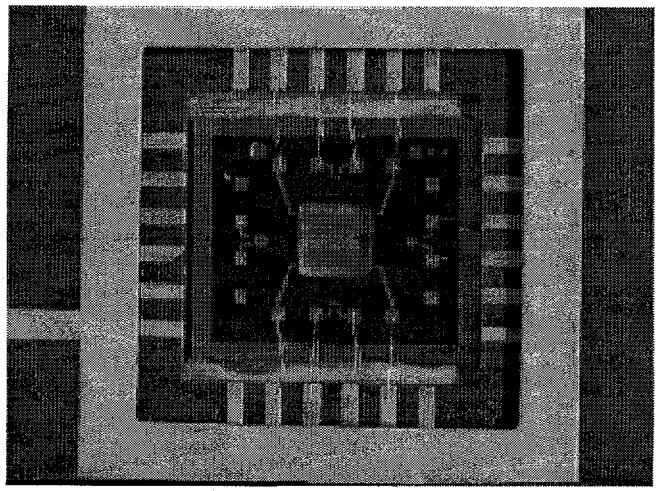

Figure 3: Photograph of a 24-PIN DIP packaged die with DRIE etched components. In the center, a Pt heater is placed on a dielectric membrane; the DIP well can be viewed through the transparent membrane. At left and right are temperature sensors placed on their own membranes for thermal isolation purposes.

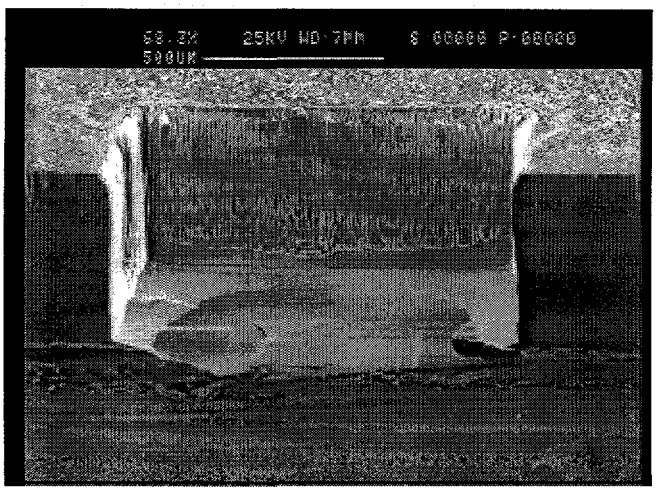

Figure 4: Cross section SEM of a DRI etched FPW device. (During dicing the membrane cracked.) For illustration purposes the FPW is inverted such that the bottom of the wafer is at the top of the SEM. Metal lines can be seen through the thin membrane. Also noticeable is a thin layer of silicon remaining near the membrane edges.

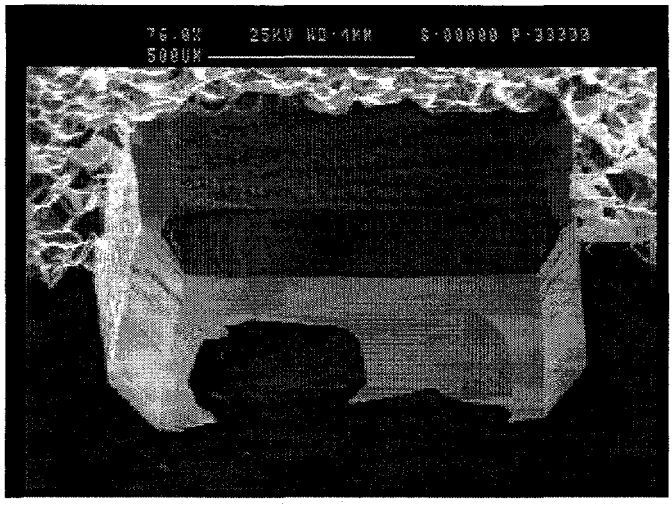

Figure 5: SEM view of a membrane produced by DRIE/KOH etching. The brief wet etch has revealed the {111} planes and reduced the size of the Si foot. With continued wet etching, the foot disappeared. The roughness on the back side of the wafer is due to KOH etching of the Si through pinholes in the nitride; the pinholes resulted from anomalous photoresist failure during DRIE.

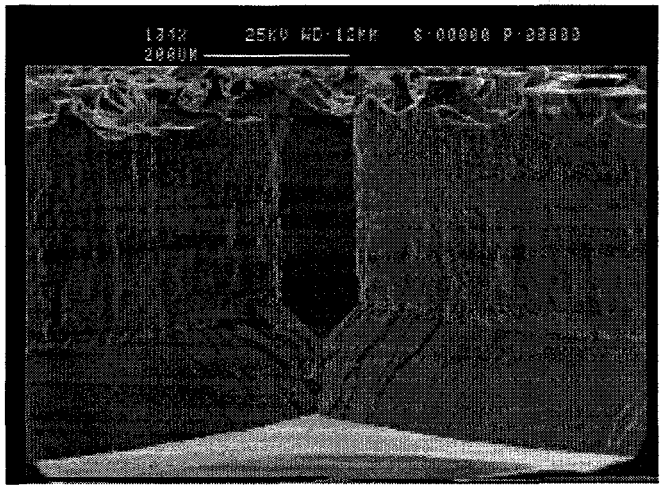

Figure 6: SEM close up of the etch pit corner of Figure 5. KOH is gradually revealing the {111} planes and reducing the size of the Si foot.

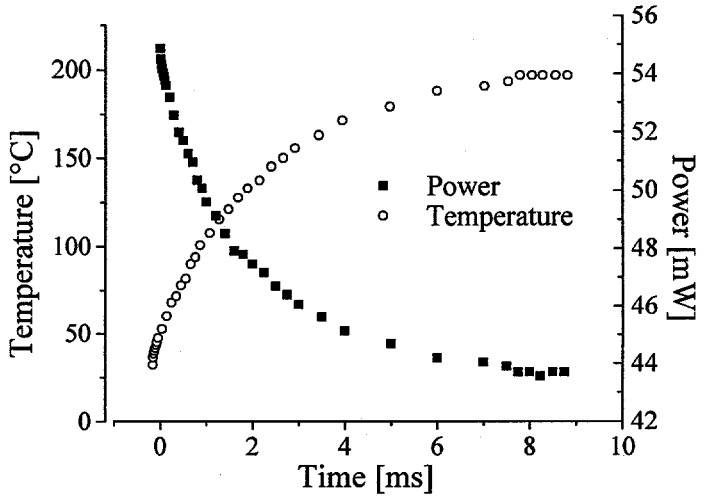

Figure 7: The time response of a 1 mm square hotplate to a square voltage pulse.