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AUTOMATED ARRAY ASSEMBLY, PHASE II

Final Report for the Period October 1977—December 1979

By
R. V. D'Aiello

October 1980
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Work Performed Under Contract No. NAS-7-100-954868

RCA Laboratories
Princeton, New Jersey

U.S. Department of Energy

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AUTOMATED ARRAY ASSEMBLY, PHASE II

October 1977 through December 1979

R. V. D'Aiello
RCA Laboratories
Princeton, New Jersey 08540

FINAL REPORT

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Prepared Under Contract No. 954868 For

JET PROPULSION LABORATORY
CALIFORNIA INSTITUTE OF TECHNOLOGY
Pasadena, California 91103

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PREFACE

This Final Report, prepared by RCA Laboratories, Princeton, NJ 08540, describes the results of work performed from September 1, 1977 to December 31, 1979 in the Energy Systems Research Laboratory, B. F Williams, Director; Materials and Process Laboratory, Solid State Division, Somerville, NJ, R. Denning, Manager; and at the Advanced Technology Laboratory, Government and Commercial Systems, Camden, NJ, F. E. Shashoua, Director. The Project Scientist is R. V. D'Aiello and the Project Supervisor is A. H. Firester, Head, Process and Applications. Others who participated in the research and writing of this report are:

E. C. Douglas	-	Ion implantation
J. Murr	-	Screen printing
W. Kern, E. Tracy, W. Kurylo	-	Spray-on AR coating
R. Daniel	-	Cost analysis
M. Couthamel, G. Lazzery, R. Coyle	-	Interconnect and panel assembly
L. Guarino	-	Processing
G. Nostrand	-	Cell testing and test system design

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SECTION I

SUMMARY

This final report contains the integrated results of a program conducted at RCA during the period September 1, 1977 to December 31, 1979. The work comprised phase II of a continued program (Automated Array Assembly, Phase I) and had an overall objective of specifying a process sequence which, when automated, would have the potential of mass producing silicon solar panels within the DOE/JPL price guideline of $0.70/W.* Such a manufacturing sequence was specified, verified, and cost-performance analysed during this program. The details of our process-sequence studies concluding with a description of the recommended sequence are given in Section V. Additional highlights which resulted from this program include (1) a comprehensive study of ion implantation applied to solar-cell processing, (2) successful development of a thick-film screen-printed metallization process, and (3) successful development and verification of a cost-effective spray-on AR coating process.

The total program consisted of three parts, (1) process assessment of previous work conducted at RCA and by other contractors who participated in the LSA - Task IV program, (2) process development for those processes selected from part (1) for which it was decided that additional improvement or verification was required, and (3) process sequence verification, which entailed a 9-month production study of three process sequences assembled from the most promising of the processes which emerged from parts (1) and (2).

The specific processes which were evaluated and studied in detail were:

(1) Junction Formation

  (a) Ion-implantation with furnace anncal
  (b) $POCl_3$ gaseous diffusion
  (c) Spin-on liquid dopant with furnace anneal

(2) Screen-Printed Thick-Film Metallization

(3) Spray-On Antireflection Coating

*All prices and costs in this report are given in 1980 dollars.

(4) Cell Interconnect

(a) Parallel-gap welding

(b) Reflow solder

(5) Double-Glass PVB Panel Assembly

Section III of this report describes the technical studies conducted on junction-formation processes, screen-printed thick-film metallization, and spray-on AR coating. A brief summary of those studies follows.

A thick-film, screen-printed metallization process was successfully developed for both front and back solar-cell contacts. This included the synthesis of screen-printable silver-based inks, evaluation of commercially available inks, and the verification of a back-contact aluminium p^+ process. A production-type screen printer was used to provide verification for the application of this process to large-scale production, including the adaptation of infrared lamps for the firing of the front and back contacts.

A cost-effective spray-on process was developed for the application of AR films. Liquid solutions were developed specifically for spray applications, and the overall process was verified with a commercial autocoater. SAMICS cost analyses show a projected price of \$0.01 to \$0.02/W for such a spray-on AR process.

The bulk of the work was centered on ion implantation since it had very promising long-range cost potential, but at that time, the performance of solar cells made by the existing implant and anneal techniques was below both performance obtainable from gaseous diffusion and that theoretically expected. As a result of extensive experimentation in which the ion-implant parameters were systematically varied, a set and range of these parameters were found which allow for the fabrication of high-efficiency solar cells having ion-implanted junctions. To obtain these results, two furnace annealing processes were used. The successful use of the first of these provided a verification of a three-step furnace annealing technique provided to the LSA program by Spire* [1]. An alternate and equally effective process involving a back-surface boron-glass furnace gettering technique was developed and verified.

Since junction formation by gaseous diffusion from a $POCl_3$ source is an established process for solar-cells and other shallow-junction silicon devices, our work in this area was devoted to establishing the processing parameters

*Spire Corp., Bedford, MA.

1. Spire Corporation, Development of Pulsed Processes for the Manufacture of Solar Cells, Quarterly Progress Report No. 4, QR-77-10052-4, DOE/JPL 954786, January 1979.

necessary to form a junction-layer compatible with the requirements of the firing schedule in the thick-film screen-printed metallization process. This process was established with the latter requirement being of paramount importance for establishing a complete internally compatible manufacturing sequence.

Liquid dopants were examined by studying the applicability of several commercial sources. Aqueous-based sources were found to be superior to sources with an alcohol base. One such source containing phosphorus was found very suitable for junction formation when spun on the wafers followed by a furnace anneal temperature/time cycle of 850°C for 50 min. Solar-cell efficiencies of 13.4 to 14.2% were achieved and, in addition, in separate tests it was shown that aqueous-based sources could be rolled or screened onto the wafers with satisfactory coverage and resultant junction quality.

Similar liquid sources containing boron were evaluated for back-surface field (BSF) and back contact formation. These sources were found incompatible with the combined use of phosphorus sources at the anneal temperature of 850°C. At higher anneal temperatures (900 to 1000°C) the boron became activated but control of the front junction depth was lost.

Section IV contains a complete description of the processes studied and those developed for cell interconnection and for the lamination of double-glass PVB panels.

Parallel-gap welding was examined for use on cells metallized with evaporated Ti/Pd/Ag (reference case) and on cells with screen-printed silver grid and back contacts. It was found that the weld parameters could be adjusted to obtain adequate bond strengths* on the evaporated metallization, but control of the weld parameters to achieve reproducible bonds to the screen-printed contacts could not be obtained.

A reflow solder process was developed which is centered around the use of a radiantly heated mass reflow solder assembly capable of the reflow-interconnect of standard size arrays at the rate of 1 linear ft/min. The entire process consists of screen-printing solder paste onto the cells, formation and solder-attachment of tabs, array layout, transfer of array to the radiant-heat reflow table, and reflow soldering of the entire array.

The work required to find suitable processes for laminating the double-glass PVB structure was more difficult than anticipated at the beginning of

*In 45° pull tests, bond strengths up to 4 lb were obtained.

this program. Standard laminating processes used in the safety glass industry were tried and found not to work because of the presence of the cells between the glass. Use of a vacuum bag in conjunction with autoclaving allowed the identification of the process parameters required to form successful laminates. This process was slow and made inefficient use of the autoclave. This led to the development of a two-step process in which the vacuum bagging is done outside the autoclave. The autoclave can then be used efficiently for curing many laminates at once.

Section V describes our manufacturing sequence studies. Three sequences were studied in detail. In these sequences the solar-cell fabrication was based on ion-implanted junctions, furnace annealing, screen-printed contacts, and spray-on AR coating. The starting material was primarily "solar-grade," n and p-type 3-in.-diameter silicon wafers, with about 500 solar cells fabricated in each sequence. In addition, a quantity of dendritic web* was evaluated for its ability to withstand the mechanical stress associated with the screen-printing and firing process steps.

As a result of this work, two problem areas common to the three sequences were identified relating to materials and process compatibility. Because of these problems, these sequences cannot be recommended on a technical basis. However, a modification of one of these sequences emerged from this work which was found to have interprocess compatibility and to work well with the starting "solar-grade" wafers. This sequence is described and is the one we recommend on the basis of both performance and cost.

In Section VI, the results of applying SAMICS analyses to all manufacturing sequences studied are given. In this section, it is shown that the recommended sequence when used in conjunction with 6-in.-diameter advanced Czochralski (CZ) wafers results in a price of $0.688/W. The differences resulting from using 3-in.- and 6-in.-diameter wafers are described, and the calculated prices for all sequences studied are given. Some compromises between the 3-in.- and 6-in.-diameter cases are possible if the costs of some process steps can be reduced. The sensitivity of the results to yield and throughput are also discussed.

Finally, all of the major conclusions of this work are summarized in Section VII.

*Purchased from Westinghouse Research and Development Center, Pittsburgh, PA.

SECTION II

INTRODUCTION

Figure 1 is a schematic representation of the work of the first year. The philosophy of this plan was to establish an experimental process line starting with 3-in.-diam silicon wafers and consisting of junction formation using $POCl_3$ gaseous diffusion, screen-printed thick-film metallization, reflow solder interconnect, and double-glass lamination panel assembly. This experimental production line produced a sufficient number of solar cells to demonstrate the technological readiness of each of those process steps. Variations (of each process) were made to set limits on the usable range of each process step and to determine the interaction with adjoining steps. Inspections, measurements, and tests were included to determine the output requirement characteristics of each step, obtain statistical variations, and evaluate the performance of the solar cells and panels. A description of this work, which was conducted from October 1977 through December 1978, is given in Sections III and IV.

This was followed by an 18-month study in which three manufacturing sequences synthesized from the above work and from studies conducted by other participants in the LSA program were exercised. The objectives were to assess the compatibility between process steps for each sequence, to generate sufficient data for comparative SAMICS cost analysis, and to make recommendations of the suitability of one or more of these sequences for the large-scale automated production of solar cells within the cost goal of $0.70/pW. The detailed experimental results of this study are described in Section V, followed by SAMICS cost analysis, recommendations, and conclusions given in Sections VI and VII.

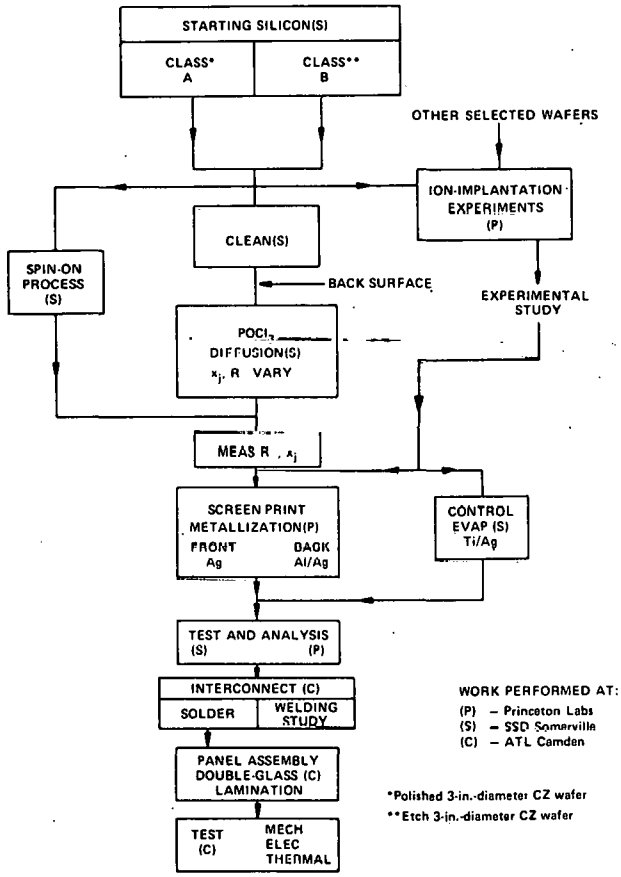


Figure 1. Block diagram of process sequence.

SECTION III

PROCESS STUDIES

In this section we will discuss the technical progress achieved in all the major process steps (see Fig. 1).

A. JUNCTION FORMATION

1. $POCl_3$ Diffusion

Diffusion from a $POCl_3$ source is a standard industrial method and has been used extensively for fabricating solar-cell junctions. Our data indicate that high performance cells with conventional evaporated Ti/Ag contacts can be made from $POCl_3$ junction diffusions 0.3 μm deep having a sheet resistance in the range of 30 to 200 ohm/square. In this work, experimental lots were made to determine the range of sheet resistance and junction depth which are consistent with the requirements for both the screen-printed contact metallization process and cost-effective performance of the solar cells. Phosphorus surface concentration and junction depth were varied by controlling the temperature of the $POCl_3$ liquid source and by adjusting the diffusion schedule.

This process was rapidly developed and extensive research on the process was not continued. Rather the process was used throughout the contract as a baseline reference against which other junction-formation processes were compared. Full details of the process were submitted to JPL in a Process Specification.

We ran more than 50 lots of wafers (10 to 50 wafers/lot) with various diffusion parameters. These runs are shown in Table 1. Selected wafers from each lot were reserved as standards for evaporated metal contacts. The remainder of the wafers were used for tests of screen printing of metallization.

These test results described in Section III.B.8 and V.C.2 show that for Ag-based screen-printed grid metallization, best cell performance in terms of acceptable fill factors is achieved with $POCl_3$ diffusions yielding sheet resistance values of less than 30 Ω/□.

2. Ion Implantation

Our earlier LSA experience showed that the ion-implantation process for junction formation required significant design and development effort.

TABLE 1. PROCESSING PARAMETERS FOR $POCl_3$ DIFFUSION

Lot No.	$POCl_3$ (°C)	N_2 (CFH)	O_2 (CFH)	$POCl_3$ Carrier O_2 (CFH)	$POCl_3$ Push (min)	$POCl_3$ Warm (min)	$POCl_3$ Deposit (min)	$POCl_3$ Drive (min)	$POCl_3$ Pull (min)	$POCl_3$ Temp (°C)
033	20	5	.5	.5	15	10	20	30	10	850
034	0	5	.5	.5	10	10	45	10	10	850
035	0	5	.5	.5	10	10	45	10	10	850
036	0	3.9	.35	.35	10	20	20	30	10	850
037	0	3.9	.35	.35	10	20	20	30	10	850
038	0	3.9	.35	.35	10	20	20	30	10	850
039	0	5	.5	.5	10	10	20	30	10	850
040	0	5	.5	.5	10	10	20	30	10	850
041	0	5	.5	.5	10	10	20	30	10	850
042	0	5	.5	.5	10	10	20	30	10	850
043	0	5	.5	.5	10	10	20	30	10	850
044	0	5	.5	.5	10	10	20	30	10	850
046	0	5	.5	.5	10	10	20	30	10	850
047	20	5	.5	.5	15	10	20	30	10	850
048	3	5	.5	.5	20	10	20	30	4	850
049	-6	5	.5	.5	10	10	20	25	10	850
050	0	5	.5	.5	15	10	20	25	10	850
051	0	5	.5	.5	15	10	20	22	10	850
055	0	5	.5	.5	15	10	20	22	10	
056	0	5	.5	.5	15	10	20	22	10	
057	26	5	.05	.5	15	10	20	30	10	850
058	26	5	.05	.5	15	10	20	30	10	850
059	25	5	.05	.5	15	10	20	30	10	850
060	26	5	.05	.5	15	10	20	22	10	850
061	0	5	.5	.5	15	10	20	22	10	
062	0	5	.5	.5	15	10	20	20		
064	30	5	.05	.5	15	10	20	30	10	850
065	30	5	.05	.5	15	10	20	30	10	850
066	26	5	.05	.5	15	10	20	30	10	850
069	30	5	.05	.5	15	10	20	30	10	850
070	26	5	.02	.5	15	10	20	30	10	850
071	26	5	.02	.5	15	10	20	30	10	850
076	--	5	0	--	30	--	--	45	30	925
		Simultaneous n and p drive - furnace mouth cool 120 min								
077	--	5	0	--	30	--	--	45	30	925
		Simultaneous n and p drive - furnace mouth cool 120 min								

TABLE 1. PROCESSING PARAMETERS FOR $POCl_3$ DIFFUSION (Continued)

Lot No.	$POCl_3$ (°C)	N_2 (CFH)	O_2 (CFH)	$POCl_3$ Carrier O_2 (CFH)	$POCl_3$ Push (min)	$POCl_3$ Warm (min)	$POCl_3$ Deposit (min)	$POCl_3$ Drive (min)	$POCl_3$ Pull (min)	$POCl_3$ Temp (°C)
078	25	5	.02	.5	15	10	20	30	15	805
079	25	5	.5	.5	15	10	20	30	15	794
080	25	5	.5	.5	15	10	30	30	15	794
081	25	5	.5	.5	15	10	40	30	15	794
082	25	5	.05	.5	15	10	40	20	15	794
083	45	5	.5	.5	10	10	30	60	10	794
084	45	5	.05	.5	15	10	30	60	15	794
085	Room	.5	.05	.05	10	10	40	90	10	854
086	Room	4.5	1.0	N_2 Carrier .5	10	10	40	90	10	850
087	27	5	.5	N_2 Carrier .5	10	10	20	30	10	850
088	27	5	.5	.5	10	10	20	30	10	850
090	Room	4.5	1.0	.5	10	10	20	30	10	850
091	Room	4.5	1.0	N_2 Carrier .5	10	10	20	30	10	850
092	Room	4.5	1.0	N_2 Carrier .5	10	10	20	30	10	850
093	40	5	.5	N_2 Carrier .5	10	10	20	30	10	850
094	45	5	.5	.5	10	10	20	30	10	850
095	45	5	.5	.5	10	10	20	30	10	850
096	35	5	.5	.5	10	10	20	30	10	850
097	30	5	.5	.5	10	5	20	30	10	850
098	45	5	.5	.5	10	10	20	30	10	850
099	45	5	.5	.5	10	10	20	30	10	850
100	46	5	.5	.5	10	10	20	30	10	850
101	45	5	.5	.5	10	10	20	30	10	850
103	45	5	.5	.5	10	10	20	30	10	850
104	45	5	.5	.5	10	10	20	30	10	850
107	45	5	.5	.5	10	10	20	63	10	850

Accordingly, we planned a separate and intensive study of the implant process and its interaction with wafer quality and subsequent contact metallization. The details of that study are listed in Table 2.

TABLE 2. ION-IMPLANTED SOLAR-CELL EXPERIMENTS

Wafers Parameters to be Tested

- Orientation <100> vs <111>
- Background Doping Level
- Starting Defect Level
- n-Type Wafers vs p-Type Wafers

Implant Parameters to be Tested

- Implant Voltage
- Dose Level
- Dose Rate
- Species (^{11}B, ^{31}P, ^{75}As)

Process Parameters to be Tested

- Anneal Temperature
- Anneal Time
- Type of Cap
- Gettering
- Contact Problems (Screen Print to Implanted Layers)

Measurements to be Made

- Illuminated I-V Curves — Conversion Efficiency, Fill Factor
- Quantum Efficiency — V_{oc} vs $J_{sc} \rightarrow J_o$
- Dark I-V Curves
- Forward-biased Recovery Lifetime in Diodes
- Reverse-biased Recovery Lifetime in Capacitors
- Diffusion Length Measurements

a. Background - Ion-implantation fabrication techniques are predicted to be among the least expensive technologies for fabricating silicon solar cells. We investigated the ion-implant conditions and suitable post-implantation annealing steps which can be used to yield p-n junctions of sufficient quality to form efficient

solar cells. When implantation is used to introduce dopant atoms into a substrate, not all of the atoms are initially electrically active, i.e., not all the atoms are located on substitutional lattice sites, and in addition, damage is introduced into the substrate lattice. High-temperature anneal steps (800 to 1000°C) are usually used to activate the implanted atoms and to reduce or eliminate the implant damage. These high-temperature steps can degrade the minority carrier diffusion length in the bulk of the wafer and, hence, can degrade the conversion efficiency of the resulting solar cell. This situation is aggravated by the fact that gettering effects which usually accompany diffusion processing are either minimal or are absent from the anneal procedures used on ion-implanted layers.

The solar cells made during the course of this experimental study were fabricated using high-quality semiconductor grade silicon wafers and optimum masking, capping, and metallization techniques. The object was to minimize as much as possible the potential conflicting factors which may interfere with the study of implantation effects that might adversely affect the performance of implanted solar cells.

This section describes the results of experiments which were designed to investigate the factors which influence the performance of ion-implanted silicon solar cells. As a result of these experiments, a process specification was written and is available upon request from the Processes and Equipment Development Area of the JPL-LSA Project. This processing procedure can be used to produce solar cells with up to 15% conversion efficiencies. The factors which were investigated include: (1) implant dose, (2) implant energy, (3) implant species, (4) various processes for forming the backside contact layer and at the same time improving diffusion length in the bulk, (5) substrate orientation, and (6) substrate resistivity.

The performance of the solar cells was evaluated under standard AM-1 conditions by measuring the open-circuit voltage V_{oc}, the short-circuit current I_{sc}, and the maximum power values I_m and V_m for cells. From these data were calculated the values of the cell fill factor

$$FF = \frac{I_m V_m}{I_{sc} V_{oc}} \tag{1}$$

and conversion efficiency

$$\eta = \frac{I_m V_m}{\Phi A} \tag{2}$$

where Φ = 100 mW/cm^2 under standard AM-1 conditions and A is the area of the solar cell.

In addition to the basic performance parameters, on selected cells the diffusion length was measured in the starting wafer, using a surface photovoltage technique [2], and in the finished cell, using curve-fitting techniques on the cell quantum efficiency data [3]. These diffusion lengths were used to evaluate effectiveness of the anneal procedures employed in the fabrication of the cells.

The mask set used to fabricate the solar cells produces not only solar cells of various sizes, but also produces diodes of various sizes so that both light and dark I-V curves could be constructed for selected cells. From these I-V curves, the values of the parameters in the diode equation [4]

$$J = J_{o1}\, e^{\left(qV/kT - 1\right)} + J_{o2}\, e^{\left(qV/nkt - 1\right)} \tag{3}$$

$$\cong J_{o1}\, e^{qV/kT} + J_{o2}\, e^{qV/nkT} \quad \text{for } V >> \frac{kT}{q}$$

can be determined. The values of J_{o2} and n indicate the amount of residual damage left in the junction depletion region by the ion-implant fabrication process. In the experiments reported here, this residual damage was found generally to be small. The value of [4]

$$J_{o1} = q\, n_i^2 \left.\frac{D_n}{N_a L_n}\right|_{\text{bulk}} + \left.\frac{D_P}{N_D L_P}\right|_{\text{emitter}} \tag{4}$$

together with a knowledge of the diffusion length L_n in the bulk region can be used to estimate the effect of recombination in the ion-implanted emitter. For

2. ASTM Tentative Test Method F391 for Minority Carrier Diffusion Length in Silicon by Measurement of Steady-State Surface Photovoltage, 1976 Annual Book of ASTM Stamdards, Part 43, Electronics (1976).
3. The diffusion length L is obtained from a best parameter fit of the measured quantum efficiency data to the diffusion-only equations described by H. J. Hovel, "Solar Cells: Carrier Collection, Spectral Response and Photocurrent," Chapter 2 in Semiconductors and Semimetals, Vol. 11, Edited by Willardson and Beer.
4. A. S. Grove, Physics and Technology of Semiconductor Devices, (Wiley-Interscience, New York, 1967), Chapter 6.

the cells constructed in this study, the recombination in the emitter is found generally to be negligible compared with the diffusion length effect associated with the bulk.

Table 3 represents a synopsis of the tests performed and the conclusions drawn from the various experiments. The major conclusions from the study are:

(1) Diffusion length in the bulk is the dominant factor in cell efficiency.

(2) Gettering and annealing techniques exist which can preserve or improve the diffusion length in the bulk, under implant anneal conditions.

(3) With regard to implantation, no effect was noted that limited cell performance.

In the following sections, the various tests listed in Table 3 will be described in detail.

b. Profiles, Junction Depths, and Sheet Resistance of Ion-Implanted Silicon Solar Cells - A majority of the solar cells described in this report were fabricated using a 5-keV, ^{31}P implant to form the n^+ high-doped layer. This implant was performed using an Extrion Model 200-1000 implantation machine equipped with a standard 3-in. ferris wheel type endstation. This type of endstation uses an x-y mechanical scan to move the wafer through a stationary beam. The endstation operates in a batch processing mode and can implant 26 3-in. cells per batch. The 5-keV implant energy is achieved by decelerating the ion, which are extracted from a hot filament source at 35 keV, with a reversed gradient field in the multigapped "acceleration tube." The dose implanted at 5 keV is usually 2×10^{15} $^{31}P+$ ions/cm^2.

The profiles* which can be expected at 5 keV are shown in Figs. 2 and 3. Figure 2 also shows the profiles which can be expected when selected energies from 5 to 100 keV are used. The wafers with the profiles given in Fig. 2 have received a 900°C anneal in flowing N_2 for 30 min. (The performance of the solar cells resulting from these implants will be discussed in a later section.) The profiles given in Fig. 3 were not annealed and are included in order to show the nature of the 5-keV profile near the surface; Fig. 3 also shows a 5-keV ^{11}B implanted profile.

*The profile measurements were obtained using SIMS (secondary ion mass spectroscopy) analysis.

TABLE 3. SYNOPSIS OF THE ION-IMPLANTED SOLAR-CELL EXPERIMENTS

Parameter Tested	Conclusion
Implant Parameter	
Implant Voltage	The optimum implant energy is in the 5- to 10-keV range.
Dose Level	The optimum dose level lies between 2×10^{15} and 4×10^{15} atoms/cm^2 (used in conjunction with a 5-μm-thick Ti-Al metallization system).
Species (^{11}B, ^{31}P, ^{75}As)	^{31}P in p-type wafers and ^{11}B in n-type wafer yield comparable results. There is no great advantage in using $^{31}P + ^{75}As$ for the n^+ layer.
Wafer Parameter	
Orientation <100> vs <111>	No difference observed.
Starting Wafer Resistivity	For ranges tested (1-2 ohm-cm and 8-12 ohm-cm), resistivity less important than achievable diffusion length after processing. Verified that V_{oc} decreases for increasing resistivity.
Starting Wafer Diffusion Length	Should be large and must not degrade with processing.
n-type vs p-type Starting Wafers	Can achieve slightly higher V_{oc} with p^+ implants into n-type starting wafers.
Anneal Temperature	With the Boron Glass Process B, anneal temperatures between 900 and 1050°C can be used to produce efficient cells.

TABLE 3. SYNOPSIS OF THE ION-IMPLANTED SOLAR-CELL EXPERIMENTS (Continued)

Parameter Tested		Conclusion
Measurement Techniques		
Cell Load Curves	Conversion Efficiency Fill Factor V_{oc} and I_{sc}	Used for basic cell performance evaluation.
Dark I-V Curves Illuminated I-V Curves		Can be used to find J_{ol} values which, in conjunction with bulk diffusion length measurements, can be used to evaluate performance of emitter layer.
Quantum Efficiency Measurements		Can be used to find bulk diffusion length after processing.
Diffusion Length Measurements in Starting Wafers		By comparing starting wafer diffusion length and post-processing bulk diffusion length, can monitor effect of processing on cell performance.

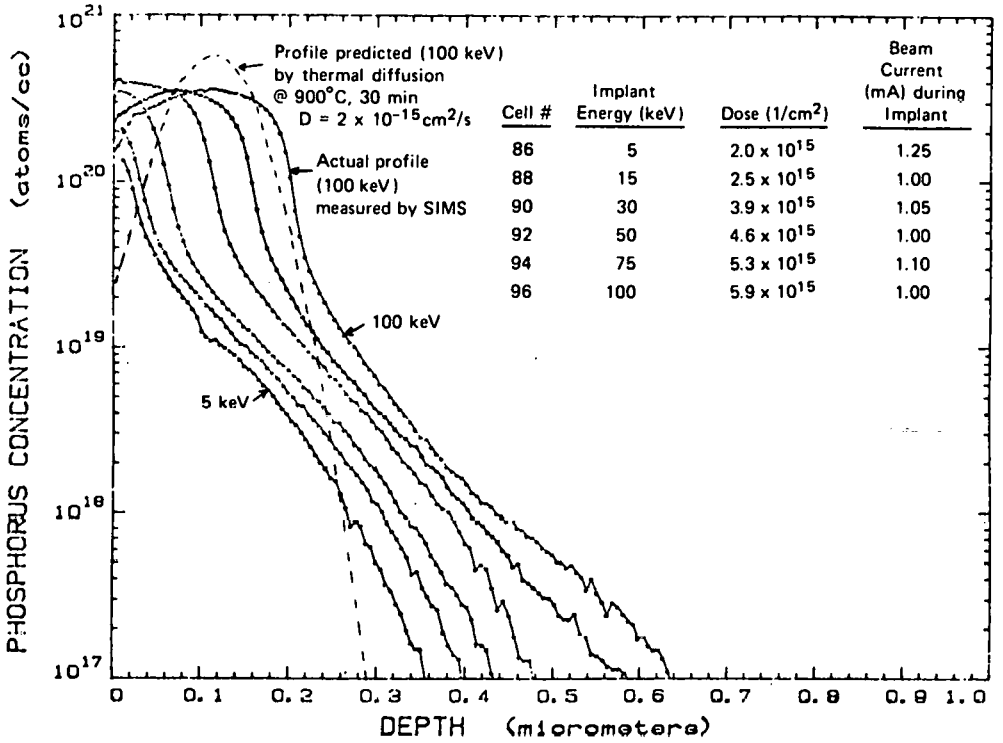


Figure 2. SIMS profile of ion-implanted ^{31}P layers that were used as the n^+ layer in silicon solar cells. The layers were annealed for 30 min at 900°C in flowing N_2.

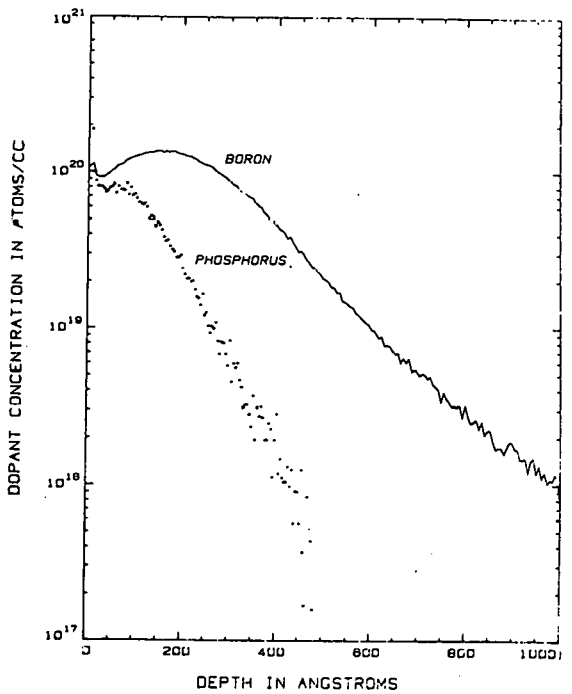


Figure 3. SIMS profiles of 5-keV ion-implanted ^{31}P and ^{11}B. These layers have received no heating steps and represent the as-implanted profiles.

An analysis of the junction depths of the n^+ layers achievable with various implant energies used in conjunction with the 900°C, 30-min anneal sequence is shown in Fig. 4. The measured depths are anomalously deeper than would be expected from a simple diffusion redistribution of the as-implanted profile. The shape of the curve is also not characteristic of profiles obtained from simple diffusion redistribution of ion-implanted profiles [5]. The shape is more characteristic of concentration-enhanced diffusion, which is very likely to be present since the density at the peak of the as-implanted profile (5.65×10^{20}/ cm^3) exceeds the solid solubility of ^{31}P in silicon at 900°C ($N_{max} = 4 \times 10^{20}$/ cm^3). Lowering the dose to avoid concentration-enhanced diffusion causes a deterioration in the cell's efficiency. (This dose effect will be discussed in a later section.) The sheet resistance of the various layers implanted at different energies is given in Fig. 5. The dose of $2 \times 10^{15}/cm^2$ at 5 keV which yields near-optimum cell effiency produces an n^+ layer, after the anneal step, having a sheet resistance of 65 Ω/□.

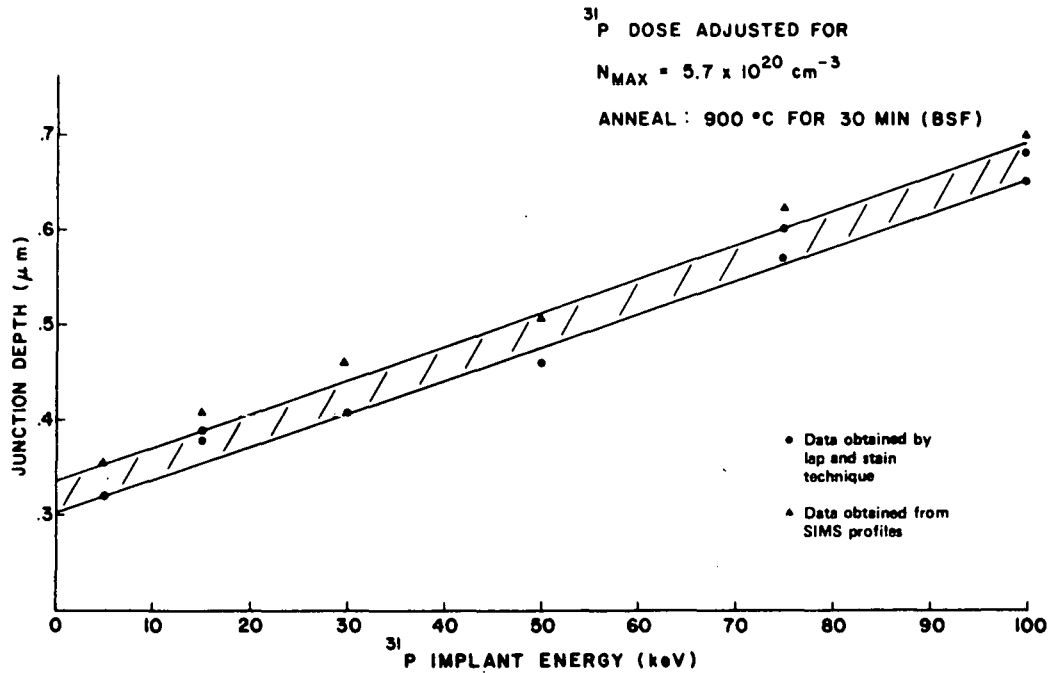


Figure 4. Results of junction depth measurements on ion-implanted layers annealed at 900°C for 30 min in flowing N_2.

5. E. C. Douglas and A. G. F. Dingwall, "Ion Implantation for Threshold Control in COSMOS Circuits," IEEE Trans. Electron Devices ED-21, 324 (1974).

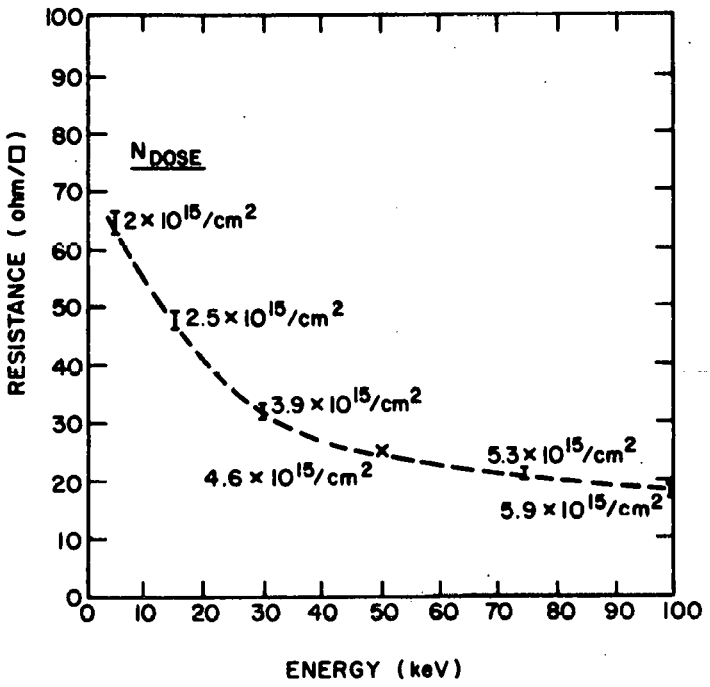


Figure 5. Results of sheet resistance measurements on ion-implanted layers of annealed at 900°C for 30 min in flowing N_2. After anneal, the peak values in the layer profile are 3 to 4 x 10^{20} atoms/cm^3.

The backside p^+ contact layer of the n^+pp^+ solar-cell structure was formed in one of two ways. Process A consists of implanting a 25-keV, ^{11}B layer on the backside of the wafer and then performing a three-step anneal which consists of heating the wafer at 550°C for 2 h in flowing N_2, then increasing the temperature to 850°C and heating for 15 min in flowing N_2, and then reducing the temperature back to 550°C and heating for another 2 h in flowing N_2. The second backside doping procedure, process B, consists of depositing a boron glass layer on the backside of the wafer using a wet boron nitride transfer process* and then performing a 900°C drive-in anneal step for 30 min in flowing N_2. This procedure produces a layer having a sheet resistance of ~50 Ω/□ and having the profile given in Fig. 6. It will be shown in a later section that both backside doping processes are capable of preserving or increasing the diffusion length in the bulk of the solar cell.

*See subsection c.(1) below.

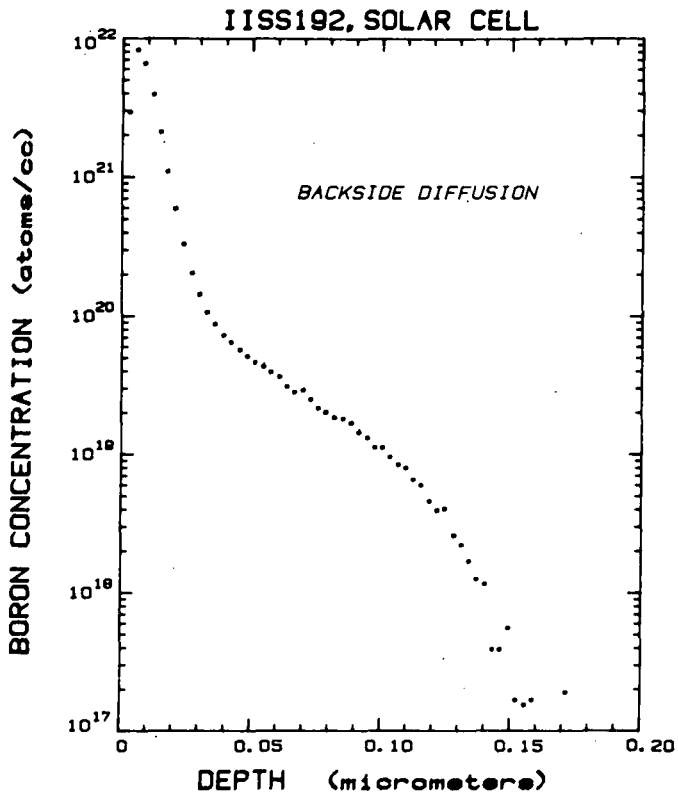


Figure 6. SIMS profile of the backside layer formed by wet boron nitride transfer process B.

c. Preserving and Improving the Diffusion Length in Ion-Implanted Silicon Solar Cells - Initial experiments in fabricating ion-implanted silicon solar cells used 950°C anneal steps and used low temperature (875°C) grown oxide or CVD oxides as capping layers. Analysis of the resulting cells showed conversion efficiencies (with spin-on AR coatings) which ranged between 8.7 and 12.6%. Measurement of the bulk lifetime in these samples, using the diode reverse recovery techniques [6] on test diodes incorporated on the same solar-cell wafer revealed that the minority carrier electron lifetime in the base

6. R. H. Kingston, "Switching Time in Junction Diodes and Junction Transistors," Proc. IRE 42, 829 (1954). Also see B. Lax and S. F. Neustadter, "Transient Response of a P-N Junction," J. Appl. Phys. 25, 1148 (1954), and R. H. Dean and C. J. Nuese, "A Refined Step-Recovery Technique for Measuring Minority Carrier Lifetimes and Related Parameters in Asymmetric P-N Junction Diodes," IEEE Trans. Electron Devices ED-18, 151 (1971).

region of these cells ranged from 0.5 to 2.1 μs, with the lowest lifetimes correlating with the poorest conversion efficiencies. This result indicated that a method was needed for improving the minority carrier lifetime in the base region of the solar cells.

(1) Boron Glass (BG) Backside Gettering - A technique for fabricating high-efficiency p^+n solar cells [7] involves the use of a p^+ layer formed using a wet boron nitride [8,9,10] transfer doping process, and this technique was used to form the backside contact layers on the n^+pp^+ ion-implanted cells. Initial tests with the boron glass (BG) backside doping process produced cells with conversion efficiencies between 12.3 and 13.9%. Cells with the BG processing displayed minority carrier lifetimes which were on average more than an order of magnitude higher (9.8 to 17.8 μs) than the earlier cells; a comparison of the quantum efficiency curves for cells made with and without the BG deposited on the backside (see Fig. 7) showed that the contributions of the deeply absorbed wavelengths were higher for the cells made using the BG backside step. This improvement in lifetime τ (or equivalently in diffusion length $L = \sqrt{D\tau}$ where D is the minority carrier diffusion length which is dependent on the wafer background doping level) indicates that the diffused boron p^+ layer accomplished gettering in much the same fashion as diffused phosphorus layers. The exact nature of the gettering process in the case of the BG layer, however, is not yet known.

A careful measurement of the diffusion lengths in selected cells made with the BG backside doping process (Table 4) showed that the diffusion lengths in the cells after BG processing (205 to 278 μm) are significantly higher than the diffusion length observed in the starting wafers. The values observed for

7. M. S. Bae and R. V. D'Aiello, "P+/N High-Efficiency Silicon Solar Cells," Appl. Phys. Lett. 31, 285 (1977).
8. D. R. Rupprecht and J. Stach, "Oxidized Boron Nitride Wafers as an In-Situ Boron Dopant for Silicon Diffusions," J. Electrochem. Soc. 120, 1266 (1973).
9. J. Stach and J. Kruest, "A Versatile Boron Diffusion Process," Solid State Technol. 19, 60 (October 1976).
10. Technical Note, "Hydrogen Injection Process Low Temperature 725°C-975°C," Form C715, June 1978, The Carborundum Co., Graphite Products Division, P.O. Box 577, Niagara Falls, New York 14302.

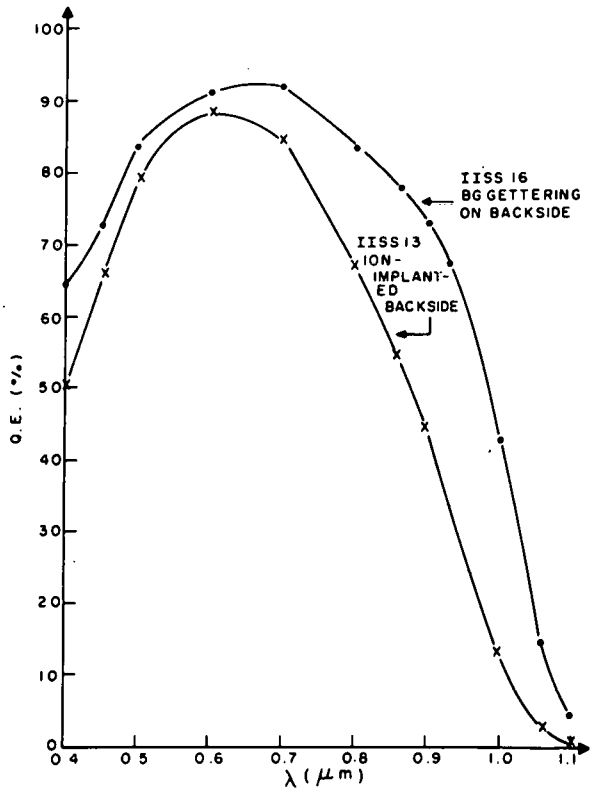


Figure 7. Quantum efficiency curves for a cell made with boron glass (BG), formed by the wet boron nitride transfer process, and ion-implanted boron as the source for the backside p^+ layer. Both cells were annealed at 900°C for 30 min in flowing N_2.

the diffusion length in Wacker* float zone starting wafers were between 100 and 160 μm.

The wet boron nitride transfer process differs from earlier processes involving boron nitride wafers in both transfer temperature and background ambient. By introducing and controlling the amount of water vapor in the gas stream, the material HBO_2 is formed and transferred to the silicon solar-cell wafer [9]. HBO_2 has a much higher vapor pressure than the B_2O_3 material which is transferred in the absence of water vapor. The transfer of HBO_2 in a wet ambient can be accomplished at 800°C, a temperature at which no boron diffusion will occur into the silicon. Thus, the transfer process only produces a boron source glass; no uncontrolled diffusion occurs. To achieve the same

*Wacker Chemical Corp., Richardson, TX.

TABLE 4. DIFFUSION LENGTH MEASUREMENTS IN ION-IMPLANTED SOLAR CELLS

Cell	^{31}P, 5-keV Dose	BG on Backside Anneal Temp. 30 min (°C)	L_P (μm) (SPV)†	L_P (μm) DRR†† (D=30)	L_P (μm) QE meas†††
IISS15 WAC1-3*	1.5×10^{15}	900	270	149	201
IISS20 WAC1-3	5×10^{14}	1000	210	212	274
IISS21 WAC1-3	7.5×10^{14}	1000	205	231	278
IISS23 MON1-3**	7.5×10^{14}	900	140	191	254
IISS26 MON1 3	1.5×10^{15}	1000	150	171	245

*1-3 Ω-cm Wacker float zone wafers, 2 in., <100>.
**1-3 Ω-cm Monsanto Co., St. Peters, MO, Czochralski wafers, 3 in., <100>.
†SPV - Diffusion length measured using the surface photovoltage method.
††DRR - Diffusion length measured using the diode reverse recovery method.
†††QE - Diffusion length measured by fitting the theoretical quantum efficiency curve to the data. L_P is a fit parameter.

vapor pressure of transfer material B_2O_3 in a dry transfer process would require a temperature of ~1200°C. The amount of H_2O in the ambient gas stream must be carefully controlled so that the glass can be removed easily at the end of the process. This is accomplished by using a ~10% H_2:N_2 forming gas mixture to which is added a controlled amount of O_2. The amount of H_2O which forms in the gas stream is thus dependent on the O_2 flow rate. (An alternate procedure is to use an N_2:O_2 ambient mixture to which is added a controlled amount of H_2.)

After depositing the boron glass layer (BG) at 800°C, the wafer is placed in a furnace at the desired drive-in anneal temperature. The p^+ layer on the backside and the ion-implanted ^{31}P layer on the front side are simultaneously annealed. Excess glass is then removed in buffered HF. After the removal step, a boron-rich layer remains on the surface as evidenced by the fact that

the backside remains hydrophilic while the front side, which was protected from boron deposition by a CVD SiO_2 layer, becomes hydrophobic. The residual boron-rich layer, however, is conductive and presents no contacting problem. If too much O_2 is used during the transfer process, an excessively thick layer of boron glass will form which results in an undesirable yellow-stained surface after the buffered HF removal step. When the wafers come out of the 800°C deposition step, they should have a pale blue color.

It has been observed that the boron nitride wafers must be periodically oxidized (it is the B_2O_3 layer on the surface that is the transfer source, not the BN) and that the furnace must be allowed to clean itself through use if the gettering effect is to be achieved. The cells after IISS83, as well as the first attempt at 3-in. solar cells (IISS45 to IISS52), do not display efficiencies as high as those before IISS83. All these cells were made with the same BG processing. Cells before IISS83 were processed in a 2-in. boron nitride transfer furnace while those after IISS83 were processed in an upgraded 3-in. BG furnace which had not achieved the required degree of cleanliness during our use of it. Subsequent tests in newly set-up BG transfer furnaces indicate that a period of furnace cleaning-by-use is required for the gettering to become effective.

(2) Three-Step Annealing - A second backside processing procedure, the three-step anneal [11] procedure which is carried out after the wafer has been implanted on both sides, was also used to produce efficient solar cells. Wafers IISS72 to 77, IISS126 to 132, IISS140 to 146 and IISS154 to 160 showed a significant improvement in bulk diffusion length after the front side n^+ implant and the backside p^+ implant had been performed, followed by the three-step anneal sequence. Again the exact reason for the increase in diffusion length is not known. The long low-temperature steps followed by the short high-temperature step nicely anneals the implanted dopant atoms; but the accompanying phenomenon which leads to longer minority carrier diffusion lengths is not

11. A. Kirkpatrick, "Process Specification for High Efficiency Implanted 3" Diameter Cells," Proceedings: 9th Project Integration Meeting, LSA Low Cost Solar Array Project, JPL, April 11-12, 1978. (See page 4-104 of Proceedings.)

obvious. We can speculate, based on the observations of Helmreich and Sirtl [12], that optimum conditions in the crystal lattice are established by the long low-temperature heating steps.

Both the three-step annealing process A and the backside boron glass (BG) procedure B are capable of preserving or increasing the diffusion length in the bulk region of the wafer. The BG process B has the advantage that it allows annealing steps in the 900 to 1000°C temperature range to be carried out (see cells IISS54 to 65) without sacrificing cell efficiency. The BG process B also requires only 65 min of process time for deposition and anneal. On the other hand, the BG process B has the disadvantage that the front side must be capped during the BG deposition. The three-step anneal procedure A has the advantage of being an all ion-implanted procedure which can be performed with no capping layer. It has the disadvantage of requiring 250 min of furnace time.

d. Solar-Cell Performance as a Function of Dose and Anneal Cycle - A series of experimental solar cells were fabricated, with different dose values for the 5-keV implanted ^{31}P atoms, to determine the optimum dose value. The results of the experiment using the boron glass backside annealing process B are shown in Figs. 8 through 11 where the annealing has been performed at both 900 and 1000°C for 30 min. Each data point in those figures and the ones to follow represents the average of four cells. It can be seen from Fig. 8 that the efficiency of both 900 and 1000°C annealed samples peaks in the dose region between $2\times10^{15}/cm^2$ and $5\times10^{15}/cm^2$. The fall-off at lower dose value is caused by a decrease of both V_{oc} and fill factor FF as the dose is lowered (see Figs. 10 and 11). Increased n^+ sheet resistance and decreased junction potential contribute to this fall-off. Notice from Fig. 9 that the AM-1 short-circuit current is relatively insensitive to the dose level. This indicates that J_{sc} is dominated by bulk effects which are relatively unaffected by the formation of the n^+ layer by implantation as long as diffusion length in the bulk is preserved or increased during the anneal cycle.

12. D. Helmreich and E. Sirtl, "Oxygen in Silicon: A Modern View," Semiconductor Silicon 1977, Proceedings of the 3rd International Symposium on Silicon Materials Science and Technology, The Electrochemical Society, Inc., P.O. Box 2071, Princeton, NJ 08540. (Article located on pages 626 to 636.)

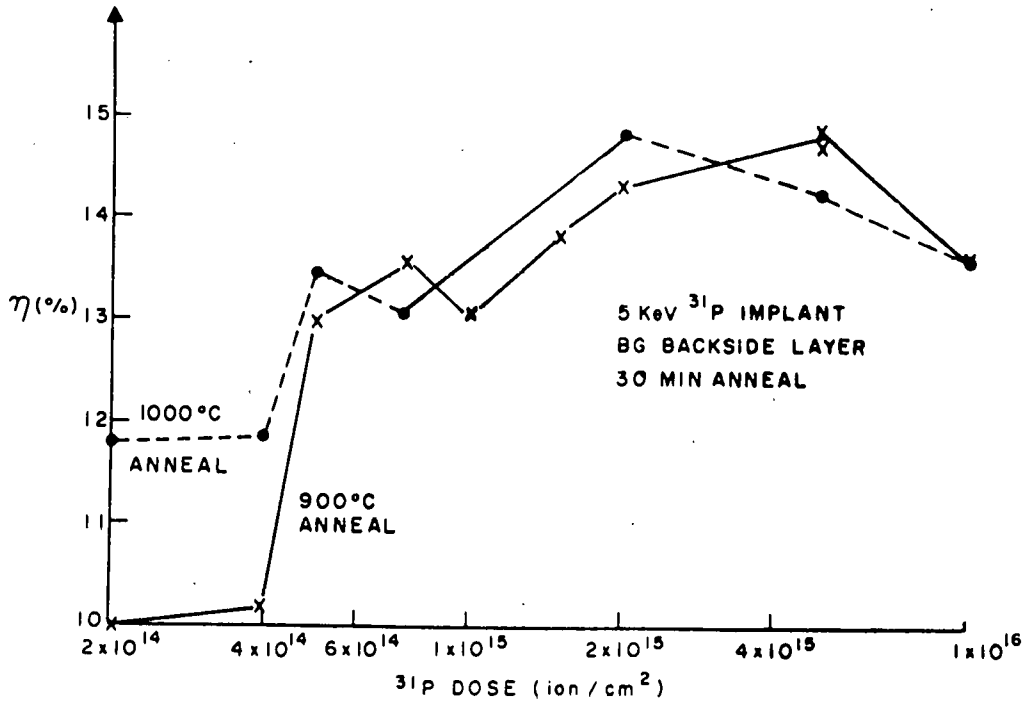


Figure 8. A plot of the conversion efficiency of solar cells made with 5-keV ^{31}P implanted at different dose levels. Boron glass process B was used during the anneal cycle which was carried out at 900 and 1000°C.

The effect of using either the three-step anneal process A or the boron glass process B on samples fabricated using different dose levels is shown in Fig. 12. The three-step anneal process and the boron glass process yield comparable results at the optimum dose levels of $2x10^{15}$ to $5x10^{15}$ atoms/cm^2. As can be seen from Fig. 13, however, the open-circuit voltage for all dose levels tested tends to increase with the anneal temperature; this is also evident in Fig. 10. It appears that at lower dose levels the three-step process suffers from insufficient annealing. It also appears that it is desirable to anneal the samples at the highest temperature that does not degrade the diffusion length in the bulk. The boron glass anneal process B has the advantage of preserving or increasing the diffusion length when anneal temperature as high as 900 to 1000°C are used.

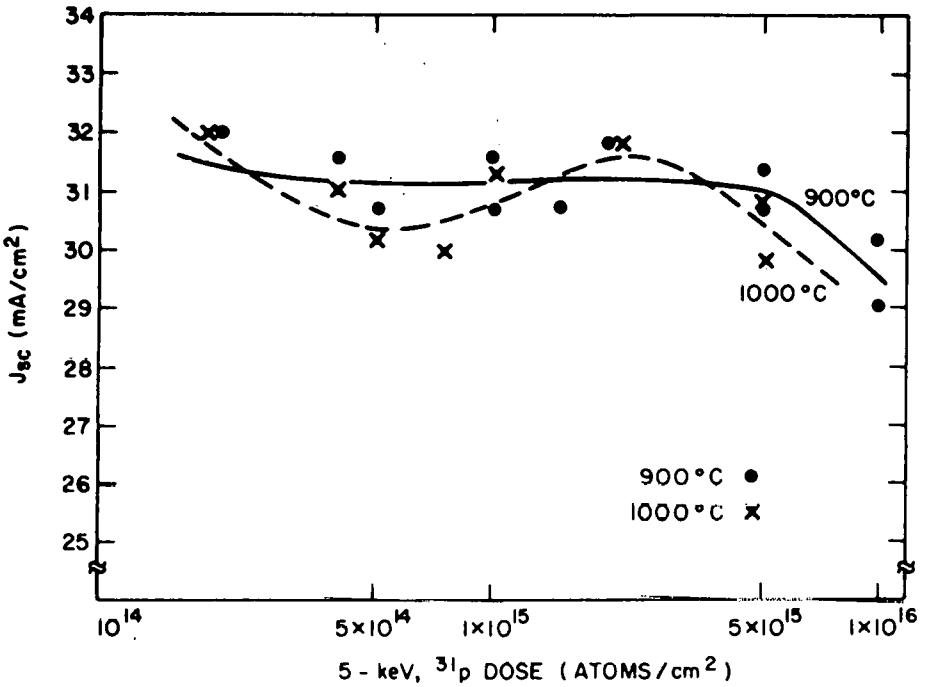


Figure 9. A plot of the short-circuit current density of solar cells made with 5-keV ^{31}P implanted at different dose levels. Boron glass process B was used during the anneal cycle which was carried out at 900 and 1000°C.

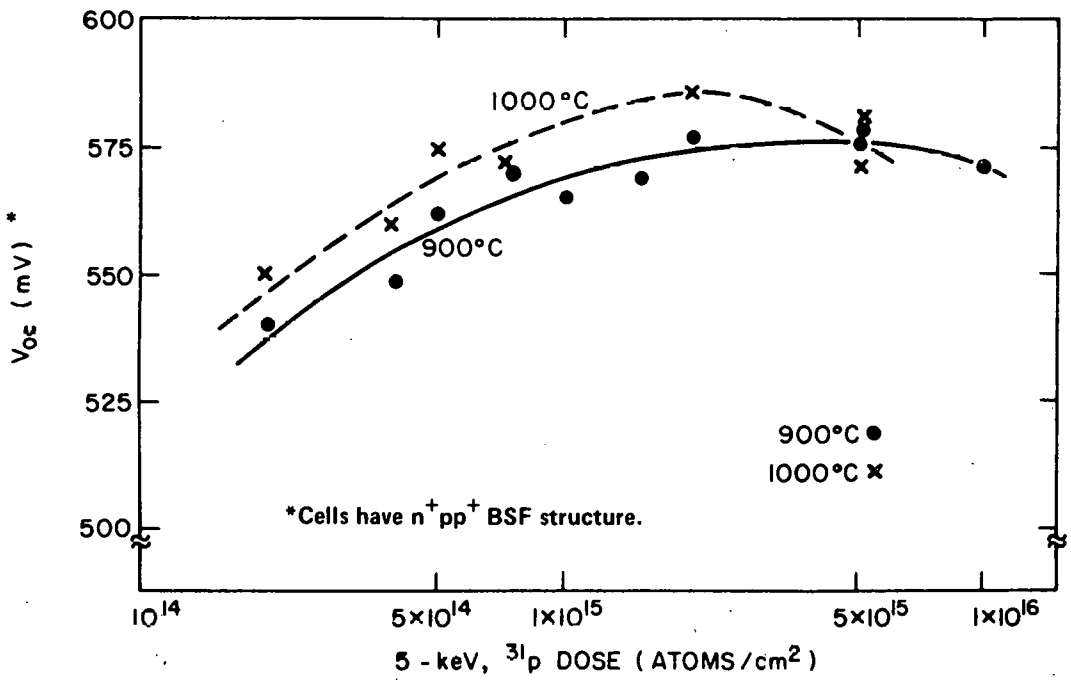


Figure 10. A plot of the open-circuit voltage of solar cells made with 5-keV ^{31}P implanted at different dose levels. Boron glass process B was used during the anneal cycle which was carried out at 900 and 1000°C.

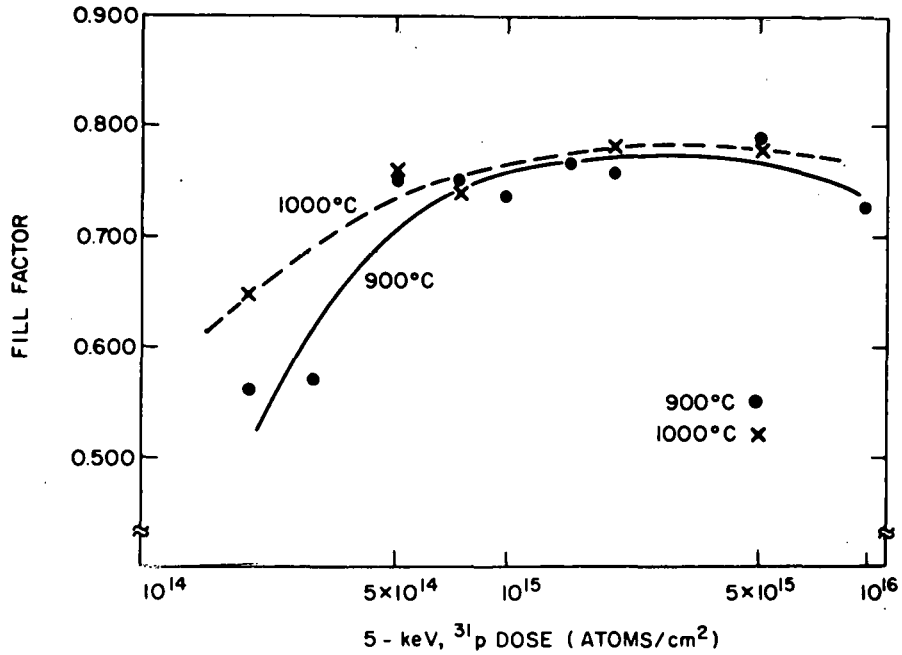


Figure 11. A plot of the fill factor of solar cells made with 5-keV ^{31}P implanted at different dose levels. Boron glass process B was used during the anneal cycle which was carried out at 900 and 1000°C.

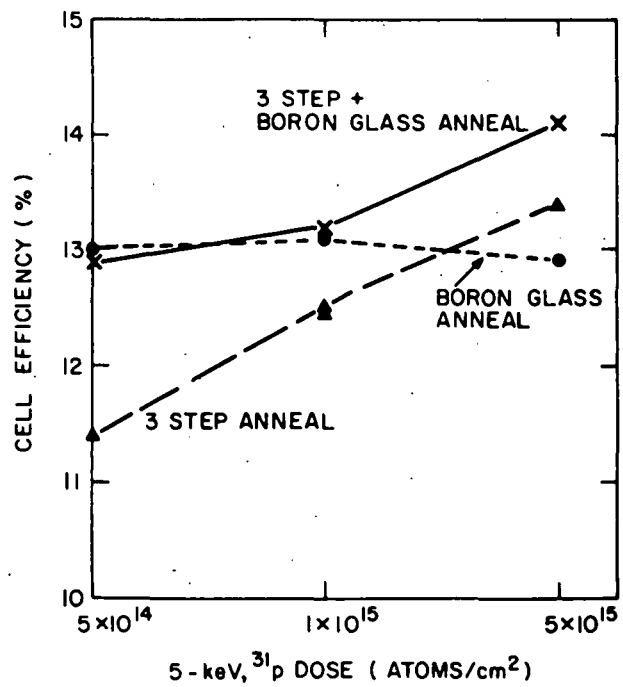


Figure 12. A plot of the conversion efficiency of solar cells made with 5-keV ^{31}P implanted at different dose levels. The anneal was performed using either the three-step anneal process A, the boron glass process B at 900°C, or a combination of the two.

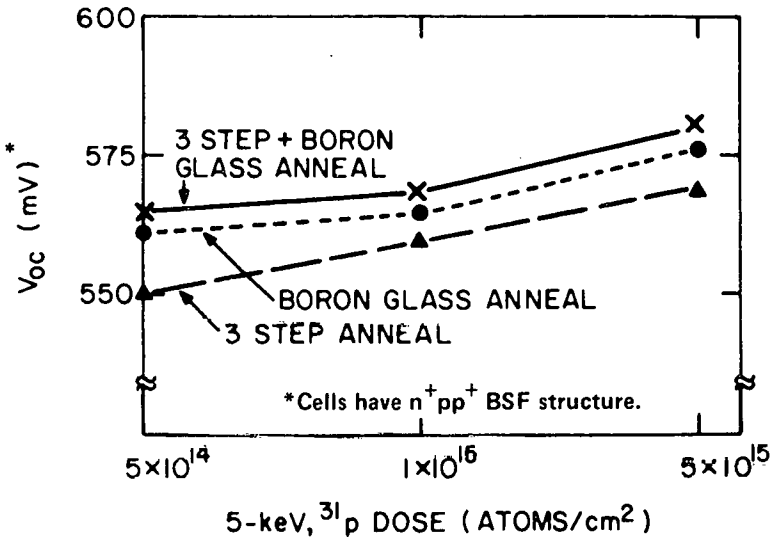


Figure 13. A plot of the open-circuit voltage of solar cells made with 5-keV ^{31}P implanted at different dose levels. The anneal is performed using either the three-step anneal process A, the boron glass process B at 900°C, or a combination of the two.

e. Solar-Cell Performance as a Function of Implanted Species - n^+p cells were fabricated using 5-keV ^{31}P, 5-keV ^{75}As, and a combination of 5-keV ^{31}P + 5-keV ^{75}As to form the n^+ layer. The cells received anneal cycles, using the boron glass process B, ranging from 900 to 1050°C. The conversion efficiencies of the resulting cells, as a function of implanted dose, are given in Figs. 14 and 15. The cells tend to peak in efficiency in the same range ($2x10^{15}$ to $5x10^{15}$/cm^2) as observed in the previous experiments. We have observed that higher temperature anneal steps are needed to produce efficient ^{75}As implanted cells. A third conclusion to be drawn is that the presence of both ^{31}P and ^{75}As in the n^+ layer of the cell does not significantly improve the conversion

13. M. Watanabe, H. Muraoka, and T. Yonezawa, "Perfect Crystal Technology," Proceedings of the 6th Conference on Solid State Devices, Tokyo, 1974, Supplement to the Journal of the Japan Society of Applied Physics, Vol. 44, 269 (1975).
14. T. Yonezewa, M. Watanabe, Y. Koshino, H. Ishida, H. Muraoka, and T. Ajina, "High Concentration Diffusion without Generation of Crystal Defects," Proceedings of the Third International Synposium on Silicon Materials Science and Technology, Philadelphia, PA 1977. Semiconductor Silicon 1977, Vol. 77-2, p. 658, The Electrochemical Society, Princeton, NJ.

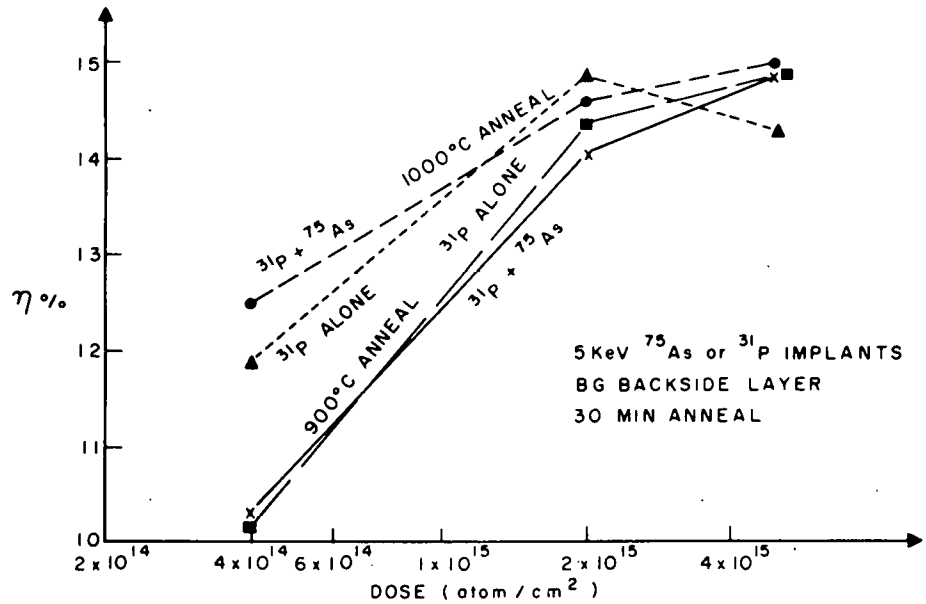


Figure 14. A plot of the conversion efficiencies of solar cells implanted with ^{13}P alone and cells implanted with both ^{31}P and ^{75}As to form the n^+ layer.

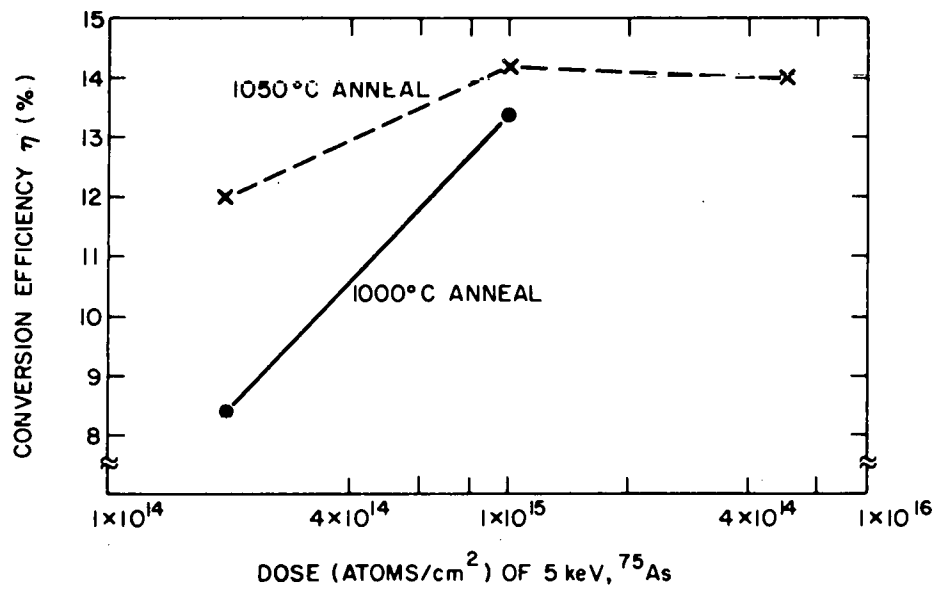


Figure 15. A plot of the conversion efficiencies of cells implanted with ^{75}As to form the n^+ layer. The backside layer of the cells was formed using the boron glass process B and the cells were annealed at 1000 or 1050°C for 30 min.

efficiency. It has been reported in the literature [13,14] that the use of both ^{31}P and ^{75}As in the emitters of bipolar transistors can reduce dislocation formation and improve the emitter characteristics. This effect does not appear to be of significance in our implanted solar cells.

p^+nn^+ cells were also fabricated using ion-implanted ^{11}B at 5 keV. The n^+ backside layer of these cells was formed by depositing CVD phosphorus-doped oxide and performing both the front side anneal and the backside diffusion at the same time. A known gettering effect [15] is achieved with this type of phosphorus treatment. Table 5 shows the performance of the p^+nn^+ cells, annealed at two different temperatures, compared with the best of the n^+pp^+ cells. Although the conversion efficiency, the short-circuit current, and the fill factors are comparable for the two types of cells, the open-circuit voltage of the p^+nn^+ structures is consistently higher than the open-circuit voltage of the n^+pp^+ cells.

f. Solar-Cells Performance as a Function of Implant Energy - Solar cells were made using different implant energies for the implantation of ^{31}P to form the n^+ layer. The profiles of the cells are given in Fig. 2 and the performance of the cells is plotted as a function of energy in Figs. 16 and 17. The boron glass process B was used during the anneal step which was carried out at 900°C for 30 min.

The fill factor and the open-circuit voltage of these cells are nearly independent of energy because the cells were designed to have the same peak concentration in the emitter. The short-circuit current of the cells, however, is a decreasing function of implant energy and this causes the conversion efficiency of the cell to drop with increasing implant energy. The reason for this loss of conversion efficiency is the drop in quantum efficiency at lower wavelengths with increasing implant energy (i.e., increasing junction depth) as shown in Fig. 18 where the quantum efficiency at four different wavelengths is plotted as a function of energy. Except for the slight initial increase in quantum efficiency for the two lower wavelengths, an effect which is probably

15. A. Goetzberger and W. Shockley, "Metal Precipitates in Silicon P-N Junctions," J. Appl. Phys. 31, 1821 (1960). See also M. N. Nakamura and T. Kato, "A Study of Gettering Effect of Metallic Impurities in Silicon," Japan J. Appl. Phys. 7, 512 (1968) and E. L. MacKenna, "Silicon and Silicon Dioxide Gettering in Perspective," Extended Abstract No. 216, Electrochem. Soc. Vol. 74-2, October 1974.

TABLE 5. A COMPARISON OF THE PERFORMANCE OF n^+pp^+ AND p^+nn^+ ION-IMPLANTED SOLAR CELLS

Cell	S	n^+pp^+	Species	Dose	Anneal Temp (°C)	η (%)	J_{sc} (mA/cm^2)	V_{oc} (mV)	FF
IISS60		n^+pp^+	^{31}P	$2.0x10^{15}$	900	14.4	31.9	577	0.760
IISS61		n^+pp^+	^{31}P	$2.0x10^{15}$	1000	14.9	31.9	587	0.780
IISS36		n^+pp^+	^{75}As	$1.0x10^{15}$	1050	14.2	31.3	578	0.760
IISS38		n^+pp^+	^{75}As	$5.0x10^{15}$	1050	14.0	30.7	580	0.760
IISS62		n^+pp^+	$^{31}P+^{75}As$**	$2.5x10^{15}$	900	14.9	31.8	583	0.780
IISS63		n^+p	$^{31}P+^{75}As$**	$2.5x10^{15}$	1000	15.0	31.1	590	0.730
IISS107		p^+nn^+	^{11}B	$2.0x10^{15}$	900	14.9	31.6	601	0.760
IISS108		p^+nn^+	^{11}B	$2.0x10^{15}$	900	14.4	31.0	600	0.751
IISS109		p^+nn^+	^{11}B	$2.0x10^{15}$	1000	14.7	31.0	600	0.766
IISS110		p^+nn^+	^{11}B	$2.0x10^{15}$	1000	14.5	31.1	600	0.755

*The n^+pp^+ cells were made with 1 to 3 ohm-cm, p-type starting substrates. The boron glass process B was used during the anneal cycle.
The p^+nn^+ cells were made with 1 to 2 ohm-cm, n-type starting substrates. The backside layer was formed using a phosphorus-doped CVD oxide as the diffusion source.
All the cells were annealed for 30 min.

**Equal amounts of each dopant.

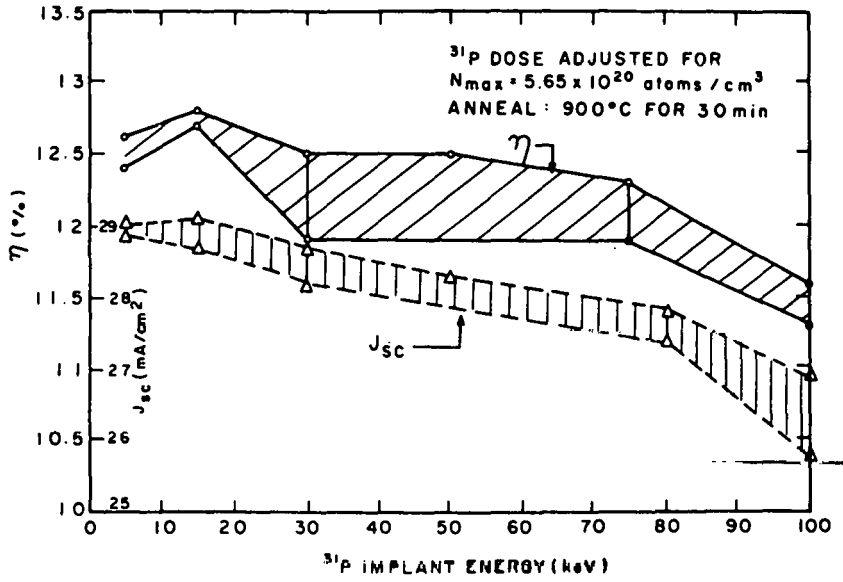


Figure 16. A plot of the conversion efficiency and the short-circuit current for ^{31}P implanted solar cells made with various implant energies. The boron glass process B was used during the 900°C - 30-min anneal cycle.

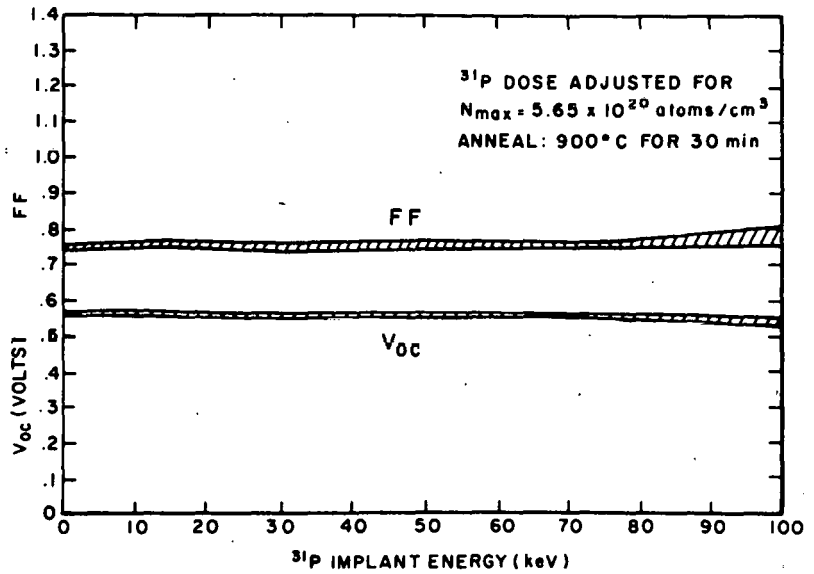


Figure 17. A plot of the open-circuit voltage and fill factor for ^{31}P implanted solar cells made with various implant energies. The boron glass process B was used during the 900°C - 30-min anneal cycle.

associated with near surface damage produced by the lowest implant energies, the quantum efficiency generally decreases with increasing energy. For longer wavelengths, the quantum efficiency tends to remain constant with increasing energy until the ratio of the layer depth to the absorption depth reaches a particular value. For deeper layer depths, the quantum efficiency begins a rapid decrease.

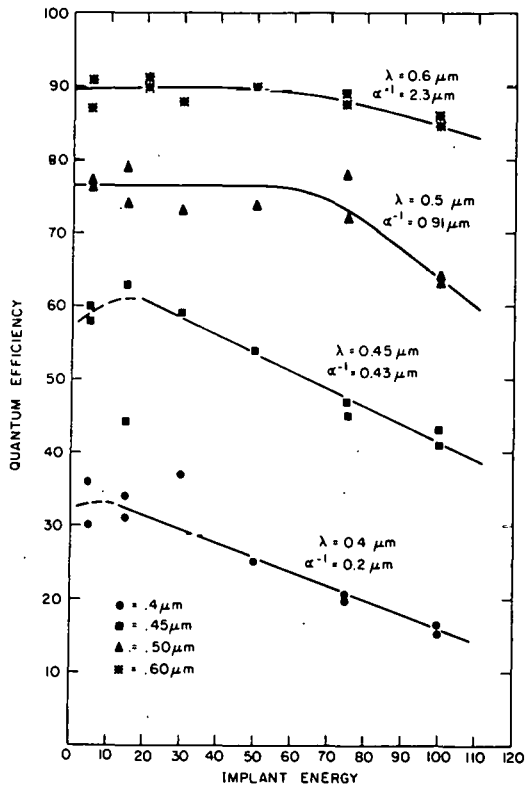


Figure 18. A plot of the quantum efficiency of the ^{31}P implanted solar cells as a function of the implant energy for various wavelengths of incident light. α^{-1} is the absorption depth in silicon for the given wavelength.

g. Solar-Cell Performance as a Function of Substrate Resistivity, Substrate Orientation, and Substrate Diffusion Length - Solar cells were fabricated using different starting wafer resistivities and different starting wafer orientations. The results of these experiments are given in Table 6. The samples were measured without AR coating, which is part of the reason for the low conversion efficiencies. Measurements were also made of the diffusion lengths in

TABLE 6. MEASUREMENTS OF SOLAR-CELL PERFORMANCE AS A FUNCTION OF OF WAFER ORIENTATION AND RESISTIVITY

Cell	Wafer Doping (ohm-cm)	Orientation	SPV Diffusion Length before Processing (μm)	SPV Diffusion Length After Processing (μm)	Diffusion Length for Parameter Fit to QE Data After Processing (μm)	η (%)	J_{sc} (mA/cm^2)	V_{oc} (mV)	FF
IISS97	WAC* 1-4	<100>	110	110	89	8.8	20.2	552	.786
IISS98	WAC* 1-4	<100>	110	100	100	8.9	20.5	553	.785
IISS99	WAC 1-4	<100>	100	70	109	8.9	20.5	556	.781
IISS100	WAC† 8-12	<100>	130,90	110	115	8.4	20.9	520	.774
IISS102	WAC† 8-12	<100>	100	350	106	8.3	20.9	516	.771
IISS103	WAC[1] 8-12	<111>	100,90	130	107	8.3	20.8	514	.774
IISS104	WAC[1] 8-12	<111>	110,100	210	150	8.3	20.6	524	.773
IISS119	MON* 8-15	<100>	120	-	23	7.8	20.0	510	.769
IISS120	MON* 8-15	<100>	105	-	83	8.2	20.7	518	.768
IISS133	MT† 1.5	<100>	110	-	80	8.6	20.1	550	.777
IISS134	MT† 1.5	<130>	130	-	71	8.5	20.0	546	.777

WAC* - Wacker Floatzone Wafers, 1-4 ohm-cm, <100>, p-type, 10-12 mil thick, 2-in. diam

WAC† - Wacker Floatzone Wafers, 8-12 ohm-cm, <100>, p-type, 10-12 mil thick, 2-in. diam

WAC[1] - Wacker Floatzone Wafers, 8-12 ohm-cm, <111>, p-type, 10-12 mil thick, 2-in. diam

MON* - Monsanto Co. (St. Peters, MO) Czochralski Wafers, 8-15 ohm-cm, <100>, p-type, 14-16 mil thick 3-in. diam, cut down to 2-in. diam

MT† - RCA Mountaintop Czochralski Wafer, 1.5 ohm-cm, <100>, p-type, 13-15 mil thick, 2-in. diam

the wafers before and after processing of the cells. Surface photovoltage (SPV) measurements of the diffusion length after processing were made on a region near the solar cell which was not covered by an n^+ junction. The reason for the low values of diffusion length observed in the finished cells, and, hence, a second reason for the low conversion efficiencies, is, as mentioned in subsection A.2.c above, that the furnace used during the boron glass processing of the wafers was not clean enough for the gettering layer to be effective in increasing the diffusion length in the samples over their starting value. In spite of the low conversion efficiencies achieved with these cells, it can be concluded from these experiments that (1) the final conversion efficiency of the solar cell depends more on the diffusion length existing in the cell after processing than it does on the starting wafer resistivity or orientation. The tests also indicate that (2) if cells of high conversion efficiency are to be fabricated, then the diffusion length found in the starting wafers, which in the cells considered here ranges from 100 to 130 μm, must be increased by a factor or two or more. This point is graphically illustrated in Fig. 19 where cell conversion efficiency is plotted as a function of diffusion length measured in the finished cell. When the diffusion length is less than the thickness of the cell, the efficiency is an increasing function of the diffusion length in the final cell, and if the diffusion lengths are not increased over their value of ~100 μm in the starting wafer, then low values of cell efficiency will be obtained. When the value of the diffusion length in the final cell equals or exceeds the thickness of the wafer, the cell efficiency tends to saturate at a value determined by the achievable values of open-circuit voltage and fill factor. This saturation effect occurs because of the narrow base effect, i.e., $L \ll W$ (the thickness of the cell). Under these conditions, for an ohmic contact, L_p in Eq. (4) can be replaced by W [16]. It should be noted here that when the diffusion length in the wafer approaches or exceeds the thickness of the wafer, the accuracy of both the SPV method and the parameter fit method becomes degraded and the experimental value measured becomes a lower bound on the actual value. For very long values of diffusion length, the effect of the back surface becomes significant and this effect is not adequately treated by the SPV method, although this parameter is included in the parameter fit to

16. J. Lindmayer, "Development of 20% Efficient Solar Cells," Final Project Report NSF/RANN/SE/GI-43090/FR/75/2, NSF Grant GI-43090, October 1975.

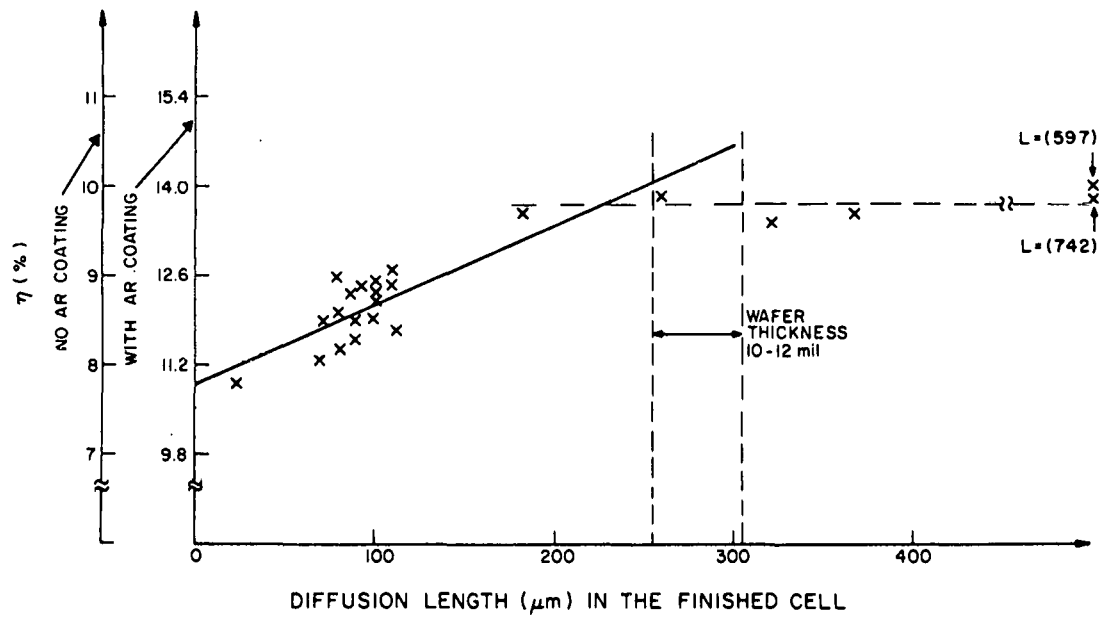


Figure 19. A plot of the efficiency of the ion-implanted solar cells as a function of the diffusion length measured in the finished cell. For the most efficient cells, the diffusion length equals or exceeds the wafer thickness.

the quantum efficiency data. The best fit value for the backside surface recombination velocity is ~150 cm/s.

h. Analysis of I-V Measurements Made on Ion-Implanted Silicon Solar Cells Under Conditions of Illumination or Total Darkness - The results of the experiments discussed so far indicate that the most important factor controlling the efficiency of the cell is the diffusion length in the base region of the cell. One method of investigating this further is to measure the J_{o1} values of the cell [see Eq. (4)]. This can be accomplished by measuring either the dark or the illuminated I-V curves and then, on a semilog plot, extrapolating the tangent to the n=1 portion of the curve to zero voltage. Figures 20 and 21 show examples of this measurement performed in the dark on small test diodes positioned on the wafer along with the active solar cells. Because the test diodes are of different areas, the J_{o1} values of the various units should scale with the diode area, but the J_{o1} values for each diode should be the same. In the example given in Fig. 20, the measured values fall in the range $J_{o1} = 4.4 \times 10^{-12} \pm 0.7 \times 10^{-12}$ A/cm^2. In actuality the data were analyzed by performing a curve fit of the measured data to Eq. (3) using as parameters J_{o1},

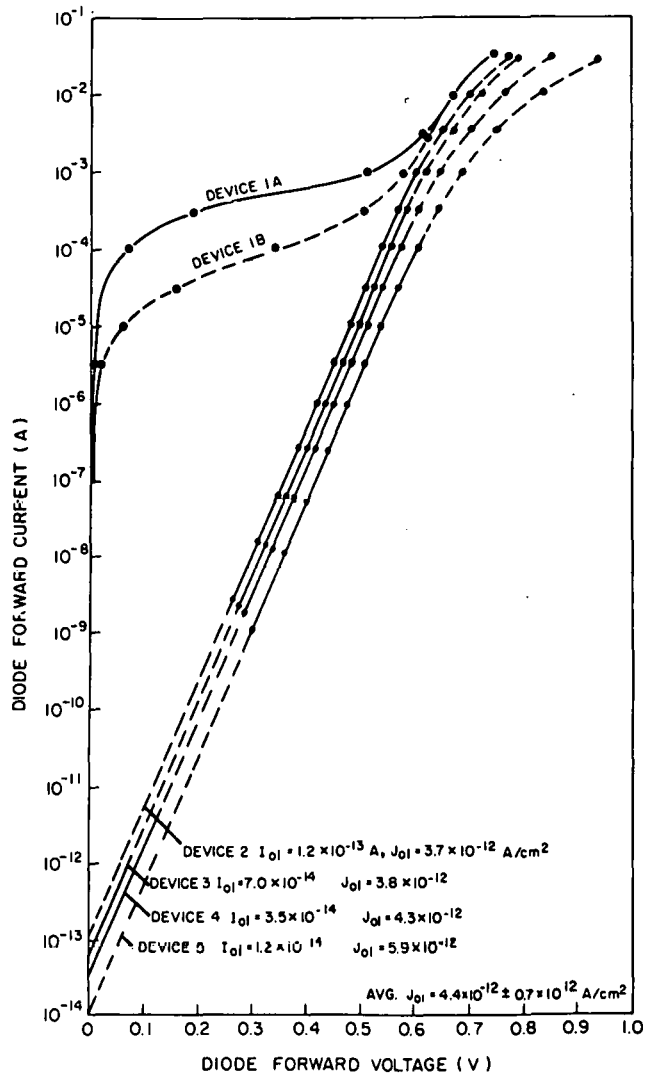


Figure 20. A plot of the dark I-V characteristics for six test diodes fabricated on solar-cell wafer IISS17. The n^+ layer was formed with a 5-keV ^{31}P implant and a dose of 5 x $10^{14}/cm^2$.

J_{o2}, and n. It is interesting to note that the J_{o2} values for the test diodes 2 to 5 on wafer IISS17 are too small to measure. The test diodes 1A and 1B on wafer IISS17, however, display a behavior that cannot be described by Eq. (3) because in this equation it is required that $1 \leq n \leq 2$. The behavior of these anomalous diodes is characteristic of shunt leakage within the diode most likely caused by wafer defects which fall in the region occupied by the

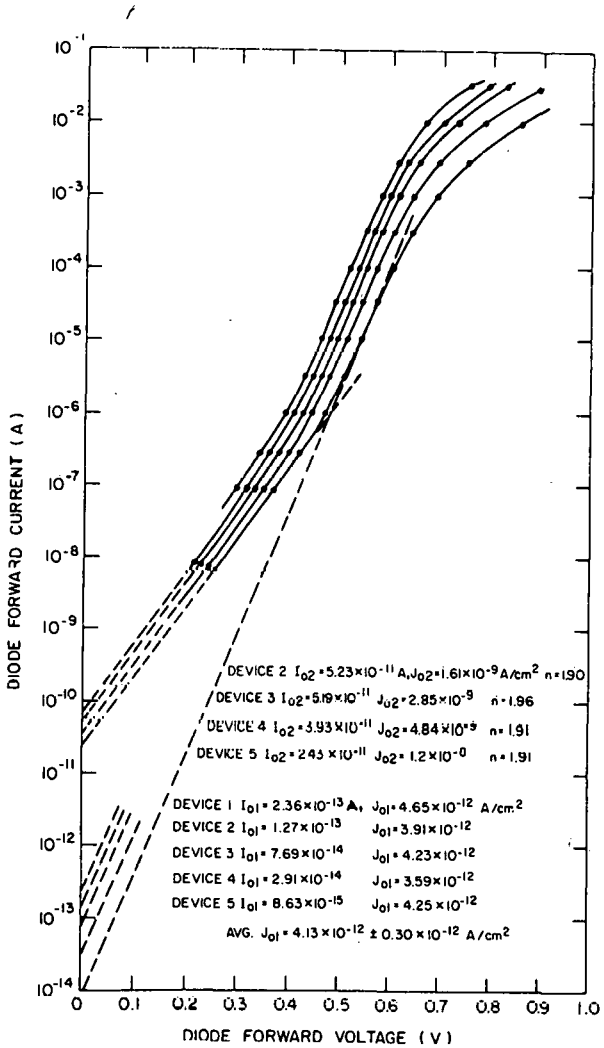


Figure 21. A plot of the dark I-V characteristics for five test diodes fabricated on solar-cell wafer IISS56. The n^+ layer was formed with a 5-keV ^{31}P implant and a dose of $4 \times 10^{14}/cm^2$.

diode or perhaps caused by alloy spiking of the metallization layer through the thin n^+ layer forming the diode.

Figure 21 shows dark I-V measurements made on test diodes on wafer IISS56. In this second case, no excess shunt leakage is observed; however, the defect recombination in the junction region is large enough to produce measurable values of J_{o2}. The values of J_{o2} in this case are respectably small and indicate that the implanted dose does not introduce damage which causes problems, at 1 sun operating levels, by becoming nucleated and driven-in during subsequent annealing steps. Table 7 lists the values of J_{o1}, J_{o2}, and n for cells

TABLE 7. VALUES OF J_{o1}, J_{o2}, AND n OBTAINED BY LEAST-SQUARES CURVE FITTING THE MEASURED DATA TO EQ. (3)

Cell	Dose (atoms/cm^2)	J_{o1} (A/cm^2)	J_{o2} (A/cm^2)	n
IISS27	2×10^{14}	$(3.00\pm0.34)\times10^{-12}$	$(1.15\pm0.48)\times10^{-8}$	1.82
IISS56	4×10^{14}	$(4.13\pm0.30)\times10^{-12}$	$(2.52\pm1.2)\times10^{-9}$	1.90
IISS17	5×10^{14}	$(4.40\pm0.70)\times10^{-12}$	-	-
IISS18	7.5×10^{14}	$(8.1\pm2.0)\times10^{-12}$	-	-
IISS60	2.0×10^{15}	$(9.3\pm1.5)\times10^{-12}$	$(5.7\pm2.1)\times10^{-10}$	1.40
IISS69	1×10^{16}	$(2.3\pm1.5)\times10^{-12}$	$(3.17\pm0.08)\times10^{-8}$	1.55

made with different implantation doses. For all dose levels considered, the values of J_{o1} are small.

To ensure that the test diodes are yielding a value of J_{o1} which also applies to the operation of the solar cell, illuminated I-V curves were also measured. If we restrict ourselves to a region of the I-V curve where n=1, then the current produced in a load across the cell is

$$J = J_o - J_{o1}(e^{qV/kT} - 1) \tag{5}$$

When the cell is open circuited, $V = V_{oc}$ and $J = 0$, hence $J_o = J_o\left(e^{qV_{oc}/kT} - 1\right)$. When the cell is short circuited, $V = 0$ and $J_{sc} = J_o$. Hence, we can write

$$J_{sc} = J_{o1}\left(e^{qV_{oc}/kT} - 1\right) \cong J_{o1}\, e^{qV_{oc}/kT} \quad \text{for } V_{oc} >> qV/kT \tag{6}$$

A plot of the $\ln(J_{sc})$ vs V_{oc} for various levels of illumination should thus extrapolate to J_{o1}. This is a useful method for measuring J_{o1} in large cells with finger metallization because it avoids problems involved with the non-uniformity of current injection under dark conditions [17]. The plots in Fig. 22 shows illuminated I-V curves for two different solar cells and show dark I-V curves for two different test diodes, all located on wafer IISS135.

17. J. Lindmayer, "Theoretical and Practical Fill Factors in Solar Cells," Comsat Tech. Rev., Vol. 2, No. 1, pp. 105-121, Spring 1972.

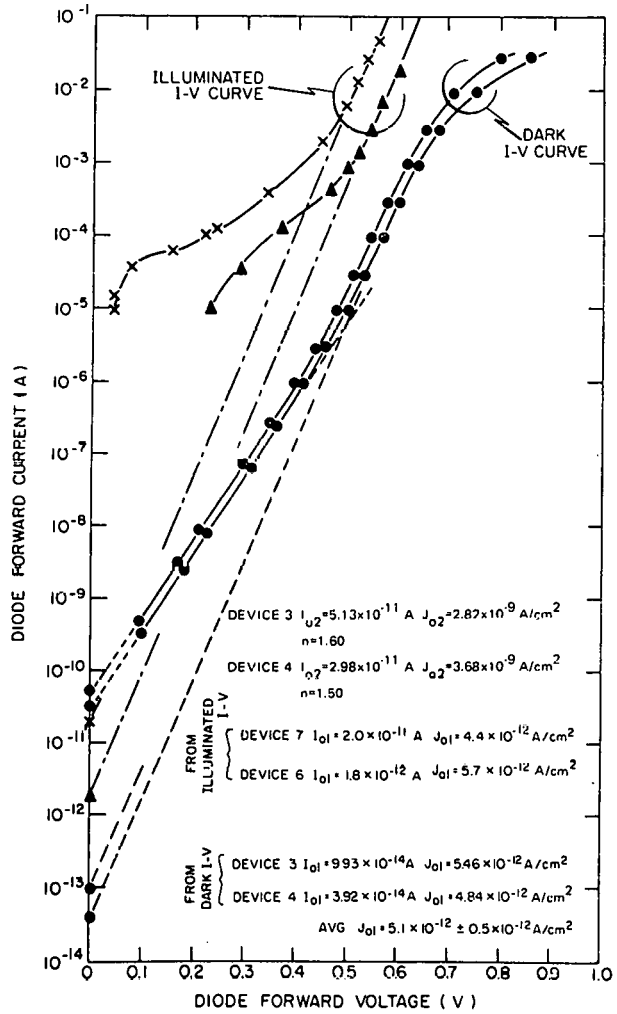


Figure 22. A plot showing both the dark and the illuminated I-V curves measured on two sizes of solar cells (0.316 cm^2 for device 6 and 4.5 cm^2 for device 7). The dark I-V curves were made on small test diodes included on wafer IISS135 along with the solar cells.

The J_{o1} values derived for the four cells are all in the range $J_{o1} = 5.1\text{x}10^{-12} \pm 0.5\text{x}10^{-12}$ A/cm^2 which is comparable to the spread observed among dark I-V measured values (see Table 6).

A plot of the J_{o1} values of a number of test wafers plotted as a function of the implant dose used to make the n^+ layer is given in Fig. 23. The horizontal dotted lines show the limits of the values of J_{o1} in 1- to 2-ohm-cm

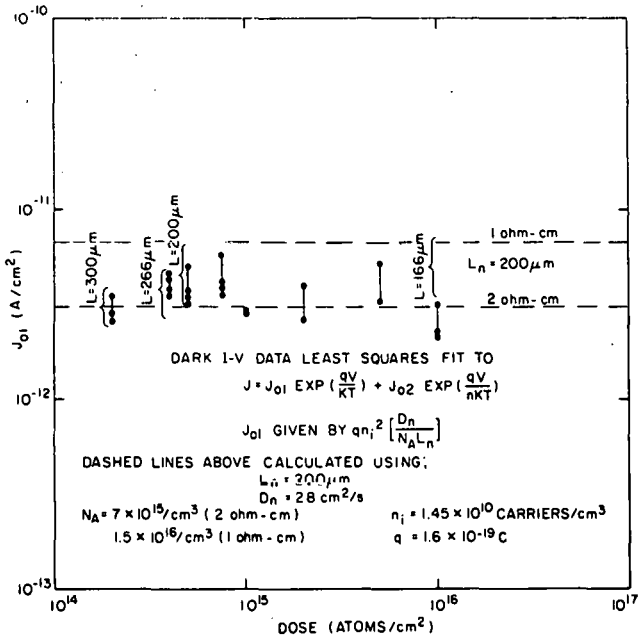


Figure 23. A plot of the values of J_{01} measured on various solar-cell wafers as a function of dose. The cells were fabricated on 1- to 2-ohm-cm wafers and the horizontal dotted lines mark the limits to be expected for a 200-μm diffusion length in the bulk. The curly brackets around the data points show the limits based on measured diffusion length in the cell.

substrates having a post-processing diffusion length of 200 μm and assuming that all contributions from the emitter [Eq. (4)] are negligible. On a few of the cells, the actual post-processing diffusion length in the bulk region was measured, and in these cases the limits of the theoretical values of J_{01} for 1- to 2-ohm-cm substrates, again assuming the contributions from the emitter term are negligible, are indicated in Fig. 23 with curly brackets. Figure 24 shows a plot of the values of J_{01} as a function of the diffusion length measured in the bulk region of the final cell. These data, measured on cells with 1- to 2-ohm-cm and 8- to 12-ohm-cm starting substrates, indicate that the J_{01} values of the cells closely track the value of the diffusion length which is obtained in the bulk. Note that the value of L obtained for cell 127 has been plotted at both the measured value (597 μm) and at the value

corresponding to the wafer thickness (381 μm). The value yielded by the curve fit to the QE data is unreasonably large.

The values plotted in Fig. 24 also indicate that the contribution to the J_{o1} value caused by the emitter term [Eq. (4)] can at most be a small fraction of the contribution from the base term. The calculated contribution from the base term is given by the solid curves. If the emitter term equalled the base term, we would expect the experimental points to fall nearly on or above the solid line in Fig. 24 corresponding to 2 or 12 ohm-cm. The data points fall in the middle or in the lower portion of the range, indicating that emitter effects have not become significant in these two resistivity ranges. This is consistent with Lindmayer's [17] observations that saturation effects due to the emitter term should not become important until substrate resistivity values fall below 1 ohm-cm.

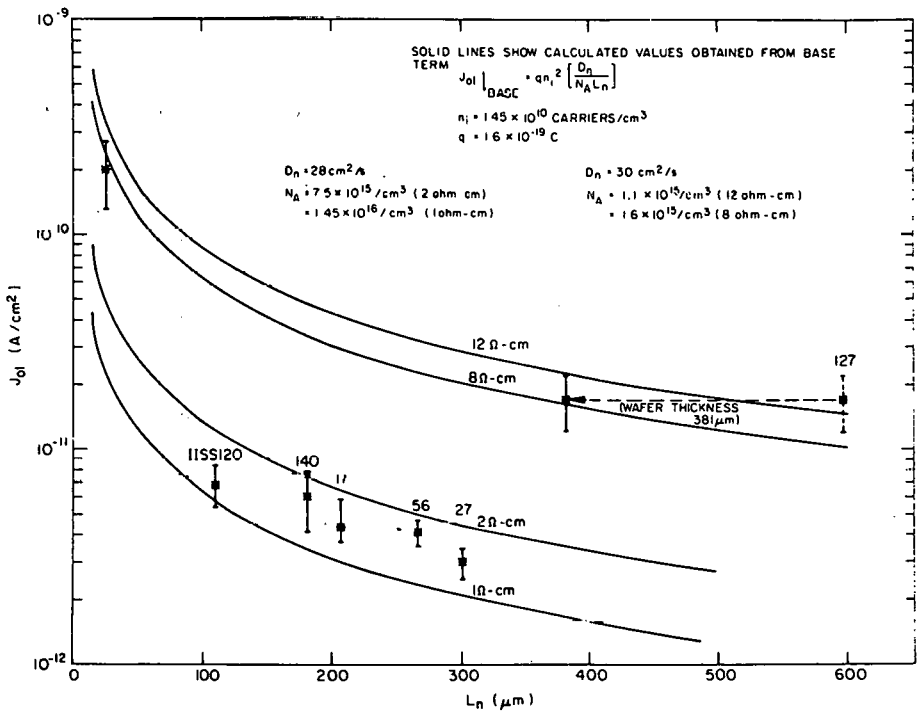


Figure 24. A plot of the values of J_{o1} measured on various solar-cell wafers as a function of diffusion length measured in the final cell.

It can be seen from Eq. (6) that a relation exists between J_{sc}, J_{o1}, and V_{oc}. It would be interesting to compute V_{oc} from the measured value of J_{sc} and J_{o1} and see how well it compares with the measured value of V_{oc}. Table 8 shows the results of the comparison for six cells made on two different wafer resistivities. The measured value of V_{oc} is generally lower than the computed value by an amount ranging from 0 to 11%. This effect could be caused by insufficiently alloyed metal contacts which allow the formation of a parasitic Schottky diode.

i. Quantum Efficiency Measurements on Ion-Implanted Solar Cells - Quantum efficiency measurements were carried out on selected solar cells and the diffusion lengths in the final cells were deduced by curve fitting the equations for the cell response (see Hovel [3]) to the measured data. The diffusion-only model was used and the junction depth was assumed to be 0.4 μm. Collection effects associated with the depletion width were neglected. Figure 25 shows plots of the data reduction. The measured data was first corrected for surface reflectance to obtain the internal quantum efficiency curve. The four parameters L_p (base), L_n (emitter), S_p/D_p (back surface), and S_n/D_n (front surface), where S is the surface recombination velocity, were then varied to obtain best fit calculated values to the internal quantum efficiency curve.

j. Discussion and Conclusions - The solar cells made during the course of this experimental study were fabricated using high-quality semiconductor grade silicon wafers and using optimum masking, capping, and metallization techniques. The object was to minimize as much as possible the potential conflicting factors which might interfere with the study of implantation effects that might adversely affect the performance of implanted solar cells.

It became apparent early in the study that the processing steps eliminated by implantation, i.e., diffusion steps involving phosphorus and boron, act as getters in conventional processing and by their absence cause a degradation in all-ion-implanted cells. This degradation can be associated with a degradation of the minority carrier diffusion length in the bulk region of the solar cell. When these gettering steps are reintroduced, usually to form the back-side contact layers, then the diffusion length in the cells can be maintained or increased above the value in the starting wafer and efficient cells can be made with ion-implanted front-side active layers. Alternate processing procedures, involving the use of long low-temperature (~500°C) anneal steps, have

TABLE 8. A COMPARISON OF THE VALUES OF MEASURED V_{oc} AND THE VALUES OF V_{oc} CALCULATED FROM THE MEASURED VALUES OF J_{ol} and J_{sc}

Sample	Substrate Resistivity (ohm-cm)	Diffusion Length (μm)	J_{ol} (meas) A/cm^2	J_{sc} (meas) (A/cm^2)	V_{oc} (meas) (volts)	$V_{oc} = \frac{kT}{q} \ln \frac{J_{sc}}{J_{ol}}$ T = 28°C	% Diff.
IISS119	8-12	23	$(2.0\pm0.7)\times10^{-10}$	20.0	0.510	0.524±1.7%	2.7
IISS127	8-12	(597)?	$(1.7\pm0.5)\times10^{-11}$	23.3	0.560	0.547±1.3%	2.3
IISS140	I-2	181	$(6.0\pm1.9)\times10^{-12}$	21.5	0.572	0.572±1.6%	0.0
IISS135	1-2	~80	$(5.1\pm09)\times10^{-12}$	19.5	0.556	0.573±.9%	3.1
IISS117	1-2	206	$(4.4\pm1.0)\times10^{-12}$	29.3	0.562	0.589±1.0%	4.8
IISS56	1-2	266	$(4.1\pm0.6)\times10^{-12}$	31.6	0.548	0.591±0.6%	7.8
IISS27	1-2	301	$(3.0\pm0.5)\times10^{-12}$	32.0	0.540	0.6600±0.6%	11.1
IISS18	1-2	-	$(8.1\pm2.0)\times10^{-12}$	30.7	0.570	0.569±1.1%	0.2
IISS60	1-2	-	$(9.3\pm1.5)\times10^{-12}$	31.9	0.577	0.566±0.7%	1.9
IISS69	1-2	-	$(2.3\pm3.8)\times10^{-12}$	30.2	0.572	0.601±0.5%	5.0

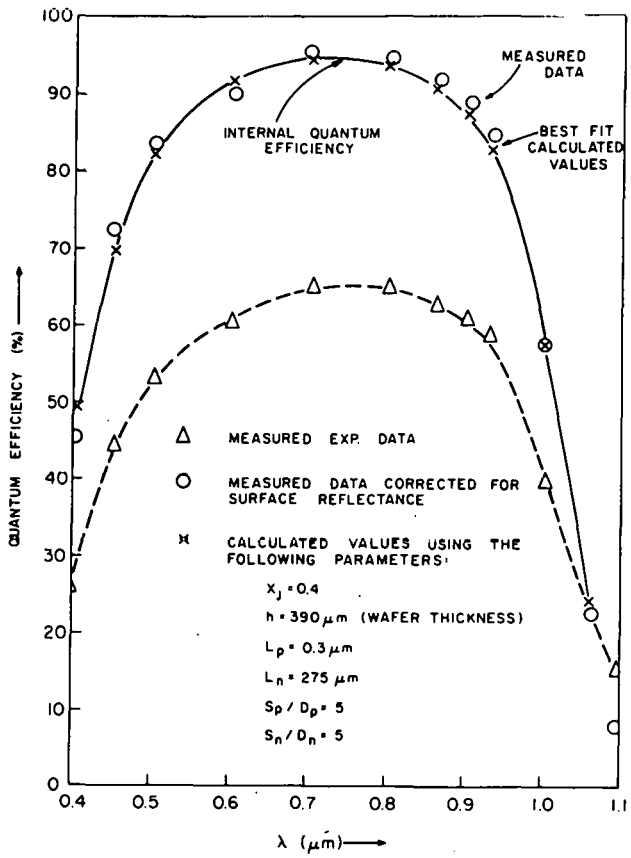


Figure 25. Plots of data reduction.

also proved effective in maintaining or increasing the diffusion length in all-ion-implanted cells.

A careful examination of the I-V curves and the J_{01} values of ion-implanted cells has indicated that for optimized implantation into substrates in the 1- to 2-ohm-cm and 8- to 12-ohm-cm resistivity ranges, the performance of the cell is dominated by the diffusion length in the bulk of the cells. Recombination effects associated with the highly doped, ion-implanted front side barrier layer are small compared to the base recombination effects. We conclude that for the procedures used here, damage in the junction region introduced by the implantation was effectively annealed or reduced to a level such that its effect is negligible in these cell structures.

Two processes have been demonstrated for annealing the ion-implanted layers while at the same time preserving or improving the diffusion length in the base

region of the cell. One of these processes, the boron glass process B, provides effective gettering at temperatures as high as 1050°C, so that anneal temperatures in the range between 900 and 1050°C can be used for efficient cell fabrication.

Experiments designed to optimize the implant procedures and the starting wafer characteristics indicate that 5- to 10-keV implant energies should be used and that doses in the range between $2x10^{15}/cm^2$ and $4x10^{15}/cm^2$ should be selected. ^{11}B into n-type wafers or ^{31}P into p-type wafers are both capable of producing cells with 15% conversion efficiency. The p^+n cells tend to have slightly higher open-circuit voltages. The characteristics of the wafer, i.e., <111> or <100>, float zone or Czochralski, n-type or p-type, are less important than the diffusion length which can be obtained in the wafer after processing. Wafer characteristics are only important, then, to the extent that they impact the observed diffusion length.

As a final observation, the technique of analyzing the initial and final diffusion length in the cells and combining these values with the J_{o1} and J_{o2} values obtained from either dark or illuminated I-V analysis has provided a data reduction procedure which has provided valuable insight into the operation of solar cells. The information obtained from cell performance tests indicates that a cell is good or bad; the diffusion length information and J_{o1}, J_{o2} information indicate why the performance is good or bad. This type of information also provides controls on the processing procedures because it can provide a continuing quantitative check on the performance of the annealing and gettering steps. Diffusion length analysis can monitor furnace problems and I-V analysis can isolate problems with shunt leakage, alloy spiking, or parasitic barriers.

The results described above show that high-efficiency solar cells can be fabricated when the proper range of ion-implantation parameters are chosen and used along with one of the prescribed furnace annealing cycles. These results show technical feasibility but not cost effectiveness since low-cost cell process steps were not used. That question was addressed in our later work and is fully described in Section V and VII.

3. Spin-On Liquid Dopant Sources

Experimental studies were conducted on both n(P,As) and p(B)-type spin-on sources. Previously we used only alcohol-based spin-on sources to fabricate

solar cells. However, wide variations in sheet resistance within lots were observed, and, moreover, alcohol-based sources have a limited and somewhat variable shelf-life. Aqueous sources have become available recently, and are thought to have better reproducibility and longer shelf-life than the alcohol-based sources.

We tested both sources for the individual and simultaneous formation of both the BSF junction and the BSF back contact. In each case, evaluations and comparisons were made of required wafer cleaning and preparation, liquid source application techniques (i.e., spin-on vs roll-on or screening), diffusion schedule and uniformity and reproducibility of resultant sheet resistance and junction depth.

We completed a test comparing alcohol- and aqueous-based phosphorus liquid dopant sources.* Solar cells of 4.4 cm^2 area were fabricated on several different starting wafers. The liquids were spun-on, and a basic junction anneal was done at 850°C for 50 min followed by two different anneal schedules for each dopant base. The results of this test are shown in Table 9.

TABLE 9. RESULTS OF A COMPARISON OF ALCOHOL- AND AQUEOUS-BASED PHOSPHORUS DOPANTS

Sample	Wafer ρ (Ω-cm)	P Dopant Base	Junction	Anneal	AM-1 Parameters J_{sc} (mA/cm^2)	V_{oc} (mV)	FF -	η (%)
3A	1-2	Alcohol	850°C 50 min	600°C 120 min	29.6	490	0.40	5.8
5B-20	1-2	Aqueous	850°C 50 min	600°C 120 min	30.8	575	0.76	13.4
2A-20	1-2	Alcohol	850°C 50 min	10 min Slow pull	29.0	500	0.55	8.0
5B	1-2	Aqueous	850°C 50 min	10 min Slow pull	30.7	580	0.77	13.7
9A	8-15	Alcohol	850°C 50 min	600°C 120 min	31.0	540	0.42	7.0
12B	8-15	Aqueous	850°C 50 min	600°C 120 min	26.7	557	0.77	11.4
16B	5	Aqueous	850°C 50 min	600°C 120 min	31.6	570	0.79	14.2

*Purchased from Emulsitone Company, Whippany, NJ.

The results clearly show that under the anneal conditions used in this test, superior junction characteristics and solar-cell performance were obtained with the aqueous-based phosphorus source when compared with the alcohol-based liquid.

In addition, in separate tests it was shown that the aqueous-based liquids can be rolled or screened onto the wafers with satisfactory coverage and resultant junction quality.

We also began a similar study of arsenic sources. Alcohol-based arsenic was used in these initial tests. Since arsenic diffuses considerably slower than phosphorus, the diffusions were done at 1000°C for 60 min as compared with 850°C for 50 min for phosphorus. Typical results for solar cells fabricated using the spin-on arsenic source are given in Table 10.

TABLE 10. CHARACTERISTICS OF SOLAR CELLS MADE WITH SPIN-ON, ALCOHOL-BASED ARSENIC SOURCE

Sample No.	Wafer ρ (Ω-cm)	Junction Formation		Spin-on Boron on Back		AM-1 Parameters			
		Diffusion	Anneal	Yes	No	J_{sc} (mA/cm^2)	V_{oc} (mV)	FF -	η (%)
51	1-3	1000°C 60 min	Slow cool to 800°C		✓	17.3	437	0.46	3.5
53	1-3	1000°C 60 min	10 min Slow pull		✓	24.6	516	0.57	7.3
55	1-3	1000°C 60 min	Slow cool to 800°C	✓		23.3	517	0.75	9.0
57	1-3	1000°C 60 min	10 min Slow pull	✓		24.7	470	0.63	7.3

Generally, poor junctions were formed, resulting in low values of open-circuit voltage and fill factor. Also, no correlation was noted with annealing conditions or back-surface boron application. The listed short-circuit currents are considerably lower than those obtained with the use of liquid phosphorus sources. A comparison of the spectral responses for two cells made with arsenic and phosphorus sources shows that the red response is much lower for the arsenic source, indicating that low diffusion length was obtained. From these test, it is not clear whether this is due to the use of the alcohol-based arsenic or to the higher processing temperature.

B. SCREEN-PRINTED THICK-FILM METALLIZATION

1. Introduction

In addition to the critical physical and electrical properties of the screen-printed metallization, the reliability of the screen-printing process as applied to solar cells was addressed initially. Therefore, this analysis will be described prior to the evaluation of metallization properties per se. The section concludes with a discussion of interface reactions and recommendations for future developmental effort.

2. Screen-Printing Parameters

To check the possibility of silicon wafer cracking during or following screen-printing, a worst-case printing test was devised. It is known that screen-printing variables, e.g., squeegee speed, snap-off distance (screen-to-substrate distance), and squeegee compression can affect the uniformity of ink deposited. For example, Fig. 26 illustrates the change in coefficient of variation of ink weight deposited as a function of the three key variables. Normal printing is done in a squeegee speed range of 3 to 6 in./s and a snap-off distance of 0.025 to 0.040 in. Squeegee compression, which directly affects the force applied to the substrate to be printed, is best kept within the 0.006- to 0.012-in. range. Excessive squeegee compression, although useful in improving deposited-ink uniformity, unnecessarily stresses the substrate and hastens squeegee wear.

The applied force vs squeegee compression was measured directly with a force gage and found to be about 0.6 lb at 0.009-in. squeegee compression as shown in Fig. 27. This mid-range compression value was then used for the test. Nine silicon solar-grade wafers, as-sawed,* about 0.022 in. thick were screen printed with the collector grid pattern on *both* sides of the wafer at 90° orientation to each other. This orientation maximized the stress applied to the wafers midway between the collector grid lines. The printed wafers were cleaned to remove the dried ink deposit and, with an unprinted control wafer, exposed to a thermal shock cycle. The wafers were immersed in liquid N_2 (-196°C) for 20 s and transferred rapidly to liquid 1-octodecanol (200°C), held there for 20 s and transferred rapidly to liquid methanol (45°C) to remove the 1-octodecanol. This cycle was repeated five times for all wafers.

*Commercial I.D. sawed wafers.

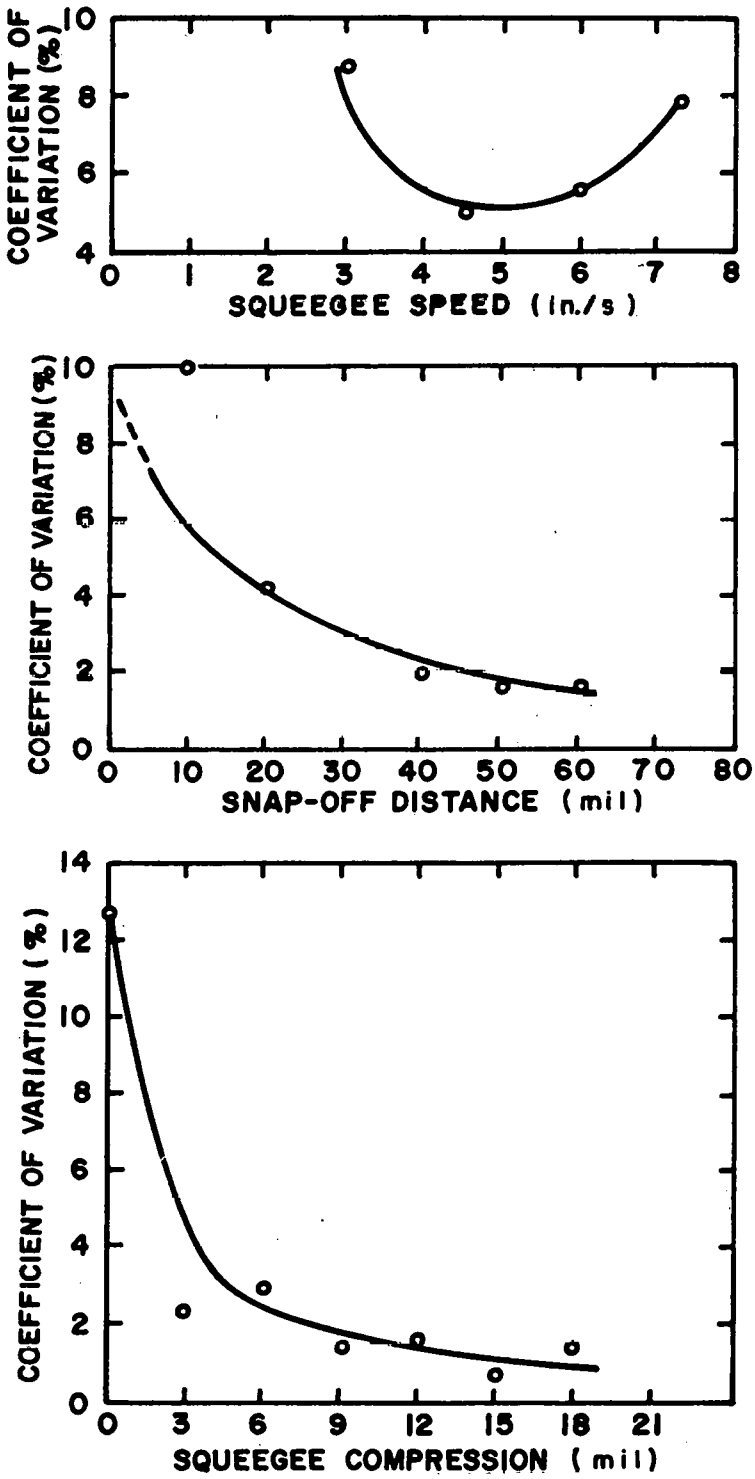


Figure 26. Effect of coefficient of variation of various screen-printing parameters.

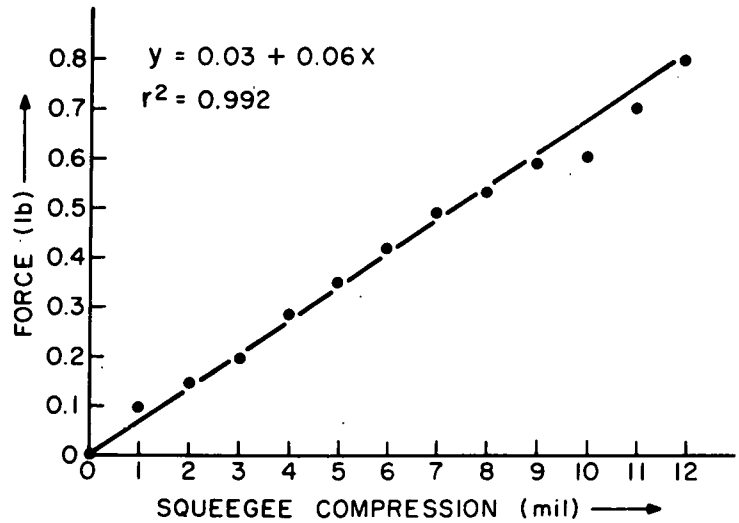


Figure 27. Applied force as a function of squeegee compression in screen-printing.

All wafers were subsequently examined microscopically and after etching* to delineate any cracks which may have formed during printing, thermal shocking, or etching. No cracks were found. It is therefore assumed that normal screen-printing forces will not damage wafers containing stress raising flaws induced by the sawing operations.

3. Materials Characterization

Several commercial inks were purchased and analyzed prior to evaluation. In the commercial frit-bearing inks, the frit generically consists of lead borosilicate in composition with varying proportions of the three major oxides PbO, B_2O_3, and SiO_2. The remaining elements are present in trace quantities and are brought in by impurities in the raw materials and/or ball-mill grinding of the frit. The solids content of the inks ranged from 78 to 83 wt pct.

For the formation of inks at RCA, three commercial Ag powders were selected, based on variation in particle size, and were analyzed for impurities by emission spectroscopy. Of those impurities found, Cu would most seriously affect the

*50 cc HNO_3, 30 cc HF, and 20 cc acetic acid.

electrical conductivity of silver, since 0.1 to 0.2 wt pct Cu is soluble near room temperature. The Metz* K-150 Ag perhaps exceeds this amount, but it was kept for comparative testing anyway.

Cellulosic polymers, which are used to control viscosity and green strength in the ink, were also analyzed. Although the Na level is significantly above background in each case, the total quantity remaining available for diffusion into silicon is negligible when the ultimate dilution with other ink ingredients is considered.

Three specific frits or adhesive agents were prepared, two by standard glass melting techniques and ball-mill grinding. The third, $AgPO_3$, was formed by chemical precipitation from the reaction between $AgNO_3$ and stabilized HPO_3. The stability of the third frit is in question, since x-ray diffraction analysis identified $Ag_4P_2O_7$ and/or Ag_3PO_4 in various instances. A summary of material properties is presented in Table 11. The good wetting exhibited by the $AgPO_3$ and $80PbO\text{-}10B_2O_3\text{-}10SiO_2$ frit makes them excellent candidates for metallization on n- and p-type silicon surfaces, respectively.

TABLE 11. MATERIAL PROPERTIES

Material (wt pct)	Specific Surface Area (m^2/g)	Density (g/cm^3)	Contact Angle* (Degree) on Si	on Ag
$PbO(80)\text{-}B_2O_3(10)\text{-}SiO_2(10)$	0.4453	6.376	5	14
$PbO(70)\text{-}ZnO(10)\text{-}B_2O_3(10)\text{-}SiO_2(10)$	0.5240	6.079	36	43
$AgPO_3$	0.0291†	3.702	18	0
Ag (Metz K-150)	3.40	10.490	--	--
Ag (Metz FS Type C)	0.88	10.490	--	--
Ag (U.S. Met. Ref. 71-2)**	0.24	10.490	--	--

*Contact angle: after 10 minutes at 675°C in air.
**U.S. Metals Refining, Carteret, NJ.
†Some difficulty was noted in obtaining this value; use with caution.

*Metz Metallurgical Co., South Plainfield, NJ.

Particle size distribution curves, determined by the x-ray sedimentation method, are shown for the three Ag powders (and one Al powder*) in Fig. 28 and confirm that the high-surface area K-150 contains the highest percentage of submicron particles. While the finer particles are an aid to rapid sintering at low firing temperatures, they require an additional organic vehicle for proper dispersion. The resultant decreased metallic content in the ink raises the effective sheet resistance. For comparative purposes, however, the three Ag powders were retained for preliminary evaluations.

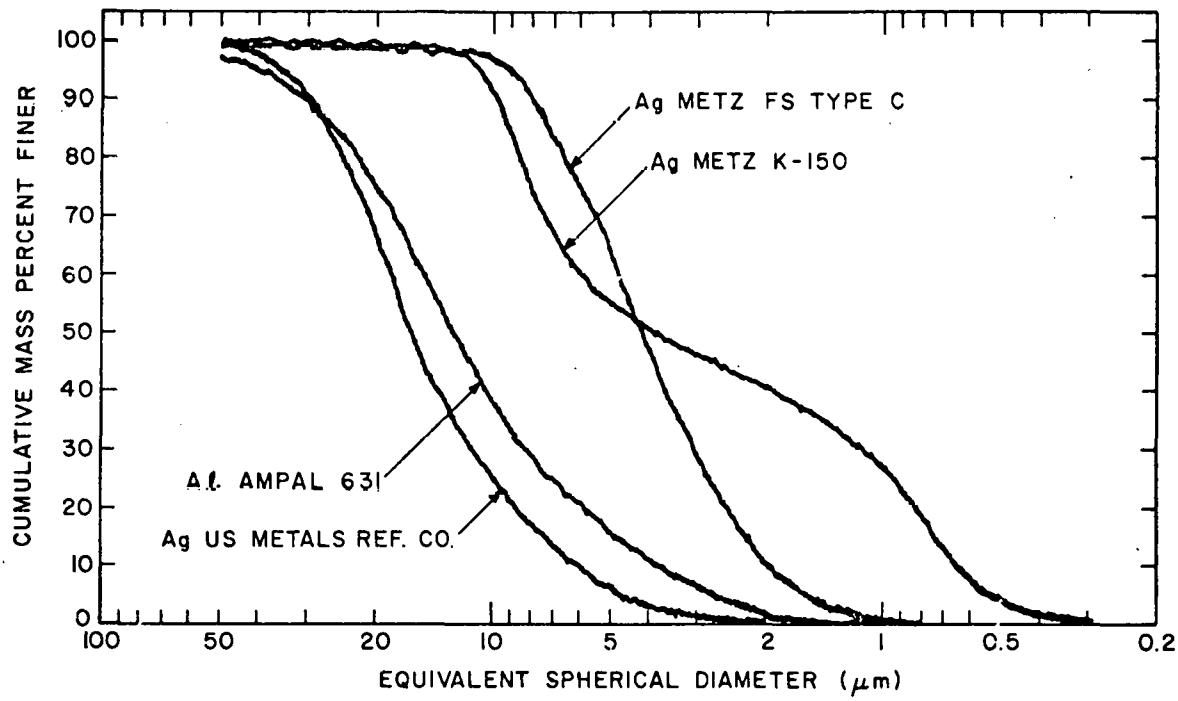


Figure 28. Powder particle size distribution curves.

4. Electrical Conductivity of RCA-Formulated and Commercial Inks

The frit and Ag powder were incorporated into an ink vehicle consisting of 6 wt pct ethyl cellulose (N-300) dissolved in butyl Carbitol,** i.e., diethylene glycol monobutyl ether. The final solids content of the ink varied with the specific surface area of the Ag powder. The solids content of the

*Ampal 631 is a product of US Bronze Powders, Flemington, NJ.
**Carbitol is a registered trademark of Union Carbide Corp., New York, NY.

Metz K-150 Ag could only achieve a maximum of 70 wt pct and still provide adequate screen-printing quality whereas the lower surface area powders, Metz FS type C and U.S. Metal Refining* Lot 71-2, could be increased to 80 wt pct and still print well.

The test inks were screen-printed through an 1874-square serpentine line pattern (0.015 in. wide, 0.015 in. spacing) onto a 1- by 1-in. 96% alumina test substrate to determine ink conductivity. As shown in Fig. 29, the sheet resistance does not appear to vary significantly when the ink is fired for various time and temperature combinations. When the fired film thickness is measured microscopically and resistivity is computed, the effect of increasing time and temperature becomes more apparent, as shown in Fig. 30. However, it became obvious that determining minute differences in electrical conductivity would require a more accurate measure of metal deposited. Consequently, after sintering the test patterns, the Ag ink and substrate were weighed, the electrical resistance was measured, the Ag ink was stripped in HNO_3, and the substrate was reweighed. Hence, the exact weight of Ag deposited was obtained and this value used to compute the ideal resistance for that amount of Ag. From the observed-to-ideal resistance ratio, the percent of bulk electrical conductivity was computed, and these values are reported for the RCA-formulated and commercial inks in Tables 12, 13, and 14. It should be noted that each test pattern was heated to 500°C for 2 min prior to heating to the listed combination in the Tables. The one exception is shown in Table 10 where the Thick Film Systems** (TFS) 3347 Ag was fired at 300 and 400°C to illustrate the poor electrical conductivity achieved at these low temperatures.

In Table 12, which compares the unfritted RCA-formulated Ag inks, the highest conductivities are achieved by the Metz K-150 (3.4 m^2/g surface area) and Metz FS Type (0.88 m^2/g). The values for the 600 to 700°C regime range from 47 to 64% of bulk electrical conductivity when fired for 600 s. However, the U.S. Metal Refining Ag (0.24 m^2/g) only achieved 30 to 43% under the same conditions. The later Ag powder was therefore excluded from further testing.

In Table 12 the influence of various frit additions upon electrical conductivity of Metz K-150 and FS Type C silver is compared. It can be seen that the presence of sufficient frit, i.e., 10 vol pct, improves conductivity as

*U.S. Metal Refining Co., Carteret, NJ.
**Thick Film Systems, Inc., Santa Barbara, CA.

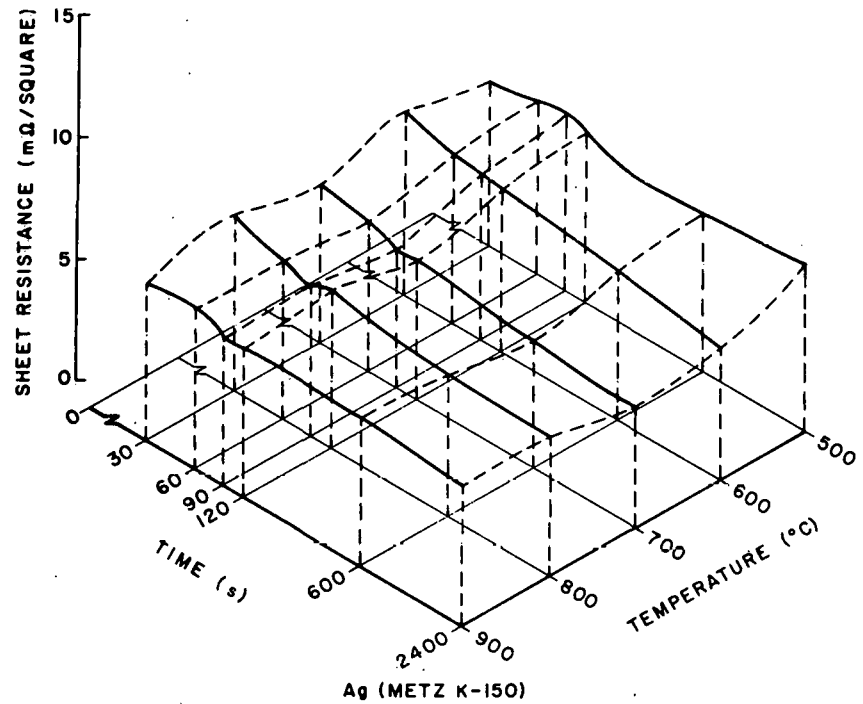


Figure 29. Firing time-temperature dependence of sheet resistance of screen-printed Metz K-150 silver ink.

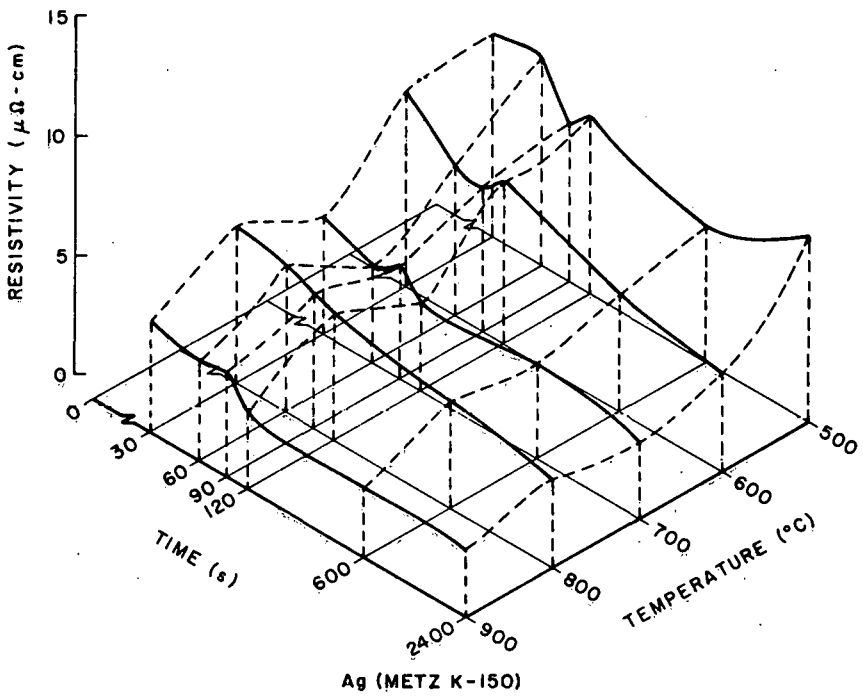


Figure 30. Firing time-temperature dependence of resistivity of sheet resistance of screen-printed Metz K-150 silver ink.

TABLE 12. PERCENT OF BULK ELECTRICAL CONDUCTIVITY OF RCA Ag INKS (NO FRIT)

	Temperature (°C)				
Time (s)	500	600	700	800	900
	RCA - Metz K-150 Ag				
30	50	46	52	47	52
60	47	49	54	52	55
90	45	49	59	55	55
120	47	50	59	47	55
600	52	55	64	57	58
2400	49	61	69	58	58
	RCA - Metz FS Type C Ag				
30	30	38	45	47	60
60	32	36	51	60	64
90	34	38	53	60	69
120	35	43	53	60	69
600	39	47	60	68	72
2400	41	53	61	70	75
	RCA - U.S. Metal Refining Lot 71-2 Ag				
30	25	26	31	--	41
60	24	26	32	33	45
90	26	28	35	35	44
120	26	29	35	35	22
600	28	30	43	37	35
2400	28	36	45	25	--

TABLE 13. PERCENT OF BULK ELECTRICAL CONDUCTIVITY OF RCA - METZ Ag vs FRIT CONTENT

	Temperature (°C)				
Time (s)	500	600	700	800	900
	RCA - Metz K-150 Ag (no frit)				
30	50	46	52	47	52
60	47	49	54	52	55
90	45	49	59	55	55
120	47	50	59	47	55
600	52	55	64	57	58
2400	49	61	69	58	58
	RCA - Metz K-150 Ag + 5 vol pct glass ($80PbO-10B_2O_3-10SiO_2$)				
30	48	47	56	60	60
60	48	48	58	59	58
90	47	55	58	59	56
120	45	56	59	63	57
600	49	51	59	62	61
2400	49	53	59	66	63
	RCA - Metz K-150 Ag + 10 vol pct glass ($80PbO-10B_2O_3-10SiO_2$)				
30	56	58	62	69	67
60	54	59	63	70	72
90	55	62	68	74	71
120	57	61	67	71	71
600	58	64	74	75	74
2400	58	70	71	74	69

TABLE 13. PERCENT OF BULK ELECTRICAL CONDUCTIVITY OF RCA - METZ Ag vs FRIT CONTENT (Continued)

	Temperature (°C)				
Time (s)	500	600	700	800	900
	RCA - Metz K-150 Ag + 5 vol pct $AgPO_3$				
30	41	36	50	55	60
60	36	41	48	56	60
90	38	44	53	63	63
120	38	46	54	64	64
600	39	46	62	69	65
2400	41	50	63	67	67
Time (s)	500	600	675		
	RCA - Metz FS Type C Ag + 10 vol pct glass ($80PbO-10B_2O_3-10SiO_2$)				
60	25	40	45		
90	32	44	48		
120	35	45	51		
600	42	54	61		
	RCA - Metz FS Type C Ag + 3 wt pct Al + 10 vol pct glass ($80PbO-10B_2O_3-10SiO_2$)				
60	24	35	40		
90	27	48	39		
120	32	40	39		
600	38	48	44		

TABLE 14. PERCENT OF BULK ELECTRICAL CONDUCTIVITY OF COMMERCIAL INKS

	Temperature (°C)				
Time (s)	300	400	500	600	700
	Thick Film Systems 3347 (Ag)				
30	15	18	44	51	59
60	15	18	47	55	64
90	15	18	47	58	67
120	15	18	48	60	68
600	15	19	53	68	75
Time (s)	500	600	700	800	900
	Owens-Illinois 6105 (Ag)				
30	54	61	61	65	74
60	54	56	68	71	80
90	53	55	70	75	83
120	50	56	72	79	87
600	50	62	79	87	95
2400	52	67	81	93	98
	Thick Film Systems A-250 (no glass) (Ag)				
30	39	53	64		
60	42	61	70		
90	43	64	72		
120	44	67	74		
600	51	73	80		
	Englehard E-422-C (Ag)				
30	55	57	63		
60	56	61	66		
90	57	62	69		
120	58	62	70		
600	61	70	76		

TABLE 14. PERCENT OF BULK ELECTRICAL CONDUCTIVITY OF COMMERCIAL INKS (Continued)

Time (s)	Temperature (°C) 500	600	700	800	900
		Engelhard E-422-E (Ag)			
30	42	45	49		
60	42	47	53		
90	43	48	55		
120	43	48	57		
600	46	52	62		
		Engelhard E-422-D (Ag/Al)			
30	42	44	36		
60	42	45	33		
90	44	45	32		
120	44	46	33		
600	46	47	32		
		Engelhard E-422-F (Ag/Al)			
30	35	37	22		
60	35	38	9		
90	35	38	9		
120	36	39	9		
600	38	39	7		

predicted by liquid-phase-assisted sintering theory [18]. For example, at the 600-s firing time, the percent of bulk electrical conductivity increases from 55 to 64% when fired at 600°C and 64 to 74% when fired at 700°C for the Metz K-150 Ag. The percent of bulk electrical conductivity for Metz FS Type C with 10 vol pct frit fired at 600°C-600 s, however, is only equivalent to the pure, unfritted Metz K-150. This result is also expected since larger Ag particles in the FS Type C powder do not sinter as rapidly as the smaller particles in the K-150 powder.

Despite the lower electrical conductivity of the FS Type C powder, a greater solids content, i.e., 80 wt pct vs 70 wt pct for the K-150, in the ink is possible due to the lower surface area of the Ag. This difference showed up in the fired film appearance which was more dense than the K-150 Ag film, and may influence solderability and adhesion properties.

The initial test completed with 8.3 vol pct addition of $AgPO_3$ showed lower conductivity (Table 13) than pure K-150 Ag when fired at 500 to 700°C. At 800 to 900°C the conductivity of the $AgPO_3$ based ink was greater than the pure K-150. This improvement at the higher temperatures implies that the $AgPO_3$ precipitate was not pure but contained higher melting compounds, e.g., $Ag_4P_2O_7$ (mp* 585°C) and Ag_3PO_4 (mp 849°C) vs $AgPO_3$ (mp 482°C). Thus the benefit derived from liquid-phase sintering did not occur until these compounds melted. Further development is needed with $AgPO_3$ stabilization to improve the desired effect of low-temperature liquid-phase-assisted sintering.

With Metz FS Type C flake silver, Figs. 31, 32, and 33 depict the changes in conductivity for firing times of 1, 2, and 5 min, respectively, at 600 to 900°C and $AgPO_3$ concentrations of 8.3 to 30.1 vol pct. If the three plots are superimposed, the conductivity results show the 5-min firing time to be slightly superior, but the 1- and 2-min firing times are almost identical. The similarity in conductivity results provides a wide latitude in processing time. Hence, optimization of metallization solderability and adhesion can proceed without too much concern for conductivity losses. The slight decline in conductivity between 8.3 and 30.1 vol pct $AgPO_3$ may imply that lower concentrations would provide higher conductivity. While apparently contrary to

18. K. R. Bube and T. T. Hitch, "Basic Adhesion Mechanisms in Thick and Thin Films," Final Report, March 1978, NASC Contract N00019-77-C-0176.

*Melting point.

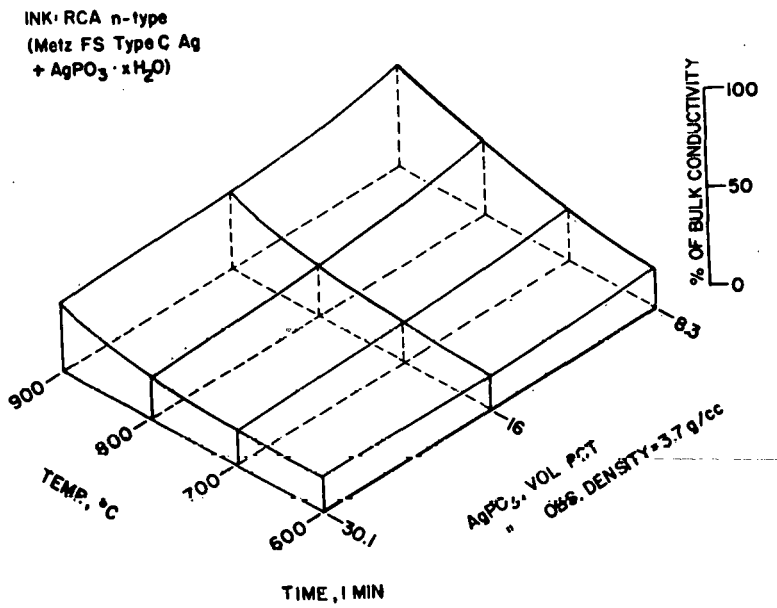


Figure 31. Conductivity vs temperature and vol pct $AgPO_3$ for RCA n-type ink. Firing time = 1 min.

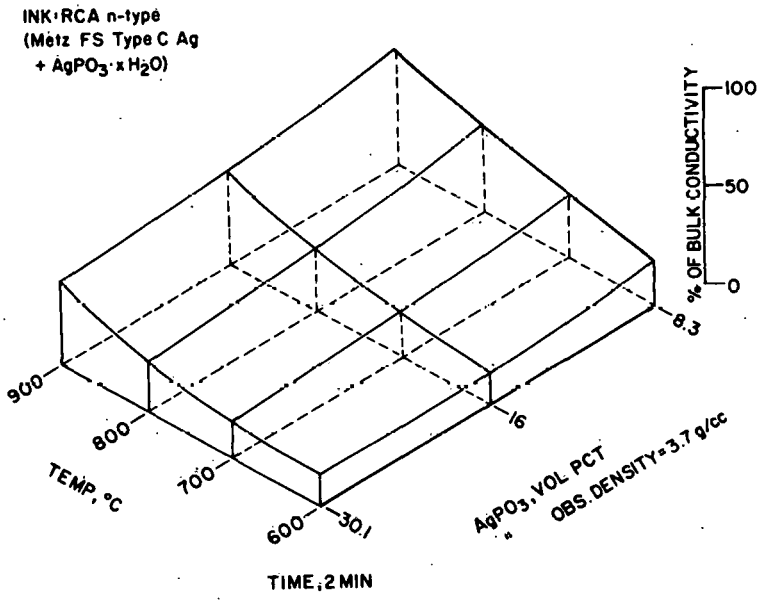


Figure 32. Conductivity vs temperature and vol pct $AgPO_3$ for RCA n-type ink. Firing time = 2 min.

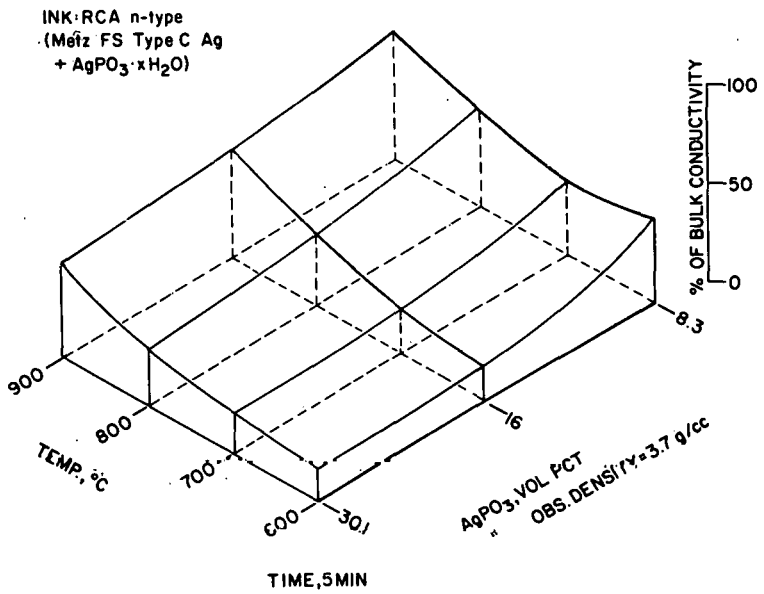


Figure 33. Conductivity vs temperature and vol pct $AgPO_3$ for RCA n-type ink. Firing time = 5 min.

liquid-phase sintering theory, the extreme wettability, e.g., the 0° contact angle between Ag and $AgPO_3$, may account for very rapid sintering at lower concentrations than are usually observed. Excessive concentrations of the nonconductive phase would then predictably increase the electrical resistance of the film.

For contact to the p-type Si on the back of the cell, a Ag + 3 wt pct Al ink was prepared containing 10 vol pct glass. As shown in Table 13, the conductivity is generally lower than the unalloyed Ag inks for equivalent firing conditions. In air firing, two competing reactions are occurring, namely, oxidation of the Al powder and alloying with the Ag. Both tend to reduce the electrical conductivity, while sintering tends to raise it. Extended time at higher temperature appears to have a neutral to negative effect upon conductivity.

The electrical conductivity of commercial inks appears in Table 14 and shows data for Thick Film Systems 3347, A-250, Owens-Illinois* (OI) 6105, Engelhard** E-422-C, E-422-E, E-422-D (Ag/Al), and E-422-F (Ag/Al). When fired at 300 to 400°C the TFS 3347 Ag never exceeds 19% of bulk electrical conductivity, indicating the basic reason for much higher peak firing temperatures.

*Owens-Illinois, Inc., Toledo, OH.
**Engelhard Industries, Inc., East Newark, NJ.

When fired at higher temperatures, the conductivities are slightly higher than the RCA-Metz K-150 with 10 vol pct glass. Without careful analysis of Ag particle size distribution and glass composition and content it is difficult to surmise which, if not all, factors are contributing to the improvement. When TFS 3347 is compared with fritless TFS A-250, the higher electrical conductivity of the latter is also difficult to assess. At least the three previously mentioned factors can influence conductivity, i.e., Ag particle size distribution, glass content, and glass composition. For example, if the glass content is not sufficiently high or the glass viscosity is not sufficiently low at the selected firing temperatures, the conductivity will not be as high as the pure Ag ink, in keeping with liquid-phase-assisted sintering.

The phosphorus-bearing OI-6105 Ag shows progressively superior conductivity with increasing temperature when compared with RCA-Metz K-150 in the 700 to 900°C range. It is the only ink which actually approaches pure Ag conductivity when fired at 900°C for 2400 s. However, in the region of interest, e.g., 600 s at 600 to 700°C, the inks are about equivalent in conductivity.

Limited testing was also completed on two Engelhard Ag and two Engelhard Ag/Al inks. Ag ink E-422-C shows slightly superior conductivity in the 600-s, 600 to 700°C region and the other one, E-422-E, considerably lower conductivity than the RCA-Metz K-150 ink. Similarly, the Ag/Al inks are about comparable or slightly lower in conductivity.

In addition to Ag inks, a Cu ink, Cermalloy* 7029-5, was analyzed and found to contain a lead borosilicate frit, similar to the Ag inks. Conductivity data for the Cu ink were obtained after firing in tank N_2 and deoxidized tank N_2, and, as shown in Table 15, the Cu ink is considerably lower in conductivity in the area of interest, e.g., 600 to 700°C, than the RCA-Metz K-150 Ag ink.

Furthermore the dot-to-dot pattern, used for determining specific contact resistance, was applied to a silicon solar cell (lot 85). The contact resistance was measured after firing at 500, 600, and 700°C for 5 min and found to be 1.77 Ω-cm^2 at 500°C, 0.70 Ω-cm^2 at 600°C and 0.41 Ω-cm^2 at 700°C. The combination of high contact resistance and low electrical conductivity for the Cu ink is not encouraging. Therefore, attention will continue to be directed toward the Ag inks.

*Division of Bala Electronics, West Conshohocken, PA.

TABLE 15. PERCENT OF BULK ELECTRICAL CONDUCTIVITY

Cermalloy 7029-5 (Cu)

Time (s)	Temperature (°C) 500	600	700	800	900
	Ambient: Tank N_2, preheat 500°C-2-min				
30	22	27	33	41	45
60	22	28	40	48	55
90	22	36	43	51	57
120	24	33	46	50	56
600	28	48	54	59	62
2400	28	53	61	57	--
	Ambient: Deoxidized N_2, without 500°C-2-min preheat				
60	4	24	35	43	55
90	9	28	40	50	58
120	12	31	50	53	61
600	19	44	53	62	71

To test the effectiveness of laser heating as a quick means of sintering a screen-printed Ag line, a small comparative test was carried out. A 0.015-in.-wide x 0.75-in.-long test bar was screen-printed onto single-crystal Si pieces. Samples A and B were preheated after printing to burn out the polymer in the ink at 400°C for 30 s. If the ink polymer is not removed prior to exposure to the laser beam, the pattern is explosively removed upon laser pulsing.

Sample A was exposed to a Nd:glass laser pulse of 2.9 J/cm^2 and a second pulse of 3.6 J/cm^2. Sample B was fired in a belt furnace set to achieve about a 10-min dwell at 675°C. Electrical measurement showed sample A (laser pulsed) decreased in electrical resistance about 13% while sample B decreased about 58%. Thus, laser pulsing does not appear to be a practical way for rapidly sintering a screen-printed Ag line on Si.

5. Solderability of RCA and Commercial Inks

Some preliminary tests were performed to determine relative solderability values. Both OI-6105 phosphated-silver ink and RCA inks were screened onto 96% Al_2O_3 substrates using the 1874-square serpentine pattern. After drying and firing for 10 min at 675°C, the metallization patterns were coated with Kester* 1544 solder flux and immersed in 215°C solder, i.e., 62Sn-36Pb-2Ag (wt pct), for varying times from 2 to 8 s. The sample patterns were visually examined to determine the extent of solder dewetting which is indicative of excessive silver dissolution by the solder or poor initial wettability. As shown in Table 16, OI-6105 is essentially unsolderable or too rapidly dissolved by the solder. The first RCA ink, Metz FS type C Ag + 10 vol pct PBS frit (i.e., $80PbO-10B_2O_3-10SiO_2$ wt pct) showed only slight dewetting up to 6 s. The second RCA ink, Metz FS type C Ag + 10 vol pct PBS frit + 3 wt pct Al, showed slightly greater dewetting but more resistance to longer immersion in molten solder.

TABLE 16. SOLDERABILITY COMPARISON - PERCENT DEWETTING

Metallization	Time (s) in 215°C - Solder (62Sn-36Pb-2Ag, wt pct)*			
	8	6	4	2
OI-6105	70-80	80-85	70-80	70-80
RCA-Metz FS Type C+ 10 vol pct PBS**	30-40	1	2	1
RCA-Metz FS Type C+ 10 vol pct PBS** +3 wt pct Al	5	5	5	5

*Flux: Kester 1544
**Frit: PBS is $80PbO-10B_2O_3-10SiO_2$ (wt pct)

The adhesion test pattern, described subsequently and shown in Fig. 34, also contained a large dot which was used in conjunction with reflowed solder balls to measure the solder-to-metallization contact angle.

A cursory examination of solderability of 4.2, 8.3, and 16 vol pct $AgPO_3$ inks showed the latter two to be unsolderable (with 62Sn-36Pb-2Ag wt pct

*Kester Solder Co., Chicago, IL.

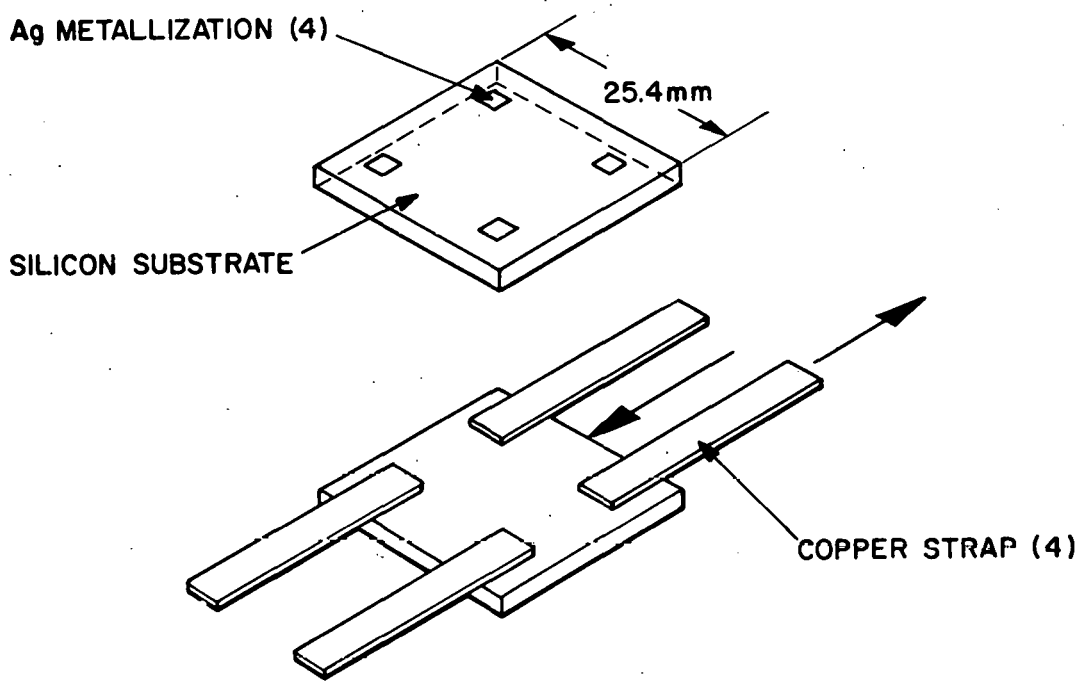


Figure 34. Adhesion test pattern.

solder and Kester 1544 flux) when the inks were fired on Si at 800 or 900°C for 1 or 2 min. The 4.2 vol pct $AgPO_3$ ink produced contact angles of 90 to 95° when the ink was fired at 700 or 800°C for 10 min.

More detailed studies of the $AgPO_3$ and lead borosilicate-based Ag ink solderabilities were conducted on n^+- and p-Si, respectively. Table 17 summarizes the data for $AgPO_3$-based inks containing 2 to 8 vol pct $AgPO_3$ and indicates progressively diminishing solderability with increasing $AgPO_3$ content. Best results are found in the 800 to 900°C ink firing temperature range with firing times of 1 to 3 min.

For lead borosilicate-based inks fired onto p-Si substrates the results, as shown in Table 18, indicate progressively decreasing solderability with increasing glass content, firing temperature, and time. With glass contents of 2.5 or 5 vol pct, solderability was acceptable for shorter firing times, e.g., 1 to 5 min, in the 600 to 900°C firing range. For the 15 vol pct glass-bearing ink, solderability results indicated a maximum firing range of 600 to 700°C for 1 to 5 min would be acceptable. Figures 35 through 40 summarize contact angle data graphically in n- and p-Si.

TABLE 17. SOLDER CONTACT ANGLE TO $AgPO_3$-BEARING Ag METALLIZATIONS ON n^+-Si (100) SUBSTRATE*

Balance Metz FS Type C Ag

Firing Conditions °C-min	$AgPO_3$ vol pct 2	4	6	8
		Angle (Degree)		
600 - 1	D†	32	58	L††
2	D	104	114	L
3	D	62	L	71
700 - 1	36	124	124	L
2	24	D	L	L
3	D	D	100	L
800 - 1	46	63	60	L
2	45	133	136	43
3	57	56	144	L
900 - 1	33	146	151	L
2	25	49	50	L
3	27	102	85	99

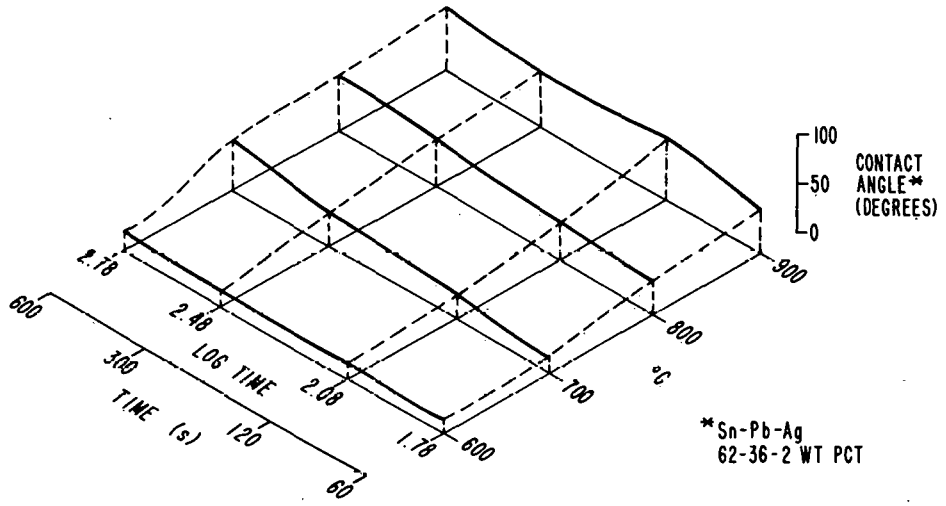
*Reflowed solder (62Sn-36Pb-2Ag wt pct) balls using Kester 1544 solder flux and 215 ±2°C interface temperature for 5 to 8 s.

†D - Ag metallization pad dissolved by molten solder.
††L - Solder ball lifted, i.e., did not wet metallization.

TABLE 18. SOLDER CONTACT ANGLE TO LEAD BOROSILICATE-BEARING Ag METALLIZATIONS on p-Si SUBSTRATE*

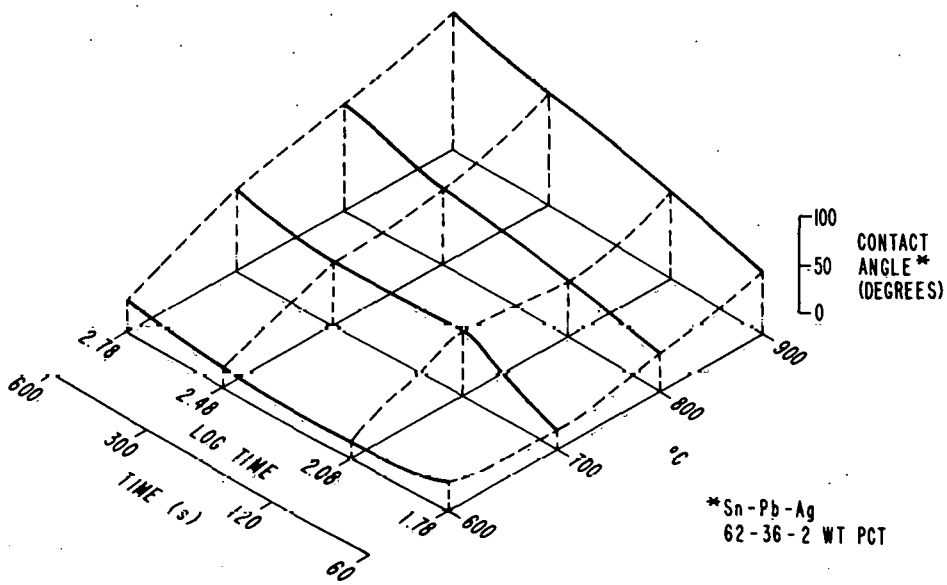
Time (min)	Temperature (°C) 600	700	800	900
	Angle (Degree)			
	2 vol pct PBS** balance Metz FS Type C Ag			
1	17	17	35	49
2	18	24	40	69
5	19	37	52	59
10	18	52	62	68
	5 vol pct PBS balance Metz FS TYPE C Ag			
1	33	22	44	67
2	19	71	60	95
5	21	70	80	117
10	35	87	112	144
	15 vol pct PBS balance Metz FS Type C Ag			
1	44	77	117	159
2	51	109	139	160
5	76	109	157	159
10	82	149	158	158

*Reflowed solder (62Sn-36Pb-2Ag wt pct) balis using Kester 1544 solder flux and 215 +2°C interface temperature for 5 to 8 s.
**PBS = 80PbO-10B_2O_3-10SiO_2, wt pct.



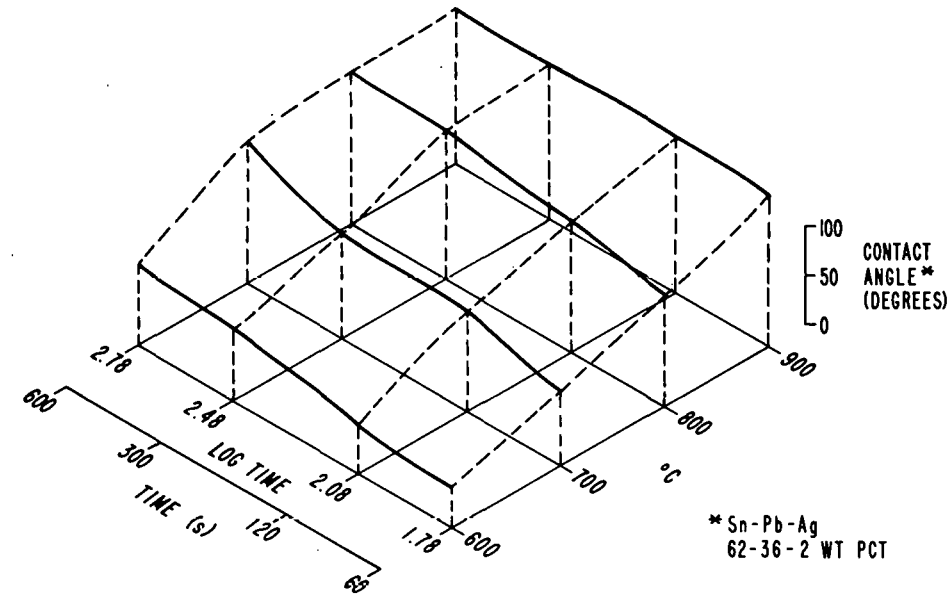
Ag (METZ FS TYPE C) + 2.5 VOL PCT PBS FRIT ON p-Si

Figure 35. Wet solder contact angle as a function of firing temperature and time for Ag + 2.5 vol pct PBS ink on p-silicon.



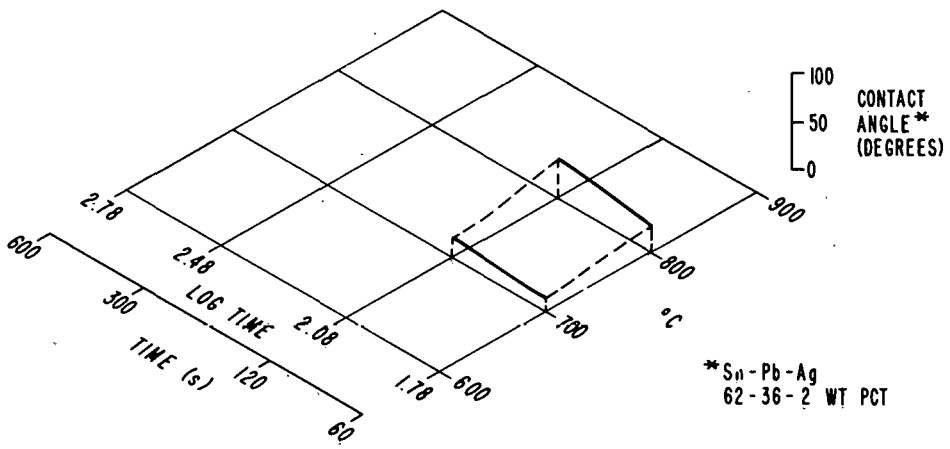
Ag (METZ FS TYPE C) +5 VOL PCT PBS FRIT ON p-Si

Figure 36. Wet solder contact angle as a function of firing temperature and time for Ag + 5 vol pct PBS ink on p-silicon.



Ag (METZ FS TYPE C) +15 VOL PCT PBS FRIT ON p-Si

Figure 37. Wet solder contact angle as a function of firing temperature and time for Ag + 15 vol pct PBS ink on p-silicon.



Ag (METZ FS TYPE C) + 2.5 VOL PCT PBS FRIT ON n-Si

Figure 38. Wet solder contact angle as a function of firing temperature and time for Ag + 2.5 vol pct PBS ink on n-silicon.

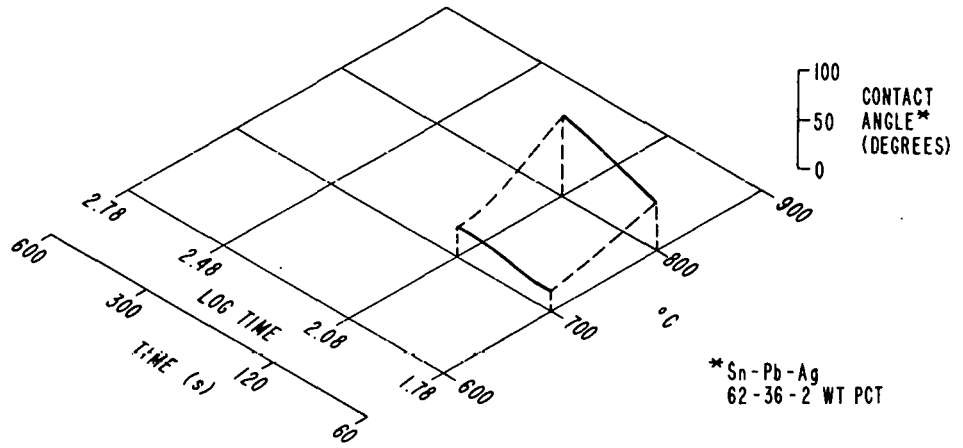


Figure 39. Wet solder contact angle as a function of firing temperature and time for Ag + 5 vol pct PBS ink on n-silicon.

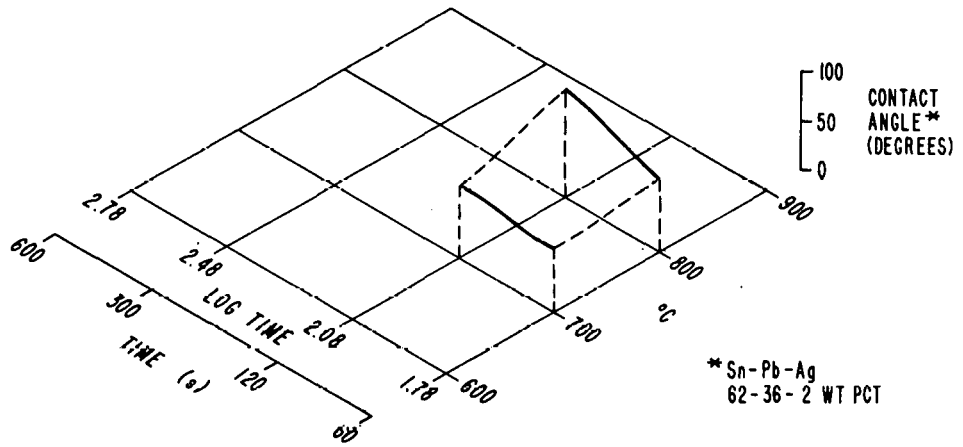


Figure 40. Wet solder contact angle as a function of firing temperature and time for Ag + 15 vol pct PBS ink on n-silicon.

Solderability can be improved by rinsing the fired metallization in HF (1 vol pct) for 30 s prior to soldering with flux. For example, as shown in Table 19, both the 15 vol pct PBS ink and commercial TFS 3347 (a lead borosilicate-based ink), which were fired for 2 min at 675 or 700°C, show a marked improvement in solderability after HF rinsing. Table 19 is also arranged to present data on adhesion strength results after thermal cycling, which is discussed below.

TABLE 19. SOLDER CONTACT ANGLE TO LEAD BOROSILICATE-BEARING Ag METALLIZATIONS ON n^+-Si (100) SUBSTRATE*

	Without Temperature Cycling		With Temperature Cycling**	
	Firing Conditions, 2 Min at			
	675°C	700°C	675°C	700°C
	Angle (Degree)			
	control			
TFS3347	33	44	49	37
RCA 15 vol pct PBS frit	47	73	49	62
	HF rinsed***			
TFS3347	20	18	16	19
RCA 15 vol pct PBS frit	20	21	19	17

*Reflowed solder (62Sn-36Pb-2Ag wt pct) balls using Kester 1544 solder flux and 215 ±2°C interface temperature for 5 to 8 s.
**Five cycles: 25°C to -40°C to 55°C to 25°C with 5-min dwell at extreme temperatures; single cycle time = 30 min.
***Immersed for 30 s in 1 vol pct HF in H_2O followed by deionized H_2O rise for 10 min at room temperature.

6. Adhesion Strength of RCA and Commercial Ag Inks

Despite the poor solderability of OI-6105 it was included in the initial adhesion strength determinations which follow. The two RCA Ag inks and frit-bearing Engelhard 422E (Ag), 422F (Ag/Al), and Thick Film Systems 3347 (Ag) were also included, as well as fritless Thick Films Systems 250 (Ag). All the

inks were screen-printed with 325 mesh screen and 0.001-in. (0.0254-mm) emulsion buildup onto polished (100) silicon substrates so as to yield four test pads measuring 0.1 x 0.1 in. (2.5 x 2.5 mm) as shown in Fig. 34. The samples were dried and fired under three separate conditions: A - 675°C for 2 min in a tube furnace, B - 675°C for 5 min in a belt furnace moving at 15.2 cm (6 in.)/min, and C - 675°C for 10 min in the belt furnace moving at 7.6 cm (3 in.)/min. Copper straps were then applied by a reflow soldering technique for adhesion shear stress testing. The copper straps, which were pretinned with solder, measured 1.34 x 0.14 x 0.003 in. (34 x 3.5 x 0.08 mm). Kester 1544 solder flux and two 62Sn-36Pb-2Ag solder balls weighing about 0.005 g each were applied to the metallization test pads. The copper straps were positioned over the test pads and the assembly was placed on a 215 ±2°C hot plate. Heating to 215°C took about 45 s, and the assembly was held at 215°C for 5 to 8 s before being quickly removed and cooled on a chilling block.

A shearing stress was then applied to the copper strap-metallization interface in an Instron Test Machine after allowing the assemblies to equilibrate for several hours at room temperature. The shearing forces, reported in Table 20, indicate a range of 0 (TFS fritless Ag 250) to 6087 g (RCA-Metz FS type C + 10 vol pct PBS frit +3 wt pct Al). This maximum value is equivalent to 1342 lb/in.^{2} (0.94 kg/mm^2) shear stress over the entire pad area. In many instances, however, the copper strap broke, in which case the silicon-metallization interface failure stress was not actually achieved, i.e., the interface strength exceeded the copper strap strength. In general, the three failure modes, e.g., copper, silicon, and interface failure, were observed on various inks with the weaker ones showing a predominance of interface failures. The stronger inks are generally noted to be the RCA inks and TFS 3347.

More detailed adhesion strength determinations were subsequently conducted on $AgPO_3$ and lead borosilicate-based Ag inks as well as the commercial lead borosilicate-based TFS 3347. The $AgPO_3$-based Ag ink was examined as a function of composition (2 to 8 vol pct $AgPO_3$), firing temperature (600 to 900°C), and time (1 to 3 min). Table 21 illustrates that acceptable adhesion strength demonstrated by copper strap failure, was found consistently only when the 2 vol pct $AgPO_3$ sample was fired at 900°C for 3 min. At lower firing temperatures, e.g., 600 and 700°C, copper strap-to-silicon delaminations were uniformly noted with no strength at low $AgPO_3$ concentrations. Consequently,

TABLE 20. METALLIZATION ADHESION SUMMARY FIRING CONDITIONS

Ink	Parameter	A 675°C-2 min (Tube)	B 675°C-5 min (Belt-6 in./min)	C 675°C-10 min (Belt-3 in./min)
OI-6105	$\bar{x}$* (g)	-	4015	4045
	%V**	-	33.3	8.7
	mode+	-	b	a,b,c
TFS 250	$\bar{x}$	0	2775	0
	%V		21.7	
	mode	c	c	c
TFS 3347	$\bar{x}$ (g)	5465	5823	4818
	%V	9.1	5.3	11.9
	mode	a,b	a	a
Eng 422E	$\bar{x}$ (g)	0	4460	3930
	%V		43.3	37.8
	mode	c	b,c	a,b,c
Eng 422F	$\bar{x}$ (g)	3310	4218	3828
	%V	35.6	14.4	16.7
	mode	c	c	a,b,c
RCA-Metz FS Type C + 10 vol pct PBS	$\bar{x}$ (g)	4785	6015	5443
	%V	2.6	7.4	3.2
	mode	b,c	a	a
RCA-Metz FS Type C + 10 vol pct PBS + 3 wt pct Al	$\bar{x}$ (g)	4785	5533	5443
	%V	3.2	8.2	27.6
	mode	a,b	a,b	a,b

*$\bar{x}$ = shearing force, average value.
**%V = coefficient of variation.
+ Legend for failure mode: a = copper strap broke
b = silicon wafer broke partially or completely.
c = delamination somewhere between copper strap and silicon.

TABLE 21. ADHESION STRENGTHS OF $AgPO_3$-BEARING Ag METALLIZATIONS ON n^+-Si (100) SUBSTRATE

$AgPO_3$, Balance Metz FS TYPE C Ag

Parameter*												
							2 vol pct					
Temp (°C)	600			700			800			900		
Time (min)	1	2	3	1	2	3	1	2	3	1	2	3
$\bar{x}$ (kg)	0	0	0	0	0	0	0	0	0	0	0	0
%V	-	-	-	-	-	-	-	-	-	114	6	8
Failure Mode	c	c	c	c	c	c	c	c	c	b,c	a,b	a
Contact Angle (deg)	D	D	D	36	24	D	46	45	57	33	25	27
							4 vol pct					
$\bar{x}$ (kg)	0	0	0	0	0	0	0	1.6	0.6	1.6	5.3	5.0
%V	-	-	-	-	-	-	-	-	-	-	32	26
Failure Mode	c	c	c	c	c	c	c	c	c	c	a,b,c	a,c
Contact Angle (deg)	32	104	62	124	D	D	63	133	56	146	49	102
							6 vol pct					
$\bar{x}$ (kg)	0	0	0.8	0	0.8	0	0.6	1.8	3.0	3.8	5.4	5.9
%V	-	-	-	-	-	-	-	81	61	47	17	5
Failure Mode	c	c	c	c	c	c	c	c	c	b,c	a,b,c	b,c
Contact Angle (deg)	58	114	L	124	L	100	60	136	144	151	50	85
							8 vol pct					
$\bar{x}$ (kg)	0	1.0	0.6	0.4	0	0.6	0	0.7	0	1.3	2.6	4.0
%V	-	-	54	-	-	-	-	-	-	-	-	27
Failure Mode	c	c	c	c	c	c	c	c	c	c	c	b,c
Contact Angle (deg)	L	L	71	L	L	L	L	43	L	L	L	99

*Legend: $\bar{x}$ = force at failure in kg, average
%V = coefficient of variation, (Standard deviation ÷ $\bar{x}$) 100, sample size, n = 4, normally

Failure mode - a = copper strap broke
b = silicon wafer fractured or silicon chip removed under metallization
c = delamination somewhere between copper strap and silicon

effort was shifted to the lead borosilicate-based inks in order to obtain improved adhesion at lower firing temperatures.

From Table 22 it is clear that adhesion strength and failure mode varied with firing temperature, time, and glass content on p-Si substrate material. At low glass concentrations, e.g., 2.5 and 5 vol pct, acceptable adhesion and failure modes were found at the higher firing temperatures and time. With the higher glass content, e.g., 15 vol pct, acceptable results shifted to the lower firing temperatures, e.g., 600°C for times of 1 to 10 min and 700°C for 1 to 5 min. The results are consistent with glass wetting and sintering phenomena. At low glass concentrations, longer time and higher temperatures are required for sufficient quantity of glass to reach the Si surface to provide adequate adhesion between sintered Ag particles and the Si substrate. At high glass concentrations, e.g., 15 vol pct, sufficient glass is almost immediately present at the Ag-Si interface. Prolonged heating at elevated temperatures increases Ag film densification but also promotes additional wetting of the available Ag surfaces away from the Ag-Si interface. This additional wetting or coating of Ag particles with glass reduces solderability, as evidenced by the increasing contact angles for the 15 vol pct samples when fired at higher temperatures and longer times. With decreased solderability, an increasing frequency of copper strap-to-silicon delaminations was observed.

Limited adhesion strength measurements were again taken after depositing the same Ag inks on n^+-Si (100) substrates. In addition, these samples were exposed to three cycles of extreme liquid-to-liquid thermal shock, e.g., -75 to 125°C, in order to confirm the superiority of the 15 vol pct material. As shown in Table 23, only the 15 vol pct ink came close to acceptable limits. The consistent silicon fracturing is due to the mismatch in thermal expansion coefficients between glass and silicon.

Since HF rinsing of the fired Ag metallizations had been shown to improve solar-cell fill factor and efficiency, a test was conducted to compare the adhesion strength of rinsed and unrinsed samples with milder thermal cycling, e.g., -40 to 55°C. Both TFS 3347 and the RCA lead borosilicate-bearing ink were tested after firing at 675 and 700°C for 2 min.

As shown in Table 24, under all conditions both inks, with the exception of one sample, exhibited acceptable adhesion strength. After 30-s immersion in 1 vol pct HF at room temperature, the solderability of both inks improved

TABLE 22. ADHESION STRENGTH OF LEAD BOROSILICATE-BEARING Ag METALLIZATION ON p-Si (100) SUBSTRATE ($80PbO\text{-}10B_2O_3 10SiO_2$ wt pct) Balance Metz FS Type C Ag

Temperature (°C)	600				700				800				900			
2.5 vol pct																
Time (min)	1	2	5	10	1	2	5	10	1	2	5	10	1	2	5	10
$\bar{x}$ (kg)	3.5	3.9	3.5	6.3	3.1	5.3	6.8	6.6	4.9	6.6	6.7	7.2	7.1	7.3	7.3	6.9
%V	22	18	45	7	33	19	3	6	27	4	2	9	4	2	1	3
Failure Mode	c	c	c	b	c	a,b,c	a	a	a,c	a,b	a,b	a	a	a	a	a,b
Contact Angle (deg)	17	18	19	18	17	24	37	52	35	40	52	62	49	69	59	68
5.0 vol pct																
$\bar{x}$ (kg)	6.2	5.5	5.8	6.0	5.9	6.7	5.7	7.1	4.0	5.8	6.8	6.7	6.5	6.7	6.4	6.5
%V	5	26	10	10	17	5	16	6	38	12	9	8	10	13	21	2
Failure Mode	c	a,c	a,c	a,c	a,c	a,b,c	b,c	a	c	c	a,b,c	a,b	a,b,c	a,b	a,b	a,b
Contact Angle (deg)	33	19	21	35	22	71	70	87	44	60	80	112	67	95	117	144
15.0 vol pct																
$\bar{x}$ (kg)	6.8	7.1	6.9	6.8	6.8	6.5	6.9	7.1	6.9	6.7	4.6	2.8	6.4	4.7	4.8	4.5
%V	7	4	9	2	8	12	4	3	4	6	30	75	6	28	49	34
Failure Mode	a	a	a	a	a	a	a	a,b,c	a	a	c	c	a	a,c	a,c	c
Contact Angle (deg)	44	51	75	82	77	109	109	149	117	139	157	158	159	160	159	158

Legend: $\bar{x}$ = force at failure in kg, average
%V = coefficient of variation, (standard deviation ÷ $\bar{x}$) 100, sample size, n=4 normally

Failure mode – a = copper strap broke
b = silicon wafer fractured or silicon chip removed under metallization
c = delamination somewhere between copper strap and silicon

TABLE 23. ADHESION STRENGTH AFTER THERMAL SHOCK FOR LEAD BOROSILICATE-BEARING Ag METALLIZATION ON n^+-Si (100) SUBSTRATE

($80PbO-10B_2O_3-10SiO_2$ wt pct) Balance Metz FS Type C Ag

Parameter				
	2.5 vol pct			
Temp (°C)	700		800	
Time (min)	1	2	1	2
$\bar{x}$ (kg)	0	0	0	0.6
%V	-	-	-	43
Failure Mode	c	c	b,c	b
Contact Angle (deg)	14	22	29	41
	5.0 vol pct			
$\bar{x}$ (kg)	0.4	0.8	1.2	0.6
%V	-	73	-	-
Failure Mode	c	b,c	b,c	b,c
Contact Angle (deg)	20	33	51	85
	15.0 vol pct			
$\bar{x}$ (kg)	1.2	1.4	2.6	5.1
%V	33	36	40	18
Failure Mode	b	b	b	a,b
Contact Angle (deg)	68	78	74	113

Legend: $\bar{x}$ = force at failure in kg, average
%V = coefficient of variation, (standard deviation ÷ $\bar{x}$) 100, sample size, n = 4 normally

Failure Mode - a = copper strap broke
b = silicon wafer fractured or silicon chip removed under metallization
c = delamination somewhere between copper strap and silicon

TABLE 24. ADHESION STRENGTH OF LEAD BOROSILICATE-BEARING Ag METALLIZATION ON n^+-Si (100) SUBSTRATE

	Without Temperature Cycling		With Temperature Cycling*	
	Firing Conditions, 2 min at			
Parameters	675°C	700°C	675°C	700°C
		Control		
TFS 3347, $\bar{x}$ (kg)	6.5	6.5	5.6	6.5
%V	7	16	-	12
Failure Mode	a	a	a	a
Contact Angle (deg)	33	44	49	37
RCA, 15 vol pct PBS, $\bar{x}$ (kg)	6.5	6.6	6.4	6.4
%V	4	2	10	5
Failure Mode	3a,1c	a	a	a
Contact Angle (deg)	47	73	49	62
		HF rinsed***		
TFS 3347, $\bar{x}$ (kg)	6.6	6.5	6.7	6.5
%V	7	4	5	6
Failure Mode	a	a	a	a
Contact Angle (deg)	20	18	16	19
RCA, 15 vol pct PBS, **$\bar{x}$ (kg)	6.8	6.2	6.5	6.8
%V	5	10	4	3
Failure Mode	a	a	a	a
Contact Angle (deg)	20	21	19	17

*Temperature cycle: five cycles from 25°C to -40°C to 55°C to 25°C, with 5-min dwell at extreme temperature; single cycle time = 30 min.

**15 vol pct PBS - 15 vol pct glass frit composed of $80PbO-10B_2O_3-10SiO_2$ (wt pct)

***Parts immersed for 30 seconds in aqueous HF (1 vol pct) solution followed by deionized water rinse for 10 min

Failure mode: a = copper strap broke
b = silicon wafer fractured or silicon chip removed under metallization
c = delamination somewhere between copper strap and silicon

notably, as evidenced by a decrease in the contact angle. Under these conditions, all samples were strong enough to sustain copper strap breaks, i.e., shear stress in excess of 1 kg/mm^2.

7. Metallization Penetration

Figure 41 illustrates the range of the typical phosphorous concentration profiles for average-depth n- on -p solar cells. Since it is known that metallization contact resistance rises abruptly if the phosphorous concentration is much below 10^{19} $atoms/cm^3$, it is apparent from Fig. 41 that metallization penetration, i.e., dissolution of the high phosphorous concentration region by ink constituents, must be less than about 0.1 μm average.

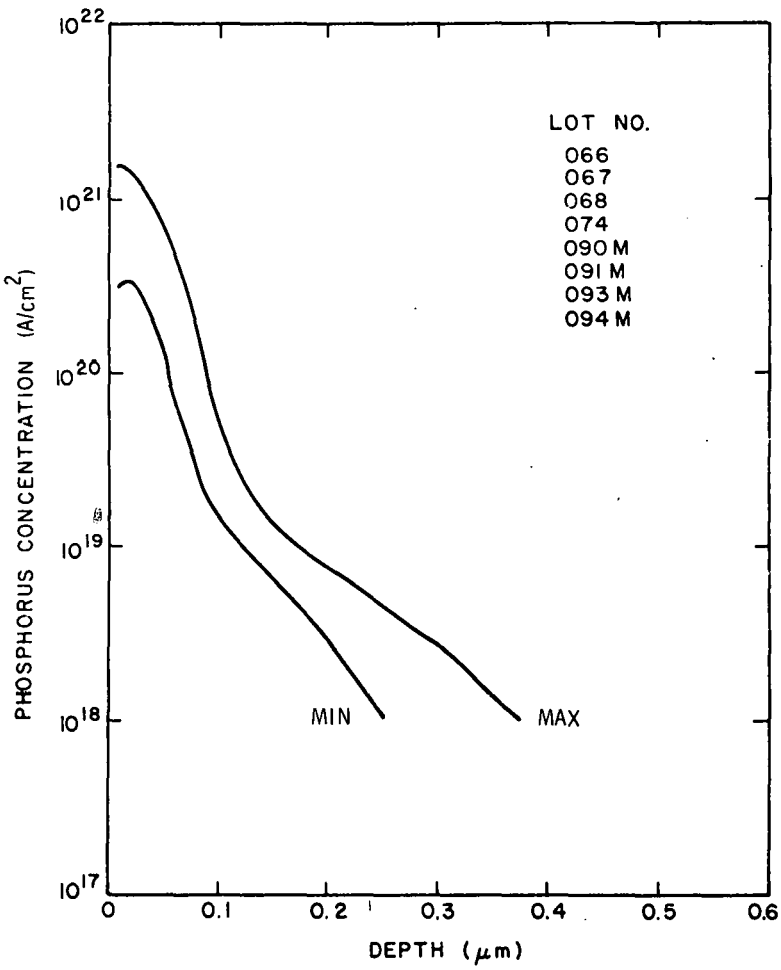


Figure 41. Range of $POCl_3$-diffused phosphorus concentration profiles.

To enable determination of the extent of penetration of the metallization, samples were treated with 1:1 NH_4OH-H_2O_2 solution to dissolve the Ag film. The remaining glass frit was dissolved in ultrasonically agitated HF solution. Scanning electron microscopy was then employed to determine the degree of attack on the underlying silicon.

For example, the RCA 15 vol pct lead borosilicate sample which was fired for 2 min at 800°C on n^+-Si is shown in Fig. 42 after metal and glass removal. Figure 42(a) illustrates the typical rectangular etch pits in (100)-oriented silicon caused by glass dissolution. Viewed at a low angle, Fig. 42(b) shows the depth of attack to be approximately 0.5 μm, essentially the entire n-layer thickness. From this observation, it is clear that such extensive dissolution would impair, if not preclude, device performance. Consequently, temperatures below 800°C must be considered as an upper boundary for solar-cell metallizing with this shallow junction design and glass composition.

8. Application of Screen-Printing Process to Solar Cells

a. Application to 3-in.-Diameter Cells with Diffused Junctions - Initial experiments were conducted with 3-in.-diameter solar-cell wafers having n^+ junction depths of ∿0.5 μm and sheet resistance of ∿30 Ω/□. These junctions were formed by a $POCl_3$ diffusion at 850°C for 60 min into p-type, 1- to 2-Ω-cm Czochralski wafers. The lots were split and printed on the sun-side with three different silver-based inks: Thick Film Systems TFS 3347, RCA-Metz type C, and Englehard E-422E. The backs of all samples were printed with Englehard E-422F Ag ink containing 3 to 4% aluminum.

The firing tests were conducted using two Argus International* #705 infrared lamp heaters. The samples were placed one at a time in a horizontal plane on a stainless-steel grid belt and fired simultaneously from both sides. A thermocouple placed on the sun-side of the wafers indicated that a temperature of 775 to 800°C was achieved in 30 s. Experiments were conducted at firing times of 1/2, 1, 1-1/2, 2, and 3 min.

The results as a function of the firing time are shown in Table 25. Good results were obtained at all firing times as indicated by the maximum

*Argus International, Hopewell, NJ.

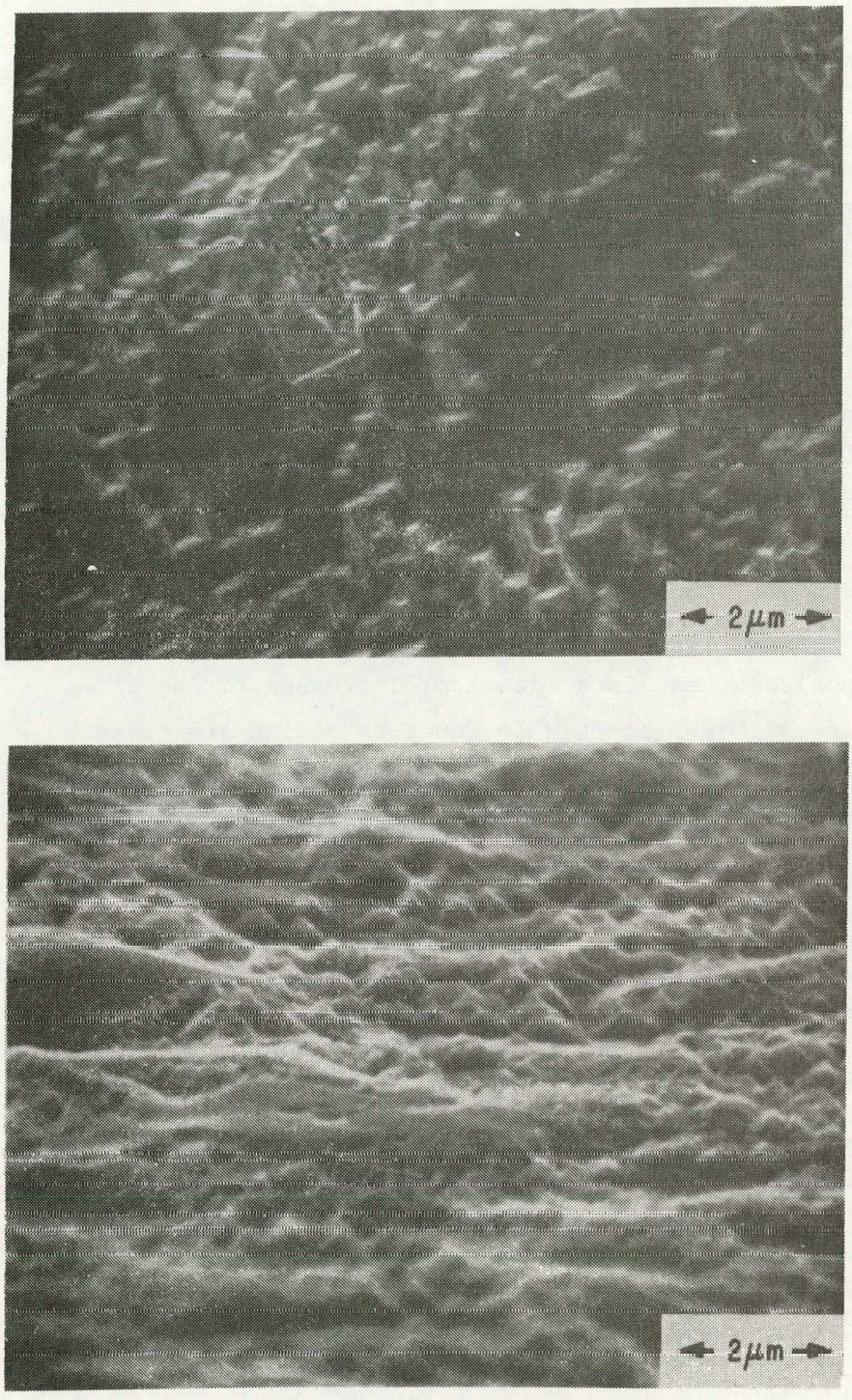


Figure 42. SEMs of n^+-silicon surface after dissolution of Ag and glass film. Film contained 15 vol pct lead borosilicate glass and was fired for 2 min at 800°C.

TABLE 25. RESULTS OF INFRARED LAMP FIRING AS A FUNCTION OF FIRING TIME

Firing Time (min)	No. of Samples	AM-1 Parameters J_{sc}* (mA/cm^2)	V_{oc} (mV)	FF -	FF_{max} -	η** (%)	η_{max}
1/2	8	20.7	577	0.662	0.731	7.9	8.9
1	9	20.5	582	0.697	0.728	8.3	9.0
1-1/2	10	20.2	577	0.679	0.713	7.9	8.8
2	8	19.8	574	0.697	0.727	7.9	8.7
3	5	20.0	572	0.703	0.717	8.0	8.6

*Cell area = 39 cm^2
**No AR coating

values shown in Table 25. However, wider variations in parameters were measured for the 30-s firing time, and some degradation in open-circuit voltage and short-circuit current is evident for increased firing time.

The solar-cell parameters as a function of ink are given in Table 26. It can be seen that the RCA type C ink yielded the best overall cell parameters with Thick Film Systems TFS 3347 a close second. The cells printed with Englehard ink E-422E generally had the lowest fill factors, caused primarily by excessive series resistance.

TABLE 26. SUMMARY OF INFRARED LAMP-FIRED SOLAR CELLS AS A FUNCTION OF INK

Ink		Firing Time	AM-1 Parameters J_{sc}*	V_{oc}	FF	FF_{max}	η	
Sun	Back	(min)	(mA/cm^2)	(mV)	-	-	(%)	η_{max}
TFS 3347	E-422F	1-3	19.8	577	0.690	0.713	8.0	8.8
RCA Type C	E-422F	1-3	20.4	582	0.700	0.717	8.2	8.8
Engelhard E-422E	E-422F	1-3	20.0	572	0.680	0.703	7.8	8.3

*No AR coating

The infrared lamp method of firing is rapid and seems to offer good stability and control. The experiments described below were conducted to assess the limits of this method and to determine optimum production parameters.

We have investigated the use of infrared-lamp heaters for firing screen-printed solar cells. The sensitivity of this method was studied by examining the effect of firing time and temperature on solar-cell parameters. The cells were from our standard lots of 3-in.-diameter wafers having junctions formed by $POCl_3$ diffusion with average junction depth of 0.5 μm and sheet resistance of 30 Ω/□. Studies were made with TFS 3347 and RCA n-type inks for the front grid metallization and RCA p-type for the back of the cells.

An attempt was made to measure the temperature of the metal film during heating rather than the surface temperature of the silicon. This was accomplished by imbedding a thermocouple in a small mass of the ink fired onto the silicon surface.

Firing times of 1 to 3 min in the 600 to 800°C temperature range were studied. An example of the results obtained for 1-min firing time is shown in Fig. 43. The temperature bandwidth is reasonably wide, about 50°C for a 1/4% decrease in efficiency. As might be expected, as the firing time is increased, the temperature for peak performance and the bandwidth decreases. Also, the onset of metal "spiking" becomes more abrupt.

b. Improvement in Fill Factor by HF Dipping - We have frequently noted a low fill factor (∿0.65) with screen-printed solar cells even though they were fired under what we consider optimum conditions. These cells often exhibit expected values of short-circuit current and open-circuit voltages. It has been reported by other contractors that dipping the cells in hydrofluoric (HF) acid solutions can cause marked improvement in the fill factor, although a critical time in the solution was sometimes noted.

In our experiments, a 1% HF solution was used and we noted the following results:

(1) For screen-printed cells, an improvement in fill factor was noted in all cases. Substantial increases in fill factor were measured as shown in Fig. 44, with no degradation in other cell parameters.

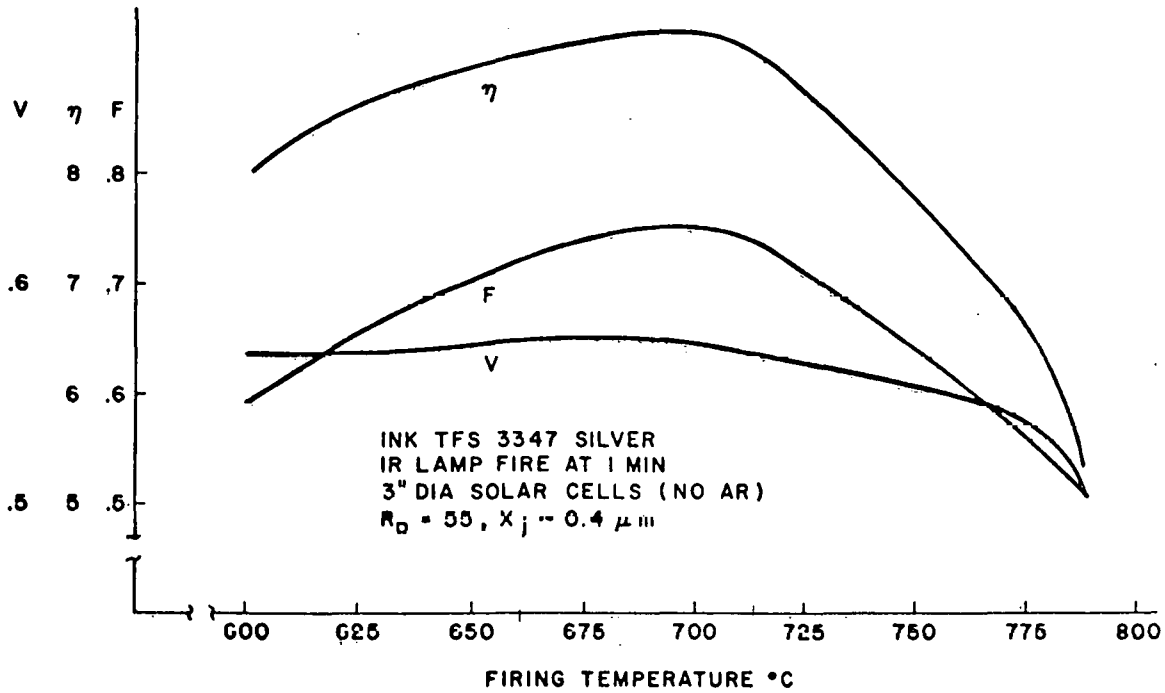


Figure 43. Results of test using infrared-lamp heater, 1-min firing time.

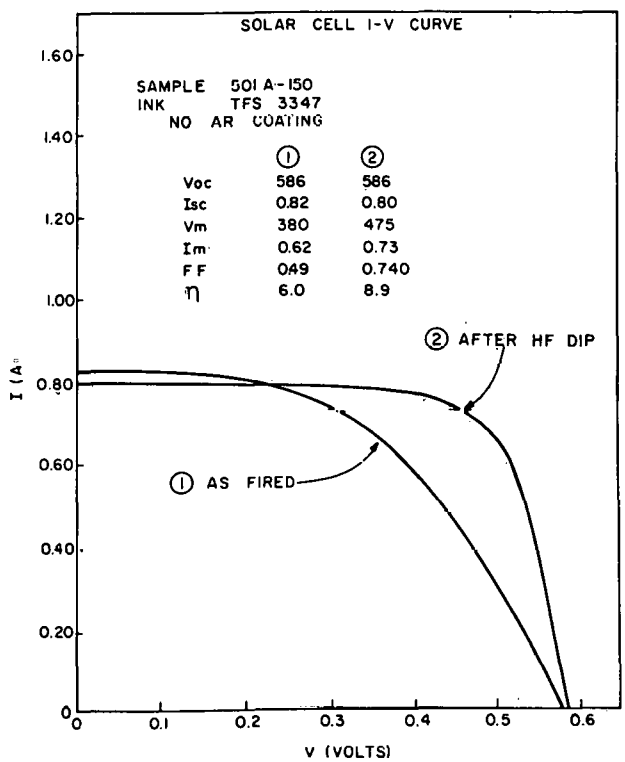


Figure 44. I-V curve produced by testing with HF dipping.

(2) No change in fill factor was measured for control cells which were metallized with conventional evaporated Ti/Pd/Ag.

(3) The time in the 1% HF solution was *not* critical. Generally, an increase in fill factor was noted for a 10-s dip and saturated after 40 s of dipping. Continuation of dipping beyond 40 s caused no apparent degradation of the cells.

At this time, we have no explanation for this effect.

In separate experiments with TFS 3347 and RCA n-type ink, the solderability and adhesion of these inks before and after a 30-s dip in 1% HF were measured. Marked improvement in solderability was measured and no change in relative bond strengths was noted.

c. Screen-Printing Applied to Ion-Implanted Solar Cells - Preliminary tests were conducted to apply screen-printing technology to cells with ion-implanted layers. Twenty-four samples were prepared, 12 for screen printing and 12 controls. The cells were fabricated with a phosphorus ^{31}P dose of 4×10^{15} A/cm^2 at 5 keV to form the n^+/p junction and the back p^+ contact was formed by either a boron implant (^{11}B, 5×10^{15} A/cm^2 at 25 keV) or by our boron glass BSF process (described in subsection A above). Furnace annealing was used to activate the implants.

For the screen printing, TFS 3347 ink was used for both the front and back. It was felt that this ink would be adequate for the back contact since a p^+ layer is present in these samples. The screen contained the same pattern of 2- x 2-cm cells (Fig. 45) as that used photolithographically to define the contacts on the control samples. Firing was done with infrared lamps; the surface temperature was 675°C for 2 min.

After firing, the electrical output of the cells was measured under AM-1 illumination. The fill factors were between 0.4 and 0.6. The 1% HF dipping procedure described above was then applied. The cells were remeasured and a summary of the average AM-1 cell parameters obtained along with those for the controls is given in Table 27. Clearly, the HF dip caused a marked improvement in the fill factor.

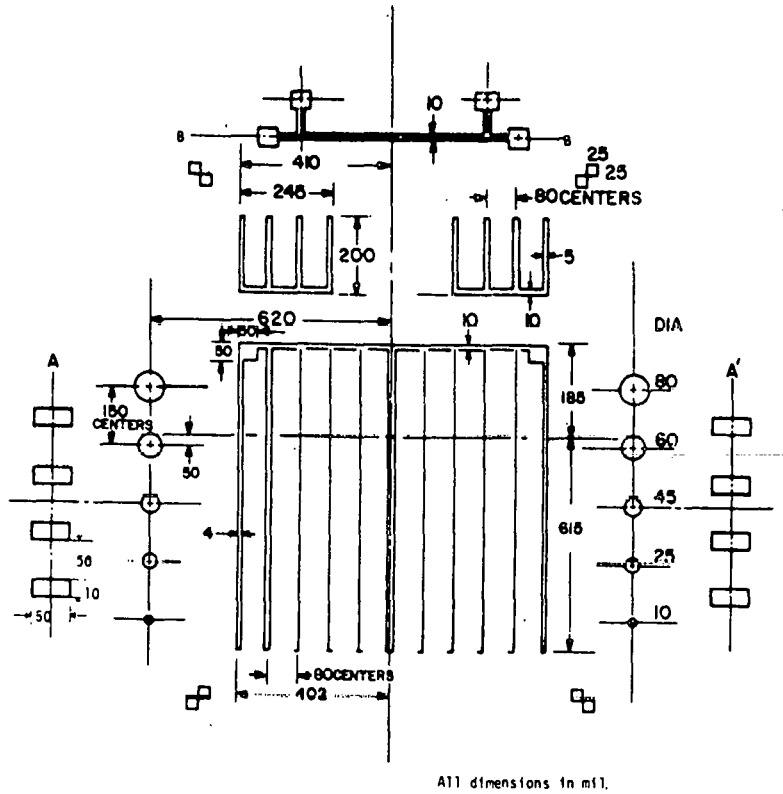


Figure 45. Solar-cell mask design including diagnostic cells.

TABLE 27. SUMMARY OF AVERAGE AM-1 CELL PARAMETERS FOR ION-IMPLANTED SOLAR CELLS WITH SCREEN-PRINTED METALLIZATION

Type of Sample	J_{sc} (mA/cm^2)	V_{oc} (mV)	FF -	η* (%)
Evap Ti/Ag; Boron-Glass BSF	20.3	555	0.785	8.8
Screen-Printed Ag**; Boron-Glass BSF	19.0	540	0.737	7.6
Evap Ti/Ag; Three-Step	22.1	582	0.777	10.0
Screen-Printed Ag**; Three-Step	20.9	550	0.750	8.6

*No AR coating
**TFS 3347 both sides

9. Discussion and Conclusions

A screen-printable lead borosilicate-doped Ag metallization ink was developed specifically for solar cells. Material constituents were characterized and the electrical conductivity, solderability, and adhesion explored as a function of ink composition and firing conditions. As a result of these evaluations, optimum material and process parameters were established for the screen printed and fired metallizing of solar cells.

It was found that at least one commercial ink, TFS 3347, and the RCA n-type and p-type inks are suitable for forming thick-film screen-printed metallizations on 3-in.-diameter solar cells. Commercially available screen printers can be used to obtain high throughputs with good yield and the use of standard screens result in acceptable line definition for collector-grid patterns. Infrared lamps used for firing the contacts were found to provide a rapid and controllable process with reasonably wide tolerance in firing temperature and time.

On the negative side, the efficiencies of solar cells fabricated with the screen-printing process described here were about 85% of the control cells made with conventional evaporated contacts. This was primarily due to lower fill factors and in some cases, lower open-circuit voltage. However, the dramatic improvement in fill factor obtained by simply rinsing the cells in a 1% HF solution is an encouragement that higher efficiencies can be obtained by improved processing techniques.

Future effort should be focused on enhancement of solar-cell efficiency via HF rinsing techniques and the development of non-noble metallizations for even lower cost solutions to the metallizing question.

C. SPRAY-ON ANTIREFLECTION COATING PROCESS

1. Background

Process development and optimization studies for low-cost spray deposition of single-layer antireflection (AR) coatings for metallized single-crystal silicon solar cells were conducted to examine: (1) effects of spray deposition machine parameters, (2) metallization bondability after AR coating, (3) cell electrical performance as a function of AR coating type and thickness, (4) heat treatment effects, and (5) characterization of AR films.

2. Spray-On AR Process Studies and Optimization

a. Effects of Spray Deposition Machine Parameters - The automatic spray system used in our work is a Zicon Series 900 autocoater.* This machine is a laboratory version of the much larger Series 11000 in-line unit which we have recommended for mass production applications. The spraying is conducted in a Class 100 laminar downdraft clean booth supplied with HEPA-filtered air. A reciprocating spray gun traverses perpendicularly to the substrate cells, which are moved by an incremental advancing transport system. The machine operates automatically over a wide range of programmed cycles adjustable by front-panel controls. At least fourteen factors can be varied to provide the desired film thickness. These variables include (1) source solution delivery pressure, (2) automization spray pressure, (3) gun-to-substrate distance, (4) propellant gas, (5) orifice size, (6) needle size, (7) spreader, (8) inserts, (9) solution flow rate, (10) number of spray guns, (11) spray gun traverse speed, (12) substrate advance rate, (13) source solution composition and reactant concentration, and (14) post-deposition heat treatments.

The first three variables are most easily manipulated for controlling film thickness with a given source solution. Three settings for each of these variables were selected to test their effects over the film thickness range of interest. All other factors were held fixed at settings we considered near optimal. The propellant gas was nitrogen, the orifice size was 0.31 mm (12 mil), and a single spray gun was used. The RCA I titanium isopropoxide-based coating solution was used with polished silicon wafers as the substrate. The results are summarized in Table 28 and are graphically presented in Figs. 46 to 48. All three graphs exhibit a slight curvature over the narrow test range of practical interest to us. The film thickness increases with increasing source solution delivery pressure, with decreasing atomization spray pressure, and with decreasing gun-to-substrate distance. The uniformity of the AR film over the 7.5-cm-diameter test wafers was excellent throughout, demonstrating that any of the three machine variables can be used to fine-tune the thickness with good uniformity.

*Zicon Corporation, Mount Vernon, NY.

TABLE 28. AR FILM THICKNESS AS A FUNCTION OF THREE MACHINE VARIABLES

Source Liquid Delivery Pressure (kPa)	(in. H_2O)	Spray Atomization Pressure (kPa)*	(psig)	Spray-Gun-to-Substrate Distance (cm)	(in.)	Film Thickness** (Å)
4.98	20	172	25	14.0	5.5	560
7.47	30	172	25	14.0	5.5	750
9.96	40	172	25	14.0	5.5	840
7.47	30	138	20	16.5	6.5	680
7.47	30	172	25	16.5	6.5	640
7.47	30	207	30	16.5	6.5	550
7.47	30	172	25	11.4	4.5	740
7.47	30	172	25	14.0	5.5	680
7.47	30	172	25	16.5	6.5	640

*Referring to the gauge pressure.

**TiO_2 from RCA I titanium isopropoxide-based source liquid after post-deposition heat treatments for 30 s each at 70, 200, and 400°C. Surface temperatures were measured accurately with a calibrated thermocouple thermometer (Digital-Heat Prober by W. Wahl Corp.).

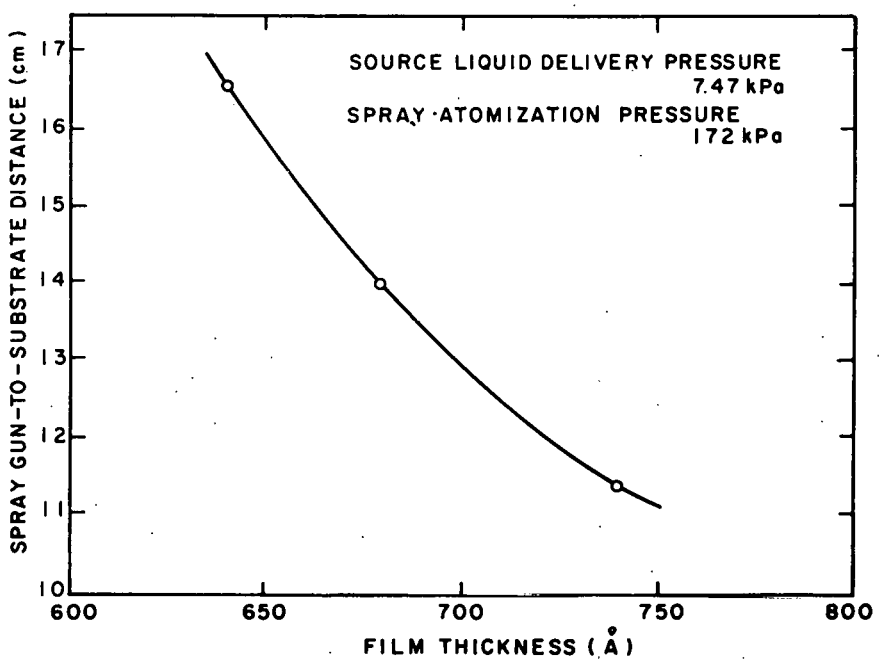


Figure 46. Effect of spray-gun-to-substrate distance as a function of film thickness.

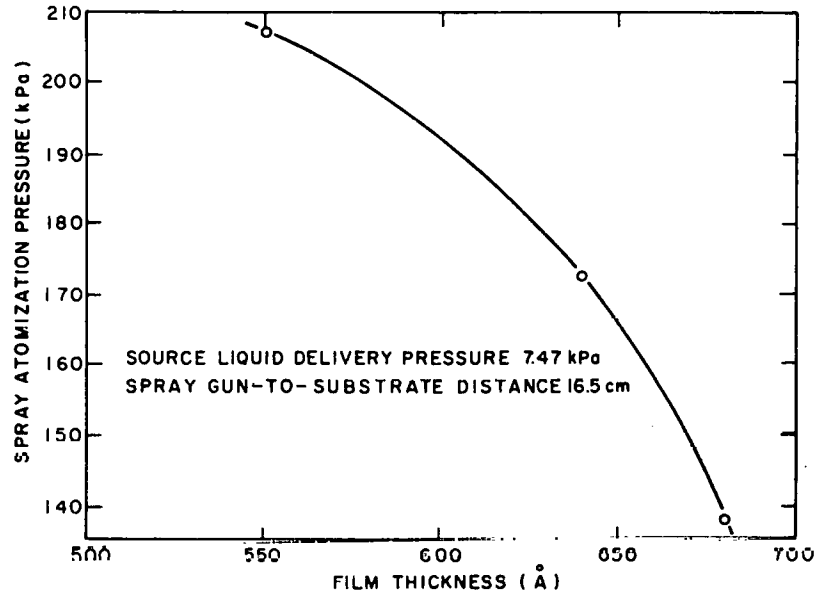


Figure 47. Effect of spray atomization pressure as a function of film thickness.

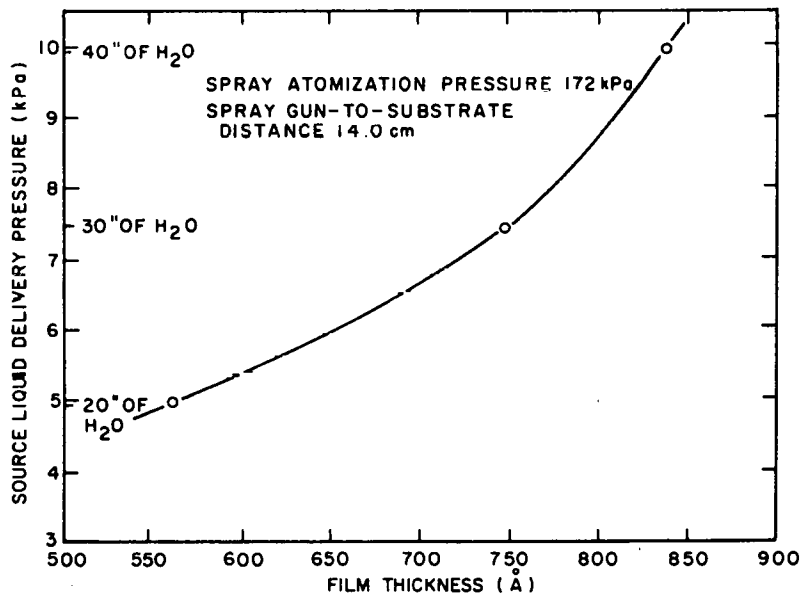


Figure 48. Effect of source liquid delivery pressure as a function of film thickness.

b. Metallization Bondability After AR Coating - The surface of the metallization grid collector pad must be free of AR coating in order to permit effective bonding of cell-to-cell interconnects. The simplest technique, suitable for laboratory applications, is masking the pad with a special solvent resistive polyethylene pressure tape with acrylic adhesive prior to spraying.* The tape tab is readily peeled off after coating but before heat treatments, leaving a clean and bondable surface.

Mechanical and chemical techniques can be used for automated high-speed processing. Selective mechanical removal of the AR coating can be accomplished by momentary application of an automatic ultrasonic vibrating or buffing tool combined with vacuum suction to remove the debris. Alternatively, since solder connection techniques are used which require fluxing of the bonding area, a flux composition could be formulated which contains a fluoride capable of selectively dissolving the thin AR coating. Rinsing with a jet of deionized water would prevent any subsequent metal corrosion.

c. Cell Electrical Performance as a Function of AR Coating Type and Thickness - We have shown previously [19] that the solar-cell conversion efficiency is not markedly affected by the AR coating thickness in the range of 600 to 800 Å. Additional studies were performed to extend the film thickness range and to compare RCA cells having screen-printed silver metallization with commercial OCLI cells** having conventional evaporated Ti/Pd/Ag metallization. The conversion efficiency of the AR-coated OCLI cells was determined by I-V measurements under a standardized light source. The AR coating, consisting of SiO_x, was then stripped by etching briefly in buffered HF solution, followed by rinsing with deionized water, and spin drying. The cells were remeasured, AR recoated by us, and again measured. The ratio of J_{sc} measured after AR coating over J_{sc} of the bare cell before coating is taken as a convenient approximation of the change in conversion efficiency under standardized irradiation conditions.

19. R. V. D'Aiello, *Automated Array Assembly, Phase II*, Quarterly Report No. 4, prepared under Contract No. 954868 for Jet Propulsion Laboratory, October 1978.

*Tape No. 480, 3M Company, St. Paul, MN.

**Cells manufactured by Optical Coating Labs, Inc., Santa Clara, CA.

The source preparations for depositing the AR coatings were RCA I titanium isopropoxide-based composition and commercial Emulsitone "Titaniumsilicafilm C" solution. The RCA II titanium ethoxide-based alternative preparation was not included since it offers no advantages over RCA I, has a shorter shelf life, and is more expensive. Formulation of the source solutions, application by centrifugal spinning, heat treatment of the films, and ellipsometric measurements of refractive index and film thickness were performed as described previously [19]. Polished single-crystal silicon wafers were used as control substrates for the optical measurements.

The results for RCA cells with 10- to 18-μm-thick screen-printed silver metallization, AR coated with RCA I source solution, are summarized in Table 29. The effect of TiO_2 film thickness on the increase in current density ratio Γ (J_{sc} after coating/J_{sc} before coating) is shown graphically in Fig. 49. A broad maximum of Γ = 1.39 is attained with a film thickness of 700 Å. Film thickness measurements were done ellipsometrically on the cells as well as on analogously AR-coated polished silicon test wafers. The films on cells gave unreliable thickness readings that averaged 22% more, apparently due to the surface roughness of sawed and chemically etched silicon surfaces. The accurate film thicknesses measured on the smooth test wafers are considered more representative and were used for plotting the graphs in Figs. 49 and 50.

Stylus profilometric traces of typical RCA cell surfaces showed silicon roughness peaks of 0.4 μm at an average frequency of 9 peaks/mm horizontal distance, rendering step-height measurements of the thin AR film also unreliable. The ellipsometrically determined index of refraction averaged 2.15 for the test wafers and 2.18 for the cells. The cell conversion efficiency (η) averaged 8.6% before and 11.5% after TiO_2 coating.

The results we obtained for OCLI cells with 2.7-μm-thick vacuum-evaporated Ti/Pd/Ag metallization are presented in Table 30 and in Fig. 50. The effectiveness of the OCLI sputter-deposited SiO_x AR coating was determined by measuring the current density before and after chemical stripping of the coating. As indicated in Fig. 50, the ratio increase (Γ) averaged 1.45 for a nominal ellipsometric film thickness range of 820 to 870 Å. No test wafers with SiO_x were available for comparison. The cell conversion efficiency averaged 7.6% for bare cells and 11.0% for SiO_x coated cells.

TABLE 29. INCREASE IN CELL EFFICIENCY AS A FUNCTION OF TiO_2 FILM THICKNESS FOR CELLS WITH SCREEN-PRINTED METALLIZATION

Source Liquid (type)	Solar Cell[1] (Å)	Film Thickness[2] (Å)	Refractive Index[2] (n)	Current Density Increase[3] (Γ)	Efficiency[4] Before Coating (%)	Efficiency[4] After Coating (%)
RCA I[5]	501A-110	903	2.141	1.26	8.7	10.9
	501A-109	801	2.150	1.29	8.5	10.8
	501A-107	697	2.137	1.39	8.8	12.1
	501A-105	639	2.137	1.36	8.5	11.7
	501A-86	539	2.182	1.35	8.6	11.6
	501A-85	483	2.150	1.36	8.6	11.8

1. Screen-printed Ag metallization, 7.5-cm-diam RCA cells. Metal thickness: 8.0 μm.
2. Ellipsometric measurement on polished silicon test wafer; Hg light at λ = 5461 Å.
3. Ratio of J_{sc} after/before coating.
4. AM-1 simulation ELH lamp at 100 mW/cm^2.
5. Titanium isopropoxide-based, yielding TiO_2; post-deposition heat treatments 30 s each at 70, 200, and 400°C.

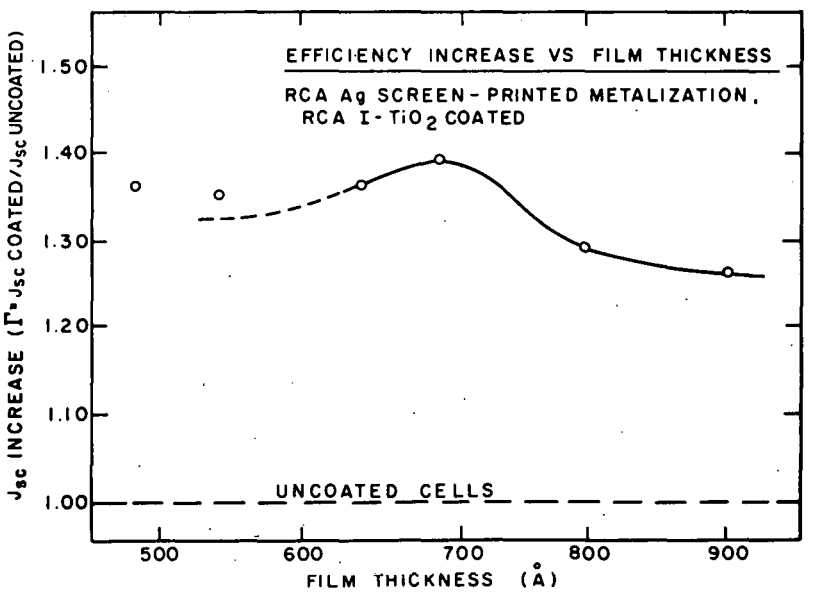


Figure 49. Electrical performance as a function of film thickness, 8-μm-thick vacuum-evaporated Ti/Pd/Ag metallization.

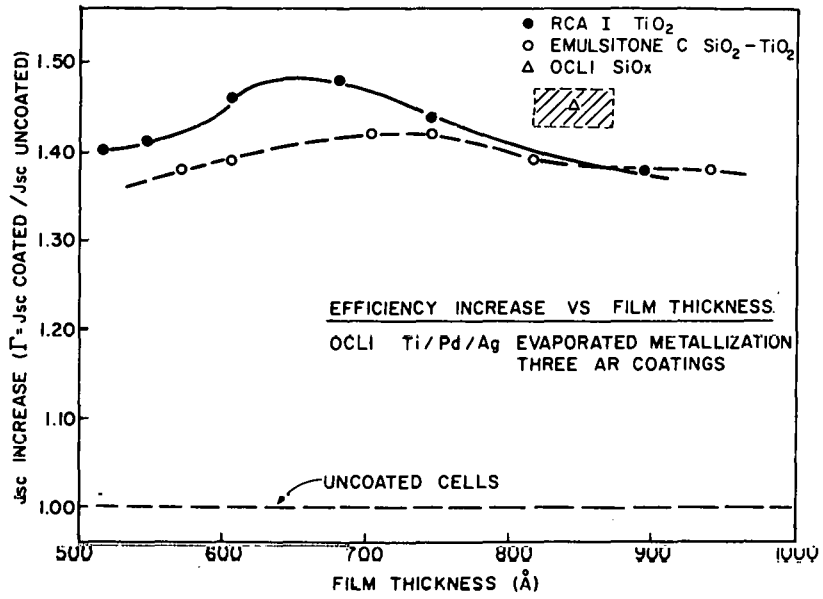


Figure 50. Electrical performance as a function of film thickness, 2.7-μm-thick vacuum-evaporated Ti/Pd/Ag metallization.

Recoating the cells with RCA I TiO_2 led to a peak increase of Γ of at least 1.48, centered between 625- and 675-Å film thickness. Recoating with Emulsitone TiO_2-SiO_2 led to a Γ maximum of 1.42 for a film thickness between 700 and 740 Å. The film thicknesses stated were obtained from ellipsometrically measured silicon test wafers. Measurements on cells again deviated, but in the opposite direction than observed for RCA cells: OCLI cells averaged 17% *less* than the test wafers. Stylus profilometery indicated a cell surface roughness of typically 0.6 μm with a frequency averaging 14 peaks/mm horizontal distance.

Ellipsometric measurements of the refractive index of the AR films also gave differences between test wafer substrates and OCLI cells: RCA I TiO_2 averaged an index of 2.20 on test wafers and "2.37" on cells; Emulsitone C TiO_2-SiO_2 was 1.94 on test wafers and "2.26" on cells; OCLI SiO_x measured "1.81" on cells, which corresponds to 1.55 to 1.69 on test wafers if corrected on the basis of the TiO_2-SiO_2 and the TiO_2 differences noted.

The OCLI cell conversion efficiency averaged 7.6% without AR coating, 10.8% with RCA I TiO_2, and 11.0% with OCLI SiO_x. The values for Emulsitone TiO_2-SiO_2 are somewhat lower, averaging 10.3%.

TABLE 30. INCREASE IN CELL EFFICIENCY AS A FUNCTION OF AR FILM THICKNESS FOR CELLS WITH EVAPORATED METALLIZATION

Source Liquid (type)	Solar Cell[1] (No.)	Film Thickness[2] (Å)	Refractive Index[2] (n)	Current Density Incr.[3] (Γ)	Efficiency[4] Before Coating (%)	Efficiency[4] After Coating (%)
RCA I[5]	10	895	2.220	1.38	7.6	10.6
	11	745	2.204	1.44	7.6	10.8
	12	677	2.193	1.48	7.9	11.4
	9	605	2.218	1.46	7.4	10.8
	7	545	2.187	1.41	7.8	11.1
	8	515	2.165	1.40	7.4	10.3
Emulsitone C[6]	1	940	1.973	1.38	7.3	10.2
	2	816	1.950	1.39	7.6	10.6
	3	745	1.940	1.42	7.4	10.0
	4	702	1.929	1.42	7.8	10.9
	6	604	1.933	1.39	7.4	9.9
	5	572	1.916	1.38	7.6	10.3

1. Vacuum-evaporated Ti/Pd/Ag metallization, 7.5-cm-diam OCLI cells stripped of their AR coating. Profilometrically measured metal thickness is 2.7 μm.
2. Ellipsometric measurement on polished silicon test wafer; Hg light at λ = 5461 Å.
3. Ratio of J_{sc} after/before recoating.
4. AM-1 simulation ELH lamp at 100 mW/cm^2.
5. Titanium isopropoxide-based, yielding TiO_2; post-deposition heat treatments 30 s each at 70, 200, and 400°C.
6. Emulsitone "Titaniumsilicafilm C" yielding $SiO_2 \cdot TiO_2$; post-deposition heat treatments 30 s each at 70, 200, and 400°C.

Several conclusions can be derived from these results:

(1) Comparison of the effectiveness of TiO_2, TiO_2-SiO_2, and SiO_x AR coatings on commercial thin-film metallized cells showed that TiO_2 from RCA I solution is superior to both Emulsitone TiO_2-SiO_2 and OCLI SiO_x. Maximal Γ values are 1.48+ at 625 to 675 Å, 1.42 at 700 to 740 Å, and 1.45 at 820 to 870 Å, respectively.

(2) Screen-print metallized RCA cells with RCA I TiO_2 coating exhibited a maximal Γ value of 1.39 at 700 Å. This apparently lower value is due to the higher initial cell conversion efficiency of RCA cells

(8.6%) than that of OCLI cells (7.6%). However, the final conversion efficiency after coating increased to 11.5% for RCA cells, but to only 10.8% for OCLI cells.

(3) The conversion efficiency for OCLI cells recoated with RCA I TiO_2 exhibited a maximum efficiency of 11.4% for a film thickness of 700 Å.

(4) The conversion efficiency for OCLI cells with their more expensively produced SiO_x coating averaged 10.9% for the presumably optimal thickness of these films. A greater effectiveness should really be expected for a physically vapor-deposited AR coating. Reduced scattering losses result from the more uniform coverage attainable, especially in comparison to the centrifugal spinning over thick-film metallized cells as used in this analytical study.

(5) The new results we obtained again emphasize the relative noncriticality of the AR film thickness. For example, the cell efficiency of RCA I TiO_2 recoated OCLI cells, averaged over the entire tested film thickness range from 500 to 900 Å, is a remarkable 10.8% (without indications of drastic decreases beyond this range), as compared to 11.4% for the maximum at about 700 Å.

(6) Ellipsometric measurements of thickness and refractive index of AR coatings on microscopically nonplanar cell surfaces are not reliable due to optical causes. Control measurements must be performed on polished silicon test wafers and correlated with cell values as was done in our present work. Alternatively, a macroscopic interferometric reflection technique of a relatively large area of the silicon cell surface may be more appropriate for direct in-line process control applications.

d. Heat-Treatment Effects and Characterization of AR Films - Effects of additional heat treatments on cell efficiency and AR film properties are being examined to ascertain whether further improvements could be achieved. The cells and silicon test wafers described in the subsection above were used for this purpose. As noted, these samples had been heat-treated after film deposition by exposure in room air to 70°C on a hot plate for 0.5 min, followed by heating at 200°C for 0.5 min, and finally by heating at 400°C for 0.5 min. Additional heating was done at 400°C for times up to 15 min,

followed by cell measurements and film analyses. The results of such extended heat treatment on coated and uncoated cells are given in Table 31. The data show that (1) the antireflective property of the spray-on film is unaffected by the extended heat treatment and (2) degradation in cell performance is confined to a reduction in the fill factor which begins after about 3 min of heat treatment at 400°C and is more severe for the uncoated cells.

TABLE 31. EFFECT OF HEAT TREATMENT ON SPRAY AR COATED AND UNCOATED CELLS

Cell No.	Spray AR	Time at 400°C (min)	I_{SO} (mA)	I_{ST} (mA)	Comments
115m - 1	Yes	1.0	1100	1091	No significant change
115m - 2	Yes	2.0	1110	1093	No significant change
115m - 3	Yes	3.0	1100	1095	No significant change
115m - 4	Yes	5.0	1090	1086	Small reduction in FF 0.760 → 0.737
115m - 5	Yes	15.0	1130	1123	Seriously degraded 0.761 → 0.600
115m - 6	No	2.0	900	900	No change
115m - 7	No	5.0	895	890	Fill factor severely degraded 0.755 → 0.591
115m - 8	No	15.0	895	895	Fill factor severely degraded 0.751 → 0.570

SECTION IV

DOUBLE-GLASS PANEL LAMINATION AND CELL INTERCONNECT

A. INTRODUCTION

The panel lamination and interconnect research studies with which this program has been concerned have been centered upon the lamination of cells between two sheets of glass. This approach was selected because of our concern for the twenty-year longevity requirements of the panelization processes required for achievement of the lifetime cost effective goals of the LSA Program. The early phases of our program dealt with the development of successful double-glass solar photovoltaic panels. In parallel with our use of polyvinyl butyral (PVB) an effort was made to use an acrylic monomer. This effort was not promising and was terminated to permit more concentration on the PVB double-glass lamination development. Later in the program RCA determined that a major problem with double-glass PVB lamination was the need to develop a process technique capable of achieving the program cost goals. To do this we investigated a two-step lamination technology which we deemed more appropriate to low-cost manufacture.

An ancillary investigation was pursued to develop appropriate cell interconnect techniques. Initially both parallel gap welding and reflow soldering were investigated. In the later stages of this program it was found necessary to eliminate hand soldering operations in order to properly continue double-glass lamination experiments without panel cracking caused by solder spikes. A novel radiant reflow soldering technique was developed in which an entire interconnected array lay-up was soldered at once. This technique is particularly suited to fully redundant series-parallel array lay-up configurations.

B. PANEL LAMINATION

1. Acrylic Casting Lamination

Acrylic casting as an alternative to PVB laminating was explored. Methyl methacrylate-butyl acrylate resin is an available and inexpensive material and has excellent weathering properties. At low temperatures, a combination of methyl methacrylate and butyl acrylate between glass plates provides a relatively soft inner core that is expected to survive temperature extremes of -40 to +90°C.

The liquid monomer is low viscosity and readily wets glass and silicon. This allows filling of the volume between glass plates - including the cells - with exclusion of all air. When cured, the acrylic adheres to the glass as well as PVB does. However, the monomer shrinks about 20% in volume during cure; and therefore, a reservoir must be provided for makeup into the panel. Experiments were run with varying mixtures of butyl/methyl methacrylate monomers, catalysts, and curing temperatures. Best results were obtained with a 60% butyl acrylate/methyl methacrylate mix, using 67% t-butyl-peroculate catalyst, at approximately 65 to 75°C oven cure. The primary difficulty encountered was the appearance of bubbles in the cured polymerized mix. Panels filled under atmospheric pressure with degassed monomer always resulted in bubbles being formed in the polymer. Pouring under vacuum conditions improved the results.

Panels were also prone to glass fracture around the cells during thermal cycling from +100 to -30°C. This is due to differential expansion of the acrylic coupled with the prestress induced by the differential polymerization shrinkage at the cell edge and the inability of the acrylic to absorb and redistribute these stresses. The higher the cure temperature, the greater the size and number of bubbles formed during the thermal cycling.

To prevent glass fracture, a monomer resulting in a polymer with a durometer very close to that of PVB is required. This softer material is able to absorb and redistribute the stresses induced during the thermal cycling and prevent stressing of the glass envelope; however, it had a definite blue haze. (See Fig. 51.) After 10 cycles of +100 to -30°C, bubbles at the perimeter of the cell enlarged and several new small bubbles appeared. However, the glass did not crack around the cell.

We concluded that the softer polymer is necessary to avoid transmitting thermally induced strains to the glass envelope. However, the penalty paid to produce a sufficiently soft polymer is the blue haze which reduced optical transmission by approximately 1%. We also concluded that the vacuum filling technique greatly reduced the formation of bubbles in the polymer and also results in shorter duration and more complete polymerization. Nonetheless, based on our experience, this process appeared to be less attractive than PVB lamination and was not pursued further.

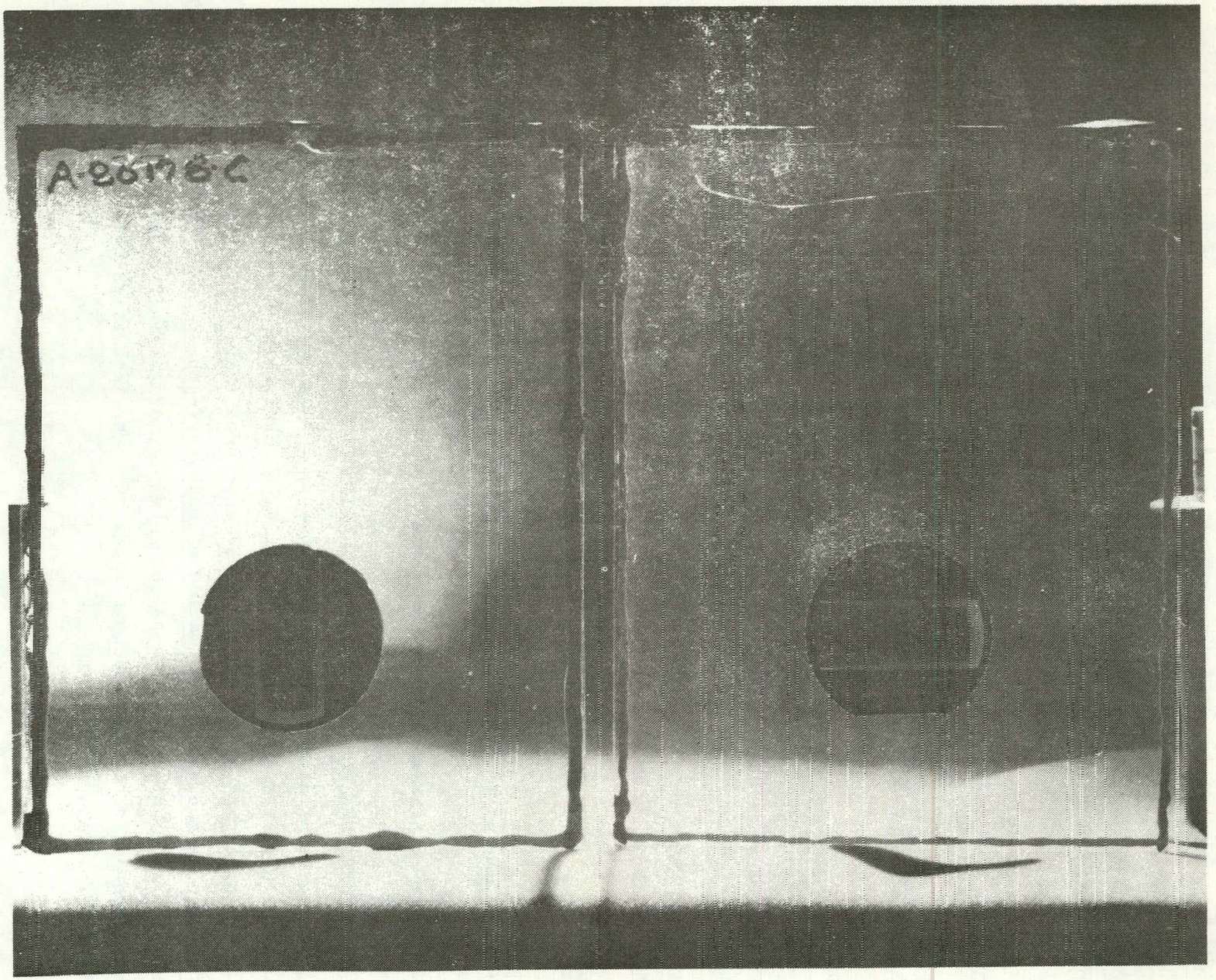


Figure 51. Comparison of optical clarity of panel as affected by composition of polymer. Panel on right is 60/40 butyl/methyl acrylic monomer mix. Panel on left is 40/60 butyl/methyl mix.

2. PVB Lamination - Pinch Roller Method

Initial work began using the pinch roller technique practiced in the current manufacture of safety glass.

This technique consists of rolling and heating the glass/PVB/cell/PVB/glass sandwich to expel as much air as possible, as well to seal the edges. The sandwich is then autoclaved at 275°F and 150 psi, which completes the flow of the PVB around the cells and drives all remaining air into solution with the PVB.

Because an extended cell array has triangular voids between cells, the PVB must extrude from the cell face into the void at some time during the process. Ideally, most of the flow should take place during the initial rolling/heating sequence, so that a minimum of air remains for the autoclaving. Sufficient flow must be obtained to seal the edges of the sandwich; otherwise, no pressure differential can be produced on the autoclave.

With the vendor's production line set for a standard process, it appeared that the temperature was too low to allow flow of PVB at low roll pressures. At higher roll pressures, the cells and/or glass cracked. Better flow would have occurred for thick PVB (0.030 in. each side), but such a product would have been uneconomical due to PVB cost. Our target is 0.030 in. of PVB total, but it was not possible to laminate by the roll process.

3. Vacuum Bag - Autoclave Method

We investigated another PVB lamination technique which is used in the manufacture of curved windshields, bullet-proof glass, and some speciality items.

It was clearly established that a temperature of 230°F or above is necessary to provide flow and extrusion of the PVB across the cell face and into the void between the cells. At 230°F the PVB is soft, but substantial pressure is necessary. At 275°F, the PVB flows readily with moderate pressure.

Successful lamination requires a minimum of air between the layers of glass, PVB, and silicon cells. Small amounts of residual air are dissolved into the PVB by high hydrostatic pressure (~150 psi) and temperature (275°F) over a period of 30 to 60 min. If too much air is entrapped between the cells, however, it will not dissolve, and bubbles remain. This will cause delamination later in the life of the panel. Therefore, it is necessary to define a process

that first applies a partial vacuum to the lay-up (consisting of glass/PVB/cell/PVB/glass), then applies a low hydrostatic pressure on the surface of the glass plates together with moderate temperature (obtaining partial flow of PVB), and then the full hydrostatic pressure and temperature. The reason for the intermediate pressure/temperature schedule is to avoid sealing off the air passages as long as possible by minimizing the amount of tack and self-sealing of the two layers of PVB.

A vacuum bag, enclosing the lay-up, is used to allow simultaneous vacuum and pressure to be applied inside the laminating autoclave. This technique is well established in the safety glass industry for laminating glass sandwiches that cannot be handled by pressure rollers. The bag allows a vacuum to be maintained between the glass layers while simultaneously pressurizing the glass sheets externally.

A typical laminating schedule (not necessarily optimized) is shown in Fig. 52. Various thicknesses and manufacturers of PVB were tried. PVB thicknesses were 0.030 in. (2 layers) and 0.015 in. (2 layers). Monsanto* (ribbed surface) and DuPont** (orange peel surface) PVB were compared for effectiveness in removing air.

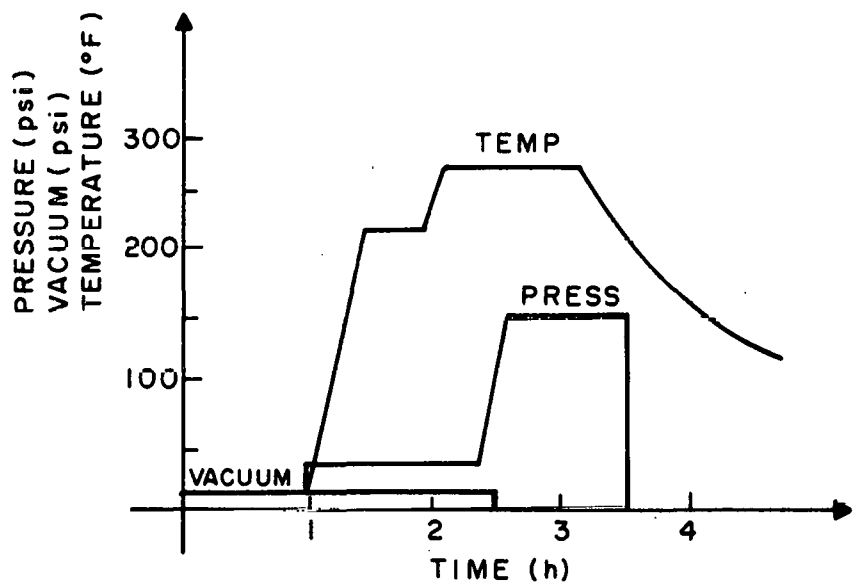


Figure 52. Lamination schedule.

*Monsanto Co., St. Peters, MO.
**du Pont de Nemours & Co., Inc., Wilmington, DE.

Even though several samples had retained bubbles, the glass itself generally remained intact. Breakage of the glass was generally caused by solder spikes and similar inclusions that cause local stress concentration.

We investigated a modification of the laminator's standard production process to determine if we could reduce the possibility of cell fracture and also reduce the duration of the autoclaving process. The duration of the autoclaving is proportional to the amount (mass) of air remaining after the initial flow of the PVB. The laminator's standard process consists of drawing down a vacuum to 27-in. Hg, heating the PVB to 107°F (partially softened), and applying 50-psig pressure. This process is optimum for laminations that do not contain inclusions such as solar cells. We demonstrated a schedule, for the initial phase of the laminating process, consisting of high vacuum, low laminating pressure, and high softening temperature that is more appropriate for laminating solar cells. By evacuating to a pressure of 5-mm Hg during the initial stage of the PVB flow, the subsequent time required to dissolve residual air by autoclaving was greatly reduced. This is so because although the volume of residual air is the same as in the standard process (absolute pressure = 76 mm Hg), the mass is reduced by a factor of 15. The lower viscosity of the hotter PVB allows flow to take place under less pressure, lessening the occurrence of cell fracture.

To illustrate the effectiveness of this modified laminating process, a small 9-cell array was laminated between two sheets of 1/8-in.-thick float glass and two sheets of 15-mil-thick PVB using 21-mil-thick (versus the standard 15 mil) 3-in.-diameter cells. Two 0.25-in.-thick glass pressing plates are employed to prevent deflecting the glass at the edges of the panel. The first stage of the lamination was done in a vacuum bag maintained at an absolute pressure of 5-mm Hg. The vacuum was drawn down for 1 hour prior to heating to 140°C. The heat- and vacuum-induced laminating pressure of 14.6 psi was maintained overnight. Then the heat was turned off and the vacuum maintained for another hour during the cooldown. The PVB flowed completely around all cells with only a few rarefied bubbles remaining. The laminate was then autoclaved at 140°C and 150-psig hydrostatic pressure in a vacuum bag. The resulting laminate was totally bubble-free.

Interestingly, due to the long duration of the lamination (>14 h) and slight inclination of the panel in the oven (<15°) the array of cells "slid" about 1/2 in. out of bottom of the panel, which illustrates the low viscosity

of the PVB at 140°C. Also, a considerable amount of PVB extruded out of the sandwich at the edges, resulting in a thinner layer of PVB between the glass sheets than if it were contained by an edge seal.

These experiments showed that under appropriate conditions, PVB will flow readily, even beyond the extent required to fill the voids between the cells. In fact, to fill the voids only, for laminating 21-mil-thick cells using two sheets of 15-mil-thick PVB, a 13.3% displacement of PVB is required. Under the same conditions, laminating 15-mil-thick cells using two sheets of 10-mil-thick PVB, only 14.3% PVB displacement is necessary. This suggested that it might be possible to laminate with 0.010-in. PVB; however, thermal stress considerations may preclude use of this thickness.

After further experiments a process schedule was developed by means of which bubble-free 4x4-ft panels were produced using a one-step lamination process. This process consists of evacuating the panel lay-up inside a vacuum bag to an absolute pressure of 2 Torr or less, for approximately 15 minutes. The panel was then heated to 290°F at ambient external pressure. At this point the autoclave was pressurized to 15 psig, and the laminate was allowed to heat to 310°F. The vacuum was then terminated, and the autoclave and bag were pressurized, maintaining a 10-psi differential between the autoclave and the bag so that the bag pressure was 140 psig and the autoclave 150 psig. The autoclaving was continued for 15 minutes and then the autoclave was cooled with pressure maintained. This resulted in a bubble-free laminate. However, the areas along the edges of the panel between the solar cells were found to be deflected. This deflection locks stresses into the glass which can cause failure in subsequent wind loading. Also, this single-step process is not as compatible with automation because the entire process must take place inside a vacuum bag which is located inside an autoclave, thereby limiting the throughput because of inefficient use of the autoclave.

Thus the development of a two-phase laminating process is critical to the automation of panel fabrication. In our automated-process concept, panels are first prelaminated in vacuum fixtures by conductive heating elements located adjacent to the glass sheet. The panels are then cooled in the vacuum fixture, removed, and then placed in batches in the autoclave for the final high-pressure bond enhancement process known as autoclaving. The heat-up rate for the prelaminated panel in the autoclave is rapid due to the enhanced heat transfer of air pressurized at 10 atmospheres. A single-step process carried out entirely

in the autoclave would require that many individual vacuum-bagged panels be placed in the autoclave at once. The panel must be heated at ambient pressure to avoid fracturing the solar cells. This constraint increases the heat-up time markedly. This factor, coupled with the multiple vacuum seals and connections which must be made, renders the single-step lamination process less desirable and more costly for automation.

It is advantageous to carry out the encapsulation in two discrete steps. First the layup is laminated using a heated vacuum bag. In the second step panels are batch autoclaved separately without a vacuum bag. A "vacuum-only" lamination process requires less complex machinery than a process that employs vacuum and pressure. For this reason, a vacuum-only lamination process was pursued. This process consists of evacuating the lay-up inside a vacuum bag to an absolute pressure of 2 Torr or less in a specified period of time. The bag is placed in an oven and heated at ambient external pressure to 290°F. The panel is then cooled with the vacuum maintained. This process results in bubbles around the edge of the panel.

The model for the formation of edge bubbles is now defined. The PVB group at Monsanto analyzed our samples of laminates that contained edge bubble defects. The analysis showed that the bubbles are composed of air. It was further concluded that the air was of external origin. The air reenters the PVB at the edge of the laminate during the cooling cycle as the PVB is contracting. The bubbles appear at the tangent point of the cell and the panel edge, where the least amount of PVB is available to supply material to the zone of uneven contraction located at the perimeter of the cell. The bubbles are predominately vented to the edge, and therefore cannot be removed by autoclaving. Although these bubbles will not cause delamination during thermal cycling because they are vented to the ambient, they could cause delamination if water entered them and was subsequently frozen.

Air can be prevented from entering the edge of the laminate by providing an impervious barrier along the edge. Aluminum tape with a pressure-sensitive adhesive was applied to the edge of the lay-up prior to laminating. A port approximately 1 in. long is placed around each power lead to allow evacuation of the interior of the panel and also to prevent short circuiting.

The process is unchanged except that the evacuation duration was arbitrarily increased from the standard 15 min to 45 min to allow for the reduced port size. Panel number 120579 was produced by this method. The panel was bubble-free prior to the autoclaving. However, the flatness of the panel was not acceptable.

Therefore, the standard 1/4-in.-thick pressing plates were replaced with plates 1/2 in. thick. This improved the flatness at the edges and especially at the unpopulated corners. Panels numbered 121479, 121379, 010380, and 010780 employed the 1/2-in.-thick plates. Both panels contained edge bubbles prior to an autoclaving but they disappeared after the autoclave operation.

Applying the aluminum tape to the edge of the panel is a tedious hand process and care must be exercised in avoiding overlaps at the corners which would cause the corners to be deflected. The tape creates a 5-mil ridge around the perimeter of the panel. To avoid uneven pressing of the edges, we included a 7-mil paper shim inside this tape perimeter.

The taped edge reduces the lateral flow of PVB out of the edge of the panel and eliminates the step of trimming excess PVB after lamination. The aluminum tape performs two important functions. First, it prevents air from reentering the PVB at the edge of the panel during the cooldown from lamination temperature, which causes the PVB to shrink. Secondly, it provides an excellent moisture barrier which will protect the PVB at the edge of the panel from (1) absorbing water which can cause delamination as well as degradation to the solar cells and (2) from losing its plasticizer as well as oxidizing, both of which will cause the PVB to become hard and brittle.

It is important that the finished laminated solar panel be flat and of equal thickness throughout the plane of the panel. Any resulting deviation in thickness translates into a prestress condition in the glass. Although the panel is not fractured after final autoclaving, it may fail during subsequent wind loading. The use of round cells creates corners on one end of the panel which are devoid of cells. This causes a problem in that these corners are easily deflected by the 15-psi laminating pressure. They are further pulled down by the volumetric contraction of the PVB as it cools down from the laminating temperature of 290°F. Also, there is a greater thickness of PVB due to the absence of cells and the thermal contraction is proportionately greater. In order to reduce the glass deflection caused by the laminating pressure the pressing plate was doubled in thickness from the standard 1/4 in. to 1/2 in. This increased the rigidity of the pressing plates by a factor of 8. This was successful in reducing the intercell deflection (Fig. 53) from a typical 2 to 4 mil to less than 1 mil. The corner deflection was also decreased from a nominal 10 mil to less than 5 mil.

The remaining deflection at the corner is primarily due to the thermal contraction of the encapsulant. To further reduce this unacceptable deflection

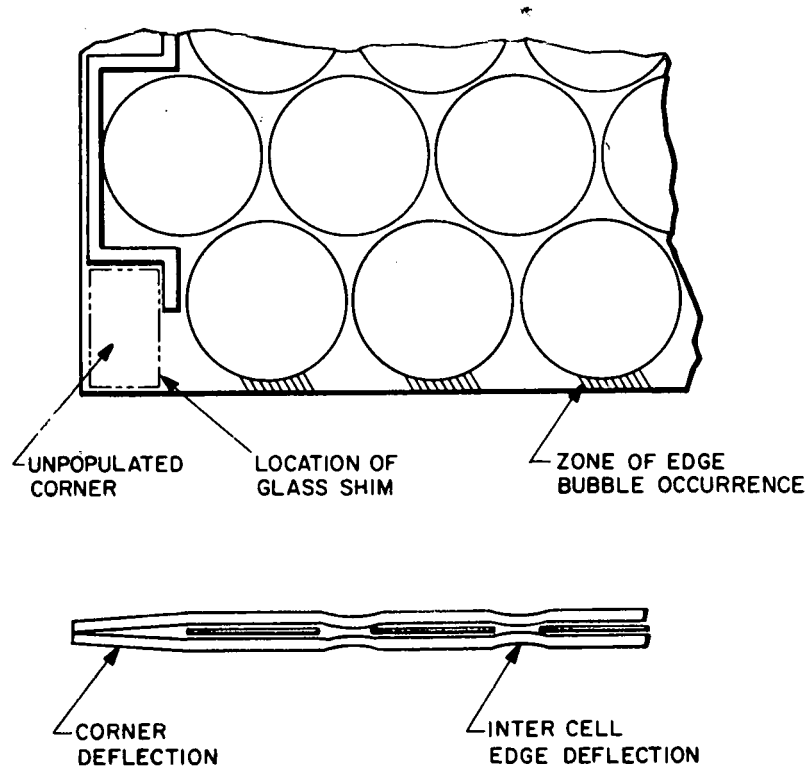


Figure 53. Intercell deflection.

we placed a 9-mil glass cover slide in each vacant corner. This successfully reduced the corner deflection to less than 4 mil.

An alternate process which used both vacuum and pressure to laminate arrays was attempted. The process employs 1/2-in.-thick pressing plates and glass shims at the corners to preserve flatness. The edge was not sealed with tape, however. The lay-up was evacuated inside a vacuum bag which was placed inside a pressurizable oven. The absolute pressure inside the bag was reduced to less than 2 Torr for 15 minutes. The lay-up was then heated to 240°F at which point the vacuum was vented to the atmosphere and the oven was pressurized to 20 psig. The lay-up was heated to 310°F, dwelled for 15 minutes, and then cooled to 130°F with pressure maintained. There were numerous bubbles located in the interior section of the array. However, there were very few edge bubbles and none were vented to the outside. All of the bubbles present after lamination either totally disappeared or were reduced in size considerably after autoclaving. No edge bubbles remained. The number and size of the bubbles found after the initial lamination step could probably be reduced markedly if the vacuum had been vented after the lay-up had achieved a higher temperature, 275°F. The additional pressure forces the PVB to flow out to the edge during cooldown,

precluding air entry. This process would require somewhat more expensive laminating equipment due to the 20-psig pressure it must contain. This process could be promising if the taped-edge approach proves too expensive to implement.

Cell breakage during lamination, which has been an ongoing problem, has been almost totally avoided by the use of the new soldering methods described elsewhere. Panel numbers 010380 and 010780 were interconnected by this method with no cell fractures observed.

C. CHRONOLOGY OF PANEL FABRICATION

Table 32 is a chronological list of all panel starts for the first 9 months of 1979. The panel number is actually the date the panel was produced. The array size is the number of cells in the parallel circuiting direction by the number cells in the series circuiting direction. The third column lists the manufacturer of the cell and the cell thickness in inches. The fourth column lists the amount of time the array lay-up was evacuated at room temperature prior to heating. The fifth and sixth columns show the peak temperature the laminate achieved and the amount of time it was maintained at that temperature. The information in the next two large columns describes the type of process employed, either single step or two step, and the particular parameters involved. The amount of additional pressing force exerted, beyond that exerted by the atmosphere for the last 5 minutes prior to autoclaving is shown in the first subcolumn under One-Step Process. The second subcolumn lists the autoclave and internal bag pressure used during the autoclaving process. The first subcolumn appearing under Two-Step Process gives the additional pressing force exerted on the laminate for the last 5 minutes of the cycle prior to cooldown. The last two subcolumns show whether the vacuum or the press or both were maintained during the cooldown. The panel is then autoclaved outside the bag in a second step of the process. The results are given in the last column.

Table 33 presents a continued chronology of panel starts from October 1979 through January 1980. The first 10 column headings are the same as those of Table 32. The last four relate to methods and parameters which were investigated during this time period. The first of these new columns tells whether a 1/4-in.- or 1/2-in.-thick pressing plate was used on a particular lamination. The next column entitled "Taped Edge/Shim" shows whether or not aluminum adhesive tape was used to seal the panel edge prior to lamination, and if so

TABLE 32. PANEL STARTS - FIRST 9 MONTHS OF 1979

Panel No.	Array Size	Cell Type Thickness (in.)	Evacuation Duration (min) T=amb	Peak Temp. (°F)	Dwell Time (min.)	One-Step Process Press (psi)	One-Step Process Autoclave Cycle (psi)	Two-Step Process Press (psi)	Two-Step Process Cooldown w/Vac	Two-Step Process Cooldown w/Press	Results, Defects
012479	5x13	0.015 Ruf-cut Wafers	15	305	15			No	x		Bubbles at edge
012979	5x13	0.015 Ruf-cut Wafers	5	295	15			No	x		Incomplete flow/edge bubbles
021079	18x15	0.015 Ruf-cut Wafers	15	285	30			No	x		Edge bubbles/cracked cells
022479	18x15	OCLL/0.015	30	270	30			No	x		Panel badly broken
030379	18x15	PCA Dum. 0.015	15	280	20			No	x		Bubbles at edge
042179A/B	18x15	OCLI/0.015	35	310	20	15	130 Bag / 150 Autoclave				Perfect except edges & corners deflected
071679	5x13	OCLI/0.015	5	300	30			15	x	x	Several small edge bubbles
071779	5x13	OCLI/0.015	5	300	30			15			More edge bubbles
073179	5x12	RCA-I/0.010	10	300	45			15	x	x	Air trapped in pores of Al metallization caused numerous bubbles in interior of panel.
081479	5x12	RCA-III/0.010	10	300	45			15	x	x	Glass cracked over high spot on power lead/cracked cells.
081579	5x12	RCA-III/0.010	5	300	45			5-15	x	x	Small bubbles along bus bar.
090179	15x15	RCA-III/0.010	15	275	30	15	140 Bag / 150 Autoclave				Edge scallop due to strain at at panel edge.
091579	15x15	RCA-III/0.010	10	275	30			15	x	x	Edge bubbles
09179	5x12	RCA-III/0.010	10	300	30			15	x	x	Cell fractures due to solder lumps/edge bubbles.

TABLE 33. PANEL STARTS - OCTOBER 1979 TO JANUARY 1980

Panel No.	Array Size	Cell* Type	Evacuation Duration (min)	Peak Temp (°F)	Dwell Time (min)	One-Step Process		Two-Step Process			Press Plate Thick (in.)	Taped Edge/ Saim	Cover Slide in Corners	Flat-ness	REMARKS
						Press (psi)	A-C Cycle (psi)	Press (psi)	Cooldown VAC	Cooldown Press					
101579	5x12	RCA I	15	300	45	15	150 Autoclave 140 Bag				1/4	No	No	Poor	Bubble free - deflected edges.
120479	5x12	RCA II	10	290	30			None	X		1/4	No	No	Fair	Edge bubbles - Pre and post autoclave.
120579	5x12	RCA II	45	290	30			None	X		1/4	Yes/No	No	Fair	Bubble free - pre & post autoclave-edge deflected.
120679	5x12	RCA II	10	310				20		X	1/2	No	No	Good	Vacuum broken in bag & autoclave pressurized to 20 psig @ T = 230°F; laminate continued to heat to 310°F - cooled w/pressure; result bubbles in interior of panel - most disappear after autoclave - no edge bubbles.
120779	5x12	RCA II	45	290	30			None	X		1/2	Yes/Yes	No	Good	Layup got wet - evac ports accidently blocked - interior bubbles caused by H_2O presence - cracked cell due to solder lump.
121179	5x12	RCA II	10	290	30			None	X		1/4	No	No	Poor	Large border (3/4") - edge deflected 5 mils - no edge bubbles; panel broken in half due to improper tiedown in autoclave.
121379	5x12	RCA II	45	290	30			None	X		1/2	Yes/Yes	Yes	Excel.	Bubbles at edge - most removed by autoclaving. Two small bubbles remain; 1 cracked cell due to solder lump/1 chipped cell due to misplacement of stress relief crimp under cell.
121479	5x12	RCA II	45	290	30			None	X		1/2	Yes/Yes	Yes	Excel.	Bubbles at edge - all removed by autoclaving - 1 cracked cell due to misplacement of stress relief crimp under cell.
010380	5x12	RCA II	45	290	30			None	X		1/2	Yes/Yes	Yes	Excel.	Bubbles at edge - all removed by autoclaving.
010780	5x12	RCA II	45	290	30			None	X		1/2	Yes/Yes	Yes	Excel.	Bubbles at edge - most removed by autoclaving.

*All cells 0.010 in. thick.

whether or not a 7-mil paper shim was employed inside the tape border to ensure even pressure on the glass. The column labeled "Cover Slides in Corner" shows if two 9-mil-thick glass cover slides were placed in the vacant corners of the panel. The last column relates to the degree of flatness achieved in the final laminate.

D. INTERCONNECT TECHNOLOGY

1. Parallel-Gap Welding

Both Ti/Ag and screen-printed silver metallizations were investigated for suitability with parallel-gap weldings as follows:

- A cell is measured for I-V and P-V response prior to welding.
- One or more interconnect straps are welded to the cell, using a Hughes HPC-500 welder. Variables are contact pressure, weld voltage, weld duration, and electrode "footprint."
- A second I-V curve is obtained for the cell and any degradation in peak power and I-V curve shape noted.
- Welded interconnects are then subjected to a peel test to failure at a 45° angle to the cell surface and examined to determine weld quality and to correlate the failure with the peel strength.

For the Ti/Ag evaporated metallizations, several cells yielded peel strengths of 4 lb per weld (2 weld "nuggets") with peak power degradation of 1% per weld. Appropriate weld parameters are 0.55 V at 100-ms duration, 2-lb tip force on 400-psi tip pressure with tips of 0.025 x 0.045 in. Gap is set at 8 mil.

However, consistent weld quality required considerable care and attention to cleanliness of interconnect strap and electrodes, as well as contact conditions (strap and cell flatness). As the first weld cycle is made, the heat oxidizes the strip and some distortion occurs. Thus the second weld cycle generally did NOT produce as good a nugget.

Screen-printed contacts were significantly worse than evaporated contacts. No combination of weld voltage and dwell time was found that would result in acceptable welds. High energy content would provide bonding to the metallization, but the metallization delaminated readily from the cell. Low energy content failed to produce bonding at all. The tentative conclusion was, therefore, that welding is not a suitable assembly process for cells of the design under investigation during the course of this program.

2. Radiant Reflow Array Soldering

A new approach has been devised to interconnect the solar photovoltaic cells to produce large panel arrays. This new process reduces manual handling of the fragile photovoltaic cells, and connects them economically and uniformly. The process also prevents solder lumps at the connections, which when left on top of the cell, cause cell breakage during lamination.

Several arrays were assembled by hand soldering early in this program to provide arrays for panel fabrication development. It became evident that the solder spikes and elevated tab positions above the cell surface were difficult to avoid. Laminating experiments revealed that these high points led to cell breakage due to uneven pressure. Therefore, a new automated process was developed and the flat character of the interconnect achieved by the automated process is particularly important in improving panel reliability. Additionally, the new process controls the temperature and time experienced by all joints to 210°C max (MP* 186°C) and 1-minute molten time. These two parameters must be closely controlled to achieve reproducible and reliable results.

Figure 54 shows the patterns on the front and back of the solar cells. The cells are 3 in. diameter, and 0.009 to 0.011 in. thick. As an interim method, RCA is using thick-film screening to apply solder paste consisting of 62Sn-36Pb-2Au particles in a thinner flux binder. There is no orientation of the collector grid patterns front to back; therefore, in the solder screening operation, a lever mechanism with a marking stylus was added so that while screening the front solder pad, the stylus can mark the cell back in relation to the front solder pad. The screening machine and plate details can be seen in Figs. 55 and 56.

A cell with screened but unmelted solder pads can be seen in Fig. 57, showing the front and the back pads in detail. The back solder pads are properly located with reference to the front grid pattern by use of the marking provided by the screen plate stylus. The screening plate is relieved to avoid smearing of the wet front pad while screening the back pads.

After the screening operation the cells are ready for the attachment of the connecting tabs. To ensure uniformity of the tabs a solder-coated ribbon slit to size was purchased, and tools were made to cut and form these tabs. (Figures 58, 59, and 60 show these fixtures.) A strain relief is required on

*MP = melting point

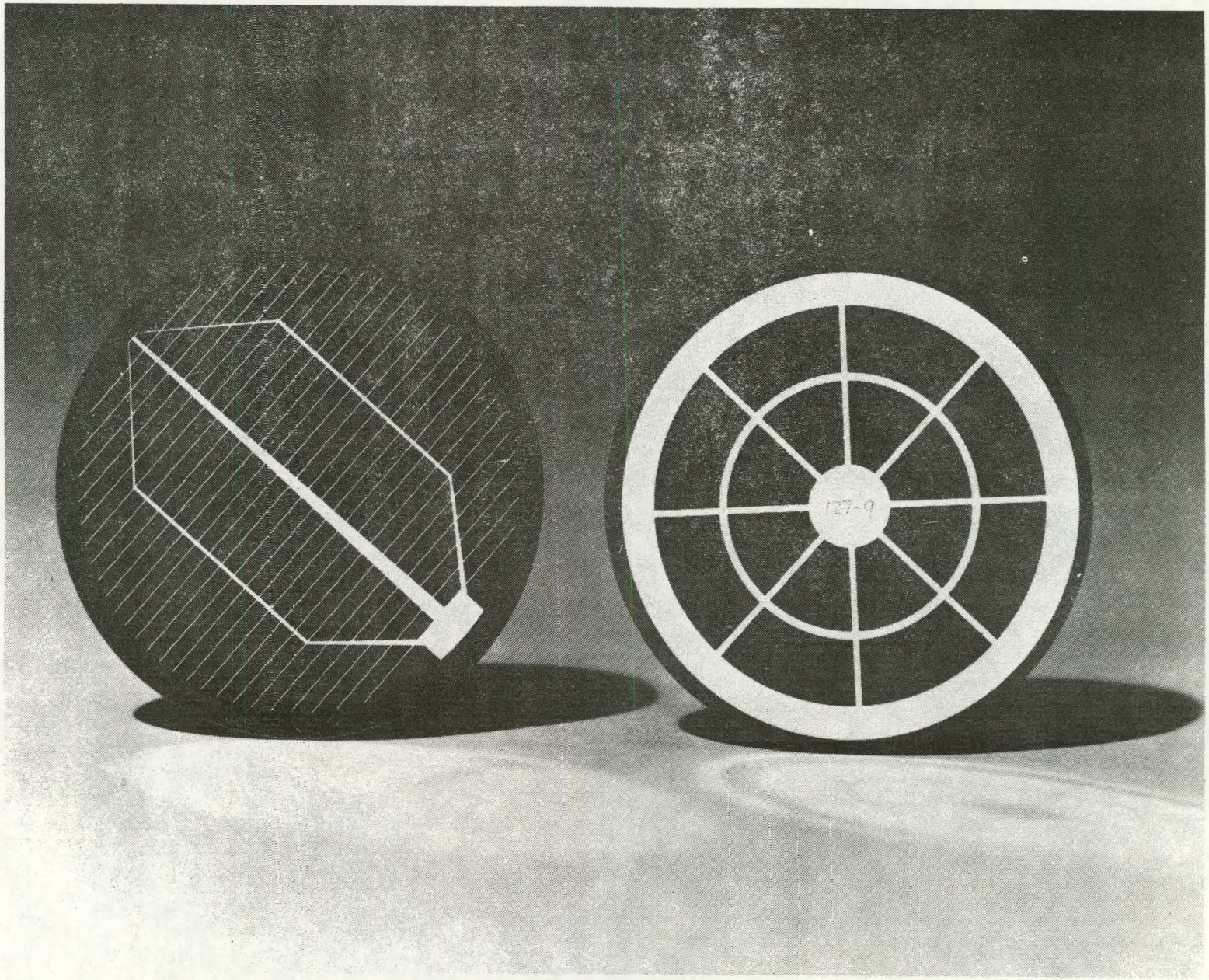


Figure 54. Patterns of front and back of solar cell.

RCA-FC790712 5-2

Figure 55. Screening machine and plate details for front of solar cell.

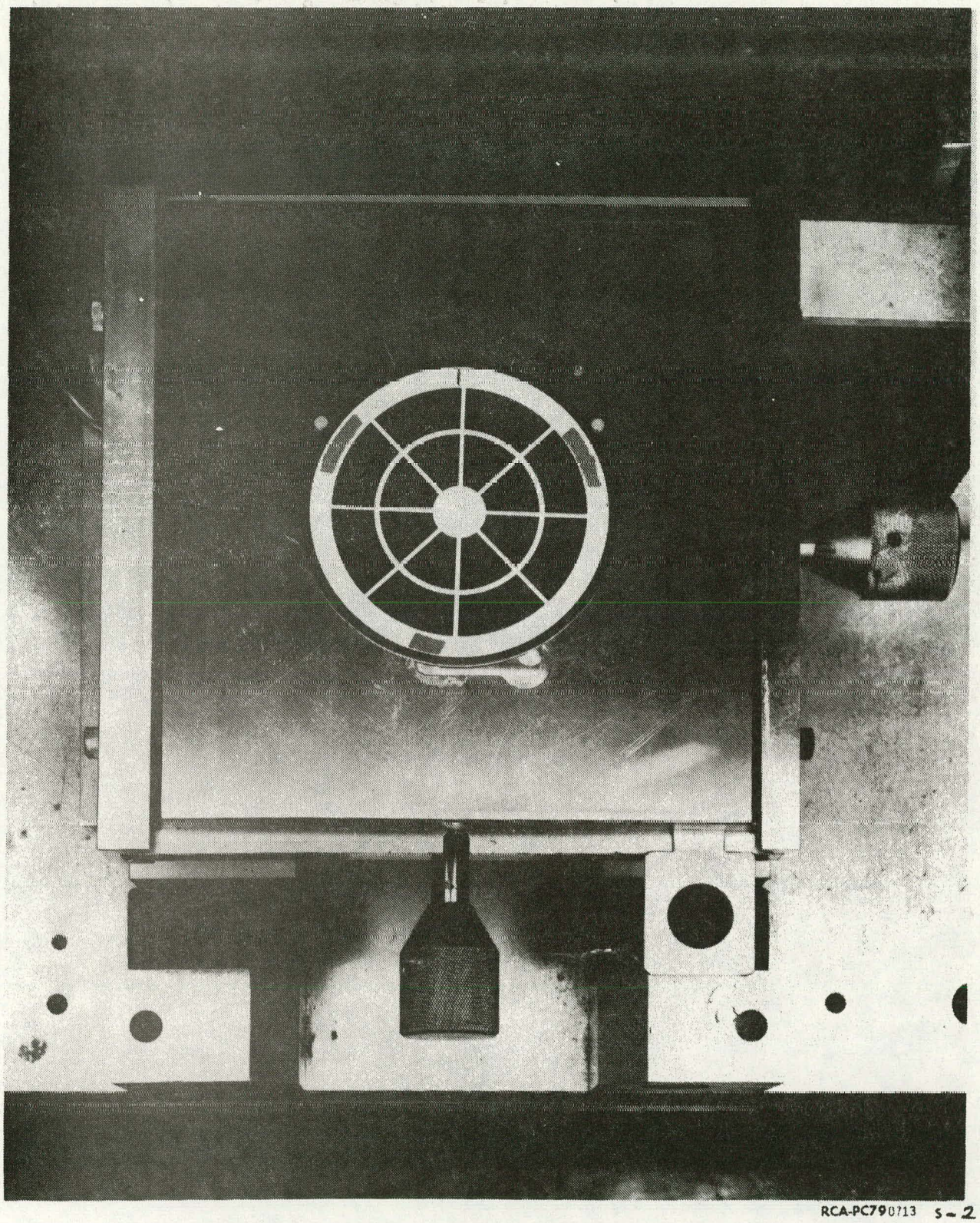


Figure 56. Screening machine and plate details for back of solar cell.

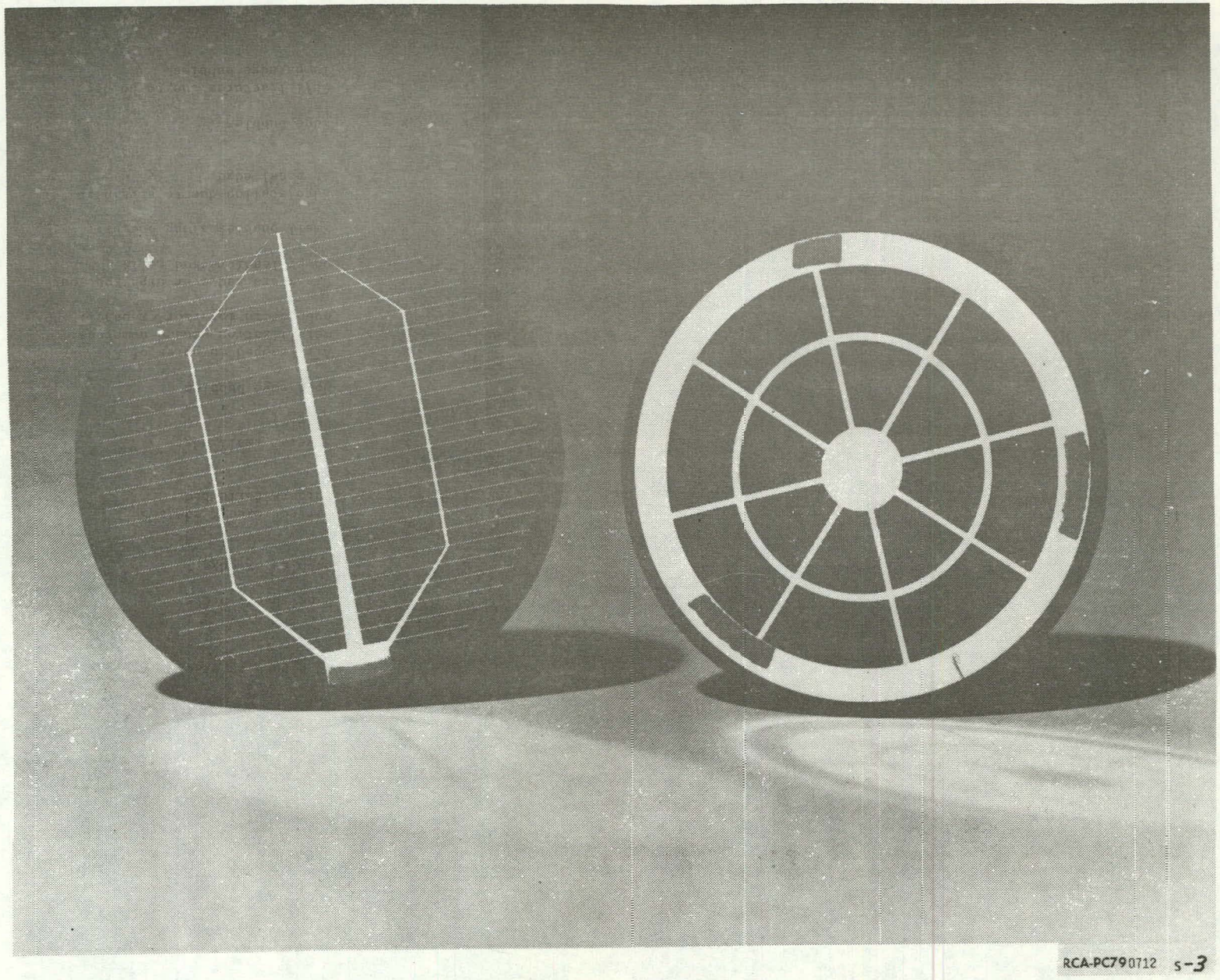


Figure 57. Front and back of solar cell with screened but unmelted solder pads.

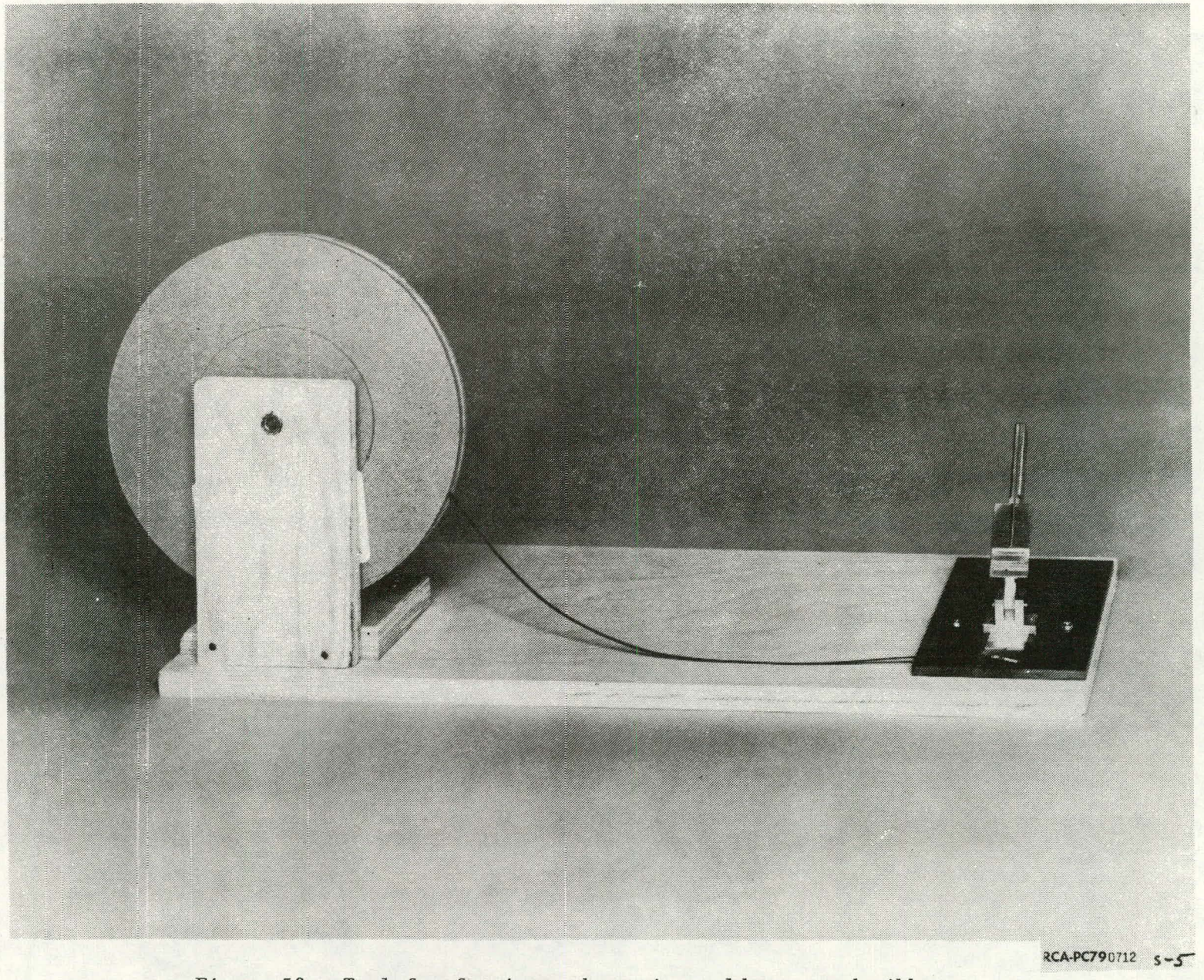


Figure 58. Tool for forming and cutting solder-coated ribbon.

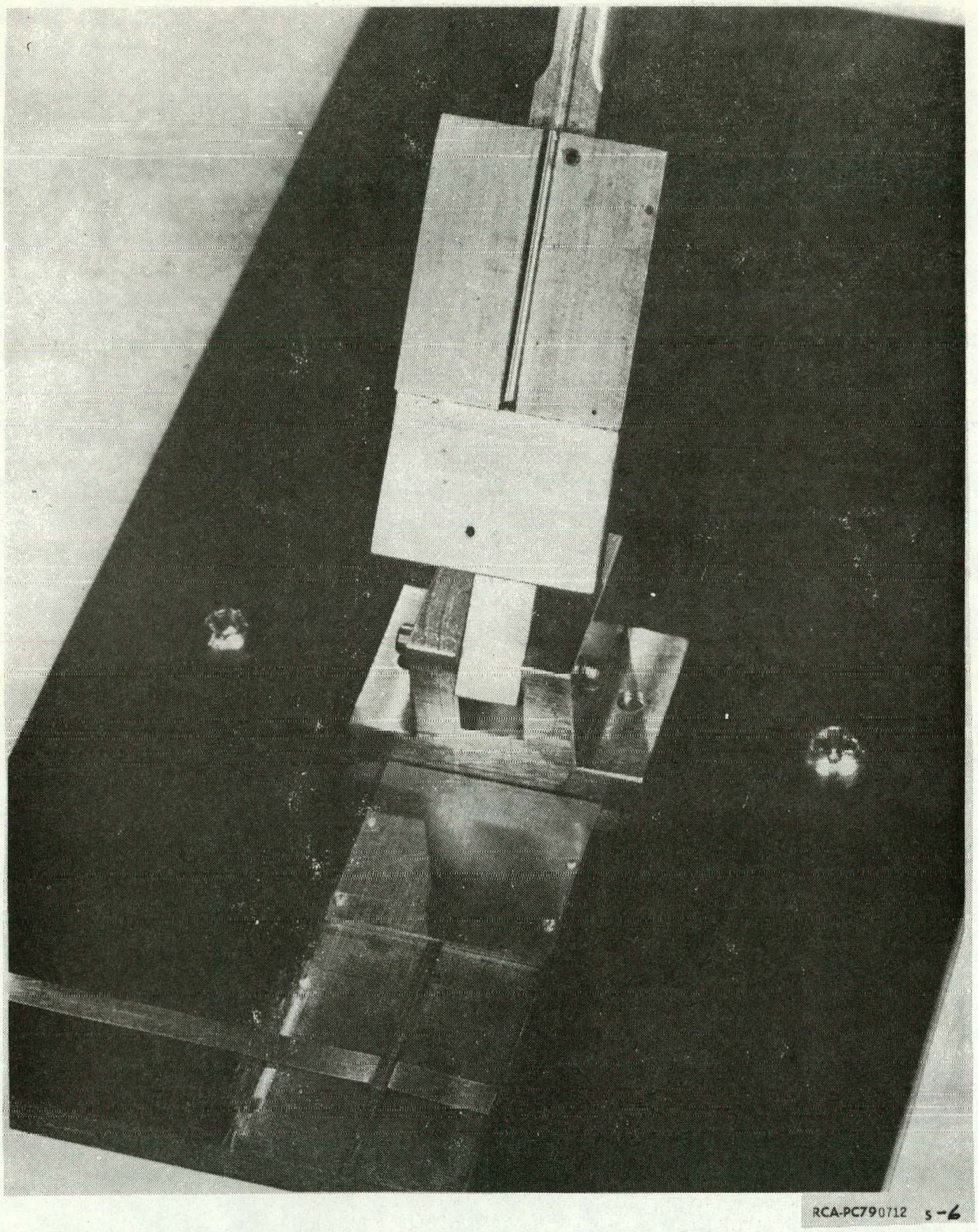


Figure 59. Close-up of cutting tool.

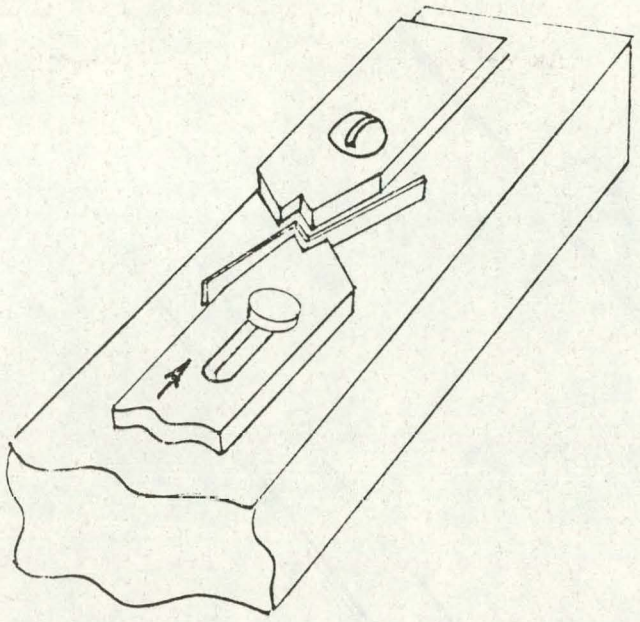


Figure 60. Crimping tool.

the tabs to take care of the dissimilar linear expansion rate between the glass, the cells, and the copper conductors. The strain relief geometry also provides compliance for the flexing of the panels due to wind and temperature changes. These strain relief contours are shown in Fig. 61.

To apply the connecting tabs on the cells arranged as shown in Fig. 62, a soldering fixture was devised. This fixture provides guides and a vacuum hold-down to locate the tabs in relation to the solder pads and to hold the cell firmly on top of the tabs to ensure a good solder joint. The heat required is 200°C for 40 to 50 s. Figure 63 shows this fixture, and Fig. 64 shows the tabbed cells.

Typical redundant arrays contain three rows of one-tab cells and two rows of three-tab cells, comprising 12 cells per row or 15 cells per row. The five rows of 12 cells will make a panel approximately 40x15 in.; and three subunits of five rows or 15 cells, a panel approximately 48x40 in.

The tabbed cells are now placed in the proper sequence on a vacuum table. A pattern for cell placement has been generated by computerized plotting of circles on true centers conforming to the designed array. It also provides directional lines to align the tabs in the proper relation to the adjacent voltaic cells. This vacuum table is presented in Fig. 65 and a close-up view is

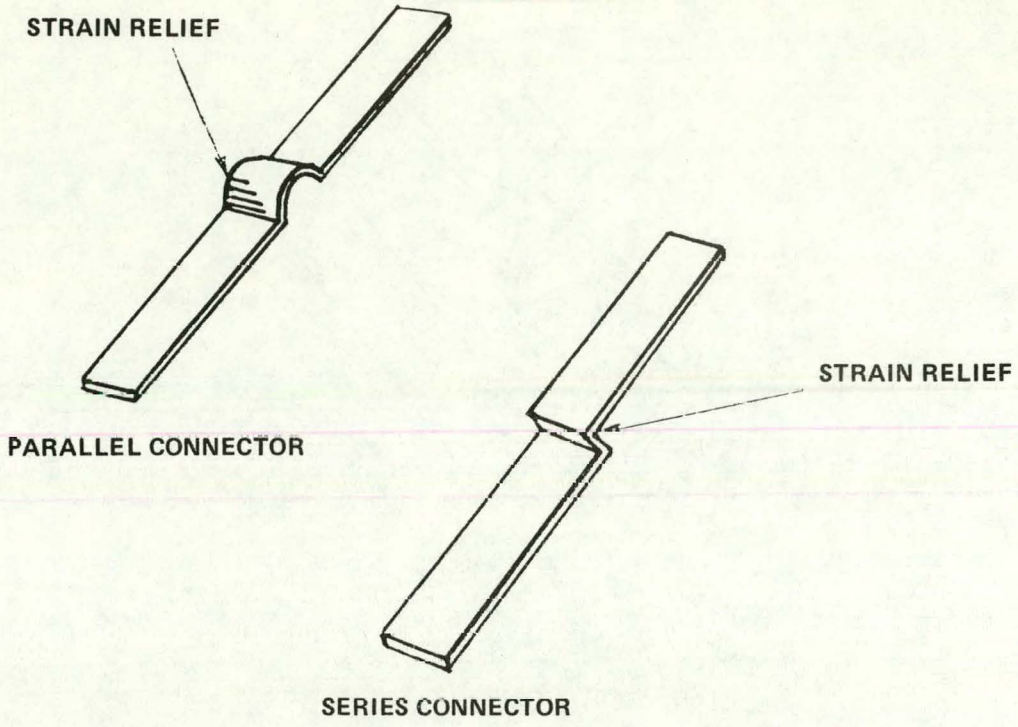


Figure 61. Strain relief geometrics.

given in Fig. 66 after locating all the cells in the desired array under vacuum. The "W" connector which was developed to prevent breakage of the glass during an autoclaving (see Fig. 67) is now applied to the array on the vacuum table. Since at one end of the cells of the array there are no connecting tabs, these connections are soldered to one of the "W" connecting bars in the proper relation to the cell soldered pads. The other "W" bar solder is applied in locations where the cell tabs terminate. As these bars are properly placed, a thin black anodized aluminum sheet is placed over the "W" connector. This thin sheet acts as a holder and the black anodization helps to absorb heat during the soldering process to equalize the temperature between "W" bars and the photovoltaic cells. A template was made to facilitate the location of the tabs on the "W" bars and the soldering pads. When everything is properly located and held down by vacuum, the unit is transferred to the radiant soldering table shown in Fig. 68. The vacuum is released on the layout table (Fig. 65) and applied to the radiant soldering table. The complete array is now ready to be connected. The table is provided with strips of Kapton covers with spring

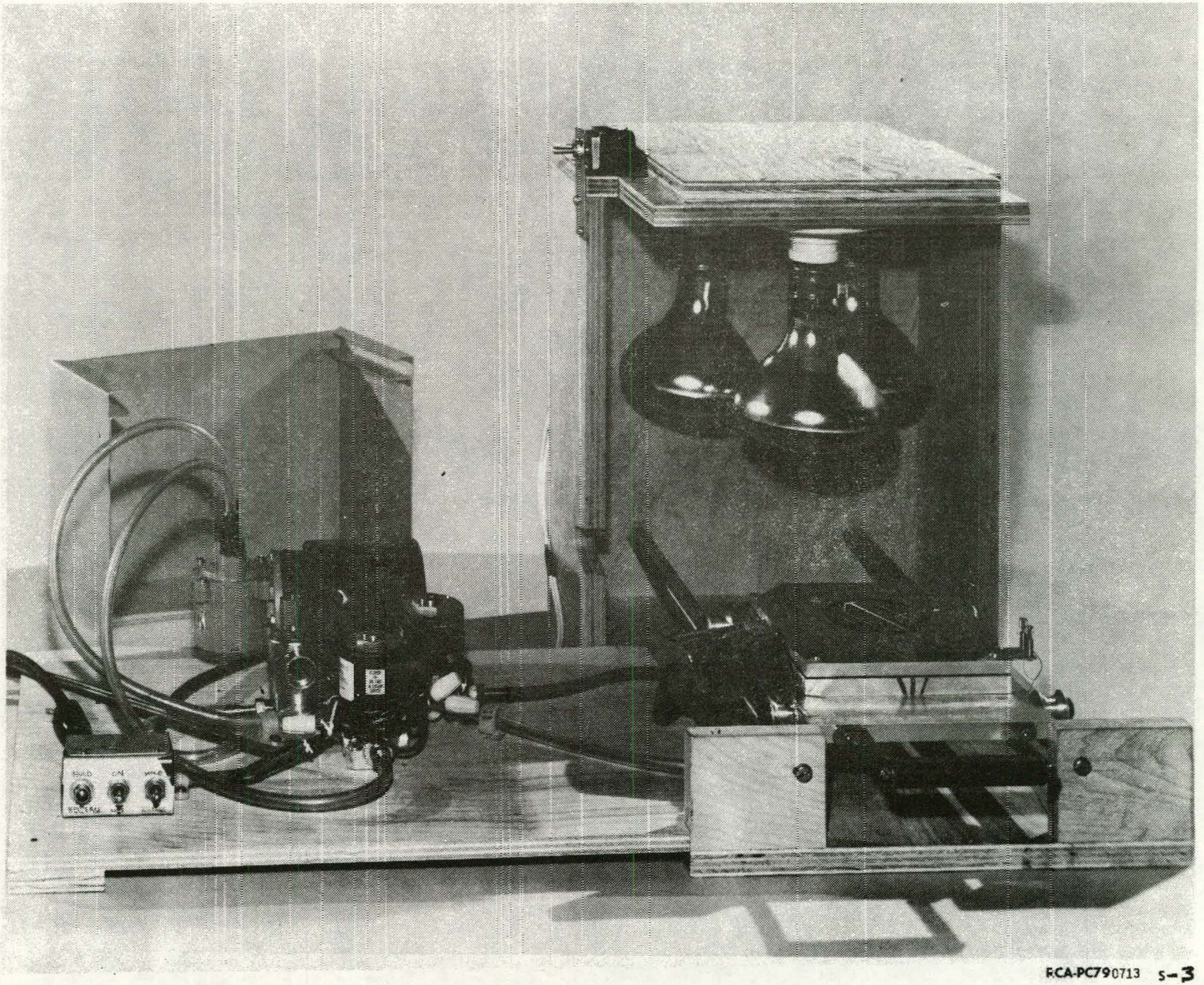


Figure 62. Soldering fixture.

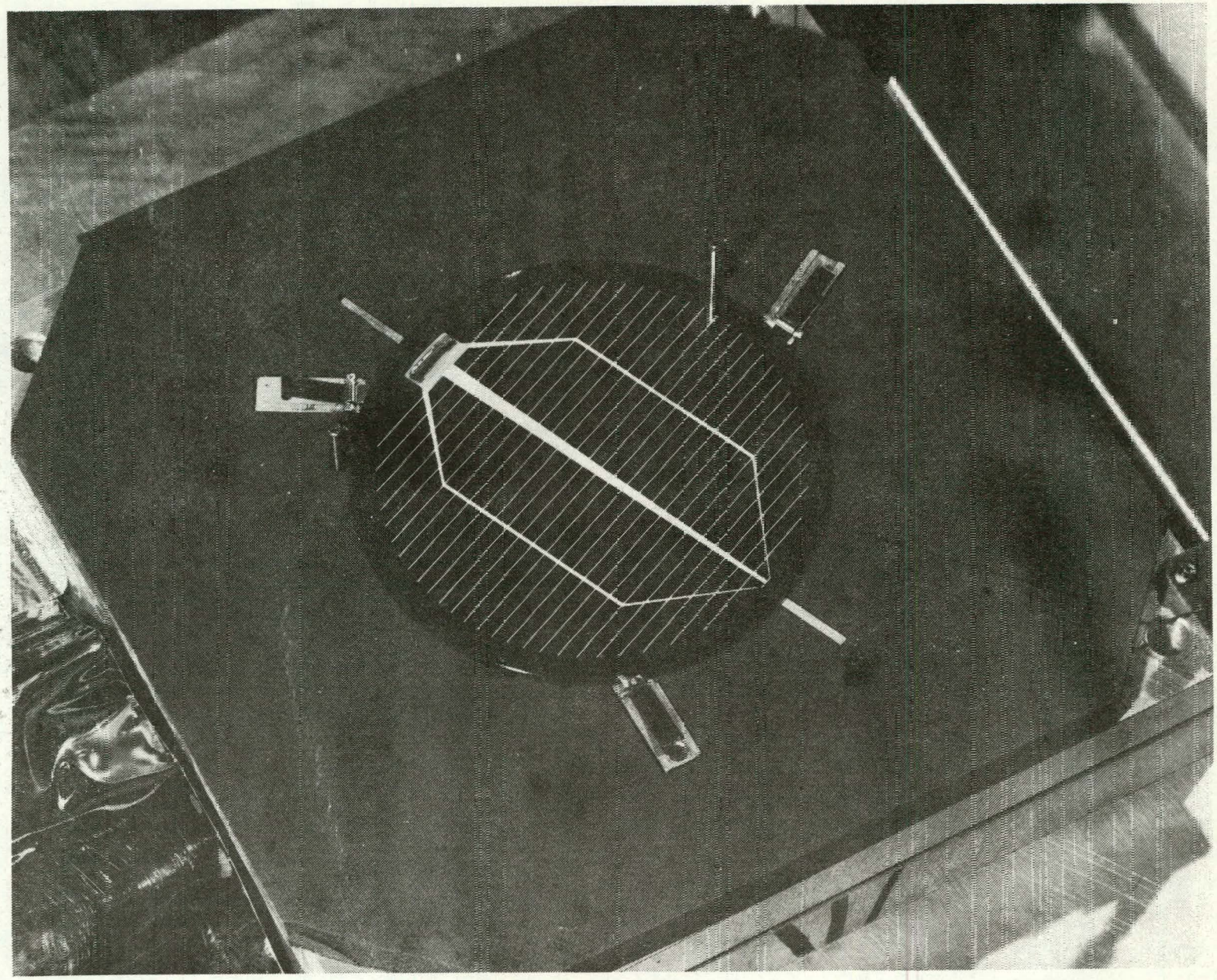


Figure 63. Detailed view of cell in place on soldering fixture.

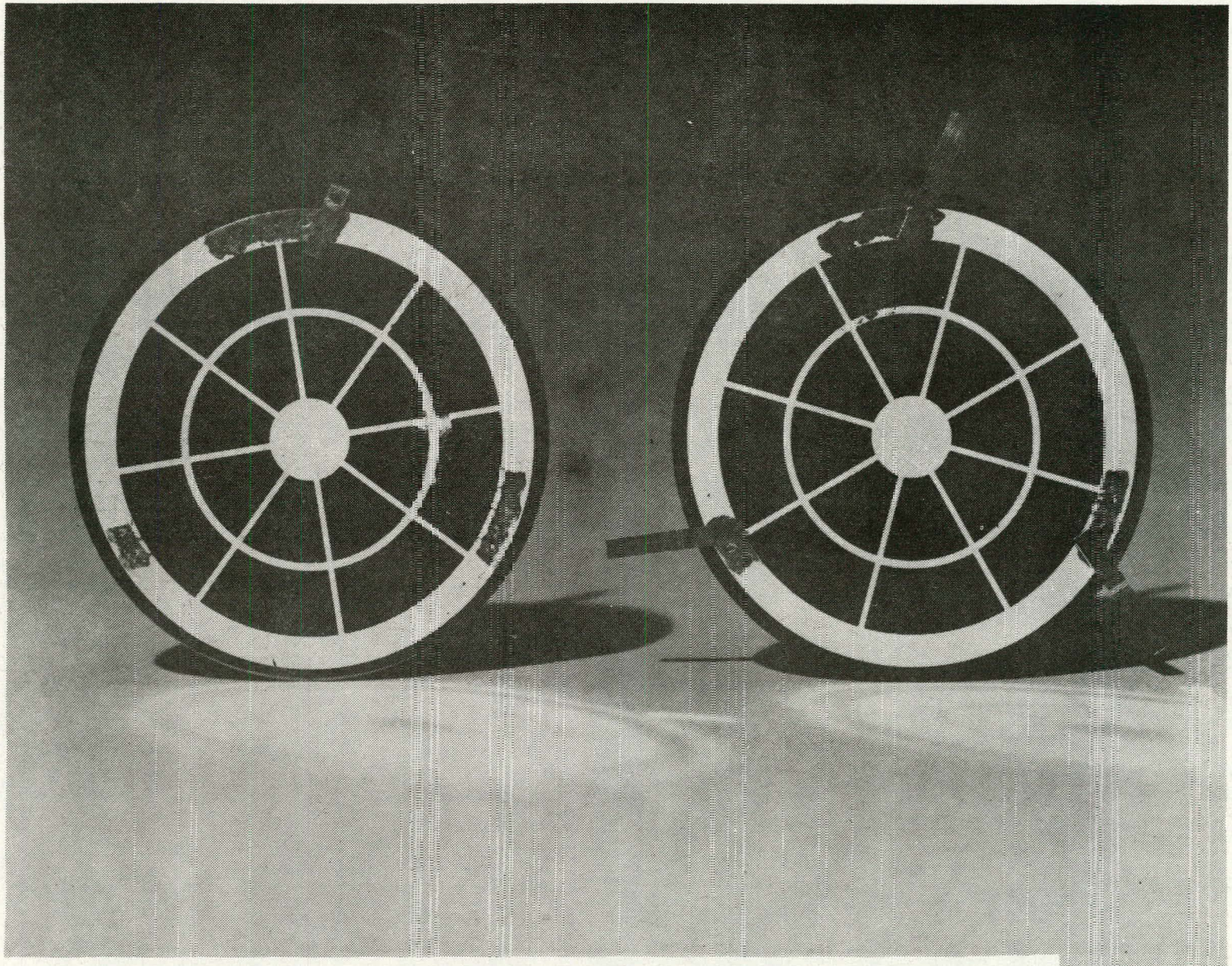


Figure 64. Tabbed solar cells.

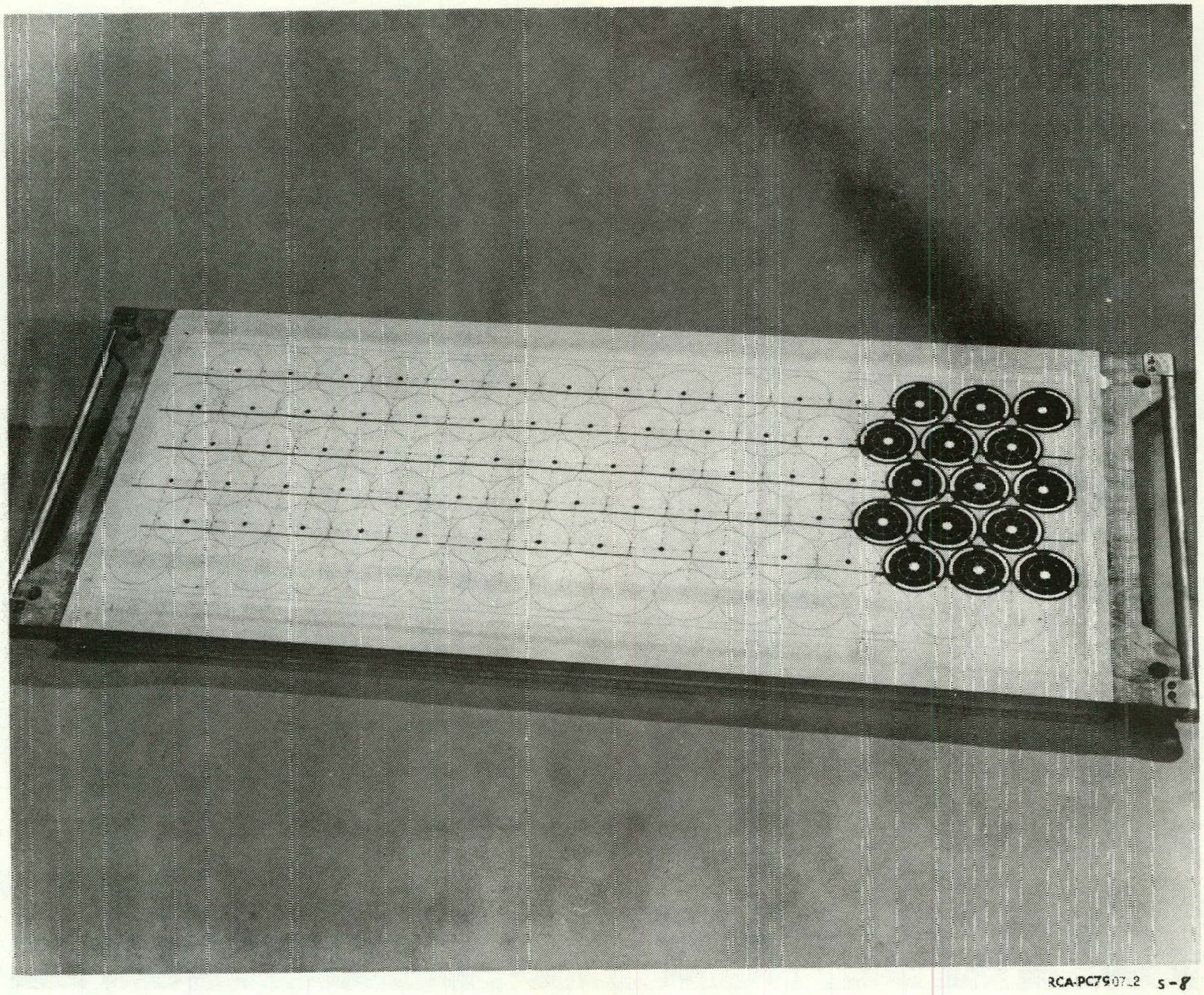


Figure 65. Vacuum table used for cell alignment.

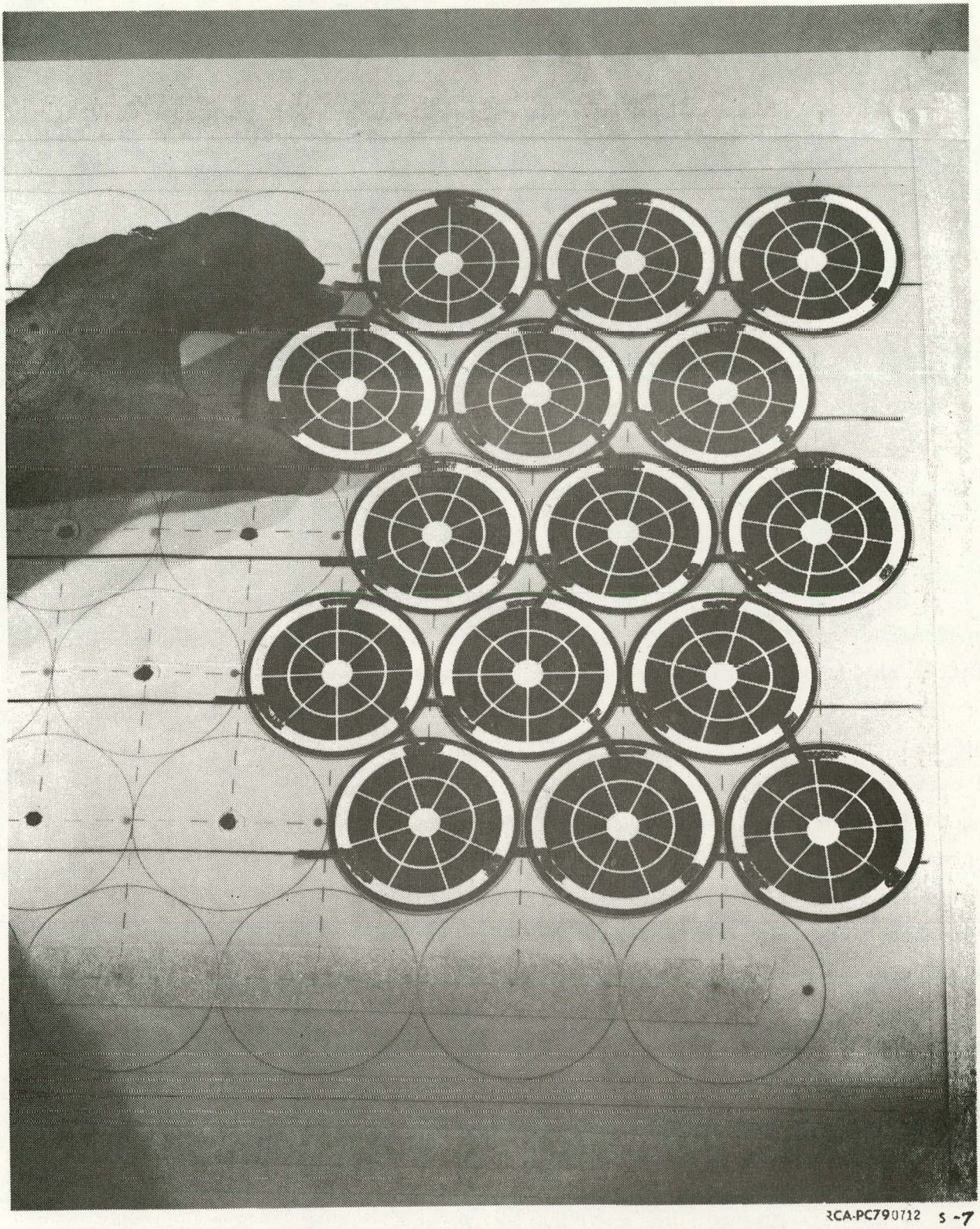


Figure 66. Detailed view of cells on alignment table.

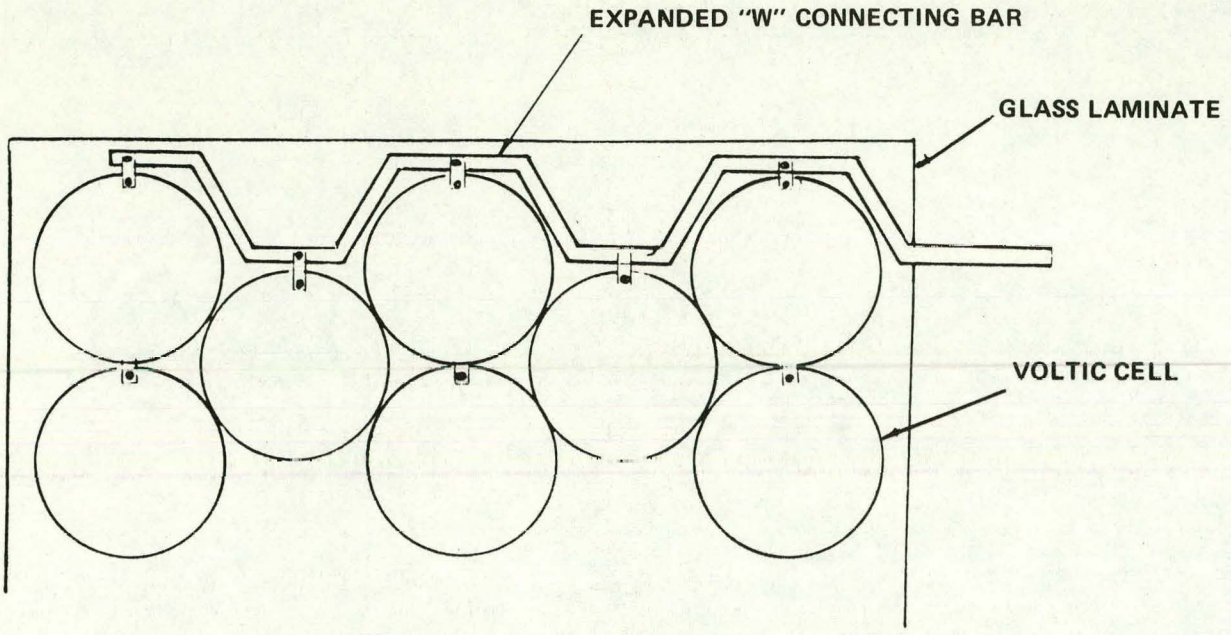


Figure 67. Expanded "W" connecting bar.

tensioners (see Fig. 68). The Kapton covers furnish a downward pressure to flatten the flexible tabs directly onto the solder pads. These forces are supplied by the vacuum pull-down (see details on Fig. 68). When the heat is applied, the Kapton expands rapidly, but the spring tension immediately relieves an otherwise detrimental wrinkling effect. The Kapton covers not only ensure a good junction, but also control the thickness of the solder in the joint to approximately 1 mil. This height control prevents the breaking of the cells during the subsequent lamination operation. After these covers are applied, a bank of heating lamps, giving an overall temperature of 200°C, is passed over the array at a rate of 1 ft/min (see Fig. 69). At the completion of the cycle the Kapton covers are removed. The layout vacuum table (Fig. 65) is placed on top of the soldered array and, by releasing the vacuum of the heating table and applying vacuum to the layout table (Fig. 65), the complete array is drawn up and removed from the soldering table. Then the array is placed on a flat surface, either the connecting table or the transport table (Fig. 70). After removing the vacuum, the five rows of connected cells are gently deposited on these surfaces. If an array of 40x48 in. is desired, the cells are connected in series on this table. This array is now ready for laminating.

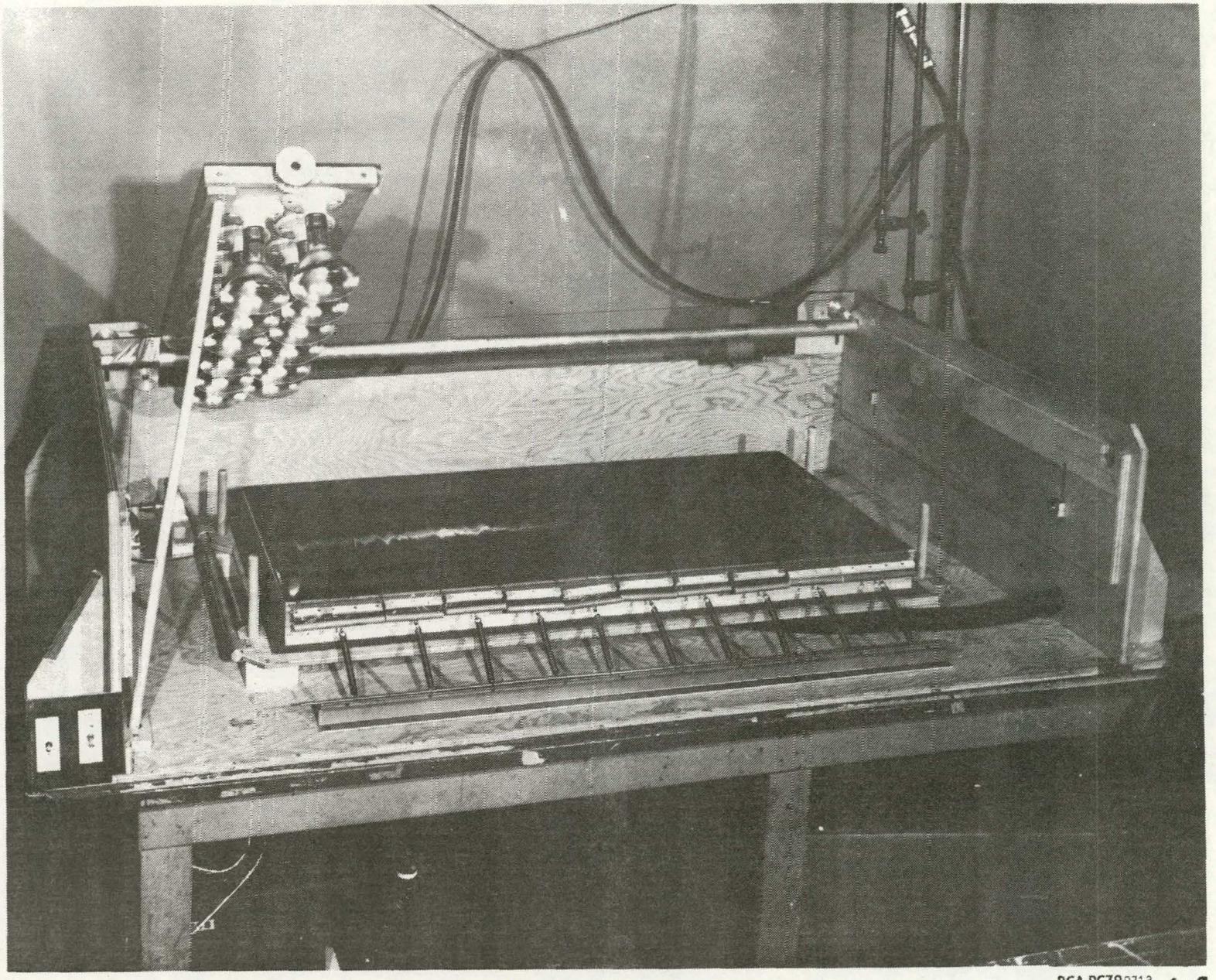


Figure 68. Radiant-soldering vacuum table.

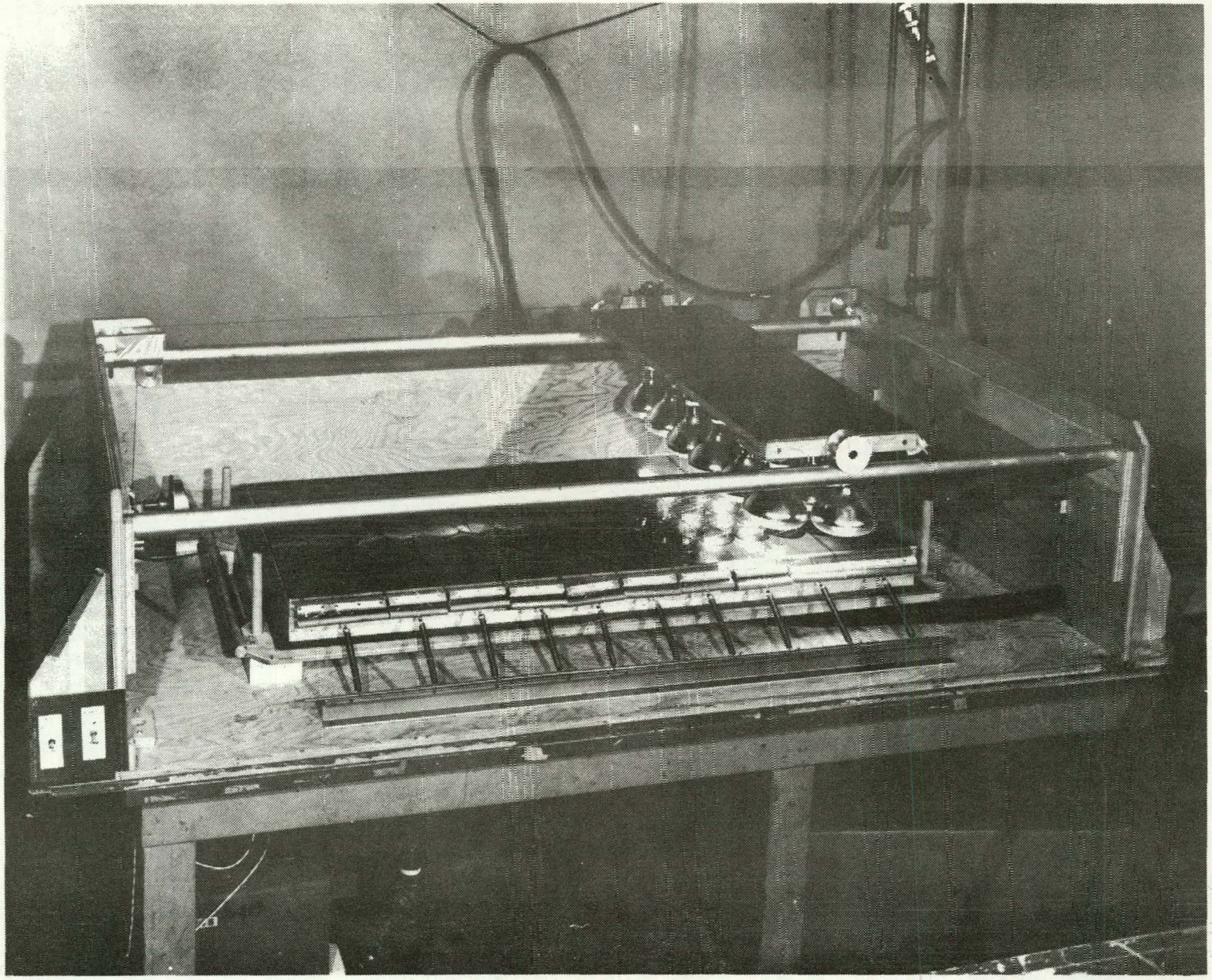


Figure 69. Radiant-soldering vacuum table in operation.

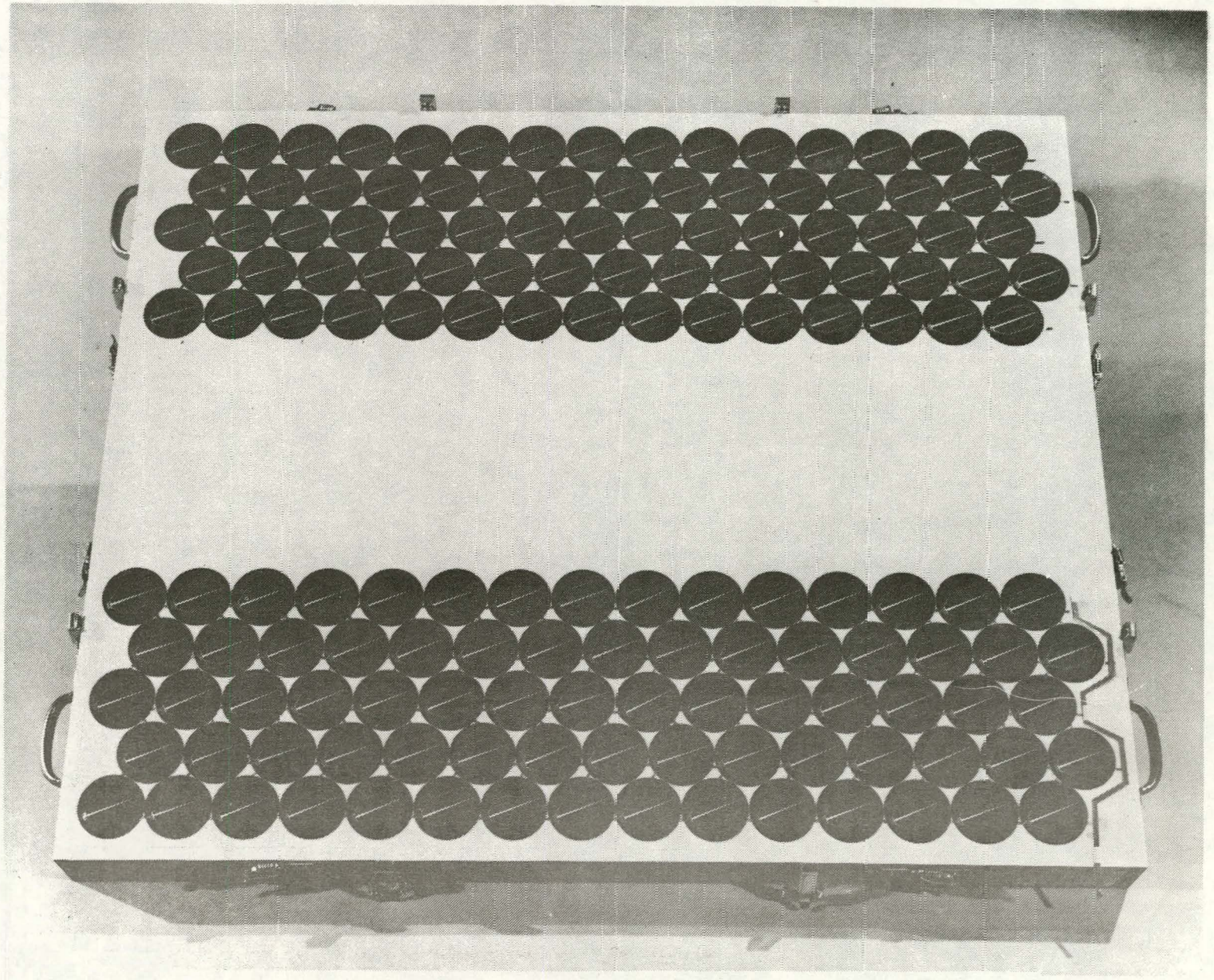


Figure 70. Layout table.

SECTION V

PROCESS SEQUENCE DEVELOPMENT

A. INTRODUCTION

In the work described in the previous sections, we identified candidate cost-effective processes for large-scale silicon solar cell and panel production, brought those processes needing development to a state of technological readiness, and verified such processes by experimental production of solar cells and panels. To obtain a selling price of less than $700/kW requires that these processes be assembled to form a manufacturing sequence possessing both material and inter-process compatibility with the capability of operating at high output and yield.

In the studies described here, the three manufacturing sequences shown in Figs. 71 and 72 were investigated to evaluate their overall cost/performance effectiveness. This evaluation was performed by studying the production flow and the performance of each sequence; it involved the processing and testing of 1500 solar cells, which are then used in the fabrication of solar panels. Two major objectives of this work were to test the performance of these sequences when low-cost forms of silicon are used for starting material and to assess the internal compatibility between process steps. The reason for this approach is two-fold in that low-cost processes have been used successfully with high-quality Czochralski silicon wafers, and on the other hand, most low-cost silicon forms have not been subjected to these specific low-cost sequences. Two forms of silicon were used: 3-in.-diameter "solar-grade"* wafers and dendritic web** silicon.

Most of the solar cells were fabricated from the solar-grade wafers, and a small amount of dendritic web was assessed for compatibility with selected low-cost processing steps.

In this overall study, both material- and process-related compatibility problems were experienced in the areas indicated on Figs. 71 and 72. These problems, their implications, and possible alternatives are discussed in subsection D, below.

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*"Solar-grade" silicon is a product of the Monsanto Corp., St. Louis, MO. These are 3-in.-diameter n- and p-type, 1/2 to 2 Ω-cm, round silicon wafers, received in a "saw-cut" form.

**Purchased from Westinghouse Research and Development Center, Pittsburgh, PA.

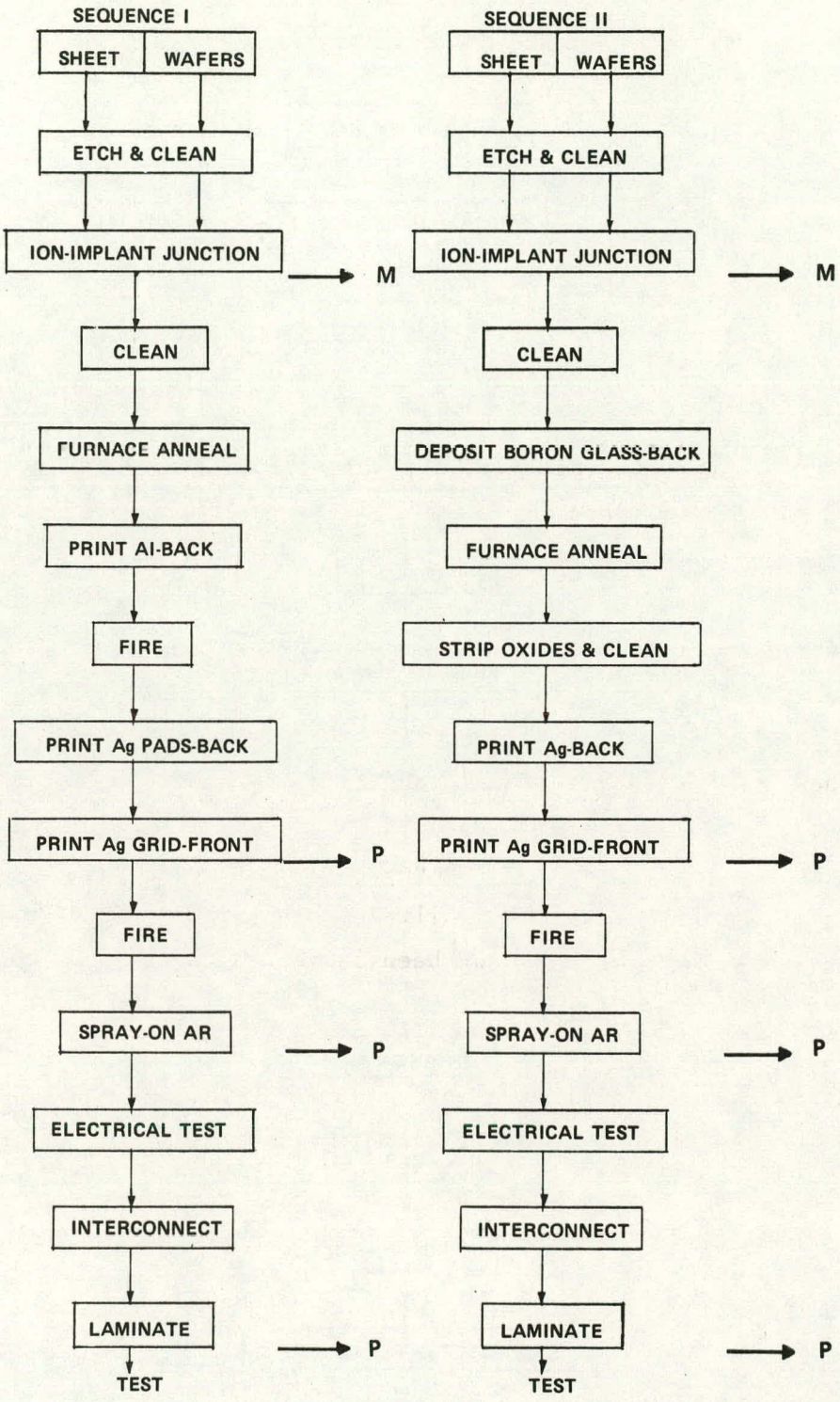


Figure 71. Manufacturing sequences I and II.

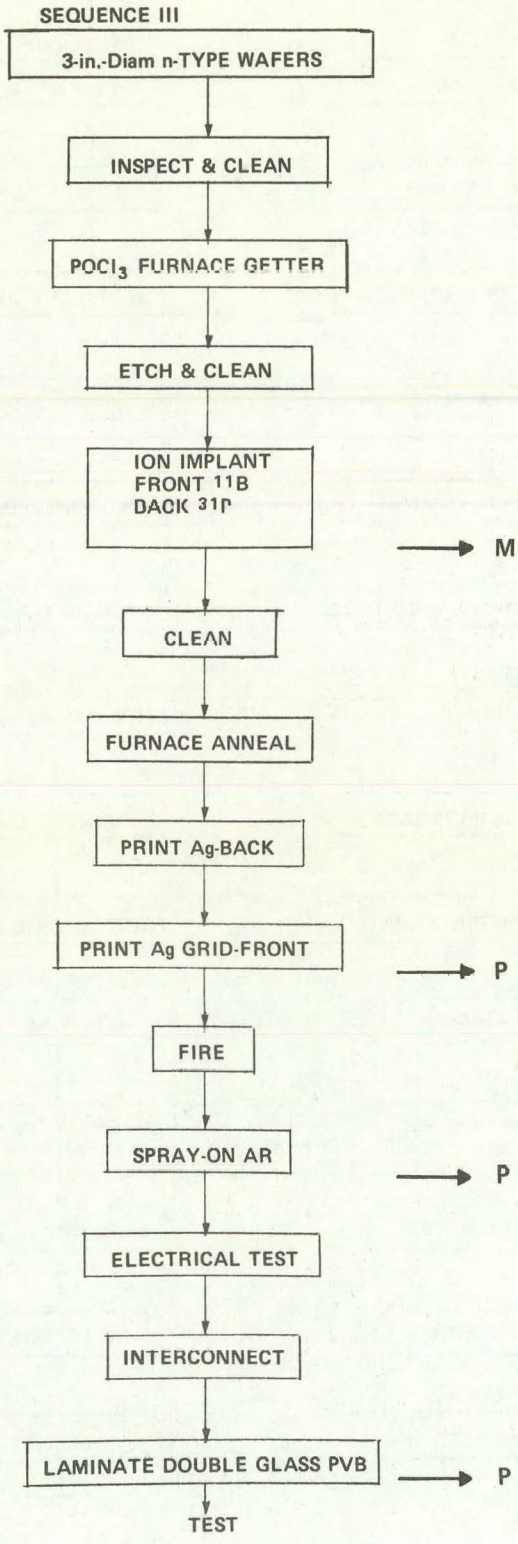


Figure 72. Manufacturing sequence III.

The performance of solar cells made by the manufacturing sequences of Figs. 71 and 72, and by an alternative sequence which uses gaseous diffusion for the junction formation is given in subsection E.

B. AUTOMATIC ELECTRICAL TEST SYSTEM

1. System Description

Complete testing of the illuminated I-V characteristics of photovoltaic devices is necessary for process control and quality assurance. This requires an automated test technique which is fast and accurate and conveniently handles the information obtained. Our automated data acquisition system comprises a calculator, digital voltmeter, and multiplexer. These are interfaced with an AM-1 illumination source and a programmed power supply. The data, raw I-V characteristics and calculated parameters, are initially recorded on magnetic tape cassettes and subsequently transmitted to a large computer system which supports a data base structure. The larger computer system more easily provides formated output, statistical analyses, and long-term, easily accessible data storage.

Figure 73 shows a block diagram of the automated test system. A Hewlett-Packard* 9845S desktop computer controls the system. It is a basic programmed calculator with 64k bytes of read-write memory, a CRT display, an 80-character line printer, and two tape drives capable of storing 214k bytes of information each. It uses an RS232C interface to communicate with other computers and an IEEE 488 bus to communicate with the test system instruments.

The digital voltmeter is a 6-½ digit, autoranging multifunction instrument. Dual-slope integration techniques, automatic self-test, and automatic calibration are combined to produce accurate and reliable operation. All operational modes can be programmed from the computer.

The scanner provides computer addressable relays. The low thermal signal relays are used to direct analog signals to the digital voltmeter. The power relays actuate the solar simulator shutter, the vacuum holddown for the solar cell, and the cell contact actuator.

The power supply programmer produces an analog voltage proportional to the commands received from the computer. This analog voltage determines the output

*Hewlett-Packard Corp., Palo Alto, CA.

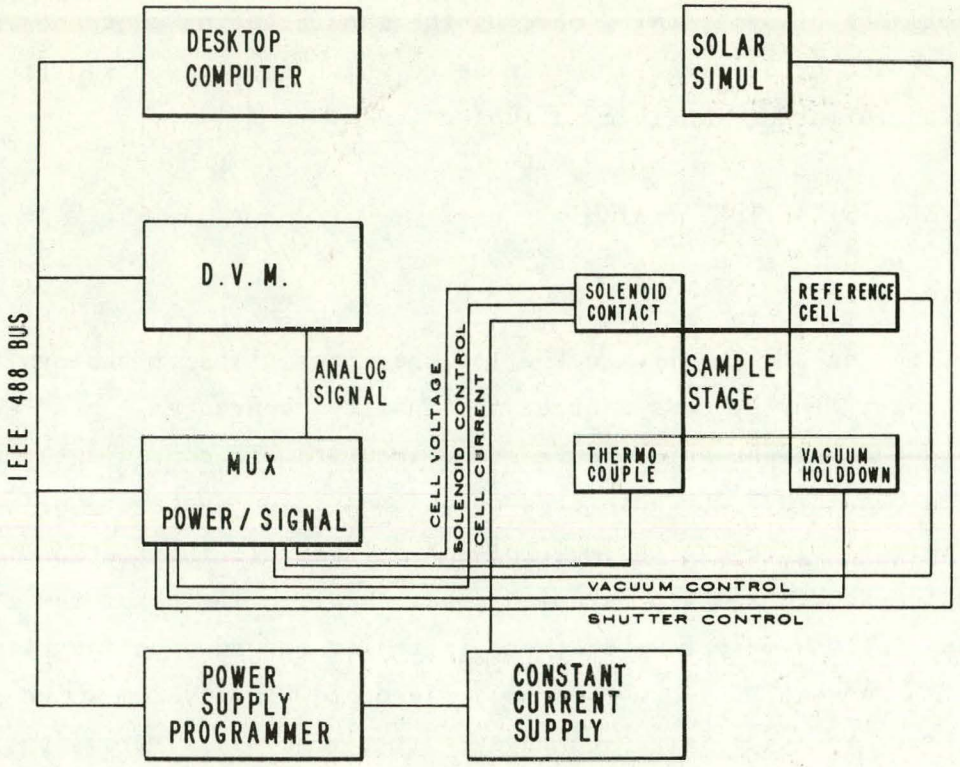


Figure 73. Automated test system block diagram.

current in the bipolar operational power supply. This supply is a constant current source and either sources or sinks the solar-cell current.

The solar simulator is a xenon arc lamp filtered to AM-1. It illuminates a 3-½-x3-½-in. area with a nonuniformity of less than 6% between the brightest and weakest points. A solenoid-activated shutter controls the output illumination. The arc lamp power supply is regulated for short and long term stability.

Figure 74 shows a cell-testing stage with a 3-in.-diam. solar cell in the test position. A reference solar cell, visible on the side of the fixture, measures the illumination level prior to each cell-testing sequence. A copper-constantan thermocouple is also part of the cell test fixture to monitor the fixture temperature and correct the data to 25°C. On the right is a solenoid-actuated contact to the metallization on the illuminated side of the cell. This contact consists of two electrically isolated probes. This allows elimination of series resistance by having separate voltage and current probes. It also allows for the measurement of resistance between these probes, assuring proper cell contact. The back contact to the solar cell consists of a spring-loaded voltage probe and the fixture surface.

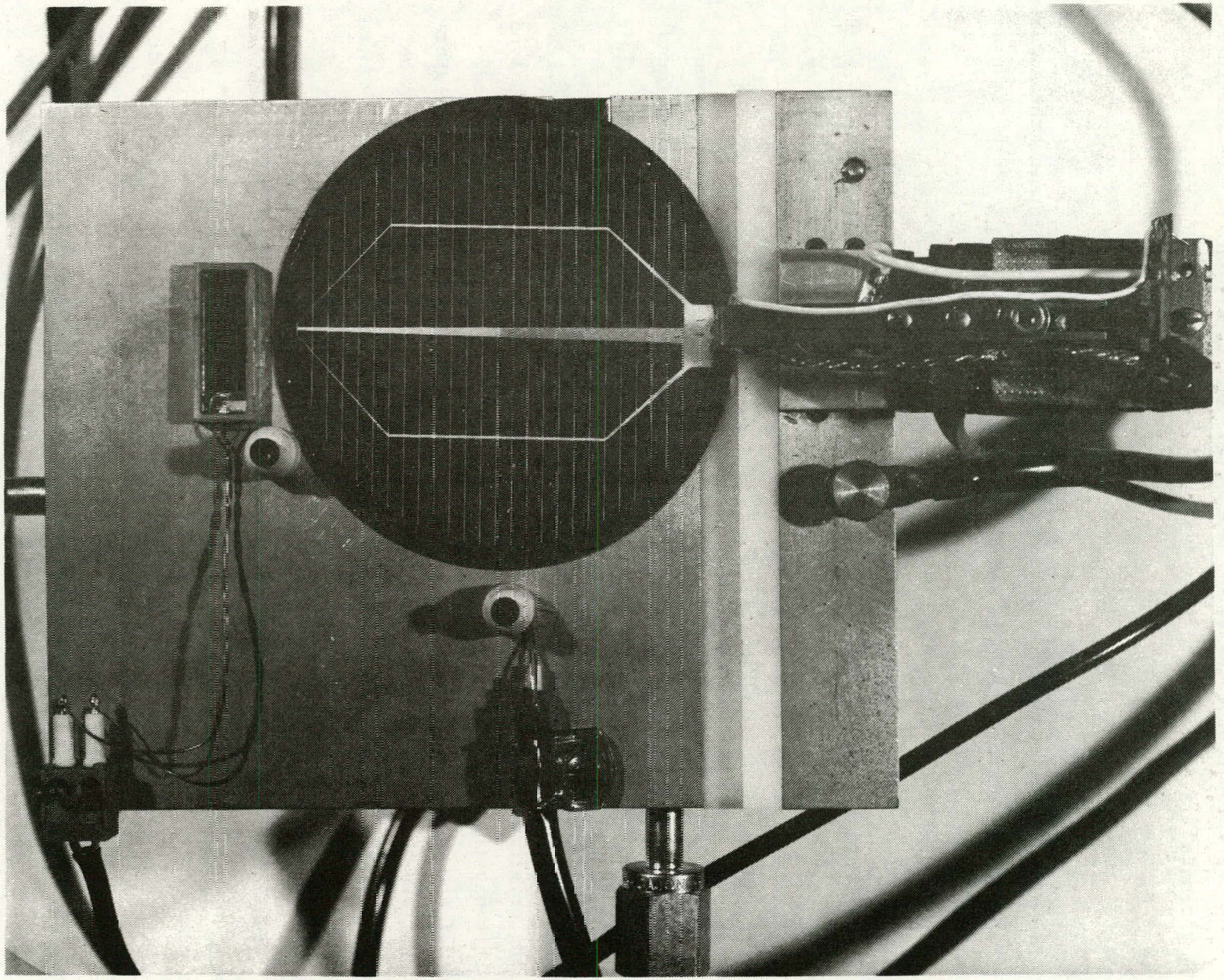


Figure 74. Photograph of cell-testing stage of testing system.

The test sequence begins with a solar cell positioned on the test fixture with the metallization beneath the contacts. The vacuum holddown is applied, the contacts are lowered, and the computer verifies electrical contact to the solar cell by programming the digital voltmeter to its ohms function and measuring the resistance between the voltage and current probes. The solar simulator is unshuttered, the computer measures the reference cell to determine the illumination level, and measures the thermocouple voltage to find the fixture temperature.

The output current was previously programmed to zero. The cell voltage is measured. The current source is now stepped to 100 mA in 10-mA steps while measuring both the cell current and cell voltage. This establishes the cell open-circuit voltage and the slope at the cell open-circuit voltage. The cell current is now increased in 64-mA steps while measuring the cell voltage. The cell current is calculated. The cell output power is monitored and when a decrease is seen, the step size is halved and the step direction is reversed. When the cell power decreases again, this process is repeated. This continues until a 2-mA current step results in a decrease in the cell output power. This is the maximum output power. The cell current is again increased in 16-mA steps until the cell voltage changes polarity. The current source is then reset to the original value before the polarity reversal, and the step size is halved. In this way the cell short-circuit current is approached. When a 2-mA increment of the cell-current results in cell voltage reversal, the solar simulator is shuttered, the constant current source programmed to zero current, and the vacuum holddown and solenoid contact released.

During the acquisition of the data, the cell current and voltage are scaled to 1 sun conditions.

The computer calculates the following: (1) open-circuit voltage, (2) short-circuit current, (3) cell voltage at maximum power, (4) cell current at maximum power, (5) maximum output power, (6) fill factor, (7) efficiency, (8) series resistance, (9) shunt resistance, (10) illumination level, and (11) fixture temperature.

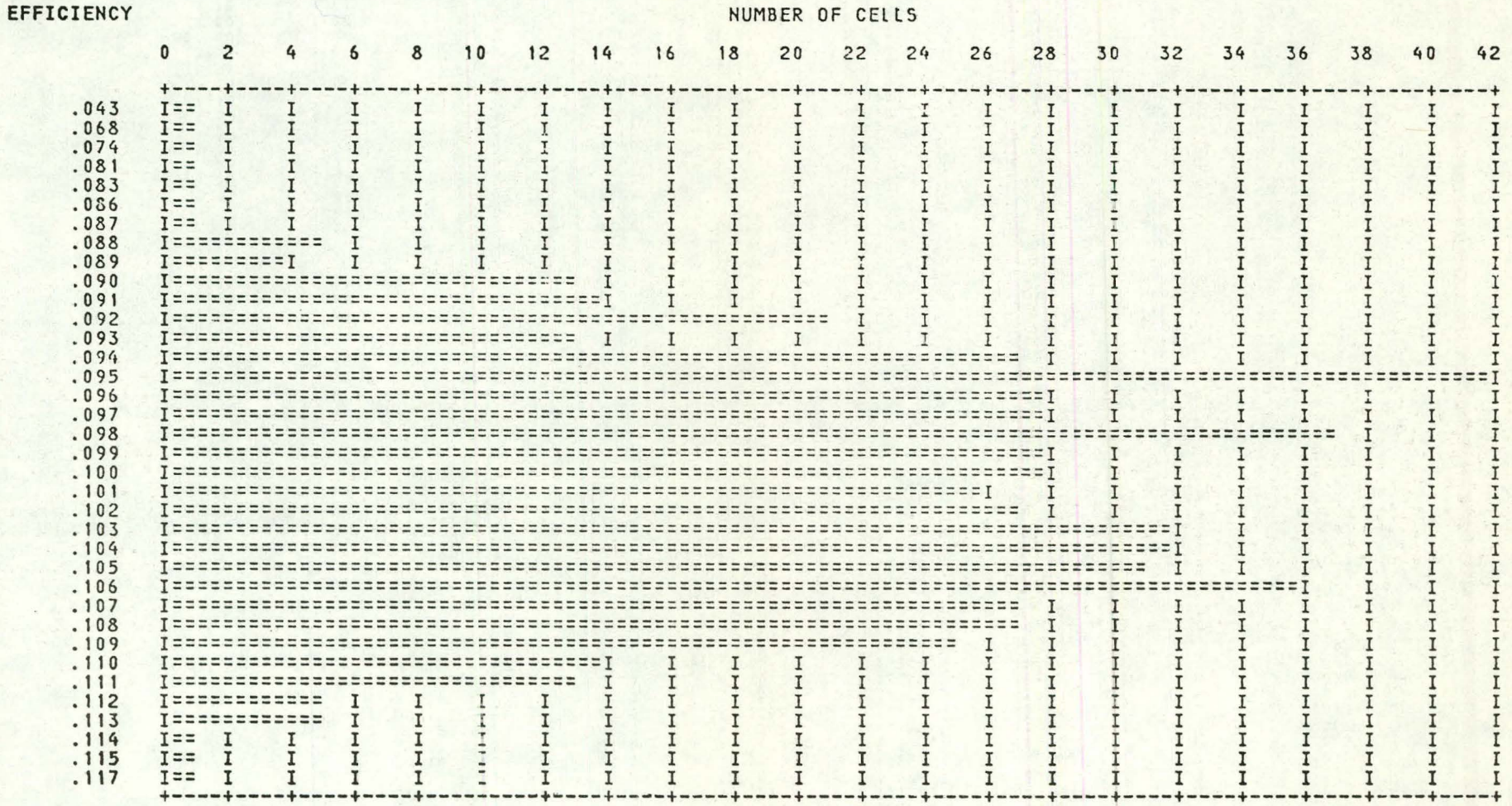
Table 34 shows a formated output of the data transmitted by the calculator to the data base. Table 35 shows a histogram of cell efficiency versus the number of cells for one lot of commercial solar cells. Features such as these as well as other statistical analyses are readily available through simple on-line commands within the data base language structure.

TABLE 34. DATA TRANSMITTED BY CALCULATOR TO DATA BASE

LOTNO	TESTDT	AREA	CELL NUMBER	IRRADANCE	OPN CIR VOLT	CELL CURRENT	MAX POWER	FILL FACTOR	SERIES RESIS
4	79/04/05	45.00	OCLI004051	102.0	.575	1,210.	10.90	.708	.068
			OCLI004052	102.0	.574	1,190.	10.80	.713	.064
			OCLI004053	101.0	.570	1,220.	9.83	.637	.093
			OCLI004054	101.0	.571	1,190.	10.50	.699	.073
			OCLI004055	100.0	.573	1,220.	10.80	.693	.072
			OCLI004056	101.0	.575	1,260.	11.00	.682	.075
			OCLI004057	101.0	.572	1,200.	10.80	.710	.069
			OCLI004058	100.0	.574	1,250.	11.10	.699	.067
			[illegible]059	100.0	.568	1,190.	10.40	.692	.073
				101.0	.574	1,240.	10.90	[illegible]	.071
				100.0	.572	1,250.	10.60		.076
				[illegible]9	.574	1,230.	1[illegible].2[illegible]		.066
					.574	1,190.	[illegible]	.7[illegible]	062
					.573	1,180.	10.70	.739	[illegible]
					[illegible]	1,2[illegible]	11.00	.698	
			[illegible]			[illegible].	10.50	.696	.06[illegible]
			OCLI004[illegible]			1,190.	10.80	.713	.067
			OCLI004094			1,150.	10.30	.704	.067
			OCLI004095	10[illegible]	[illegible]	1,160.	10.10	.689	.073
			OCLI004096	100.0	.567	1,130.	10.40	.725	.067
			OCLI004097	100.0	.574	1,240.	11.30	.712	.065
			OCLI004098	100.0	.568	1,190.	10.50	.701	.071
			OCLI004099	100.0	.568	1,150.	10.40	.720	.065
			OCLI004100	101.0	.573	1,220.	10.80	.694	.067

SHUNT RESIST	JCT DEPTH	SHEET RESIST	CONTACT RST	METAL RST	PMAX CURRENT	PMAX VOLTAGE	EFFICIENCY	BASE TEMP
5.03	1.00	1.0	1.00	1.00	1,110.	.442	.107	27.5
16.60	1.00	1.0	1.00	1.00	1,070.	.454	.106	27.8
13.90	1.00	1.0	1.00	1.00	1,070.	.415	.098	28.0
24.60	1.00	1.0	1.00	1.00	1,070.	.443	.105	28.1
4.34	1.00	1.0	1.00	1.00	1,080.	.448	.107	28.1
10.50	1.00		1.00	1.00	1,130.	.437	.109	28.1
3.08	1.00		[illegible]0	1.00	1,100.	.443	.108	28.0
4.61		1.0	.	1.00	1,130.	.443	.111	28.[illegible]
10.10		1.0	1.0[illegible]	1.00	1,090.	.432	.104	
3[illegible]	[illegible]00	1.0	1.00	1.00	1,130.	.437	.108	[illegible].0
	1.00	1.0	1.00	00	1,110.	.431		28.0
	1.00	1.0	1.00		1,130.	.448		28.2
.44	1.00	1.0	1.00		1,110.	.449	[illegible]	28.0
4.55	1.00	1.0	1.00	1.	[illegible]070.		.106	28.1
7.08	1.00	1.0	1.00	1.00			.112	28.2
5.06	1.00	1.0	1.00	1.00		[illegible]	.110	27.9
7.39	1.00	1.0	1.00	1.00	1,0[illegible]	454	.108	28.1
4.59	1.00	1.0	1.00	1.00	1,060.	443	.105	28.2
27.10	1.00	1.0	1.00	1.00	1,090.	448	.108	28.2
7.39	1.00	1.0	1.00	1.00	1,100.	.438	.106	28.4
10.90	1.00	1.0	1.00	1.00	1,110.	.455	.112	28.3
3.55	1.00	1.0	1.00	1.00	1,100.	.453	.109	28.6
307.00	1.00	1.0	1.00	1.00	1,070.	.443	.105	28.4
3.00	1.00	1.0	1.00	1.00	1,120.	.426	.106	28.6
3.75	1.00	1.0	1.00	1.00	1,130.	.437	.109	28.4
3.87	1.00	1.0	1.00	1.00	1,050.	.442	.102	27[illegible]
5.96	1.00	1.0	1.00	1.00	1,030.	.453	.103	
7.58	1.00	1.0	1.00	1.00	1,090.	.437	.105	
11.60	1.00		1.00	1.00	1,080.	.454	.1[illegible]	
17.50	[illegible]		[illegible]	1.00	1,090.	.454		
2.33				1.00	961.	.448		
208.00				1.00	1,030.	.43[illegible]		
[illegible]				[illegible]0	1,130.			
					1,100.			
					1,090			

TABLE 35. HISTOGRAM OF EFFICIENCY AT P_{MAX}* VS CELLS (500 CELLS)



*P_{MAX} determined from AM-1 I-V curve - cells AR coated.

2. Qualification Testing

In order to obtain accurate and reproducible values of cell parameters, the output illumination level from the Oriel filtered xenon light source must be adjusted to the AM-1 level for each measurement. A better approach for high-speed measurements is to set the output level to AM-1, monitor it with a small standard cell, and correct the data for any change in light level. This latter approach was taken by placing a small (1.3 cm^2) silicon cell adjacent to the cell under test as shown in Fig. 75.

The initial level is set by using a calibrated silicon cell* and a set of measurements was made and compared to those obtained on a previously calibrated ELH lamp simulator. The results of such a comparison are shown in Table 36, where it is seen that good agreement between the two sets of values are obtained with the difference in short-circuit current in all cases less than 3.8%.

3. Temperature Corrections

The temperature beneath the cell under test is measured by means of a thermocouple permanently mounted in the stage. This value is recorded for each measurement and the cell parameters V_{oc}, FF and η are corrected back to 25°C using the following equations:

$$V_{ocT} = V_{oc} + S\ (T-25) \tag{7}$$

where $S = 0.002$ V/°C

$$EFF_T = \eta_T = \eta + \varepsilon\ (T-25) \tag{8}$$

where $\varepsilon = 0.04$ %/°C

and

$$FF = \frac{FF\ [1 + \varepsilon/\eta\ (T-25)]}{[1 + S/V_{oc}\ (T-25)]} \tag{9}$$

A typical set of measured and corrected parameters is illustrated in Table 37.

*Reference standard cell No. 49, provided by NASA Lewis Research Center, Cleveland, OH.

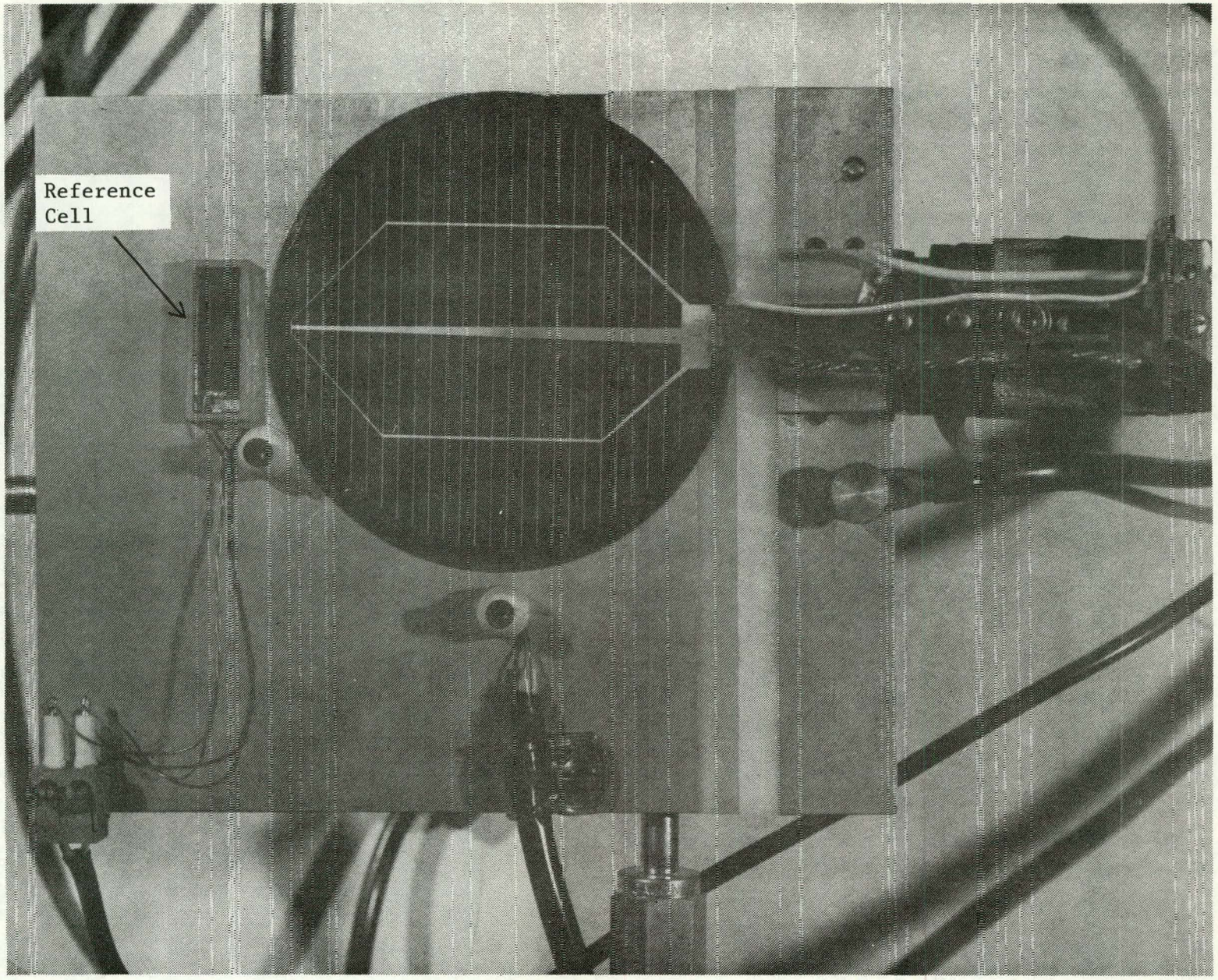


Figure 75. Photograph of cell-testing stage showing reference cell mounted adjacent to the cell under test.

TABLE 36. COMPARISON OF CELL PARAMETERS ELH VS ORIEL AM-1 SIMULATION SYSTEM

Sample	V_{oc} (mV)	I_{sc} (mA)	V_m (mV)	I_m (mA)	FF -	η (%)
1 ELH	599	865	490	800	0.760	9.58
1 ORIEL	585	871	481	804	0.758	9.43
2 ELH	591	885	470	810	0.728	9.26
2 ORIEL	583	888	457	800	0.707	8.93
3 ELH	592	880	475	810	0.739	9.36
3 ORIEL	583	886	456	824	0.727	9.17
4 ELH	591	865	485	820	0.768	9.56
4 ORIEL	582	870	471	811	0.753	9.31
5 ELH	592	870	485	801	0.754	9.45
5 ORIEL	581	869	462	814	0.745	9.17
6 ELH	591	811	485	762	0.771	9.0
6 ORIEL	579	842	466	790	0.754	9.0
7 ELH	590	802	480	750	0.762	8.76
7 ORIEL	580	822	476	770	0.769	8.9
8 ELH	581	810	475	752	0.759	8.69
8 ORIEL	574	818	475	760	0.769	8.8
9 ELH	592	820	490	759	0.767	9.05
9 ORIEL	581	820	479	765	0.769	8.93
10 ELH	586	795	485	730	0.760	8.61
10 ORIEL	574	810	471	748	0.758	9.59
11 ELH	591	855	485	791	0.759	9.33
11 ORIEL	581	847	466	792	0.750	9.00

C. SOLAR-CELL PROCESSING

The following section deals with tests conducted to assure the proper operation of equipment, presents some results which relate to the production of ion-implanted solar cells, and gives a description of the initial performance of such cells made in accordance with the manufacturing sequences shown in Figs. 71 and 72.

TABLE 37. TEMPERATURE CORRECTIONS OF CELL PARAMETERS

CELL NUMBER	VOC	VOT	ISC	FF	FFT	EFF	EFFT	BT	IRR
OCLI004001	.580	.582	1,240.	.702	.702	.113	.113	25.9	99.6
OCLI004002	.578	.581	1,230.	.677	.677	.108	.109	26.3	99.1
OCLI004003	.579	.581	1,220.	.697	.697	.109	.109	26.1	100.0
OCLI004004	.579	.582	1,250.	.683	.683	.109	.110	26.4	100.0
OCLI004005	.577	.580	1,240.	.683	.683	.109	.110	26.3	99.5
OCLI004006	.579	.583	1,240.	.690	.690	.110	.111	26.8	100.0
OCLI004007	.577	.581	1,240.	.682	.682	.108	.109	26.9	100.0
OCLI004008	.576	.580	1,260.	.670	.670	.109	.110	27.0	99.3
OCLI004009	.571	.573	1,170.	.683	.683	.102	.102	26.0	99.8
OCLI004010	.573	.576	1,190.	.679	.679	.104	.105	26.3	99.6
OCLI004011	.567	.570	1,130.	.675	.676	.096	.097	26.5	100.0
OCLI004012	.577	.580	1,200.	.697	.697	.107	.108	26.7	100.0
OCLI004013	.577	.581	1,240.	.664	.664	.105	.106	26.8	100.0
OCLI004014	.577	.581	1,220.	.697	.697	.109	.110	26.9	100.0
OCLI004015	.569	.572	1,180.	.671	.671	.100	.101	26.5	99.6
OCLI004016	.576	.580	1,170.	.713	.713	.107	.108	26.9	100.0
OCLI004017	.576	.580	1,300.	.676	.676	.113	.114	26.9	99.6
OCLI004018	.575	.579	1,250.	.694	.694	.111	.112	26.9	100.0
OCLI004019	.576	.580	1,240.	.698	.698	.111	.112	27.1	100.0
OCLI004020	.576	.580	1,230.	.692	.692	.110	.111	27.1	99.8
OCLI004021	.566	.570	1,160.	.686	.687	.100	.101	27.1	100.0
OCLI004022	.578	.582	1,210.	.728	.728	.113	.114	27.2	100.0
OCLI004023	.577	.582	1,230.	.699	.699	.110	.111	27.6	100.0
OCLI004024	.577	.582	1,240.	.707	.707	.113	.114	27.7	99.8
OCLI004025	.576	.581	1,220.	.703	.703	.109	.110	27.5	100.0
OCLI004026	.566	.571	1,160.	.686	.687	.100	.101	27.6	99.7
OCLI004027	.576	.581	1,230.	.701	.701	.110	.111	27.7	100.0
OCLI004028	.569	.575	1,160.	.720	.720	.106	.107	27.8	100.0
OCLI004029	.575	.581	1,250.	.670	.670	.107	.108	27.8	101.0
OCLI004030	.569	.574	1,170.	.716	.716	.106	.107	27.7	100.0
OCLI004031	.569	.574	1,130.	.684	.685	.098	.099	27.5	100.0
OCLI004032	.573	.578	1,200.	.726	.726	.110	.111	27.5	100.0
OCLI004033	.574	.580	1,200.	.730	.730	.112	.113	27.8	100.0
OCLI004034	.575	.580	1,160.	.748	.748	.111	.112	27.6	99.9
OCLI004035	.569	.575	1,150.	.716	.717	.104	.105	27.8	99.9
OCLI004036	.575	.580	1,220.	.693	.693	.108	.109	27.6	99.9
OCLI004037	.572	.578	1,190.	.696	.697	.105	.106	27.8	100.0
OCLI004038	.573	.579	1,240.	.692	.692	.109	.110	27.8	100.0
OCLI004039	.576	.582	1,220.	.703	.703	.109	.110	27.8	101.0
OCLI004040	.575	.581	1,230.	.709	.709	.111	.112	27.8	100.0
OCLI004041	.571	.577	1,170.	.707	.708	.105	.106	27.8	100.0
OCLI004042	.570	.576	1,180.	.711	.711	.106	.107	28.0	100.0
OCLI004043	.573	.579	1,210.	.716	.716	.110	.111	27.9	100.0
OCLI004044	.573	.579	1,230.	.685	.685	.107	.108	28.0	100.0
OCLI004045	.573	.580	1,200.	.691	.692	.104	.105	28.3	101.0
OCLI004046	.573	.580	1,200.	.705	.705	.108	.109	28.4	100.0
OCLI004047	.574	.581	1,220.	.704	.704	.109	.110	28.5	100.0
OCLI004048	.574	.581	1,210.	.707	.707	.109	.110	28.5	100.0
OCLI004049	.574	.581	1,250.	.686	.686	.108	.109	28.4	102.0
OCLI004050	.574	.581	1,240.	.680	.680	.107	.108	28.4	101.0

TABLE 37. (Continued)

CELL NUMBER	VOC	VOT	ISC	FF	FFT	EFF	EFFT	ST	IRR
OCLI004051	.575	.580	1,210.	.708	.708	.107	.108	27.5	102.0
OCLI004052	.574	.580	1,190.	.713	.713	.106	.107	27.6	102.0
OCLI004053	.570	.576	1,220.	.637	.638	.098	.099	28.0	101.0
OCLI004054	.571	.577	1,190.	.699	.700	.105	.106	28.1	101.0
OCLI004055	.573	.579	1,220.	.693	.693	.107	.108	28.1	100.0
OCLI004056	.575	.581	1,260.	.682	.682	.109	.110	28.1	101.0
OCLI004057	.572	.578	1,200.	.710	.710	.108	.109	28.0	101.0
OCLI004058	.574	.580	1,250.	.699	.699	.111	.112	28.0	100.0
OCLI004059	.568	.574	1,190.	.692	.693	.104	.105	28.0	100.0
OCLI004060	.574	.580	1,240.	.691	.691	.108	.109	28.2	101.0
OCLI004061	.572	.578	1,250.	.671	.671	.106	.107	28.0	100.0
OCLI004062	.574	.580	1,230.	.716	.716	.112	.113	28.1	99.9
OCLI004063	.574	.580	1,190.	.731	.731	.110	.111	28.2	101.0
OCLI004064	.573	.579	1,160.	.724	.724	.108	.109	27.9	101.0
OCLI004065	.571	.577	1,200.	.689	.690	.105	.106	28.1	100.0
OCLI004066	.574	.580	1,220.	.700	.700	.108	.109	28.2	101.0
OCLI004067	.574	.580	1,200.	.694	.695	.106	.107	28.2	101.0
OCLI004068	.574	.581	1,190.	.736	.736	.112	.113	28.4	99.9
OCLI004069	.574	.581	1,200.	.720	.720	.109	.110	28.3	101.0
OCLI004070	.570	.577	1,190.	.699	.700	.105	.106	28.6	100.0
OCLI004071	.572	.579	1,240.	.671	.672	.106	.107	28.4	99.9
OCLI004072	.574	.581	1,240.	.692	.692	.109	.110	28.6	100.0
OCLI004073	.568	.575	1,160.	.704	.705	.102	.103	28.4	101.0
OCLI004074	.567	.573	1,140.	.721	.722	.103	.104	27.9	101.0
OCLI004075	.572	.578	1,210.	.688	.689	.105	.106	28.2	100.0
OCLI004076	.573	.579	1,210.	.706	.706	.109	.110	28.2	99.9
OCLI004077	.573	.580	1,240.	.696	.696	.110	.111	28.3	99.9
OCLI004078	.565	.572	1,120.	.681	.682	.095	.096	28.4	100.0
OCLI004079	.568	.575	1,190.	.665	.666	.100	.101	28.4	100.0
OCLI004080	.573	.580	1,230.	.708	.708	.111	.112	28.6	100.0
OCLI004081	.573	.580	1,200.	.721	.721	.110	.111	28.7	100.0
OCLI004082	.571	.578	1,210.	.691	.692	.105	.106	28.7	101.0
OCLI004083	.572	.579	1,240.	.692	.692	.109	.110	28.6	99.9
OCLI004084	.570	.577	1,180.	.723	.724	.106	.107	28.6	102.0
OCLI004085	.573	.580	1,240.	.707	.707	.111	.112	28.7	101.0
OCLI004086	.572	.579	1,210.	.704	.704	.107	.108	28.6	101.0
OCLI004087	.571	.578	1,210.	.709	.709	.109	.110	28.5	100.0
OCLI004088	.567	.574	1,150.	.688	.689	.099	.100	28.5	100.0
OCLI004089	.570	.577	1,160.	.733	.733	.108	.109	28.6	99.9
OCLI004090	.569	.576	1,150.	.739	.740	.106	.107	28.6	101.0
OCLI004091	.571	.578	1,240.	.698	.698	.109	.110	28.7	101.0
OCLI004092	.569	.576	1,190.	.696	.697	.104	.105	28.7	100.0
OCLI004093	.570	.578	1,190.	.713	.713	.108	.110	28.8	100.0
OCLI004094	.568	.575	1,150.	.704	.705	.102	.103	28.7	100.0
OCLI004095	.567	.575	1,160.	.689	.690	.100	.102	28.8	101.0
OCLI004096	.567	.575	1,130.	.725	.726	.104	.106	28.8	100.0
OCLI004097	.574	.581	1,240.	.712	.712	.112	.113	28.7	100.0
OCLI004098	.568	.576	1,190.	.701	.702	.105	.107	28.9	100.0
OCLI004099	.568	.576	1,150.	.720	.721	.104	.106	28.8	100.0
OCLI004100	.573	.580	1,220.	.694	.695	.107	.108	28.7	101.0

1. Equipment and Process Qualification

Preliminary to running ion-implanted solar cells of sequences I, II, and III through production-model screen printing and spray-on AR coating, these processes were tested on 3-in.-diameter solar-cell wafers containing a junction formed by $POCl_3$ diffusion. This was done because the performance level of such cells had previously been established on laboratory versions of this equipment.

These tests were performed on a group of 37, 3-in.-diameter solar-cell wafers split into two lots containing 12 and 25 cells. In the first lot of 12 wafers, six were screen printed on the sun-side with a previously used grid pattern having 14% shadowing and six with our new grid design [20] (9% shadowing). In the second lot, all wafers were printed with the new mask. In all cases, TFS* 3347 silver ink was used on the junction side and RCA p-type [19] on the back (84% coverage on the back). Examination of the new grid pattern after printing revealed good line definition; the minimum designed line width (0.005 in.) printed with an average width of 5-1/2 mil. After firing at 675°C for 2 min between dual infrared lamps, these lines slumped at the edges, yielding a line of ~0.006-in. width.

After firing, the AM-1 illuminated cell parameters were measured, and the statistical results comparing grid patterns are summarized in Table 38. The cell characteristics for both patterns are very good; for the new grid, no significant reduction in fill factor was experienced, and a 6% increase in short-circuit current was obtained, as expected. Similarly good results were obtained on the 25-wafer lot as illustrated in the following data:

$\overline{J_{sc}}^{*}$	σ_i^{**}	$\overline{V_{oc}}$	σ_v	$\overline{FF}$	σ_F	$\bar{\eta}$	σ_n	$J_{sc\ max}$	$V_{oc\ max}$	FF_{max}	η_{max}
(mA/cm^2)	(mA/cm^2)	(mV)	(mV)	-	-	(%)	(%)	(mA/cm^2)	(mV)	-	(%)
20.7	0.35	579	2.1	0.761	0.007	9.23	0.15	21.5	586	0.772	9.66

*Cell area = 42 cm^2, no AR coating.
**σ_i = standard deviation of ith parameter.

20. R. V. D'Aiello, Automated Array Assembly, Phase II, Quarterly Report No. 5, prepared under Contract No. 954868 for Jet Propulsion Laboratory, DOE/JPL-954868-79/2, March 1979.

*Thick Film Systems, Inc., Santa Barbara, CA.

TABLE 38. AVERAGE AND STANDARD DEVIATION FOR ALL PARAMETERS OF SCREEN-PRINTED CELLS*

Grid Pattern	$\overline{J_{sc}}$ (mA/cm^2)	σ_j (mA/cm^2)	$\overline{V_{oc}}$ (mV)	σ_v (mV)	$\overline{FF}$ -	σ_F -	$\bar{\eta}$ *	σ_n	$J_{sc\ max}$ (mA/cm^2)	$V_{oc\ max}$ (mV)	FF_{max} -	η_{max} ** (%)
Old (No AR)	19.9	0.57	588	4.5	0.763	0.008	8.89	0.30	20.9	592	0.769	9.33
New (No AR)	21.1	0.65	593	3.1	0.754	0.017	9.37	0.22	21.6	599	0.771	9.56

*Cell area = 41 cm^2

**No AR coating

+σ = standard deviation

These cells were spray AR coated with the RCA I TiO_2 solution using the Zicon Model 9000 autocoater as previously described [20]. Typical results before and after coating are shown in Table 39. The coated-cell parameters are reasonably good; however, the uniformity and film quality were found to be sensitive to the ambient relative humidity (RH) for values of RH greater than ~45%.

TABLE 39. COMPARISON OF AVERAGE AM-1 PARAMETERS BEFORE AND AFTER SPRAY AR COATING

	$\overline{J_{sc}}$ (mA/cm^2)	$\overline{V_{oc}}$ (mV)	$\overline{FF}$ -	$\overline{\eta}$ (%)	$J_{sc\ max}$ (mA/cm^2)	$V_{oc\ max}$ (mV)	FF_{max} -	η_{max} (%)
Before	21.1	593	0.754	9.37	21.6	599	0.771	9.56
After	28.7	601	0.752	12.65	29.3	610	0.761	13.2

The model 9000 Zicon autocoater was used to spray the RCA I AR coating solution on several lots of cells to establish baseline performance. Typical values of short-circuit current before and after the AR coating process are given in Table 40. The average increase in short-circuit current is +31% which is 4% lower than our previous experience [19]. Some nonuniformity in film thickness was noted, especially near the metal, causing individual values (samples 910-7, 910-11, and 910-12) to be lower than expected.

Additional analyses have been carried out to determine the structure and refractive index of the RCA I derived TiO_2 (more realistically TiO_x) coating and the Emulsitone* C TiO_2-SiO_2 coating as a function of heat-treatment time at 400°C. Electron diffraction indicated an amorphous structure of the TiO_2-SiO_2 coating and of the TiO_x coating heated for only 30 s which is our normal heat treatment. After the TiO_x film was heated for 5.5 and 55 min, a crystalline TiO_2 phase appeared which was identified as Anastase. The refractive index was measured by ellipsometry. These results are presented graphically in Fig. 76. The TiO_x film reaches a constant refractive index value of 2.22 after the 5.5- or 55-min heat treatment, indicating a stable film structure. The TiO_2-SiO_2 film, on the other hand, keeps increasing in refractive index with heating time.

*Emulsitone Company, Whippany, NJ.

TABLE 40. SHORT-CIRCUIT CURRENT BEFORE AND AFTER SPRAY AR PROCESS FOR LOT 910

Cell No.	$I_{sc\ No\ AR}$ (mA)	$I_{sc\ AR}$ (mA)	$\Gamma = \frac{I_{sc\ AR}}{I_{sc\ No\ AR}}$ -
910 - 1	875	1170	1.34
910 - 2	870	1150	1.32
910 - 3	890	1180	1.33
910 - 4	842	1090	1.29
910 - 5	848	1170	1.38
910 - 6	869	1150	1.32
910 - 7	906	1150	1.27
910 - 8	871	1140	1.31
910 - 9	849	1110	1.31
910 - 10	864	1200	1.39
910 - 11	870	1050	1.21
910 - 12	909	1150	1.27
910 - 13	875	1170	1.34
910 - 14	881	1130	1.29
			Ave. 1.31

Absolute reflection of the RCA I TiO_x coating on polished silicon slices as a function of wavelength for the 30-s heat-treatment period is shown in Fig. 77. A broad reflection minimum of 1.3% is reached at a wavelength of 6000 Å. A measurement of the transmittance of the coating on a quartz substrate gives a measure of the absorption. Such measurements for films heat-treated at 0.5, 5, and 50 min are shown in Fig. 78 where it can be seen that there is no significant absorption down to a wavelength of 0.37 μm.

These tests have established the material requirements and operating conditions for the screen-printing and spray-on AR coating processes.

2. Ion Implantation and Furnace Annealing

The three manufacturing sequences to be studied require the formation of a junction by ion implantation and furnace annealing. A lot of 100 "solar-grade" wafers was processed through ion implantation and furnace annealing,

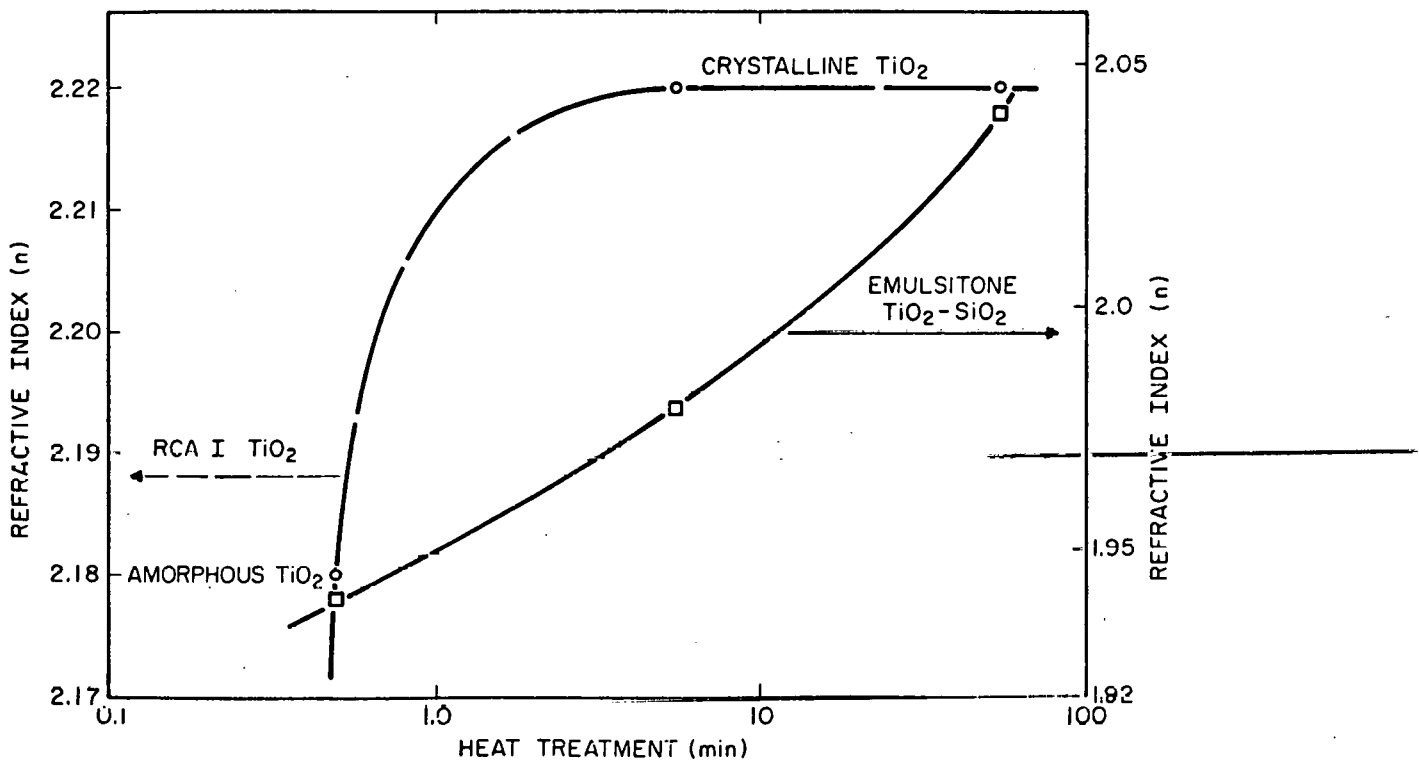


Figure 76. Refractive index vs heat treatment time at 400°C.

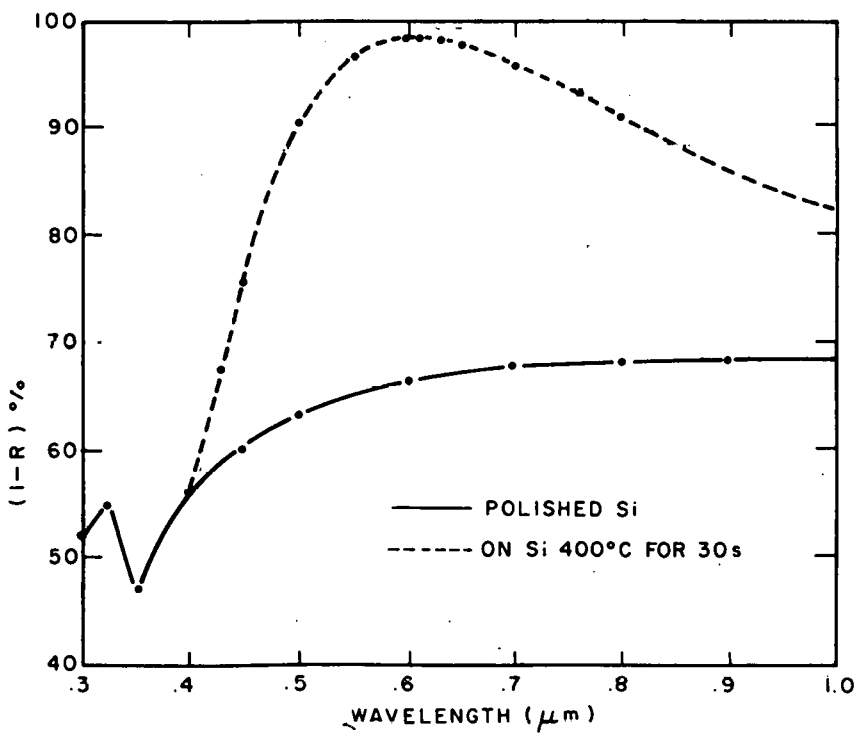


Figure 77. Reflection spectrum for spray-on AR film on silicon.

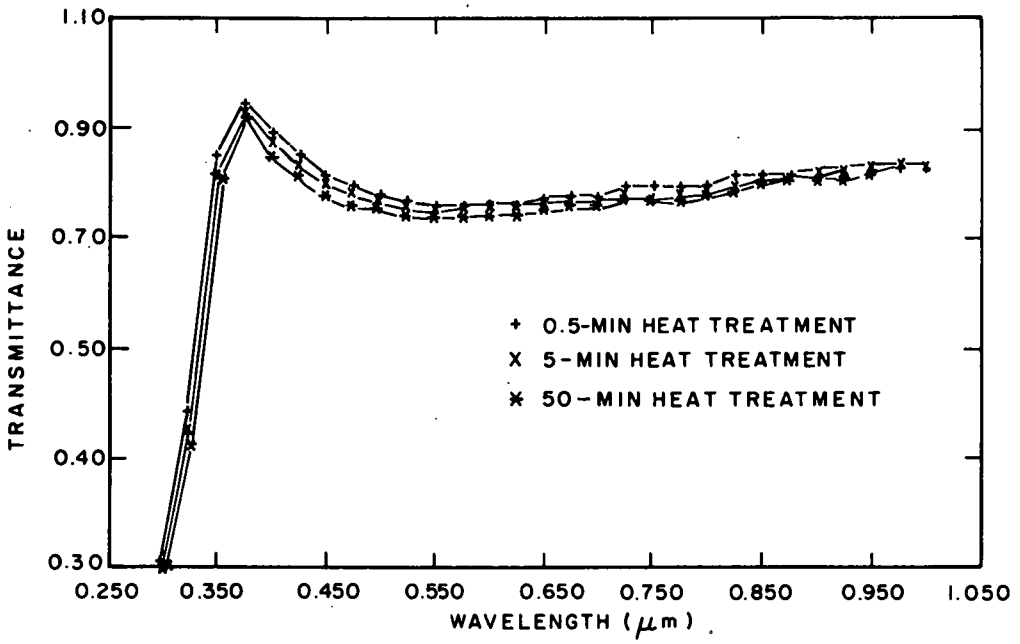


Figure 78. Transmittance data.

and the distribution of junction-layer sheet resistances was measured prior to screen printing the contacts. These wafers were implanted with 2×10^{15} A/cm^2, ^{31}P followed by a three-step (500°C, 2 h; 850°C, 30 min; 500°C, 2 h) furnace anneal. The distribution of measured sheet resistances is shown in Fig. 79. Both the average value (95 Ω/□) and the spread are higher than previously experienced under similar dose and furnace conditions. However, ion-implanted layers are normally capped with an SiO_2 film to prevent impurity contamination and/or out-diffusion of the phosphorus during the high-temperature anneal, and these wafers were not capped because the capping step was not considered to be cost-effective.

The wide range (75 to 194 Ω/□) of sheet resistance values made this lot suitable for testing the sensitivity of the screen-printing and firing process to the absolute value of sheet resistance. Twenty-five wafers were selected from the lot and were screen-printed and fired as described in subsection C.1 above. The cell characteristics were measured and are listed in Table 41 along with the sheet-resistance values for each cell. It is seen from these data that the fill factors are low and decrease almost monotonically with increasing sheet resistance as shown in Fig. 80. The grid metallization pattern

Figure 79. Distribution of sheet resistance for lots 950, 951, and 952.

is designed for sheet resistivities slightly greater than 100 Ω/□. Thus, the effect shown in Fig. 80 is not due simply to the increased sheet resistivity, but rather results from the interaction of the present screen-printed metallization process and the silicon surface.

It can be concluded from these data that junction layers formed in solar-grade wafers with a phosphorus dose of 2×10^{15} A cm^{-2} and annealed in the manner described are not compatible with the present thick-film screen-printing process. The results of increasing the phosphorus dose level and adjustments in the annealing temperature are described below.

3. Adjustments to Implant Parameters Based on Initial Tests

Based on the results described above, adjustments were made in the phosphorus dose and/or anneal schedule in order to reduce the resultant sheet resistance of the junction layer. Three lots of 25 wafers each were formed; Table 42 shows the conditions for furnace annealing and ^{31}P dose along with the average sheet resistance obtained after annealing. Figures 81, 82, and 83 show that the spread in the distribution of measured sheet resistance is very much less than that obtained with both a lower ^{31}P dose and anneal temperature as described above.

TABLE 41. AM-1 PARAMETERS FOR LOTS 950, 951, and 952

CELL NUM	OPEN CIR VOLT	CELL CURRENT	MAX POWER	FILL FACT	SER RESIS	SHEET RESIS	SHUNT RESIS	PMAX CURRENT	PMAX VOLT	EFF	BASE TEMP
D1NS950001	.531	826.	6.47	.620	.107	74	11.40	707.	.384	.066	27.3
D1NS950003	.518	810.	6.05	.606	.114	77	19.80	680.	.373	.061	27.3
D1NS950004	.514	790.	5.52	.571	.137	82	399.00	650.	.357	.056	27.8
D1NS950005	.527	780.	5.94	.607	.121	83	22.60	639.	.390	.060	27.9
D1NS950006	.533	785.	6.00	.605	.127	85	7.21	645.	.391	.061	28.2
D1NS950007	.527	821.	5.88	.572	.128	86	99.00	651.	.380	.060	28.2
D1NS950008	.525	782.	5.81	.595	.126	89	11.20	636.	.384	.059	28.3
D1NS950009	.531	803.	5.85	.576	.140	91	6.37	648.	.379	.060	28.3
D1NS950010	.512	808.	5.58	.567	.131	94	32.30	637.	.368	.057	28.3
D1NS951001	.528	796.	5.67	.568	.139	98	8.74	619.	.385	.058	27.8
D1NS951002	.426	859.	4.25	.488	.174	104	4.07	652.	.274	.044	28.0
D1NS951003	.324	742.	1.52	.336	.298	108	.76	449.	.179	.020	28.1
D1NS951004	.518	855.	5.26	.499	.164	114	12.90	617.	.358	.054	28.2
D1NS951005	.506	820.	5.20	.527	.146	118	8.70	609.	.359	.053	28.3
D1NS952001	.521	832.	4.78	.464	.223	119	3.35	600.	.335	.049	27.9
D1NS952002	.512	839.	5.03	.492	.162	121	7.56	631.	.335	.052	28.3
D1NS952003	.405	870.	4.09	.487	.162	122	3.34	654.	.263	.042	28.3
D1NS952004	.426	873.	4.09	.464	.191	124	4.48	654.	.263	.042	28.4
D1NS952005	.495	836.	4.60	.467	.191	126	4.53	597.	.324	.047	28.5
D1NS952006	.497	804.	4.49	.472	.206	132	3.80	582.	.324	.046	28.4
D1NS952007	.510	799.	4.75	.490	.195	139	6.36	595.	.335	.049	28.5
D1NS952008	.463	866.	4.66	.490	.171	141	3.16	637.	.307	.048	28.5
D1NS952009	.275	848.	2.31	.417	.162	144	2.62	574.	.169	.025	28.7

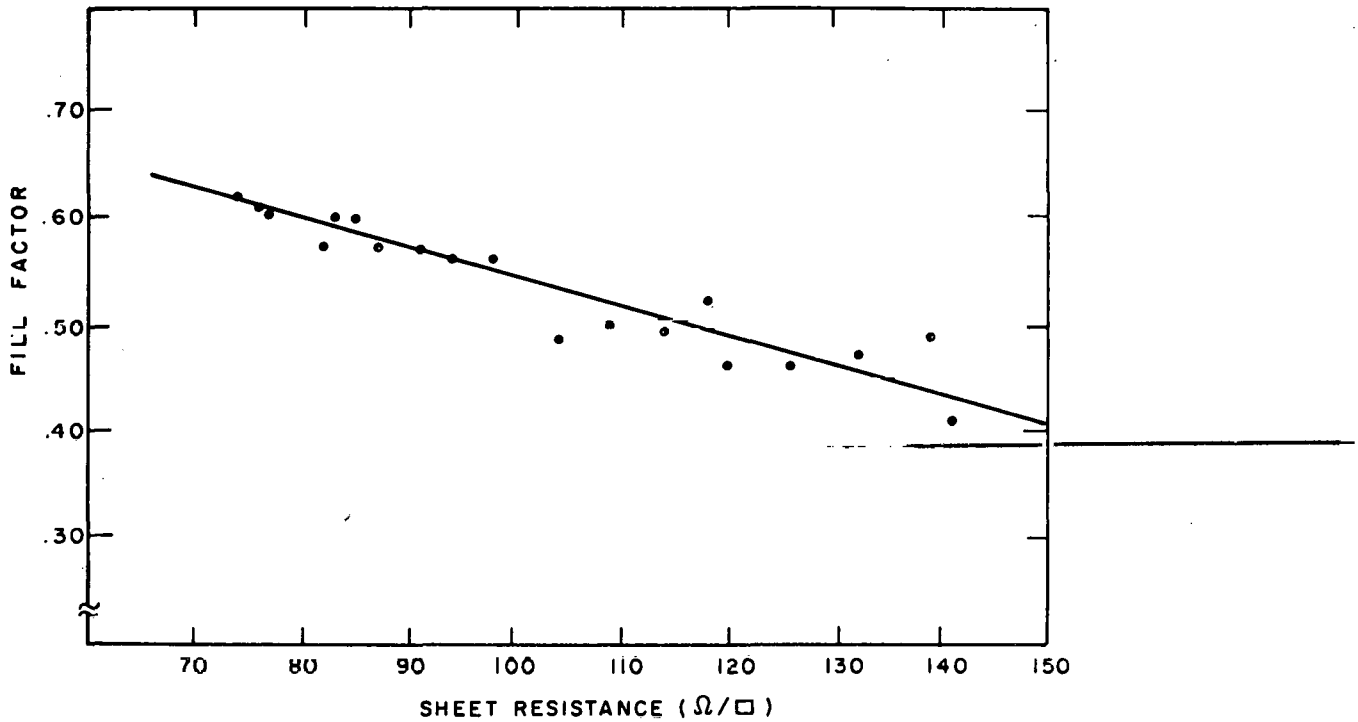


Figure 80. Measured fill factor as a function of sheet resistance for lots 950, 951, and 952.

TABLE 42. ^{31}P DOSE AND ANNEAL CONDITIONS FOR THREE LOTS OF SOLAR-CELL WAFERS

Lot No.	^{31}P Dose (A/cm^2)	Furnace Anneal	$\bar{R}_{\square}$ ($\Omega/\square$)
107P	$4x10^{15}$	L* 850°C L 30 min	58
106P	$4x10^{15}$	L 950°C L 30 min	34
910P	$2x10^{15}$	L 950°C L 30 min	52

*L = 500°C, 2 h

After screen printing and firing, the cell characteristics for the three lots were measured. Table 43 lists the average values of the AM-1 illuminated cell parameters along with the average for lots 950, 951, and 952. Clearly, a significant improvement in cell characteristics, especially in the fill

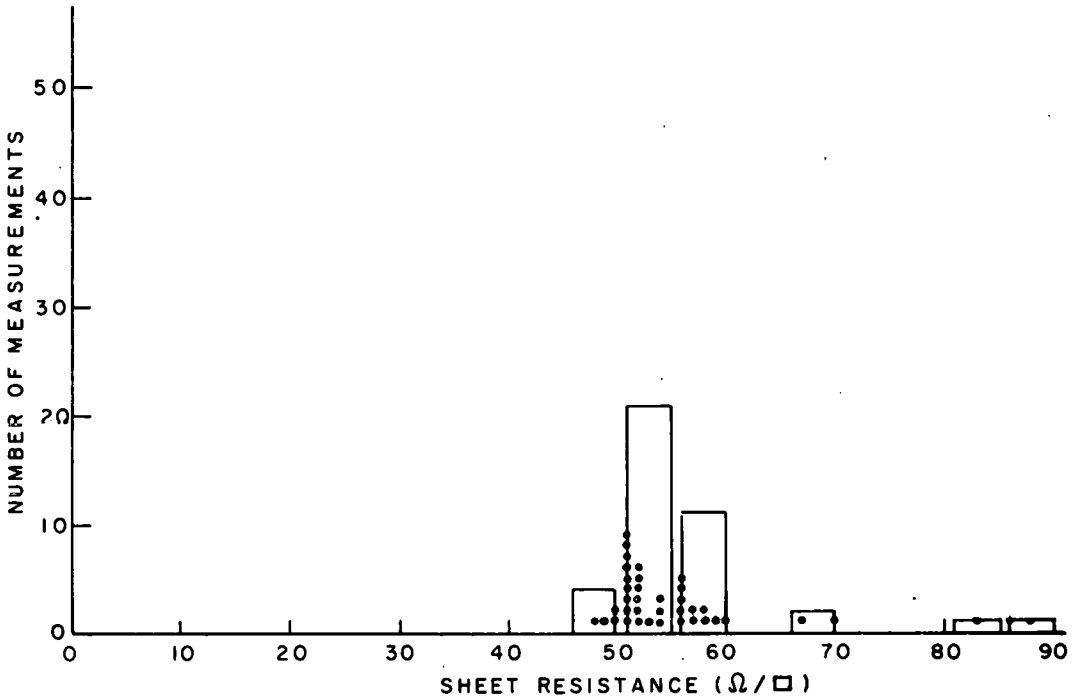


Figure 81. Distribution of sheet resistance for wafers of lot 907P.

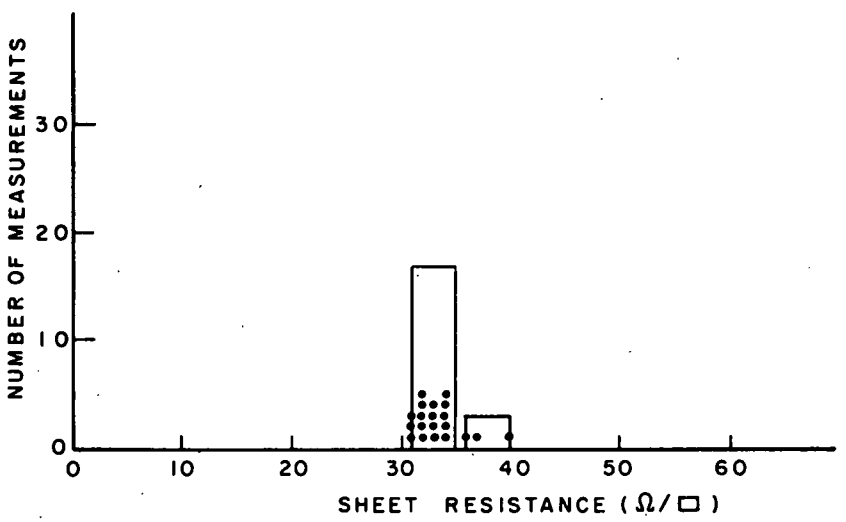


Figure 82. Distribution of sheet resistance for wafers of lot 106P.

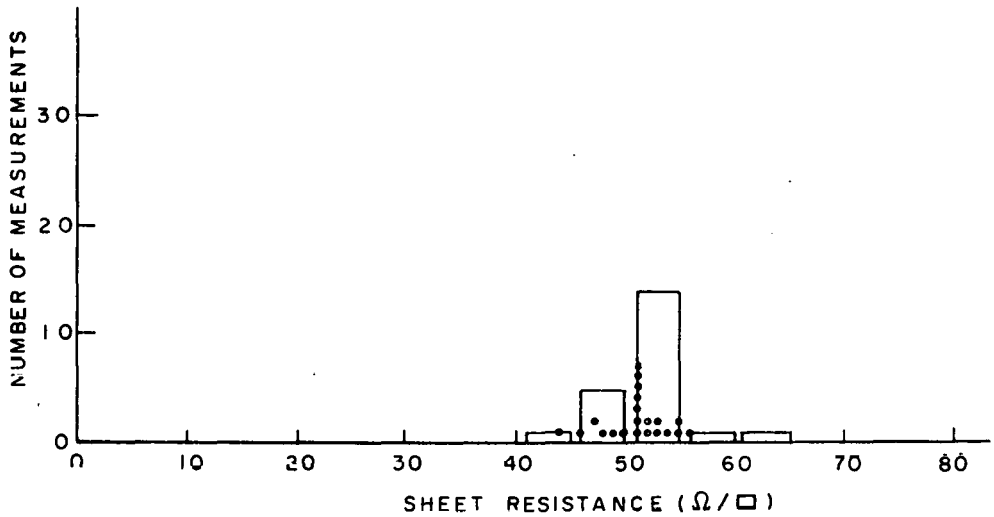


Figure 83. Distribution of sheet resistance for wafers of lot 910P.

TABLE 43. AVERAGE AM-1 ILLUMINATED CELL PARAMETERS FOR THE WAFER LOTS OF TABLE 42.

Lot No.	$\overline{J_{sc}}$ (mA/cm^2)	$\overline{V_{oc}}$ (mV)	$\overline{FF}$ -	$\bar{\eta}$* (%)	$\overline{R_{\square}}$ (Ω/□)
107P	21.7	552	0.659	7.9	58
106P	20.7	557	0.710	8.2	34
910P	20.5	560	0.700	8.0	52
950 - 952	19.5	499	0.518	5.1	75-150

*No AR Coating

factor, is obtained when the surface layer sheet resistance is lowered. It is interesting to compare the fill factors obtained on all lots processed as an extension to the data shown in Fig. 80. In Fig. 84, an extended linear fit to the data of Fig. 80 is shown and data points showing the average value of fill factor for all other lots are plotted.

To investigate this problem further, an experimental test matrix was formed involving a combination of starting wafers, implant and anneal conditions, and

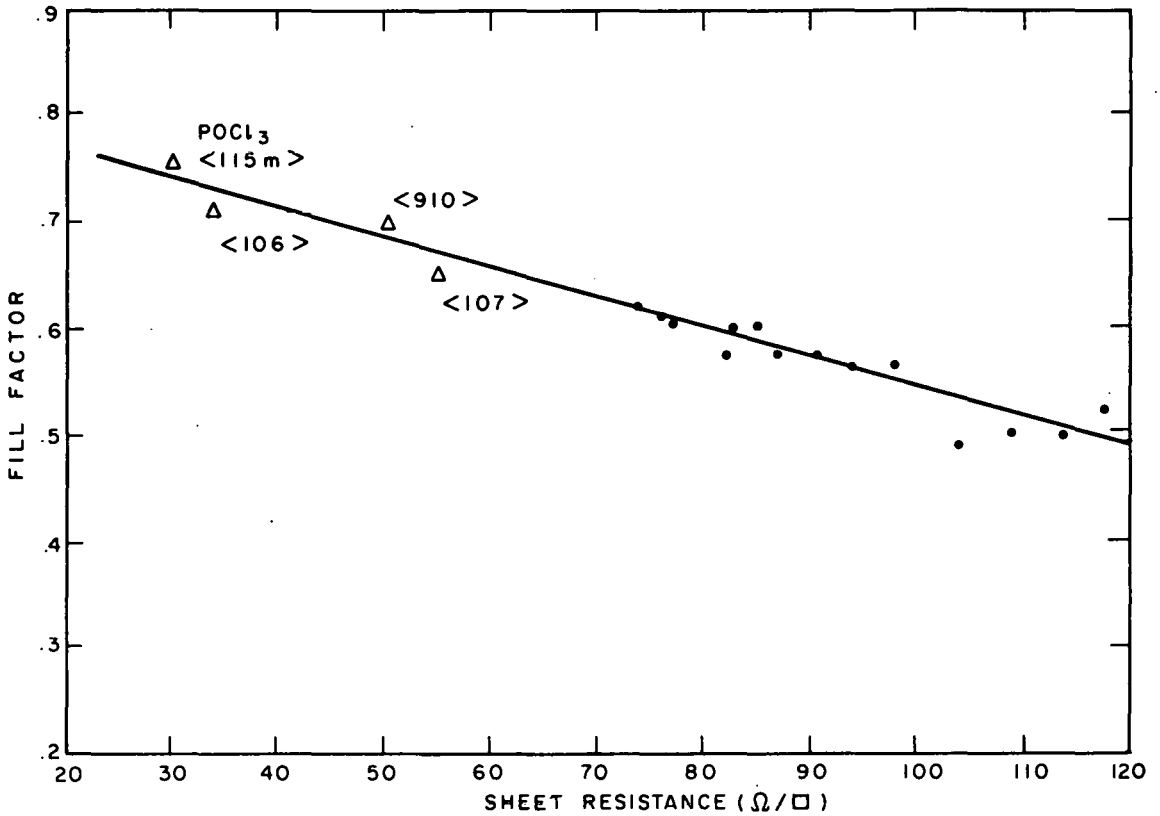


Figure 84. Fill factor as a function of sheet resistance including average values for lots 106, 107, 910, and 115m.

the addition of junction layers formed by $POCl_3$ diffusion. The conditions for this experiment are shown in Table 44 along with the post-anneal values of average sheet resistance for each lot of 25 wafers. Solar cells were completed for each lot by screen-printing and firing with the ink combinations given in the last two columns of Table 44.

The average AM-1 solar-cell parameters measured for each lot are listed in Table 45. From these results, the following conclusions can be drawn:

(1) For ^{31}P ion-implanted junctions, the 950°C anneal and $4x10^{15}$ cm^{-2} dose are preferred for best cell parameters.

(2) $POCl_3$ diffused-junctions yield the best overall solar-cell performance.

(3) Under the same implant and anneal conditions, the resultant sheet resistance is higher for solar-grade wafers than for polished or etched CZ wafers.

(4) Even when the sheet-resistance values obtained with ion-implanted solar-grade wafers approach those for $POCl_3$ diffused junctions, the solar-cell parameters (V_{oc} and FF) are not equally as good.

TABLE 44. TEST-MATRIX CONDITIONS

Lot, Material	Wafer Surface	Wafer Resistivity (Ω-cm)	^{31}P Implant Dose (cm^{-2})	Furnace Anneal	Sheet Resistance (Ω/□)	Screen-Print Ink Front	Screen-Print Ink Back
910P, SG*	Etched	2	$2x10^{15}$	L** 950°C 30 min L	52	TFS 3347	Al/Ag
107P, SG	Etched	2	$4x10^{15}$	L 850°C 30 min L	58		
106P, SG	Etched	2	$4x10^{15}$	L 950°C 30 min L	34		
121, Wacker CZ	Polished	1.5	$4x10^{15}$	L 950°C 30 min L	25		
123, Monsanto CZ	Etched	12	$4x10^{15}$	L 950°C 30 min L	27		
115m, Monsanto CZ	Etched	1.5	$POCl_3$ diffusion	850°C 60 min -	30		

*SG = Solar Grade
** L = 500°C, 2 h

TABLE 45. RESULTS OF TEST MATRIX

Lot	$R_{\square}$ ($\Omega/\square$)	$\overline{J_{sc}}$ (mA/cm^2)	$\overline{V_{oc}}$ (mV)	$\overline{FF}$	$\overline{\eta}$* (%)
910P	52	20.5	560	0.700	8.0
107P	58	21.7	552	0.659	7.9
106P	34	20.7	557	0.710	8.2
121	25	19.3	553	0.743	7.9
123	27	19.6	518	0.698	7.1
115m	30	20.7	580	0.761	9.2

* No AR coating.

Based on these results, we increased the ^{31}P dose to $4x10^{15}$ cm^2 and changed the high temperature anneal to 950°C, 30 min for all subsequent process lots in sequences I and II. This is a compromise in favor of forming lower resistance screen-printed contacts to the n^+ layer since higher short-circuit current is expected, and does result (see lot 107P in Table 45) from a lower temperature anneal. In addition to a possible reduction in cell efficiency which implies greater cost per watt, the requirement for increased implant dose would require implanters of higher beam current or greater capacity to attain the same throughput.

4. Application of Selected Processes to Dendritic Web Silicon

A quantity of dendritic web silicon was purchased from Westinghouse to assess the compatibility of a sheet form of silicon with selected process steps for which problems relating to the mechanical properties of sheet forms were anticipated. The processing steps examined here are listed in Table 46 along with our comments related to the handling or processing experienced. It should be noted that with the exception of the construction and use of a modified platen for the screen printer, no special equipment or modifications were made for handling or processing the web.

The web was received in 30-cm-long sections. The nominal width of most samples was 3 cm with some at 2 cm. These sections were tapered with typical

TABLE 46. PROCESSES APPLIED TO DENDRITIC WEB

Process	Comment
General Handling	Retention of dendrite rails provides mechanical stability. Minimizes manual handling.
Cleaning	Removal of yellow-brown film on the surface requires mechanical scrubbing. Can cause leakage and is slow.
Ion Implantation	Requires special platen-holder to accommodate shape and rails
Furnace Anneal	No problems encountered
Screen Printing Ag front grid Al p^+ BSF	Requires special platen sample holder to prevent break-off of rails. Otherwise, printing of grid and back contact was satisfactory. See Fig. 85.
Firing Al p^+ BSF Ag front grid	Web will warp if rails are not retained. Minimize thermal shock. No problems experienced.

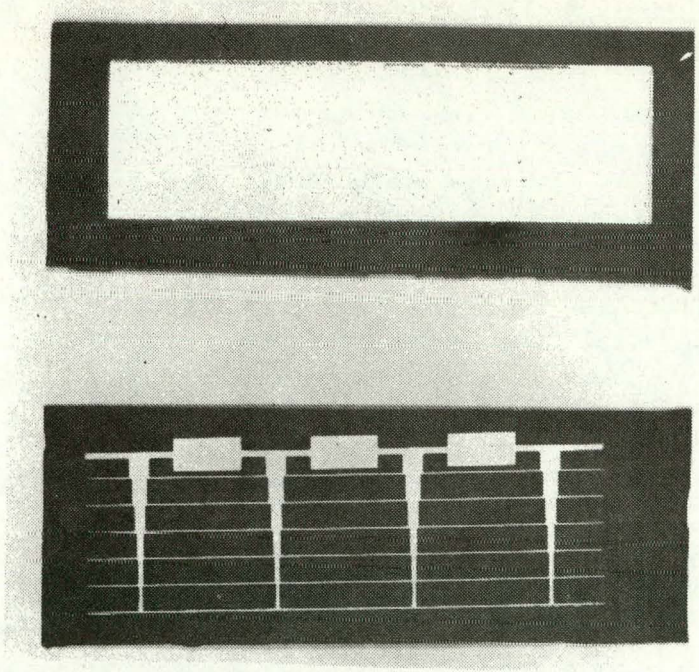


Figure 85. Screen-printed front grid and back contact metallization on dendritic web silicon.

dimensions of 3.0 to 2.7 cm at the ends. The section to section thicknesses were 7 to 9 mil, and the variation along a section was about 0.5 mil.

Before the 30-cm-long web sections were cut into 4-cm sections for processing, it was necessary to remove a yellow-brown film from the surfaces. Swabbing the surface with a 5% HF solution was required to completely remove this film. This process is slow, and without specially designed equipment, a high breakage rate of the web can occur. No other problems were encountered in the remaining cleaning steps when our standard cleaning procedures were used.

The experiments consisted of processing small lots (about 10 samples/lot) through ion implantation, furnace anneals, screen printing of both thick-film Al back contact and Ag front grid metallization, and the firing steps for each printing. In all lots except one, the dendrite rails were retained throughout the processing steps. For the case where the rails were removed, extensive breakage was experienced and severe warping occurred after firing the aluminum paste. For all other lots, the rails were removed as a last step; however, no suitable method of edging the junctions was available, and cell performance of completed samples could not be assessed adequately because of edge-current leakage.

Definitive conclusions concerning the throughput, yield, or performance of web in these processes cannot be made on the basis of this work. To accomplish this work would require that special equipment and process modifications be designed and implemented to accommodate the web.

D. PROCESS COMPATIBILITY PROBLEMS

Even when the implant and anneal parameters indicated above were made, process compatibility problems were noted which are intimately related to the screen-printed metallization process. First, we have consistently observed that screen-printed, thick-film inks do not contact ion-implanted junctions as well as diffused-junction layers. As described in subsection C.1, we had demonstrated screen-printed contacts and determined suitable "in-house" and commercial ink formulations and firing techniques on diffused-junction solar cells. We found that when identical techniques were applied to ion-implanted junctions, such excessive contact resistance is experienced that an additional process step consisting of dilute hydrofluoric acid (HF) rinsing is required after firing, and that even with the addition of this step, cell fill factors

seldom exceed 70%. In contrast, in most cases, the performance of $POCl_3$ diffused-junction solar cells is good immediately after the screen-printed inks are fired. This situation is illustrated in Figs. 86 and 87 for both ion-implanted and diffused-junction cells. For the diffused-junction cells, a small improvement in fill factor does result from HF dipping for 30 s. Beyond 30 s very little increase in fill factor was noted.

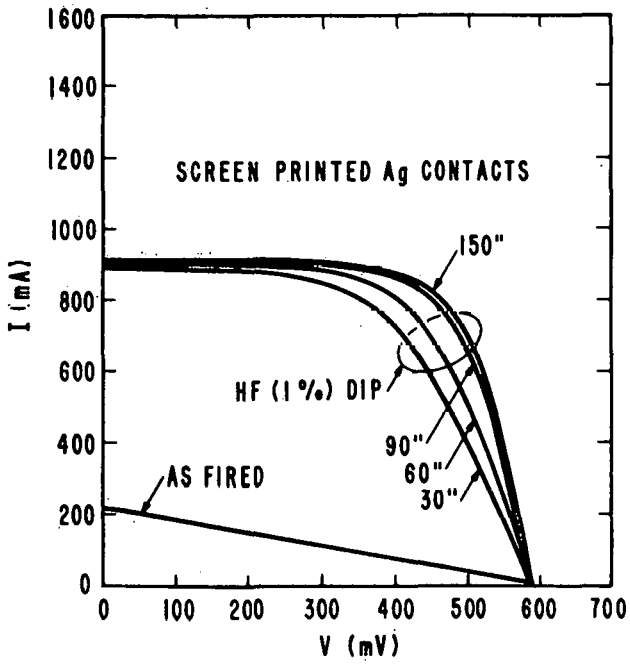


Figure 86. Performance of sequence II ion-implanted cells.

The situation shown in Fig. 86 is typical of the ion-implanted cells in that the fill factor is very low ($\lesssim$30%) after firing, with a large increase in fill factor resulting from the HF dipping process. The improvement in fill factor is largest for initial dipping times of from 10 to 30 s; however, in some cases continued increases in fill factor were measured for dipping times up to 3 min. Dipping for times in excess of 3 min generally results in staining of the silicon surface and ultimately in peeling of the printed metallization.

Because of this, optimum dipping times had to be experimentally determined for each of the ion-implanted junction cases represented by the three sequences under study. The optimum conditions were found to be different for the three sequences, with the $p^+/n/n^+$ cells of sequence III requiring the least amount of dipping (30 s) and sequence II cells the longest (150 s).

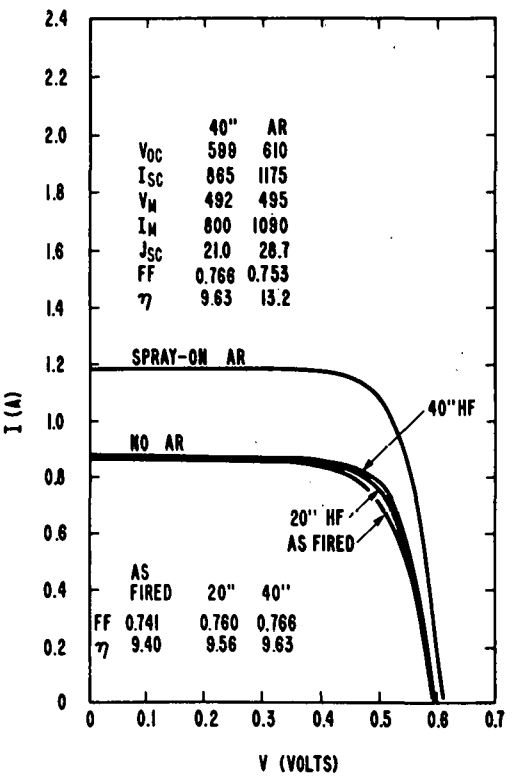


Figure 87. Performance of $POCl_3$-junction cells.

While HF dipping appears to be a panacea, there are a number of serious problems associated with its use. First, it becomes an extra required process step, adding cost to the manufacturing sequence. It is a process requiring the use of acid with the attendant safety and waste-removal problems. Also, at this time, the mechanism by which the HF solution improves the contact between the screen-printed metal film and the silicon is not known, thereby making control of this process difficult. Furthermore, as will be described below, while the HF dipping improves the fill factor in all cases, it sometimes leaves the metal-film-silicon interface susceptible to serious degradation causing incompatibility with the next process step of spray-on AR coating.

In preparation for the spray-on AR coating process, cells are batch-dipped, 25 at a time, in a 2% solution of $HF:H_2O$ (60 ml:3000 ml), thoroughly rinsed in bubbling DI water, and dryed. For purposes of comparison, the AM-1 characteristics of all cells are measured before and after AR coating. The spray-on AR coating process described previously [19,20] was used for all results reported here.

From previous data and verification tests, it is expected that application of the AR coating will result in an increase in the short-circuit current and cell efficiency of about 35% with little effect on other cell parameters. These results were obtained on cells with evaporated Ti/Ag metallization or cells with screen-printed thick-film metal but generally not dipped in HF solutions. When ion-implanted cells which require HF dipping are spray-coated, sporadic instabilities and degradation of the cell fill factor are observed. This effect is illustrated in Fig. 88 which shows that while the short-circuit current is increased by 33%, the fill factor is substantially reduced resulting in a net decrease in cell efficiency. In addition, some instability is also present in the AR coated case as shown by the two I-V traces in Fig. 88 taken about 15 s apart. The sporadic nature of the degradation in fill factor within a cell lot is illustrated in Tables 47 and 48 which show the measured cell characteristics for lot 147 (sequence II processing) before and after spray AR coating. Extreme cases in which an entire lot was degraded, and other cases in which no cells were adversely affected by the spray-on AR process have also been observed.

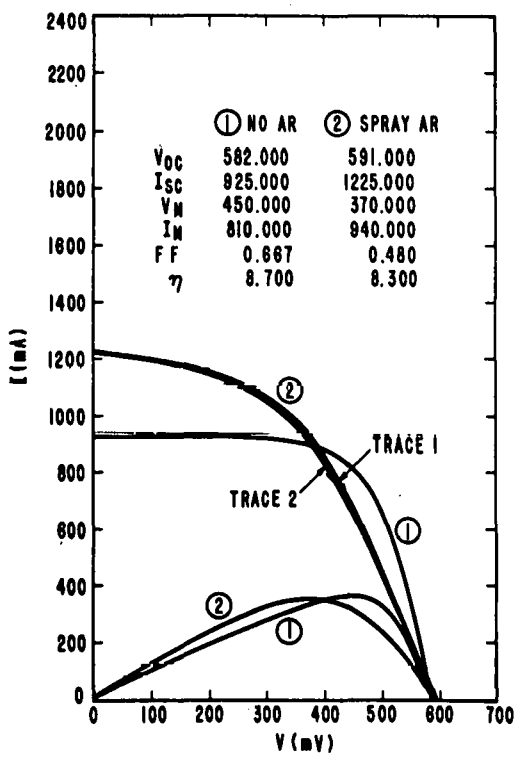


Figure 88. Effect of spray AR coating on performance of ion-implanted cells.

TABLE 47. MEASURED CELL PARAMETERS PRIOR TO COATING FOR LOT 147

CELL NUM	OPEN CIR VOLT	CELL CURRENT	MAX POWER	FILL FACT	SER RESIS	SHUNT RESIS	PMAX CURRENT	PMAX VOLT	EFF	BASE TEMP
D2NS147001	.575	979.	9.01	.671	.067	39.41	859.	.441	.090	24.4
D2NS147002	.570	982.	8.16	.611	.476	12.84	786.	.436	.081	24.4
D2NS147003	.579	999.	9.03	.655	.930	20.99	851.	.446	.090	24.6
D2NS147004	.579	1,025.	8.94	.631	.561	23.07	861.	.436	.089	24.5
D2NS147005	.583	1,003.	9.04	.649	.652	17.12	853.	.445	.090	24.7
D2NS147006	.573	1,009.	8.42	.611	.485	40.47	822.	.430	.084	24.9
D2NS147007	.577	1,008.	8.79	.634	.643	57.25	827.	.447	.088	24.9
D2NS147008	.578	1,004.	8.97	.649	.674	53.45	857.	.440	.090	24.9
D2NS147009	.583	1,023.	9.38	.660	.054	20.76	892.	.442	.094	25.0
D2NS147010	.582	1,021.	9.05	.639	.049	82.74	858.	.443	.090	24.9
D2NS147011	.569	1,005.	8.13	.597	.217	29.54	794.	.430	.081	25.1
D2NS147012	.556	993.	6.99	.532	.356	20.93	718.	.409	.070	25.0
D2NS147013	.570	1,000.	8.15	.600	.934	260.00	809.	.423	.081	25.1
D2NS147014	.577	1,017.	8.83	.630	.596	52.83	842.	.440	.088	24.5
D2NS147015	.576	1,013.	8.53	.614	.391	341.40	815.	.440	.085	24.7
D2NS147016	.573	1,012.	8.36	.606	.176	162.10	810.	.434	.084	24.9
D2NS147017	.574	997.	8.19	.601	.291	11.59	818.	.421	.082	24.9
D2NS147018	.569	994.	7.85	.583	.279	459.50	762.	.433	.079	25.1
D2NS147019	.580	1,019.	9.11	.648	.243	9.41	874.	.438	.091	25.0
D2NS147020	.568	1,014.	7.98	.581	.544	13.58	801.	.419	.080	25.0
D2NS147021	.576	1,000.	8.73	.637		1,201.00	846.	.433	.087	25.1
D2NS147022	.575	1,017.	8.95	.643	.210	60.90	868.	.433	.090	25.1
D2NS147023	.575	1,000.	8.79	.642	.709	51.01	832.	.444	.088	25.1
D2NS147024	.579	1,027.	9.05	.640	.569	13.01	855.	.445	.091	25.3
D2NS147025	.580	1,004.	9.00	.658	.458	22.80	855.	.442	.090	25.2

TABLE 48. MEASURED CELL PARAMETERS AFTER SPRAY-ON AR COATING FOR LOT 147

CELL NUM	OPEN CIR VOLT	CELL CURRENT	MAX POWER	FILL FACT	SER RESIS	SHUNT RESIS	PMAX CURRENT	PMAX VOLT	EFF	BASE TEMP
D2NS147001	.581	1,273.	10.73	.610	.219	34.89	1,105.	.408	.107	25.0
D2NS147002	.579	1,274.	10.28	.586	.137	13.15	1,031.	.419	.103	25.1
D2NS147003	.586	1,301.	10.86	.599	.180	45.67	1,104.	.413	.109	25.2
D2NS147004	.583	1,278.	8.07	.456	.191	2.25	893.	.379	.081	25.4
D2NS147005	.587	1,285.	8.53	.476	.365	15.37	883.	.406	.085	25.2
D2NS147006	.582	1,299.	10.37	.577	.214	6.78	1,091.	.399	.104	25.4
D2NS147007	.585	1,300.	10.77	.596	.981	671.10	1,082.	.418	.108	25.4
D2NS147008	.585	1,288.	9.69	.542	.241	146.90	1,005.	.405	.097	25.4
D2NS147009	.584	1,126.	4.41	.283	.377	.35	572.	.324	.044	25.5
D2NS147010	.587	1,314.	9.60	.524	.500	517.90	1,006.	.401	.096	25.5
D2NS147011	.579	1,303.	10.49	.585	.277	31.36	1,092.	.404	.105	25.5
D2NS147012	.566	1,288.	9.05	.522	.270	29.29	963.	.395	.091	25.4
D2NS147013	.580	1,287.	10.36	.585	.062	9.30	1,057.	.412	.104	25.6
D2NS147014	.583	1,292.	7.94	.444	.281	6.36	872.	.383	.080	25.6
D2NS147015	.583	1,296.	8.00	.446	.276	67.83	860.	.391	.080	25.5
D2NS147016	.582	1,301.	10.26	.571	.015	30.88	1,085.	.397	.103	25.6
D2NS147017	.583	1,266.	10.42	.595	.506	7.67	1,041.	.421	.104	25.6
D2NS147018	.579	1,286.	9.61	.543	.734	58.95	1,037.	.389	.096	25.6
D2NS147019	.585	1,303.	9.24	.511	.503	199.90	966.	.402	.093	25.7
D2NS147020	.574	1,294.	7.30	.414	.622	92.06	842.	.364	.073	25.8
D2NS147021	.583	1,293.	10.69	.596	.166	7.96	1,072.	.419	.107	25.6
D2NS147022	.582	1,289.	8.15	.458	.603	174.60	964.	.355	.082	25.8
D2NS147023	.583	1,286.	8.44	.475	.062	54.80	1,020.	.347	.085	25.7
D2NS147024	.583	1,303.	9.07	.503	.995	9.14	995.	.383	.091	25.8
D2NS147025	.584	1,251.	6.64	.383	.605	21.30	822.	.339	.067	25.8

The sensitivity of such cells to evaporated AR coating was tested by a random selection of eight cells from four lots and by evaporating a ZrO_2 coating of nominal 725-Å thickness after screen-printing and HF dipping. The results of this test, given in Table 49 along with selected data from these lots of cells processed in the ordinary way, show that the degradation is not induced by an evaporated AR coating.

It is also important to note that this effect does not occur with solar cells made with $POCl_3$-diffused junction even when such cells are HF dipped. This is illustrated in Fig. 88.

E. SOLAR-CELL RESULTS - SEQUENCES I, II, AND III

The total number of cells fabricated was about 1500, with about 500 in each of the three sequence categories. The AM-1 illuminated electrical characteristics for all cells were measured and stored in our data bank. These data have been examined, but because of the compatibility problems described in Section D, it is difficult to make quantitative statistical comparisons of the completed cell performance. However, since all cells were subjected to HF dipping in such a manner as to optimize their performance, comparisons can be made prior to AR coating, and estimates of the completed-cell parameters made on the basis of the known effect of the AR coating in the absence of compatibility problems.

The composite average values of the AM-1 parameters measured prior to AR coating for all cells in sequences I, II, and III are given in Table 50. The estimated values listed with AR coating were obtained by assuming a 31% increase in short-circuit current, a logarithmic increase in open-circuit voltage, i.e., $V_{oc_{AR}} = V_{oc} + 0.026 \ln(1.31)$, and a decrease in fill factor due to series resistance. It was noted that for some processed cell lots, no apparent degradation was noted due to the spray-on AR coating process. The measured parameters of the best performing cells from these lots are also listed in Table 50 to indicate peak values obtainable with these processes. In addition, in the course of our work, 100 cells were fabricated with junctions formed by $POCl_3$ diffusion, and the average parameters for these cells are also listed in Table 50 for comparative purposes.

TABLE 49. COMPARISON OF ZrO_2 EVAPORATED AR WITH SPRAY AR (SCREEN-PRINTED CELLS)

Lot, Cell No.	I_{sc_1} (mA)	I_{sc_2} (mA)	$\Gamma = \frac{I_{sc_2}}{I_{sc_1}}$	η_1 (%)	η_2 (%)	FF_1	FF_2	F_2/F_1	Comment
994, 14	965	1312	1.35	8.16	10.44	0.603	0.559	0.927	Evaporated ZrO_2
939, 1	942	1315	1.39	9.50	13.16	0.716	0.709	0.978	Evaporated ZrO_2
943, 5	995	1375	1.38	9.87	13.45	0.702	0.679	0.966	Evaporated ZrO_2
941 25	990	1333	1.35	9.82	12.86	0.700	0.668	0.954	Evaporated ZrO_2
939, 2	935	1300	1.39	9.58	13.08	0.727	0.703	0.967	Evaporated ZrO_2
944, 13	935	1325	1.42	9.00	12.50	0.703	0.679	0.966	Evaporated ZrO_2
941, 10	1005	1368	1.36	9.73	12.78	0.688	0.653	0.949	Evaporated ZrO_2
943, 6	990	1340	1.35	9.80	13.0	0.700	0.673	0.961	Evaporated ZrO_2
941, 23	972	1318	1.36	9.4	11.9	0.696	0.644	0.925	Spray AR, best in lot
941, 14	984	1286	1.31	9.6	6.5	0.696	0.360	0.517	Spray AR, typical degraded cell
944, 23	992	1308	1.32	10.0	12.3	0.712	0.659	0.926	Spray AR, best in lot
944, 19	959	1162	1.21	9.8	5.9	0.697	0.373	0.535	Spray AR, typical degraded cell
943, 3	992	1342	1.35	9.7	12.8	0.699	0.673	0.963	Spray AR, best in lot
943, 14	991	1325	1.34	9.8	8.0	0.701	0.425	0.606	Spray AR, typical degraded cell

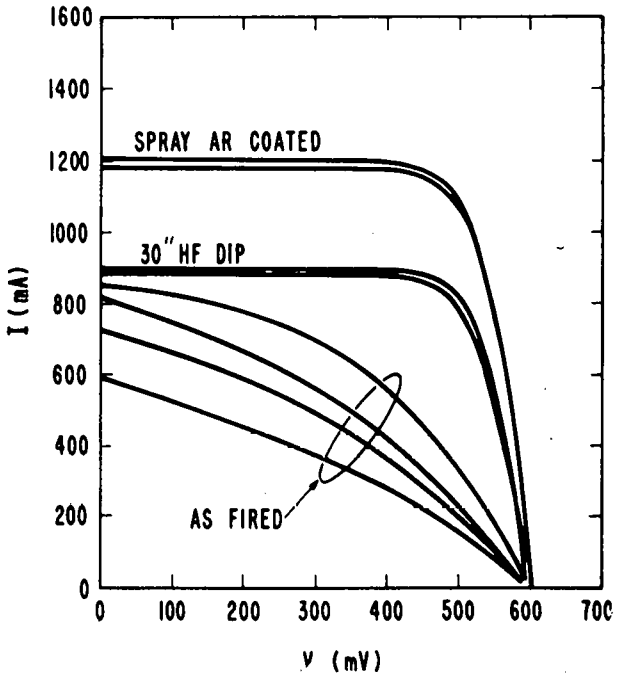


Figure 89. Effect of spray AR coating on performance of $POCl_3$-junction cells.

The relative ranking in performance of the cells made by the three manufacturing sequences and by the $POCl_3$ process warrants some comment.

From among the three sequences, clearly the sequence III process yielded the best cells with measured AM-1 efficiencies reaching 13% even though the fill factors were consistently below 70%. These solar cells are made using n-type solar-grade starting silicon with an initial $POCl_3$ "gettering" diffusion step; after etching they are implanted with boron and phosphorus in such a manner that a $p^+/n/n^+$ structure results. The importance of the $POCl_3$ gettering step was assessed by omitting that step for several lots, then merging these lots with others for common subsequent processing. The results for one such lot and a typical sequence III lot are given in Tables 51 and 52. The benefit from the gettering shows up as a net increase of 15% in average cell efficiency due mostly to a +9.6% increase in short-circuit current.

That the inclusion of the $POCl_3$ gettering step is cost-effective can be seen in Tables 53 and 54 which show a net savings of $0.133/W resulting from the increased efficiency.

TABLE 50. COMPARISON OF AVERAGE SOLAR-CELL PARAMETERS FOR SEQUENCES I, II, AND III

Manufacturing Sequence	Structure	Measured - No AR				Estimated - With AR				Best Measured With AR			
		$\overline{I_{sc}}$ (mA)	$\overline{V_{oc}}$ (mV)	$\overline{FF}$ -	$\bar{\eta}$* (%)	$\overline{I_{sc}}$ (mA)	$\overline{V_{oc}}$ (mV)	$\overline{FF}$ -	$\bar{\eta}$ (%)	I_{sc} (mA)	V_{oc} (mV)	FF -	η (%)
I	$n^+/p/p^+$	870	557	0.701	8.1	1140	567	0.673	10.4	1146	571	0.685	10.7
II	$n^+/p/p^+$	970	574	0.675	8.9	1280	584	0.650	11.6	1268	578	0.680	11.9
III	$p^+/n/n^+$	1020	585	0.686	9.7	1336	595	0.660	12.5	1368	597	0.670	13.0
$POCl_3$	$n^+/p/p^+$	867	584	0.755	9.3	{1177	594	0.748	12.7}**	1205	610	0.761	13.3

*Cell area = 42 cm^2
**Measured values

TABLE 51. SEQUENCE III CELLS

PAGE 1

TABLE TO CHECK CALCULATOR INPUT PRIOR TO COATING FOR LOT NUMBER 983

CELL NUM	OPEN CIR VOLT	CELL CURRENT	MAX POWER	FILL FACT	SER RESIS	SHUNT RESIS	PMAX CURRENT	PMAX VOLT	EFF	BASE TEMP
D3NS983001	.576	968.	9.26	.699	.767	285.70	850.	.458	.093	25.7
D3NS983002	.576	962.	9.17	.697	.828	690.30	863.	.447	.092	25.7
D3NS983003	.566	935.	8.72	.695	.872	2,814.00	808.	.453	.087	25.6
D3NS983004	.591	1,042.	9.96	.682	1.885	29.81	888.	.471	.100	25.8
D3NS983005	.583	1,015.	9.62	.685	1.676	127.60	876.	.461	.097	25.9
D3NS983006	.592	1,035.	9.23	.685	1.724	25.35	867.	.447	.093	25.9
D3NS983007	.590	1,040.	10.06	.692	1.464	1,759.00	925.	.457	.101	26.1
D3NS983008	.592	1,055.	10.16	.686	1.593	167.20	919.	.464	.102	26.1
D3NS983009	.591	1,037.	10.06	.692	1.318	22.37	905.	.467	.101	26.1
D3NS983010	.592	1,054.	10.11	.684	1.257	1,550.00	906.	.469	.102	26.1
D3NS983011	.586	1,045.	9.77	.674	.694	174.90	897.	.458	.098	26.2
D3NS983012	.590	1,042.	10.22	.701	1.385	131.20	911.	.471	.103	26.2
D3NS983013	.591	1,042.	10.10	.692	.339	99 65	925.	.459	.101	26.3
D3NS983014	.584	1,044.	9.96	.689	1.079	26.67	905.	.462	.100	26.4
D3NS983015	.567	940.	8.61	.683	.744	813.70	810.	.447	.087	26.4
D3NS983016	.596	1,053.	10.23	.681	.534	1,802.00	918.	.468	.103	26.4
D3NS983017	.577	1,044.	9.76	.684	1.178	895.40	912.	.449	.098	26.3
D3NS983018	.590	1,047.	10.03	.686	.281	1,435.00	907.	.464	.101	26.9
D3NS983019	.586	1,041.	9.97	.690	1.929	607.90	904.	.463	.100	26.4
D3NS983020	.588	1,034.	9.98	.694	.137	176.80	903.	.464	.100	26.4
D3NS983021	.591	1,047.	10.06	.687	2.179	364.70	913.	.463	.101	26.4
D3NS983022	.592	1,049.	9.89	.672	2.322	3,418.00	894.	.465	.099	26.4
D3NS983023	.589	1,044.	10.14	.696	1.697	17.44	919.	.463	.102	26.4

PAGE 1

AVERAGE CALCULATOR INPUT VALUES PRIOR TO COATING FOR LOT NUMBER 983

AVE OPEN CIR VOLT	AVE CELL CURRENT	AVE MAX POWER	AVE FILL FACTOR	AVE SER RESIS	AVE SHUNT RESIS	AVE PMAX CURRENT	AVE PMAX VOLTAGE	AVE EFF	AVE BASE TEMP
.585	1,028.	9.79	.686	1.212	758.03	892.	.460	.098	26.2

TABLE 52. SEQUENCE III CELLS PROCESSED WITHOUT $POCl_3$ GETTERING

PAGE 1

TABLE TO CHECK CALCULATOR INPUT PRIOR TO COATING FOR LOT NUMBER 114

CELL NUM	OPEN CIR VOLT	CEL. CURRENT	MAX POWER	FILL FACT	SER RESIS	SHUNT RESIS	PMAX CURRENT	PMAX VOLT	EFF	BASE TEMP
D3NS114001	.571	942.	8.37	.661	1.065	28.22	828.	.424	.085	27.2
D3NS114002	.569	920.	8.50	.688	.372	126.60	804.	.444	.086	27.1
D3NS114003	.570	929.	8.64	.693	.619	99.45	827.	.439	.087	27.2
D3NS114004	.575	939.	7.70	.606	.719	41.24	773.	.418	.078	27.3
D3NS114005	.575	947.	8.31	.648	.481	128.10	852.	.419	.084	27.3
D3NS114006	.572	953.	8.66	.674	.902	142.30	855.	.436	.088	27.4
D3NS114007	.569	936.	8.56	.633	.160	18.99	860.	.433	.086	27.4
D3NS114008	.570	946.	8.76	.689	.513	276.80	851.	.443	.089	27.4
D3NS114009	.576	944.	8.01	.627	.852	150.40	779.	.432	.081	27.6
D3NS114010	.575	938.	8.01	.632	.405	29.02	786.	.428	.081	27.5
D3NS114011	.572	944.	8.69	.684	.212	264.60	820.	.445	.088	27.5
D3NS114012	.570	940.	8.72	.692	.307	451.70	832.	.440	.088	27.6
D3NS114013	.569	937.	8.59	.686	.871	13.70	828.	.436	.087	27.7
D3NS114014	.573	938.	8.14	.645	.032	311.40	783.	.437	.082	27.8
D3NS114015	.572	949.	8.26	.647	.041	1,136.00	842.	.412	.084	27.7
D3NS114016	.568	925.	8.38	.678	1.204	13.60	839.	.430	.085	27.7
D3NS114017	.568	928.	8.47	.682	1.323	302.80	870.	.423	.086	27.8
D3NS114018	.569	940.	8.66	.639	1.754	170.40	819.	.444	.088	27.7
D3NS114019	.572	938.	8.33	.661	.038	58.75	804.	.435	.084	27.7
D3NS114020	.572	932.	8.12	.648	.953	164.30	794.	.429	.082	27.8
D3NS114021	.570	933.	8.64	.691	.281	119.30	831.	.437	.087	27.7
D3NS114022	.569	936.	8.65	.690	.259	695.70	816.	.445	.088	27.6
D3NS114023	.571	940.	8.34	.654	1.113	438.70	806.	.430	.084	27.8
D3NS114024	.572	938.	8.20	.650	.549	28.66	793.	.434	.083	27.8

PAGE 1

AVERAGE CALCULATOR INPUT VALUES PRIOR TO COATING FOR LOT NUMBER 114

AVE OPEN CIR VOLT	AVE CELL CURRENT	AVE MAX POWER	AVE FILL FACTOR	AVE SER RESIS	AVE SHUNT RESIS	AVE PMAX CURRENT	AVE PMAX VOLTAGE	AVE EFF	AVE BASE TEMP
.571	938.	8.40	.667	.626	217.11	815.	.433	.085	27.6

TABLE 53. COST ANALYSIS WITH $POCl_3$ GETTERING STEP, 13% EFFICIENCY CELL

COST ANALYSIS:SEQUENCE #3(B):3" WAFER;13% CELL;30MW;AG FRONT;AG BACK. 10/19/79 16:39:59 PAGE 1

PROCESS COST OVERVIEW-$/WATT

ASSUMPTIONS: 0.621 WATTS PER SOLAR CELL AND 7.8 CM (3") DIAMETER WAFER
CELL THICKNESS: 10.0 MILS. CELL ETCH LOSS: 3.0 MILS. CELL KERF LOSS:10.0 MILS.

STEP	YIELD	PROCESS		MAT'L.	D. L.	EXP.	P. OH.	INT.	DEPR.	SUBTOT	SALVG.	TOTALS	%	INVEST	%
1	99.5%	MEGASONIC CLEANING	(B)	0.0	0.007	0.003	0.002	0.001	0.001	0.014	0.0	0.014	1.1	0.007	0.4
2	99.0%	POCL3 DEPOSITION AND DIFFUSION	(B)	0.0	0.003	0.015	0.004	0.003	0.005	0.030	0.0	0.030	2.4	0.023	1.4
3	95.0%	SODIUM HYDROXIDE ETCH:3 MILS	(A)	0.0	0.055	0.001	0.008	0.001	0.001	0.066	0.0	0.066	5.2	0.006	0.4
4	99.5%	MEGASONIC CLEANING #2	(B)	0.0	0.007	0.003	0.002	0.001	0.001	0.014	0.0	0.014	1.1	0.007	0.4
5	99.0%	ION IMPLANTATION:B,2.E+15,10 KEV	(B)	0.0	0.062	0.027	0.057	0.090	0.107	0.344	0.0	0.344	27.2	0.750	43.5
6	99.0%	ION IMPLANTATION:P,2.E+15,30 KEV	(B)	0.0	0.061	0.027	0.056	0.088	0.105	0.336	0.0	0.336	26.6	0.733	42.5
7	99.5%	MEGASONIC CLEANING #3	(B)	0.0	0.006	0.003	0.002	0.001	0.001	0.012	0.0	0.012	0.9	0.005	0.3
8	98.0%	900C. DEG. DIFFUSION:1/2 HR.	(B)	0.0	0.011	0.003	0.003	0.002	0.003	0.021	0.0	0.021	1.7	0.013	0.7
9	99.5%	MEGASONIC CLEANING #4	(B)	0.0	0.006	0.003	0.002	0.001	0.001	0.012	0.0	0.012	0.9	0.005	0.3
10	99.0%	POST DIFFUSION INSPECTION:10%	(B)	0.0	0.000	0.000	0.000	0.001	0.001	0.002	0.0	0.002	0.2	0.005	0.3
11	98.0%	THICK AG METAL:33% BACK & DRY	(B)	0.053	0.006	0.005	0.007	0.003	0.003	0.078	0.0	0.078	6.2	0.024	1.4
12	98.0%	THICK AG METAL:9% FRONT & FIRE	(B)	0.025	0.006	0.007	0.008	0.004	0.005	0.055	0.0	0.055	4.3	0.035	2.0
13	99.0%	HF DIP	(B)	0.0	0.002	0.001	0.000	0.000	0.000	0.004	0.0	0.004	0.3	0.003	0.2
14	99.0%	AR COATING:SPRAY-ON	(B)	0.001	0.006	0.000	0.003	0.001	0.002	0.013	0.0	0.013	1.0	0.012	0.7
15	90.0%	TEST	(B)	0.0	0.005	0.000	0.004	0.005	0.006	0.020	0.0	0.020	1.6	0.041	2.4
16	98.0%	REFLOW SOLDER INTERCONNECT 1	(B)	0.002	0.011	0.0	0.004	0.004	0.004	0.026	0.0	0.026	2.0	0.029	1.7
17	99.5%	GLASS/PVB/CELL ARRAY ASSEMBLY 1	(B)	0.168	0.028	0.0	0.005	0.003	0.004	0.208	0.0	0.208	16.5	0.027	1.6
18	100.0%	ARRAY MODULE PACKAGING	(A)	0.006	0.002	0.0	0.000	0.000	0.000	0.009	0.0	0.009	0.7	0.001	0.0
	72.4%	TOTALS		0.256	0.282	0.098	0.169	0.207	0.249	1.261	0.0	1.261	100.0	1.726	100.0
			%	20.33	22.38	7.77	13.37	16.42	19.73	100.00					

FACTORY FIRST COST,$/WATT: 0.24 DEPRECIATION,$/WATT: 0.01 INTEREST,$/WATT: 0.03
LAND COST,$/WATT: 0.0 INTEREST,$/WATT: 0.0

NOTE: (A)=EXISTING TECHNOLOGY; (B)=NEAR FUTURE; (C)=FUTURE ANNUAL PRODUCTION: 30.0 MEGAWATTS.
345 DAYS OF FACTORY PRODUCTION PER YEAR. 8.00 HOURS PER SHIFT. NO. OF SHIFTS PER DAY VARIES BY PROCESS STEP
EQUIPMENT NOT SHARED. FULL ALLOCATION TO PROCESS.

TABLE 54. COST ANALYSIS WITHOUT $POCl_3$ GETTERING STEP, 11.5% EFFICIENCY CELL

COST ANALYSIS:SEQUENCE #3(B):3" WAFER:11.5% CELL:30MW:AG FRONT:AG BACK. 10/19/79 16:39:59 PAGE 1

PROCESS COST OVERVIEW-$/WATT

ASSUMPTIONS: 0.549 WATTS PER SOLAR CELL AND 7.8 CM (3") DIAMETER WAFER
CELL THICKNESS: 10.0 MILS. CELL ETCH LOSS: 3.0 MILS. CELL KERF LOSS:10.0 MILS.

STEP	YIELD	PROCESS		MAT'L.	D. L.	EXP.	P. OH.	INT.	DEPR.	SUBTOT	SALVG.	TOTALS	%	INVEST	%
1	99.5%	MEGASONIC CLEANING	(B)	0.0	0.007	0.003	0.002	0.001	0.001	0.014	0.0	0.014	1.0	0.007	0.3
2	95.0%	SODIUM HYDROXIDE ETCH:3 MILS	(A)	0.0	0.061	0.001	0.009	0.001	0.001	0.072	0.0	0.072	5.2	0.007	0.4
3	99.5%	MEGASONIC CLEANING #2	(B)	0.0	0.007	0.003	0.002	0.001	0.001	0.014	0.0	0.014	1.0	0.007	0.3
4	99.0%	ION IMPLANTATION:B,2.E+15,10 KEV	(B)	0.0	0.069	0.030	0.063	0.100	0.119	0.382	0.0	0.382	27.4	0.833	43.0
5	99.0%	ION IMPLANTATION:P,2.E+15,30 KEV	(B)	0.0	0.069	0.038	0.063	0.100	0.119	0.382	0.0	0.382	27.4	0.833	43.0
6	99.5%	MEGASONIC CLEANING #3	(B)	0.0	0.007	0.003	0.002	0.001	0.001	0.014	0.0	0.014	1.0	0.007	0.3
7	98.0%	900C. DEG. DIFFUSION:1/2 HR.	(B)	0.0	0.011	0.003	0.003	0.002	0.003	0.021	0.0	0.021	1.5	0.013	0.7
8	99.5%	MEGASONIC CLEANING #4	(B)	0.0	0.007	0.003	0.002	0.001	0.001	0.014	0.0	0.014	1.0	0.007	0.3
9	99.0%	POST DIFFUSION INSPECTION:10%	(B)	0.0	0.001	0.000	0.001	0.001	0.001	0.003	0.0	0.003	0.2	0.005	0.3
10	98.0%	THICK AG METAL:33% BACK & DRY	(B)	0.060	0.007	0.006	0.009	0.003	0.004	0.088	0.0	0.088	6.3	0.027	1.4
11	98.0%	THICK AG METAL:9% FRONT & FIRE	(B)	0.028	0.007	0.008	0.009	0.005	0.006	0.063	0.0	0.063	4.5	0.040	2.1
12	99.0%	HF DIP	(B)	0.0	0.003	0.001	0.000	0.000	0.000	0.005	0.0	0.005	0.4	0.003	0.1
13	99.0%	AR COATING:SPRAY-ON	(B)	0.001	0.006	0.000	0.003	0.001	0.002	0.013	0.0	0.013	1.0	0.012	0.6
14	90.0%	TEST	(B)	0.0	0.006	0.000	0.005	0.006	0.007	0.023	0.0	0.023	1.6	0.047	2.4
15	98.0%	REFLOW SOLDER INTERCONNECT 1	(B)	0.002	0.015	0.0	0.005	0.005	0.006	0.033	0.0	0.033	2.4	0.040	2.1
16	99.5%	GLASS/PVB/CELL ARRAY ASSEMBLY 1	(B)	0.191	0.033	0.0	0.006	0.006	0.007	0.242	0.0	0.242	17.4	0.051	2.6
17	100.0%	ARRAY MODULE PACKAGING	(A)	0.007	0.002	0.0	0.000	0.000	0.000	0.010	0.0	0.010	0.7	0.001	0.0
	73.1%	TOTALS		0.290	0.314	0.093	0.185	0.233	0.278	1.394	0.0	1.394	100.0	1.939	100.0
			%	20.80	22.55	6.70	13.30	16.70	19.94	100.00					

FACTORY FIRST COST,$/WATT: 0.26 DEPRECIATION,$/WATT: 0.01 INTEREST,$/WATT: 0.03
LAND COST,$/WATT: 0.0 INTEREST,$/WATT: 0.0

NOTE: (A)=EXISTING TECHNOLOGY; (B)=NEAR FUTURE; (C)=FUTURE ANNUAL PRODUCTION: 39.0 MEGAWATTS.
345 DAYS OF FACTORY PRODUCTION PER YEAR. 8.00 HOURS PER SHIFT. NO. OF SHIFTS PER DAY VARIES BY PROCESS STEP
EQUIPMENT NOT SHARED. FULL ALLOCATION TO PROCESS.

In the processing of sequence III cells, problems similar to those in sequences I and II were experienced. The ^{11}B implant dose for the junction layer had to be doubled to 4×10^{15} cm^{-2} in order to obtain consistent sheet resistance values of ~50 Ω/□. Even at this dose level, problems were encountered in obtaining low-resistance screen-printed contacts, and dilute HF rinsing for 30 to 60 s was required to obtain marginally acceptable fill factors approaching 70%. In addition, instability and degradation of the fill factors after spray-on AR coating were noted about as frequently as with sequence I and II processing.

The importance of back-surface-field (BSF) effects and gettering can also be seen in a comparison of the performance of sequence I and II solar cells. The major difference is in the processing associated with the doping or contacting of the back surface of the cells. In sequence II, a boron-glass deposition and high-temperature drive-in are used both to diffuse boron into the back of the wafer and to anneal the phosphorus implant in the front-junction layer. We have shown in previous work [20] that the boron-glass, high-temperature anneal performs an effective gettering treatment resulting in an increase in diffusion length or preservation of long diffusion length in the starting silicon. In sequence I, an aluminum alloying process [20] is used to form the p^+ BSF and back contact, and no intentional gettering processes are employed.

A comparison of the performance data for sequence I and II solar cells given in Table 50 shows that the average cell efficiency for sequence II cells is higher than that of the cells produced by sequence I. Furthermore, the lower fill factor of sequence II cells is more than compensated for by considerably higher short-circuit current and open-circuit voltage, factors which are known to be affected by gettering and BSF effects.

F. RECOMMENDED PROCESS SEQUENCE

1. Major Results and Conclusions for Sequences I, II, and III.

The major results and conclusions concerning manufacturing sequences I, II, and III are summarized as follows:

- Ion-implantation/screen printing/spray-on AR compatibility problems were evident in all three sequences, preventing high yield at high efficiency.

- Gettering (sequences II and III) is required and was shown to be successful and cost effective.
- Some high efficiencies ($\eta \sim 13\%$) were achieved despite problems.
- Sequence III $P^+/N/N^+$ structures had the highest cell efficiency.

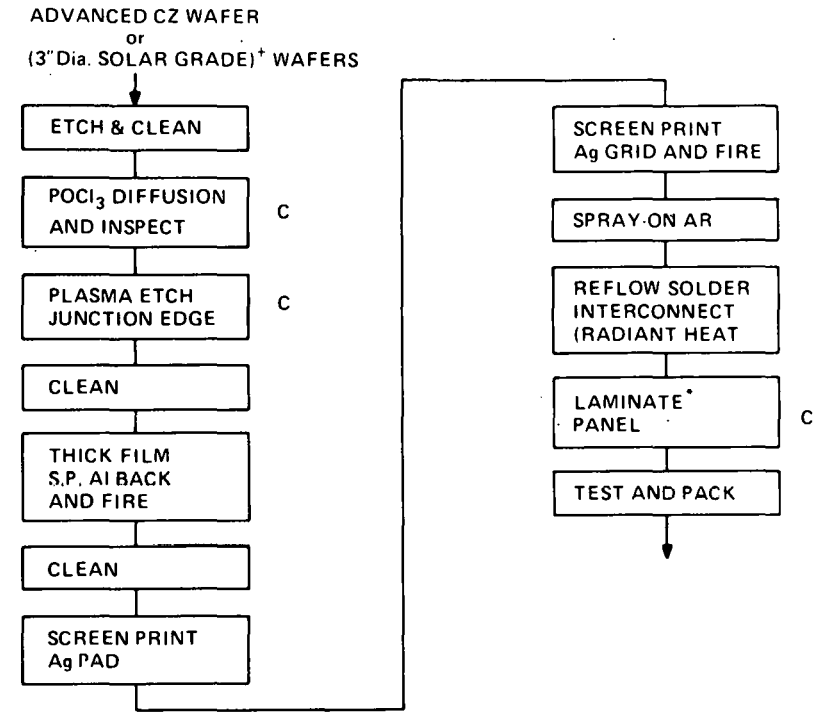
Process compatibility problems prevent an affirmative recommendation of these sequences from a technical standpoint. However, in the absence of these problems, the SAMICS analysis presented in Section VI shows that with the use of lower cost or larger (>3 in. diam) area silicon sheet, these sequences can come close to meeting the 1986 price goal.

2. Recommended Manufacturing Sequence

The problems encountered with sequences I, II, and III are directly related to the use of ion-implantation in conjunction with screen-printed silver thick-film metallization. These sequences are otherwise technically sound and cost effective. The selection of an alternative junction-formation process ($POCl_3$ diffusion) has been shown to remove the compatibility problems and to result in a high-performance, cost-effective sequence. The changed and recommended process sequence is shown in Fig. 90. This process closely resembles sequence I with the changes indicated. The rationale for these changes and the development which was conducted to fill in the new process steps and test this sequence are described below.

The change to junction formation by $POCl_3$ gaseous diffusion was prompted by the good performance (see Section V.E Table 50) experienced when this process was used in conjunction with screen-printed contacts and the spray-on AR coating process. When gaseous diffusion is used to form the junction, an n^+-type layer forms over the entire surface of the water which raises the need to cleanly, reproducibly, and economically separate the n^+/p junction at the periphery. For this purpose, we developed a plasma etch process described below.

The plasma etcher used was an I.P.C. 2000 tunnel etcher. This machine has two cylindrical etch-chambers which may be operated simultaneously. Immediately after the $POCl_3$ diffusion, the wafers are "coin-stacked" in a specially constructed aluminum holder and placed in the tunnel. The stack can contain 400 to 600 wafers per run per tunnel. The etching was done with 96:4 CF_4:O_2 gaseous ambient at a starting temperature of 50°C. Since the



* Conformal flexible back now preferred for high yield.
C Indicates changes from previous sequences.
\+ Used 3-in.-diam solar grade wafers in the experimental verification.

Figure 90. Recommended process sequence.

wafers are "coin-stacked," only the edges which are exposed to the plasma are etched. Measurements on specially prepared wafers with radial photoresist stripes indicated that ~2-μm depth of silicon is removed in 30 min of etching. The average electrical characteristics of a 100-wafer lot of cells etched for 30 min compared with control samples which received no etching are shown in Table 55. As expected, the edge-leakage current of the etched cells is greatly reduced, resulting in higher open-circuit voltage and fill-factor. The reduced (-5.8%) short-circuit current in the etched cells is due to the excess surface area removed at the periphery. This was due to the taper at the wafer edges which exposes about a 1-mm annulus to the plasma resulting in a removal of ~6% of the surface area.

A cost analysis of this process was conducted assuming a throughput rate of 800, 3-in.-diam wafers/hour and using the machine and material parameters experienced in our tests along with an initial cost for the I.P.C. 2000 of $30K. The result for 500 MW/yr production rate was $0.017/W.

The recommended change from a double-glass panel construction to a flexible or conformal-back design results from the uncertain yield of the double-glass lamination processes which we examined. The difficulties experienced in attempting to find a high-yield, high-throughput lamination process for the double-glass structure were described in Section IV. We have examined several commercially available flexible-back laminated panels and have conducted small-scale experiments to fabricate such structures and assess their manufacturability. We found, for example, that a glass*/PVB/cell-array/PVB/Tedlar structure was relatively easy to laminate, with the conformal nature of the Tedlar backing removing the major causes of cell and/or glass breakage associated with a rigid glass back.

These observations have led us to conclude that flexible-back panel designs should be manufacturable at high-yield and with reasonably high throughput. However, the question of which backing material is best from a cost/performance viewpoint is still open. All known polymer-based extrusible sheet materials will allow the transmission of water vapor and gases to the interior of the panel in times much shorter than the desired 20-year life. The resulting long-term degradation effects will have to be assessed and weighed against the cost savings afforded by such structures.

TABLE 55. RECOMMENDED SEQUENCE PERFORMANCE
PLASMA ETCH, JUNCTION EDGE

		J_{sc}	V_{oc}	FF	η	
Plasma Etch	<AVE>	29.2	598	0.753	13.1	<FF> ± 1%
No Plasma Etch	TYP.	30.9	579	0.555	10.0	<FF> ± 2%

*Tempered glass.

SECTION VI

COST ANALYSIS AND RECOMMENDATIONS

A. INTRODUCTION

The overall objective of this work was to specify one or more process sequences which, when automated, would have the potential of meeting the 1986 price goals set forth by DOE/JPL. In the previous sections, the development of low-cost process steps were described, and the technical performance of solar cells made by assembling these processes to form manufacturing sequences was given in detail. In this section, the manufacturing cost associated with each of the sequences studied under this program is estimated with the aid of the SAMICS cost analysis method as implemented by the SAMIS III computer program.

Subsection VI.B gives the results of applying SAMICS to analyze the four manufacturing sequences described in Section V. These analyses show that if the starting silicon is 3-in.-diameter CZ wafer obtained at $0.31/W, none of these sequences will meet the $0.70/W goal. However, a further analysis is described which shows that if an equivalent 6-in.-diameter starting wafer is used, a price of $0.689/W can be achieved.

Subsection VI.C describes the effect of the yield of individual process steps on the overall cost of a given manufacturing sequence. A simple analytical expression is given which can be used to estimate the change in the overall cost due to a change in the yield associated with a given process step.

B. SAMICS ANALYSIS

The SAMICS III computer program was used to obtain price projections for five manufacturing sequences. These sequences are listed below along with their distinguishing features and the major assumptions which went into the analysis. SAMICS input process specification data are contained in Appendix A.

A 14% cell efficiency is assumed for the $POCl_3$ diffused-junction cases. Only a small number (~100 cells) of solar cells were fabricated with this sequence; however, an average efficiency of 12.7% and a peak efficiency of 13.3% (see Table 50) were obtained. For 1986 cost projections, it is reasonable to assume that this process can be further optimized so that the average efficiency can be increased to 14%.

For sequences I, II, and III, the compatibility problems described in Section V caused wide variations in cell efficiency so that the use of average values is not meaningful. Instead, in order to minimize these effects on our cost projections, the value of cell efficiency was assumed equal to the average of the best 50 cells produced with each sequence.

Needless to say, the 90% test yield assumed for sequences I, II, and III is considerably higher than was obtained in our experimental production studies with these processes. It was assumed here for comparative purposes and to indicate a lower-limit price for these sequences which might be attained in the absence of the problems experiences here. In contrast, the 90% test yield assumed for the RCA3 diffused-junction sequence is a conservative estimate.

(1) RCA3: $POCl_3$ diffused-junction process
Wafer diameter = 3.07 in. (7.8 cm)
Cell efficiency, η = 14%
225 cells/panel
150.43 W/panel
10 panels/package

(2) RCA6: Same process as RCA3 but scaled-up to 6-in.-(15.1 cm) diameter wafers.
Cell efficiency, η = 14%
65 cells/panel
161.28 W/panel
10 panels/package

(3) Sequence I: Ion-implanted (^{31}P) junction, Al screen-printed back contact.
Wafer diameter = 3.07 in. (7.8 cm)
Cell efficiency, η = 10.7%
225 cells/panel
114.97 W/panel
10 panels/package

(4) Sequence II: Ion-implanted (^{31}P) junction, deposited and diffused boron doping on back.
Wafer diameter = 3.07 in. (7.8 cm)
Cell efficiency, η = 11.9%
225 cells/panel
127.93 W/panel
10 panels/package

(5) Sequence III: $P^+/N/N^+$ cell structure with ion-implanted (^{11}B) junction and back (^{31}P) surface field (BSF) contact.

Wafer diameter = 3.07 in. (7.8 cm)

Cell efficiency, η = 13%

225 cells/panel

139.69 W/panel

10 panels/package

For all simulations, we used the SAMIS "DEFAULT" run control and standard at a production level of 500 MW/year. All costs are given in 1980 dollars.

Tables 56 through 59 summarize the assumed step-yields and throughput/min and give the resulting cumulative and step costs for each of the five sequences.

C. YIELD SENSITIVITY ANALYSIS

Although there are many parameters against which one might want to check process cost sensitivity, a change in process yield has one of the greatest impacts. While a change in yield primarily leaves the individual process and the production sequence unchanged, it does affect the useable output of the process whose yield was changed, and the workload of that process and all other processes that precede it in the sequence.

We chose to test the sensitivity of the RCA6 process sequence for four different yield changes. This analysis assumes that there are no provisions for reworking cells at any stage in the production sequence. Although the lack of rework facilities may not be a real condition in a production environment, it highlights the costliness of "downstream" yield losses on "upstream" processes.

After investigating the data produced by actually running the simulations for each sensitivity test, it was observed that the same results could have been arrived at by an analytical technique.

In brief, if we let $\kappa = \frac{y^*}{y}$, where y^* is the new yield and y is the original yield, then the new cumulative cost at any process step can be calculated as follows. $C^* = \frac{C}{\kappa}$, where C^* is the new cumulative cost and C is the original cumulative cost. Furthermore, the same κ factor can be applied to any process step preceding the one where the yield had been changed in order to observe the effect at that other process step.

TABLE 56. RCA3 AND RCA6 RESULTS

Process	Yield	Throughput		RCA3 ($/W) Cum Cost	RCA3 ($/W) Process	RCA6 ($/W) Cum Cost	RCA6 ($/W) Process
RWAFER	1.00	60	Slice	0.3142	0.3142	0.3035	0.3035
ETCHWAFER	0.99	60	Slice	0.3294	0.0152	0.3086	0.0051
MSCLN-1	0.995	41.7	Slice	0.3513	0.0219	0.3176	0.0090
POCL3DEP	0.995	70	Slice	0.3628	0.0112	0.3245	0.0069
PDI:10%	0.995	240	Slice	0.3694	0.0066	0.3262	0.0017
JUNCTPE	0.99	20	Slice	0.3846	0.0152	0.3302	0.0040
MSCLN-2	0.995	41.7	Slice	0.4061	0.0215	0.3391	0.0089
SPALBACK	0.98	60	Slice	0.4277	0.0166	0.3489	0.0098
MSCLN-3	0.995	41.7	Slice	0.4437	0.0210	0.3575	0.0086
SPAGPAD	0.995	60	Slice	0.4644	0.0207	0.3716	0.0141
SPAGFRONT	0.99	60	Slice	0.5072	0.0428	0.4128	0.0412
HFDIP	0.99	100	Slice	0.5209	0.0137	0.4189	0.0061
SPRAYAR	0.99	75	Slice	0.5376	0.0167	0.4237	0.0049
TEST	0.98	60	Cells	0.5420	0.0044	0.4250	0.0013
RSINTERCN	0.98	0.22	Layup	0.5926	0.0506	0.4708	0.0458
ARRAYASSM	0.98	1.20	Layup	0.8094	0.2168	0.6676	0.1968
FRAMEASSM	0.995	1.33	Module	0.8132	0.0038	0.6697	0.0021
PACKAGING	1.000	0.6	Module	0.8330 *	0.0198	0.6879 *	0.0181
Net Yield	0.842						

*Net price

TABLE 57. SEQUENCE I RESULTS

Process	Yield	Throughput	Cum ($/W)	Step
RWAFER	1.000	60	0.3222	0.3222
ETCHWAFER	0.99	60	0.3418	0.0196
IONIMPLPJ	0.99	150	0.3838	0.0420
MSCLN-1	0.995	41.7	0.4122	0.0284
4HRANNEAL	0.99	150	0.4293	0.0170
SPALBACK	0.98	60	0.4510	0.0217
MSCLN-2	0.995	41.7	0.4784	0.0274
SPAGPAD	0.995	60	0.5057	0.0273
SPAGFRONT	0.99	60	0.5670	0.0614
HFDIP	0.99	100	0.5796	0.0126
SPRAYAR	0.99	75	0.6017	0.0221
TEST	0.98	60	0.6074	0.0057
RSINTERCN	0.98	0.22	0.6738	0.0664
ARRAYASSM	0.98	1.20	0.9581	0.2843
FRAMEASSM	0.995	1.33	0.9628	0.0047
PACKAGING	1.000	0.60	0.9886 *	0.0258
Net Yield	0.851			

*Net price

TABLE 58. SEQUENCE II RESULTS

Process	Yield	Throughput	Cum ($/W)	Step
RWAFER	1.000	60	0.3125	0.3125
ETCHWAFER	0.99	60	0.3301	0.0176
IONIMPLPJ	0.99	150	0.3672	0.0371
MSCLN-1	0.995	41.7	0.3926	0.0254
BORONDEP	0.990	273	0.4101	0.0175
900DEGDIF	0.995	70	0.4203	0.0102
GLASSREM	0.99	100	0.4305	0.0101
CONGRD	0.99	60	0.4874	0.0569
SPAGFRONT	0.99	60	0.5426	0.0552
HFDIP	0.99	100	0.5538	0.0113
SPRAYAR	0.99	75	0.5734	0.0196
TEST	0.98	60	0.5785	0.0051
RSINTERCN	0.98	0.22	0.6378	0.0592
ARRAYASSM	0.98	1.20	0.8923	0.2545
FRAMEASSM	0.995	1.33	0.8965	0.0042
PACKAGING	1.000	0.60	0.9196 *	0.0231
Net Yield	0.856			

* Net price

TABLE 59. SEQUENCE III RESULTS

Process	Yield	Throughput	Cum ($/W)	Step
RWAFER	1.000	60	0.3104	0.3104
MSCLN-1	0.995	41.7	0.3341	0.0237
PDCL3DEP	0.995	70	0.3462	0.0121
ETCHWAFER	0.99	60	0.3621	0.0159
IONIMPLPJ	0.99	150	0.3962	0.0340
IONIMPLBB	0.99	150	0.4298	0.0336
MSCLN-2	0.995	41.7	0.4526	0.0229
900DEGDIF	0.995	70	0.4618	0.0092
CONGRD	0.99	60	0.5129	0.0510
SPAGFRONT	0.99	60	0.5634	0.0505
HFDIP	0.99	100	0.5737	0.0103
SPRAYAR	0.99	75	0.5917	0.0180
TEST	0.98	60	0.5964	0.0047
RSINTERCN	0.98	0.22	0.6507	0.0543
ARRAYASSM	0.98	1.20	0.8840	0.2333
FRAMEASSM	0.995	1.33	0.8879	0.0039
PACKAGING	1.000	0.60	0.9092 *	0.0212
Net Yield	0.855			

*Net price

This analytical approach assumes a continuously smooth cost as a function of yield while, because one cannot purchase a fraction of a machine, the cost of capital equipment is a step function with yield. However, the calculated result differs from the simulated value by less than 1%. The benefit of the analytical technique is in the time and cost savings for not having to run the simulation. See Table 60 for comparison of results.

TABLE 60. YIELD SENSITIVITY ANALYSIS

Process	Yield	Cumulative Cost ($/W)	New Yield	New Cumulative Cost ($/W)	Simulated Cumulative Cost ($/W)
ETCHWAFER	0.99	0.3086	0.94	0.3244	0.3250
ETCHWAFER	0.99	0.3086	0.79	0.3840	0.3866
ARRAYASSM	0.98	0.6676	0.93	0.7027	0.7035
ARRAYASSM	0.98	0.6676	0.78	0.8350	0.8387

D. DISCUSSION

The essential points which emerge from the preceding cost analyses are detailed below.

- In order to achieve the 1986 goal of $0.70/W with the recommended process sequence, 6-in.-diameter wafers (or equivalent area) must be used at the same throughput rate and yield assumed for the 3-in.-diameter case. The key advantage of using a 6-in.-diameter starting wafer is the effective quadrupling of the throughput which reduces the cost of most steps to close to the limiting materials cost. Obviously, wafers smaller than 6-in.-diameter could be used if the throughput rate in the critical steps could be increased beyond those assumed here for the 3-in.-diameter case, or if the costs associated with the panel fabrication and/or metallization (see below) could be further reduced. The throughput rates used in this analysis were arrived at by carefully considered extrapolations of either those rates observed in our process sequence studies or of estimates provided by vendors for future machines similar to those used in our work, so that substantial increases beyond those values will require new machine development.

• The SAMICS price estimates for sequences I, II, and III are all above the $0.70/W goal. Because of the higher cell-efficiency (13%) obtained in the case of sequence III, it has the lowest cost of these three sequences, and on an equal efficiency basis would compare favorably with the RCA3 diffused-junction sequence. In similar fashion then, it could be argued that sequence III processing scaled-up to use 6-in.-diameter wafers would result in a price close to the $0.70/W goal. Similar arguments could be made for sequence I and II, if higher efficiencies could be obtained for these cases. If these improvements in efficiency could be achieved, and if then compatibility problems which we experienced in working with these processes were removed, then these sequences would be viable candidates for achieving the cost goal. However, it should be stressed that the compatibility problem relating to the screen-printed contact on ion-implanted layers was experienced with all three sequences and no method to obviate the problem was found. To achieve the high yields assumed for these sequences either an alternative metallization process should be explored and/or additional research be directed toward an understanding of the problem.

• A major cost-driver in all cases is the array assembly step. For the double-glass PVB laminate used here, a cost of $0.196/W was arrived at in the most optimistic case. Of that total, $0.152/W was required for direct materials and supplies, so that to achieve a lower cost for panel fabrication, less expensive substitute materials (i.e., EVA* in place of PVB) or a different panel configuration (soft-back) will be required. The double-glass design was selected because of the excellent environmental protection and structural strength it provides. These virtues are not reflected in the SAMICS cost analysis, but would be of considerable importance in other methods of estimating the cost of PV systems over projected lifetimes such as the life-cycle cost method [21].

• A second important cost-driver is metallization. Even in the most optimistic case the total cost of the process steps associated with front and back metallization is over $0.07/W of a total of $0.688/W. This cost

*EVA = ethylene-vinyl acetate

21. R. G. Ross, Jr., presentation at 13th IEEE Photovoltaic Specialists Conference, Washington, D.C., June 5-8, 1979.

is dominated by the cost of the silver metal in the ink used for the front-grid and for a solderable (Ag) back-pad. The recent work of Bernd Ross [22] in which a screen-on copper-based ink was successfully used for back contacting indicates that the full advantages of low-cost screen-printed contacts may be achievable.

22. Bernd Ross Associates, "Development of Economical, Improved Thick-Film Solar-Cell Contact," Contract No. DOE/JPL 955164.

SECTION VII

CONCLUSIONS

The major conclusion of importance to the LSA project is that we were able to identify a manufacturing sequence which can produce solar cells with the desired performance and which when fully automated can be projected to meet the 1986 price goal of $0.70/W. That sequence was described in Section V and is repeated here as Fig. 91 along with the prices arrived at in the cost analysis of Secton VI. This sequence was arrived at after considerable research, development, and evaluation of many processes, and the experimental study of three related manufacturing sequences. The successes and problem areas identified in that work form a body of experience which can be drawn upon as the need arises. Those processes have been documented here and in our other contract reports covering the period October 1977 through December 1979. The highlights of that work along with the major conclusions drawn follow.

A. JUNCTION FORMATION - ION-IMPLANTATION AND $POCl_3$ DIFFUSION

A comprehensive study of the use of ion implantation for junction formation and BSF formation was undertaken and completed. As a result of that study, optimized implant parameters and furnace-annealing condition were found which allow for the fabrication of 14 to 15% (AM-1) efficient solar cells when metallized with conventional evaporated Ti/Ag contacts. In this work, the furnace-annealing process provided to JPL by Spire [1] was verified, and in addition, an alternate and equally effective annealing process was developed and provided to JPL. The details of this work can best be found in the Interim Report, DOE/JPL-954868-79/1, Jan. 1979 and in reference 23.

In the study of the integration of the above ion-implantation techniques into manufacturing sequences, an incompatibility was identified relating to screen-printed contacts on the implanted layers. The details of this problem were described in Section V.D of this report. It was found that junction formation by $POCl_3$ diffusion is compatible with the screen-printing process and resulted in a compatible and cost/performance effective sequence.

23. E. C. Douglas and R. V. D'Aiello, IEEE Trans. Electron. Devices ED-27, 792 (1980).

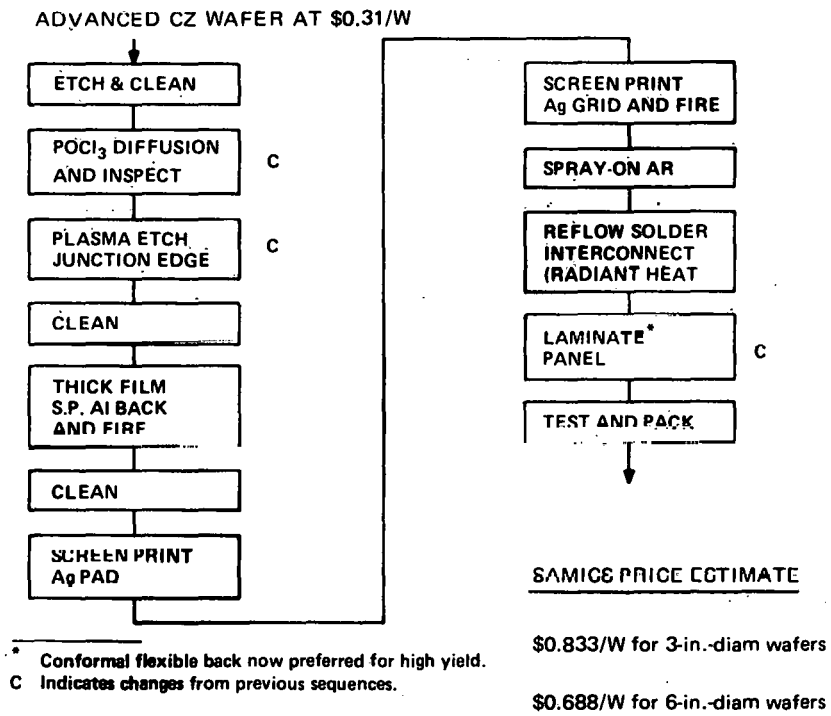


Figure 91. Recommended manufacturing sequence.

B. SCREEN-PRINTED THICK-FILM METALLIZATION

A thick-film, screen-printed metallization process was successfully developed for both the front and back contact. A screen-printable lead borosilicate-doped silver-based ink was synthesized at RCA specifically for application to solar-cell metallization. Material constituents and the electrical conductivity, solderability, and adhesion were measured as a function of ink composition and firing conditions. As a result of these evaluations, optimum material and process parameters were established for screen-printing and firing the ink on solar cells.

Commercially available silver inks were also explored, and one such ink TFS* 3347 was found to be suitable for the formation of the front-grid pattern.

Production-type screen printers were surveyed and it was found that many commercially available models can be readily modified for screen printing on round or rectangular silicon wafers with linear dimensions up to 6 inches.

*Thick Film Systems, Santa Barbara, CA.

Machines exist which are almost totally automated and have throughputs in excess of 3000 wafers/hour. A model CP-885* was purchased and used throughout the process assessment phase of this program. This machine was found to be highly suitable in terms of reliability and yield, and with the use of standard screens, an acceptable line definition (5 mil) for collector-grid patterns was readily achieved.

Infrared lamps arranged in symmetrical horizontal pairs were adapted for use in firing the front and back contacts simultaneously. This method was found to provide a rapid and controllable firing process with reasonably wide tolerance in firing temperature and time.

As part of our process sequence development (Sequence I) it was necessary to verify an aluminum, p^+, BSF back-contact process.** We verified the aluminum ink synthesis, printing and firing of the ink to form an effective ohmic back contact. Air-firing of the aluminum ink resulted in the formation of an adherent oxide film which was somewhat difficult to remove. To allow for current collection, and solder bonding to the back of the cell, a small-area grid/pad of silver or copper can be printed and fired over the remaining Si-Al eutectic.

C. SPRAY-ON AR COATING PROCESS

A cost-effective spray-on process was developed for application of anti-reflective (AR) film coatings. An organometallic (TiO_2) liquid solution was synthesized specifically for application by a spray-on process and made adaptable to commercial spray machines. A model 9000 Zicon*** autocoater was used to verify this process as part of our process sequence studies. SAMICS cost analyses show a projected cost for the spray-on AR process of about \$0.02/W for 3-in.-diameter wafers and \$0.01/W for 6-in.-diameter wafers. We have verified this process for the case of $POCl_3$ junction cells with screen-printed metallization and consider it ready for implementation in large-scale solar-cell production.

*Manufactured by AMI-PRESCO, North Branch, NJ.
**Process developed by Spectrolab, Inc., Sylmar, CA and process specification provided to RCA by JPL.
***Zicon Corp., Mt. Vernon, NY.

D. ELECTRICAL TESTING

Rapid and accurate methods of testing and the acquisition of cell performance data has always been an important part of our research and development programs. During the course of this work, two solar simulators along with the associated electronics were developed. The first system, whose initial development predates this contract, is relatively simple and inexpensive, but useful for laboratory testing of a small number of cells. This system is shown in Fig. 92. The simulator consists of an array of three ELH lamps mounted horizontally over a thermoelectrically cooled cell-stage. The output of the solar cell under test is fed into an electronic sweeper (arrow in Fig. 92) which allows for the semiautomatic plotting of the illuminated I-V and power curve on an x-y recorder. The design and construction of the electronic sweeper was not part of the present contract; however, a duplicate model was provided to PP&E at JPL for evaluation. This simulator system provided a simple, reliable, and accurate means of cell testing in a laboratory environment. We have also provided a similar system along with instructions in its use to Kulicke and Soffa as an aid in their contract work with JPL [24].

A computer-aided simulator measurement system capable of providing rapid test and data acquisition was designed, built, and used to analyze cell performance during our production sequence studies. This system is described in Section V.B.

E. PANEL ASSEMBLY

The major objective of our panel assembly work was to develop a production process for the lamination of double-glass PVB panels. Although we have identified process procedures and parameters which can be successfully used to fabricate such a panel design, the yield and throughput of this process are not sufficiently high to be cost-effective within the limits set by the LSA cost goals. We therefore cannot recommend the double-glass PVB lamination process for panel fabrication because a low-yield or low-throughput in the panel assembly step would place a severe cost penalty on the overall manufacturing price.

24. Kulicke and Soffa Industries, Inc., Automated Solar Module Assembly Line, Quarterly Technical Report No. 4, DOE/JPL-955287-79/4, December 1979.

Figure 92. I-V measuring apparatus.

Our original assessment of the superior environmental protection afforded by double-glass designs remains as a major advantage of this structure. If life-cycle costs become a major consideration or if a cost-effective method of manufacture for double-glass becomes available, this structure should be reconsidered.

F. PROCESS SPECIFICATION

During the course of this contract, seven process specifications were submitted to the PP&E Task at JPL. The specifications in the form of process recipes available from JPL upon request are:

(1,2) Ion-implantation with two furnace-annealing techniques.

(3) $POCl_3$ junction formation by gaseous diffusion.

(4) Screen-printed thick-film metallization.

(5) Spray-on AR coating process.

(6) Reflow-solder interconnect process.

(7) Double-glass panel lamination process.

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APPENDIX A

SAMICS DATA

The items listed below were used in our SAMICS analysis but were not in the SAMICS cost catalog.

Process Referent Descriptive Name	
RWAFER	Receive purchased wafer
ETCHWAFER	Sodium hydroxide wafer etch, 1.5 mil/side
MSCLN-1,2,3	Megasonic cleaning: advanced system
POCL3DEP	Phosphorous oxychloride deposition and diffusion
PDI:10%	Post diffusion inspection, 10% sample rate
JUNCEPE	Junction edge plasma etch
SPALBACK	Screen print Al on back of wafer & fire (100% coverage)
SPAGPAD	Screen print Ag pad on back of wafer (2% coverage)
SPAGFRONT	Screen print Ag grid on front of wafer (9% coverage)
HFDIP	Glass removal
SPRAYAR	Spray-on antireflection coating
TEST	Test cell
RSINTERCN	Reflow solder interconnection
ARRAYASSM	Glass/PVB/cell array assembly
FRAMEASSM	Frame assembly
PACKAGING	Array module packaging
IONIMPLPJ	Ion implantation:phosphorous, $2x10^{15}$, 10 keV, junction side
4HRANNEAL	4-hour furnace anneal
BORONDEP	Boron deposition back of wafer
900DEGDIF	900°C degree diffusion for half-hour
GLASSREM	Glass removal
CONGRD	Contact grid on back of wafer
IONIMPLBB	Ion implantation:Boron, $2x10^{15}$, 10 keV, backside

Cost items not in catalog:

Referent	Descriptive Name	$(1980)	Unit
EWRCA	Wafer, CZ, 75 mm, 14 mil	0.14[+]	Slice
EG1548D	PVB sheet	0.30	Sq ft
EPSET	Panel connector set	1.42	Connector
EG1165D	Bus bars	0.12	Bus bar
ERTRD	Transducer sets	413.19	Set
EG1116D	AR coating	0.004	cm^3
E1072R	Solder-coated CU strap	0.04	Ft
EFRRCA	Freon 14	1.53	Lb
EWRCA6	Wafer, CZ, 150 mm, 14 mil	0.51	Slice
EG15910	Boron nitride source wafers	11.41	Wafer

[+]Price specified by JPL at $0.31/W.

APPENDIX B

FORMAT A SHEETS

SOLAR ARRAY MANUFACTURING INDUSTRY COSTING STANDARDS

FORMAT A

JET PROPULSION LABORATORY
California Institute of Technology
4800 Oak Grove Dr. / Pasadena, Calif. 91103

PROCESS DESCRIPTION

Note: Names given in brackets [ ] are the names of process attributes requested by the SAMIS III computer program.

A1 Process [Referent] R Wafer

A2 [Descriptive Name] Receive Purchased Wafer

PART 1 – PRODUCT DESCRIPTION

A3 [Product Referent] P Wafer

A4 Descriptive Name [Product Name] Purchased Wafer

A5 Unit Of Measure [Product Units] Slices

PART 2 – PROCESS CHARACTERISTICS

A6	[Output Rate] (Not Thruput)	60	Units (given on line A5) Per Operating Minute
A7	Average Time at Station [Processing Time]	.02	Calendar Minutes (Used only to compute in-process inventory)
A8	Machine "Up" Time Fraction [Usage Fraction]	1.00	Operating Minutes Per Minute

PART 3 – EQUIPMENT COST FACTORS (Machine Description)

A9	Component [Referent]	RWAF		
A9a	Component [Descriptive Name] (Optional)	Received Wafer		
A10	Base Year For Equipment Prices [Price Year]	1980		
A11	Purchase Price ($ Per Component) [Purchase Cost]	0		
A12	Anticipated Useful Life (Years) [Useful Life]	0		
A13	[Salvage Value] ($ Per Component)	0		
A14	[Removal and Installation Cost] ($/Component)	0		

Note: The SAMIS III computer program also prompts for the [payment float interval], the [inflation rate table], the [equipment tax depreciation method], and the [equipment book depreciation method]. In the LSA SAMICS context, use 0.0, (1975, 6.0), DDB, and SL.

Format A: Process Description (Continued)

A15 Process Referent (From Page 1 Line A1) R Wafer

PART 4 – DIRECT REQUIREMENTS PER MACHINE (Facilities) OR PER MACHINE PER SHIFT (Personnel)
[Facilities and Personnel Requirements]

A16 Catalog Number [Expense Item Referent]	A18 Amount Required Per Machine (Per Shift) [Amount per Machine]	A19 Units	A17 Requirement Description

PART 5 – DIRECT REQUIREMENTS PER MACHINE PER MINUTE
[Byproduct Outputs] and [Utilities and Commodities Requirements]

A20 Catalog Number [Expense Item Referent]	A22 Amount Required Per Machine Per Minute [Amount per Cycle]	A23 Units	A21 Requirement Description
EWRCA	60	Wafer/Min	Wafer
or EWRCA 6	60		

PART 6 – INTRA-INDUSTRY PRODUCT(S) REQUIRED [Required Products]

A24 [Product Reference]	A28 [Yield]* (%)	A26 [Ideal Ratio]** Of Units Out/Units In	A27 Units Of A26***	A25 Product Name
			/	
			/	
			/	

Prepared by R.E. Daniel Date

* 100% minus percentage of required product lost.
** Assume 100% yield here.
*** Examples: Modules/Cell or Cells/Wafer.

SOLAR ARRAY MANUFACTURING INDUSTRY COSTING STANDARDS

FORMAT A

JET PROPULSION LABORATORY
California Institute of Technology
4800 Oak Grove Dr. / Pasadena, Calif. 91103

PROCESS DESCRIPTION

Note: Names given in brackets [ ] are the names of process attributes requested by the SAMIS III computer program.

A1 Process [Referent] SPAGFRONT

A2 [Descriptive Name] Screen print AG Grid on Front of Wafer (9% Coverage)

PART 1 – PRODUCT DESCRIPTION

A3 [Product Referent] Cellnoar

A4 Descriptive Name [Product Name] Cell, without Anti-Reflection Coating

A5 Unit Of Measure [Product Units] Slice

PART 2 – PROCESS CHARACTERISTICS

A6	[Output Rate] (Not Thruput)	60	Units (given on line A5) Per Operating Minute
A7	Average Time at Station [Processing Time]	.433	Calendar Minutes (Used only to compute in-process inventory)
A8	Machine "Up" Time Fraction [Usage Fraction]	.96	Operating Minutes Per Minute

PART 3 – EQUIPMENT COST FACTORS (Machine Description)

A9	Component [Referent]	SPAG		
A9a	Component [Descriptive Name] (Optional)	Screen Print Silver		
A10	Base Year For Equipment Prices [Price Year]	1979		
A11	Purchase Price ($ Per Component) [Purchase Cost]	62600		
A12	Anticipated Useful Life (Years) [Useful Life]	7		
A13	[Salvage Value] ($ Per Component)	12520		
A14	[Removal and Installation Cost] ($/Component)	2500		

Note: The SAMIS III computer program also prompts for the [payment float interval], the [inflation rate table], the [equipment tax depreciation method], and the [equipment book depreciation method]. In the LSA SAMICS context, use 0.0, (1975, 6.0), DDB, and SL.

Format A: Process Description (Continued)

A15 Process Referent (From Page 1 Line A1) SPAGFRONT

PART 4 – DIRECT REQUIREMENTS PER MACHINE (Facilities) OR PER MACHINE PER SHIFT (Personnel)
[Facilities and Personnel Requirements]

A16 Catalog Number [Expense Item Referent]	A18 Amount Required Per Machine (Per Shift) [Amount per Machine]	A19 Units	A17 Requirement Description
A2064D	5 E + 2	SQ. Ft.	Manuf. Space (Type A)
~~B3688D~~	2.5 E - 2	Prsn. Yrs	Elec. Maint. Man
B3064D	7 E - 1	"	Gen. Assemb. (Elec)
B3736D	5 E - 2	"	Maint. Mech. II

PART 5 – DIRECT REQUIREMENTS PER MACHINE PER MINUTE
[Byproduct Outputs] and [Utilities and Commodities Requirements]

A20 Catalog Number [Expense Item Referent]	A22 Amount Required Per Machine Per Minute [Amount per Cycle]	A23 Units	A21 Requirement Description
C1032B	1.94 E - 2	KW. HR	Elec.
E1624D	4.8 E - 2	Squeeges	Squeeges
EC1130D	3.67 E - 4	Cu. Ft.	Toluene ink solvent
E1696D	4.37 E - 2	Dollars	Thermo couple
E1064D	2.15	Grams	Paste, Silver 80%
E1576D	3. E - 3	Screens	Screen

PART 6 – INTRA-INDUSTRY PRODUCT(S) REQUIRED [Required Products]

A24 [Product Reference]	A28 [Yield]* (%)	A26 [Ideal Ratio]** Of Units Out/Units In	A27 Units Of A26***	A25 Product Name
DWAFERBM	99	1.0	Slice / Slice	Diffused wafer
			/	Back AL & AG Pad

Prepared by R.E. Daniel Date

* 100% minus percentage of required product lost.
** Assume 100% yield here.
*** Examples: Modules/Cell or Cells/Wafer.

SOLAR ARRAY MANUFACTURING INDUSTRY COSTING STANDARDS

FORMAT A

PROCESS DESCRIPTION

Note: Names given in brackets [ ] are the names of process attributes requested by the SAMIS III computer program.

A1 Process [Referent] SPALBACK

A2 [Descriptive Name] Screen print AL on back of wafer fire (100% coverage)

PART 1 – PRODUCT DESCRIPTION

A3 [Product Referent] DWAFERBM

A4 Descriptive Name [Product Name] Diffused wafer with back metallization

A5 Unit Of Measure [Product Units] slice

PART 2 – PROCESS CHARACTERISTICS

A6	[Output Rate] (Not Thruput)	60	Units (given on line A5) Per Operating Minute
A7	Average Time at Station [Processing Time]	.433	Calendar Minutes (Used only to compute in-process inventory)
A8	Machine "Up" Time Fraction [Usage Fraction]	.96	Operating Minutes Per Minute

PART 3 – EQUIPMENT COST FACTORS [Machine Description]

A9	Component [Referent]	SPAL		
A9a	Component [Descriptive Name] (Optional)	Screen Print AL		
A10	Base Year For Equipment Prices [Price Year]	1979		
A11	Purchase Price ($ Per Component) [Purchase Cost]	62650		
A12	Anticipated Useful Life (Years) [Useful Life]	7		
A13	[Salvage Value] ($ Per Component)	12520		
A14	[Removal and Installation Cost] ($/Component)	2500		

Note: The SAMIS III computer program also prompts for the [payment float interval], the [inflation rate table], the [equipment tax depreciation method], and the [equipment book depreciation method]. In the LSA SAMICS context, use 0.0, (1975, 6.0), DDB, and SL.

Format A: Process Description (Continued)

A15 Process Referent (From Page 1 Line A1) SPALBACK

PART 4 – DIRECT REQUIREMENTS PER MACHINE (Facilities) OR PER MACHINE PER SHIFT (Personnel)
(Facilities and Personnel Requirements)

A16 Catalog Number (Expense Item Referent)	A18 Amount Required Per Machine (Per Shift) (Amount per Machine)	A19 Units	A17 Requirement Description
A2064D	5 E + 2	SQ. Ft.	Manuf. Space (Type A)
B3064D	7 E - 1	Prsn. Yrs	Gen. Assemb. (Elec)
B3688D	2.5 E - 2	"	Elec. Maint. Man
B3736D	5.0 E - 2	"	Maint. Mech II

PART 5 – DIRECT REQUIREMENTS PER MACHINE PER MINUTE
(Byproduct Outputs) and (Utilities and Commodities Requirements)

A20 Catalog Number (Expense Item Referent)	A22 Amount Required Per Machine Per Minute (Amount per Cycle)	A23 Units	A21 Requirement Description
C1032B	1.94 E - 2	KW. HR.	Elec.
E1576D	3.0 E - 3	Screens	Screen
E1624D	4.8 E - 2	Squeeges	Squeeges
EG1130D	3.048 E - 4	Cu. Ft.	Toluene ink solvent
E1696D	4.368 E - 2	Dollars	Thermo couples
EP27D	4.8 E - 2	LBS	Paste, Al

PART 6 – INTRA-INDUSTRY PRODUCT(S) REQUIRED (Required Products)

A24 (Product Reference)	A28 (Yield)* (%)	A26 (Ideal Ratio)** Of Units Out/Units In	A27 Units Of A26***	A25 Product Name
CLNWF-2	98	1.0	Slice / Slice	Clean Wafer
			/	
			/	

Prepared by R.E. Daniel Date

* 100% minus percentage of required product lost.
** Assume 100% yield here.
*** Examples: Modules/Cell or Cells/Wafer.

SOLAR ARRAY MANUFACTURING INDUSTRY COSTING STANDARDS

FORMAT A

JET PROPULSION LABORATORY
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PROCESS DESCRIPTION

Note: Names given in brackets [ ] are the names of process attributes requested by the SAMIS III computer program.

A1 Process [Referent] Frameassm

A2 [Descriptive Name] Frame Assembly

PART 1 – PRODUCT DESCRIPTION

A3 [Product Referent] Array

A4 Descriptive Name [Product Name] Array Module Frame Assembly

A5 Unit Of Measure [Product Units] Frame

PART 2 – PROCESS CHARACTERISTICS

A6	[Output Rate] (Not Thruput)	1.33	Units (given on line A5) Per Operating Minute
A7	Average Time at Station [Processing Time]	1.0	Calendar Minutes (Used only to compute in-process Inventory)
A8	Machine "Up" Time Fraction [Usage Fraction]	.95	Operating Minutes Per Minute

PART 3 – EQUIPMENT COST FACTORS [Machine Description]

A9	Component [Referent]	Framer		
A9a	Component [Descriptive Name] (Optional)	Frame Assembly Equip		
A10	Base Year For Equipment Prices [Price Year]	1976		
A11	Purchase Price ($ Per Component) [Purchase Cost]	45000		
A12	Anticipated Useful Life (Years) [Useful Life]	7		
A13	[Salvage Value] ($ Per Component)	9000		
A14	[Removal and Installation Cost] ($/Component)	1000		

Note: The SAMIS III computer program also prompts for the [payment float interval], the [inflation rate table], the [equipment tax depreciation method], and the [equipment book depreciation method]. In the LSA SAMICS context, use 0.0, (1975, 6.0), DDB, and SL.

Format A: Process Description (Continued)

A15 Process Referent (From Page 1 Line A1) Frameassm

PART 4 – DIRECT REQUIREMENTS PER MACHINE (Facilities) OR PER MACHINE PER SHIFT (Personnel)
[Facilities and Personnel Requirements]

A16 Catalog Number [Expense Item Referent]	A18 Amount Required Per Machine (Per Shift) [Amount per Machine]	A19 Units	A17 Requirement Description
B3688D	2.5 E - 2	Prsn. Yrs.	Elec. Maint. Man
A2064D	2.25 E + 2	SQ. Ft.	Manuf. Space (Type A)
B3064D	6.5 E - 1	Prsn. Yrs	Gen. Assemb (Elec)
B3736D	1.0 E - 2	Prsn. Yrs.	Maint. Mech. II

PART 5 – DIRECT REQUIREMENTS PER MACHINE PER MINUTE
[Byproduct Outputs] and [Utilities and Commodities Requirements]

A20 Catalog Number [Expense Item Referent]	A22 Amount Required Per Machine Per Minute [Amount per Cycle]	A23 Units	A21 Requirement Description
C1032B	8.0 E - 3	KW HR	Elec.
E1100D	2.13 E + 1	Ft	Channel, Aluminum

PART 6 – INTRA-INDUSTRY PRODUCT(S) REQUIRED [Required Products]

A24 [Product Reference]	A28 [Yield]* (%)	A26 [Ideal Ratio]** Of Units Out/Units In	A27 Units Of A26***	A25 Product Name
Module	99.5	1.0	Frame / Array	Array Module
			/	
			/	

Prepared by _____ Date _____

* 100% minus percentage of required product lost.
** Assume 100% yield here.
*** Examples: Modules/Cell or Cells/Wafer.

SOLAR ARRAY MANUFACTURING INDUSTRY COSTING STANDARDS

FORMAT A

PROCESS DESCRIPTION

Note: Names given in brackets [ ] are the names of process attributes requested by the SAMIS III computer program.

A1 Process [Referent] MSCLN-1 (MSCLN-2 or MSCLN-3)

A2 [Descriptive Name] Megasonic Cleaning; Advanced System

PART 1 – PRODUCT DESCRIPTION

A3 [Product Referent] CLNWF-1 (CLNWF-2 or CLNWF-3)

A4 Descriptive Name [Product Name] Clean Wafer (Etched)

A5 Unit Of Measure [Product Units] Slice

PART 2 – PROCESS CHARACTERISTICS

A6 [Output Rate] (Not Thruput) 41.7 Units (given on line A5) Per Operating Minute

A7 Average Time at Station [Processing Time] 10 Calendar Minutes (Used only to compute in-process inventory)

A8 Machine "Up" Time Fraction [Usage Fraction] .9 Operating Minutes Per Minute

PART 3 – EQUIPMENT COST FACTORS [Machine Description]

A9	Component [Referent]	MSYS		
A9a	Component [Descriptive Name] (Optional)	Megasonic Cleaning System		
A10	Base Year For Equipment Prices [Price Year]	1979		
A11	Purchase Price ($ Per Component) [Purchase Cost]	46500		
A12	Anticipated Useful Life (Years) [Useful Life]	7		
A13	[Salvage Value] ($ Per Component)	0		
A14	[Removal and Installation Cost] ($/Component)	0		

Note: The SAMIS III computer program also prompts for the [payment float interval], the [inflation rate table], the [equipment tax depreciation method], and the [equipment book depreciation method]. In the LSA SAMICS context, use 0.0, (1975, 6.0), DDB, and SL.

Format A: Process Description (Continued)

A15 Process Referent (From Page 1 Line A1) MSCLN-1 (MSCLN-2 or MSCLN-3)

PART 4 – DIRECT REQUIREMENTS PER MACHINE (Facilities) OR PER MACHINE PER SHIFT (Personnel)
[Facilities and Personnel Requirements]

A16 Catalog Number [Expense Item Referent]	A18 Amount Required Per Machine (Per Shift) [Amount per Machine]	A19 Units	A17 Requirement Description
A2080D	5.0 E + 1	SQ. Ft.	Manuf. Space (Type B)
B3096D	1.0	Prsn. Yrs	Semicond. Assemb. (Elec)
~~B3088D~~	1.0 E - 1	Prsn. Yrs	Elec. Maint. Man

PART 5 – DIRECT REQUIREMENTS PER MACHINE PER MINUTE
[Byproduct Outputs] and [Utilities and Commodities Requirements]

A20 Catalog Number [Expense Item Referent]	A22 Amount Required Per Machine Per Minute [Amount per Cycle]	A23 Units	A21 Requirement Description
C1032B	8.35 E - 2	KW. HR	Elec.
E1110D	6.146 E - 4	Cu. Ft	Ammonium Hydroxide
E1336D	4.25 E - 2	LBS	Hydrogen Peroxide
E1282D	3.4 E - 3	Dollars	Filters
C1144D	1.1 E - 1	Cu. Ft.	Water Deionized
ERTRD	2.22 E - 5	Sets	Transducer Sets

PART 6 – INTRA-INDUSTRY PRODUCT(S) REQUIRED [Required Products]

	A24 [Product Reference]	A28 [Yield]* (%)	A26 [Ideal Ratio]** Of Units Out/Units In	A27 Units Of A26***	A25 Product Name
	E Wafer	99.5	1.0	Slice / Slice	Etched Wafer
(PLETWF or DWAFERBM)				/	(Edge etched wafer or Diffused wafer with back met.)
				/	

Prepared by R.E. Daniel Date

* 100% minus percentage of required product lost.
** Assume 100% yield here.
*** Examples: Modules/Cell or Cells/Wafer.

SOLAR ARRAY MANUFACTURING INDUSTRY COSTING STANDARDS

FORMAT A

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PROCESS DESCRIPTION

Note: Names given in brackets [ ] are the names of process attributes requested by the SAMIS III computer program.

A1 Process [Referent] RSINTERCN

A2 [Descriptive Name] Reflow Solder Interconnection

PART 1 – PRODUCT DESCRIPTION

A3 [Product Referent] Cell-set

A4 Descriptive Name [Product Name] Set of 225 Interconnected cells with bus bars

A5 Unit Of Measure [Product Units] layup

PART 2 – PROCESS CHARACTERISTICS

A6 [Output Rate] (Not Thruput) .22 Units (given on line A5) Per Operating Minute

A7 Average Time at Station [Processing Time] 90 Calendar Minutes (Used only to compute in-process inventory)

A8 Machine "Up" Time Fraction [Usage Fraction] .9 Operating Minutes Per Minute

PART 3 – EQUIPMENT COST FACTORS [Machine Description]

A9	Component [Referent]	RSINT		
A9a	Component [Descriptive Name] (Optional)	Reflow Solder Interconnector		
A10	Base Year For Equipment Prices [Price Year]	1977		
A11	Purchase Price ($ Per Component) [Purchase Cost]	44100		
A12	Anticipated Useful Life (Years) [Useful Life]	7		
A13	[Salvage Value] ($ Per Component)	0		
A14	[Removal and Installation Cost] ($/Component)	0		

Note: The SAMIS III computer program also prompts for the [payment float interval], the [inflation rate table], the [equipment tax depreciation method], and the [equipment book depreciation method]. In the LSA SAMICS context, use 0.0, (1975, 6.0), DDB, and SL.

Format A: Process Description (Continued)

A15 Process Referent (From Page 1 Line A1) RSINTERCN

PART 4 – DIRECT REQUIREMENTS PER MACHINE (Facilities) OR PER MACHINE PER SHIFT (Personnel)
[Facilities and Personnel Requirements]

A16 Catalog Number [Expense Item Referent]	A18 Amount Required Per Machine (Per Shift) [Amount per Machine]	A19 Units	A17 Requirement Description
A2080D	2.5 E + 2	SQ. Ft.	Manuf. Space (Type B)
B3096D	2.0	Prsn. Yrs	Semicond. Assember (Elec)
B3688D	6.0 E - 1	Prsn. Yrs	Elect. Maint. Man

PART 5 – DIRECT REQUIREMENTS PER MACHINE PER MINUTE
[Byproduct Outputs] and [Utilities and Commodities Requirements]

A20 Catalog Number [Expense Item Referent]	A22 Amount Required Per Machine Per Minute [Amount per Cycle]	A23 Units	A21 Requirement Description
C10328	1.7 E - 1	KW. HR.	Elec.
E1072R	4.5	Ft.	Solder Coated Cu. Strap
EG1165D	4.4 E - 1	Units	Bus bars

PART 6 – INTRA-INDUSTRY PRODUCT(S) REQUIRED [Required Products]

A24 [Product Reference]	A28 [Yield]* (%)	A26 [Ideal Ratio]** Of Units Out/Units In	A27 Units Of A26***	A25 Product Name
P Cells	98	.0044	Layup / Cell	Tested Cells
			/	
			/	

Prepared by R.E. Daniel Date

* 100% minus percentage of required product lost.
** Assume 100% yield here.
*** Examples: Modules/Cell or Cells/Wafer.

SOLAR ARRAY MANUFACTURING INDUSTRY COSTING STANDARDS

FORMAT A

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PROCESS DESCRIPTION

Note: Names given in brackets [ ] are the names of process attributes requested by the SAMIS III computer program.

A1 Process [Referent] PDI:10%

A2 [Descriptive Name] Post Diffusion Inspection, 10% sample rate

PART 1 – PRODUCT DESCRIPTION

A3 [Product Referent] DSLI

A4 Descriptive Name [Product Name] Diffused slice after edge polish, glass removal and inspection.

A5 Unit Of Measure [Product Units] Slice

PART 2 – PROCESS CHARACTERISTICS

A6 [Output Rate] (Not Thruput) 240 Units (given on line A5) Per Operating Minute

A7 Average Time at Station [Processing Time] 21 Calendar Minutes (Used only to compute in-process inventory)

A8 Machine "Up" Time Fraction [Usage Fraction] .8 Operating Minutes Per Minute

PART 3 – EQUIPMENT COST FACTORS (Machine Description)

A9	Component [Referent]	Probe			
A9a	Component [Descriptive Name] (Optional)	Glass Removal and Test			
A10	Base Year For Equipment Prices [Price Year]	1977			
A11	Purchase Price ($ Per Component) [Purchase Cost]	150000			
A12	Anticipated Useful Life (Years) [Useful Life]	7			
A13	[Salvage Value] ($ Per Component)	0			
A14	[Removal and Installation Cost] ($/Component)	0			

Note: The SAMIS III computer program also prompts for the [payment float interval], the [inflation rate table], the [equipment tax depreciation method], and the [equipment book depreciation method]. In the LSA SAMICS context, use 0.0, (1975, 6.0), DDB, and SL.

Format A: Process Description (Continued)

A15 Process Referent (From Page 1 Line A1) PDI:10%

PART 4 – DIRECT REQUIREMENTS PER MACHINE (Facilities) OR PER MACHINE PER SHIFT (Personnel)
[Facilities and Personnel Requirements]

A16 Catalog Number [Expense Item Referent]	A18 Amount Required Per Machine (Per Shift) [Amount per Machine]	A19 Units	A17 Requirement Description
A2080D	2.0 E + 2	SQ. Ft.	Manuf. Space (Type B)
B3096D	1.0	Prsn. Yrs	Semicond. Assemb. (Elec)
B3688D	8.0 E - 2	Prsn. Yrs	Elect. Maint. Man

PART 5 – DIRECT REQUIREMENTS PER MACHINE PER MINUTE
[Byproduct Outputs] and [Utilities and Commodities Requirements]

A20 Catalog Number [Expense Item Referent]	A22 Amount Required Per Machine Per Minute [Amount per Cycle]	A23 Units	A21 Requirement Description
C1032B	8.33 E - 2	KW. HR.	Elect.

PART 6 – INTRA-INDUSTRY PRODUCT(S) REQUIRED [Required Products]

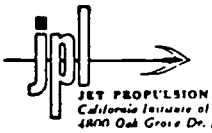
A24 [Product Reference]	A28 [Yield]* (%)	A26 [Ideal Ratio]** Of Units Out/Units In	A27 Units Of A26***	A25 Product Name
Wafer POCL	99.5	1.0	Slice / Slice	Wafer after POCL3 Diffusion
			/	
			/	

Prepared by R.E. Daniel Date

* 100% minus percentage of required product lost.
** Assume 100% yield here.
*** Examples: Modules/Cell or Cells/Wafer.

SOLAR ARRAY MANUFACTURING INDUSTRY COSTING STANDARDS

FORMAT A



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PROCESS DESCRIPTION

Note: Names given in brackets [ ] are the names of process attributes requested by the SAMIS III computer program.

A1 Process [Referent] HFDIP

A2 [Descriptive Name] Glass Removal

PART 1 – PRODUCT DESCRIPTION

A3 [Product Referent] DWafer

A4 Descriptive Name [Product Name] Diffused Wafer

A5 Unit Of Measure [Product Units] Slice

PART 2 – PROCESS CHARACTERISTICS

A6	[Output Rate] (Not Thruput)	100	Units (given on line A5) Per Operating Minute
A7	Average Time at Station [Processing Time]	30	Calendar Minutes (Used only to compute in-process inventory)
A8	Machine "Up" Time Fraction [Usage Fraction]	.85	Operating Minutes Per Minute

PART 3 – EQUIPMENT COST FACTORS [Machine Description]

A9	Component [Referent]	Oxstrip		
A9a	Component [Descriptive Name] [Optional]	Oxide Strip Station		
A10	Base Year For Equipment Prices [Price Year]	1977		
A11	Purchase Price ($ Per Component) [Purchase Cost]	80000		
A12	Anticipated Useful Life (Years) [Useful Life]	7		
A13	[Salvage Value] ($ Per Component)	0		
A14	[Removal and Installation Cost] ($/Component)	0		

Note: The SAMIS III computer program also prompts for the [payment float interval], the [inflation rate table], the [equipment tax depreciation method], and the [equipment book depreciation method]. In the LSA SAMICS context, use 0.0, (1975, 6.0), DDB, and SL.

Format A: Process Description (Continued)

A15 Process Referent (From Page 1 Line A1) HFDIP

PART 4 – DIRECT REQUIREMENTS PER MACHINE (Facilities) OR PER MACHINE PER SHIFT (Personnel)
[Facilities and Personnel Requirements]

A16 Catalog Number [Expense Item Referent]	A18 Amount Required Per Machine (Per Shift) [Amount per Machine]	A19 Units	A17 Requirement Description
A2080D	9.6 E + 1	SQ. Ft.	Manuf. Space (Type B)
B3096D	5.0 E - 1	Prsn. Yrs	Semicond. Assemb. (Elec)
B3688D	1.5 E - 1	Prsn. Yrs	Elec. Maint. Man

PART 5 – DIRECT REQUIREMENTS PER MACHINE PER MINUTE
[Byproduct Outputs] and [Utilities and Commodities Requirements]

A20 Catalog Number [Expense Item Referent]	A22 Amount Required Per Machine Per Minute [Amount per Cycle]	A23 Units	A21 Requirement Description
C1032B	5.0 E - 1	KW. HR.	Elect.
E1328D	2.2 E - 2	LBS	Acid Hydrofloris
C1144D	5.9 E - 1	Cu. Ft.	Water, Deionized

PART 6 – INTRA-INDUSTRY PRODUCT(S) REQUIRED [Required Products]

A24 [Product Reference]	A28 [Yield]* (%)	A26 [Ideal Ratio]** Of Units Out/Units In	A27 Units Of A26***	A25 Product Name
Cellnoar	99	1.0	Slice / Slice	Cell without AR
			/	
			/	

Prepared by R.E. Daniel Date

* 100% minus percentage of required product lost.
** Assume 100% yield here.
*** Examples: Modules/Cell or Cells/Wafer.

SOLAR ARRAY MANUFACTURING INDUSTRY COSTING STANDARDS

FORMAT A

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PROCESS DESCRIPTION

Note: Names given in brackets [ ] are the names of process attributes requested by the SAMIS III computer program.

A1 Process [Referent] POCL3DEP

A2 [Descriptive Name] Phosphorous Oxychloride Deposition and Diffusion

PART 1 – PRODUCT DESCRIPTION

A3 [Product Referent] WaferPOCL

A4 Descriptive Name [Product Name] Wafer after POCL3 Diffusion

A5 Unit Of Measure [Product Units] Slice

PART 2 – PROCESS CHARACTERISTICS

A6	[Output Rate] (Not Thruput)	70	Units (given on line A5) Per Operating Minute
A7	Average Time at Station [Processing Time]	60	Calendar Minutes (Used only to compute In-process Inventory)
A8	Machine "Up" Time Fraction [Usage Fraction]	.94	Operating Minutes Per Minute

PART 3 – EQUIPMENT COST FACTORS [Machine Description]

A9	Component [Referent]	Fursys	Coilin	
A9a	Component [Descriptive Name] (Optional)	Furnace System	Coils Liners	
A10	Base Year For Equipment Prices [Price Year]	1977	1977	
A11	Purchase Price ($ Per Component) [Purchase Cost]	92600	13600	
A12	Anticipated Useful Life (Years) [Useful Life]	7	7	
A13	[Salvage Value] ($ Per Component)	0	0	
A14	[Removal and Installation Cost] ($/Component)	0	0	

Note: The SAMIS III computer program also prompts for the [payment float interval], the [inflation rate table], the [equipment tax depreciation method], and the [equipment book depreciation method]. In the LSA SAMICS context, use 0.0, (1975, 6.0), DDB, and SL.

Format A: Process Description (Continued)

A15 Process Referent (From Page 1 Line A1) POCL3DEP

PART 4 – DIRECT REQUIREMENTS PER MACHINE (Facilities) OR PER MACHINE PER SHIFT (Personnel)
[Facilities and Personnel Requirements]

A16 Catalog Number [Expense Item Referent]	A18 Amount Required Per Machine (Per Shift) [Amount per Machine]	A19 Units	A17 Requirement Description
A2080D	4.5 E + 2	SQ. Ft.	Manuf. Space (Type B)
B3096D	2.5 E - 1	Prsn. Yrs	Semicond. Assemb. (Elec)
B3688D	2.5 E - 2	"	Elect. Maint. Man
B3064D	1.0 E - 1	"	Gen. Assemb. (Elec)

PART 5 – DIRECT REQUIREMENTS PER MACHINE PER MINUTE
[Byproduct Outputs] and [Utilities and Commodities Requirements]

A20 Catalog Number [Expense Item Referent]	A22 Amount Required Per Machine Per Minute [Amount per Cycle]	A23 Units	A21 Requirement Description
C1032B	1.402 E - 1	KW. HR.	Elec.
E1504D	4.54 E - 3	LBS	POCL3, Phosphorous Oxychloride
E1416D	4.69	Cu. Ft.	Nitrogen Gas, Reg Pre-Purified
E1448D	1.158 E - 1	Cu. Ft.	Oxygen Gas

PART 6 – INTRA-INDUSTRY PRODUCT(S) REQUIRED [Required Products]

A24 [Product Reference]	A28 [Yield]* (%)	A26 [Ideal Ratio]** Of Units Out/Units In	A27 Units Of A26***	A25 Product Name
CLNWF-1	99.5	1.0	Slice / Slice	Clean Wafer
			/	
			/	

Prepared by R.E. Daniel Date

* 100% minus percentage of required product lost.
** Assume 100% yield here.
*** Examples: Modules/Cell or Cells/Wafer.

SOLAR ARRAY MANUFACTURING INDUSTRY COSTING STANDARDS

FORMAT A

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PROCESS DESCRIPTION

Note: Names given in brackets [ ] are the names of process attributes requested by the SAMIS III computer program.

A1 Process [Referent] Etch Wafer

A2 [Descriptive Name] Sodium hydroxide wafer etch, 1.5 mils/side

PART 1 – PRODUCT DESCRIPTION

A3 [Product Referent] E Wafer

A4 Descriptive Name [Product Name] Etched Wafer

A5 Unit Of Measure [Product Units] Slice

PART 2 – PROCESS CHARACTERISTICS

A6 [Output Rate] (Not Thruput) 60 Units (given on line A5) Per Operating Minute

A7 Average Time at Station [Processing Time] 30 Calendar Minutes (Used only to compute in-process inventory)

A8 Machine "Up" Time Fraction [Usage Fraction] .95 Operating Minutes Per Minute

PART 3 – EQUIPMENT COST FACTORS (Machine Description)

A9	Component [Referent]	EWAF		
A9a	Component [Descriptive Name] (Optional)	NAOH Wafer Etch System		
A10	Base Year For Equipment Prices [Price Year]	1978		
A11	Purchase Price ($ Per Component) [Purchase Cost]	10000		
A12	Anticipated Useful Life (Years) [Useful Life]	7		
A13	[Salvage Value] ($ Per Component)	2000		
A14	[Removal and Installation Cost] ($/Component)	300		

Note: The SAMIS III computer program also prompts for the [payment float interval], the [inflation rate table], the [equipment tax depreciation method], and the [equipment book depreciation method]. In the LSA SAMICS context, use 0.0, (1975, 6.0), DDB, and SL.

Format A: Process Description (Continued)

A15 Process Referent (From Page 1 Line A1) Etch Wafer

PART 4 – DIRECT REQUIREMENTS PER MACHINE (Facilities) OR PER MACHINE PER SHIFT (Personnel)
(Facilities and Personnel Requirements)

A16 Catalog Number (Expense Item Referent)	A18 Amount Required Per Machine (Per Shift) (Amount per Machine)	A19 Units	A17 Requirement Description
A2064D	1.0 E + 2	SQ. Ft.	Manuf. Space (Type A)
B3064D	1.0	Prsn. Yrs	Gen. Assemb. (Elec)
B3736D	1.5 E - 1	"	Maint. Mech. II

PART 5 – DIRECT REQUIREMENTS PER MACHINE PER MINUTE
(Byproduct Outputs) and (Utilities and Commodities Requirements)

A20 Catalog Number (Expense Item Referent)	A22 Amount Required Per Machine Per Minute (Amount per Cycle)	A23 Units	A21 Requirement Description
C1032B	8.35 E - 1	KW. HR	Elec.
C1144D	3.5 E - 4	Cu. Ft	Water-Deionized
E1600D	2.05 E - 2	LBS	Sodium Hydroxide

PART 6 – INTRA-INDUSTRY PRODUCT(S) REQUIRED (Required Products)

A24 (Product Reference)	A28 (Yield)* (%)	A26 (Ideal Ratio)** Of Units Out/Units In	A27 Units Of A26***	A25 Product Name
PWafer	99	1.0	Slice / Slice	Purchased Water
			/	
			/	

Prepared by R.E. Daniel Date

* 100% minus percentage of required product lost.
** Assume 100% yield here.
*** Examples: Modules/Cell or Cells/Wafer.

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PROCESS DESCRIPTION

Note: Names given in brackets [ ] are the names of process attributes requested by the SAMIS III computer program.

A1 Process [Referent] Ionimplpj

A2 [Descriptive Name] Ion Implantation: Phosphorous, 2E 15, 10 Kev, Junction side

PART 1 – PRODUCT DESCRIPTION

A3 [Product Referent] IF Wafer

A4 Descriptive Name [Product Name] Ion Implanted Wafer

A5 Unit Of Measure [Product Units] Slice

PART 2 – PROCESS CHARACTERISTICS

A6	[Output Rate] (Not Thruput)	150	Units (given on line A5) Per Operating Minute
A7	Average Time at Station [Processing Time]	45	Calendar Minutes (Used only to compute in-process inventory)
A8	Machine "Up" Time Fraction [Usage Fraction]	.85	Operating Minutes Per Minute

PART 3 – EQUIPMENT COST FACTORS [Machine Description]

A9	Component [Referent]	EXIMPLP		
A9a	Component [Descriptive Name] (Optional)	Extrion Ion Implanter		
A10	Base Year For Equipment Prices [Price Year]	1980		
A11	Purchase Price ($ Per Component) [Purchase Cost]	200000		
A12	Anticipated Useful Life (Years) [Useful Life]	7		
A13	[Salvage Value] ($ Per Component)	40000		
A14	[Removal and Installation Cost] ($/Component)	6000		

Note: The SAMIS III computer program also prompts for the [payment float interval], the [inflation rate table], the [equipment tax depreciation method], and the [equipment book depreciation method]. In the LSA SAMICS context, use 0.0, (1975, 6.0), DDB, and SL.

Format A: Process Description (Continued)

A15 Process Referent (From Page 1 Line A1) Ionimplpj

PART 4 – DIRECT REQUIREMENTS PER MACHINE (Facilities) OR PER MACHINE PER SHIFT (Personnel)
[Facilities and Personnel Requirements]

A16 Catalog Number (Expense Item Referent)	A18 Amount Required Per Machine (Per Shift) (Amount per Machine)	A19 Units	A17 Requirement Description
A2064D	450	SQ. Ft.	Manuf. Space (Type A)
B3672D	1.0	Prsn. Yrs	Chem. Op. II
B3688D	.15	Prsn. Yrs	Elect. Maint. Man

PART 5 – DIRECT REQUIREMENTS PER MACHINE PER MINUTE
[Byproduct Outputs] and [Utilities and Commodities Requirements]

A20 Catalog Number (Expense Item Referent)	A22 Amount Required Per Machine Per Minute (Amount per Cycle)	A23 Units	A21 Requirement Description
C10323	5.0 E - 1	KW. HR.	Elec.
C1080D	2.25 E - 2	Cu. Ft.	Nitrogen, Liquid
C1128D	2.67	Cu. Ft.	Water, Cooling
EM1460D	1.55 E - 6	Cu. Ft.	Phosphine Gas

PART 6 – INTRA-INDUSTRY PRODUCT(S) REQUIRED [Required Products]

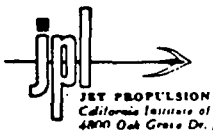
A24 [Product Reference]	A28 [Yield]* (%)	A26 [Ideal Ratio]** Of Units Out/Units In	A27 Units Of A26***	A25 Product Name
E Wafer	99	1.0	Slice / Slice	Etched Wafer
			/	
			/	

Prepared by R.E. Daniel Date

* 100% minus percentage of required product lost.
** Assume 100% yield here.
*** Examples: Modules/Cell or Cells/Wafer.

SOLAR ARRAY MANUFACTURING INDUSTRY COSTING STANDARDS

FORMAT A



PROCESS DESCRIPTION

Note: Names given in brackets [ ] are the names of process attributes requested by the SAMIS III computer program.

A1 Process [Referent] 4 Hr. Anneal

A2 [Descriptive Name] 4 Hour furnace anneal

PART 1 – PRODUCT DESCRIPTION

A3 [Product Referent] D Wafer

A4 Descriptive Name [Product Name] Diffused Wafer

A5 Unit Of Measure [Product Units] Slice

PART 2 – PROCESS CHARACTERISTICS

A6	[Output Rate] (Not Thruput)	150	Units (given on line A5) Per Operating Minute
A7	Average Time at Station [Processing Time]	240	Calendar Minutes (Used only to compute in-process inventory)
A8	Machine "Up" Time Fraction [Usage Fraction]	.95	Operating Minutes Per Minute

PART 3 – EQUIPMENT COST FACTORS (Machine Description)

A9	Component [Referent]	Furnace		
A9a	Component [Descriptive Name] (Optional)	Anneal Furnace		
A10	Base Year For Equipment Prices [Price Year]	1980		
A11	Purchase Price ($ Per Component) [Purchase Cost]	150000		
A12	Anticipated Useful Life (Years) [Useful Life]	7		
A13	[Salvage Value] ($ Per Component)	30000		
A14	[Removal and Installation Cost] ($/Component)	4500		

Note: The SAMIS III computer program also prompts for the [payment float interval], the [inflation rate table], the [equipment tax depreciation method], and the [equipment book depreciation method]. In the LSA SAMICS context, use 0.0, (1975, 6.0), DDB, and SL.

Format A: Process Description (Continued)

A15 Process Referent (From Page 1 Line A1) 4 Hr. Anneal

PART 4 – DIRECT REQUIREMENTS PER MACHINE (Facilities) OR PER MACHINE PER SHIFT (Personnel)
[Facilities and Personnel Requirements]

A16 Catalog Number [Expense Item Referent]	A18 Amount Required Per Machine (Per Shift) [Amount per Machine]	A19 Units	A17 Requirement Description
A2064D	2400	SQ. Ft.	Manuf. Space(Type A)
B3064D	1.0	Prsn. Yrs	Gen. Assemb.
B3736D	1. E - 2	Prsn. Yrs	Maint. Mech. I

PART 5 – DIRECT REQUIREMENTS PER MACHINE PER MINUTE
[Byproduct Outputs] and [Utilities and Commodities Requirements]

A20 Catalog Number [Expense Item Referent]	A22 Amount Required Per Machine Per Minute [Amount per Cycle]	A23 Units	A21 Requirement Description
C10328	3.33 E - 1	KW. HR.	Elec.
E1416D	60	Cu. Ft.	Nitrogen Gas
C11285	2.67	Cu. Ft.	Cooling-Water

PART 6 – INTRA-INDUSTRY PRODUCT(S) REQUIRED [Required Products]

A24 [Product Reference]	A28 [Yield]* (%)	A26 [Ideal Ratio]** Of Units Out/Units In	A27 Units Of A26***	A25 Product Name
CLN WF -1	99	1.0	Slice / Slice	Clean Wafer
			/	
			/	

Prepared by R.E. Daniel Date

* 100% minus percentage of required product lost.
** Assume 100% yield here.
*** Examples: Modules/Cell or Cells/Wafer.

SOLAR ARRAY MANUFACTURING INDUSTRY COSTING STANDARDS

FORMAT A

PROCESS DESCRIPTION

Note: Names given in brackets [ ] are the names of process attributes requested by the SAMIS III computer program.

A1 Process [Referent] Borondep

A2 [Descriptive Name] Boron Deposition Back of Wafer

PART 1 – PRODUCT DESCRIPTION

A3 [Product Referent] Wafer BD

A4 Descriptive Name [Product Name] Wafer, Boron Glass Deposited on Back

A5 Unit Of Measure [Product Units] Slice

PART 2 – PROCESS CHARACTERISTICS

A6 [Output Rate] (Not Thruput) 273 Units (given on line A5) Per Operating Minute

A7 Average Time at Station [Processing Time] 30 Calendar Minutes (Used only to compute in-process inventory)

A8 Machine "Up" Time Fraction [Usage Fraction] .95 Operating Minutes Per Minute

PART 3 – EQUIPMENT COST FACTORS [Machine Description]

A9	Component [Referent]	Bonid		
A9a	Component [Descriptive Name] (Optional)	Boron Nitride System		
A10	Base Year For Equipment Prices [Price Year]	1980		
A11	Purchase Price ($ Per Component) [Purchase Cost]	330000		
A12	Anticipated Useful Life (Years) [Useful Life]	7		
A13	[Salvage Value] ($ Per Component)	66000		
A14	[Removal and Installation Cost] ($/Component)	10000		

Note: The SAMIS III computer program also prompts for the [payment float interval], the [inflation rate table], the [equipment tax depreciation method], and the [equipment book depreciation method]. In the LSA SAMICS context, use 0.0, (1975, 6.0), DDB, and SL.

Format A: Process Description (Continued)

A15 Process Referent (From Page 1 Line A1) Borondep

PART 4 – DIRECT REQUIREMENTS PER MACHINE (Facilities) OR PER MACHINE PER SHIFT (Personnel)
[Facilities and Personnel Requirements]

A16 Catalog Number [Expense Item Referent]	A18 Amount Required Per Machine (Per Shift) [Amount per Machine]	A19 Units	A17 Requirement Description
A2080D	1560	SQ. Ft.	Manuf. Space (Type B)
B3064D	2.0	Prsn. Yrs	Gen. Assemb.
B3736D	2 E - 2	Prsn. Yrs	Chem. Op II

PART 5 – DIRECT REQUIREMENTS PER MACHINE PER MINUTE
[Byproduct Outputs] and [Utilities and Commodities Requirements]

A20 Catalog Number [Expense Item Referent]	A22 Amount Required Per Machine Per Minute [Amount per Cycle]	A23 Units	A21 Requirement Description
C1032B	2.1 E - 1	KW. HR.	Elec.
E1416D	29.3	Cu. Ft.	Nitrogen Gas
EG1144D	3.30 E - 2	Cu. Ft.	Hydrogen Gas
EG1121D	1. E - 2	Boat.	Boats Ceramic
EG1591D	7 E - 2	Wafer	Boron Nitride Source Wafers

PART 6 – INTRA-INDUSTRY PRODUCT(S) REQUIRED [Required Products]

A24 [Product Reference]	A28 [Yield]* (%)	A2G [Ideal Ratio]** Of Units Out/Units In	A27 Units Of A26***	A25 Product Name
C1nwf-1	99	1.0	Slice /Slice	Clean Wafer

Prepared by R.E. DANIEL Date

* 100% minus percentage of required product lost.
** Assume 100% yield here.
*** Examples: Modules/Cell or Cells/Wafer.

SOLAR ARRAY MANUFACTURING INDUSTRY COSTING STANDARDS

FORMAT A

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PROCESS DESCRIPTION

Note: Names given in brackets [ ] are the names of process attributes requested by the SAMIS III computer program.

A1 Process [Referent] 900 Degdif

A2 [Descriptive Name] 900 C Degree Diffusion For Half-Hour

PART 1 – PRODUCT DESCRIPTION

A3 [Product Referent] DWAFERNC

A4 Descriptive Name [Product Name] Diffused Wafer, Not Cleaned

A5 Unit Of Measure [Product Units] slices

PART 2 – PROCESS CHARACTERISTICS

A6 [Output Rate] (Not Thruput) 70 Units (given on line A5) Per Operating Minute

A7 Average Time at Station [Processing Time] 30 Calendar Minutes (Used only to compute in-process inventory)

A8 Machine "Up" Time Fraction [Usage Fraction] .94 Operating Minutes Per Minute

PART 3 – EQUIPMENT COST FACTORS [Machine Description]

A9	Component [Referent]	Fursys	Coilin	
A9a	Component [Descriptive Name] (Optional)	Furnace System	Coils Liners	
A10	Base Year For Equipment Prices [Price Year]	1977	1977	
A11	Purchase Price ($ Per Component) [Purchase Cost]	92600	13600	
A12	Anticipated Useful Life (Years) [Useful Life]	7	4	
A13	[Salvage Value] ($ Per Component)	18500	0	
A14	[Removal and Installation Cost] ($/Component)	3000	500	

Note: The SAMIS III computer program also prompts for the [payment float interval], the [inflation rate table], the [equipment tax depreciation method], and the [equipment book depreciation method]. In the LSA SAMICS context, use 0.0, (1975, 6.0), DDB, and SL.

Format A: Process Description (Continued)

A15 Process Referent (From Page 1 Line A1) 900 Degdif

PART 4 – DIRECT REQUIREMENTS PER MACHINE (Facilities) OR PER MACHINE PER SHIFT (Personnel)
[Facilities and Personnel Requirements]

A16 Catalog Number (Expense Item Referent)	A18 Amount Required Per Machine (Per Shift) (Amount per Machine)	A19 Units	A17 Requirement Description
A2030D	450	SQ. Ft.	Manuf. Space (Type B)
~~B3096D~~	.25	Prsn. Yrs.	Semicond. Assemb.
B3688D	2.5 E - 2	"	Elec. Maint.
B3064D	.1	"	Gen. Assemb. (Elec)

PART 5 – DIRECT REQUIREMENTS PER MACHINE PER MINUTE
[Byproduct Outputs] and [Utilities and Commodities Requirements]

A20 Catalog Number (Expense Item Referent)	A22 Amount Required Per Machine Per Minute (Amount per Cycle)	A23 Units	A21 Requirement Description
C1032B	1.4 E - 1	KW. HR.	Elec.
E1416D	4.69	Cu. Ft.	Nitrogen Gas

PART 6 – INTRA-INDUSTRY PRODUCT(S) REQUIRED [Required Products]

A24 (Product Reference)	A28 (Yield)* (%)	A26 (Ideal Ratio)** Of Units Out/Units In	A27 Units Of A26***	A25 Product Name
Wafer BD	99.5	1.0	Slice / Slice	Wafer, Boron Glass Deposited on Back
			/	
			/	

Prepared by R.E. Daniel Date

* 100% minus percentage of required product lost.
** Assume 100% yield here.
*** Examples: Modules/Cell or Cells/Wafer.

SOLAR ARRAY MANUFACTURING INDUSTRY COSTING STANDARDS

FORMAT A

PROCESS DESCRIPTION

Note: Names given in brackets [ ] are the names of process attributes requested by the SAMIS III computer program.

A1 Process [Referent] Glass Rem
Glass Removal

A2 [Descriptive Name] _____

_____

PART 1 – PRODUCT DESCRIPTION

A3 [Product Referent] D Wafer

A4 Descriptive Name [Product Name] Diffused Wafer

_____

A5 Unit Of Measure [Product Units] Slices

PART 2 – PROCESS CHARACTERISTICS

A6 [Output Rate] (Not Thruput) 100 Units (given on line A5) Per Operating Minute

A7 Average Time at Station [Processing Time] 30 Calendar Minutes (Used only to compute in-process inventory)

A8 Machine "Up" Time Fraction [Usage Fraction] .85 Operating Minutes Per Minute

PART 3 – EQUIPMENT COST FACTORS (Machine Description)

A9	Component [Referent]	Oxstrip		
A9a	Component [Descriptive Name] (Optional)	Oxide Strip Station		
A10	Base Year For Equipment Prices [Price Year]	1977		
A11	Purchase Price ($ Per Component) [Purchase Cost]	80000		
A12	Anticipated Useful Life (Years) [Useful Life]	7		
A13	[Salvage Value] ($ Per Component)	16000		
A14	[Removal and Installation Cost] ($/Component)	2400		

Note: The SAMIS III computer program also prompts for the [payment float interval], the [inflation rate table], the [equipment tax depreciation method], and the [equipment book depreciation method]. In the LSA SAMICS context, use 0.0, (1975, 6.0), DDB, and SL.

Format A: Process Description (Continued)

A15 Process Referent (From Page 1 Line A1) Glass Rem

PART 4 – DIRECT REQUIREMENTS PER MACHINE (Facilities) OR PER MACHINE PER SHIFT (Personnel)
[Facilities and Personnel Requirements]

A16 Catalog Number (Expense Item Referent)	A18 Amount Required Per Machine (Per Shift) (Amount per Machine)	A19 Units	A17 Requirement Description
A2080D	96	SQ. Ft.	Manuf. Space (Type B)
B3096D	.5	Prsn. Yrs	Semicond. Assemb.
B3688D	.15	"	Elec. Maint. Man

PART 5 – DIRECT REQUIREMENTS PER MACHINE PER MINUTE
[Byproduct Outputs] and [Utilities and Commodities Requirements]

A20 Catalog Number (Expense Item Referent)	A22 Amount Required Per Machine Per Minute (Amount per Cycle)	A23 Units	A21 Requirement Description
C1032B	.5	KW. HR.	Elec.
EI328D	2.2 E - 2	LBS	Acid Hydrofluric
CI144D	.59	Cu. Ft.	Water, Deionized

PART 6 – INTRA-INDUSTRY PRODUCT(S) REQUIRED [Required Products]

A24 [Product Reference]	A28 [Yield]* (%)	A26 [Ideal Ratio]** Of Units Out/Units In	A27 Units Of A26***	A25 Product Name
DWAFERNC	99	1.0	Slice / Slice	Diffused Wafer, No cleaned
			/	

Prepared by R.E. Daniel Date

* 100% minus percentage of required product lost.
** Assume 100% yield here.
*** Examples: Modules/Cell or Cells/Wafer.

SOLAR ARRAY MANUFACTURING INDUSTRY COSTING STANDARDS

FORMAT A

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PROCESS DESCRIPTION

Note: Names given in brackets [ ] are the names of process attributes requested by the SAMIS III computer program.

A1 Process [Referent] Congrd

A2 [Descriptive Name] Contact Grid on Back of Wafer

PART 1 – PRODUCT DESCRIPTION

A3 [Product Referent] D Wafer B:D

A4 Descriptive Name [Product Name] Diffused Wafer With Back Contact

A5 Unit Of Measure [Product Units] Slice

PART 2 – PROCESS CHARACTERISTICS

A6	[Output Rate] (Not Thruput)	60	Units (given on line A5) Per Operating Minute
A7	Average Time at Station [Processing Time]	.433	Calendar Minutes (Used only to compute in-process inventory)
A8	Machine "Up" Time Fraction [Usage Fraction]	.96	Operating Minutes Per Minute

PART 3 – EQUIPMENT COST FACTORS [Machine Description]

A9	Component [Referent]	Spag		
A9a	Component [Descriptive Name] (Optional)	Screen Printer		
A10	Base Year For Equipment Prices [Price Year]	1979		
A11	Purchase Price ($ Per Component) [Purchase Cost]	62000		
A12	Anticipated Useful Life (Years) [Useful Life]	7		
A13	[Salvage Value] ($ Per Component)	12520		
A14	[Removal and Installation Cost] ($/Component)	2500		

Note: The SAMIS III computer program also prompts for the [payment float interval], the [inflation rate table], the [equipment tax depreciation method], and the [equipment book depreciation method]. In the LSA SAMICS context, use 0.0, (1975, 6.0), DDB, and SL.

Format A: Process Description (Continued)

A15 Process Referent (From Page 1 Line A1) Congrd

PART 4 – DIRECT REQUIREMENTS PER MACHINE (Facilities) OR PER MACHINE PER SHIFT (Personnel)
[Facilities and Personnel Requirements]

A16 Catalog Number [Expense Item Referent]	A18 Amount Required Per Machine (Per Shift) [Amount per Machine]	A19 Units	A17 Requirement Description
A2064D	500	SQ. Ft.	Manuf. Space (Type B)
B3688D	2.5 E - 2	Prsn. Yrs	Elec. Maint. Man
B3064D	.7	"	Gen. Assemb. (Elec)
B3736D	5 E - 2	"	Maint. Mech. I

PART 5 – DIRECT REQUIREMENTS PER MACHINE PER MINUTE
[Byproduct Outputs] and [Utilities and Commodities Requirements]

A20 Catalog Number [Expense Item Referent]	A22 Amount Required Per Machine Per Minute [Amount per Cycle]	A23 Units	A21 Requirement Description
C10328	1.94 E - 2	KW. HR.	Elec.
E1624D	4.8 E - 2	Squeeges	Squeeges
EC1730D	3.672 E - 4	Gal.	Toluene Ink Solvent
E1696D	4.37 E - 2	Dollars	Thermo couple
E1064D	2.15	Grams	Paste, Silver 80%
E1576D	3 E - 3	Screens	Screen

PART 6 – INTRA-INDUSTRY PRODUCT(S) REQUIRED [Required Products]

A24 [Product Reference]	A28 [Yield]* (%)	A26 [Ideal Ratio]** Of Units Out/Units In	A27 Units Of A26***	A25 Product Name
D Wafer	99	1.0	Slice / Slice	Diffused Wafer
			/	
			/	

Prepared by R.E. Daniel Date

* 100% minus percentage of required product lost.
** Assume 100% yield here.
*** Examples: Modules/Cell or Cells/Wafer.

SOLAR ARRAY MANUFACTURING INDUSTRY COSTING STANDARDS

FORMAT A

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PROCESS DESCRIPTION

Note: Names given in brackets [ ] are the names of process attributes requested by the SAMIS III computer program.

A1 Process [Referent] Ionimplbb

A2 [Descriptive Name] Ion Implantation: Boron, 2E 15, 10 Kev, Back side

PART 1 – PRODUCT DESCRIPTION

A3 [Product Referent] Wafer IB

A4 Descriptive Name [Product Name] Wafer, Implanted Back

A5 Unit Of Measure [Product Units] Slice

PART 2 – PROCESS CHARACTERISTICS

A6 [Output Rate] (Not Thruput) 150 Units (given on line A5) Per Operating Minute

A7 Average Time at Station [Processing Time] 45 Calendar Minutes (Used only to compute in-process inventory)

A8 Machine "Up" Time Fraction [Usage Fraction] .85 Operating Minutes Per Minute

PART 3 – EQUIPMENT COST FACTORS [Machine Description]

A9	Component [Referent]	Eximpld		
A9a	Component [Descriptive Name] (Optional)	Extrion Ion Implanter		
A10	Base Year For Equipment Prices [Price Year]	1980		
A11	Purchase Price ($ Per Component) [Purchase Cost]	200000		
A12	Anticipated Useful Life (Years) [Useful Life]	7		
A13	[Salvage Value] ($ Per Component)	40000		
A14	[Removal and Installation Cost] ($/Component)	6000		

Note: The SAMIS III computer program also prompts for the [payment float interval], the [inflation rate table], the [equipment tax depreciation method], and the [equipment book depreciation method]. In the LSA SAMICS context, use 0.0, (1975, 6.0), DDB, and SL.

Format A: Process Description (Continued)

A15 Process Referent (From Page 1 Line A1) Ionimplbb

PART 4 – DIRECT REQUIREMENTS PER MACHINE (Facilities) OR PER MACHINE PER SHIFT (Personnel)
(Facilities and Personnel Requirements)

A16 Catalog Number (Expense Item Referent)	A18 Amount Required Per Machine (Per Shift) (Amount per Machine)	A19 Units	A17 Requirement Description
A2064D	450	SQ. Ft.	Manuf. Space (Type A)
B3672D	1.0	Prsn. Yrs	Chem. Op. II
B3688D	.15	"	Elec. Maint. Man

PART 5 – DIRECT REQUIREMENTS PER MACHINE PER MINUTE
(Byproduct Outputs) and (Utilities and Commodities Requirements)

A20 Catalog Number (Expense Item Referent)	A22 Amount Required Per Machine Per Minute (Amount per Cycle)	A23 Units	A21 Requirement Description
C1032B	5 E - 1	KW. HR.	Elec.
C1080D	2.25 E - 2	Cu. Ft.	Nitrogen, Liquid
C1128D	2.67	Cu. Ft.	Water-Cooling
EM1124D	1.55 E - 6	Cu. Ft.	Boron Triflouride Gas

PART 6 – INTRA-INDUSTRY PRODUCT(S) REQUIRED (Required Products)

A24 (Product Reference)	A28 (Yield)* (%)	A26 (Ideal Ratio)** Of Units Out/Units In	A27 Units Of A26***	A25 Product Name
IF Wafer	99	1.0	Slice / Slice	Implanted Wafer
			/	
			/	

Prepared by _____ Date _____

* 100% minus percentage of required product lost.
** Assume 100% yield here.
*** Examples: Modules/Cell or Cells/Wafer.

SOLAR ARRAY MANUFACTURING INDUSTRY COSTING STANDARDS

FORMAT A

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PROCESS DESCRIPTION

Note: Names given in brackets [ ] are the names of process attributes requested by the SAMIS III computer program.

A1 Process [Referent] Test

A2 [Descriptive Name] Test Cell

PART 1 – PRODUCT DESCRIPTION

A3 [Product Referent] P cells

A4 Descriptive Name [Product Name] Tested Cell

A5 Unit Of Measure [Product Units] Cell

PART 2 – PROCESS CHARACTERISTICS

A6 [Output Rate] (Not Thruput) 60 Units (given on line A5) Per Operating Minute

A7 Average Time at Station [Processing Time] .017 Calendar Minutes (Used only to compute in-process inventory)

A8 Machine "Up" Time Fraction [Usage Fraction] .95 Operating Minutes Per Minute

PART 3 – EQUIPMENT COST FACTORS [Machine Description]

A9	Component [Referent]	Tester		
A9a	Component [Descriptive Name] (Optional)	Siltec		
		Wafer		
		Sorter		
A10	Base Year For Equipment Prices [Price Year]	1976		
A11	Purchase Price ($ Per Component) [Purchase Cost]	80000		
A12	Anticipated Useful Life (Years) [Useful Life]	7		
A13	[Salvage Value] ($ Per Component)	16000		
A14	[Removal and Installation Cost] ($/Component)	2400		

Note: The SAMIS III computer program also prompts for the [payment float interval], the [inflation rate table], the [equipment tax depreciation method], and the [equipment book depreciation method]. In the LSA SAMICS context, use 0.0, (1975, 6.0), DDB, and SL.

Format A: Process Description (Continued)

A15 Process Referent (From Page 1 Line A1) Test

PART 4 – DIRECT REQUIREMENTS PER MACHINE (Facilities) OR PER MACHINE PER SHIFT (Personnel)
(Facilities and Personnel Requirements)

A16 Catalog Number (Expense Item Referent)	A18 Amount Required Per Machine (Per Shift) (Amount per Machine)	A19 Units	A17 Requirement Description
B3688D	2.5 E - 2	Prsn. Yrs	Elect. Maint. Man
A2064D	1.0 E + 2	SQ. Ft.	Manuf. Space (Type A)
B3064D	2.5 E - 1	Prsn. Yrs	Gen. Assemb. (Elect.)

PART 5 – DIRECT REQUIREMENTS PER MACHINE PER MINUTE
(Byproduct Outputs) and (Utilities and Commodities Requirements)

A20 Catalog Number (Expense Item Referent)	A22 Amount Required Per Machine Per Minute (Amount per Cycle)	A23 Units	A21 Requirement Description
C1032B	2.5 E - 1	KW HR.	Elect.

PART 6 – INTRA-INDUSTRY PRODUCT(S) REQUIRED (Required Products)

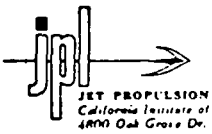
A24 (Product Reference)	A28 (Yield)* (%)	A26 (Ideal Ratio)** Of Units Out/Units In	A27 Units Of A26***	A25 Product Name
Cellar	98	1.0	Cell / Slice	Cell with AR Coating
			/	
			/	

Prepared by R.E. Daniel Date

* 100% minus percentage of required product lost.
** Assume 100% yield here.
*** Examples: Modules/Cell or Cells/Wafer.

SOLAR ARRAY MANUFACTURING INDUSTRY COSTING STANDARDS

FORMAT A



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PROCESS DESCRIPTION

Note: Names given in brackets [ ] are the names of process attributes requested by the SAMIS III computer program.

A1 Process [Referent] Arrayassm

A2 [Descriptive Name] Glass/PVB/Cell Array Assembly

PART 1 – PRODUCT DESCRIPTION

A3 [Product Referent] Module

A4 Descriptive Name [Product Name] Array Module Consisting of 1 layup of 225 cells. (needs frame)

A5 Unit Of Measure [Product Units] Array

PART 2 – PROCESS CHARACTERISTICS

A6 [Output Rate] (Not Thruput) 1.2 Units (given on line A5) Per Operating Minute

A7 Average Time at Station [Processing Time] 60 Calendar Minutes (Used only to compute in-process inventory)

A8 Machine "Up" Time Fraction [Usage Fraction] .94 Operating Minutes Per Minute

PART 3 – EQUIPMENT COST FACTORS [Machine Description]

A9	Component [Referent]	Assemb.		
A9a	Component [Descriptive Name] (Optional)	Array Assembler		
A10	Base Year For Equipment Prices [Price Year]	1978		
A11	Purchase Price ($ Per Component) [Purchase Cost]	200000		
A12	Anticipated Useful Life (Years) [Useful Life]	7		
A13	[Salvage Value] ($ Per Component)	20000		
A14	[Removal and Installation Cost] ($/Component)	6000		

Note: The SAMIS III computer program also prompts for the [payment float interval], the [inflation rate table], the [equipment tax depreciation method], and the [equipment book depreciation method]. In the LSA SAMICS context, use 0.0, (1975, 6.0), DDB, and SL.

Format A: Process Description (Continued)

A15 Process Referent (From Page 1 Line A1) Arrayassm

PART 4 – DIRECT REQUIREMENTS PER MACHINE (Facilities) OR PER MACHINE PER SHIFT (Personnel)
(Facilities and Personnel Requirements)

A16 Catalog Number (Expense Item Referent)	A18 Amount Required Per Machine (Per Shift) (Amount per Machine)	A19 Units	A17 Requirement Description
B3688D	1.5 E – 2	Prsn. Yrs	Elec. Maint. Man
A2064D	1.75 E + 3	SQ. Ft.	Manuf. Space (Type A)
B3064D	1.2	Prsn. Yrs	Gen. Assemb (Elec)

PART 5 – DIRECT REQUIREMENTS PER MACHINE PER MINUTE
(Byproduct Outputs) and (Utilities and Commodities Requirements)

A20 Catalog Number (Expense Item Referent)	A22 Amount Required Per Machine Per Minute (Amount per Cycle)	A23 Units	A21 Requirement Description
C1032B	4.63 E – 1	KW HR	Elect.
EGI548D	4.074 E + 1	SQ. Ft.	PVB Sheet
E1812D	4.074 E + 1	SQ. Ft.	Glass, Float 1/8 inch Soda Lime
EPSET	1.2	SET	Panel Connector Set

PART 6 – INTRA-INDUSTRY PRODUCT(S) REQUIRED (Required Products)

A24 (Product Reference)	A28 (Yield)* (%)	A26 (Ideal Ratio)** Of Units Out/Units In	A27 Units Of A26***	A25 Product Name
Cell-Set	98	1.0	Array / Layup	Set of 225 Inter. cells
			/	
			/	

Prepared by R.E. Daniel **Date**

* 100% minus percentage of required product lost.
** Assume 100% yield here.
*** Examples: Modules/Cell or Cells/Wafer.

SOLAR ARRAY MANUFACTURING INDUSTRY COSTING STANDARDS

FORMAT A

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PROCESS DESCRIPTION

Note: Names given in brackets [ ] are the names of process attributes requested by the SAMIS III computer program.

A1 Process [Referent] SPAGPAD

A2 [Descriptive Name] Screen print AG Pad on Back of Wafer (2% Coverage)

PART 1 – PRODUCT DESCRIPTION

A3 [Product Referent] DWAFERBMD

A4 Descriptive Name [Product Name] Diffused Wafer, back AL + AG Pad

A5 Unit Of Measure [Product Units] Slice

PART 2 – PROCESS CHARACTERISTICS

A6	[Output Rate] (Not Thruput)	60	Units (given on line A5) Per Operating Minute
A7	Average Time at Station [Processing Time]	.433	Calendar Minutes (Used only to compute in-process inventory)
A8	Machine "Up" Time Fraction [Usage Fraction]	.96	Operating Minutes Per Minute

PART 3 – EQUIPMENT COST FACTORS [Machine Description]

A9	Component [Referent]	SPAG		
A9a	Component [Descriptive Name] (Optional)	Screen Print Silver		
A10	Base Year For Equipment Prices [Price Year]	1978		
A11	Purchase Price ($ Per Component) [Purchase Cost]	62600		
A12	Anticipated Useful Life (Years) [Useful Life]	7		
A13	[Salvage Value] ($ Per Component)	12520		
A14	[Removal and Installation Cost] ($/Component)	2500		

Note: The SAMIS III computer program also prompts for the [payment float interval], the [inflation rate table], the [equipment tax depreciation method], and the [equipment book depreciation method]. In the LSA SAMICS context, use 0.0, (1975, 6.0), DDB, and SL.

Format A: Process Description (Continued)

A15 Process Referent (From Page 1 Line A1) SPAGPAD

PART 4 – DIRECT REQUIREMENTS PER MACHINE (Facilities) OR PER MACHINE PER SHIFT (Personnel)
(Facilities and Personnel Requirements)

A16 Catalog Number (Expense Item Referent)	A18 Amount Required Per Machine (Per Shift) (Amount per Machine)	A19 Units	A17 Requirement Description
B3688D	2.5 E - 2	Prsn. Yrs	Elec. Maint. Man
A2064D	5 E + 2	SQ. Ft.	Manuf. Space (Type A)
B3064D	7 E - 1	Prsn. Yrs	Gen. Assemb. (Elec)
B3736D	5 E - 2	"	Maint. Mech. II

PART 5 – DIRECT REQUIREMENTS PER MACHINE PER MINUTE
(Byproduct Outputs) and (Utilities and Commodities Requirements)

A20 Catalog Number (Expense Item Referent)	A22 Amount Required Per Machine Per Minute (Amount per Cycle)	A23 Units	A21 Requirement Description
C1032B	1.94 E - 2	KW. HR.	Elec
E1624D	4.8 E - 2	Squeeges	Squeeges
EC1130D	3.048 E - 4	Cu. Ft.	Toluene ink solvent
E1696D	4.368 E - 2	Dollars	Thermo couple
E1576D	3 E - 3	Screens	Screen
E1064D	4.78 E - 1	Grams	Paste, silver 80%

PART 6 – INTRA-INDUSTRY PRODUCT(S) REQUIRED (Required Products)

A24 (Product Reference)	A28 (Yield)* (%)	A26 (Ideal Ratio)** Of Units Out/Units In	A27 Units Of A26***	A25 Product Name
CLNWF-3	99.5	1.0	Slice / Slice	Clean Wafer
			/	
			/	

Prepared by R.E. Daniel Date

* 100% minus percentage of required product lost.
** Assume 100% yield here.
*** Examples: Modules/Cell or Cells/Wafer.

SOLAR ARRAY MANUFACTURING INDUSTRY COSTING STANDARDS

FORMAT A

JET PROPULSION LABORATORY
California Institute of Technology
4800 Oak Grove Dr. / Pasadena, Calif. 91103

PROCESS DESCRIPTION

Note: Names given in brackets [ ] are the names of process attributes requested by the SAMIS III computer program.

A1 Process [Referent] Sprayar

A2 [Descriptive Name] Spray on Anti-Reflection Coating

PART 1 – PRODUCT DESCRIPTION

A3 [Product Referent] Cellar

A4 Descriptive Name [Product Name] Cell with AR Coating

A5 Unit Of Measure [Product Units] Slice

PART 2 – PROCESS CHARACTERISTICS

A6	[Output Rate] (Not Thruput)	75	Units (given on line A5) Per Operating Minute
A7	Average Time at Station [Processing Time]	45	Calendar Minutes (Used only to compute in-process inventory)
A8	Machine "Up" Time-Fraction [Usage Fraction]	.90	Operating Minutes Per Minute

PART 3 – EQUIPMENT COST FACTORS [Machine Description]

A9	Component [Referent]	Arcoater		
A9a	Component [Descriptive Name] (Optional)	Zicon Model 11000		
A10	Base Year For Equipment Prices [Price Year]	1977		
A11	Purchase Price ($ Per Component) [Purchase Cost]	85000		
A12	Anticipated Useful Life (Years) [Useful Life]	7		
A13	[Salvage Value] ($ Per Component)	0		
A14	[Removal and Installation Cost] ($/Component)	0		

Note: The SAMIS III computer program also prompts for the [payment float interval], the [inflation rate table], the [equipment tax depreciation method], and the [equipment book depreciation method]. In the LSA SAMICS context, use 0.0, (1975, 6.0), DDB, and SL.

Format A: Process Description (Continued)

A15 Process Referent (From Page 1 Line A1) Sprayar

PART 4 – DIRECT REQUIREMENTS PER MACHINE (Facilities) OR PER MACHINE PER SHIFT (Personnel)
[Facilities and Personnel Requirements]

A16 Catalog Number [Expense Item Referent]	A18 Amount Required Per Machine (Per Shift) [Amount per Machine]	A19 Units	A17 Requirement Description
A2080D	4.0 E + 2	SQ FT	Manuf. Space (Type B)
B3096D	1.0	Prsn. Yrs	Semic. Assembler (Elec)
B3688D	1.0 E - 1	Prsn. Yrs	Elec. Maint. Map ./
B3224B	2.5 E - 1	Prsn. Yrs	Indust. Engr

PART 5 – DIRECT REQUIREMENTS PER MACHINE PER MINUTE
[Byproduct Outputs] and [Utilities and Commodities Requirements]

A20 Catalog Number [Expense Item Referent]	A22 Amount Required Per Machine Per Minute [Amount per Cycle]	A23 Units	A21 Requirement Description
C1032B	5.0 E - 2	Kw. Hr.	Electricity
E1416D	5.0 E - 1	Cu. FT.	Nitrogen Gas, Reg. Pre-Purifi
EG1116D	7.5 E - 3	Cu. Cm	AR Coating

PART 6 – INTRA-INDUSTRY PRODUCT(S) REQUIRED [Required Products]

A24 [Product Reference]	A20 [Yield]* (%)	A26 [Ideal Ratio]** Of Units Out/Units In	A27 Units Of A26***	A25 Product Name
DWafer	99.0	1.0	Slice / Slice	Diffused Wafer
			/	
			/	

Prepared by R.E. Daniel Date

* 100% minus percentage of required product lost.
** Assume 100% yield here.
*** Examples: Modules/Cell or Cells/Wafer.

SOLAR ARRAY MANUFACTURING INDUSTRY COSTING STANDARDS

FORMAT A

JET PROPULSION LABORATORY
California Institute of Technology
4800 Oak Grove Dr. / Pasadena, Calif. 91103

PROCESS DESCRIPTION

Note: Names given in brackets [ ] are the names of process attributes requested by the SAMIS III computer program.

A1 Process [Referent] Packaging

A2 [Descriptive Name] Array Module Packaging

PART 1 – PRODUCT DESCRIPTION

A3 [Product Referent] PSM

A4 Descriptive Name [Product Name] Packaged Array MOdule

A5 Unit Of Measure [Product Units] PSM

PART 2 – PROCESS CHARACTERISTICS

A6 [Output Rate] (Not Thruput) .6 Units (given on line A5) Per Operating Minute

A7 Average Time at Station [Processing Time] 1.0 Calendar Minutes (Used only to compute in-process inventory)

A8 Machine "Up" Time Fraction [Usage Fraction] 1.0 Operating Minutes Per Minute

PART 3 – EQUIPMENT COST FACTORS [Machine Description]

A9	Component [Referent]	MODPKR		
A9a	Component [Descriptive Name] (Optional)	Module Packaging		
A10	Base Year For Equipment Prices [Price Year]	1977		
A11	Purchase Price ($ Per Component) [Purchase Cost]	25000		
A12	Anticipated Useful Life (Years) [Useful Life]	7		
A13	[Salvage Value] ($ Per Component)	0		
A14	[Removal and Installation Cost] ($/Component)	0		

Note: The SAMIS III computer program also prompts for the [payment float interval], the [inflation rate table], the [equipment tax depreciation method], and the [equipment book depreciation method]. In the LSA SAMICS context, use 0.0, (1975, 6.0), DDB, and SL.

Format A: Process Description (Continued)

A15 Process Referent (From Page 1 Line A1) Packaging

PART 4 – DIRECT REQUIREMENTS PER MACHINE (Facilities) OR PER MACHINE PER SHIFT (Personnel)
[Facilities and Personnel Requirements]

A16 Catalog Number [Expense Item Referent]	A18 Amount Required Per Machine (Per Shift) [Amount per Machine]	A19 Units	A17 Requirement Description
B3064D	1.0	Prsn. Yrs	Gen. Assemb. (Elec)
A2064D	1.0 E + 2	SQ. FT.	Manuf. Space (Type A)

PART 5 – DIRECT REQUIREMENTS PER MACHINE PER MINUTE
[Byproduct Outputs] and [Utilities and Commodities Requirements]

A20 Catalog Number [Expense Item Referent]	A22 Amount Required Per Machine Per Minute [Amount per Cycle]	A23 Units	A21 Requirement Description
E1180D	2.0 E + 1	Cu. Ft.	Crates, Wooden

PART 6 – INTRA-INDUSTRY PRODUCT(S) REQUIRED [Required Products]

A24 [Product Reference]	A28 [Yield]* (%)	A26 [Ideal Ratio]** Of Units Out/Units In	A27 Units Of A26***	A25 Product Name
Array	100	.1	PSM / Frame	Array Module
			/	Frame Assemb.
			/	

Prepared by R.E. Daniel Date

* 100% minus percentage of required product lost.
** Assume 100% yield here.
*** Examples: Modules/Cell or Cells/Wafer.

SOLAR ARRAY MANUFACTURING INDUSTRY COSTING STANDARDS

FORMAT A

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4800 Oak Grove Dr. / Pasadena, Calif. 91103

PROCESS DESCRIPTION

Note: Names given in brackets [ ] are the names of process attributes requested by the SAMIS III computer program.

A1 Process [Referent] Juncepe

A2 [Descriptive Name] Junction Edge Plasma Etch

PART 1 – PRODUCT DESCRIPTION

A3 [Product Referent] PLETWF

A4 Descriptive Name [Product Name] Edge Etched Wafer

A5 Unit Of Measure [Product Units] Slice

PART 2 – PROCESS CHARACTERISTICS

A6	[Output Rate] (Not Thruput)	20.0	Units (given on line A5) Per Operating Minute
A7	Average Time at Station [Processing Time]	75	Calendar Minutes (Used only to compute in-process inventory)
A8	Machine "Up" Time Fraction [Usage Fraction]	.85	Operating Minutes Per Minute

PART 3 – EQUIPMENT COST FACTORS [Machine Description]

A9	Component [Referent]	Pletch	Alboat	
A9a	Component [Descriptive Name] (Optional)	Plasma Etcher	Al. Boat Holder	
A10	Base Year For Equipment Prices [Price Year]	1980	1980	
A11	Purchase Price ($ Per Component) [Purchase Cost]	30000	20	
A12	Anticipated Useful Life (Years) [Useful Life]	7	3	
A13	[Salvage Value] ($ Per Component)	0	0	
A14	[Removal and Installation Cost] ($/Component)	0	0	

Note: The SAMIS III computer program also prompts for the [payment float interval], the [inflation rate table], the [equipment tax depreciation method], and the [equipment book depreciation method]. In the LSA SAMICS context, use 0.0, (1975, 6.0), DDB, and SL.

Format A: Process Description (Continued)

A15 Process Referent (From Page 1 Line A1) Juncepe

PART 4 – DIRECT REQUIREMENTS PER MACHINE (Facilities) OR PER MACHINE PER SHIFT (Personnel)
(Facilities and Personnel Requirements)

A16 Catalog Number (Expense Item Referent)	A18 Amount Required Per Machine (Per Shift) (Amount per Machine)	A19 Units	A17 Requirement Description
A2080D	1.6 E + 1	SQ. Ft.	Manuf. Space (Type B)
B3096D	2.5 E - 1	Prsn. Yrs.	Semicon. Assemb. (Elec)
B3688D	1.5 E - 1	Prsn. Yrs.	Elec. Maint. Man

PART 5 – DIRECT REQUIREMENTS PER MACHINE PER MINUTE
(Byproduct Outputs) and (Utilities and Commodities Requirements)

A20 Catalog Number (Expense Item Referent)	A22 Amount Required Per Machine Per Minute (Amount per Cycle)	A23 Units	A21 Requirement Description
C1032B	1.67 E - 2	KW HR.	Elec.
E1416D	8.83 E - 3	Cu. Ft.	Nitrogen Gas, Reg. Pre-
			Purified
E1448D	7.06 E - 5	Cu. Ft.	Oxygen Gas
EFRRCA	4.17 E - 4	LBS	Freon 14

PART 6 – INTRA-INDUSTRY PRODUCT(S) REQUIRED (Required Products)

A24 (Product Reference)	A28 (Yield)* (%)	A26 (Ideal Ratio)** Of Units Out/Units In	A27 Units Of A26***	A25 Product Name
DSLI	99	1.0	Slice / Slice	Diffused Slice After Edge Polish
			/	
			/	

Prepared by R.E. Daniel Date

* 100% minus percentage of required product lost.
** Assume 100% yield here.
*** Examples: Modules/Cell or Cells/Wafer.

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