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THIN FILMS OF GALLIUM ARSENIDE ON LOW-COST SUBSTRATES

Final Technical Report for Period July 5, 1976—December 5, 1978

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March 1980

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Rockwell International
Electronics Research Center
Anaheim, California

U.S. Department of Energy

Solar Energy

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FINAL TECHNICAL REPORT

for the period

July 5, 1976 — December 5, 1978

R.P. Ruth, P.D. Dapkus, R.D. Dupuis, R.E. Johnson, L.A. Moudy, J.J. Yang, and R.D. Yingling

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March 1980

PREPARED FOR THE DIVISION OF SOLAR TECHNOLOGY, UNITED STATES DEPARTMENT OF ENERGY, UNDER CONTRACT NO. EY-76-C-03-1202

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ABSTRACT

Work during the final five months of the contract program is described, the results of the first year of the contract are summarized, and the activities of the entire second year (fourteen months) are reviewed in detail.

In this program the metalorganic chemical vapor deposition (MO-CVD) technique was applied to the growth of thin films of GaAs and GaAℓAs on inexpensive polycrystalline or amorphous substrate materials (primarily glasses and metals) for use in fabrication of large-area low-cost photovoltaic device structures. Trimethylgallium (TMG), arsine (AsH_3), and trimethylaluminum (TMAℓ) are mixed in appropriate concentrations at room temperature in the gaseous state and pyrolyzed at the substrate, which is heated in a vertical reactor chamber to temperatures of 700-750°C, to produce the desired film composition and properties.

The principal results achieved during the second year were the following:

1. Detailed studies of the properties of grain boundaries in polycrystalline GaAs films by the use of transport measurements as a function of temperature indicated that the grain boundary regions are depleted of majority carriers by a large density of neutral traps at the grain boundary interface, causing a barrier to majority carrier flow in the material. These interfacial traps decrease exponentially in density away from the band edge and overlap at mid-gap. Details of the development of the model are given.

2. Schottky-barrier solar cells of ~3 percent efficiency (simulated AM0 illumination, no AR coating) were demonstrated on thin-film polycrystalline GaAs n/n^+ structures on Mo sheet, Mo film/glass, and graphite substrates. The improved efficiencies were due in part to optimization of the thickness of the Au layers.

3. Substantial enhancement of average grain size in polycrystalline MO-CVD GaAs films on Mo sheet was obtained by the addition of HCℓ to the growth atmosphere during deposition. The competing etching and deposition reactions resulted in selective growth of the larger crystallites and in an increase in uniformity of grain size, as well.

4. Extensive investigation of polycrystalline thin-film p-n junctions indicated that the forward voltage of such devices is apparently limited to 0.5-0.6V. Several different structures were investigated to attempt to reduce the junction leakage currents; $p^+/i/n^+$ structures exhibited the lowest leakage.

5. A laboratory-type deposition apparatus for the formation of TiO_2 antireflection (AR) coatings by pyrolysis of titanium isopropoxide was assembled and tested, and used for growth of layers found to have the properites required for AR coatings on GaAs solar cells.

6. Detailed analyses were made of the materials and labor costs involved in the laboratory-scale fabrication of MO-CVD thin-film GaAs solar cells, and long-term consumption rates and process efficiencies with respect to the principal reactants used in the MO-CVD process were determined.

It was concluded that achievement of the DoE annual production goal for solar array power generating capacity for the year 2000 can be realized with 10-percent-efficient GaAs cells made by the MO-CVD process provided certain conditions regarding the process itself and the future availability of TMG (and thus of Ga metal) are met.

Recommendations for additional work are given.

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1. INTRODUCTION

This is the Final Report for a research program that extended from July 5, 1976, through September 4, 1977, under Energy Research and Development Administration Contract No. E(04-3)-1202 and from September 5, 1977, through December 5, 1978, under Department of Energy Contract No. EY-76-C-03-1202.

The work of the first year (through July 2, 1977) was described in detail in an interim report (Ref 1) that was issued in 1978.

Because of a delay in authorization of the renewal funding for the second year, resumption of the experimental program did not occur until October 5, 1977; the work then continued through December 5, 1978.

This report covers that 14-month period in detail, with emphasis on the activities of the final five months (July through November, 1978), since that period was not previously covered by a quarterly technical progress report.

1.1 PROGRAM OBJECTIVES AND GOALS

The long-range objective of the National Photovoltaic Conversion Program is to ensure that photovoltaic conversion systems play a significant role in the nation's energy supply by stimulating an industry capable of providing approximately 50 Gwe of installed electricity generating capacity by the year 2000.

One of the specific shorter-term objectives of the national program is to conduct research and advanced development on thin-film materials, cell structures, and advanced concentrator material systems to show the feasibility of reducing photovoltaic array costs to $300 per peak kwe by 1986, and to establish the viability of this advanced technology by the year 1990.

The Research and Advanced Development activity of the national program has among its specific technical goals the demonstration of at least 10 percent AM1 cell efficiency in more than one thin-film solar cell material or configuration by the end of FY80, with continued emphasis on reaching the longer-term goals. The latter consist primarily of (1) achieving flat-plate module or concentrator array prices (1975 dollars) of less than $0.50 per peak watt (electric) by 1986 with an annual production rate of at least 500 peak Mw of arrays/modules, and (2) achieving flat-plate module or concentrator array prices (1975 dollars) of $0.10 to $0.30 per peak watt (electric) by 1990 with an annual production rate of such arrays/modules of at least 10-20 peak Gw by the year 2000. The work of this contract was directed toward those goals specifically for thin-film GaAs solar cells on low-cost substrate materials.

The overall objective of the contract was the performance of intensive studies that would constitute an initial step in DoE's program to overcome problems and deficiencies in design and fabrication of arrays of extremely low-cost thin-film photovoltaic cells of relatively high efficiency and long life. Acquisition of further important knowledge of thin-film deposition methods and thin-film technology for polycrystalline GaAs on various substrates was also anticipated.

1.2 ADVANTAGES OF GaAs FOR THIN-FILM SOLAR CELLS

In the years since the modern era of photovoltaic cell development began in the early 1950's, considerable research and engineering have gone into achieving improvements in the single-crystal Si solar cell and into developing experimental cells of single-crystal GaAs and other compound semiconductors. The Si cell became the industry standard and has received by far the greatest amount of engineering and production effort. Arrays of Si cells have supplied reliable auxiliary power for most of the space vehicles and satellites launched throughout the world in various space programs over the past 18 years.

However, theoretical considerations (see, e.g., Ref 2) have shown that various compound semiconductors - especially GaAs - should provide significantly higher conversion efficiencies than are achievable with Si cells. Although pilot-line quantities of GaAs solar cells were fabricated many years ago, the performance of experimental arrays in actual space missions was generally disappointing (Ref 3).

However, more recent work with composite cells involving GaAs and a front layer of a GaAlAs alloy of appropriate composition, used either as a "window" layer for a cell structure with the active junction formed in the GaAs (Ref 4) or as the material forming a heterojunction at the GaAlAs-GaAs interface (Ref 5), has produced very encouraging results and cells of very high performance. This has led to renewed interest in the potential advantages of GaAs as a solar cell material and to greatly expanded activity in exploiting those advantages, which include the following:

1. The bandgap (~1.4 eV) is a better match to the solar spectrum; higher theoretical efficiencies (in excess of 20 percent) than for Si are thus to be expected.

2. The decrease of power output with increasing temperature for GaAs is about half of that for Si cells, because of the larger bandgap that allows higher temperature operation of the junction.

3. GaAs cells typically have lower minority carrier lifetimes and diffusion lengths than Si cells, and so are less susceptible to radiation damage.

4. The larger bandgap of GaAs results in higher output voltage per cell than for Si, although the current per unit area is smaller for the solar spectrum.

5. The optical absorption edge in GaAs is very steep (it is a direct-bandgap semiconductor), so most solar radiation is absorbed very near the surface, eliminating the need for thick cells to capture adequate amounts of the incident solar energy.

There are some disadvantages of GaAs relative to Si, not the least of which is related to the last item above. Because of the absorption and generation of charge pairs so close to the surface, the high surface recombination velocity that is also characteristic of GaAs (10 to 100 times that found in Si) results in reduced minority carrier collection efficiencies in junction-type devices, due to surface recombination losses. Additionally, since the minority carrier diffusion lengths in GaAs are

typically small compared with those found in single-crystal Si, very thin (0.5-1.0 μm) layers with extensive electroding (grids) are typically required on the illuminated side of the junction to reduce cell series resistance as much as possible. Even with these measures, the losses at the front of a simple GaAs cell have been found to be too high for acceptable cell operation under normal conditions.

This problem was the principal motivation for development of the window-type GaAs cell, in which a layer of another semiconductor, usually GaAlAs, is applied to the illuminated surface of the GaAs to remove the active junction region sufficiently far from the incident-light surface to reduce recombination losses, and at the same time add conductive material that reduces the series resistance of the cell. The window material must provide an interface with the GaAs that is sufficiently good structurally that the interface does not itself become a source of recombination losses. Additionally, the bandgap of the window material must be large enough that there are no significant losses of the incident solar radiation due to absorption in the window material, unless other aspects of the design allow the carriers generated by such absorption also to be collected by the active junction.

The difference in bandgap energy for GaAs and for Si means that GaAs responds only to that portion of the total solar spectrum that is to the short-wavelength side of ~0.9 μm, while Si responds to those photons to the short-wavelength side of ~1.1 μm. Although there is a significant amount of solar energy in the band between these two wavelengths, the net result of all factors that bear on photovoltaic conversion efficiency is that the theoretical values for GaAs are significantly higher than for Si (Ref 2).

The fact that GaAs is a direct-bandgap material and Si an indirect-bandgap semiconductor means that the transition from non-absorbing to absorbing is much more abrupt for GaAs than for Si in progressing from long wavelengths to shorter wavelengths, past the band edge. The large absorption coefficient of GaAs in the wavelength region to the high-energy side of its absorption edge is such that most (i.e., 90 percent or more) of the available radiation in the solar spectrum is absorbed within a thickness of 2 μm or less. A Si thickness in excess of 100 μm is required for similar absorption.

The small thickness of GaAs required for adequate absorption of solar radiation strongly suggests the use of deposited films of the material instead of bulk single-crystal wafers. This would clearly help in reducing the cost of the cell by requiring less of the expensive active material; it should also assist in the effort to reduce the weight of photovoltaic cell arrays, irrespective of whether they are intended for space or terrestrial applications. Since GaAs is more than an order of magnitude more costly than Si of comparable quality (single-crystal material) this advantage is important. However, the ultimate controlling factor remains the total cost per unit output power of the processed cells or arrays in the two cases, and not simply the relative costs of the semiconductor materials involved.

Ideally, single-crystal thin films of GaAs would be most desirable, but the known methods for producing single-crystal (i.e., epitaxial) deposited films of the III-V compounds all require single-crystal substrates (Ref 6), and this does not allow the needed extensive reduction in total materials costs. Furthermore, if only

single-crystal substrate materials are considered then there are serious limitations on the maximum area that can be achieved for the basic cell module to be fabricated by thin-film growth procedures. This reasoning leads to consideration of less expensive substrate materials that are available in relatively large areas. It also leads to the realization that the resulting thin-film cells will almost certainly be polycrystalline as grown, because of the absence of any strong ordering forces associated with the surface of such a substrate material.

Several important new considerations are introduced when thin-film polycrystalline solar cell structures are involved. One relates to the nature of the crystal grain structure in the film and to the collection of photogenerated carriers by the active barrier or junction forming the solar cell, and has been probably the main deterrent to the use of polycrystalline films for cell fabrication in the past. Thus, if the individual crystal grains are of random size and are randomly oriented on the substrate, as shown in Figure 1a, it is likely that only those crystallites intersecting both the illuminated surface and the charge-separating barrier will contribute to the photocurrent collected at the cell contacts. Carriers generated in other crystallites, such as those at the surface that do not intersect the barrier (grain "A") or those that include the barrier but do not intersect the top surface and its contact (grain "B") or those relatively deep in the film that intersect neither the barrier nor the top surface (grain "C"), will tend to be lost by trapping or recombination at the intervening grain boundaries.

A second important consideration relates to the problem of contacting the individual crystal grains in order to collect the photogenerated carriers. Many crystallites that intersect both the barrier and the top surface, such as grain "D" in Figure 1a, may not happen to be contacted by one of the top contact grid lines; only if a continuous transparent conducting contact layer can be developed will this problem be avoided completely. Otherwise, the separated carriers above the barrier in grain "D" will have to reach the top contact by traversing horizontally across one or more grain boundaries, and this introduces another consideration encountered in polycrystalline layers — the generally higher transverse sheet resistance of the material relative to similarly doped single-crystal material.

A more desirable polycrystalline growth configuration in shown in Figure 1b, in which the grains are larger and more uniform in size and the grain boundaries are depicted as being oriented predominantly normal to the film surface (and thus also normal to the barrier). In this film structure the carriers generated in the individual grains are far more likely to be collected across the barrier, except for those lost due to a lateral diffusion component that still allows them to encounter a grain boundary. The long-standing rule-of-thumb that suggests that average grain sizes must be at least of the same magnitude as the film thickness for reasonable thin-film solar cell performance has its origin in such considerations. It is still possible for crystallites in this configuration to miss contact with an element of the top contact grid (grain "E"), so the sheet resistance problem persists. However, the larger the crystallites the less severe this problem.

A complex situation can arise when one of the top contact grid elements makes direct contact with a grain boundary, as shown at F in Figure 1a and G in Figure 1b.

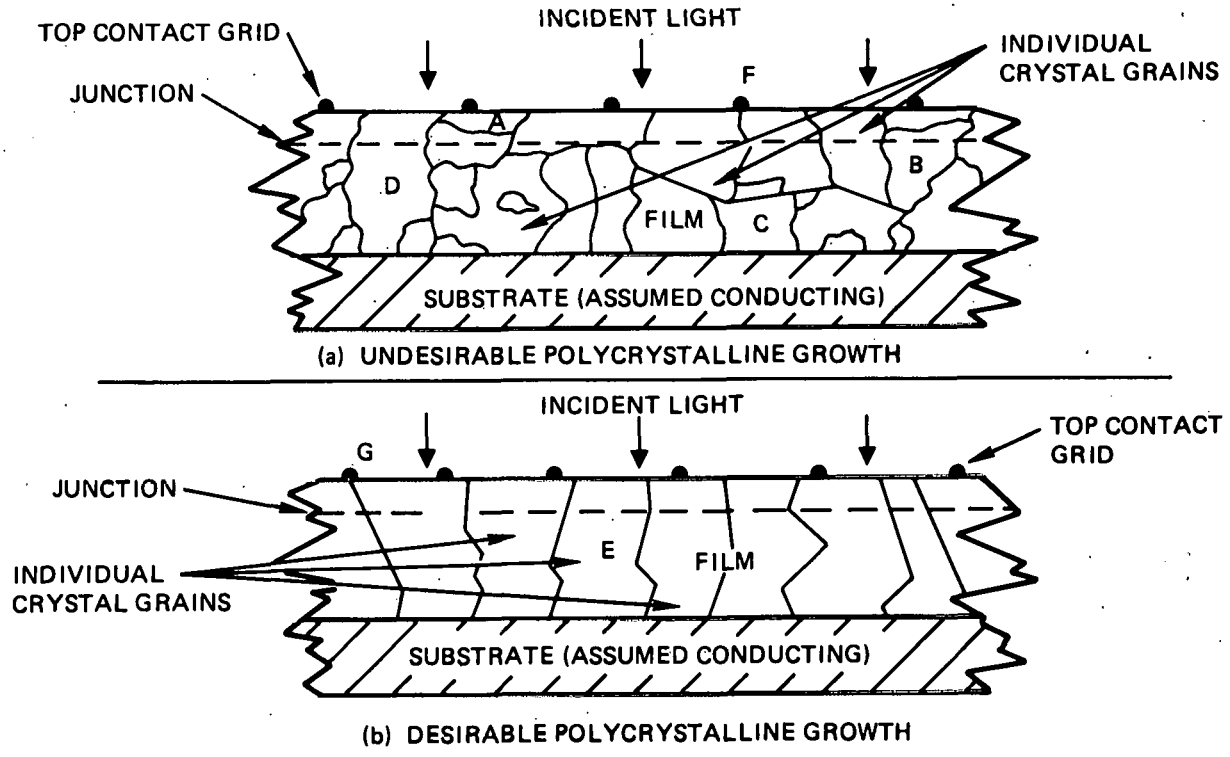

Figure 1. Two Possible Crystallite Configurations in Polycrystalline Film Solar Cells Grown on Foreign Substrates

In the latter case, the grain boundary could, depending upon its conduction properties, provide a short-circuit path between the front and back cell contacts. The consequences of the situation shown at F are not as clearly damaging to cell performance but would again depend upon the properties of the grain boundary.

The fact that GaAs thicknesses of only 1 to 2 μm are required to absorb up to 90 percent of the useful solar radiation (in the proper energy range) indicates that polycrystalline films with average grain sizes of 1 to 2 μm might be expected to exhibit respectable solar efficiencies, whereas for Si polycrystalline film cells the same criterion dictates that average grain sizes approaching 100 μm are required unless some type of surface texturing or other method is introduced to obtain comparable optical path lengths in layers of thickness less than ~100 μm.

Early attempts to predict the performance of polycrystalline GaAs thin-film solar cells were made by Woodall and Hovel (Ref 7); comparisons were made of the expected performance of GaAs cells 1 μm thick and Si cells 10 μm thick, with 1 μm average grain sizes assumed for each. Using a conservative analysis carried out by Soclof and Wes (Ref 8) for Si cell projected performance as a function of grain size as a basis, Woodall and Hovel suggested a theoretical efficiency of 11 percent for GaAs and 1.5 percent for Si cells of the above dimensional configurations. Although such predictions must be viewed with caution, there appeared to be enough validity in the analyses to suggest that significantly higher efficiencies should be expected for

polycrystalline cells in thin-film GaAs than in thin-film Si, if average grain sizes the order of only 1 μm are obtainable in both cases.

Such dimensions seemed well within the realm of achievement for GaAs films deposited on non-crystalline substrates by the chemical vapor deposition technique, so there appeared to be good prospect for fabricating thin-film solar cells that could meet the 10 percent AM1 efficiency goal of the national program. If grain sizes significantly larger than 1 μm could be achieved then the chances for success would be even better.

1.3 METALORGANIC CHEMICAL VAPOR DEPOSITION OF GaAs FOR SOLAR CELLS

The general technical approach used in this program has involved the metal-organic chemical vapor deposition (MO-CVD) technique for the growth of thin films of GaAs and GaAlAs on inexpensive polycrystalline or amorphous substrate materials in configurations permitting fabrication of photovoltaic devices. The parameters of the CVD process have been chosen to maximize the chances of achieving the required properties in the deposited films and the efficiency goal of the photovoltaic devices (10 percent AM1), subject to the constraints imposed by the properties of the selected substrate material(s).

As applied in this contract, the MO-CVD process involves the mixing of a metalorganic compound of a Group III element with a hydride or metalorganic compound of a Group V element, and pyrolysis of this mixture or its reaction product under appropriate conditions to produce the Group III-Group V semiconductor. Thus, trimethylgallium (TMG) and AsH_3 are mixed at room temperature in the gaseous state and pyrolyzed at established temperatures in a cold-wall reactor to form GaAs according to the following simplified equation:

$$(CH_3)_3\ Ga + AsH_3 \longrightarrow GaAs + 3CH_4.$$

By mixing TMG in the gas phase with trimethylaluminum (TMAl) and AsH_3, GaAlAs is obtained upon pyrolysis at appropriate temperatures; the composition of the alloy is controlled by the ratio of the reactants. The organic byproduct, methane (CH_4), is stable at film growth temperatures. In similar fashion, AlAs can be prepared from TMAl and AsH_3, if desired. Many such compounds and alloys have been prepared by the MO-CVD process (Ref 9).

The process has several attributes that are important to the application involved in this program:

1. The basic process is completely free of halides, thus eliminating competing etching reactions, reducing generation of unwanted impurities by reactions with the low-cost substrate materials, and minimizing complication of the heterogeneous film-growth process involved.

2. Only a single high-temperature zone is required, greatly simplifying the apparatus and the necessary control systems, and allowing the deposition chamber walls to remain relatively cool because only the pedestal and the samples are heated.

3. The reactants used are either liquid or gaseous at room temperature, facilitating their handling and introduction into the reactor system carrier gas upstream from the deposition chamber, and allowing control of composition of the deposited film by means of flowmeter adjustments.

4. Impurity doping of the deposited films can be achieved by introduction of appropriate dopant compounds (liquid metalorganic and/or gaseous hydride sources) into the primary reactant gas stream, with doping levels controllable by means of flowmeter adjustments.

5. Large-area, uniform surface coverage can be achieved in a single growth sequence, using the same type of commercially available apparatus that is used for epitaxial growth of elemental semiconductors if desired.

6. The process requires neither single-crystal GaAs material nor semiconductor-grade (ultrahigh-purity) polycrystalline GaAs for its application, since only compounds of Ga and of As are used in the reaction; this eliminates the expensive and energy-wasteful processes of producing melt-grown GaAs source material that is required for other crystal growth and/or film deposition techniques.

7. The growth process can be observed directly by the operator, since the reactor walls are transparent and unobstructed, thus allowing changes in growth conditions to be made during an experiment if it is desired or necessary.

The availability of high-purity reactants is a primary requisite for the ultimate success of the MO-CVD process in the application involved in this contract. This is a matter that needs considerable attention; it requires cooperation of the relatively small number of manufacturers now engaged in supplying the various compounds used for this work, to assure that materials of increasing purity and improved control of quality will become available when required in larger quantities in the future.

The general technical problems to be solved in applying the MO-CVD technique in this work were (1) identifying suitable substrate materials that survive the environment of the MO-CVD process and are potentially inexpensive and available in large areas, yet are as favorable as possible to GaAs and GaAlAs grain growth; (2) establishing preferred CVD process parameters (temperature, reactant concentrations, carrier gas composition, doping impurities, growth rate) for optimized intragrain properties of the films grown on various substrate materials; and (3) achieving adequate grain size in the films to produce satisfactory solar cell properties.

1.4 SUMMARY OF FIRST YEAR'S RESULTS

The results of the first year's activities have previously been reported in detail (Ref 1). That work verified some of the strengths of the MO-CVD process and also defined further some of the technical problems that still required attention.

The first year's investigations involved five main technical tasks:

Task 1. Substrate Material Selection, Evaluation, and Development

Task 2. CVD Experiments and Parameter Studies

Task 3. Evaluation of Film Properties

Task 4. Experimental Photovoltaic Device Fabrication and Evaluation

Task 5. Analysis and Projection of Cell Fabrication Costs

A summary of the results obtained in these five areas of activity is included here.

1.4.1 Principal Results

The principal results obtained in the first year were as follows:

1. High-efficiency epitaxial thin-window GaAlAs/GaAs solar cells were prepared by the MO-CVD process. Efficiencies as high as 12.8 percent (simulated AM0 illumination, no AR coating) were demonstrated.

2. A new highly automated MO-CVD reactor system for growth of GaAs and GaAlAs was designed, constructed, tested, and used for preparation of films, with good control and reproducibility of properties.

3. Polycrystalline GaAs films with apparent grain sizes (2-5μm) suitable for fabrication of thin-film solar cells were prepared on several low-cost or potentially low-cost substrate materials. In most cases {111} preferred orientation was observed in the films.

4. Schottky-barrier solar cells with 2.25 percent efficiency (simulated AM0 illumination, no AR coating) and short-circuit current densities up to 12.5mA/cm^2 were fabricated on thin polycrystalline GaAs films on Mo/glass composite substrates, using Au barrier-forming layers.

5. The electrical properties of polycrystalline GaAs films prepared by MO-CVD were evaluated, and it was demonstrated that the resistivities of polycrystalline films are 2-3 orders of magnitude larger than those of comparably doped single-crystal material and that charge carrier transport is dominated by the presence of grain boundaries. Ohmic contact at a GaAs/Mo interface was shown to be achievable if the donor doping in the GaAs exceeds ~10^{18} cm $^{-3}$.

6. Various characterization methods were used in studying the polycrystalline films to analyze their properties and to establish the limitations of the methods for this application. C-V measurements for carrier concentration, x-ray measurements for Al concentration, SEM EBIC-mode and etching techniques for grain size, and van der Pauw Hall-effect measurements for electrical properties were all employed to obtain useful information.

7. Studies of polycrystalline p-n junctions grown by MO-CVD were begun, but the structures obtained showed excessive leakage currents.

8. Preliminary analyses of materials and processing costs associated with the fabrication of GaAs thin-film cells by MO-CVD were prepared, and some projections of future materials requirements for large-scale production were made.

1.4.2 Summary of Activities in First Year

Ten candidate materials were initially selected for detailed experimental investigation, on the basis of a set of qualification criteria and initial experimental tests. Those evaluated most extensively included certain glasses, polycrystalline aluminas, and metals, as well as composite substrates of Mo metal films and Ge films on insulating substrates. Some of the glasses were found to be physically and/or chemically unsuited to the growth of GaAs films in H_2, as were the Kovar-like (Co-Ni-Fe alloy) metals. Mo and Ge intermediate layers deposited on Corning Code 0317 glass substrates appeared to be compatible with the MO-CVD growth of GaAs. The large-grained alumina and bulk-metal substrates were considered too expensive to meet the cost goals of the national program but were used nonetheless for experimental film growth to provide a comparison with growth on amorphous or small-grained polycrystalline substrates.

A new dedicated reactor system was designed and constructed for use in the program; it was completed in the second quarter of the contract and was used thereafter as one of three MO-CVD reactor systems employed in these investigations. MO-CVD experiments undertaken in the two primary systems established that good control and reproducibility of the doping of GaAs:Se, GaAs:Zn, and GaAlAs:Zn single-crystal films could be achieved. Doping experiments with polycrystalline GaAs films on low-cost insulating substrates established that a conducting intermediate layer probably would have to be employed to allow adequate contact to the back surface of a polycrystalline GaAs solar cell grown on such substrates. Such intermediate layers of CVD Ge and sputtered Mo were used in the experimental growth of polycrystalline GaAs n/n^+ films for the fabrication of experimental Schottky-barrier solar cells and polycrystalline GaAs p-n junction structures.

The electrical properties of the polycrystalline GaAs films were analyzed by Hall-effect measurements using the van der Pauw method, and the resistivities were found to be 2-3 orders of magnitude greater than that of single-crystal material of the same input doping level. No difference was observed in the resistivity of polycrystalline n-type and p-type GaAs of comparable doping levels. However, because it was possible to dope p-type GaAs more heavily than n-type material the lowest resistivities were achieved in p-type GaAs films.

The limits of applicability of C-V measurements for determining impurity concentration were explored. Only when a back-plane contact to the films was made available could these measurements be successfully applied. In addition, films doped higher than $\sim 10^{16}$ cm^{-3} were not successfully measured, owing to excessive leakage in the Schottky barriers.

The physical and structural properties of the polycrystalline GaAs films were examined by SEM and x-ray diffraction analysis. The films all showed similar general surface features, with apparent grain sizes of 2-10μm. The grain size most typically seen for films $\sim 5\mu$m thick was $\leq 5\mu$m in apparent horizontal dimension. Films deposited on refired Vistal alumina substrates exhibited some 1mm-size grains that had grown epitaxially on the large individual α-Al_2O_3 grains in the alumina. The preferred orientation of GaAs grown on most of the substrates was found to be {111}, but the preferred orientation of films grown on glasses was shown to vary with temperature of deposition.

Techniques for determining the Al concentration in GaAlAs films were established. Epitaxial films grown on GaAs were analyzed by electron microprobe x-ray fluorescence techniques and double-crystal x-ray lattice constant measurements to establish a working calibration curve for film composition, which was then available for use in further studies of Al concentration in polycrystalline GaAlAs films.

Techniques for the determination of grain size in polycrystalline films were explored in some detail, especially during the fourth quarter of the first year. EBIC-mode measurements in the SEM on Schottky-barrier devices on polycrystalline films demonstrated the presence of localized nonradiative recombination regions that in many cases coincided with apparent grain boundaries in the polycrystalline films.

Both single-crystal and polycrystalline experimental solar cells were grown by MO-CVD, fabricated, and evaluated. Contact technologies were explored and usable ohmic contacts developed. To establish a baseline reference of performance for cells made by the MO-CVD technique, single-crystal thin-film GaAlAs/GaAs p-n junction cell structures were prepared with thin (~500Å) $Ga_{1-x}Al_xAs$ ($x \approx 0.8$) windows and GaAs:Zn-GaAs:Se deposited junction regions. Efficiencies as high as 12.8 percent under simulated AM0 illumination with no antireflection (AR) coating were obtained, indicating the high quality of the semiconductor layers grown by the MO-CVD technique. Extrapolation of these results to those expected from similar devices with appropriate AR coatings indicated that efficiencies as high as those obtained by liquid-phase epitaxy (LPE) growth methods should be achievable with material made by the MO-CVD process.

Films with grain sizes in the $\sim 5\mu$m range were used for fabrication of polycrystalline film solar cells on a variety of substrates. Most attention was devoted to Schottky-barrier cells. The best result obtained with these devices was an efficiency of 2.25 percent for AM0 illumination and no AR coating, for n/n^+ GaAs films grown on composite Mo/glass substrates. Short-circuit current densities of up to 12.5 mA/cm^2 were achieved in such devices. The particular substrate combination of sputtered Mo on Corning Code 0317 glass was found to be a good low-cost baseline reference with which to compare other substrate materials. The GaAs-Mo interface was found to be ohmic as long as the donor impurity concentration in the GaAs film exceeded $\sim 10^{18}$ cm^{-3}.

P-n junctions in polycrystalline GaAs films were also formed by growing alternate p and n layers by MO-CVD. The electrical properties of these junction structures generally showed excessive leakage currents, resulting in soft and sometimes shorted characteristics for p-on-n devices and considerably less leaky characteristics for n-on-p devices. It was suspected that diffusion of Zn along grain boundaries may have been responsible for the leaky device characteristics.

Preliminary analyses of material and processing costs associated with the fabrication of two different conceptual designs of GaAℓAs/GaAs heterostructure solar cells - one involving the conventional configuration on an opaque substrate and one involving an inverted configuration utilizing a transparent substrate - were prepared. Some consideration was also given to the future material requirements and costs of producing such cells in large quantity. The principal conclusions reached from these analyses were as follows:

1. Reduction by a factor of 10 to 15 in the cost of the input semiconductor materials relative to present values would probably permit thin-film GaAℓAs/GaAs cells to meet the 1986 DoE cost goals.

2. Substrate cost appeared to be the predominant factor in the overall materials costs for thin-film GaAℓAs/GaAs solar cells; glasses appeared as potentially the best substrate material prospect for allowing total array costs to come within the established DoE goals.

3. Added-value costs of ~$17 per m^2 for fabrication of large-area films of GaAs and a similar figure for cell and array fabrication, borrowed from the DoE/JPL LSSA Project, were adopted as reasonable 1986 cost goals for GaAs low-cost solar array fabrication.

4. In terms of deposited thin-film GaAℓAs/GaAs solar cells on substrates of materials other than single-crystal GaAs, there appears to be enough recoverable Ga metal in projected future bauxite ore supplies to meet the DoE solar array production goals for the years 1986 and 2000, especially if improvements in Ga recovery technology are introduced to increase process efficiencies by relatively modest amounts.

5. The MO-CVD process for fabrication of GaAs cells appears adaptable to continuous or semicontinuous manufacture of large-area thin-film cells in the quantities required for meeting the DoE 1986 and 2000 production goals, primarily through design of the necessary scaled-up apparatus and through development of companion processes for producing satisfactory substrates at sufficiently low cost.

The results of the first year's work demonstrated that the MO-CVD technique is capable of producing materials of quality sufficient to meet the goals of the national photovoltaic conversion program, and that the technique is also a strong candidate for eventual use in fabrication of single-crystal GaAℓAs/GaAs cells for high-efficiency applications (e.g., space power supplies), with or without concentrator systems.

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2. RESULTS OF SECOND YEAR'S INVESTIGATIONS

The contract Statement of Work for the experimental program that began on October 5, 1977, specified that the contract activity should fall within the following technical task areas:

1. Evaluate the use of glass, glass-ceramic and graphite as low-cost substrates and perform the detailed analysis and experimental studies necessary to grow thin films of GaAs with enhanced grain size on these substrates by the metalorganic chemical vapor deposition technique.

2. Perform the proposed parametric studies and measurements to determine the pertinent mechanical, electrical, and optical properties of the films, with special emphasis on adherence, morphology, uniformity, doping, carrier concentration, mobility, lifetime, properties of the electrical contact adjacent to the substrate, and the properties of grain boundaries and the role they have in determining the microscopic properties of the polycrystalline films.

3. Investigate epitaxial growth, diffusion, ion implantation, indium tin oxide, and thin Au Schottky barriers for the formation of collecting junctions in polycrystalline GaAs.

4. Develop the optimal solar cell design and fabrication techniques for the fabrication of thin-film GaAs photovoltaic devices with a conversion efficiency greater than 10 percent, and evaluate the electrical and optical performance of the cells.

5. Determine estimated cost, quality, and requirements of the feedstock materials as appropriate for scaled-up production of 50,000 Mw/year.

6. Beginning with the inception of the contract, supply a minimum of 4 cm^2 of representative samples of current production of thin films each month to DoE, for whatever purpose DoE deems suitable.

The second year's investigations were planned to emphasize further substrate development as well as improved understanding of the properties and effects of grain boundaries in the polycrystalline films. In addition, further attention was to be devoted to junction formation techniques and techniques yielding larger grain sizes. Further development of solar cell fabrication technology, including contacts and AR coatings, was also to be undertaken.

To pursue such a program the work of the second year was organized into five main technical tasks:

Task 1. Experimental Evaluation of Low-cost Substrates and Methods for Obtaining Enhanced Grain Size in MO-CVD Films

Task 2. Evaluation of Film Properties and Grain Boundary Effects and Correlation with CVD Growth Parameters

Task 3. Investigation and Development of Barrier Formation Techniques

Task 4. Development of Photovoltaic Device Designs and Fabrication Techniques

Task 5. Analysis and Projection of Cell Material Requirements and Fabrication Costs.

The review of these investigations given in this report follows the above task descriptions.

2.1 TASK 1. EXPERIMENTAL EVALUATION OF LOW-COST SUBSTRATES AND METHODS FOR OBTAINING ENHANCED GRAIN SIZE IN MO-CVD FILMS

The primary activities of this task involved evaluation of various low-cost substrate materials - such as glasses and graphite - for use in GaAs MO-CVD film growth and experimental studies and analyses directed at obtaining thin films of GaAs with enhanced grain size on one or more of these materials using the MO-CVD process. Work in these two areas is reviewed in the following two sections.

2.1.1 Evaluation of Various Low-cost Substrate Materials

The potential substrate materials prepared and used at various times in the second year of the program included the following:

Corning Code 0317 glass

Sputtered polycrystalline Mo films on glass (Corning Code 0317, Corning Code 7059, Corning Code 1723)

CVD-grown polycrystalline Ga films on glass (0317, 7059, 1723)

Annealed (large-grained) bulk Mo sheet

Polycrystalline bulk large-grained GaAs

Commercial-grade bulk Al alloy sheet

Large-grained polycrystalline alumina ceramic

High-density graphite (several grades)

Those materials most used included sputtered Mo films on glass, high-density graphites, bare 0317 glass, and large-grained polycrystalline alumina ceramic - the last two especially in the study of the transport properties of polycrystalline doped GaAs films and the electrical properties of grain boundaries in such material, as described in detail in the Task 2 discussion (Section 2.2). Experiments with the various graphites and the other materials are discussed below.

2.1.1.1 High-density Graphite

Graphite is an attractive potential substrate for deposition of GaAs polycrystalline thin-film solar cells. The purity, conductivity and chemical inertness of several potentially low-cost grades of graphite make it an almost ideal substrate for chemical vapor deposition of GaAs polycrystalline films (Ref 10).

Six different modifications of four basic grades of high-density graphite were examined as possible substrate material for growth of GaAs by the MO-CVD process: (1) Poco Grade DFP-3 as sawed; (2) Poco Grade DFP-3 polished; (3) Poco DFP-3 polished and repurified; (4) Poco Grade ACF-10Q as sawed; (5) Poco Grade AXF-9Q as sawed; (6) Carbone-Lorraine Grade 5890 as sawed. Early in the contract year most of the experiments involved the Poco graphites, but the most encouraging results were obtained late in the program with the Carbone-Lorraine material. as indicated below.

High-purity polished Poco Grade DFP-3 graphite substrates ordered during the first year of the program were received early in the second year, but still required repolishing to provide an acceptable finish. This work was undertaken at Rockwell and resulted in improved surfaces, but small pores remained in the materials and were found to trap cleaning liquids or other materials that contacted the graphite. Some of the repolished graphite substrates were returned to Poco for repurification, to be used later as experimental substrates for GaAs film growth.

Some of the repolished (but not repurified) substrates retained by Rockwell were treated in H_2 at ~1000°C in the MO-CVD reactor and then used for growth of undoped GaAs at ~725°C, using the standard deposition procedure developed during the first year of the contract. The films were fairly reflective after light etching in a Br_2-MeOH solution and appeared to have large (10-20 μm) grains. Unfortunately, however, the film adherence was poor; the Scotch-tape test for adherence resulted in film removal, and some of the films simply peeled away from the substrate during normal handling. Because of the poor results obtained with the repolished but not repurified substrates no further film growth experiments were done with that material.

During the sixth and seventh quarters, after the substrates repurified by Poco had been received, further GaAs deposition experiments were done with that material as well as with the as-sawed modifications of the four basic graphite grades listed above. The growth of polycrystalline GaAs films on these graphite substrates at ~725°C by the MO-CVD process typically resulted in films having apparent grain sizes (as indicated by surface features) in the 2-5μm range for film thicknesses ~10μm. The as-sawed surfaces of the various graphites were not further prepared mechanically, as a rule, and only degreased in organic solvents prior to use in a deposition experiment. Typically, however, they were baked out at temperatures of 900-1000°C for 10-30 min in H_2 in the CVD reactor chamber before GaAs film growth was begun. Only minor differences were seen in the results obtained with the various graphites during these experiments - not sufficient to indicate a preference for any one of them at that stage of the investigations.

The effects of various cleaning and baking procedures and coatings (specifically, thin films of Ge and Mo) upon the photovoltaic properties of cells formed in polycrystalline GaAs grown on the four grades of graphite were investigated.

Typical surfaces for GaAs films grown on unpolished surfaces of these graphites are shown in the SEM photographs in Figure 2. Grain sizes at the surface range from less than 1 μm to~10μm, with slightly different crystal growth habit evident for each of the four cases. The films shown in Figure 2 were grown simultaneously in a single deposition experiment, with average thicknesses of 4-5μm and a deposition temperature of 725°C.

No substantial difference was found in the photovoltaic device performance achieved on films grown on any of the four graphites in this case. Evaluation was accomplished by the use of n/n+ structures consisting of n+ layers doped to $N_D \approx 5 \times 10^{18}$ cm^{-3} and undoped n layers with $N_D - N_A \approx 2 \times 10^{15}$ cm^{-3}. The n+ layer was used to provide adequate ohmic contact to the substrate. The thickness of the layers was varied by varying deposition time. Schottky-barrier solar cells were then fabricated by depositing an array of thin (~50-100Å) Au pads 0.05 x 0.05 in. on the surface. The thickness of the Au was controlled during vacuum deposition by a quartz-crystal deposition thickness monitor.

A series of devices of this type was used to provide a comparison of the effects on the quality of the deposited GaAs layer of different surface cleaning procedures used for the graphites. Representative I-V characteristics for these devices are shown in Figure 3. The data for films grown on all of the graphite substrates showed no significant or reproducible photovoltaic effect, similar to the situation illustrated in the figure. In most cases any light-induced change appeared to be a modulation of the forward resistance of the device. As indicated in the curves of Figure 3 the devices also exhibited substantially higher forward voltages than those typically observed for Schottky-barrier devices. This may have been indicative of an interface problem at the GaAs-graphite interface.

The devices illustrated by Figure 3 were prepared on substrates that had been solvent-cleaned, dried, and baked at ~1000°C in H_2 for 15 min. Increasing the bake time to 30 min and omitting the solvent cleaning made no substantial change in device performance.

To further determine the effect of substrate surface condition on device performance, samples of GaAs were then grown on graphite substrates that were coated with either Ge or Mo deposited films. The Ge films were prepared by CVD and were approximately 5μm thick. The Mo films were sputtered by the same process that was typically used for the Mo/glass substrates used in this program. Representative I-V curves for two of these samples are shown in Figure 4. Note that substantial photocurrent was generated in these devices - similar to that seen in the best devices previously grown on Mo or Mo/glass substrates.

However, the I-V characteristics measured across a given wafer showed a great deal more variation and the forward I-V characteristics were generally "softer" than for similar devices in GaAs on Mo or Mo/glass substrates. The Ge and Mo coatings on the graphite either sealed the surface of the graphite (at least in some areas) or altered the GaAs growth habit so that films with better properties resulted. The cause of the very low conversion efficiencies achieved and of the large variation in device properties observed on a given GaAs/graphite sample was not identified at first, although the possibility of cross-contamination among the several substrates used simultaneously in most experiments was recognized and prompted examination of each of the materials separately.

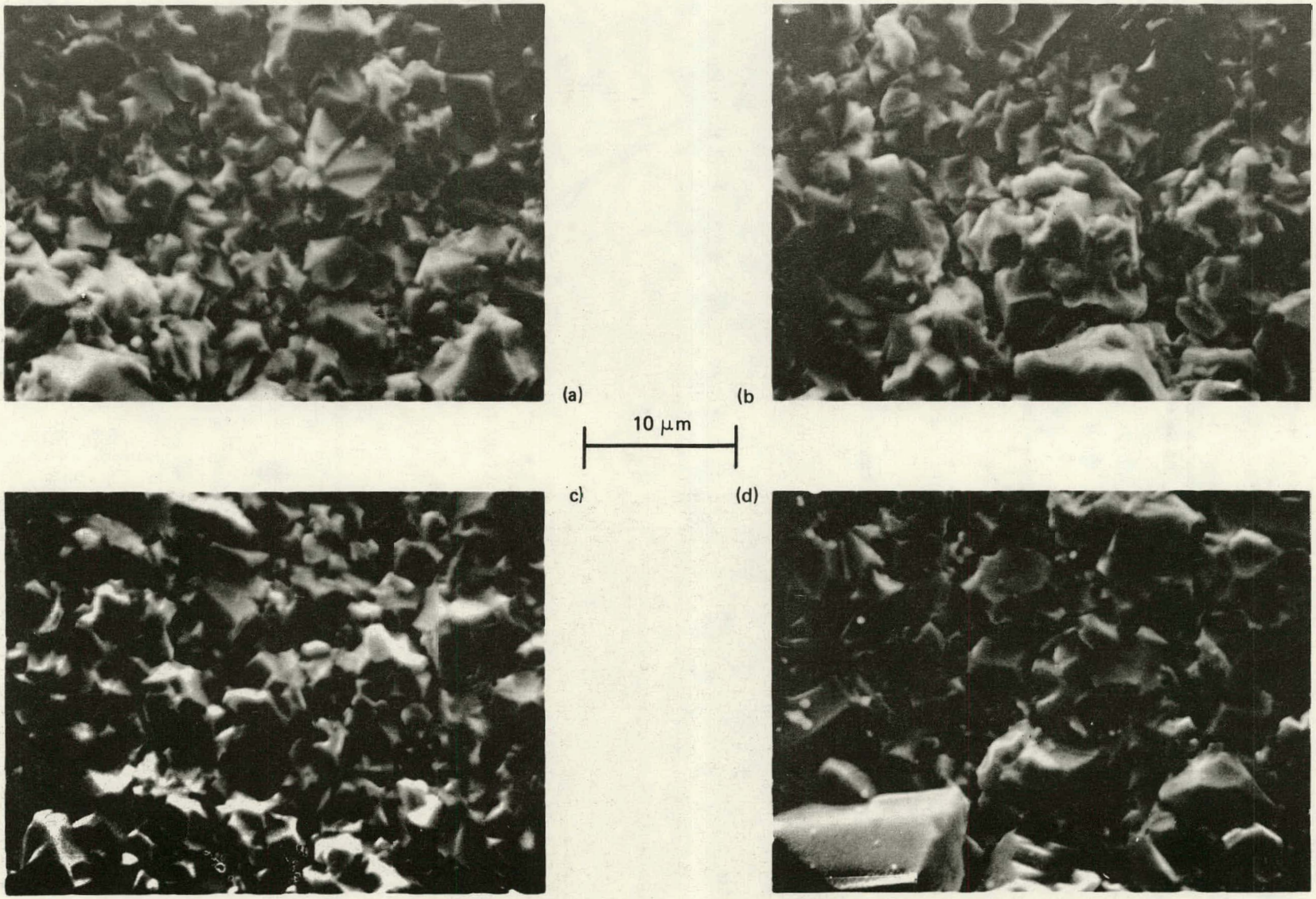


Figure 2. SEM Photographs of Surfaces of GaAs Films Grown by MO-CVD on Several Different As-sawed Graphite Substrates: a) Carbone-Lorraine Grade 5890, b) Poco Grade DFP-3, c) Poco Grade AXF-9Q, d) Poco Grade ACF-10Q.

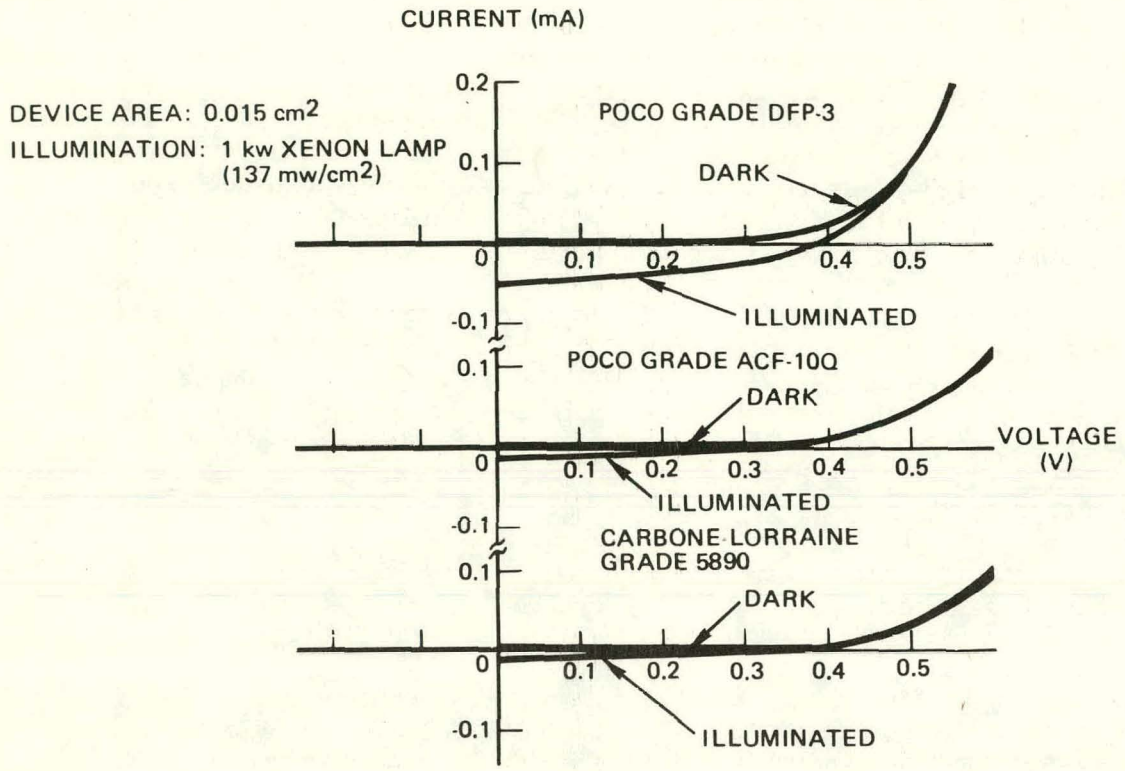


Figure 3. I-V Characteristics of Au Schottky-barrier Solar Cells on n/n+ GaAs Structures Grown by MO-CVD on Three Different Grades of Graphite

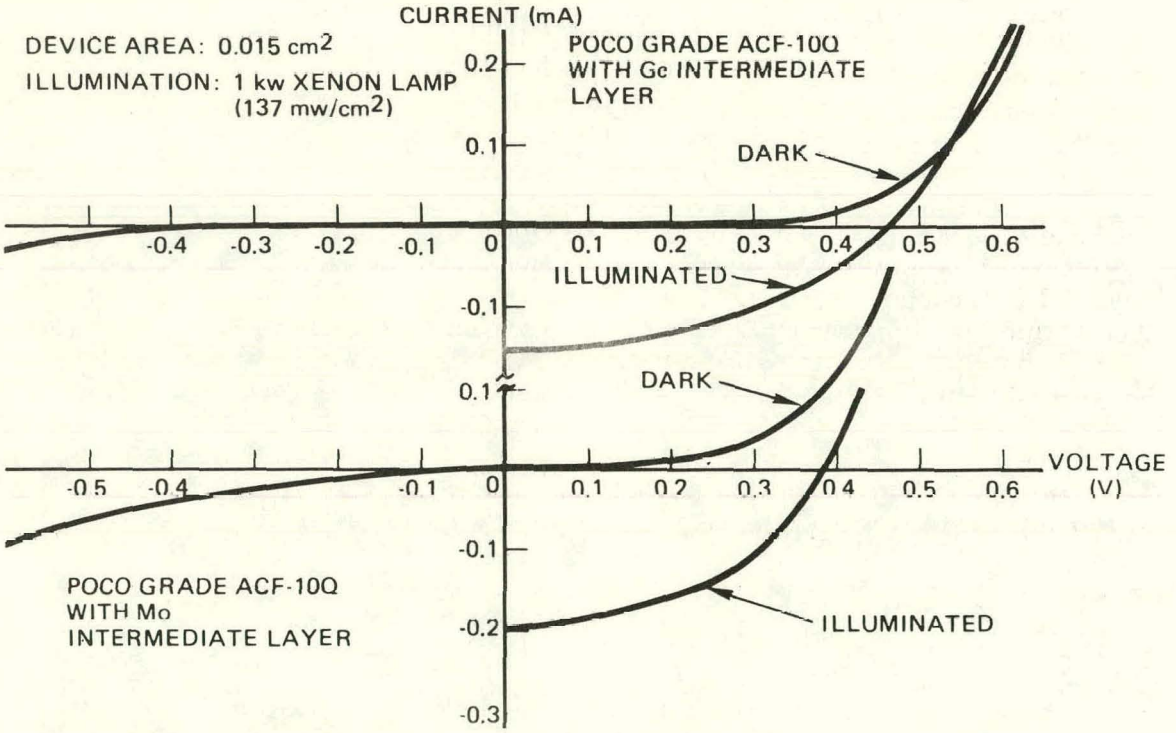


Figure 4. I-V Characteristics of Au Schottky-barrier Solar Cells on n/n+ GaAs Structures Grown by MO-CVD on Poco Grade ACF-10Q Graphite Substrates with Ge and Mo Intermediate Layers

When these separate evaluations were made a dramatic improvement was achieved for films grown on Carbone-Lorraine Grade 5890 graphite, a material previously reported by other investigators as being superior for substrate use with GaAs CVD growth (Ref 10). Significantly improved GaAs solar cell performance was realized for Schottky-barrier cells made on these polycrystalline films. Small-area (50 mil x 50 mil) individual cells exhibited efficiencies of up to 2.7 percent under illumination by a high-pressure Xe lamp, with no AR coatings applied. These results compare favorably with the best achieved for polycrystalline GaAs cells prepared on any other substrate, simple or composite, in this program.

Figure 5 shows the light and dark I-V characteristics of one such GaAs Schottky-barrier solar cell on a Carbone-Lorraine Grade 5890 substrate. The short-circuit current is comparable to the best achieved with any other substrate used in this work. Furthermore, the fill factor and the open-circuit voltage exceed the best achieved with Mo or Mo/glass substrates. Similar results were reproducibly achieved in several growth runs, and the results were also found to be relatively uniform across a large (1 in. x 1 in.) substrate.

This success however, was achieved only with the Carbone-Lorraine graphite - not with any of the others, even when they also were used separately in a given experiment. It thus appeared that the dramatic improvement in cell performance exemplified by Figure 5 (compared with Figure 3) was the result of elimination of unidentified contaminants caused by the presence of the other graphite materials of poorer quality in the reactor during the same deposition run. Although earlier experiments in which several different graphites were evaluated simultaneously in a single deposition afforded the convenience of comparing GaAs films grown on different substrates under identical conditions, they also allowed the films grown on the Carbone-Lorraine material to be adversely affected by impurities transferred via the gaseous atmosphere from the lower quality graphites present. Use of the 5890 graphite alone eliminated this problem. It is interesting, however, that no obvious contamination associated with the other grades of graphite had ever been detected visually either during or subsequent to the earlier deposition experiments.

To verify the situation, an additional deposition experiment was done with both Carbone-Lorraine 5890 and Poco AXF-9Q graphite substrates used simultaneously, after several runs had been made with Carbone-Lorraine substrates alone and had resulted in the increased efficiencies indicated above. Schottky-barrier cells were then formed on the polycrystalline GaAs films on both graphites. The cells on the film on the 5890 graphite exhibited efficiencies of only 1.6 percent at most, considerably below the previous performance.

The I-V curves for a Schottky-barrier cell on GaAs grown on the Carbone-Lorraine graphite used in this experiment are shown in Figure 6. The reduced efficiency attained was primarily caused by the much lower short-circuit current

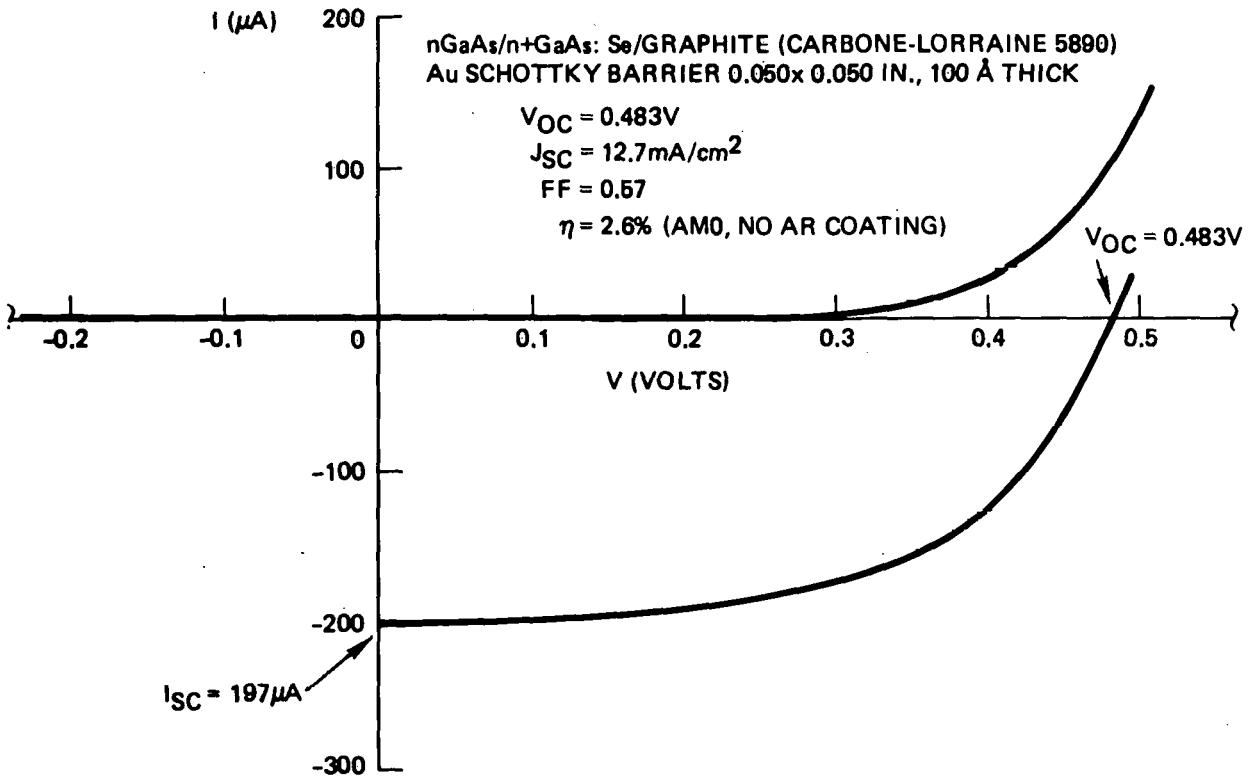


Figure 5. I-V Characteristics of Au Schottky-barrier Solar Cell on Polycrystalline n/n+ GaAs Structure Grown by MO-CVD on As-sawed Surface of Carbone-Lorraine Grade 5890 Graphite Used Alone in Reactor.

achieved with these devices. The result substantiates the hypothesis that the presence of the other graphites caused contamination of the films grown on the Carbone-Lorraine 5890 graphite and the consequent lower cell efficiencies observed.

The improved cell performance obtained with the 5890 graphite substrates, although not achieved until late in the program, was significant for the following reasons. First, it demonstrated that cells of relatively high efficiency can be made with polycrystalline GaAs films deposited directly on graphite substrates, without the need for intermediate layers (such as Mo or Ge) that were previously thought to be necessary for "sealing" the graphite surface for satisfactory GaAs growth by MO-CVD. Second, it introduced for further investigation and development another potentially low-cost substrate material that is not only conducive to growth of satisfactory GaAs films but also electrically conductive, facilitating contact to the back side of the solar cell.

Third, the encouraging results showed that growth of GaAs films by MO-CVD in the presence of HCℓ vapor, investigated in this program primarily with substrates of Mo and Mo films on glass (see Section 2.1.2), should also be undertaken with graphite as the substrate material. While Mo and Mo-coated glass substrates were found to require deposition of a thin layer of GaAs without HCℓ present before

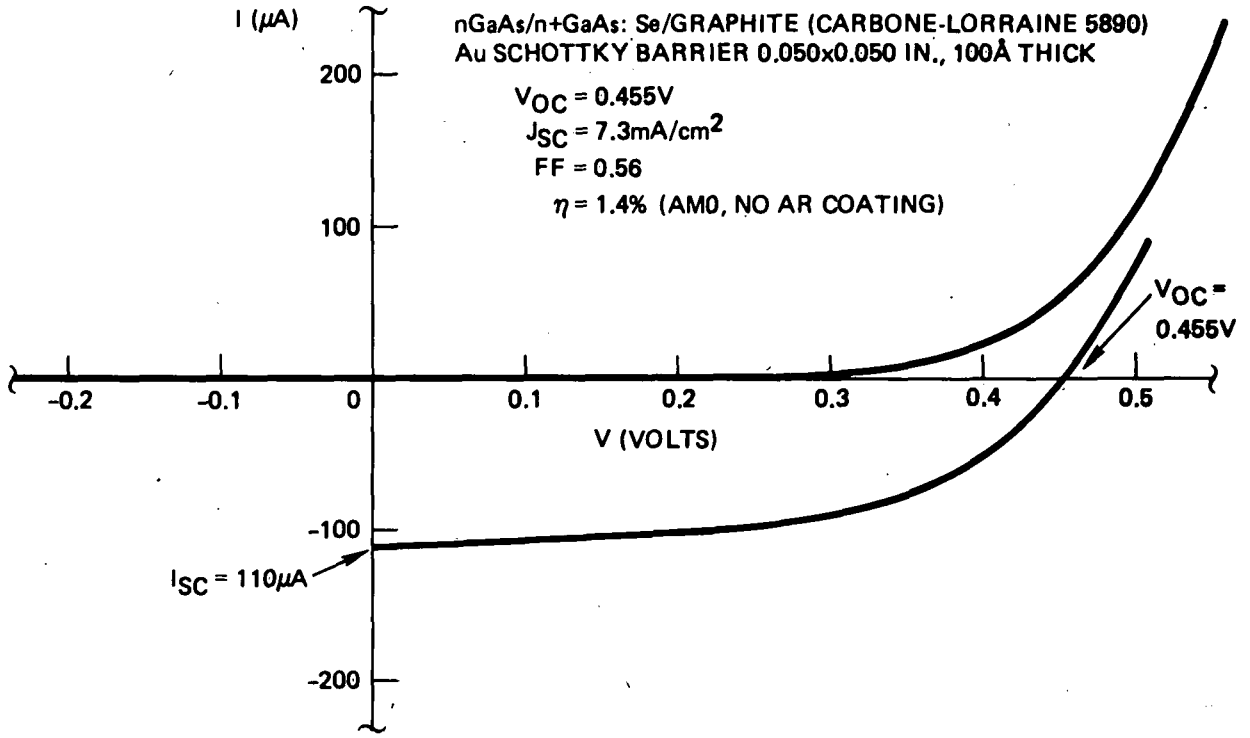


Figure 6. I-V Characteristics of Au Schottky-barrier Solar Cell on Polycrystalline n/n+ GaAs Structure Grown by MO-CVD on As-sawed Surface of Carbone-Lorraine Grade 5890 Graphite in Presence of Second Substrate of Another Grade of Graphite.

deposition with HCℓ, in order to avoid attack of the Mo surface and/or the Mo glass bond, it should be possible with graphite to initiate GaAs deposition with the HCℓ present from the beginning and thus fully realize the benefits associated with HCℓ, as described in Section 2.1.2, throughout the growth of the entire film.

2.1.1.2 Mo, Glasses, and Other Materials

Because of the success realized in the first year of the program with substrates of Mo films sputtered onto Corning Code 0317 glass wafers, that composite was again used extensively during the part of the study covered by this report. The investigation of the use of HCℓ in the MO-CVD process for growing GaAs films, described in detail in the next section (Section 2.1.2), employed Mo/glass composites as well as Mo sheet substrates. Also, the study of various device structures in polycrystalline GaAs, described in the Task 3 and Task 4 discussions in Sections 2.3 and 2.4, respectively, utilized these composite substrates involving sputtered Mo films. On the other hand, the extended investigation of the transport properties of polycrystalline GaAs films conducted in the second year (see Section 2.2) made primary use of bare Corning 0317 glass substrates and polished large-grain polycrystalline alumina substrates (Vistal, manufactured by Coors) as GaAs growth surfaces. The other substrate materials listed at the beginning of Section 2.1.1 were used much less frequently in the second year's work.

Early in the second year composite substrates consisting of sputtered Mo films ~ 2000Å thick on wafers of Corning Code 0317 glass, Corning Code 7059 glass, and Corning Code 1723 glass and also Ge films grown by CVD (GeH_4 pyrolysis) on these same glasses were prepared for use in various GaAs film growth experiments. Some substrates of annealed bulk Mo sheet having relatively large grains and others of commercial-grade Aℓ alloy sheet were also prepared for use, as were wafers of large-grained bulk polycrystalline GaAs. When such substrates were used in a deposition experiment a polished wafer of single-crystal GaAs:Si was also usually included in the run as a control substrate.

The limited investigation of annealed bulk Mo sheet took place mainly in the sixth quarter. This material had been obtained from GTE Sylvania, Inc., and had been heat-treated by the supplier at ~1000°C for various periods to produce grain growth of varying amounts. When this material was used as substrates for GaAs film deposition, however, there appeared to be no significant differences in the apparent grain size (as determined by average dimensions of surface features) of polycrystalline GaAs films grown simultaneously on the annealed Mo sheet and on conventional unannealed Mo sheet. That is, the enlarged grains in the annealed Mo substrates did not appear to influence the grain size in the GaAs films deposited by the MO-CVD process. Rather, the same factors appeared to determine the GaAs grain size on the unannealed and annealed Mo sheet, and these factors were evidently not controlled by the grain size in the Mo itself.

Even more limited evaluation was made in the sixth quarter of commercial-grade Aℓ alloy sheet as a possible substrate material for GaAs film growth. Deposition had to be carried out at temperatures below ~640°C to avoid melting the Aℓ. It was found that GaAs films deposited on Aℓ sheet at such low temperatures adhered adequately, with no evidence of the films flaking off of the Aℓ surfaces. However, growth rates were low and the film surfaces were not very good. For these reasons the work with this substrate material was not pursued further in this program.

2.1.2 Experimental Procedures for Producing Enhanced Grain Size in Polycrystalline GaAs Films Grown by MO-CVD

One of the major advantages of the MO-CVD process is the unidirectional nature of the pyrolysis reaction, i.e., the absence of a competing reverse or etching reaction during film growth (see Section 1.2). This makes it possible to grow GaAs (or other) films on a wide variety of substrates that might otherwise be subject to severe attack in other CVD processes.

The unidirectionality of this process, however, may result in certain disadvantages. In some cases, for example, the virtually unrestricted nucleation and island growth in the early stages of film deposition may result in smaller average grain size in polycrystalline films than might be obtained on the same substrate using other processes.

To evaluate the effects of such etching on the growth of GaAs by MO-CVD an investigation was undertaken using HCℓ vapor as a constituent in the reactant gas mixture in a modified MO-CVD process. The HCℓ was added to the gas stream just

prior to its entering the top port of the cold-wall deposition chamber. The modified process thus should retain many of the advantages inherent in the MO-CVD process, yet the overall chemistry of the process would be expected to be modified considerably. It was expected that the modified MO-CVD process would result in rather complex chemical reactions, with a variety of intermediate compounds being formed in the bidirectional reaction. It was hoped, however, that the presence of HCℓ would enhance the average grain size in the polycrystalline GaAs films by increasing the definition of certain crystallographic facets and thus increase growth on those planes. It was believed that discrimination against the continued development of smaller nuclei and grains might also increase the final grain size, as the result of the etching mechanism. It is a well-established experimental fact (Ref 11) that the etching of single-crystal GaAs is highly preferential crystallographically at temperatures below 800°C. Bhat and others (Ref 11) have shown there is a strong tendency toward pitting of {100} facets in GaAs and major differences in etch rates for various low-index planes in GaAs at temperatures below 800°C. Above that temperature, however, all low-index planes appear to etch at the same rate and without pitting.

2.1.2.1 Experimental Film Growth in Presence of HCℓ

A series of preliminary experiments was undertaken about midway through the second year, as the first step in this study. A third separate reactor system was used for the experiments so that the other ongoing studies in the program would not be interrupted or otherwise perturbed by the very different growth conditions used in the HCℓ experiments.

Several calibration runs were first conducted to be sure that the system was equivalent in operation and in resulting film properties to the other two systems being used on the contract. Those experiments included determination of film growth rate and deposition temperature control as well as impurity doping control. The dependence of apparent grain size upon film thickness in polycrystalline GaAs films grown on Mo/glass and on Mo sheet substrates was also determined experimentally, to provide a baseline reference for the experiments to follow. The results of the thickness-dependence study are described in Section 2.2; it was found that apparent grain size increased almost linearly with film thickness, as is observed in most other polycrystalline deposited film systems.

In the initial MO-CVD experiments done with HCℓ added to the reactant gas stream using Mo/glass substrates, at first very dilute and then increasing amounts of HCℓ were added to the growth environment through the gas inlet manifold. As the HCℓ flow rate (and thus partial pressure) was increased an increasing problem of poor adherence of the GaAs film to the substrate was observed. At high HCℓ flow rates ($p_{HC\ell} \approx 0.1\ p_{TMG}$) it became obvious that the HCℓ was attacking the Mo film and thus undercutting the growing GaAs film. Mo sheet substrates were substituted for the Mo/glass composites and showed somewhat better resistance to this effect, but the undercutting still occurred to an undesirable extent.

In an attempt to "seal" the substrate and still allow the influence of HCℓ on film growth, thin layers of GaAs were first deposited on the Mo without HCℓ present and the HCℓ was added for the remainder of the growth. A GaAs thickness of ~2μm was found necessary to provide the required sealing of the surface for Mo sheet substrates and somewhat thicker layers were required for the Mo/glass substrates. As a result all further experiments were done with thin Mo sheet substrates. It should be pointed out that at times the sealing layer would have a pinhole and the introduction of HCℓ would result in local undercutting of the substrate and subsequent film peeling. However, a pinhole-free sealing layer of GaAs always resulted in an adherent uniform film, so this procedure was followed in all subsequent experiments with HCℓ .

A series of runs was then made with increasing HCℓ flow rates, using Mo sheet substrates. The growth rate was determined by measuring the total thickness of the GaAs film, including the sealing layer, and dividing by the total growth time. In most cases the film was grown to a total thickness of 12-16 μm. Figure 7 shows the dependence of growth rate upon relative HCℓ concentration in the reactor. Although there is considerable scatter in the data it can be seen that there was no substantial decrease in the growth rate with HCℓ addition in the range examined. Since etching of GaAs with HCℓ is strongly temperature-activated it would be expected that these results might be greatly changed at higher growth temperatures. However, higher growth temperatures would probably also require less HCℓ to produce similar changes in the morphology of growth.

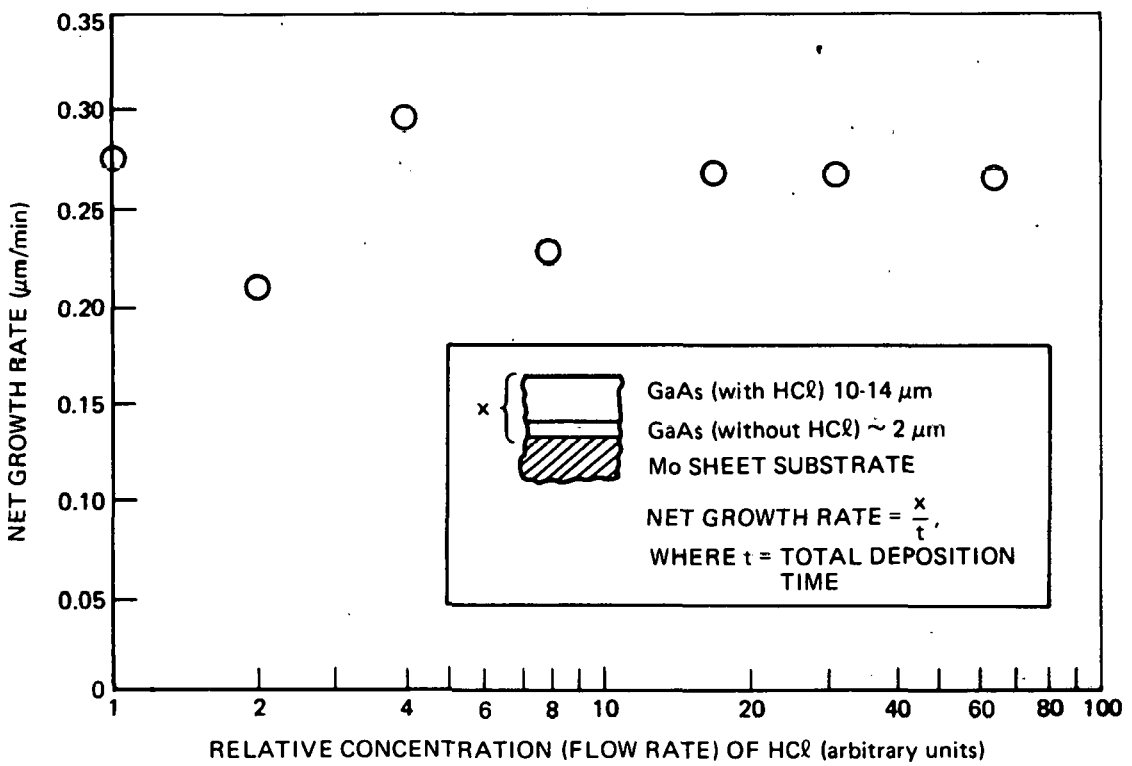


Figure 7. Dependence of Net Growth Rate of GaAs Film, Deposited by MO-CVD on Mo Sheet Substrate at 725°C, upon Relative Concentration (i.e., Flow Rate) of HCℓ Vapor Added to Reactant Gas Stream

The change in growth morphology for GaAs deposited by MO-CVD on Mo sheet with no HCℓ added and with the highest flow rate of HCℓ added (~3 ccpm) is shown in Figure 8 for thick films (~40 μm) grown at 725°C. Note the increase in average grain size and the increased uniformity of grain size that results with the use of HCℓ during growth.

Figure 9 shows a series of four GaAs films grown at 725°C on Mo sheet substrates with increasing HCℓ partial pressure. The highest HCℓ flow rate represented is half of that used during deposition of the film shown in Figure 8b. It can be seen that the major effects of the HCℓ additions on the film morphology occurred in the films deposited with HCℓ flow rates greater than 0.75 ccpm. Generally, it was difficult to determine accurately the actual partial pressure of the HCℓ in the vicinity of the substrate since the flow patterns in that region of the deposition chamber were not well known; HCℓ flow rates were thus usually used as a measure of the HCℓ concentration.

These results clearly established that the presence of HCℓ in sufficient concentration in the deposition chamber can have a significant effect upon both morphology and grain size in polycrystalline GaAs films grown by MO-CVD. It appeared that the most effective concentration of HCℓ might be near that for which the etch rate and the normal deposition rate were equal, for a given deposition temperature.

Unfortunately, the beneficial effects of HCℓ were not achieved without penalty. Several problems were encountered in association with its use in the MO-CVD process. The most annoying of these was the need to clean thoroughly not only the reactor deposition chamber after every run (the normal procedure) but also the neighboring portions of the reactor system after at most a few runs because of the formation of a black, oily volatile substance that formed in the output lines of the reactor system when HCℓ was used. It was not determined if this substance was formed as part of the deposition reaction and merely collected in the lines or was formed in place in those cold reactor parts. At any rate, its presence made the reactor difficult to evacuate during film growth and in the worst cases impeded nucleation and growth on the substrate in subsequent runs. As a result, a policy of cleaning the reactor output section after every run was adopted. Also, the HCℓ was added to a side-arm port at the top of the deposition chamber rather than in the gas manifold.

Another significant problem associated with the use of HCℓ was the increase in the net carrier concentration of GaAs films grown with HCℓ present. The cause of this increase was not at first known, but its effect was seen in the performance of devices formed in the films. Figure 10 shows the dark and illuminated I-V characteristics of two representative Au Schottky-barrier solar cell devices formed on n/n+ polycrystalline GaAs structures deposited at 725°C on Mo substrates with HCℓ present. Although reasonable short-circuit currents (~9 mA/cm^2) were obtained the I-V characteristics were soft and symmetrical. Whether this was caused by high intragrain doping concentrations or preferential grain-boundary doping was not established at the time. However, since single-crystal GaAs films grown on single-crystal substrates with HCℓ present were found to be doped to concentrations of ~10^{17} cm^{-3} in some cases, it appeared that intragrain doping was involved to some degree.

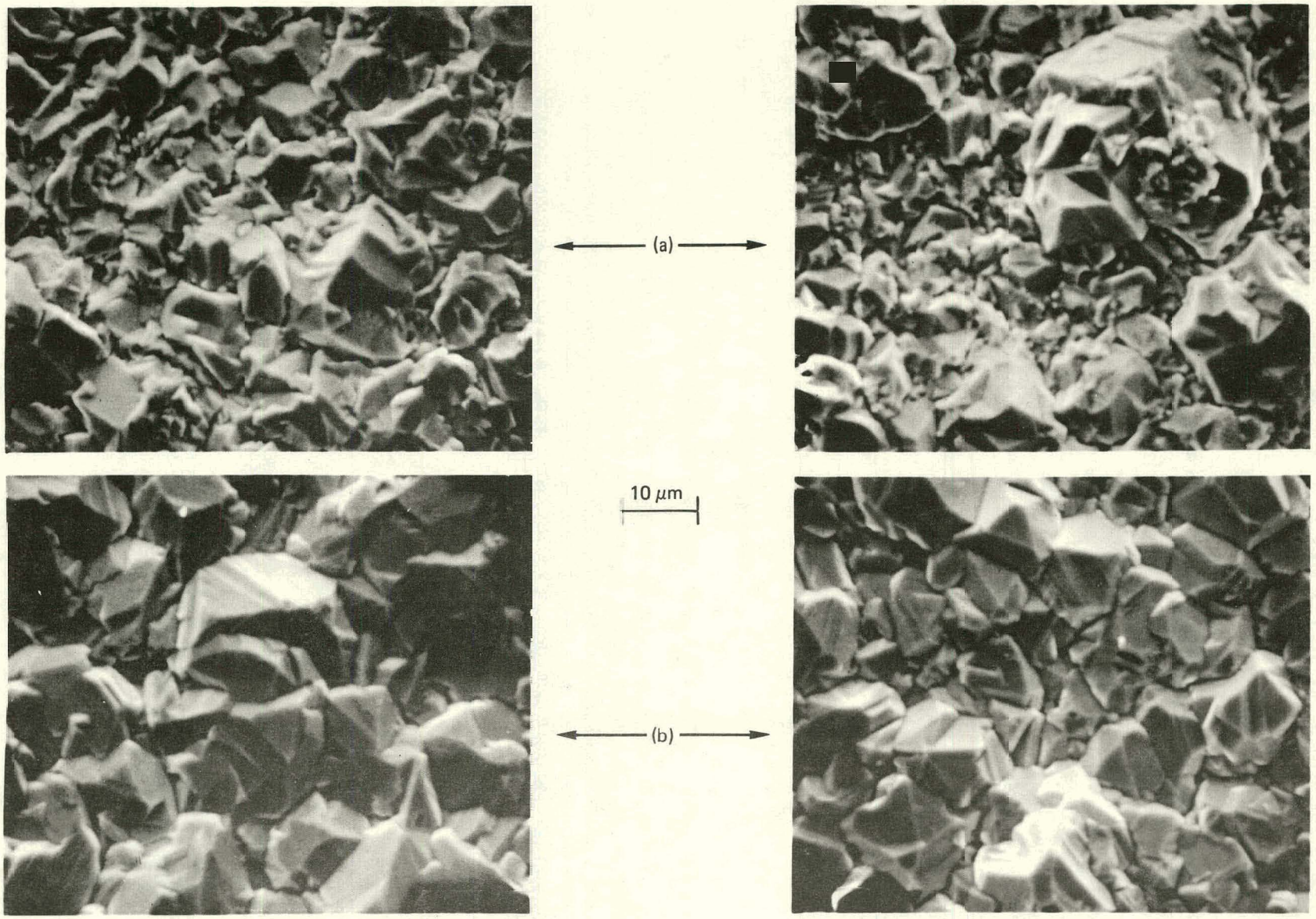


Figure 8. SEM Photographs Showing Effect of HCℓ Addition on MO-CVD GaAs Film Growth Morphology on Mo Sheet Substrates. a) No HCℓ (two different film regions); b) High Flow Rate (~3 ccpm) of HCℓ (two different film regions). (Films ~40μm thick, deposited at 725°C.)

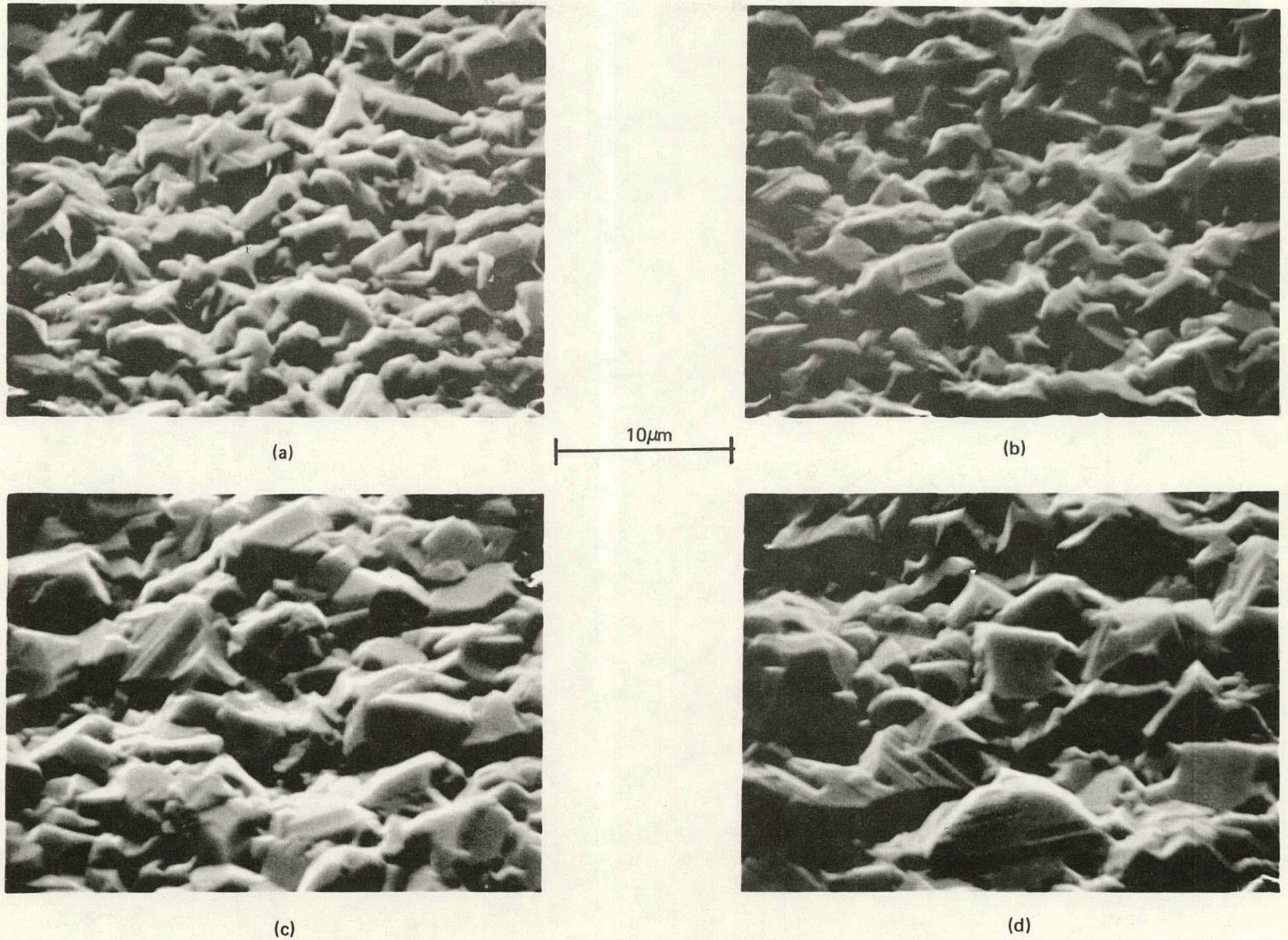


Figure 9. SEM Photographs Showing Effect of Increasing HCℓ Partial Pressure (Flow Rate) on Average Grain Size and Surface Morphology of MO-CVD GaAs Films Grown on Mo Sheet Substrates at 725°C. HCℓ Flow Rates a) 0.085 ccpm, b) 0.37 ccpm, c) 0.75 ccpm, d) 1.5 ccpm.

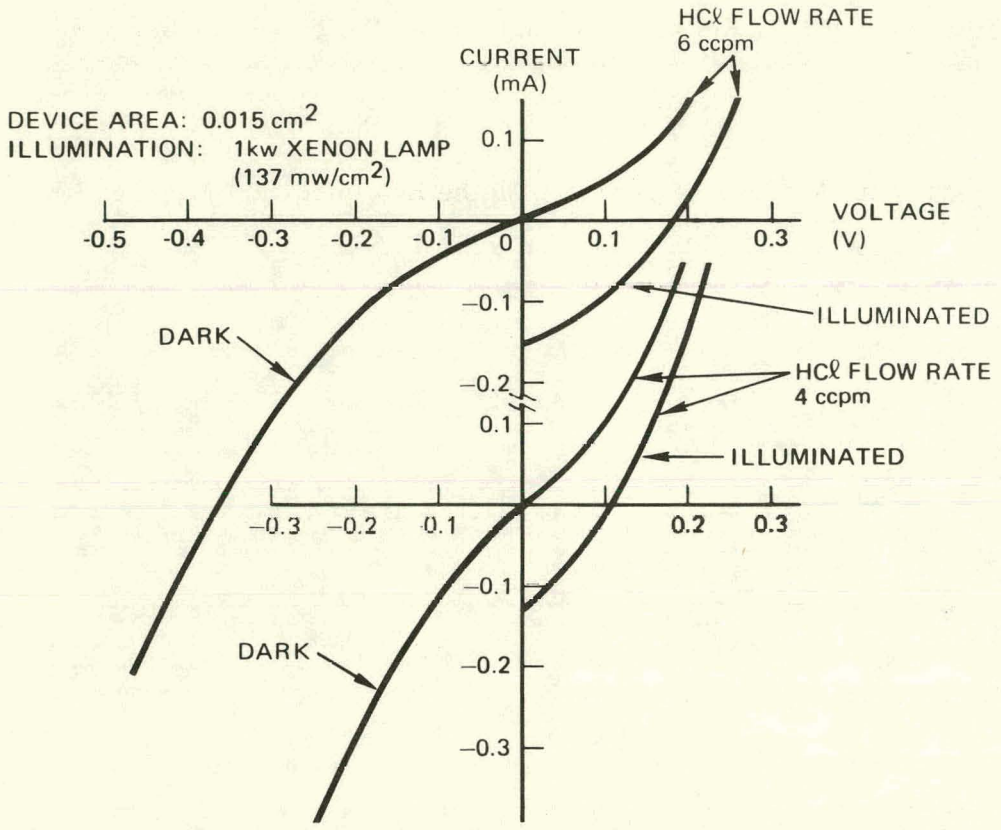


Figure 10. Dark and Illuminated I-V Characteristics of Two Schottky-barrier Solar Cells on n/n+ GaAs Polycrystalline Structure Grown by MO-CVD on Mo Sheet Substrate at 725°C with HCℓ Vapor Present during Growth.

The need for thoroughly cleaning the deposition chamber and all adjoining parts of the reactor system after every experiment in which HCℓ vapor was used in the process clearly showed that the complexity of the chemical reactions involved had been greatly increased. To improve the understanding of the chemistry involved, a few simple experiments were conducted in which various concentrations of HCℓ were mixed with TMG, AsH_3, and H_2, each separately, at room temperature to observe any possible formation of compounds under those conditions. These experiments showed that for very high concentrations of HCℓ and TMG a white crystalline material was formed on most surfaces in the reactor chamber when these two reactants were mixed. After 15 to 20 min, two clear liquids also began to form. When the HCℓ and TMG flows were terminated the crystalline deposits sublimed rapidly back into the vapor phase, followed more slowly by one of the liquids. The second liquid remained and was found to be difficult to transport inside the reactor system, even under vacuum conditions and with moderate heat applied to the chamber walls.

No compound formation or other reaction was observed for the HCℓ-AsH_3 and the HCℓ-H_2 mixtures under the above conditions. However, the fact that the compound formation did occur for the HCℓ -TMG mixture under the specific conditions of the above experiment verified that there is an added reaction

complexity when HCℓ is present. To determine the extent of this complexity under normal GaAs film growth conditions would require extensive experimental study. This work was not pursued, since under normal conditions it appeared as though the formation of these compounds did not seriously affect the film growth.

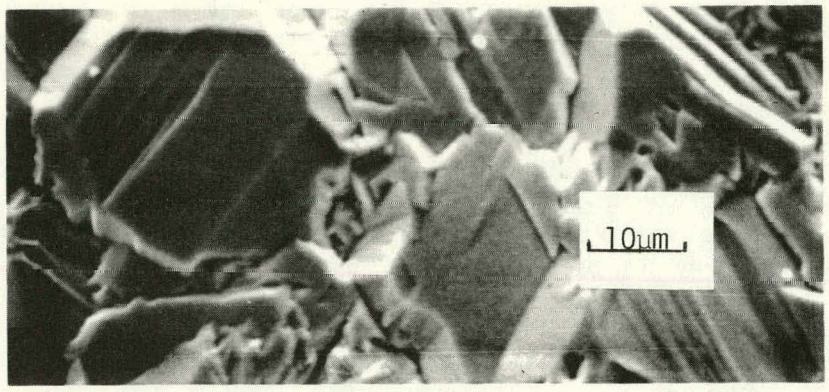
To study the kinetics of growth with the HCℓ-modified MO-CVD process and to test the hypothesis that the modified process did involve competing growth and etching reactions, several experiments were undertaken at a variety of temperatures. A series of films was grown on both unetched and etched Mo sheet substrates at temperatures of 650, 675, and 700°C. All of these experiments were done with identical flow rates of TMG and AsH_3 and with HC flow rates of 5 and 10 ccpm. In this temperature range the growth rate of the standard MO-CVD process is not strongly temperature-dependent, and the morphology of polycrystalline films grown in this temperature range appeared, by most analytical methods, to be essentially the same. The previous experiments with HCℓ had been done at a deposition temperature of 725°C; the lower temperatures used in this new series of experiments allowed higher partial pressures of HCℓ (0.85 torr to 1.70 torr) to be used, since the HCℓ etch rate is exponentially dependent on temperature. It was hoped that such higher partial pressures of HCℓ would further enhance the GaAs grain size increase over that already observed for lower HCℓ concentrations. A sapphire single-crystal substrate was usually included in the experiment to provide a means for determining the thickness of the deposited GaAs.

SEM examination of the polycrystalline films grown on the etched and unetched Mo surfaces indicated similar-sized surface features in the two cases. The etchant that was used for the Mo was 6:1:1 H_2O:HNO_3:H_2SO_4 applied for 15 sec, with a final "cleanup" in HCℓ solution with ultrasonic agitation.

The apparent grain size (inferred by observation of surface features in SEM photographs) of the GaAs films deposited at 650°C was only slightly increased over the normal size by addition of 5 ccpm of HCℓ vapor to the main reactant gas stream flowing into the reactor chamber. However, a dramatic increase resulted for a flow of 10 ccpm of HCℓ . Exact comparisons could not be made because of an approximate 20 percent variation of film thickness from run to run in the experiments done at 650°C, but the effect is clearly shown in the SEM photographs in Figure 11.

Deposition at 675°C resulted in a more nearly linear increase in apparent grain size with increasing HCℓ flow rate (i.e., partial pressure). Grain sizes approaching those achieved at 650°C growth temperature were realized at equivalent HCℓ flow rates. Figure 12 shows the surfaces of films obtained at this temperature without HCℓ and with flow rates of 5 and 10 ccpm of HCℓ .

For the films deposited at 700°C the apparent grain size was increased by addition of 5 ccpm of HCℓ , as for growth at 675°C. However, for a flow rate of 10 ccpm of HCℓ the net rate of growth was negative, that is, the etching rate exceeded the deposition rate. Figure 13 shows SEM photographs of the surfaces of films grown without HCℓ and with a flow rate of 5 ccpm of HCℓ .



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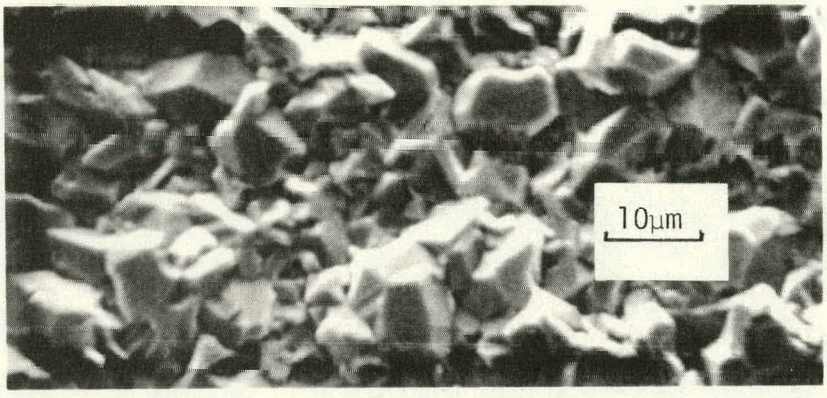
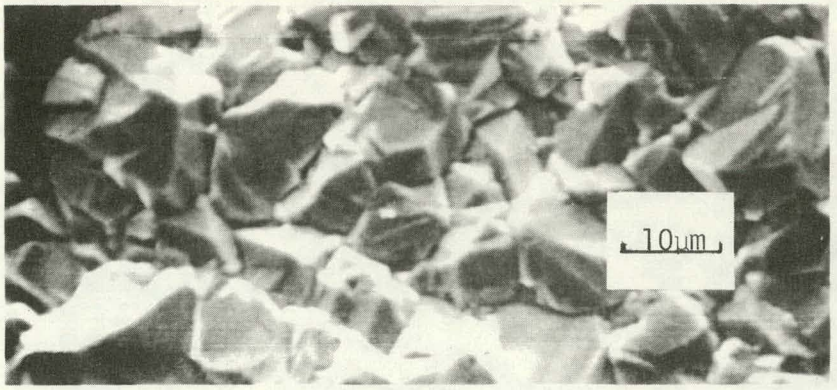


(b)

(a)

Figure 11. SEM Photographs of Surfaces of GaAs Films Deposited by MO-CVD at 650°C onto Etched Surfaces of Mo Sheet Substrates. a) No HCℓ Present (film 35μm thick); b) HCℓ Flow Rate 5 ccpm (film 29μm thick); c) HCℓ Flow Rate 10 ccpm (film 45μm thick).



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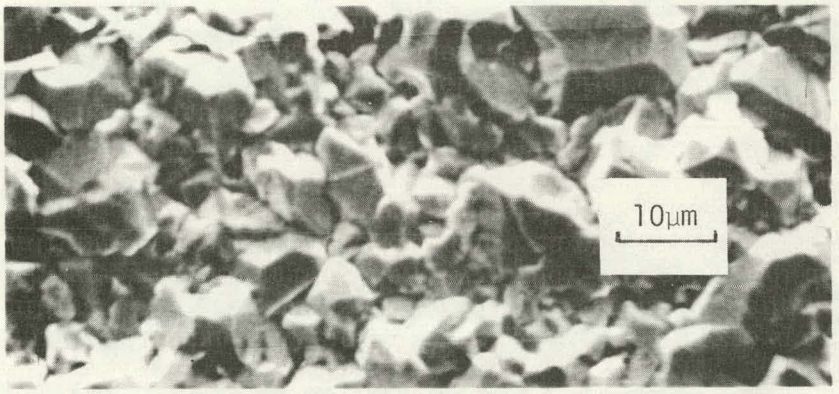

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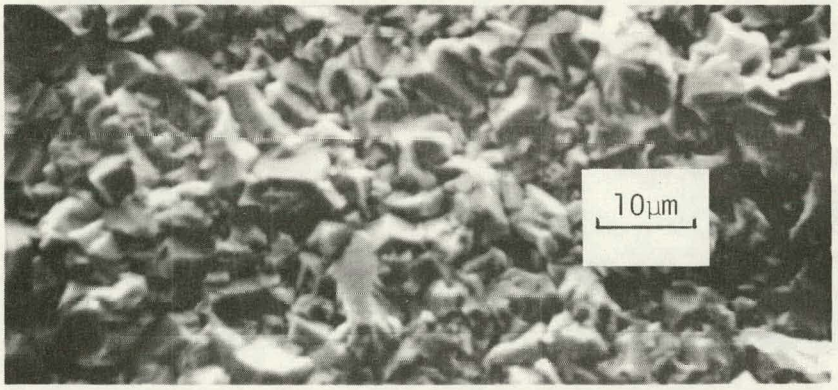
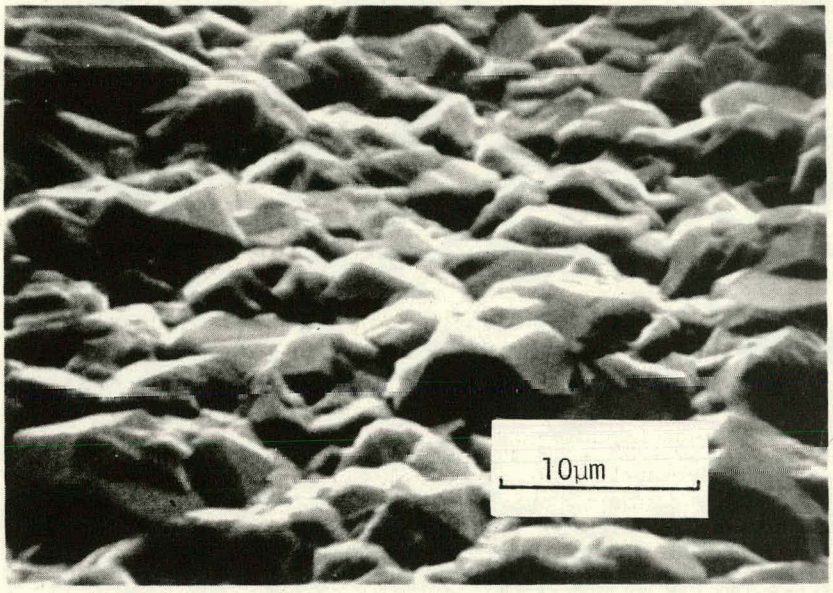


(a)

Figure 12. SEM Photographs of Surfaces of GaAs Films Deposited by MO-CVD at 675°C onto Etched Surfaces of Mo Sheet Substrates. a) No HCℓ Present (film 26μm thick); b) HCℓ Flow Rate 5 ccpm (film 29μm thick); c) HCℓ Flow Rate 10 ccpm (film 33μm thick).



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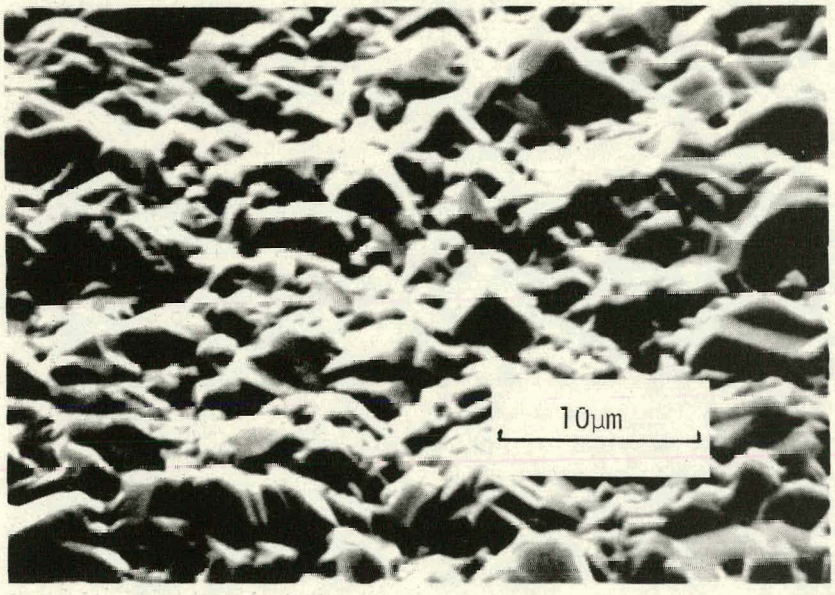

(a)

Figure 13. SEM Photographs of Surfaces of GaAs Films Deposited by MO-CVD at 700°C onto Etched Surfaces of Mo Sheet Substrates. a) No HCℓ Present (film 12.5 μm thick); b) HCℓ Flow Rate 5 ccpm (film 13μm thick).

These results appear to be consistent with a film growth mechanism that involves competing selective etching and growth processes that discriminate among various crystallographic orientations, favoring certain ones over others. Since the GaAs etch rate in HCℓ vapor is known to be strongly temperature-dependent it follows that as the temperature increases the effect of HCℓ on the GaAs film morphology will increase for a fixed HCℓ flow rate. Also, since the attack of GaAs by HCℓ at relatively low temperatures is known to be crystallographically selective, the observed formation of large facets by the etching process was to be expected.

2.1.2.2 Film Counterdoping in HCℓ-modified Process

During the final quarter of the program the emphasis of the investigation of GaAs film growth in the presence of HCℓ vapor was on the growth of n/n+ GaAs structures to permit fabrication of Schottky-barrier solar cells, to observe the effect of grain size differences on the performance of the cells. As for all previous experiments with GaAs film growth using HCℓ , a protective cover layer of GaAs approximately 2 μm thick was first deposited on the substrate without use of HCℓ to prevent undercutting of the substrate surface by the HCℓ early in the growth. The n^+ layer was then formed by adding suitable amounts of H_2Se to the reactor gas stream during deposition of the next 5-10 μm thickness of GaAs in the presence of HCℓ . The remaining (n-type) layer was then deposited as nominally undoped material, again with HCℓ present.

The resulting set of samples was analyzed using point-contact reverse-breakdown measurements. These measurements indicated that there were major difficulties with the procedure being used to grow the samples. The top layer, which should have been n type, was highly conductive (n^+) with carrier concentrations the order of 5×10^{17} cm^{-3}. Earlier, experiments had been performed using semi-insulating GaAs substrates without any n^+ layers, and the background carrier concentration was determined to be the order of 10^{16} cm^{-3}. Several experiments were done to determine the source of the undesirable impurities, believed at the time to be originating either in the HCℓ gas itself or in the deposits remaining on the reactor walls and susceptor from the preceding deposition of doped n^+ GaAs material. In the first set of experiments, the HCℓ flow was stopped along with the H_2Se after deposition of the n^+ layer, so that the undoped n-type layer was deposited in the absence of HCℓ . An n-type layer only lightly doped resulted, but the grain size was significantly reduced relative to that obtained with HCℓ present. This suggested that HCℓ was required for a longer fraction of the deposition period to preserve the large grains, whereas it had been assumed that after the HCℓ had helped to initiate larger grain growth early in the deposition process the grains would continue to grow (epitaxially) and enlarge after removal of the HCℓ .

Additional samples were then prepared by depositing the n^+ layer with HCℓ present, terminating the growth experiment, removing the samples and completely cleaning the reactor chamber and parts, reinserting the samples (Mo substrates with n^+ layers), and growing the undoped n-type layers in the presence of HCℓ . The last-grown layers obtained by this procedure were also found to be n^+. This result largely eliminated the deposits on the system walls and other parts as the source of impurities, and indicated that either the HCℓ or the n^+ layer was the probable source, the latter probably inducing the effect by an autodoping mechanism. Since

single-crystal films of GaAs were readily grown on semi-insulating substrates in the presence of HCℓ with carrier concentrations the order of 10^{16} cm^{-3}, it appeared that the n^+ layer was responsible for the observed effect through an autodoping process that occurred only when HCℓ was present.

An attempt was made to achieve enhanced grain growth and produce the desired lightly doped n-type layer by depositing the n/n+ configuration with HCℓ present and then depositing another 5μm layer undoped (presumably n type) without the HCℓ gas. The resulting GaAs structure showed considerable improvement in the doping level in the top n layer. Structures of this type were deposited at 650, 675, and 700°C, although the previous HCℓ experiments described above were nearly all done at a deposition temperature of 700°C. Unfortunately, none of these samples survived the processing used to fabricate Schottky-barrier solar cells.

Further experiments of this type should be undertaken to determine if the early formation of large grains in a polycrystalline GaAs film can be propagated by subsequent "epitaxial" growth with the normal MO-CVD process, that is, in the absence of HCℓ.

2.1.2.3 Appraisal of HCℓ-modified MO-CVD Process

The study of the effects of the addition of HCℓ on the MO-CVD growth process for GaAs polycrystalline films resulted in the following general observations:

1. The addition of HCℓ to the main reactant gas stream during the MO-CVD growth of GaAs beneficially affects both the film growth morphology and the average grain size in the resulting polycrystalline films. Films grown under this condition in general have much larger grain sizes and more fully developed crystalline facets than those grown with the normal MO-CVD process.

2. The use of HCℓ with Mo or Mo/glass substrates requires deposition of a GaAs layer approximately 2 μm thick with no HCℓ present in order to seal the substrate prior to the introduction of HCℓ. As a consequence of this requirement, GaAs films that are relatively thin (5 μm or less) show little grain size enhancement or other effect of the HCℓ.

3. HCℓ significantly changes the nature of the chemical reactions that occur in the system during deposition; there is some evidence suggesting the formation of addition compounds or other intermediate products that may strongly influence the growth kinetics. As a minimum, there are competing etching and deposition reactions that result in the net film growth rate being very temperature-sensitive when HCℓ is added in sufficient quantity to produce grain-size enhancement. The persistent formation of reaction products at the inlet to the deposition chamber, as described earlier, requires more extensive cleaning of the deposition system after each run than is necessary when no HCℓ is used. This complication, however, could probably be reduced by modified reactor design.

4. Schottky-barrier devices formed on polycrystalline GaAs films in which the final (top) layer was deposited in the presence of HCℓ did not generally exhibit acceptable properties. Data obtained late in the program suggested that such results may have been due to an intragrain doping effect, in which the n layer of an n/n+ structure was doped unintentionally from the n+ layer. An alternative explanation, however, is that the grain boundaries of the n layer became doped to form n+ regions within the grain boundaries. If this is the dominant mechanism, it may be possible to selectively anodize the grain boundaries at the film surface and control this negative effect.

It is evident that additional investigation of the use of HCℓ in the MO-CVD process for the growth of GaAs is necessary to establish more details of the various effects and thus optimize its use in terms of the desired film properties. Such work is recommended for the future.

2.2 TASK 2. EVALUATION OF FILM PROPERTIES AND GRAIN BOUNDARY EFFECTS AND CORRELATION WITH CVD GROWTH PARAMETERS

The three main activities included in this task were (1) improvement of film growth and doping procedures, (2) routine evaluation of film properties, and (3) study of grain boundary effects in the polycrystalline films grown on various low-cost substrates. Results obtained in these three areas during the second year of the program are described in the next three sections.

2.2.1 Development of Film Growth and Doping Procedures

During the first two quarters of the second year some additional attention was given to improving the film growth and doping procedures developed in the first year of the program, especially with respect to polycrystalline films of GaAs and GaAlAs deposited on various low-cost substrate materials.

Both single-layer and multilayer structures of polycrystalline GaAs were deposited on various substrates, although the emphasis was on multilayer structures including p^+/n, n^+/p, n^+/n, and $p^+/i/n^+$ (the i layer being n-type). The low-cost substrates used for these experiments primarily involved composites of Mo or Ge films deposited on glasses (Corning Codes 0317, 7059, or 1723). In several instances bulk polycrystalline GaAs substrates were also used, as were graphite substrates and annealed Mo sheet substrates in a few experiments. Additionally, some single-crystal thin-window GaAlAs/GaAs heteroface solar cell structures were grown on single-crystal GaAs substrates, and other single-crystal films (GaAs/Ge and Ge/GaAs) were grown for the purpose of examining the GaAs/Ge interface. Results obtained with some of these structures are discussed in other sections of this report.

A series of polycrystalline GaAs p-n junction structures was grown with a range of doping concentrations in the p-type Zn-doped GaAs layers. Usually a Si-doped GaAs single-crystal substrate was also included in the run to serve as a control wafer and to provide information on the properties of the simultaneously grown single-crystal p-n junction.

In some cases a two-step growth sequence was used for producing the junction structures. A deposition run was first made to grow a GaAs:Se n-type film $\sim 4\,\mu m$ thick on the surface of the Mo/glass or the Ge/glass composite substrate. The resulting film was then etch-polished with Br_2-MeOH (1% solution) to a final thickness of $\sim 2\,\mu m$. This produced a very smooth surface, thus making it possible to grow the upper (p-type) layer of the junction structure on a smooth substrate, Zn-doped to the desired concentration level. In some cases the p-type layer was also etch-polished in a similar fashion prior to evaluation. To monitor the impurity doping concentration obtained in each layer of these two-step junction structures a GaAs:Cr high-resistivity substrate was usually used in each of the runs of the growth sequence. Measurements of carrier concentration in the companion epitaxial samples then provided the desired data.

Some of the polycrystalline p-n junction structures were angle-lapped (3-deg bevel) to permit measurement of the layer thicknesses. The thicknesses determined by this technique generally agreed well with the thicknesses measured on the single-crystal companion samples using the same measurement procedure. This angle-lapping and staining process failed to provide any evidence of detectable Zn diffusion along the grain boundaries from the upper Zn-doped layer into the polycrystalline bottom layer (Se-doped, n-type), although it is possible that such Zn diffusion was simply not detectable by this relatively insensitive procedure.

Results of the evaluation of the device properties of these junction structures are given in the Task 3 discussion (Section 2.3).

Several series of experiments were also conducted during the same period with single-crystal GaAs film growth, partly to provide further baseline reference data on film properties and doping characteristics that could be used in interpreting results obtained with the doped polycrystalline films. These experiments included the growth of GaAs:Zn and GaAlAs:Zn films 6-10 μm thick on GaAs:Cr single-crystal substrates to verify previously established Zn doping curves using diethylzinc (DEZn) as the Zn source and to establish conditions for the growth of heavily doped p-type GaAs:Zn and GaAlAs:Zn films.

It was found that doping concentrations in excess of 10^{19} cm^{-3} for GaAs:Zn layers (epitaxial) could be grown routinely. Heavily doped layers of several $Ga_{1-x}Al_xAs$ alloy compositions, with $p > 10^{18}$ cm^{-3}, were also grown for two different temperatures of the DEZn source. The results are shown in Figure 14, in which the open data points (circles and squares) correspond to the same DEZn flow rate into the reactor chamber but are for two different DEZn source temperatures (0°C and 24°C). The solid data points (dots) are for a somewhat lower DEZn flow rate and for a DEZn source temperature of 0°C. Clearly, as the Al content in the alloy increases, especially above about $x = 0.8$, it becomes more difficult to obtain heavily doped (and thus high-conductivity) p-type material.

Other single-crystal GaAs films that were grown included a group of undoped layers on (100)-oriented Ge substrates, for use in the study of the role of intermediate layers of Ge formed on low-cost substrates for the purpose of influencing the growth habit and/or grain size of subsequently deposited GaAs films. The nominally undoped GaAs films exhibited evidence of Ge incorporation, based on point-contact rectification (PCR) measurements (see Section 2.2.2) compared with similar measurements on undoped GaAs films grown directly on GaAs:Cr single-crystal substrates.

In addition, a group of single-crystal Ga-doped Ge films was separately grown by the CVD process by adding TMG to the reactant gas stream during growth of Ge from GeH_4. These films were found to be heavily doped p-type and were very conductive, and thus could be used as p-type intermediate layers for the growth of n-p polycrystalline GaAs junction structures.

The effect of deposition temperature in the MO-CVD process on GaAs film properties was examined in the first year for growth on several low-cost substrate materials, but because of the increased interest in Mo sheet and Mo-coated glass

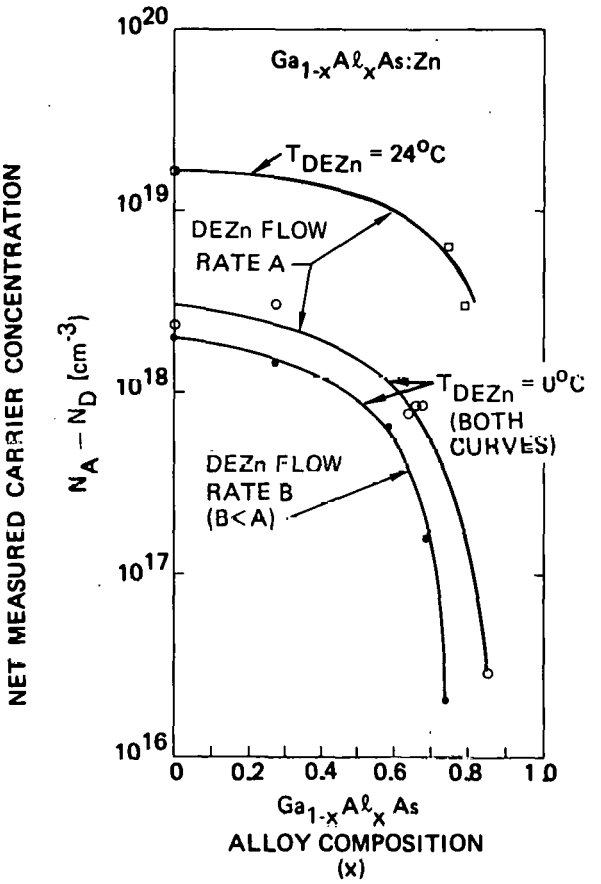

Figure 14. Net Carrier Concentration Measured in $Ga_{1-x}Al_xAs$ Films Grown by MO-CVD at 725°C, as Function of Al Content for Three Different Growth Conditions.

substrates in this program a series of experiments was undertaken with these substrates to establish the effect of growth temperature. Polycrystalline GaAs films were deposited in the range 600-750°C, with a substrate of single-crystal sapphire used in each experiment to serve as a monitor of the deposition and film growth process. Although this was not a detailed study, it was clearly established that film grain size (as indicated by the size of surface features on the film) was larger for films deposited in the 700-750°C range. Only the films grown at 600°C appeared to have significantly smaller grains than these grown at the higher temperatures. Since no appreciable grain size variation was detected for films deposited at temperatures in the 650-750°C range, the previously identified preferred deposition temperature range of 700-725°C was selected for continued use in subsequent experiments with substrates of Mo sheet and Mo film on Corning Code 0317 glass.

These same substrate materials were used in another series of experiments to determine the variation of GaAs film properties with film thickness, for deposition at 725°C and an average growth rate of 0.3 μm/min. Apparent average grain size, as determined by observation of surface features in the SEM, was found to increase with increasing film thickness, although there was considerable variation in the sizes of individual grains on a given film.

Figure 15 shows the observed trend, with the vertical bars representing the spread in the measured grain sizes on a given sample. An accurate measurement of true grain size distribution was not made in obtaining the data shown in Figure 15. In particular, the films were not etched to determine if some of the larger crystallographic features seen at the surface and assumed to be large individual crystallites might actually have consisted of aggregates of smaller individual crystal grains. However, the absence of submicron-size surface features and the increased number of large surface features in the thicker films was clear semiquantitative corroboration of the trend shown by the SEM observations presented in Figure 15.

These results emphasized the fact that films of comparable thickness must be used if the effects of variations in deposition parameters on film grain size and surface morphology are being examined. The results also tended to confirm the feasibility of the concept of using thick layers of AlAs as underlayers for the active GaAs regions of thin-film cells for the purpose of achieving enlarged grain sizes in the cell. Actual proof of feasibility of this concept, however, was not undertaken experimentally in this program, and would depend strongly on the extent to which deposition of stable and properly doped AlAs layers with good ohmic contact to the substrate could be achieved.

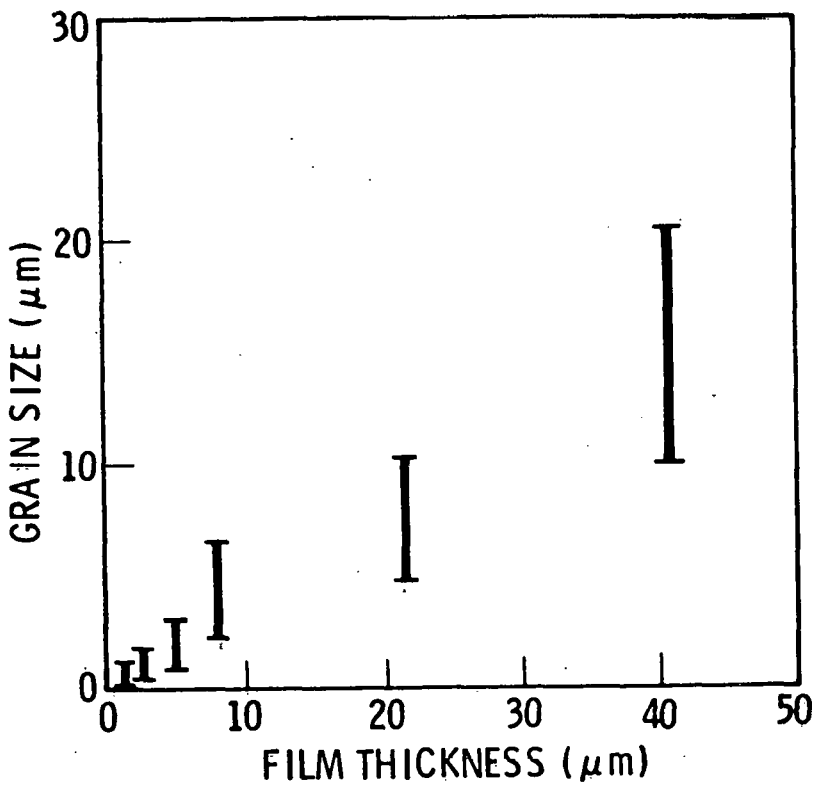

Figure 15. Range of Apparent Grain Sizes for Polycrystalline GaAs Films Grown by MO-CVD at 725°C on Substrates of Mo Sheet and Mo Film/Corning Code 0317 Glass. (Grain sizes indicated by surface features as observed in SEM.)

2.2.2 Evaluation of Film Properties

Routine evaluation of the structural and electrical properties of the GaAs and GaAlAs films deposited by the MO-CVD process under various experimental conditions continued throughout the period covered by this report. Much of this work was concentrated on the study of the properties of multilayer structures, to determine the effects of subsequent GaAs growth on the final properties of the various layers. Also, it was hoped that such investigations would determine if the properties of the individual layers showed any recognizable relationship to the junction transport properties of the various device structures being grown.

Angle-lapping techniques were commonly used for thickness determination. This procedure revealed planar junctions, generally, with no detectable deviations from planarity that could be attributed to Zn diffusion along grain boundaries, as mentioned earlier. However, no firm conclusion was possible on the basis of these experiments because of scratches and other defects resulting from the angle-lapping procedure used. The high degree of planarity of the junctions was actually somewhat surprising in view of the fact that the morphology of these films typically became quite rough after ~5 μm of growth.

Selective-area step-etching was also used to study film properties, most often in conjunction with PCR measurements to determine the electrical properties of the various layers. The latter proved to be a valuable technique, as is emphasized in the Task 3 discussion. In general, Br_2:MeOH (2 percent) was used for the etchant. Layer thicknesses predicted by growth-rate calibration were at least grossly confirmed by this technique, and the observed breakdown voltage usually agreed with the expected value based on the intended doping of the film.

The PCR measurements were performed by applying two tungsten probes to the surface of the material. The first probe was first charged by a Tesla coil to break down the surface potential for ohmic conduction, and the second probe was then placed in contact with the surface at a nearby location. A curve tracer was then connected across the two probes, and the resulting voltage polarity and breakdown voltage gave a measure of the conductivity type and carrier concenération. The voltage breakdown readings were "calibrated" (during the first year of the contract) by van der Pauw measurements on many samples of both n- and p-type polycrystalline GaAs material. However, the results were found to be somewhat substrate-dependent and sharply dependent on film doping, so that only approximate doping concentrations could be inferred by this convenient method. Except for the highest doping levels ($\geq 10^{18}$ cm^{-3}), however, it provided a quick and useful indication of doping type.

When comparisons were made of the measured breakdown voltages for n-type layers in p/n/n+ structures before and after growth of the p-type layer no differences were observed. These results appeared to confirm the earlier conclusion that shunting due to impurity diffusion along grain boundaries was not responsible for the leaky I-V characteristics typically found for the polycrystalline p-n junctions formed in GaAs films in this program. (See Task 3 discussion, Section 2.3.)

An exploratory examination of a polycrystalline GaAs film sample containing a p-n junction was undertaken using the ion microprobe mass analyzer (IMMA).* However, it was not successful in detecting Zn in the junction region of the angle-lapped sample. The intention of the analysis was to determine if Zn, if present in the grain boundaries in sufficiently high concentrations, could be detected and possibly mapped as a function of position in the sample. Zn is one of the more difficult elements to detect by IMMA, however, and none was found in this single attempt.

A new and completely automated Hall-effect apparatus was made operational early in the second year,** and is shown schematically in Figure 16. The system is based on a Hewlett-Packard 3052 data acquisition system, and consists of a Hewlett-Packard 9825A calculator as the system controller and data processor. The acquisition of data is accomplished by controlling the functions of two switching interfaces. One is a Hewlett-Packard low-leakage relay-scanner directly interfaced to the calculator. This scanner determines which of the legs of the van der Pauw sample receives current and which are connected to the voltage-measuring apparatus. The current is controlled by the use of a Keithley picoampere current source, and the voltages are measured by a Hewlett-Packard high-impedance DVM. The magnetic field is switched by an interface designed and built at Rockwell. This interface is also controlled directly by the calculator, and is software-variable.

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*The IMMA analyses were conducted at the Aerospace Corporation Research Laboratories, El Segundo, CA.

**This system was designed and assembled at no direct cost to this contract.

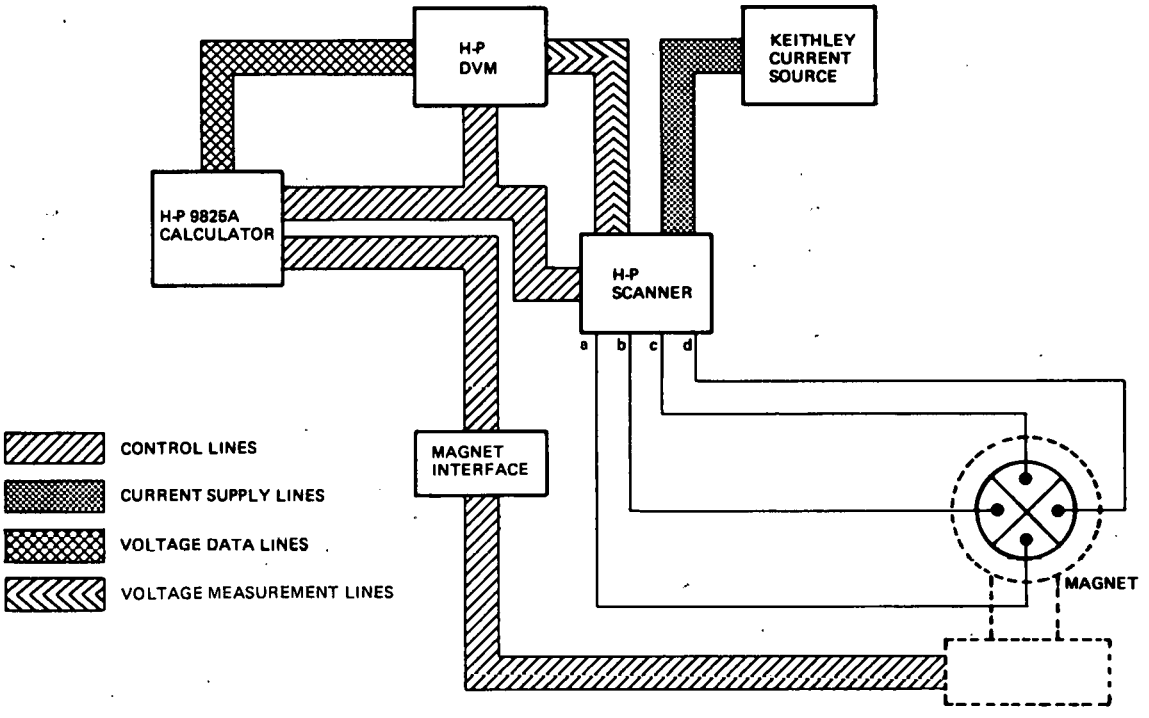

Figure 16. Schematic Diagram of Automated Hall-effect Apparatus Used for Film Characterization Measurements

The system was used in this program was capable of measuring samples with impedances up to 10^{10} ohms at current levels ranging from 10^{-12} to 10^{-3} amperes, depending on sample resistance. It performed the entire measurement in less than 2 min and was found to be reproducible to better than 1 percent. Measurements of transport properties as a function of sample temperature were carried out with manual control of temperature, since the automatic temperature control interface was not completed at the time of this work.

A variety of other procedures was used, as required, for characterizing the properties of the single-layer and multilayer films prepared in this program, and the results of those characterizations are discussed in other sections of this report.

2.2.3 Investigation of Grain Boundary Effects in Polycrystalline GaAs Films Grown by MO-CVD

Investigations in the first year of this program demonstrated that both n- and p-type polycrystalline GaAs are highly resistive – from two to three orders of magnitude larger than single-crystal material comparably doped with impurity (Ref 1). Experiments undertaken early in the second year were designed to develop a more detailed understanding of the properties of polycrystalline GaAs, considered essential to maximum exploitation of these properties in photovoltaic devices.

Measured transport properties of polycrystalline Si were used by Seto (Ref 12) in developing a model to describe the electronic structure of grain boundaries in that material. The model developed in that work was applied, with appropriate modifications, to the polycrystalline GaAs films grown by MO-CVD in these investigations.

Two types of polycrystalline film samples were prepared for this study. One consisted of GaAs films deposited on large-grain polycrystalline alumina (Coors Vistal 5*) and the other involved similar films deposited on an amorphous glass (Corning Code 0317), prepared simultaneously in pairs and doped with impurity in the range $\sim 10^{16}$ to $\sim 10^{19}$ cm^{-3}. Two full sets of p-type films (doped with Zn) were prepared for the initial measurements. Subsequently, similar sets of Se-doped n-type films were prepared and characterized.

In each deposition experiment a substrate of (0001)-oriented single-crystal sapphire was also included. The GaAs growth on the sapphire substrate was epitaxial in each case, of (111) orientation (Ref 6). The assumption was made that the impurity doping concentration within the individual grains of the polycrystalline films on the alumina and the glass substrates was the same as that in the simultaneously grown epitaxial layer on the sapphire and that this could be adequately represented by the measured hole concentration in the epitaxial film. A similar assumption was made in earlier measurements of the properties of p-type polycrystalline CVD Si films at Rockwell (Ref 13). (See also Section 2.2.3.2 of this report.)

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* The designation Vistal 5 was applied in earlier Rockwell studies (Ref 13) employing this specially prepared substrate material for Si polycrystalline film growth. It indicates that commercial grade Coors Vistal alumina (99.9 percent purity) has been subjected to five consecutive annealing steps under controlled conditions for 5 hr each at ~1800°C to produce grain-size enhancement.

The GaAs films on the Vistal 5 substrates consisted of large but variously sized (200-100 μm) individual grains duplicating the grain boundary pattern of the alumina growth surface. The crystallographic orientations of many of the alumina substrate grains were such that epitaxial growth of the GaAs film occurred on those grains, while highly preferred multicrystalline growth occurred on other individual grains. The result was a large-grained GaAs film containing a wide distribution of crystallographic perfection in the individual grains. The GaAs films on the glass substrates, on the other hand, were characterized by only moderately preferred orientation (shown earlier in this program to be mainly in the {111} planes); grain sizes were typically small (2-10 μm) and relatively uniform, with the average size strongly dependent upon details of the nucleation and early-stage growth mechanisms on the amorphous surface. In general, however, since grain size typically increases almost linearly with film thickness, as observed in films on Mo (see Section 2.2.1), the conduction process in these films on glass may have been quite inhomogeneous.

Measurement of the transport properties of the polycrystalline films was done by the van der Pauw technique using the automated Hall-effect apparatus described in Section 2.2.2. Sample temperatures from 77 to 450°K were employed, controlled manually as mentioned earlier. The automatically logged data were printed and/or stored on tape for subsequent retrieval and automatic plotting.

2.2.3.1 Properties of p-type Polycrystalline Films

Ohmic contact to the Zn-doped p-type polycrystalline GaAs films on both substrate materials was achieved by alloying In dots into the film surface at~450°C for 1 min. Lightly doped p-type films were contacted with In-Zn dots.

Figure 17 shows the room-temperature resistivity as a function of p-type doping density for polycrystalline GaAs films deposited in pairs simultaneously on substrates of Vistal 5 alumina and Corning Code 0317 glass. The films on alumina had resistivities nearly an order of magnitude lower than those of the films on glass at a given doping density.

Plots of film resistivities vs 1/T, where T is the sample temperature, are shown in Figure 18 for the films on Vistal 5 and Figure 19 for the films on 0317 glass. In both instances the resistivity ρ varies as exp (E_b/kT) in the temperature range 250-450°K, where E_b is an effective barrier height that increases with decreasing nominal doping density in the films.

Figure 20 shows the variation of resistivity, carrier concentration, and carrier (hole) mobility in one of the films on Vistal 5 as a function of temperature. In the temperature range where the resistivity exhibits the exponential dependence on barrier height, as noted above, the hole mobility is seen to vary as exp ($-E_b$/kT) while the carrier concentration remains essentially constant, confirming that the observed resistivity variation with temperature resulted from the variation of mobility with temperature.

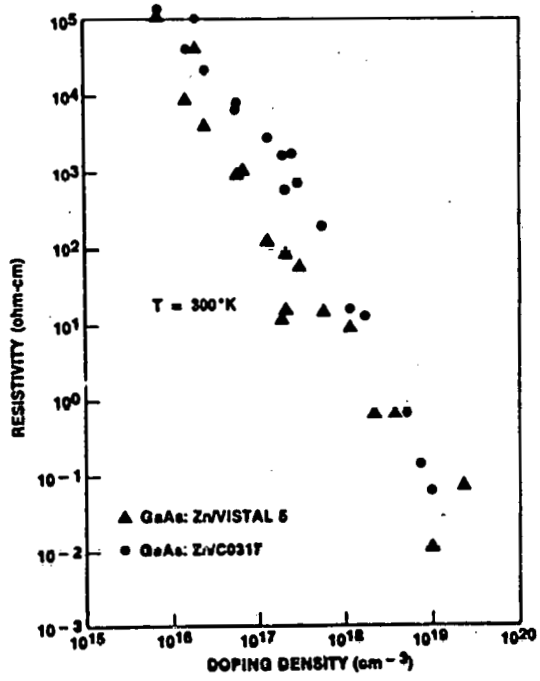

Figure 17. Room-temperature Resistivity of p-type Polycrystalline GaAs Films Deposited by MO-CVD on Substrates of Vistal 5 Alumina and Corning Code 0317 Glass, as Function of Zn Doping Concentration (see text).

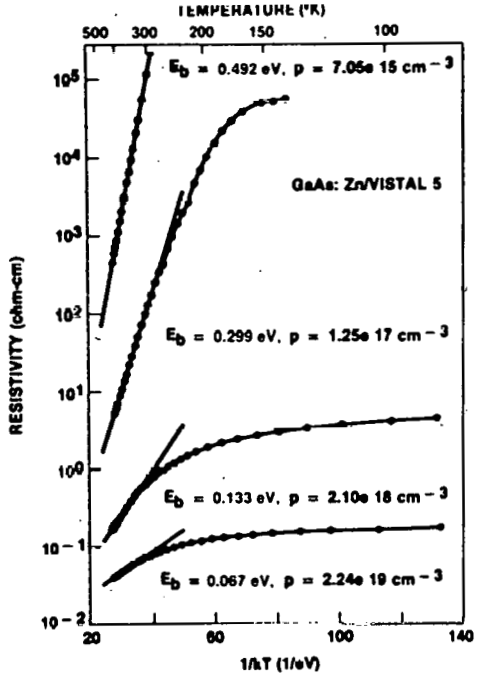

Figure 18. Measured Resistivity of p-type Polycrystalline GaAs Films, Deposited by MO-CVD on Vistal 5 Alumina Substrates, as Function of Sample Temperature for Various Doping Impurity Concentrations (see text).

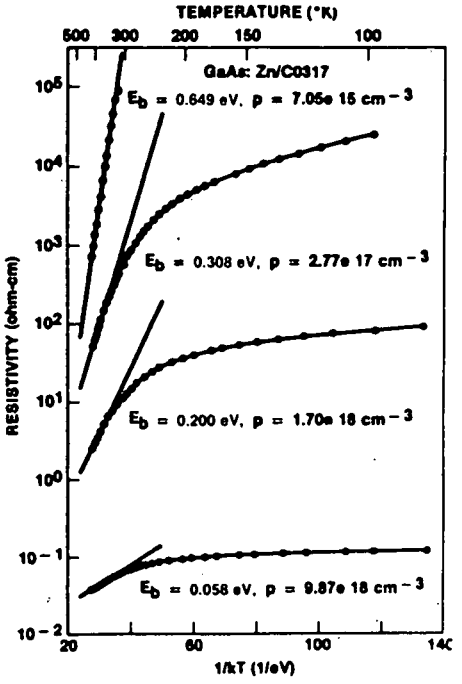

Figure 19. Measured Resistivity of p-type Polycrystalline GaAs Films, Deposited by MO-CVD on Corning Code 0317 Glass Substrates, as Function of Sample Temperature for Various Doping Impurity Concentrations (see text).

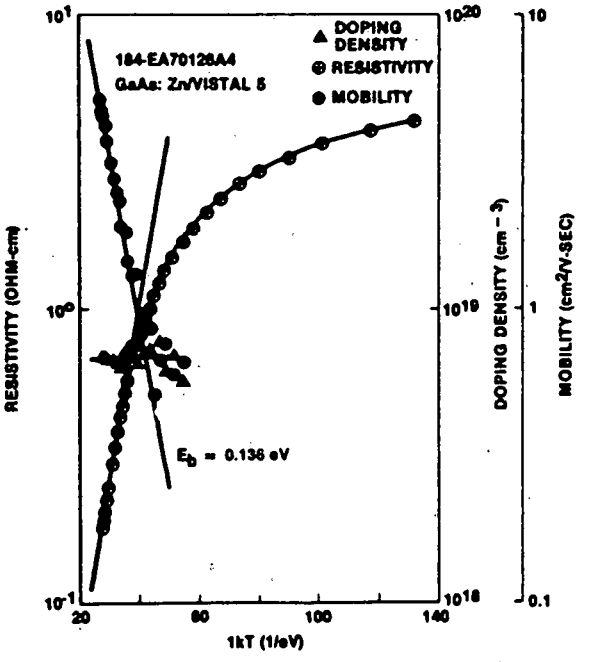

Figure 20. Resistivity, Hole Concentration (Doping Density), and Mobility of p-type Polycrystalline GaAs Film, Deposited by MO-CVD on Vistal 5 Alumina Substrate, as Function of Sample Temperature (see text).

The model that was invoked to explain the data for p-type films involves the assumption that the interface between individual grains is highly defected, with N_t neutral traps per cm^2 of interface area. These traps capture majority carriers until n_t per cm^2 are filled. This results in a depletion region of width (thickness) ℓ on either side of the interface (i.e., the grain boundary). The dipole layer associated with this causes a change in the energy band structure such that a barrier of height E_b is formed at the interface, as shown schematically in Figure 21 for the case of n-type material discussed in the next section.

When the dimension ℓ is much smaller than the size of the grain the barrier height is determined by the number of trapped carriers and the doping density N_D in the grain according to the following relation:

$$E_b = \frac{e^2 n_t^2}{8 \epsilon N_D} , \qquad (1)$$

where e is the electronic charge and ϵ is the dielectric constant of GaAs. The need for carriers to be thermally excited to surmount the barriers at the grain boundaries leads to the expectation that the transport properties of the polycrystalline GaAs films would be temperature-activated. The observed activation energies E_b in the data of Figures 18, 19, and 20 represent those barrier heights.

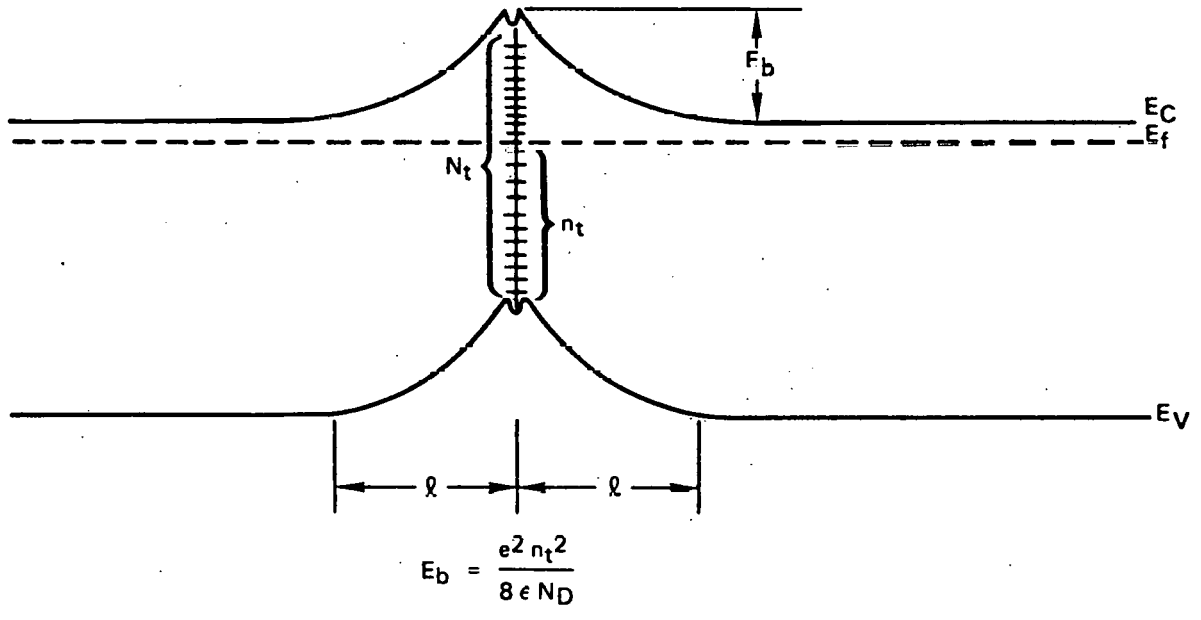

Figure 21. Schematic Diagram of Energy-band Structure at Grain Boundary in n-type Polycrystalline GaAs Film Grown by MO-CVD, Based on Model Discussed in Text.

The above expression for E_b indicates an inverse variation with the doping density N_D – i.e., $E_b \propto 1/N_D$. Figure 22 shows the observed variation of E_b with measured carrier (hole) concentration for both sets of p-type samples. For the range of doping densities investigated (~10^{16} to ~10^{19} cm^{-3}) the variation of barrier height was $E_b \propto \ell n\ (1/p)$, where p is the hole concentration, and not linear with 1/p as the model suggests. This slower observed variation of barrier height with carrier concentration (doping density) is discussed further in Sections 2.2.3.2 and 2.2.3.5.

2.2.3.2 Properties of n-type Polycrystalline Films

The n-type polycrystalline GaAs films were also doped in the ~10^{16} to ~10^{19} cm^{-3} range, with H_2Se used as the dopant source and deposition temperatures again ~725°C. The polycrystalline n-type films on Vistal 5 substrates again contained large numbers of individual crystal grains grown epitaxially on certain orientations of the large grains in the alumina substrates, resulting in generally large-grained growth. The n-type GaAs films grown on the glass substrates were relatively small-grained, as in the p-type case, typically in the range 2-5 μm at the film surface for the film thicknesses (8-10 μm) involved. Ohmic contact to the Se-doped n-type films was made by alloying In dots into the film surface for about 1 min at ~450°C.

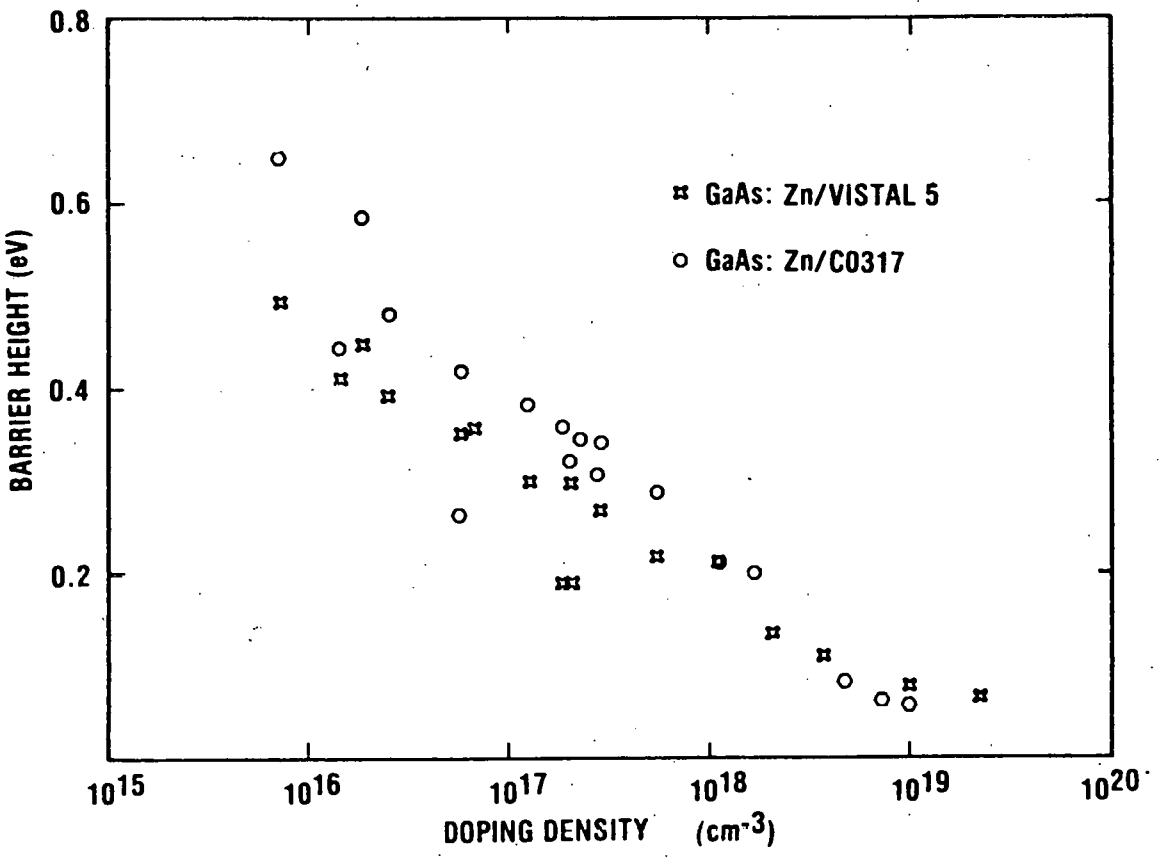

Figure 22. Measured Barrier Height as Function of Doping Impurity Density in p-type Polycrystalline GaAs Films Grown by MO-CVD on Vistal 5 Alumina and Corning Code 0317 Glass Substrates.

Figure 23 shows the room-temperature resistivity of n-type polycrystalline GaAs on both Vistal 5 and 0317 glass substrates as a function of doping concentration. As in the case of p-type material, the resistivity of polycrystalline n-type GaAs is 2-3 orders of magnitude higher than that of single-crystal material doped to the same nominal concentration. Further, the resistivities of films on Vistal 5 are seen to be considerably lower than those of films of the same nominal doping concentration on 0317 glass.

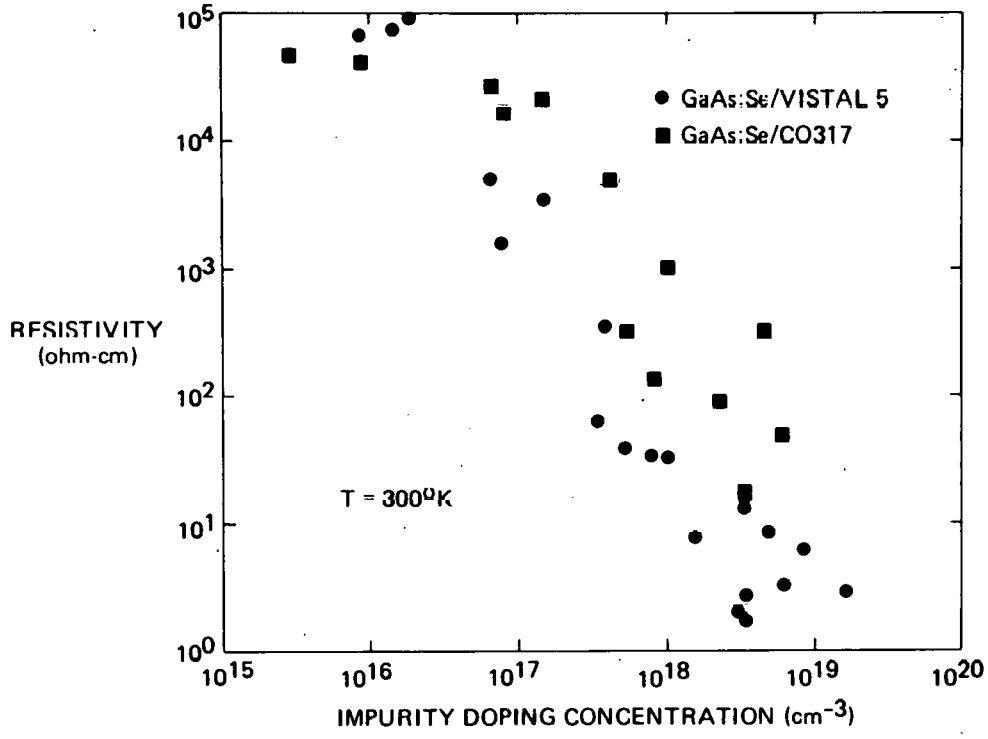

Figure 23. Room-temperature Resistivity of n-type Polycrystalline GaAs Films Deposited by MO-CVD on Substrates of Vistal 5 Alumina and Corning Code 0317 Glass, as Function of Se Doping Concentration (see text).

Resistivity as a function of sample temperature for the n-type polycrystalline films on Vistal 5 substrates and 0317 glass substrates is shown in Figures 24 and 25, respectively. In the temperature range 250-450°K the resistivity in both cases varies as exp (E_b/kT). The activation energy or effective barrier height E_b increases with decreasing doping concentration in the film. Most of the resistivity variation with temperature is caused by a variation of the carrier mobility with temperature, as was found to be the case for the p-type films.

The model discussed in the preceding section for p-type films (but illustrated in Figure 21 for the case of n-type material in the vicinity of a grain boundary) is equally applicable to either conductivity type. The barrier heights E_b obtained from the measured data in Figures 24 and 25 for the n-type films are shown as a function of the measured carrier (electron) concentration in the films grown on the two substrate materials in Figures 26 and 27. Whereas the model (Eq. (1)) leads to the expectation that the barrier height would vary as $E_b \propto 1/N_D$ (i.e., as 1/n for n-type films) the data again show that $E_b \propto \ell n$ (1/n) for the n-type films. Figures 26 and 27 also show the corresponding data for the p-type films on the two substrates, taken from Figure 22. The similar behavior of barrier height as a function of measured carrier concentration for polycrystalline GaAs films of both conductivity types is clearly shown for both Vistal 5 (Figure 26) and Corning Code 0317 glass (Figure 27) substrates.

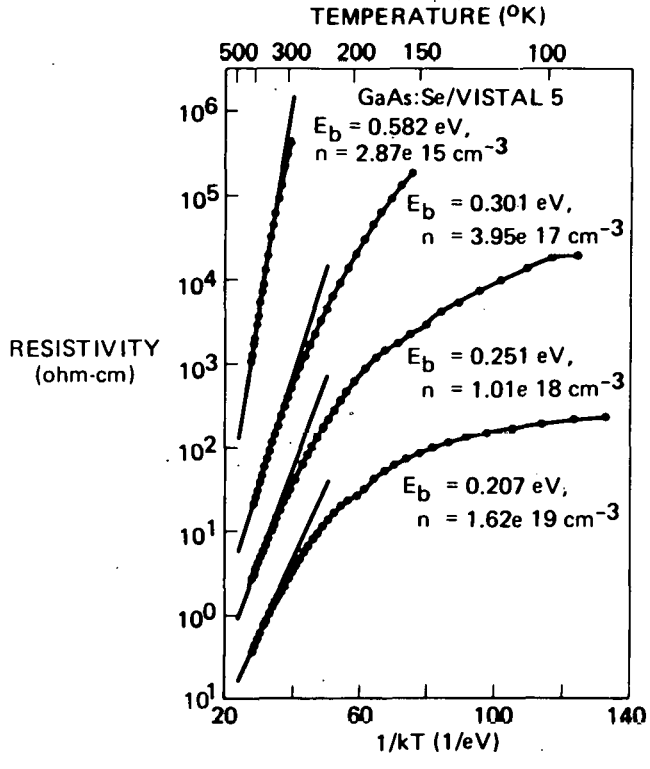

Figure 24. Measured Resistivity of n-type Polycrystalline GaAs Films, Deposited by MO-CVD on Vistal 5 Alumina Substrates, as Function of Sample Temperature for Various Doping Impurity Concentrations (see text).

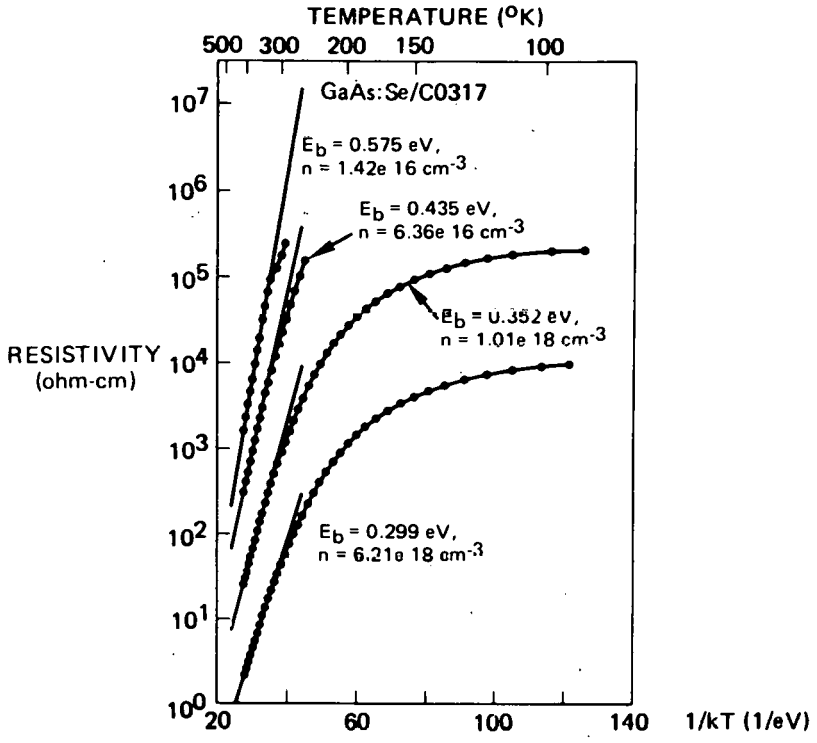

Figure 25. Measured Resistivity of n-type Polycrystalline GaAs Films, Deposited by MO-CVD on Corning Code 0317 Glass Substrates, as Function of Sample Temperature for Various Doping Impurity Concentrations (see text).

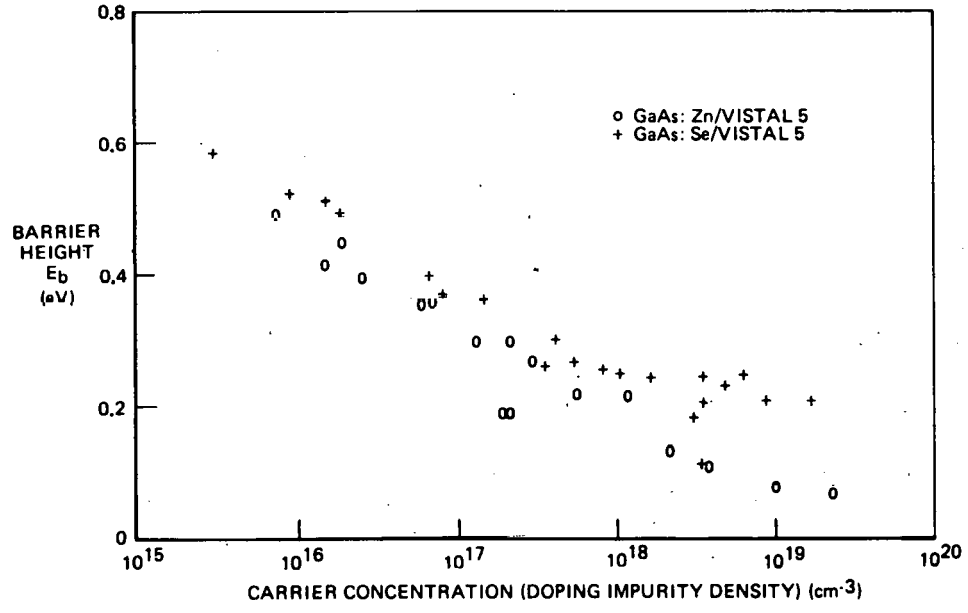

Figure 26. Barrier Height as Function of Measured Majority Carrier Concentration (Doping Impurity Density) for n-type and p-type Polycrystalline GaAs Films Grown by MO-CVD on Vistal 5 Alumina Substrates.

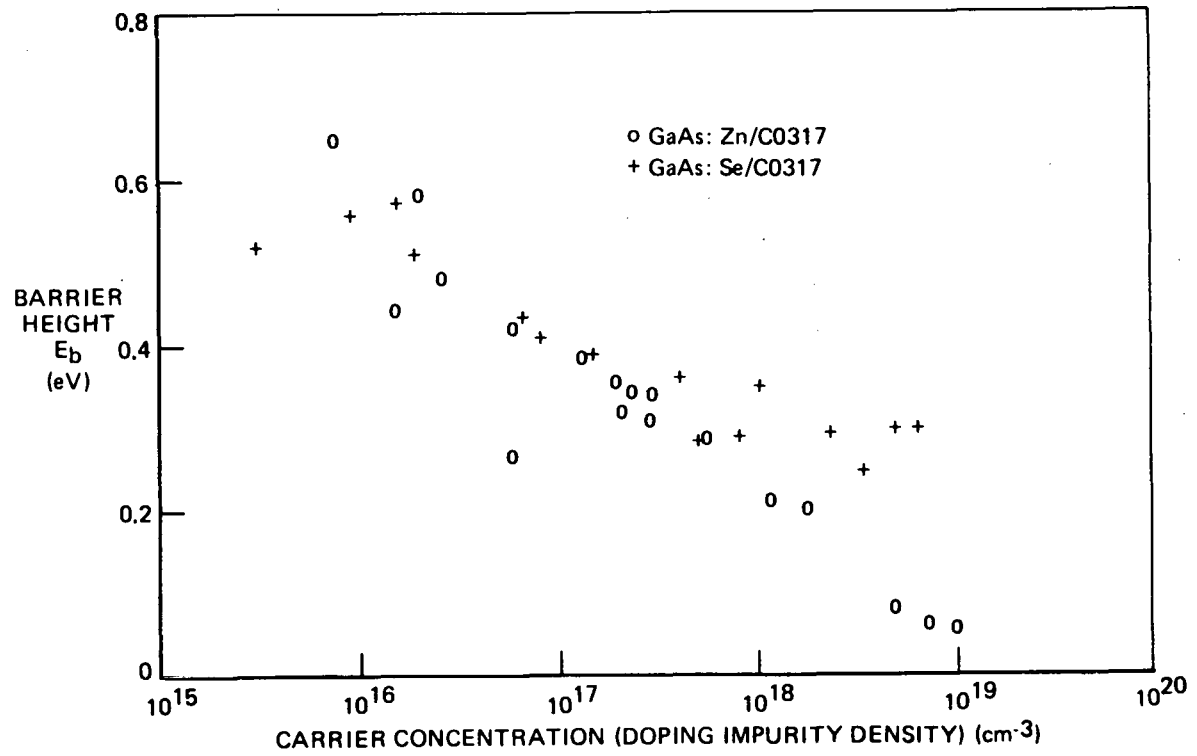

Figure 27. Barrier Height as Function of Measured Majority Carrier Concentration (Doping Impurity Density) for n-type and p-type Polycrystalline GaAs Films Grown by MO-CVD on Corning Code 0317 Glass Substrates.

Since the grain sizes in these polycrystalline films of both conductivity types were large enough that the grains would not be fully depleted over their entire dimensions, it appeared that the model provided a reasonable description of the observed barrier height behavior. It was thus concluded that the density of filled traps n_t must change with doping concentration in such a manner as to give the reduced dependence of E_b upon N_D that was observed in both types of material.

That point was examined further by extracting the value of n_t, the trapped charge density at the grain boundary, from the experimental data using the model and then plotting n_t vs the doping concentration (i.e., the measured carrier concentration) for both types of film. That the measured carrier concentration in the polycrystalline films did in fact bear a linear relationship to the added impurity doping density is indicated in Figure 28. In that figure the carrier concentrations (measured at 400°K) in both n-type (Se-doped) and p-type (Zn-doped) polycrystalline films on Vistal 5 substrates are plotted vs the carrier concentration of the accompanying epitaxial film on sapphire (measured at room temperature), the latter being accepted as a reasonably accurate measure of the actual doping concentration added to all three films in a given deposition experiment. The temperature of 400°K was chosen for the measurements on the polycrystalline films so that films in a wider range of doping concentration could be measured. At this elevated temperature the carrier mobility in the films was sufficiently high (see Figure 20) to permit the measurement of carrier concentration to be successfully made.

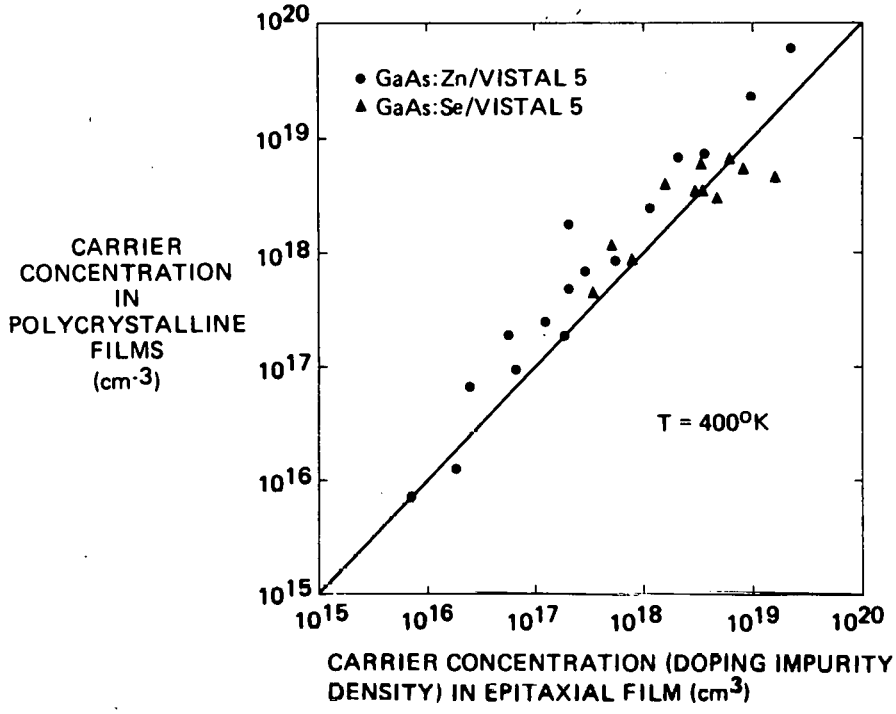

Figure 28. Measured Carrier Concentrations in n-type and p-type Polycrystalline GaAs Films Grown by MO-CVD on Vistal 5 Alumina Substrates as Function of Measured Carrier Concentration (Impurity Density) in Simultaneously Grown Epitaxial GaAs Film on Single-crystal Sapphire Substrate.

Values of n_t were then obtained from Eq. (1) and plotted as a function of doping concentration, with the results shown in Figures 29 and 30 for films on Vistal 5 alumina and 0317 glass, respectively. The value of n_t is seen to increase monotonically with doping concentration up to concentrations approaching 10^{19} cm^{-3}, corresponding to trap densities appraoching 10^{13} cm^{-2}. There is also seen to be strong similarity in the variation of n_t with doping concentration for n-and p-type films on a given substrate material, although a distinct increasing separation of the two curves does occur for increasing doping. Further, there is evident similarity in the two pairs of curves shown in the two figures.

The similarities represented in Figures 29 and 30 viewed in the light of the considerably different values found for the resistivities of the polycrystalline GaAs films on these substrate materials (see Figures 17 and 23) indicated that more quantitative detail was needed for the model to account adequately for all of the observations. Before such additional detail was developed, however, two other questions were examined experimentally - the effect of film thickness on transport properties and the effect of post-deposition thermal annealing on transport properties - to determine if the experimental data being used in developing the model did, in fact, adequately describe the characteristics of the polycrystalline GaAs films.

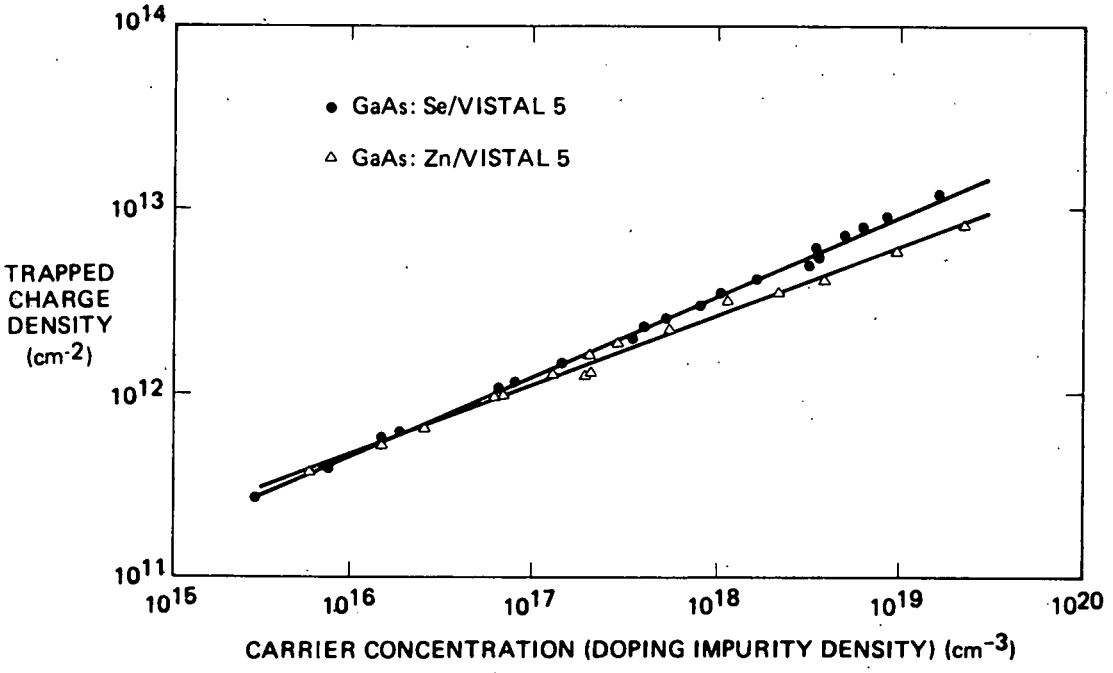

Figure 29. Trapped Charge Density at Grain Boundaries as Function of Impurity Doping Density (Measured Carrier Concentration) in n-type and p-type Polycrystalline GaAs Films Grown by MO-CVD on Vistal 5 Alumina Substrates.

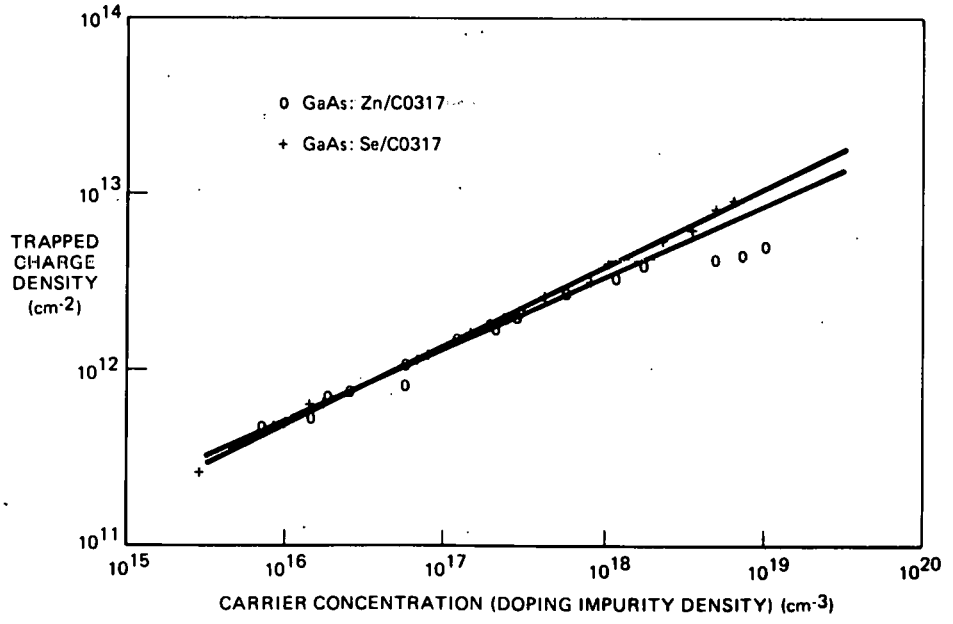

Figure 30. Trapped Charge Density at Grain Boundaries as Function of Impurity Doping Density (Measured Carrier Concentration) in n-type and p-type Polycrystalline GaAs Films Grown by MO-CVD on Corning Code 0317 Glass Substrates.

2.2.3.3 Effect of Film Thickness on Transport Properties of Polycrystalline GaAs Films

The p-type and n-type polycrystalline GaAs films used in the study described in the two preceding sections were all in the thickness range 5-8 μm. It was shown earlier (see Figure 15) that the average grain size in such films tends to increase monotonically with distance from the film-substrate interface. Thus, any film property dependent upon grain size would be expected to depend upon film thickness. Furthermore, the model used to describe the observed film properties indicated that if grain sizes became small compared with the dimensions of the depletion regions at the grain boundaries then the grains would become completely depleted and the film would acquire very high resistivity. For grain sizes of approximately 1 μm this would be expected to occur for doping concentrations of $\sim 10^{15}$ cm^{-3}. Most of the films studied in this work were doped to concentrations greater than 10^{15} cm^{-3}.

However, a variation would be expected in the transport properties of the film with increasing distance from the substrate interface due solely to the presence of the substrate-GaAs interface itself, which would cause depletion of the majority carriers near that interface in each of the individual grains. This would result in a high-resistivity region near the interface, a region totally depleted of free carriers. It would further be expected that in this region the barriers to majority-carrier flow would become quite small, owing to the depletion of the majority carriers and the total exhaustion of the grain. Because of these considerations a systematic study of the dependence of the resistivity of polycrystalline GaAs upon film thickness was undertaken.

This dependence was examined with two approaches. First, previously measured films were remeasured after controlled amounts of GaAs had been etched from the surface of the sample. This produced a thinner film and one which was devoid of the uppermost larger-grain-size regions. While it is quite difficult to ensure totally uniform etching of such polycrystalline films, it had been previously demonstrated that the use of a bromine-methanol etch on polycrystalline GaAs can often produce a film surface that is considerably smoother and flatter than the original surface, with the etch rate apparently uniform and not strongly orientation-dependent. This etch was used on all of the samples in the study described here.

The second approach used was to grow new films of various thicknesses and to study their transport properties as a function of the thickness. No major differences were seen in the results obtained with the two approaches.

Two sets of both p-type (Zn-doped) and n-type (Se-doped) polycrystalline GaAs samples were selected for the study. One was heavily doped, in the range of 10^{19} cm^{-3}, and one was lightly doped, in the range of 10^{16} cm^{-3}, for each of the substrate materials used in the previous detailed studies of transport properties. Measurements of the transport properties were then made as a function of sample temperature in the range 77 to 420°K. The exponential variation of the resistivity vs 1/T in the high-temperature region gave an activation energy for transport in these films. After each such measurement the sample was etched to remove 2-3 μm of the film, and the transport measurements were made again on the thinned film.

For p-type polycrystalline films, it was found after four such cycles of thinning and measuring that the film resistivity consistently increased as the thickness was reduced, for films on both 0317 glass and Vistal 5 substrates. Figure 31 shows the trend observed for both the lightly doped and the heavily doped films on these substrates. However, the barrier heights obtained by observing the thermal activation energies of these p-type films on Vistal 5 were found to be almost independent of thickness, while films on 0317 glass exhibited barrier heights that first increased slightly with reduced thickness and then remained essentially constant for further thickness reductions below about 6.5 μm. These trends were observed in one set of heavily doped p-type films (~10^{19} cm^{-3}) and two sets of lightly doped p-type films (10^{16} cm^{-3} range). Figure 32 shows the variation of the barrier height with thickness in these polycrystalline films. Note that the changes observed were not large; in fact, it was questionable as to whether the changes were experimentally significant or not.

Most of the trends observed in the p-type films were also found in the n-type films. Thus, barrier heights obtained by determining the thermal activation energies from measurements of resistivity remained essentially constant as the film thickness was reduced for n-type films grown on Vistal 5 substrates, and n-type films on 0317 glass exhibited similar behavior for the heavily doped GaAs material. However, for lightly doped n-type GaAs films on 0317 glass the barrier heights first increased as thickness was reduced and then began to decrease with further reduction in thickness to approximately 4 μm. At that point, careful microscopic examination of the films showed that minute holes through the films, distributed over the entire film surface, had appeared either as a result of etching down to voids in the film or due to selective etching along grain boundaries. Consequently, the results for these thinnest layers cannot be considered completely valid.

Thus, the examination of both types of film on both substrate materials indicated the following facts:

1) The resistivity of polycrystalline GaAs films increased as the film thickness decreased, for both n- and p-type material.

2) The intergrain barrier height was found to be essentially independent of film thickness for films deposited on Vistal 5 alumina substrates.

3) The barrier height for films grown on Corning 0317 glass showed some variation with film thickness, increasing initially and then remaining essentially constant with decreasing thickness for thicknesses less than about 6.5 μm.

These observations were interpreted in the following way. The polycrystalline GaAs films deposited on Vistal substrates probably had their structural properties largely determined at the time of initial nucleation and early-stage growth on the individual alumina grains of the Vistal. The epitaxial GaAs growth occurring on many of the large grains of alumina propagated in single-crystal fashion over relatively large areas throughout the film thickness. Transport properties of these films were thus dominated throughout the thickness by grains that were essentially constant in size (i.e., area). As a consequence, not much variation would be expected in the transport properties of much films as the thickness was reduced until thicknesses of perhaps 1 μm or less were realized. Unfortunately, however, most films grown

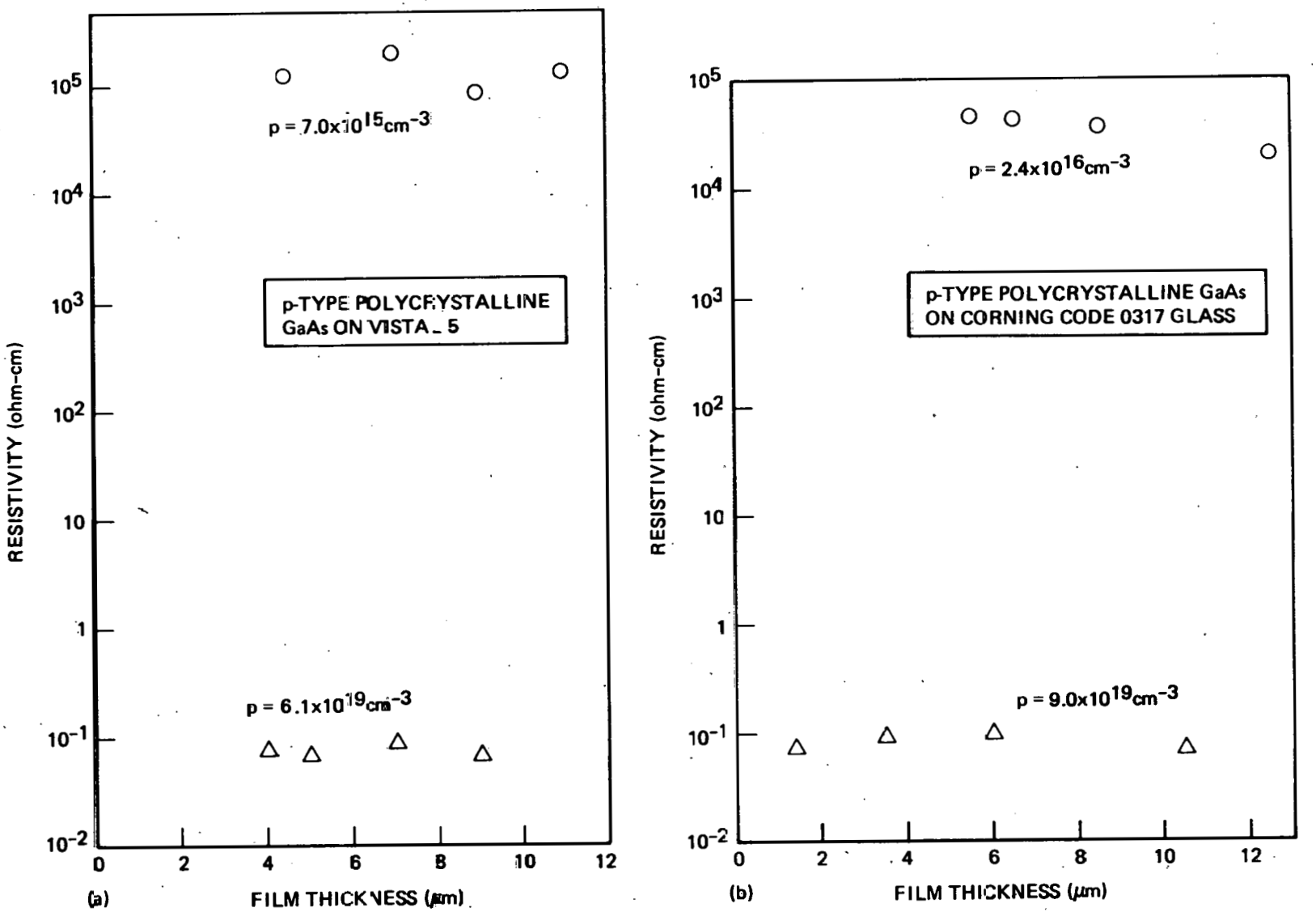

Figure 31. Resistivity as Function of Film Thickness for p-type Polycrystalline GaAs Films for Low and High Doping Concentrations, on Substrates of a) Vistal 5 Polycrystalline Alumina and b) Corning Code 0317 Glass.

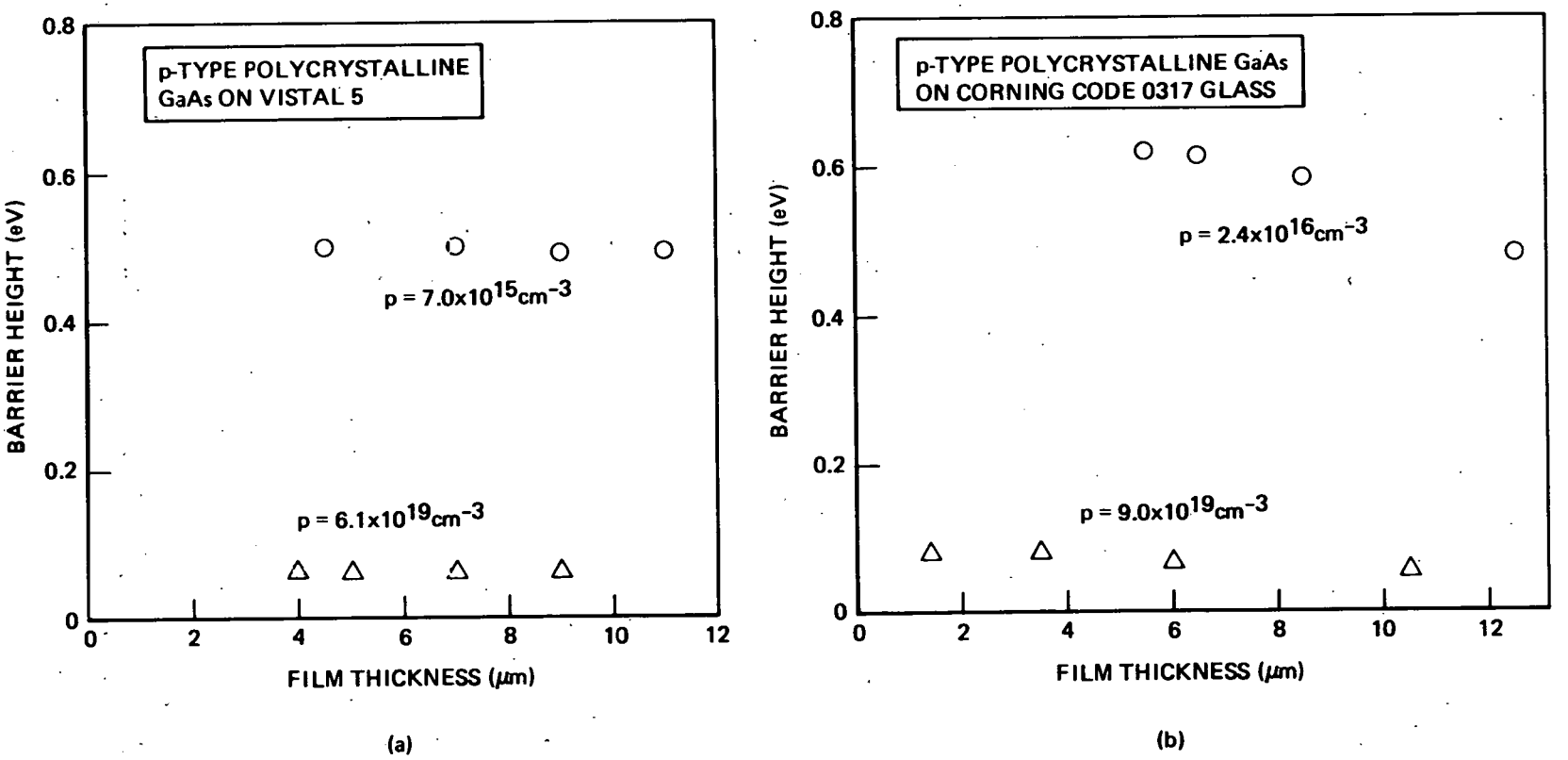

Figure 32. Barrier Height as Function of Film Thickness for p-type Polycrystalline GaAs Films for Low and High Doping Concentrations, on Substrates of a) Vistal 5 Polycrystalline Alumina and b) Corning Code 0317 Glass.

on these substrates in thicknesses of only ~1 μm (average) were discontinuous and could not be used satisfactorily in these studies. Further, thicker films etched to thickness as small as ~1 μm contained sizeable pinholes that rendered electrical measurements invalid. Thus, only films in the range 4-8 μm appeared to permit reasonably valid conclusions to be reached, and for those there appeared to be no significant variation in film transport properties with thickness for growth on Vistal substrates.

Largely similar conclusions were reached for the case of polycrystalline GaAs films deposited on the 0317 glass substrates. As was previously shown in this program (cf Figure 15) and in other studies, there is a nearly linear increase in average grain size with film thickness in polycrystalline GaAs films grown on glass and other amorphous (or microcrystalline) substrates. Since the average grain size found in these films on glass was in the 2-10 μm range for thicknesses of 8-10 μm, the nearly linear variation of grain size with film thickness indicated that films initially 8-10 μm thick that were etched down to thicknesses of only about 4 μm would still not be dominated by grains small enough to have an appreciable effect on the transport properties. Thus, for films exhibiting such a relationship between grain size and thickness (presumably associated with grain growth strongly columnar in nature) relative independence of transport properties and thickness would be expected in the thickness range examined, as was observed.

2.2.3.4 Effect of Thermal Annealing on Transport Properties of Polycrystalline GaAs Films

Most of the GaAs films prepared in this program were deposited at temperatures of 700°C or above in the presence of Ga, As, and H_2. However, it was considered important to investigate the effect of annealing the films at temperatures approaching 700°C for various periods of time in controlled gaseous atmospheres to determine if such treatment would have any effect on the transport properties of the films that might indicate some modification of the grain boundaries that dominate the properties of the films.

To examine such possibilities a series of n- and p-type films with a wide range of doping was subjected to a variety of annealing experiments. Each material type was annealed in H_2 and in H_2-AsH_3 mixtures at temperatures of 500, 600, and 700°C; annealing times were varied from 30 min to 2-1/2 hr. Certain select samples were also submitted to longer anneals, the order of several hours, in AsH_3 and in H_2. Although the study was conducted near the end of the contract and was not completed, the following general conclusions were reached:

1. Significant changes in the resistivity of both n- and p-type polycrystalline GaAs films were observed for several different annealing conditions. In some instances the changes were observed only for measurements in the sample temperature range above room temperature, while in other cases the resistivity changes were found only in the sample temperature range near 77°K. The various annealing experiments that were carried out did not provide sufficient consistent data to permit development of an explanation for the results obtained. However, the results emphasized the inhomogeneous nature of the conduction process in the films and the fact that in different temperature ranges the dominant conduction mechanism in these films may itself be different.

2. There were no significant changes, except in one group of samples, in the measured activation energies for these films following the various annealing treatments. It was thus tentatively concluded that annealing in H_2 and/or in AsH_3 had no major effect on the intergrain barrier heights that control the transport properties of these polycrystalline films.

The variety of annealing effects that were observed in this uncompleted study was such that no single model for the processes involved appeared applicable. Additional experiments must be done to clarify the results obtained. It is possible that a greater variety of sample environments during annealing, a larger number of samples, and films deposited on a greater variety of substrate materials would lead to a consistent model for the effects of thermal annealing. However, the structural complexity of these polycrystalline films - especially with regard to crystallographic orientation relationships at the grain boundaries - and the degree of inhomogeneity of the annealing effects that could result for the various regions of the material indicate that it might be more instructive to carry out the additional studies on samples having more systematically related (i.e., less random) grain boundaries - for example, on large-grain bulk polycrystalline GaAs. Such samples might even permit an analysis of annealing effects on transport across single grain boundaries. In any case, the simpler structures represented in such samples should make it possible to identify annealing processes that also probably occur in the more complex structures of the polycrystalline films, and thus to better understand the annealing effects observed in these preliminary studies.

2.2.3.5 Model for Grain-boundary Surface States in Polycrystalline GaAs Films

The model used for interpreting the results of the transport measurements on polycrystalline GaAs films described in Sections 2.2.3.1 and 2.2.3.2 assumes that the juxtaposition of two individual crystal grains produces an interface that contains defect states. These defect states, which are neutral initially, can become charged by the capture of majority carriers from the inside of the individual grains, thus depleting a region of the grain of its free majority carriers. The number of carriers so captured depends upon the density of the interface states and the available number of free carriers within the grain. For most of the samples that were studied in this work the number of free carriers within the grain was much greater than that which was depleted to fill the interface states at the grain boundary.

The resulting grain-boundary region was represented schematically in Figure 21, for the case of n-type material. The bulk of each grain is characterized by a Fermi level which specifies the number of free carriers within the conduction band (for n-type material). In the region near the grain boundary the conduction band for n-type material is bent upward, as indicated in Figure 21, to accommodate the depletion region caused by the capture of carriers at the interface states. These interface states or traps, of density N_t per cm^2 of interface area, in turn are partially filled to a density of n_t per cm^2 with carriers from the bulk of the grain. This results in the barrier of height E_b, as shown in the diagram in Figure 21.

The number of carriers captured at the grain boundary can be related to the total number of traps in the grain boundary by the expression

$$n_t = \int_{-\infty}^{\infty} N_t(E)F(E)dE \quad , \tag{2}$$

where F(E) is the Fermi distribution function. This expression states that the total number of carriers trapped at the interface is the integral sum of the number of available states distributed in energy at the interface times the probability that each one of these states is, in fact, occupied. More can be learned from this expression by taking its partial derivative with respect to E_b, the barrier height:

$$\frac{\partial n_t}{\partial E_b} = \int_{-\infty}^{\infty} N_t(E) \frac{\partial F(E)}{\partial E_b} dE. \tag{3}$$

At low and moderate temperatures the Fermi function F(E) changes rapidly from a value of unity at energies below the Fermi level E_F to zero at energies immediately above the Fermi level. As a result, the derivative of the Fermi function is sharply peaked, with the peak located at the argument of the Fermi energy. Thus, since $\partial F(E)/\partial E \approx \delta E$, Eq. (3) becomes

$$\begin{aligned} \frac{\partial n_t}{\partial E_b} &= \int_{-\infty}^{\infty} N_t(E) \frac{\partial F(E+E_b)}{\partial E} dE \approx \int_{-\infty}^{\infty} N_t(E)\, \delta(E-E_F+E_b)dE \\ &\approx N_t(E_F-E_b) \quad . \end{aligned} \tag{4}$$

Substitution of Eq. (1) of Section 2.2.3.1 into Eq. (4) gives the following:

$$N_t(E_F-E_b) \approx \frac{4\epsilon N_D}{en_t} \quad , \tag{5}$$

which represents the distribution of traps over the energy gap of the material with impurity doping concentration N_D.

Thus, the distribution of traps among the various energy levels within the bandgap can be determined by relating the barrier heights and the trapped carrier densities for a given impurity concentration in the polycrystalline material. Using the experimentally determined barrier heights and trapped carrier densities and calculating the Fermi level at each doping concentration the distribution of traps at the interface was determined.

Figure 33 shows the distribution of traps $N_t(E)$ at the interface determined by this analysis. The density of both electron and hole traps increases exponentially

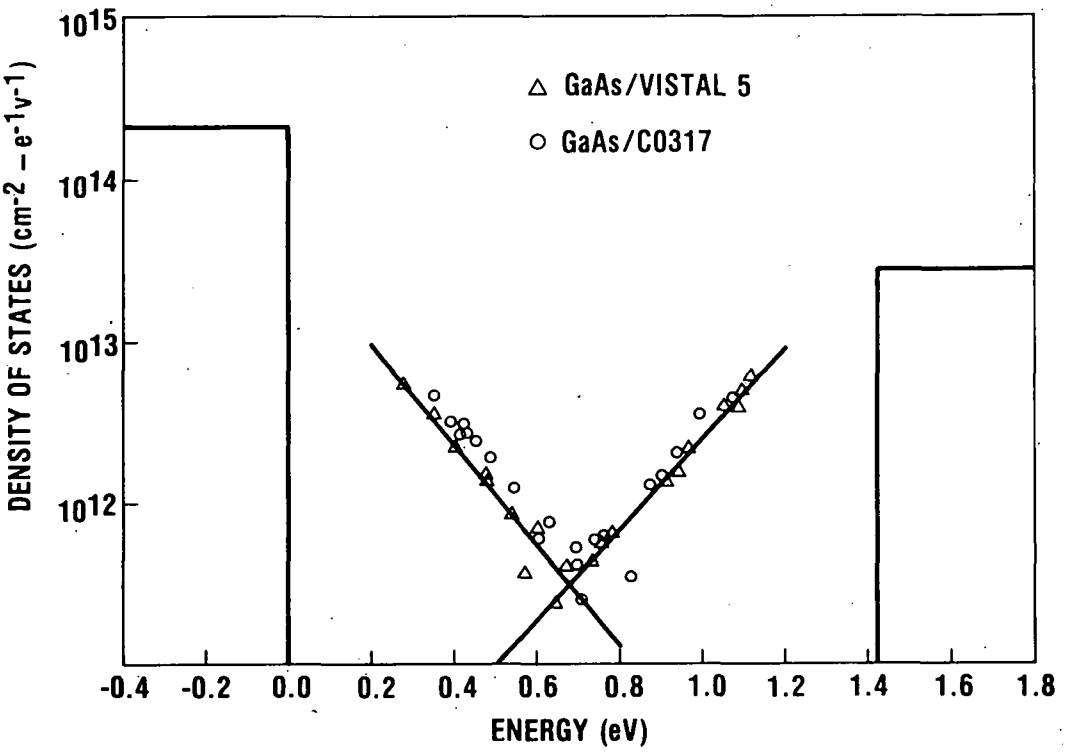

Figure 33. Schematic Representation of Densities of Interface States at Grain Boundary and Partial Densities of States in Valence and Conduction Bands in Polycrystalline GaAs.

away from mid-gap toward the band edge, appearing much like an exponential band-tail of exceedingly high density. When these experimental results are compared with the densities of states in the conduction and valence bands the result is a band model with a high density of localized states "tailing in" from the conduction band and the valence band, with the tails of the conduction and valence bands overlapping at mid-gap.

These results are reminiscent of models previously put forth for the properties of amorphous materials. When the disorder and band bending in the material is large enough the density of states at the edges of the conduction and valence bands becomes considerably "smeared," and tails extend deep into the forbidden gap of an ordered semiconductor resulting in material in which the conduction band and valence band tails essentially overlap. It is possible that the regions in the grain boundaries that are controlling the transport properties of these polycrystalline GaAs films are amorphous in nature. That is, they may be highly disordered, with bands that are extremely distorted and which in turn result in energy band distributions that are extremely "fuzzy" and poorly defined in energy.

In summary, it can be stated that these calculations and the detailed measurements of the transport properties of polycrystalline GaAs together constitute a relatively comprehensive study of the properties of these materials as prepared by the MO-CVD process. It should be emphasized, however, that the interpretation presented here extends considerably beyond the fundamental measurements made,

and as a result is subject to some question. The interpretation is based on the concept that transport within the polycrystalline films is dominated by certain grain boundaries that are characterized by large barrier heights. Many, if not all, of the other grain boundaries that are in series with those having large barrier heights may, in fact, be characterized by low barrier heights and thus not represent serious impediments to the flow of majority carriers. However, the few grain boundaries that do represent significant barriers to the flow of majority carriers tend to dominate the transport properties of the films. This concept is similar to the "percolation" model previously suggested by Bube (Ref 14) and by Seager (Ref 15) to explain the properties of other polycrystalline materials, and it appears to provide a reasonable interpretation of the transport properties of the polycrystalline GaAs films.

2.3 TASK 3. INVESTIGATION AND DEVELOPMENT OF BARRIER FORMATION TECHNIQUES

This task involved investigation and development of various techniques for the formation of the necessary charge collecting barriers in polycrystalline GaAs thin-film photovoltaic devices. Emphasis was on direct growth of p-n junction structures by the MO-CVD process, but also included were alternate barrier-forming techniques such as the use of a thin Schottky barrier at the film surface and the use of deposited indium-tin-oxide (ITO) layers on the film surface.

The work of this task during the second year of the program included activity in the following specific areas: 1) p-n junction formation by doping during growth; 2) preparation of Schottky-barrier devices using deposited Au layers; and 3) formation of ITO-GaAs heterostructures. This work is summarized in the following sections.

2.3.1 Investigation of p-n Junction Structures Formed in Polycrystalline GaAs Films by Doping during Growth

Most of the deposited polycrystalline GaAs p-n junction structures made during the first year of this contract had exhibited excessive leakage currents (Ref. 1). Considerable attention was given this problem during the second year in an attempt to obtain a better understanding of the causes.

2.3.1.1 Characteristics of Deposited p-n Junctions

Early in the year a series of polycrystalline junction structures was prepared by MO-CVD growth using three different composite subtrates - 1) sputtered Mo (~0.2 μm thick) on Corning Code 0317 glass, 2) sputtered Mo (~0.2 μm thick) on Corning Code 7059 glass, and 3) Ge deposited by CVD (GeH_4 pyrolysis) on Corning Code 0317 glass. Both n/p and p/n structures were investigated. The doping concentration of the bottom layer (adjoining the substrate) was typically varied slightly in the 10^{17} - 10^{18} cm^{-3} range. Layer thicknesses were also varied slightly, ranging from ~2.5 μm each to ~5.0 μm each.

The junction structures were prepared for evaluation by one of two procedures. In the first, a lightly alloyed contact of In was formed on the top (p-type) layer, followed by etching of the edges of the composite sample around the entire sample

periphery, to remove any edge-shorting effects. This simple procedure suffered, however, from the uncertainty concerning the resulting area of the device and the possibility that the In might have alloyed completely through the upper layer. The second procedure, intended to avoid the latter possibility, involved a point contact in place of the alloyed contact. For the heavily doped top layers used in most of the devices such a contact was found to be sufficiently ohmic to permit adequate qualitative determination of the junction properties. However, such a contact was of limited value in determining the properties of large-area junctions at high current densities because of the high sheet resistance of the polycrystalline GaAs. Nonetheless, the point-contact method was useful as a non-destructive screening procedure for use with polycrystalline materials, as discussed in Section 2.2.2.

The typical procedure for evaluating a polycrystalline junction was 1) to step-etch the sample in such as way as to reveal a portion of each layer in some region of the sample, 2) to obtain an indication of the doping concentration in each layer by the point-contact reverse-breakdown (PCR) measurements described earlier, and 3) to obtain the junction I-V characteristics on a curve tracer by making probe contacts to the top layer and to the conducting layer of the composite substrate. In most cases the doping level indicated by the PCR measurement was as expected on the basis of the growth parameters used.

The first samples that were examined involved mainly substrates with Ge intermediate layers. When the resulting junctions consistently showed shorted or excessively leaky characteristics at ~10 mA/cm^2 current densities the use of Ge intermediate layers was stopped. While it was not clear that the presence of Ge created additional problems, the removal of any additional degrees of uncertainty was considered necessary.

Mo-coated substrates dominated the next group of samples studied. Initial samples were grown with junction doping profiles that simulated those of single-crystal cells prepared earlier in the program. Subsequent samples involved variations in both n- and p-layer doping levels. In all cases, the junctions showed excessive leakage currents and generally poor I-V characteristics.

The most likely reasons for these observed junction properties appeared to be (1) a film growth morphology that was such that the top layer (usually p type) did not fully cover the bottom layer, and (2) diffusion of Zn from the p-type top layer along the grain boundaries of the polycrystalline structure so as to short the bottom n-type layer.

The first possible cause appeared to be ruled out by the flat and continuous p-type layer that was repeatedly observed in the angle-lapped sections made on junction samples having p layers ~5 μm thick, as indicated earlier (Section 2.2.2). Also, the fact that similar junction structures grown in two separate deposition experiments - by depositing a p-type Zn-doped layer on the smooth etch-polished surface of a previously grown n-type layer - were also shorted tended to argue against the validity of the first cause listed above.

The second possible cause, that of Zn diffusion along grain boundaries, seemed far more likely. To examine the possibility further, p-n junctions with asymmetric doping concentrations (i.e., p^+-n and p-n^+ structures) were grown and characterized.

Again, for both structures excessively leaky junction properties were observed. In addition, it was found that the voltage breakdown properties of n layers were no different before and after the growth of p layers on top. This indicated that there were probably no shorting regions extending from the junction to the conducting substrate as would be expected if Zn had diffused down the grain boundaries.

Whereas essentially all small-grained polycrystalline p-n junctions with doped p and n regions grown on low-cost substrates had shown very leaky I-V characteristics, p-n junction structures similarly grown on large-grained bulk polycrystalline GaAs substrates exhibited quite good rectifying I-V characteristics and were very light-sensitive. In the latter devices a small-area (50 mil x 50 mil) Au-Zn-Au contact was applied to the top of the p-type polycrystalline layer and alloyed to form an ohmic contact, and the n-type contact was made directly to the substrate. The top contacts were then used as masks for the etching of mesa diodes into the polycrystalline GaAs layer structure. The possibility that different types of grain-boundary properties were involved in the fine-grained films grown on low-cost substrates and the large-grained films grown on bulk polycrystalline GaAs wafers appeared to be indicated by these results.

Further attempts were made to determine if grain-boundary shorting was occurring in the MO-CVD layers by use of Schottky-barrier structures deposited directly over grain boundaries. Those experiments are described in Sections 2.3.1.2 and 2.3.1.3.

2.3.1.2 Properties of p^+-i-n^+ Multilayer Junctions

A group of experimental junction structures was prepared involving very low doping concentrations on one side of the junction, and preliminary measurements indicated that junction leakage was reduced considerably by this simple modification. These p^+-i-n^+ structures, in which the undoped i region was n type due to a low concentration of some unidentified donor, were deposited on substrates of large-grained bulk Mo and also sputtered Mo films ($\sim$0.2 μm thick) on Corning Code 0317 glass. The middle (I) layer was intentionally undoped in an attempt to eliminate the possibility of forming a tunnel junction in the grain boundaries. Such tunnel junctions might be formed as a result of impurity segregation in the grain boundaries, especially since relatively high doping concentrations had been used in the polycrystalline p-n structures to obtain as low a series resistance as possible, and could be the cause of the high leakage currents observed.

Consequently, various polycrystalline GaAs multilayer structures that were modifications of the basic p-i-n structure were prepared. Thus, $p^+/p/I/n/n^+$, $p^+/i/n^+$, and $n^+/n/i/p$ structures were deposited on substrates of bulk Mo sheet and sputtered Mo films on Corning Code 0317 glass, with the thickness of the i layer having various values in the range 1.5-4.0 μm and the impurity doping concentration on both sides of the junction (the p-i interface) also varied. Typical combinations of doping concentrations and thicknesses for the various layers were as follows:

$p^+ \approx 1 \times 10^{19}$ cm^{-3} $\qquad$ $t_{p^+} \approx 1.5$ μm

$p \approx 1 \times 10^{18}$ cm^{-3} $\qquad$ $t_p \approx 6$ μm

$n_i \approx 1 \times 10^{15}$ cm^{-3} $\qquad$ $t_i \approx 1.5$-4.0 μm

$n \approx 2 \times 10^{18}$ cm^{-3} $\quad t_n \approx 6$ μm

$n^+ \approx 2 \times 10^{19}$ cm^{-3} $\quad t_{n^+} \approx 1$ μm

The n^+ layer, when used, was designed to facilitate ohmic contact to the Mo substrate. The indicated doping concentration in the i layer represents the measured carrier (electron) concentration found to be characteristic of the background doping level being obtained in the MO-CVD reactor system at the time these samples were prepared.

It was found that the structures with thicker i layers (3.5-4.0 μm) gave significantly better results, although the I-V characteristics were still quite "soft" and forward turn-on voltages in the best of the devices were still only 0.5-0.6V. Also, the structures with reduced doping concentration in the p layer gave slightly less leaky I-V characteristics, but the general junction properties were still inferior.

To provide larger GaAs grains in which to fabricate similar devices, thicker composite-layer structures were grown on Mo sheet substrates. Structures in the $p^+/n/n^+/Mo$ configuration (actually $p^+/i/n^+/Mo$) were prepared with 10 μm n-type layers and 20 μm n^+ layers. The p layers were only 1 μm thick. The carrier concentration in the undoped n layers was ~10^{15} cm^{-3}, as previously.

Mesa devices were fabricated on these layers by etching through the p layer to a depth of ~5 μm. The top of the p layer was contacted with Cr-Au to avoid the need for alloying. The I-V characteristics of these devices were not substantially different from those seen on thin samples 5 - 10 μm thick. All were excessively leaky and permitted no worthwhile photovoltaic measurements.

These results suggested the following: (1) grain sizes in the range 5 - 10 μm were probably not sufficient to provide reasonable quality p-n junctions in this material, and (2) diffusion of Zn along grain boundaries to provide a shunt path was probably not a significant problem, since the devices of thickness ~30 μm and those of thickness only 5 μm behaved similarly.

To test the latter hypothesis a 5-8 μm thick $p^+/i/n^+$ structure with relative layer thicknesses 1:4:1 was evaluated by I-V and C-V analyses. The I-V characteristic showed a turn-on voltage of 0.5-0.6V and shunt leakage across the junction. The C-V characteristics showed an abrupt junction with a built-in barrier of 0.5V. The player was then etched off the sample and Au Schotty barriers were deposited on the n layer. The resultant devices showed good Schotty-barrier characteristics with reasonably low leakage, lower than found for the p-n junction. If Zn were diffused into the grain boundaries the Schottky barrier would be expected to draw a low forward voltage and exhibit considerable leakage. The C-V characteristics showed a non-ideal

plot of $1/C^2$ vs V and an extrapolated barrier height of 2.0 eV; these results are not easily explained. It is possible that an m-i-n structure was formed by the inclusion of an inadvertent oxide, but this was not established.

2.3.1.3 Effect of Grain Boundaries on p-n Junction Cell Properties

To determine the effect of discrete grain boundaries in polycrystalline GaAs films on the I-V characteristics of p-n junctions grown in these films a series of p/n and n/p device structures was deposited on large-grained bulk polycrystalline GaAs substrates.

The epitaxial but multicrystalline layers were etched to form 0.050 x 0.050 in mesas so that the I-V characteristics of a number of regions of differing structural characteristics could be compared. In particular, an attempt was made to correlate the junction leakage in a given mesa diode with the apparent number of grain boundaries intercepting the mesa. The strongest correlation observed was that among various diodes in certain areas of the sample all of the I-V characteristics were leaky regardless of the number of intercepting grain boundaries involved. No strong correlation could be found between mesa-diode leakage current and the number of grain boundaries in the mesa, even for mesas containing as many as 20-40 grain boundaries.

Detailed low current I-V characteristics were also obtained for many of these mesas, and these were compared with the data taken on an I-V curve tracer. The initial observations were confirmed; that is, no strong correlation could be observed between the number of grain boundaries in a mesa and the forward I-V characteristic of the device. This prompted speculation as to the cause of this lack of correlation, including possible experimental errors which could have caused it.

Earlier work on the etching of fine-grained polycrystalline materials had indicated that bromine-methanol etching resulted in uniform non-selective etching of grains as well as grain-boundary regions in polycrystalline GaAs. As a result, this etch was used in the mesa etching step mentioned above. However, upon closer microscopic examination of the mesas etched in this study it was discovered that in virtually all cases very strong and highly selective etching of the grain-boundary regions had occurred during mesa delineation. In fact, in most cases the grain-boundary region was selectively etched completely through the mesa, so that the grain-boundary regions were effectively removed as contributors to the electrical properties of each of the mesas. Only those mesas where excessive leakage occurred had grain boundaries that were not completely etched through the mesas.

This result seemed to indicate that the grain boundaries were strong contributors to junction leakage. However, in the few samples that were prepared for this study not enough mesas with varying numbers of grain boundaries and types of grain boundaries were available for examination after the processing to provide the amount of data required to indicate distinct trends. Further investigation of the type undertaken here should be carried out to explore the problem in greater detail. It is believed that such studies would provide valuable information on the effects of grain boundaries on junction and cell properties.

It is interesting to note that the presence of grain boundaries in the region of a p-n junction grown in a film on a bulk polycrystalline GaAs substrate did not result in any marked tendency for high leakage currents and/or low forward voltages. The fact that these weaknesses in the junction characteristics were found, however, for the polycrystalline GaAs structures grown on low-cost substrates again suggests that the grain boundaries generated by the vapor-growth process (on dissimilar substrate material) may be considerably different from those that are produced during bulk crystal solidification from the melt (and propagated into the film during the deposition process). This possibility should be further investigated.

2.3.1.4 Effect of Modified MO-CVD Growth Parameters on p-n Junction Cell Properties

A brief investigation of the effects of modified MO-CVD film growth parameters on the I-V characteristics of p-n junction cell structures formed by sequential deposition of polycrystalline films was undertaken late in the program. Most of the previously grown p-n junction cells in fine-grained polycrystalline material had exhibited leaky I-V characteristics with strong evidence of a shunt resistance component in both the forward and the reverse characteristics, and in some cases showed complete shorting, as discussed in earlier sections. Several of the p-i-n structures prepared with modified deposition parameters, however, exhibited some improvement, although the I-V characteristics so obtained were still considerably poorer than those considered necessary for high-efficiency cells.

Since p-n and n-p structures had usually exhibited more severe leakage and much lower shunt resistances, all of the structures in this series were prepared in the p-i-n configuration. The n (i.e., the i layer) and n^+ layers were deposited in the usual deposition temperature range of 700-725°C, with Mo as the substrate material. Because of continuing concern about the possible role of Zn diffusion along grain boundaries in the leaky I-V characteristics usually observed, it was determined that the p layers would be deposited at significantly lower temperatures, specifically, 550 to 600°C. It was believed that this might reduce Zn diffusion along grain boundaries sufficiently to bring about an improvement in device performance.

The forward and reverse characteristics of the devices appeared not to be dominated by shunt resistances at bias voltages less than 0.5V. However, the forward I-V characteristics indicated a turn-on voltage of 0.5-0.6V, considerably less than the 0.9-1.0V expected for single-crystal GaAs devices. Detailed I-V characteristics at low currents were to be obtained on these devices to determine the differences in current transport between these devices and earlier structures which showed a stronger shunting resistance. However, those measurements were not completed prior to the end of the contract program.

2.3.2 Preparation of Schottky-barrier Devices on Polycrystalline GaAs Films

Schottky-barrier device structures employing thin Au layers were routinely used for evaluation of polycrystalline GaAs films and multilayer structures in this program. Such devices were successfully fabricated on a variety of materials. The

typical device design involved a vacuum-deposited Au film ~50Å thick to form the Schottky-barrier. (However, see Section 2.3.2.2.) The principal results of the work with Schottky-barrier structures are described in the following sections.

2.3.2.1 Properties of Au Schottky-barrier Solar Cells on n/n^+ Polycrystalline GaAs Structures

The dependence of Schottky-barrier solar cell efficiency upon the doping concentration in the polycrystalline GaAs was found to be a complicated multivariable problem. The depletion layer depth and diffusion length in n-type material are expected to decrease with increasing doping concentration, thus reducing short-circuit current. The resistance of the device should decrease but the leakage current in the device should increase with increasing doping. Furthermore, the importance of these effects may be masked or enhanced by the details of the processes ocurring at grain boundaries.

A brief study of the effect of n-layer doping upon the performance of Schottky-barrier solar cells on polycrystalline GaAs was carried out by varying the doping of the n layer of n/n+/Mo structures. The short-circuit currents derived from such devices under 1 kw xenon lamp excitation of 137 mw/cm^2 intensity are given in Table 1. These devices were all fabricated at the same time and had approximately the same Au layer thickness of ~50Å. The doping concentrations were determined indirectly on the basis of the measured properties of similar films prepared with the same deposition parameters at the same time.

The sharp decrease in short-circuit current for n-layer concentration above 10^{16} cm^{-3} was not expected and is not understood. It suggests, however, that in films with this range of grain sizes (~2 μm) the collection of current in the depletion layer plays a significant role in the short-circuit current collection process. The table also shows the corresponding depletion depths for single-crystal GaAs doped

Table 1. Characteristics of Au* Schottky-barrier Solar Cells Fabricated on Polycrystalline GaAs n/n^+ Structures Deposited by MO-CVD on Mo Sheet Substrates

Impurity Doping Concentration in n Layer (cm^{-3})	Short-circuit Current under Illumination** (μA)	Depletion Layer Depth at Zero Bias (μm)
10^{15}	185	1.2
10^{16}	170	0.35
10^{17}	10	0.12
10^{16} (on Mo/glass substrate)	170	0.35

* Au vacuum-deposited layer ~50Å thick

** 1 kw xenon lamp illumination of 127 mw/cm^2 intensity

to the listed concentrations. It appears that there must also have been a strong dependence of diffusion length upon doping in these films to account for the effects illustrated by the data. To obtain high conversion efficiencies in Schottky-barrier solar cells in such small-grained materials may require doping concentrations of 10^{16} cm^{-3} or below in the n-type layers. This point requires additional investigation.

2.3.2.2 Effect of Au Layer Thickness on Performance of Schottky-barrier Devices on Polycrystalline GaAs

Most of the Schottky-barriers used in this program prior to the final five months of the contract were formed by vacuum-depositing Au to a thickness of approximately 50Å onto the GaAs surface. This thickness was selected primarily on the basis of previous experience with such structures on single-crystal GaAs.

At times, however, especially when the polycrystalline GaAs films used were relatively rough, it appeared that the 50A Åu metallization was too thin to provide good contact to all of the surface grains. Consequently, a limited study was made of the effect of the Au layer thickness on the resulting performance of Schottky-barrier devices.

A set of similar n/n^+ GaAs structures deposited on Mo sheet substrates in a single run was used to fabricate a group of Schottky-barrier solar cells. Au layer thicknesses of 25, 50, 75, and 100Å were deposited on these structures in the usual way. The n layer thickness was ~10 μm, with a doping concentration of 10^{16} cm^{-3}; the n^+ layer was 5 μm thick, doped to a concentration of 2×10^{18} cm^{-3}. The thickness of the Au layer in each case was deduced from the deposition parameters by observing the frequency change in a quartz-crystal film-thickness deposition monitor, based on a calibrated frequency for a Au film of known thickness (500Å).

The observed photoresponses for these Schottky-barrier cells on polycrystalline GaAs are summarized in Table 2. All of the data are for AM0 operation, with no antireflection coating applied. The device with the 25A Au layer exhibited no photovoltaic response, due probably to inadequate coverage by the metal film. The data indicate that once the barrier metal is thick enough there is only a small

Table 2. Photoresponse* of Au Schottky-barrier Solar Cells as Function of Thickness of Au Layer

Au Layer Thickness (Å)	V_{OC} (2 C. volts)	I_{SC} (mA)	Fill Factor	Conversion Efficiency (%)
25	0.67	0	--	--
50	0.47	0.20	0.44	1.9
75	0.40	0.20	0.58	2.1
100	0.43	0.19	0.56	2.2

*Illumination ~AM0 (xenon lamp), with no AR coating

change in the collected current with further increase in the Au thickness up to 100Å. Most of the observed change in conversion efficiency in these samples was caused by an increase in the cell fill factor with increase in Au thickness due to the lowered series resistance of the cell. There was some variation observed in open-circuit voltage from device to device on a given sample in this group; the efficiencies given in the table represent the best obtained among the various individual devices on a given sample.

Based on these limited results it was determined that Au film thicknesses of 75-100Å would be used thereafter for the Schottky-barriers prepared on polycrystalline GaAs films in this program.

2.3.2.3 Effect of Atmospheric Exposure on Properties of Au Schottky-barrier Solar Cells on Polycrystalline GaAs

A limited investigation of the effect of atmospheric exposure on the properties of Au Schottky-barrier solar cells on polycrystalline GaAs was carried out. The purpose of the study was to determine if the apparently random variation in V_{OC} values occasionally observed from sample to sample in these devices might actually have been the result of varying amounts of native oxide inadvertently grown on the GaAs surface.

Schottky-barrier solar cells previously formed in this program on polycrystalline GaAs were typically measured within 24 hours of the time of fabrication of the devices. However, in some cases the devices were measured after a longer period of time. Because of the extreme thinness of the Au Schottky barrier, it was speculated that the diffusion of oxygen through the gold layer could result in the oxidation of the GaAs surface, producing an MIS structure. This was suggested on the basis of the apparent disagreement of data obtained in this program and results obtained by investigators at Rensselaer Polytechnic Institute (Ref 16), in which virtually all Schottky-barriers formed on polycrystalline GaAs had been found to exhibit completely shorted I-V characteristics unless the grain boundaries had been selectively anodically passivated. On the other hand, Schottky barriers routinely formed on polycrystalline GaAs in this program usually had I-V characteristics that were reproducible and reasonably stable. That is, open-circuit voltages of 0.4-0.5V and conversion efficiencies of 2.0-2.5 percent were routinely achieved. It was further speculated that the time period that elapsed between growth of the film sample and fabrication of the Schottky barrier might also have resulted in the formation of a thin oxide, affecting the I-V characteristics of the devices. This was suspected on the basis of the fact that GaAs layers that were etched in HCℓ prior to the deposition of the Au Schottky barrier typically had much poorer I-V characteristics than those that were fabricated without the etching procedure.

To test these questions, a set of similar n/n^+ GaAs structures deposited on Carbone-Lorraine Grade 5890 graphite substrates was used for the experiments. The films were processed to make Au Schottky barriers in three groups, after exposure to the laboratory atmosphere for 1) 24 hrs (the usual situation); 2) 14 days; and 3) 14 days, but with the surface etched in HCℓ just before deposition of the

Schottky barrier metal. A small (~50mV) decrease in the V_{OC} values was seen in the samples processed after the 14-day exposure, but this decrease was eliminated in those samples exposed for 14 days but HCℓ-etched first.

Many of these devices, however, did show shorted characteristics, although the best of the devices prepared after 14 days were as good as those on the samples prepared with exposure to the atmosphere for only one day. These results appeared to indicated that failure to process samples directly out of the reactor and allowing them to be exposed to the atmosphere for a day did not cause a major modification of the device characteristics. However, the question of whether or not a thin oxide was formed during the 24 hours was not answered. It is quite possible that such an oxide was, in fact, formed and that the results that were achieved routinely for these polycrystalline solar cells were actually enhanced by the presence of this oxide. Further study of this problem would be required to establish this fact with reasonable certainty.

2.3.3 Investigations of ITO-GaAs Heterostructures

On the strength of the possibility that indium-tin oxide (ITO) layers might be found to have considerable potential value in the GaAs solar cell materials system, either as one component of a heterojunction device (ITO/GaAs) or as a transparent ohmic contact on GaAs devices having the active barrier formed by some other process, a preliminary examination of the polycrystalline ITO-GaAs configuration was undertaken.

Deposited ITO layers were prepared by an rf sputtering process previously developed at Rockwell for use in producing transparent ITO contacts on Si CCD imagers. The polycrystalline GaAs film sample was not heated during the ITO deposition except for the normal slight heating that accompanied the rf sputtering deposition process, but this still allowed the sample to remain near room temperature. The extent of possible surface damage to the GaAs as a result of the deposition process was not known, however.

Unfortunately, the deposition process used in these initial experiments produced ITO with very high resistivity as deposited; annealing at 500°C in air for 1-5 min was required to reduce the resistivity to ~0.05 ohm-cm. Samples of ITO/nGaAs/n^+GaAs and ITO/pGaAs/p^+GaAs were prepared for evaluation of the ITO/GaAs heterojunction, and several more samples were prepared for examination of ITO as a possible ohmic contact. It was found for the latter samples that ITO contacts on both n^+ and p^+GaAs layers exhibited very high forward voltages, as seen in the I-V characteristics, indicative of a high contact resistance between the ITO and the GaAs in both instances.

It thus appeared that ITO layers deposited by the existing process (developed for another application) would not be satisfactory for achieving ohmic contact to the polycrystalline GaAs films. Modifications in the deposition process were considered for the requirements of this program, and the possibility of collaborating with other laboratories producing ITO by processes more compatible with the GaAs films was also considered. However, these alternatives were not considered to be of sufficiently

high priority compared with other program activities during the period covered by this report, and so were not pursued further.

2.4 TASK 4. DEVELOPMENT OF PHOTOVOLTAIC DEVICE DESIGNS AND FABRICATION TECHNIQUES

This task involved develpment of solar cell designs and fabrication techniques for the preparation of thin-film GaAs photovoltaic devices, and evaluation of the electrical and optical performance of any cells so fabricated. Further development of appropriate contact materials and procedures for applying them to polycrystalline device structures, including the investigation of indium-tin oxide (ITO) films as transparent ohmic contacts, was part of this task. Also included was investigation of suitable antireflection (AR) coatings for polycrystalline GaAs cells; initial attention was given to TiO_2 layers deposited by chemical pyrolysis.

Since the emphasis of the second-year program was on studying the properties of polycrystalline GaAs films and understanding the factors controlling those properties there was relatively little effort expended in this task. Most of the activity was devoted to examination of contact problems and to development of a process for deposition of TiO_2 AR coatings, as described in the following sections.

Periodically throughout the period covered by this report, however, various solar cell structures were fabricated, including both large-area single-crystal window-type cell structures on GaAs substrates and smaller-area polycrystalline cells (either junction-type or Schottky-barrier-type) on low-cost substrates. Among the variety of multilayer cell structures prepared by MO-CVD during this period were 1) large-area ($\sim$5 cm^2) single-crystal GaAlAs/GaAs thin-window ($\sim$400Å) structures, with a range of thicknesses for the p-type GaAs region, grown on single-crystal GaAs substrates; 2) five-layer large-area ($\sim$4 cm^2) single-crystal double-heterostructure cells with the configuration pGaAlAs/pGaAs/nGaAs/nGaAlAs/nGaAs, grown epitaxially on a single-crystal n-type GaAs substrate, with the central nGaAs layer undoped ($n < 1 \times 10^{15}$ cm^{-3}) so that it would be almost fully depleted and grown with either of two different thicknesses, and GaAlAs window layers with several different thicknesses; 3) large-area n^+/p shallow-junction GaAs homojunction cell structures on single-crystal GaAs substrates; and 4) three-layer polycrystalline GaAlAs/GaAs window-type cell structures grown on bulk Mo substrates and on sputtered Mo films on Corning Code 0317 glass substrates.

However, in none of the first three structures was the performance of the window-type GaAlAs/GaAs cells made by MO-CVD during the first year of the contract (Ref 1) exceeded, due in part to contact limitations. In the case of the polycrystalline cell structures the previously described leaky junction characteristics were the principal limiting factor, with the results discussed in earlier sections.

2.4.1 Investigation of Various Electrical Contact Problems

Some attention was given early in the second year to several possible alternative contact systems to those used previously in the program. The contact

metalization typically used for both single-crystal and polycrystalline solar cells had consisted of Au/Zn/Au for p-type layers and Au-Ge for n-type layers. Both of these contact materials required sintering in the temperature range 400-500°C. However, in several instances when Au/Zn/Au was applied as the contact to p-type GaAs in large-area (~4 cm^2) single-crystal cell structures it was found that when the deposited multilayer was heated to ~500°C to produce ohmic contact properties severe balling of the metal occured. A eutectic point had evidently been reached at which alloying took place. This resulted in high contact resistance and excessive junction leakage. Furthermore, some concern had arisen from time to time because of occasional difficulties encountered in the lift-off processing used to define the multifingered top contact patterns on single-crystal solar cell structures. This type of processing was considered less than optimum for polycrystalline p-n junctions as well because of the possibility of diffusion of Zn or Ge along grain boundaries.

Consequently, examination of various possibilities for non-sintered ohmic contacts was begun, especially for use with p-type material. However, each of the alternatives that was considered for p-type GaAs required a heavily doped "cap layer." These alternatives included (1) ITO, (2) thin Au, (3) Cr/Au, (4) Pd/Ag, (5) Ag/Mn, 6) Ti/Pt/Au, and (6) Al. Factors such as ultimate cost and preferred deposition techniques were weighed in comparing the various possibilities. Experimental verification of acceptably low contact resistance was required for selecting the best combination of material and method of application.

As was indicated in Section 2.3.3 a preliminary evaluation of ITO as a transparent contact material for polycrystalline GaAs was undertaken, but all evidence pointed toward a high resistance at the ITO-GaAs interface.

Vacuum-deposited contacts of Pd and of Ag/Mn were prepared on large-area single-crystal thin-film solar cell structures. The Pd was found to produce good ohmic contact to p-type GaAs without alloying, but it was found to be difficult to process into a grid configuration by the lift-off process because of very poor adherence to the GaAs.

The Ag/Mn contact to the p-type GaAs, however, was very satisfactory. A bottom layer of Mn ~100Å thick and a top layer of Ag ~2000Å thick were deposited in sequence, and the composite was annealed in H_2 at ~400°C. Following such heat treatment a low-resistance contact with good adherence resulted. The lift-off process for grid definition with this metallization was also successful. As a result, Ag/Mn was used for the p-type GaAs contact in all subsequent cell structures fabricated in this program. It was found, however, that Ag/Mn used alone tarnished slowly. To avoid such tarnishing a thin layer (~1000Å) of Cr-Au was deposited over the Ag/Mn contact after the alloying process. This required a second contact mask alignment procedure and a second lift-off step in the processing. However, the ohmic contacts so formed were exceedingly good in that they had low resistance, showed long-term stability, and readily survived the lift-off procedure.

2.4.2 Development of TiO_2 Deposition Apparatus and Procedure for Preparation of AR Coatings

Early in the second year attention was given to the assembly and performance verification of a system for depositing layers of TiO_2 by means of low-temperature pyrolysis of titanium isopropoxide, for use as AR coatings on GaAs solar cells. The system that was prepared was based on a design described by Hovel (Ref 17).

The deposition apparatus was constructed entirely of pyrex and used teflon-plug pyrex stopcocks. Joints were clamped pyrex greaseless ball-and-socket joints with elastomer O-rings. The hot stage supporting the sample to be coated was simply the plate of a laboratory-type electric hot plate, with a plated Au-over-Ni Cu block on it for temperature uniformity. Temperature was indicated by a thermocouple embedded in the Cu block. The sample to be coated was placed on the Cu block directly above the location of the embedded thermocouple bead. The titanium isopropoxide was contained in a pyrex bubbler, and a similar bubbler contained distilled H_2O for use if the H_2O vapor content of the laboratory air was found insufficient. Argon gas was directed through both bubblers to carry the reactants into the reaction chamber and to the region of the heated substrate.

The reaction chamber initially was simply a large inverted pyrex flask with sidearm tubes for introducing the gaseous reactants. However, the films deposited with this apparatus were quite nonuniform. Consequently, a reaction chamber incorporating a swivel tube fitting through a ground ball-and-socket joint centrally located in its top was fabricated. The swivel tube was connected to the source bubbler by means of a flexible stainless steel tube. The configuration of this modified apparatus is shown in the simplified schematic diagram in Figure 34.

Films of TiO_2 were deposited by moving the swivel tube manually in a random motion so that its exit aperture described a back-and-forth "painting" pattern above the substrate surface until a film of the desired uniformity and appropriate color was achieved. Reasonable uniformity of TiO_2 film thickness (± 10 percent) was achieved by this technique on 2 in. diameter Si wafers used as test substrates.

The thicknesses of the films deposited in this simple apparatus were measured, along with the indices of refraction, by ellipsometry. This procedure was followed for a variety of film deposition temperatures under various reactant flow conditions which had been found to allow control of film thickness and thickness uniformity.

One of the main advantages of this simple low-temperature process was that it permitted the growth of films with a wide range of index of refraction. This made it possible to prepare single-layer AR coatings for semiconductor devices, which require an AR coating index of ~ 1.8, or for metal-semiconductor devices, which require a coating index of ~ 2.4 (Ref 18).

The variation of index of refraction with deposition temperature achieved for films prepared in this apparatus is shown in Figure 35. The index is seen to increase from ~ 1.95 for deposition at $\sim 50°C$ to ~ 2.45 for deposition at $\sim 275°C$.

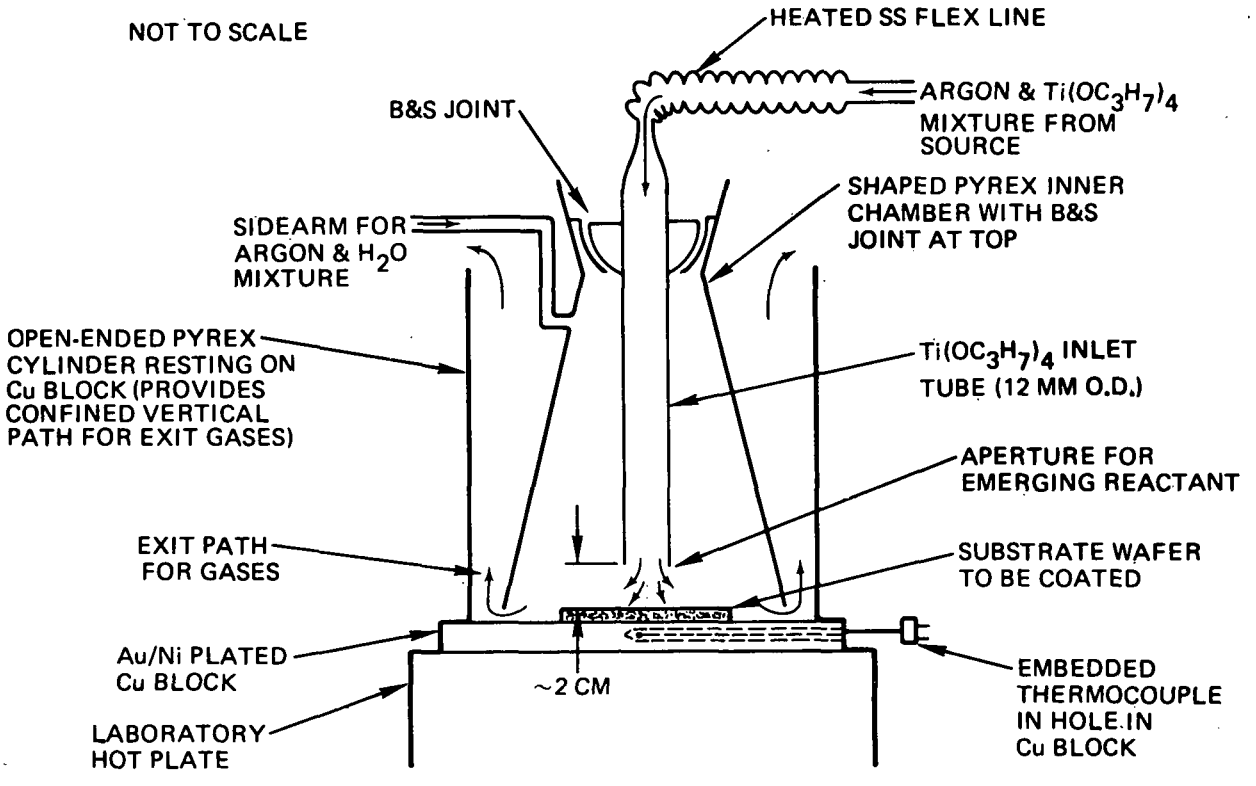

Figure 34. Simplified Schematic Diagram of Apparatus for Producing AR Coatings of TiO_2 by Pyrolysis of Titanium Isopropoxide at Temperatures of 50-300°C

For higher deposition temperatures the index remains approximately constant and then appears to decrease slightly as the temperature is further increased. Spontaneous gas-phase nucleation and resulting non-uniform films were probably produced by this process at temperatures above ~275°C. This system appeared to allow the formation of layers with the necessary range of index values.

The requirements for AR coatings are such that good control of film thickness is necessary. The thckness control method used for these TiO_2 layers was simply visual observation of the color of the depositing film as it developed. A single-layer AR coating on Si should have an index of refraction $n_{AR} \approx \sqrt{n_{Si}} \approx 1.9$ and a thickness $t_{AR} = \lambda_{min}/4n_{AR}$, where λ_{min} is the wavelength where the reflectivity minimum is desired.

TiO_2 layers were deposited in this apparatus at 70°C to produce an index of 1.95 and allowed to grow to a thickness for which a dark blue color was achieved. Figure 36 shows the relative reflectance as a function of wavelength for such a film found to be 856Å thick. The reflectance of the TiO_2-coated Si wafer was measured relative to the reflectance of an uncoated Si wafer, and an approximate absolute reflectivity scale - assuming a 30 percent reflectivity for Si - is indicated on the

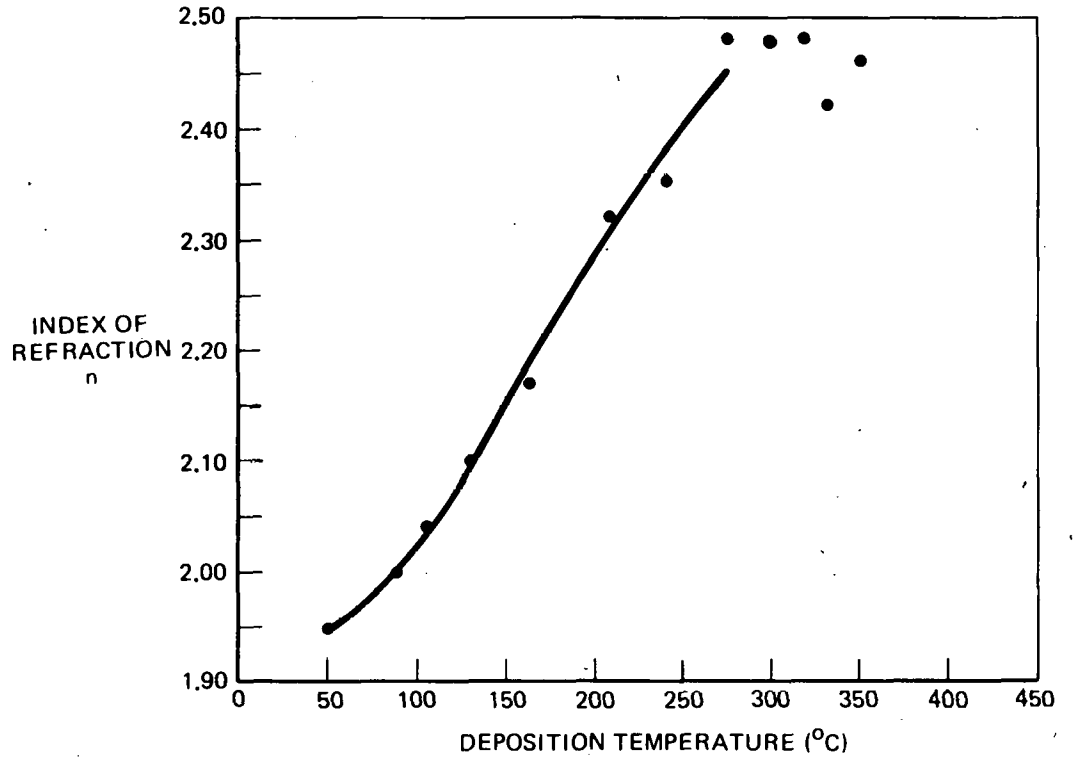

Figure 35. Index of Refraction of TiO_2 Layers as Function of Pyrolysis Deposition Temperature

right vertical axis in the figure. The minimum reflectivity is of the order of 0.15 percent, indicating a film of high optical quality and a good interface. Data for a thinner film (667Å) are also shown, and the appropriate shift to shorter wavelengths occurs. These results showed that the system was, in fact, capable of producing the AR coatings that would be required for solar cells prepared in this program.

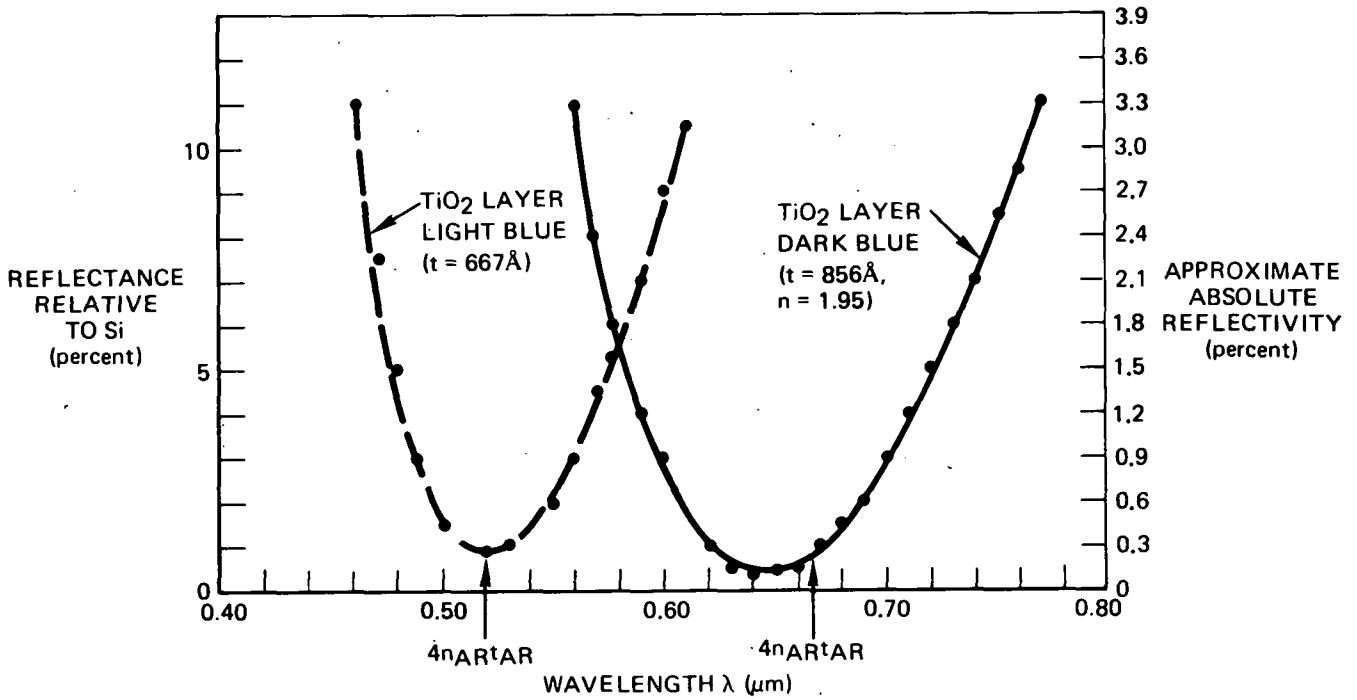

Figure 36. Relative Spectral Reflectance and Estimated Absolute Spectral Reflectivity for TiO_2 Layers Deposited on Si Substrates by Pyrolysis of Titanium Isopropoxide. (Calculated wavelengths for minimum reflectivity shown by arrows along horizontal axis.)

2.5 TASK 5. ANALYSIS AND PROJECTION OF CELL MATERIAL REQUIREMENTS AND FABRICATION COSTS

The purpose of this task was to extend the earlier (Ref 1) preliminary analysis and projection of cell costs, material quality, and material quantity requirements associated with scaled-up production of $5x10^4$ Mwe (peak) solar array generating capacity per year (the DoE program goal for the year 2000) using the MO-CVD process.

The planned work involved analysis of fabrication costs for complete thin-film GaAℓAs/GaAs solar cells made by the MO-CVD process on a laboratory scale, as well as updated projections of future materials requirements for fabricating large quantities of cells of the selected design by the MO-CVD process on certain low-cost substrates.

A detailed analysis was made of the materials and manpower required in the step-by-step procedures used in the laboratory for depositing the required composite film structure and applying the necessary contact structures. This analysis was then used to develop estimates of present costs (in 1978 dollars) for fabricating the cells in the laboratory, using the research-type MO-CVD reactor system employed in this program and the associated laboratory procedures. The results are given in the following sections.

2.5.1 GaAs Solar Cell Design Used in Analysis

The experimental GaAs thin-film solar cell design that was used as the basis for the analysis was the conventional window-type GaAℓAs/GaAs p-n junction configuration deposited by the MO-CVD process on a non-conducting substrate, so that contact access to the n-type base region adjoining the substrate must be achieved by etching through the two upper (p-type) layers. The design was thus basically that of conceptual Design No. 1 of Figure 2-35a of Reference 1, reproduced here in Figure 37a, which shows the cell design in generalized form. This was one of the two conceptual designs set forth early in the program for use in preliminary cost estimates and as exemplary design concepts for the experimental studies that ensued. The second conceptual design (Figure 2-35b, Reference 1) involved an inverted window-type thin-film cell structure on a transparent substrate such as glass, with illumination through the substrate. This configuration was not considered in the analysis discussed here.

The thicknesses of the various layers of the completed cell structure are given in Figure 37b, which shows a cross-section view of the cell to indicate the way in which the two active regions would be contacted. The effective area of the cell is that of a large comb-like mesa, with two sets of interdigitated contacts. No antireflection coating was included in the design used for this analysis.

Since obtaining detailed estimates of the materials and labor costs involved in fabricating a GaAs thin-film solar cell using the MO-CVD process in the laboratory was the primary objective of this exercise, the actual operating efficiency of the resulting cell was not of major concern at the time. Obviously, the actual power conversion efficiency of the cell would be a parameter of first-order importance in any final appraisal of the film growth and cell fabrication techniques under consideration.

2.5.2 Costs Involved in MO-CVD Growth of Multilayer Cell Structure in Laboratory-type Apparatus

A typical MO-CVD film-growth experiment in a laboratory-type reactor system such as those used for the work of this contract (shown schematically in Figure 2-4 and photographically in Figure 2-5 of Reference 1) consisted of eight main steps or procedures: (1) substrate preparation; (2) reactor chamber loading; (3) reactor pump-down and pre-deposition flush; (4) substrate heating and equilibration; (5) deposition of layer(s); (6) sample cooling and reactor shutdown; (7) sample removal; and (8) reactor system and susceptor cleaning.

Each of these eight procedures was carefully analyzed for the directly consumed materials of all types and the required expenditure of manpower for preparation of the experimental multilayer cell structure shown in Figure 37 (exclusive of etching the large mesa and applying the contacts). Specifically, an n-type Se-doped GaAs layer ~5 μm thick was grown on a substrate of Corning Code 0317 glass 15 mils (375 μm) thick, and on that were grown in succession a p-type Zn-doped GaAs layer 1.5 μm thick and a p-type Zn-doped GaAℓAs window layer 500Å thick.

The susceptor diameter was 2 in. (5 cm), so the effective area of the susceptor (which also served as the sample platform) was ~20 cm^2. In this program typically

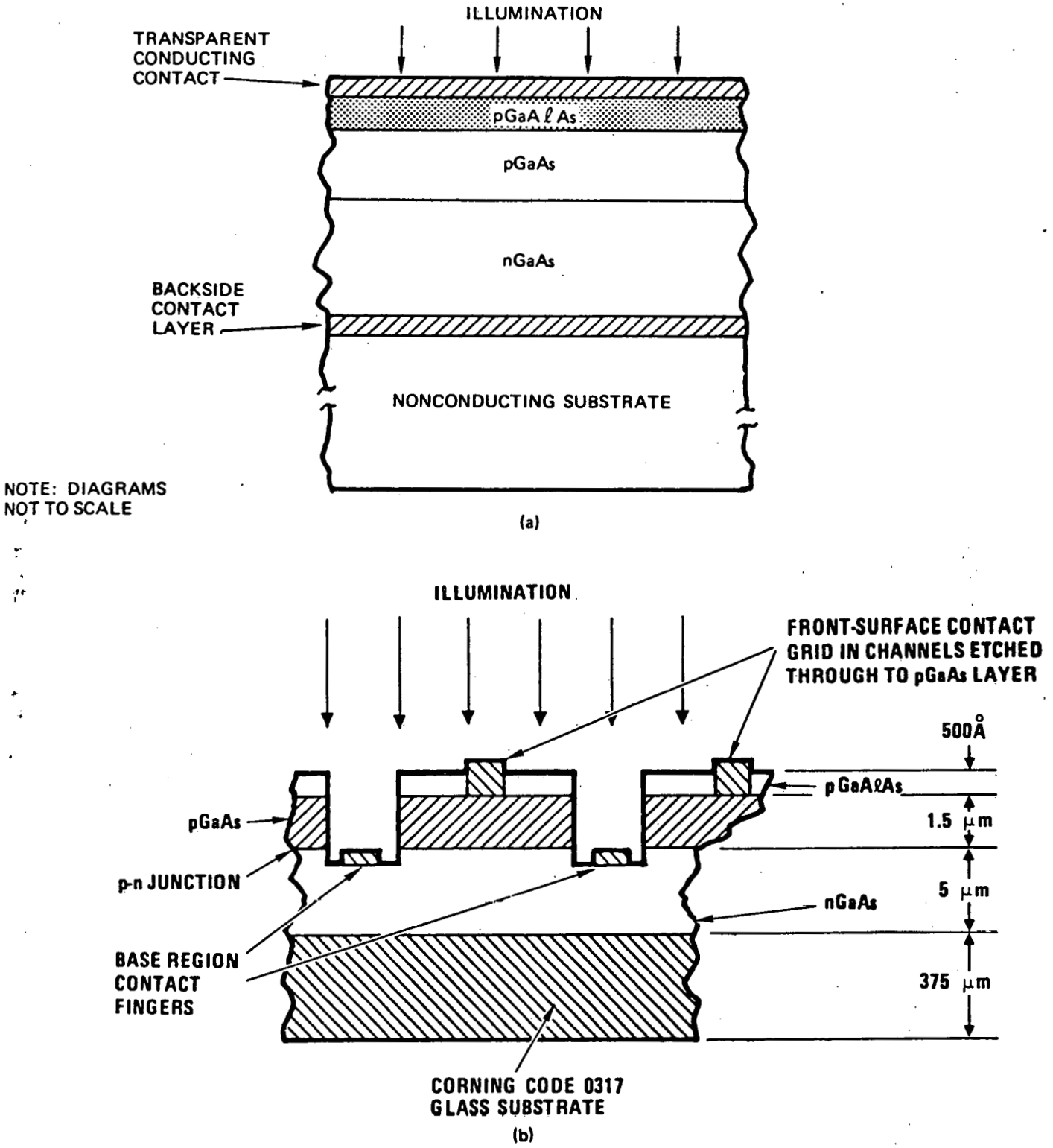

Figure 37. Thin-film GaAℓAs/GaAs Window-type Heteroface Solar Cell Structure Used as Basis for Analysis of Costs to Fabricate on Laboratory Scale by MO-CVD Process. a) Generalized Configuration; b) Cross-section View, Showing Layer Thicknesses and Method of Contacting.

only one or two substrates were used in a given deposition experiment, depending upon the particular purpose of the experiment. Experimental cell structures of the type involved in this analysis had typical lateral dimensions of 2x2 cm (area 4 cm^2), but because of the exceptionally good uniformity of film growth in the GaAs materials system in these MO-CVD reactors it is possible to utilize essentially all of the available susceptor area for substrate(s). Thus, in this cost analysis a total usable cell area of 20 cm^2 was assumed.

Table 3 lists the eight main steps in the growth of the required multilayer structure by MO-CVD and shows the costs of the various materials consumed in each of the eight steps. Although the analysis was made in terms of every identifiable material used in the overall procedure, only a coarse breakdown into material type is given for each step except for the case of the reactants required for film growth, where the specific materials are listed separately.

The costs of materials as given in Table 3 were determined on the basis of 1978 prices for the highest purity and generally highest quality materials available for research use in the laboratory, in most cases purchased in limited quantities and therefore generally quite expensive. It should be understood that the costs shown do not represent a projection of costs for a production operation nor even for moderately large-quantity preparation in the laboratory; they represent actual costs for preparation of a multilayer cell structure in a single deposition run in the laboratory at the time the analysis was made.

Not included explicitly as consumed items in this tabulation of costs are the electrical energy required by apparatus used in the eight steps of the growth process and the other miscellaneous consumed utilities (water, gas, lighting, air conditioning, etc) that constitute significant real cost items. However, such items along with other support expenses (miscellaneous supplies and services, management and supervision, building maintenance, etc) were taken into account in the overhead and the "general and administrative" (G&A) factors that were used in obtaining the bottom-line costs that are also shown in the table. A representative G&A rate of 20 percent (i.e., a G&A factor of 1.20) was used in adjusting the base material and labor costs developed in this analysis. The only item that would be considered to be part of an eventual "market price" that was omitted from the tabulated data is a profit or fee, but it was considered inappropriate to attach such an item to a preliminary estimate of costs associated with exploratory device fabrication carried out under premium-cost conditions.

The expended labor for each of the eight procedures is also given in Table 3. It should again be emphasized that the exploratory nature of this work normally required relatively close attention of laboratory personnel in most stages of the processing. Operations that would be unattended or only intermittently checked in a production environment were generally monitored almost constantly in these laboratory procedures. A representative indirect labor or overhead rate of 200 percent was used in this analysis.

A capital equipment amortization cost was added for the MO-CVD reactor alone. On the basis of an approximate 1978 market value of $60,000 for the laboratory-type reactor system used for this work, and assuming a five-year straight-line depreciation, an amortization rate of $48 per day of use was applied (5-day week, 50-week year). Since three runs were typically made per eight-hour day in these research

Table 3. Costs of Materials Consumed and Time and Costs* of Labor Required for MO-CVD Growth of 20 cm^2 Multilayer Solar Cell Structure Shown in Figure 37. (Work done by research laboratory personnel using research-type reactor system)

Procedure	Cost of Materials Directly Consumed ($)†										Labor Required (min/hr)	Labor Cost ($)†	Total Cost ($)†
	Substrate (Note 1)	Solvents (Note 2)	Acids (Note 3)	Carrier Gas (H_2)	TMG	TMAℓ	AsH_3	Dopants (Note 4)	Misc. (Note 5)	Total			
1. Substrate preparation	2.50	10.00	11.00	7.22	–	–	–	–	0.03	30.75	37.0/0.62	21.39	52.14
2. Reactor chamber loading	–	–	–	0.49	–	–	–	–	–	0.49	2.5/0.042	1.45	1.94
3. Reactor pumpdown and predeposition flush	–	–	–	10.53	–	–	–	–	–	10.53	47.0/0.78	26.91	37.44
4. Substrate heating and equilibration	–	–	–	3.20	–	–	5.83	0.0048	–	9.03	11.0/0.18	6.21	15.24
5. Deposition of layers	–	–	–	9.09	2.94	0.02	18.01	0.03	–	30.09	31.0/0.52	17.94	48.03
6. Sample cooling and reactor shutdown	–	–	–	7.31	–	–	0.58	–	–	7.89	32.0/0.53	18.28	26.17
7. Sample removal	–	–	–	0.25	–	–	–	–	–	0.25	1.5/0.025	0.86	1.11
8. Reactor system and susceptor cleaning	–	17.00	13.70	3.22	–	–	–	–	0.02	33.94	16.5/0.28	9.66	43.60
TOTALS (without G&A)	2.50	27.00	24.70	41.31	2.94	0.02	24.42	0.03	0.05	122.97**	178.5/2.98	102.70**	225.67**

*Labor costs are determined by using $11.50/hr. base rate for direct labor and 200 percent overhead (indirect labor) rate, or an equivalent total labor rate of $34.50/hr. See text.

†1978 dollars, without general and administrative (G&A) factor (see text). To obtain "bottom line" costs the tabulated amounts must be multiplied by the 1.20 G&A factor adopted for this analysis.

**Total adjusted cost = ($122.97 + $102.70) x (G&A factor) = $225.67 x 1.20 = $270.80. Capital cost of MO-CVD reactor system of $60,000 amortized (straight line) over 5-year period adds $48 per day (5-day week, 50-week year) or $16 per run (3 runs per 8-hr day) to total cost before G&A, or $19.20 per run for bottom-line cost. Thus, total cost per run = $270.80 + $19.20 = $290.

Notes:
1. Cost used for glass substrate is more than order of magnitude larger than expected actual cost for as-received material, which was obtained from Corning Glass Works for this study at no charge.
2. Solvents consist primarily of highest quality methanol, acetone, and 1-1-1 trichloroethane.
3. Acids consist primarily of highest purity HCℓ, H_2SO_4, HF, HNO_3; H_2O_2 is also included here.
4. Diethylzinc (DEZ) is the p-type dopant and H_2Se the n-type dopant.
5. Principal material involved here is high-resistivity deionized water.

reactors, it followed that a capital amortization cost of $16 per run was applicable. No other capital costs were included in this analysis.

It should be noted that the G&A and the overhead rates used in these estimates did not necessarily reflect the values used for these parameters at Rockwell for the period covered by this report (or at any other time). However, the net result of this simplified approach was a set of final costs that closely duplicated the actual costs experienced for the work described.

2.5.3 Costs Associated with Fabrication of Solar Cell Contact Structures

Three main steps were involved in formation of the ohmic contacts on the multilayer cell structure prepared by MO-CVD and the procedures itemized in Table 3. These were (1) n-type (base region) contact formation; (2) p-type (front layer) contact formation; and (3) contact alloying.

Table 4 lists these three steps and the costs of the materials consumed directly in each, adjusted from actual consumption for the typical experimental cell size (2x2 cm) to a total assumed cell area of 20 cm^2, as indicated earlier. A relatively coarse breakdown into material type is again given for each step except in the case of the contact metals employed, where the specific materials are separately tabulated. The direct labor involved for each of the three main steps is also shown and the approximate labor cost for each is given, as in Table 3.

2.5.4 Discussion of Estimated Costs

It was not the intention of this analysis to examine the functional sensitivity of the total cost of fabricating these thin-film cells to specific cost variations in individual materials or procedures. However, several observations based on the results of the cost analysis given in Tables 3 and 4 can be made. These are as follows:

1. Even for the experimental cell fabrication process represented in this analysis the substrate does not dominate the materials costs for the deposition sequence (Table 3). Substrate costs as high as those of single-crystal GaAs wafers (~20 cm^2 area) could be involved and still be only about equal to that of the H_2 carrier gas consumed in the present laboratory-scale process.

2. Materials costs for the deposition sequence are dominated by those of the chemical solvents, acids, AsH_3, and especially the H_2 carrier gas, the latter accounting for ~1/3 of the total. Of the principal reactants, AsH_3 and H_2 together account for over half of the total deposition sequence materials costs, while TMG is responsible for only about 2 percent.

3. The AsH_3 cost is high because of the large amount used in this process (see Section 2.5.5), rather than the unit cost being particularly high. (The cost per gram of AsH_3 is only about 8 percent of that for TMG and for TMAℓ.)

Table 4. Costs of Materials Consumed and Time and Costs* of Labor Required for Preparing Ohmic Contacts on 20 cm^2 Multilayer Solar Cell Structure of Figure 37. (Work done by research laboratory personnel using laboratory-type processing equipment).

Procedure	Cost of Materials Directly Consumed ($)†									Labor Required (min/hr)	Labor Cost ($)†	Total Cost ($)†
	Solvents (Note 1)	Acids (Note 2)	Gases (Note 3)	Photoresists (Note 4)	Au-Ge Alloy	Au	Zn	Misc. (Note 5)	Total			
1. Formation of n-type (base region) contact	11.25	0.72	0.02	2.62	1.10	–	–	0.02	15.73	95/1.58	54.51	70.24
2. Formation of p-type (front layer) contact	5.62	–	0.01	1.31	–	0.58	0.01	0.01	7.54	56/0.93	32.08	39.62
3. Contact alloying (at elevated temperature)	–	–	0.99	–	–	–	–	–	0.99	21/0.35	12.08	13.07
TOTALS (without G&A)	16.87	0.72	1.02	3.93	1.10	0.58	0.01	0.03	24.26**	172/2.86	98.67**	122.93**

*Labor costs are determined by using $11.50/hr base rate for direct labor and 200 percent overhead (indirect labor) rate, or an equivalent total labor rate of $34.50/hr. See text.

†1978 dollars, without general and administrative (G&A) factor (see text). To obtain "bottom line" costs the tabulated amounts must be multiplied by the 1.20 G&A factor adopted for this analysis.

**Total adjusted cost = ($24.26 + $98.67) x (G&A factor) = $122.93 x 1.20 = $147.52. No capital costs were included for this processing sequence.

Notes: 1. Solvents consist primarily of highest quality acetone.
2. Acids consist primarily of highest purity H_2SO_4; H_2O_2 is also included here.
3. Gases consist primarily of highest purity H_2 and N_2.
4. Included here are both photoresist and developer.
5. Principal materials involved here are high-resistivity deionized water and liquid nitrogen (coolant for vacuum-system traps).

4. For the eight main steps in the deposition sequence (Table 3) materials costs account for ~54 percent of the total and labor costs for ~46 percent (excluding amortization of capital equipment).

5. Substrate preparation and reactor cleaning after deposition and sample removal (steps 1 and 8) together account for 30 percent of the total labor costs for the overall deposition process.

6. Labor costs for the actual multilayer-structure deposition (step 5, Table 3) represent only about 1/6 of the total for the entire deposition sequence (steps 1 through 8).

7. Constant monitoring by laboratory personnel is probably not absolutely essential for all periods of the eight main steps in Table 3, so the labor costs obtained in the analysis represent an upper limit that could be reduced.

8. Use of less-highly-trained personnel than those involved in this contract work, such as would be employed in a pilot line or production facility, would – if assigned to carry out the same eight procedures as shown in Table 3 – reduce the labor cost by only about 30 percent and thus the total cost for the deposition sequence of Table 3 by only about half of that percentage if the materials costs remained unchanged.

9. The total materials costs for the contact processing (Table 4) are dominated by the solvent costs, which account for ~70 percent of the total. Costs of photoresist and developer are next, amounting to ~16 percent of the total.

10. The labor invested in applying contacts is very nearly as extensive as that required for the multilayer-structure deposition sequence. That is, the contact processing is labor-intensive, with ~80 percent of the total cost being attributed to labor costs. That this is the case is partly the result of the two separate vacuum deposition operations (n and p contacts) and separate alloying step, in addition to the usual sequence of mask processing.

11. Formation of the n-type (base region) contact dominates the time (i.e., labor) requirement for the contact processing of Table 4, accounting for ~55 percent of the labor costs for that sequence. The need for etching through the p-type GaAlAs window layer and p-type GaAs front layer to form the large comb-like mesa and expose the base region for contact access contributes heavily to this cost.

12. The use of less-highly-trained labor for all steps of the contact processing sequence could reduce the corresponding labor cost by about 30 percent, as in Item 8 above, but in this case the total cost of the contact processing would be reduced by about 24 percent because of its labor-intensive nature.

There are clear opportunities for cost reduction in each of the eight steps in the deposition sequence and each of the three main steps in the contacting sequence, both in materials consumed and in labor required. Further, by the obvious expedient

of increasing the cell area capacity per deposition run and the contact processing capacity of each step in that sequence the effective cost per unit area of cell could be greatly reduced. The first of these modifications is considered briefly in the next section.

2.5.5 Reactant Consumption Rates and MO-CVD Process Efficiency

The MO-CVD reactor chamber design used in this program (Figures 2-4 and 2-5 of Reference 1) involved a rotating susceptor ~5 cm in diameter horizontally disposed in the vertical cylindrical chamber of 8.0 cm inside diameter. The susceptor thus intercepted about 0.4 of the cross-sectional area of the interior of the reactor chamber normal to the cylindrical chamber axis – the region through which the reactant gas mixture flowed during the MO-CVD film growth process. Pyrolysis occurred at the hot surface of a substrate resting on the heated susceptor and/or on the hot susceptor surface itself in any regions not covered by substrate, resulting in deposition of GaAs or GaAℓAs, depending upon the composition of the reactant mixture.

Based on the assumption that the flow of the reactant mixture downward in the reactor chamber was laminar (i.e., non-turbulent) it followed that 40 percent of the reactants consumed impinged on the surface of the hot substrate (or uncovered susceptor) in the reactor design then in use, with the remaining 60 percent passing through the surrounding annulus and either undergoing spurious reaction downstream or exiting from the chamber into the exhaust line. The reactor system design did not provide for any recycling or salvage of the unused reactants or of the carrier gas.

From the basic pyrolysis reaction equations for formation of GaAs and GaAℓAs by the MO-CVD process as used in this work (Equations 2-1 and 2-2, Reference 1) the minimum quantities of the reactants TMG, TMAℓ, and AsH_3 required for deposition of the experimental cell structure shown in Figure 37 were calculated. For a cell area of 20 cm^2 (the full area of the susceptor surface) these quantities are as shown in the second column of Table 5. However, in terms of the actual reactant flow rates used in a single deposition experiment the corresponding quantities of reactants consumed were those given in the third column of the table.

Based on these two sets of numbers the absolute overall efficiency of utilization of each of the three reactants with respect to the theoretical minimum amount required for the 20 cm^2 multilayer structure of Figure 37 was found to be as shown in the fourth column. When allowance was made for the fact that only 40 percent of the reactant mixture was intercepted by the susceptor (i.e., by the 20 cm^2 substrate in this analysis) an indication of the actual efficiency of the pyrolysis reaction – that is, the efficiency of use of the intercepted reactant flow – was obtained relative to each reactant. The resulting values are shown in the fifth column of the table.

The data shown in Table 5 lead to the following conclusions:

1. The overall efficiency of utilization of the principal reactants could be increased by redesigning the substrate support (susceptor) to intercept a larger fraction of the flowing gas stream. However, as this faction increases toward unity greater turbulence of the flow in the vicinity of the susceptor surface can be expected, and thus less uniformity of film growth rate and perhaps other film properties is likely.

Table 5. Calculated and Actual Quantities of MO-CVD Reactants Required for Deposition of GaAℓAs/GaAs Solar Cell Structure* of Figure 37, and Efficiency of Utilization of Reactants in Growing the Structure.

Reactant	Theoretical Minimum Quantity Required for Pyrolysis Reaction**	Reactant Quantity Required Based on Flow Rates Used	Calculated Overall Efficiency of Use of Reactants†	Calculated Efficiency of Pyrolysis Reaction Relative to Each Reactant
TMG	5.50×10^{-2} g	0.294 g	0.19	0.47
TMAℓ	2.20×10^{-4} g	2.2×10^{-3} g	0.10	0.25
AsH_3	3.74×10^{-2} g	29.4 g	0.0013	0.0032

*Area 20 cm^2.

**Calculated from Equations 2-1 and 2-2 of Reference 1.

†Calculated from data in columns 2 and 3.

2. In terms of the intercepted reactants the reaction efficiency is reasonably good (nearly 50 percent) for TMG, the reactant about which there is the most concern relative to cost and general availability. Reaction efficiency with respect to TMAℓ, also quite expensive in the purity required for this work, is only about 25 percent. This raises questions as to the exact nature of the pyrolysis reactions when TMAℓ is present and as to the molecular state of the compound (i.e., monomer or polymer) when in the vapor phase at elevated temperatures.

3. A very large excess of AsH_3 was used in this process as it was applied to the GaAs materials system, to maintain the stoichiometric integrity and the surface quality of the deposited films. An AsH_3 mass flow many times larger than that theoretically required for the pyrolysis reaction to proceed to completion was employed. It is probable that this over-pressure could be reduced by a yet-undetermined amount and still retain the required film stability, thus reducing the AsH_3 consumption rate and the associated cost, which is appreciable (see Table 3).

The actual consumption of TMG in one series of more than 300 deposition experiments in the program was found to correspond to an average consumption of 0.235g per experiment. On the basis of careful estimates of the weighted average amount of GaAs and/or GaAℓAs deposited per run in this long series of experiments it was determined that the multilayer cell structure of Figure 37 corresponded to an adjusted average consumption of approximately 0.19g of TMG per deposition run. When this is compared with the theoretical minimum amount of TMG required by the pyrolysis reaction (in a reactor chamber of the size used here – 50 cm^2 cross-sectional area) for deposition of the multilayer structure under consideration an average efficiency of utilization of about 73 percent is obtained. The assumptions made in obtaining this figure are relatively tenuous, however, and it is believed that the lower efficiencies given in the previous paragraphs more accurately indicate the actual situation.

2.5.6 Projected Material Quantity Requirements for Production of Solar Arrays with 5 x 10^4 Mwe (peak) Power Generating Capacity

The DoE National Photovoltaic Conversion Program goal for the year 2000 is an annual solar array production capacity of 5 x 10^4 Mwe (peak) power generating capability with an array power conversion efficiency of 10 percent or better (AM1 illumination).

No attempt was made in this program to describe or specify a future production process that might be used in the year 2000 to prepare large-area arrays of GaAs solar cells by the MO-CVD method. There are still too many unknowns about the process and the ways in which it will best be adapted to large-volume production to permit a meaningful attempt at design of such a future manufacturing process at this time.

However, as a means of establishing extreme upper limits on some of the materials requirements for producing a cell array area equivalent to the annual power generating capacity goal defined above, a straightforward materials quantity projection was made for several of the materials represented in Tables 3 and 4. This involved simply multiplying the material quantity required for preparing the 20 cm^2 laboratory-model cell shown schematically in Figure 37 (and serving as the basis for the cost tabulations of Tables 3 and 4) by the area scale factor 2.5 x 10^{11}, to arrive at the material required to produce 5 x $10^8 m^2$ of such cells.

Clearly, such a procedure would have no validity whatever for some of the materials involved, since even modest expansion of the batch-type laboratory procedures used for preparing the experimental cells of this program could easily result in significantly larger cell areas being handled in essentially the same steps outlined in Tables 3 and 4 but with relatively little – if any – more of certain of the materials being required. Furthermore, design of a process for large-scale manufacturing purposes would entail continuous, rather than batch, processing as well as major modifications in the way some of the required materials would be used. It would also introduce various modifications, such as recycling and repurifying of reactants, that would improve the overall efficiency of utilization of many of the materials.

However, the quantity requirements projected for several of the materials by this area-scaling procedure serve to illustrate a number of important points relative to the thin-film GaAs cell and to the MO-CVD process for making it. These projections are given in Table 6 for the substrate, the TMG, and the Au and Zn used in contacting the cell.

The listed substrate requirement was obtained on a straightforward area basis and makes no allowance for waste (that is, less than 100 percent yield) or for operating the cells at concentration ratios greater than 1. The area given is approximately 4.7 times the total 1970 U.S. production of flat window glass (sheet, not rolled) and about 2.7 times the total 1975 U.S. production of plate and float glass (of all thicknesses). The estimated values of the two types of U.S. glass production for the years cited were $132 million 1970 dollars) and $388 million (1975 dollars), respectively. This emphasizes the magnitude of the production effort needed to fulfill the substrate requirement alone for the DoE annual cell array production goal for the year 2000.

Table 6. Projected Quantity Requirements for Selected Materials Used in Preparing GaAs Solar Cell Structure of Figure 37 by Laboratory-scale Process in Total Area of $5 \times 10^8 m^2$,

Material	Projected Quantity Required
Substrate (Corning Code 0317 glass sheet)	$\sim 5 \times 10^8 m^2$
TMG	$\sim 7.4 \times 10^7$ kg (74,000 mt)
Au (contacts*)	$\sim 4.9 \times 10^7$ kg (49,000 mt)
Zn (contacts)	$\sim 2.5 \times 10^6$ kg (2,500 mt)

*Includes both Au metal and Au-12% Ge alloy contacts.

The specific glass proposed for the GaAs cell structure is not now produced in large-volume lots, and is, in fact, manufactured only in limited quantities under controlled conditions. However, glass manufacturers have indicated that most glasses can be adapted to large-volume low-cost production if there is sufficient market demand to justify the specific initial process development and assure continuing sales to amortize the plant investment and generate long-term profits. In fact, glass industry production methods represent probably the best example of the type of manufacturing that must be applied to photovoltaic power conversion arrays to permit realization of the DoE production capacity and economic goals (Ref 1).

The TMG requirement given in Table 6 is based on the amount of TMG consumed in making the 20 cm^2 experimental cell of Figure 37 and Tables 3 and 4, and reflects the process efficiency in utilization of this reactant in the laboratory apparatus as discussed in Section 2.5.5. This quantity of TMG has a Ga content of $\sim 4.5 \times 10^7$ kg or about 45,000 mt. If the process were 100 percent efficient in its use of TMG instead of ~19 percent, as shown earlier (Section 2.5.5 and Table 5), then the quantity of TMG required for the pyrolysis reaction would be the minimum – approximately 14,000 mt of TMG, corresponding to ~8500 mt of Ga. This approximate amount of Ga also follows from the tabulated value for the theoretical minimum quantity of TMG required by the MO-CVD pyrolysis reaction for formation of a 20 cm^2 cell structure, as given in Table 5.

The current annual production of electronic-grade TMG in the United States is probably less than 20 kg, prepared in relatively small batches (500-1000g) by only two or three suppliers (Ref 19). There has been relatively little demand for this metalorganic compound until recent years, but since Rockwell's introduction of the MO-CVD process for growing GaAs films (Ref 6) the demand has been increasing slowly but steadily. Obviously, however, the quantity of TMG indicated in Table 6 will require immense expansion of present manufacturing capabilities – in fact, an entire new chemical manufacturing subindustry will have to be established.

Depending upon whether a process efficiency similar to that found in the laboratory-scale apparatus used in this program or one closer to the theoretical

maximum is assumed, the amount of Ga metal required to meet the year 2000 annual cell production goal of 5 x $10^8 m^2$ will thus range from ~45,000 mt down to ~8500 mt. As shown in the Annual Report for the first year of this contract (Ref 1) the projected annual production of Ga metal for the year 2000 is close to the bottom end of this range, depending upon the projection basis used and the portion of the world included. Table 7 shows several projected amounts for Ga production in that year, based on different methods of projection as discussed in that report.

Table 7. Projected Annual Production of Ga Metal for Year 2000 Based on Projected Bauxite Ore Production and Projected Aluminum Industry Growth*

Basis for Projection	Annual Amount of Ga (mt)		
		Produced	
	Potentially Available	Present** Recovery Technology	Improved† Recovery Technology
Projected Production of Bauxite Ore			
In U.S., Australia, Jamaica, Guinea, Surinam, Guyana, France, Brazil	10,550	4220	8440
World Total	13,440	5380	10,800
Projected Growth of Aluminum Industry††			
World Total	17,090	6840	13,700

*Taken from Table 2-9, Reference 1

**Present recovery technology could extract ~40 percent of the Ga from bauxite economically

†Increase to ~80 percent economical recovery is considered possible with adequate development and capital investment (Ref 20)

††Projected 6 percent annual growth in aluminum production

It is seen that present recovery technology, which could extract about 40 percent of the Ga metal available in bauxite ore economically (Ref 20), is projected to produce 4220 mt of Ga in the United States and seven other leading bauxite-producing countries (Australia, Jamaica, Guinea, Surinam, Guyana, France, and Brazil) and 5380 mt total throughout the world in the year 2000, based on bauxite ore production projections. On the basis of a 6 percent annual growth in aluminum production (a conservative estimate, in view of the aluminum industry's growth history) and the 1974 worldwide production of bauxite ore, a somewhat higher projected value of 6840 mt of Ga is obtained.

If, however, an improvement in recovery technology to ~80 percent Ga yield were to be achieved – a result considered feasible given sufficient development and capital investment (Ref 20) – then the annual Ga production figures would increase to 8440 mt for the eight countries and ~10,800 mt for the entire world based on the bauxite ore projections, and ~13,700 mt for the world based on the aluminum industry expansion projection.

It appears that achievement of the year 2000 cell array annual production goal of GaAs cells made by the MO-CVD process as investigated and developed in this program will require development of an improved Ga recovery technology relative to that now in use. If an improvement to ~80 percent recovery were realized then nearly identically the amount of Ga required in the theoretical minimum quantity of TMG necessary to produce the $5 \times 10^8 m^2$ of GaAs cells would be produced in the United States and the seven other countries mentioned above, and up to 1.6 times that amount worldwide.

If, however, the achieved MO-CVD process efficiency for TMG use is similar to the 47 percent realized in the laboratory-scale work when allowance is made for geometrical inefficiencies of design (see column 5 of Table 5) then the total amount of TMG required will have a Ga metal content of ~18,200 mt. This is about 1-1/3 times the projected worldwide annual production for the year 2000 even with the 80 percent recovery technology and using the aluminum industry expansion projection (Table 7). It thus appears essential for at least three developments to occur if the DoE annual cell production goal for the year 2000 is to be achieved using the MO-CVD process and if the resulting cells do not exceed 10 percent in AM1 efficiency:

1. Fugure Ga metal production must be expanded beyond the levels projected by current estimates, as discussed in Reference 1.

2. Ga metal recovery technology for bauxite must be improved to increase the yield from its present value (~40 percent maximum) to at least 80 percent.

3. Efficiency of the MO-CVD process must be maximized with respect to TMG utilization, with at least 50 percent efficiency indicated.

The optimum situation would see development work in all three areas beginning as soon as possible. Any continuation of the work of this contract would naturally include considerable attention to the third item. Of course, any improvement in the basic polycrystalline cell efficiency of 10 percent (AM1) used in the calculations of the materials requirements would proportionately relax the urgency for the above developments, and any continued work on the GaAs cell should have this as a primary goal.

2.5.7 Future Materials and Fabrication Costs

No attempt was made during the conduct of this program to predict either materials costs or labor costs for the years 1985 and 2000. Such projections would be only speculative at this time and would not have a constructive effect on the technical evaluations that constituted the primary activity of the contract program.

3. SUMMARY AND RECOMMENDATIONS

This section contains first a separate summary of the work of the final five months of the contract and then an overall summary of the entire 14-month second year. Finally, a brief outline of recommendations for continued work is given.

3.1 RESULTS IN FINAL FIVE MONTHS OF CONTRACT

The technical activities of the final five months of the contract were concentrated on 1) further studies of the effect of $HC\ell$ on the properties of polycrystalline GaAs thin films; 2) further studies of the use of graphite as a low-cost substrate for thin-film GaAs solar cell fabrication; 3) studies of the details of effects of grain boundaries on the properties of polycrystalline thin films; 4) examination of the properties of Schottky-barrier solar cells formed on polycrystalline thin films; 5) evaluation of the effects of modified growth procedures in producing higher quality p-n junctions in polycrystalline GaAs; 6) improvement in contacting procedures for single-crystal GaAs solar cells; and 7) analysis of fabrication costs for complete thin-film $GaA\ell As$/GaAs solar cells made by the MO-CVD process on a laboratory scale.

Perhaps the principal achievement during this period was development of the capability to fabricate GaAs solar cells of improved efficiency on graphite substrates using the MO-CVD process. In earlier work the efficiency of such cells was considerably less than 1 percent. However, by modifying the deposition procedures so that only ultra-clean graphite was used during the growth, it was found possible to increase the efficiency of the polycrystalline Schottky-barrier solar cells on Carbone-Lorraine Grade 5890 graphite to values comparable to what had been achieved on other polycrystalline substrates. This is a significant achievement because it now allows consideration of graphite as a substrate for use in these thin-film solar cells, and graphite is conductive and is amenable to high-temperature deposition and growth in the presence of $HC\ell$. It is expected that further work using graphite as a substrate for GaAs deposition by the MO-CVD process will result in larger grain sizes and higher-efficiency thin-film cells.

The initial phase of the study of the effects of the addition of $HC\ell$ during growth of polycrystalline films by MO-CVD was completed. The general conclusion reached from this work is that the addition of $HC\ell$ to the gas stream beneficially affects film morphology and average grain size. However, the nature of the chemical reactions that occur during the deposition is significantly altered by the presence of $HC\ell$, and there was some evidence suggesting the formation of addition compounds and other intermediate products which affect the growth kinetics. As a result, some of the benefits which accrue from the use of $HC\ell$ are offset by increased reactor complexity and more elaborate and tedious cleaning procedures. In addition, a considerable counter-doping problem was encountered using $HC\ell$ during the growth of thin films. Whether or not this can be overcome remains to be investigated. It is evident that additional investigation of the use of $HC\ell$ in the MO-CVD process for fabrication of GaAs thin-film solar cells is necessary.

A relatively complete model for the energy band structure of grain boundaries in thin-film polycrystalline GaAs was developed, based on analysis of the transport properties of the thin films. It leads to the conclusion that an extremely large density of interfacial states at the grain boundaries controls barrier height and the transport across the grains in this material. The density of these states appears to vary exponentially with energy from mid-gap toward the band edges for both n- and p-type materials, and in fact approaches the density of conduction-band states at the conduction-band edge. In many respects, the density of states is reminiscent of the density of states of amorphous materials, and leads to the speculation that the grain boundary regions in these thin films may be highly disordered and almost amorphous-like in behavior.

Procedures for the fabrication of Schottky-barrier solar cells, including the Au Schottky-barrier thickness and the need for processing within a short period after growth, were established. It was concluded that 75 to 100 Å of Au deposited during the first twenty-four hours after growth of the cell structure is sufficient to result in reproducible device characteristics.

It was demonstrated that the use of a modified MO-CVD growth procedure for the fabrication of p-i-n structures, in which the p layer was formed at significantly lower temperatures that the usual 700-725°C used for n and n^+ layers, produced p-i-n devices having considerably lower shunt resistance than those fabricated at a single temperature. This result, although not completely understood, may be attributable to suppression of impurity diffusion along grain boundaries.

The use of Mn-Ag contacts was determined to result in contacts of low series resistance to single-crystal GaAs solar cells. In addition, reproducible lift-off was achieved with this metallization. The major difficulty in the use of the metallization, however, is that it is necessary to overcoat the contact with a layer of Au after alloying to prevent tarnishing of the contact during exposure to the atmosphere.

Finally, an upper-limit projection of the materials requirements for achieving the DoE annual array production goal of 5×10^4 Mwe power generating capacity in the year 2000 by means of GaAs solar cells fabricated by the MO-CVD process was made. It was concluded that achievement of this goal with 10 percent efficiency cells made by the MO-CVD process will require 1) expansion of Ga metal production beyond the levels projected for the year 2000 by current estimates; 2) improvement in the technology for recovery of Ga metal from bauxite ore from the present 40 percent economic limit to at least 80 percent; and 3) achievement of at least 50 percent, and preferably higher, efficiency of the MO-CVD process with respect to TMG utilization.

3.2 SUMMARY OF SECOND-YEAR ACTIVITIES

On the basis of the first year's results, the contract program for the second year was planned to emphasize gaining an improved understanding of the properties and effects of grain boundaries in polycrystalline GaAs films. Also to be included were further substrate development and additional attention to junction formation techniques and experimental procedures which would yield larger grain sizes for equivalent Ga content. Continued development of solar cell fabrication technology, including contacts and AR coatings, was also included in the program plan.

Substrate evaluation for polycrystalline solar cells continued through the second year. Most of the emphasis of the program, however, centered on the use of Mo, Mo-coated glass, and graphite as substrate materials. The Mo/glass substrates were used most often for device work and consisted of a thin (2000Å) film of sputtered Mo on Corning Code 0317 glass, although other glasses were also investigated. Mo sheet was employed later in the year as the most suitable choice for use with HCℓ additions to the MO-CVD process owing to its greater resistance to undercut etching by the HCℓ. Other substrates, such as large-grained bulk polycrystalline GaAs, large-grained alumina (Vistal 5), and composite substrates consisting of CVD-grown Ge films on a variety of amorphous and polycrystalline substrates, were also evaluated to improve film characteristics or to grow special structures. In most cases these substrates were considered impractically expensive or offered no major advantage over others already emphasized. The use of Ge intermediate layers, however, appeared promising.

Graphite emerged during the second year as a promising substrate for thin-film solar cells, although the early efforts with this substrate were not encouraging. At first, no photovoltaic effect was observed in GaAs films grown on a variety of graphites, including Poco Grade DFP-3 and Carbone-Lorraine Grade 5890. Polishing the graphite to improve surface smoothness resulted in very poor GaAs film adherence, presumably due to the presence of a fine particulate residue on the graphite surface. A variety of cleaning and baking procedures were examined with the eventual result that a procedure was developed for producing high quality GaAs films on the Carbone-Lorraine 5890 graphite. This included using the substrate alone (i.e., without other graphites present) and with no additional cleaning steps except a high-temperature (~1000°C) bake in situ for 30 min. Schottky-barrier solar cells with efficiencies of ~3 percent (AM0, no AR coating) were routinely fabricated under these conditions. These results are comparable to the best obtained for thin-film polycrystalline cells fabricated on any other substrate and provide a new option for future work.

Studies to improve the quality of GaAs films by the introduction of an etching species into the growth environment during deposition were begun during the second year. Substantial improvements in the grain size of polycrystalline GaAs were obtained by the introduction of HCℓ gas into the reactant gas mixture during deposition of the film. Typically the average grain size increased and the overall uniformity of grain size improved when partial pressures of HCℓ comparable to the TMG partial pressure were used in the reactor. The optimum HCℓ partial pressure was found to depend critically upon the growth temperature, owing to the competing deposition and etching reactions that occur. The most notable increases in grain size were observed for films grown to a thickness of 20 μm or more, but substantial morphology changes were observed in films of all thicknesses down to 5-8 μm.

Several problems were found to exist with the use of HCℓ during growth that must be overcome before it can become a fully useful grain-size enhancement technique. First, a suitable substrate that is compatible with the presence of HCℓ must be found. Mo and Mo/glass substrates were used in the early experiments, but both were attacked by the HCℓ. This caused severe undercutting of the film during growth and subsequent film peeling unless the substrate was covered with a pinhole-free (~2 μm thick) film of GaAs before the introduction of HCℓ. Graphite appears to be suitable in this respect and must be further explored. A second problem, yet unsolved, is that of a higher net impurity level in films grown with HCℓ.

The carrier concentrations achieved were not low enough to permit the formation of low-leakage Schottky-barrier cells. Autodoping problems from the n^+ contact layer were also found more severe in the presence of $HC\ell$. Perhaps the most vexing problem experimentally was the formation of volatile reaction products in the exit portions of the reactor that can affect nucleation of films in subsequent growth runs. Formation of these compounds required that the exit portion of the reactor chamber be cleaned after every run. Finally, the competing etching and deposition reactions occurring with $HC\ell$ additions render the growth process strongly temperature dependent at the $HC\ell$ flow rates for which grain size enhancement occurs.

In an effort to learn more about the properties of the grain boundaries in MO-CVD polycrystalline films, detailed studies of the transport properties of polycrystalline GaAs films grown on substrates of Vistal 5 alumina and Corning Code 0317 glass were carried out. Initial emphasis was on p-type Zn-doped films in the 10^{16}-10^{19} cm^{-3} concentration range, although work was later carried out with similarly doped n-type films. The large-grained films on alumina exhibited resistivities nearly an order of magnitude lower than those of simultaneously grown small-grained films on glass for a given concentration of added dopant. Measurement of transport properties as a function of sample temperature in the range 77-450°K demonstrated that the presence of barriers to majority carrier flow at the grain boundaries in these films controls the carrier transport process. The height of these barriers (E_b) was shown experimentally to decrease with increasing impurity doping concentration according to the expression $E_b \propto \ell n\ (1/p)$, where p is the measured hole concentration, for films on both the large-grained polycrystalline and the amorphous substrates. These results were explained in terms of a model for polycrystalline GaAs films that assumes that the intergrain boundaries have a high density of neutral traps that capture majority carriers, produce a depletion region on both sides of the boundary, and thus result in the experimentally observed barrier of height E_b.

Effects similar to those found in p-type films were observed in the study of transport properties of n-type polycrystalline GaAs films; the properties are controlled by transport across grain boundaries, with the grain boundaries providing barriers to majority carrier flow and the barrier heights depending upon doping concentration (decreasing with increased doping). The barrier height dependence upon doping concentration was again found to be of the form $E_b \propto \ell n\ (1/N_D)$ instead of $E_b \propto (1\ N_D)$ as predicted by the model used to describe the observed properties. The discrepancy was explained in terms of an increasing density of trapped charges at the intergranular interface as the doping concentration if increased.

Additional consideration of the model used to describe majority carrier transport in polycrystalline GaAs led to the conclusion that the density $N_t(E)$ of majority-carrier traps in the grain boundary has an energy distribution that decreases exponentially from the band edge toward the center of the band gap, for both p- and n-type films. This results in a band model with a high density of localized states "tailing in" from the conduction band and the valence band, overlapping at mid-gap.

Study of the uniformity of the transport properties of large- and small-grained polycrystalline GaAs films grown on Vistal 5 alumina and Corning Code 0317 glass, respectively, showed that in both cases film resistivities increased as film

thickness decreased. Also, intergrain barrier heights were found to be relatively independent of film thickness (i.e., distance from the film substrate interface) for films grown on Vistal 5 alumina but to increase slightly as the thickness was decreased below 10 μm for films on 0317 glass until thicknesses ⩽6μm were reached, below which the barrier height appeared to remain unchanged. These effects were observed in both p-type and n-type doped films.

Preliminary investigation of the effects of annealing on the transport properties of both n-type and p-type (up to $\sim 10^{18}$ cm^{-3}) polycrystalline GaAs films grown ~10 μm thick on the alumina and the glass substrates was also undertaken. Annealing for 30 min and for 150 min periods in H_2 and in H_2 and AsH_3 mixtures at temperatures of 500, 600, and 700°C produced varied results. The p-type material was affected most, especially when an atmosphere of only H_2 gas was used, perhaps reflecting the importance of an AsH_3 environment when GaAs is heated to elevated temperatures. When H_2 and AsH_3 mixtures were used there was essentially no change in either electrical resistivity or barrier height after 30 min at any of the three temperatures, for either n-type or p-type films. After 150 min, however, both resistivity and barrier height decreased slightly for 500°C annealing and incraased slightly for 600 or 700°C annealing. Additional experiments are required to clarify the nature and possible mechanisms of these changes.

An extensive empirical study of the properties of deposited p-n junctions was carried out during this year. Both n/p and p/n structures were examined, although most of the effort was concentrated on the p/n structure owing to the possibility of obtaining higher conductivity in the p layers. A variety of doping concentrations, layer thicknesses, growth temperatures, and substrate configurations were systematically examined in an effort to produce high quality p-n junctions. However, low-leakage p-n junctions were not formed for any configuration studied. The major effect noted was that low-leakage devices are obtained in p-i-n structures where the i layer is an undoped layer with $n \approx 10^{15}$ cm^{-3}. Diagnostic studies of several configurations produced no corroborative evidence of Zn diffusion along grain boundaries being the cause of the high leakage seen in these devices. Angle-lapping and staining and selective layer removal were used to study this problem. In the latter case the n regions of p-n junctions were examined after removal of the p layers. Both point-contact probing of the n layers and Schottky-barrier device characteristics of the n layers showed no evidence for Zn diffusion along grain boundaries.

However, the growth of p-i-n structures with a modified two-step growth procedure did result in some improvement of device properties. The p layer was grown at much lower temperature than the rest of the structure (550-600°C vs 700-725°C). A possible result of this lower growth temperature is the reduction of Zn diffusion along grain boundaries. The device structures grown in this way showed considerably higher shunt resistance but still had forward voltages of 0.5-0.6V, instead of 0.9-1.0V as expected for high quality GaAs p-n junctions. The differences are not yet understood, but there is indication that the grain boundaries generated by the vapor-growth process on dissimilar substrate material may be considerably different from those produced during bulk solidification from the melt and propagated into a film during CVD growth. To verify this an attempt was also made to correlate the junction leakage in a given mesa diode formed in p/n and n/p device structures grown on bulk polycrystalline GaAs with the apparent number of grain boundaries intercepting the area of the mesa. However, no strong correlation could be established, even for mesas with up to 40 grain boundaries.

Schottky barriers were used routinely as an evaluation tool to screen substrates and to determine the effect of changing growth parameters. A study of optimum Au layer thickness was performed to ensure that maximum efficiencies were obtained with these devices. Structures of n/n^+ GaAs on Mo substrates were used in the study, and photoresponses of the completed devices to AM0 simulated illumination (no AR coatings) were used to evaluate the results. It was found that Au film thicknesses of 75-100Å, rather than the 50Å used previously, produced the best results.

The effects of atmospheric exposure of the GaAs surface prior to application of Au Schottky barriers were also investigated to determine if the apparently random variation in V_{OC} observed from sample to sample in Schottky-barrier cells might be associated with the presence of varying amounts of inadvertent native oxide on the GaAs. Similar GaAs structures grown on Carbone-Lorraine graphite substrates were processed into devices after exposure to the laboratory environment for 1) 24 hr (the usual occurrence), 2) 14 days, and 3) 14 days but with the surface etched in $HC\ell$ prior to the metal barrier deposition. A small (~50 mV) decrease in V_{OC} was observed after the 14-day exposure but this was "recovered" in those cells formed with the $HC\ell$ etch treatment. Actually, variations of this magnitude were typically seen as normal run-to-run random variations, so the results appeared inconclusive.

A laboratory-type deposition system capable of producing uniform TiO_2 layers by pyrolysis of titanium isopropoxide at temperatures in the range 50-350°C was assembled and used for exploratory layer deposition. Layers with index of refraction in the range from 1.9 to 2.4 were produced by control of (primarily) deposition temperature and appeared to be suitable for use on GaAs cell structures when required.

A detailed analysis was made of the materials and labor requirements for producing thin-film $GaA\ell As$/GaAs window-type solar cells by the MO-CVD process on a laboratory scale in research-type reactors. The resulting cost estimates were examined briefly with respect to areas of possible reduction in material and labor costs for this scale of operation. Estimates were also made of consumption rates of the three principal reactants (TMG, $TMA\ell$, and AsH_3) and of the apparent efficiency of the MO-CVD pyrolysis reaction as used in this program. It was determined that the process is nearly 50 percent efficient in terms of the consumption of TMG, the reactant of primary concern with respect to cost and availability. Projections of the upper limits on the materials requirements for achieving the DoE year-2000 annual array production goal of 5×10^4 Mwe power generating capacity by use of 10-percent-efficient polycrystalline GaAs cells made by the MO-CVD process showed that 1) the MO-CVD process efficiency must be maximized, 2) the Ga recovery process efficiency (using bauxite ore) must be increased to 80 percent or more, and 3) the future production of Ga metal must be expanded beyond those projections now being made based on current growth trends.

3.3 RECOMMENDATIONS FOR CONTINUED WORK

Several important problem areas and broad technical questions remain unsolved upon completion of the second contract year, although considerable progress was

made – as reviewed in this report. These unresolved issues, which should constitute the basis for continued work, are as follows:

1. It must be determined if there is some other substrate material than Mo (either as bulk sheet or as deposited film on glass) and graphite that might be more satisfactory for growth of GaAs polycrystalline solar cell structures by MO-CVD, or if these two materials should be accepted as the state-of-the-art standards and efforts be concentrated on optimizing film growth and cell processing on these two materials.

2. It must be established whether procedures such as addition of HCℓ vapor to the reactant mixture during film deposition or annealing of post-nucleation partial-coverage films by temperature excursions can be developed to the point where they will result in significant increases in average grain size in MO-CVD polycrystalline GaAs films grown on low-cost substrates without excessively complicating or damaging the overall process in other ways.

3. Sufficiently effective methods must be developed for reducing – or at least controlling – the adverse effects that grain boundaries in polycrystalline GaAs films have on the electrical properties of the films, either by means of impurity additions or special processing steps introduced during film deposition or by means of special treatment undertaken on the film after its growth is completed.

4. Film deposition parameters, doping impurities, post-deposition processing (such as surface anodization or impurity injection and diffusion), or other procedures that will allow the preparation of good p-n junction structures in polycrystalline GaAs films grown by MO-CVD must be established.

5. Contact materials and contact designs must be identified that will permit the fabrication of polycrystalline thin-film solar cells in MO-CVD GaAs with adequately low series resistance and sufficiently high fill factor to make possible the achievement of satisfactory photovoltaic performance.

6. Individual layer characteristics and multilayer cell configurations and order of growth that will lead to polycrystalline solar cells exhibiting the maximum photovoltaic performance obtainable within the constraints of polycrystalline materials grown on low-cost substrates must be established.

There were specific accomplishments in each of the above problem areas, but additional work is required to provide adequate data and understanding for subsequent technical and programmatic decisions that must be made about the materials and the processes involved and the way in which they will be further pursued in the National Photovoltaic Conversion Program.

Such continued work should include at least the following four main areas of investigation: 1) study of methods for influencing grain-growth mechanisms during MO-CVD film growth (control of properties of growth surface, variation of CVD parameters and growth procedures, control of chemical environment in deposition

chamber); 2) investigation of methods for controlling properties of grains and grain boundaries after film deposition (selective passivation by surface processing, doping and compensation by impurity introduction, structural modification by annealing and/or recrystallization); 3) characterization of polycrystalline films and device structures, with emphasis on grain boundary properties; and 4) investigation of barrier formation techniques, and fabrication and evaluation of solar cell structures (barrier formation and design, contact development, antireflection coating development, experimental cell fabrication and characterization).

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