C/ORNL95-0367

ORNL/M--6390

ornl

OAK RIDGE NATIONAL LABORATORY

LOCKHEED MARTIN

Final Report for
CRADA Number ORNL95-0367

MONOLITHIC CIRCUITS FOR BARIUM FLUORIDE DETECTORS USED IN NUCLEAR PHYSICS EXPERIMENTS

R. L. Varner
J. L. Blankenship
J. R. Beene
Oak Ridge National Laboratory

R. A. Todd
RIS Corp.

Date Published - February 1998

Prepared by the
Oak Ridge National Laboratory
Oak Ridge, Tennessee 37831
managed by
Lockheed Martin Energy Research Corp.
for the
U.S. Department of Energy
under contract DE-AC05-96OR22464

UNLIMITED DISTRIBUTION

MANAGED AND OPERATED BY
LOCKHEED MARTIN ENERGY RESEARCH CORPORATION
FOR THE UNITED STATES
DEPARTMENT OF ENERGY

ORNL-27 (3-96)

APPROVED FOR PUBLIC RELEASE

C/ORNL95-0367

CRADA Final Report
for
CRADA Number ORNL95-0367

MONOLITHIC CIRCUITS FOR BARIUM FLUORIDE DETECTORS USED IN NUCLEAR PHYSICS EXPERIMENTS

R. L. Varner, J. L. Blankenship, J. R. Beene
Oak Ridge National Laboratory

R. A. Todd
RIS Corp.

Prepared by the
Oak Ridge National Laboratory
Oak Ridge, Tennessee 37831
managed by
Lockheed Martin Energy Research Corporation
for the
U.S. Department of Energy
under contract DE-AC05-96OR22464

UNLIMITED DISTRIBUTION

Final Report for CRADA ORNL95-0367 Monolithic Circuits for Barium Fluoride Detectors Used in Nuclear Physics Experiments

R. L. Varner, J. L. Blankenship, J. R. Beene, R. A. Todd

January 7, 1998

1 Abstract

Custom monolithic electronic circuits have been developed recently for large detector applications in high energy physics where subsystems require tens of thousands of channels of signal processing and data acquisition. In the design and construction of these enormous detectors, it has been found that monolithic circuits offer significant advantages over discrete implementations through increased performance, flexible packaging, lower power and reduced cost per channel. Much of the integrated circuit design for the high energy physics community is directly applicable to intermediate energy heavy-ion and electron physics.

This STTR project, DE-FG05-95ER86029, conducted in collaboration with researchers at the Holifield Radioactive Ion Beam Facility (HRIBF) at Oak Ridge National Laboratory, sought to develop a new integrated circuit chip set for barium fluoride (BaF_2) detector arrays based upon existing CMOS monolithic circuit designs created for the high energy physics experiments. The work under the STTR Phase I demonstrated through the design, simulation, and testing of several prototype chips the feasibility of using custom CMOS integrated circuits for processing signals from BaF_2 detectors. Function blocks including charge-sensitive amplifiers, comparators, one shots, time-to-amplitude converters, analog memory circuits and buffer amplifiers were implemented during Phase I effort. Experimental results from bench testing and laboratory testing with sources were documented.

2 Objectives of the CRADA

The objectives of the CRADA were to complete the Phase I studies associated with the STTR project funded by the DOE Office of High Energy and Nuclear Physics. In conducting this project, both parties learned about the intricacies of CMOS design, especially the unpredictably long turn-around time of the foundries which prepare the prototype chips. We also learned much about

collaboration on the designs and the need for close interaction between the engineers and the scientists during the design and specification of the system. The reviews of the project were generally positive, but in the end, the Phase II proposal was not funded by DOE because of tight funding in the STTR program.

3 Benefits to DOE

This work benefitted the DOE Office of High Energy and Nuclear Physics in several ways. It was educational for the staff at ORNL in learning about CMOS design and its application to BaF_2 processing. We established a working relationship with RIS Corp. which is now being used in development of electronics for other detectors used in the nuclear physics research program of the Physics Division. Finally, the experience has motivated us to continue working on alternative high-density electronics with more features than can be obtained commercially for the BaF_2 array.

4 Technical Report

See the attached "STTR Phase I Final Project Report"

5 Inventions Made

No inventions were made or reported in this work.

6 Commercialization Possibilities

There is no immediate possibility for commercialization of the work done here. The CMOS circuits developed by RIS Corp. may have some commercial potential if incorporated in other devices developed by RIS.

7 Plans for Future Collaborations

At present we have no plans for future collaborations of this sort with RIS. In the future we may discuss the possibility of redefining the research done for the STTR to apply for DOE SBIR grants.

8 Conclusions

We have engaged in an STTR Phase I collaboration with RIS, Corp to develop CMOS prototype circuits for BaF_2 detectors. This collaboration is intended to develop the case for the later, Phase II, work on the project. Although we learned much about the CMOS prototype and development process and had

begun the work of fully specifying the components needed, the project was not awarded a Phase II grant. This was at least in part because STTR is a very small program and its goals are not well-suited to projects as exploratory as this. A better program would have been the SBIR program, which is better funded and is designed to support projects such as this. Nevertheless the project was stimulating to all the participants and has resulted in several development and research activities of benefit to DOE.

STTR

Phase I Final Project Report
to
U. S. Department of Energy

Monolithic Circuits for Barium Fluoride Detectors used in Nuclear Physics Experiments

Grant # DE-FG05-95ER86029

submitted by:

RIS Corporation
Oak Ridge, TN 37830

and

Oak Ridge National Laboratory
Physics Division
Oak Ridge, TN 37831

July 15, 1996

STTR RIGHTS NOTICE (MAR 1994)

These STTR data are furnished with STTR rights under Grant No. DE-FG05-95ER86029. For a period of 4 years after acceptance of all items to be delivered under this grant, the Government agrees to use these data for Government purposes only, and they shall not be disclosed outside the Government (including disclosure for procurement purposes) during such period without permission of the grantee, except that, subject to the foregoing use and disclosure prohibitions, such data may be disclosed for use by support contractors. After the aforesaid 4-year period the Government has a royalty-free license to use, and to authorize others to use on its behalf, these data for Government purposes, but is relieved of all disclosure prohibitions and assumes no liability for unauthorized use of these data by third parties. This Notice shall be affixed to any reproductions of these data in whole or in part.

Phase I Project Summary

Abstract

Custom monolithic electronic circuits have been developed recently for high energy physics large detector applications where subsystems require tens of thousands of channels of signal processing and data acquisition. In the design and construction of these enormous detectors, it has been found that monolithic circuits offer significant advantages over discrete implementations through increased performance, flexible packaging, lower power and reduced cost per channel. Much of the integrated circuit design for the high energy physics community is directly applicable to intermediate energy heavy-ion and electron physics. In collaboration with researchers at the Holifield Radioactive Ion Beam Facility (HRIBF) at Oak Ridge National Laboratory, this project is developing a new integrated circuit chip set for Barium Fluoride detector arrays based upon existing CMOS monolithic circuit designs created for the high energy physics experiments. Phase I work demonstrated the feasibility of using custom CMOS integrated circuits for signal processing of BaF_2 detectors through the design, simulation, and testing of several prototype chips. Function blocks including charge-sensitive amplifiers, comparators, one shots, time-to-amplitude converters, analog memory circuits and buffer amplifiers were implemented during Phase I effort. Experimental results from bench testing and laboratory testing with detectors are included. Future efforts will extend the present work from prototype function blocks to a completed chip set for BaF_2 detectors. Included in Phase II development will be a multichannel analog-to-digital converter chip, and an 8-channel front end chip with emphasis on extensive testing during the design cycle.

Potential Applications

This project will make available integrated electronics which will extend and simplify the processing of signals from photomultipliers coupled to BaF_2 or similar detectors. In addition to enhancing research efforts at the HRIBF at Oak Ridge National Laboratory, other experimenters throughout the world using BaF_2 arrays for nuclear physics experiments such as the Three-Arm-Photon-Spectrometer (TAPS) collaboration in Europe will be interested in the enhanced performance and cost savings of such integrated electronics.

TABLE OF CONTENTS

Page

LIST OF FIGURES

TECHNICAL OBJECTIVE AND TECHNICAL APPROACH

The principal objective of this research is to design and assemble a prototype module which integrates the signal processing requirements of BaF_2 detectors using very-large-scale integrated circuits. This module will be a lower cost replacement of conventional modules, reducing the number of components which can fail, allowing us to setup the array more quickly and precisely, and permitting us to add several features to improve the quality of detector operation. The function blocks developed during Phase I will be tested and refined and finally merged into a final set of one or two chips. Additional level 1 trigger logic using FPGA technologies will be added for flexible definition of trigger logic schemes. The sections below describe our intentions for the final product of this effort which will be realized through implementing the chip set in a VXI module.

Functional Summary

A summary of the functions required are shown in Figure 1. The scintillation light from BaF_2 has two components at 220 nm and 310 nm with decay time of 0.6 ns and 600 ns, respectively. The integral of the fast pulse is about 20% that of the slow, but the amplitude we record is closer to 10% because of the lower sensitivity of our phototubes to the 220 nm component and self-absorption in BaF_2. The pulses from each BaF_2 detector are integrated and digitized to extract the fast component separately from the slow component. The light from the slow component is used for nuclear spectroscopy. We need to be able to accurately measure pulses as small as 0.25 MeV in the same experiment with 100 MeV pulses, a dynamic range of 400:1. The phototube signal is compared to a low threshold equivalent to 0.25 MeV photon energy in the fast component, to determine if a pulse is present. Another discriminator is used to determine if enough energy was deposited in the detector to be of interest for the measurement. Both of these logic signals go to a level 1 trigger which determines if an interesting event has occurred, based on information from all the detectors in the array. The low threshold logic signal starts the digitization of the energy signals and provides the time-of-flight "stop" pulse. This "self-gated" operation of the system reduces our need for precise time alignment of the different detectors, which would otherwise be critical for accurate integration of the fast component signal.

There are additional functions we will add to the basic signal processing. First, we need the ability to inject calibrated pulses into the front-end to verify the operation of the circuits. A copy of the linear pulses goes into an analog sum by banks, packs or whatever geometry is appropriate, for use in forming the trigger. The linear pulses also go into a multiplexed line that permits us to view the signals produced by each detector in order to diagnose problems online. We will also multiplex the logic signals. Finally, we will count each logic output with scalers to keep track of the efficiency and general status of the system.

In some detector configurations, each BaF_2 detector will have a charged-particle veto, a thin plastic scintillator which will give a signal only when a charged particle passes it. We can use this to immediately identify charged particles striking the detector and form a trigger sensitive only to neutral particles. The time of the veto firing will be digitized to help identify charged particle events in later processing of the experiment. Charged-particle hits will be readout if they occur in coincidence with interesting neutral events.

These functions will be controlled by computer. Digitized data will also be read by computer.

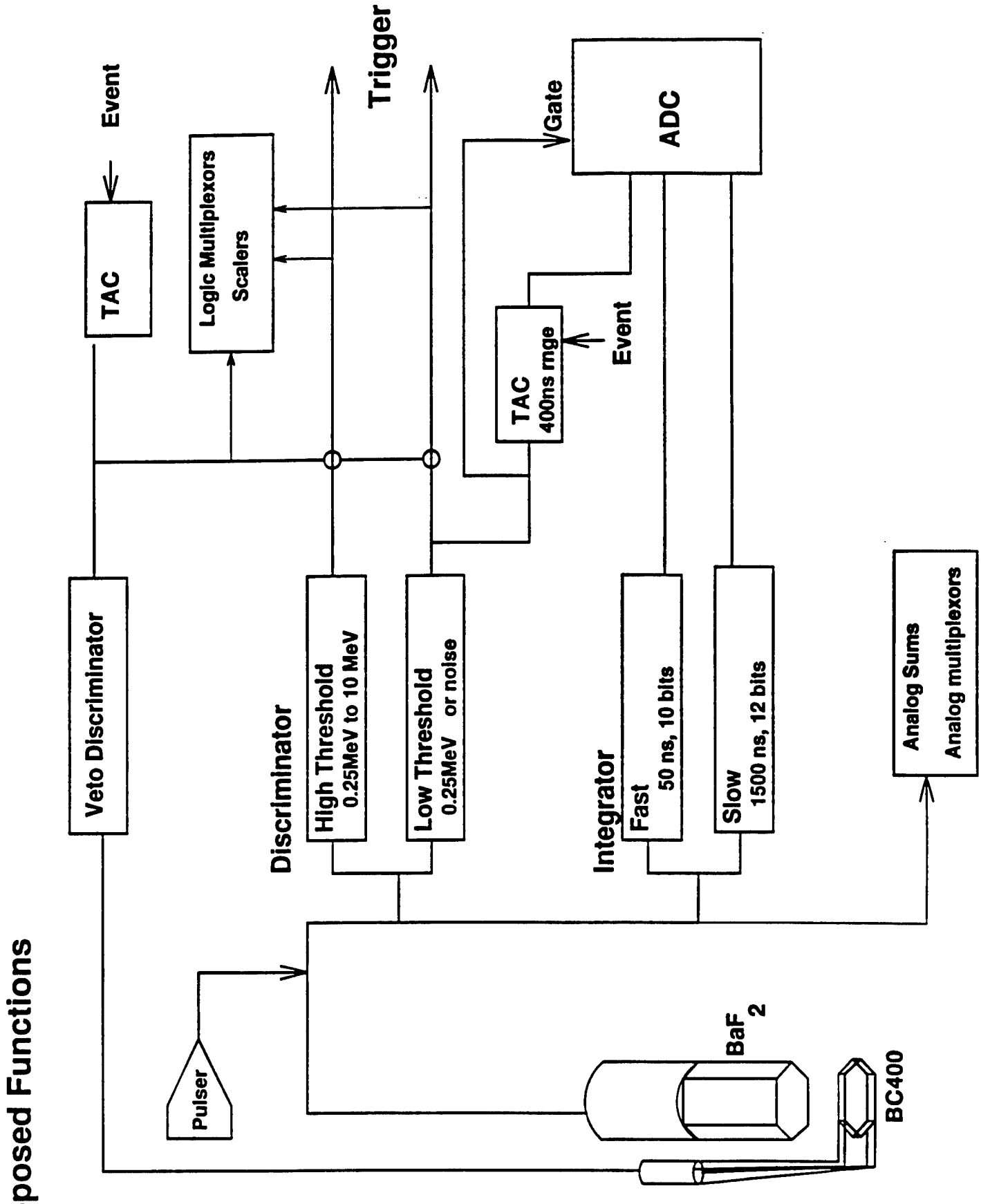


Fig. 1 Functional Summary

Detailed Specifications

The unusual problems we face in completion of this project are the dynamic range required of the integrators, the large difference in the integration times of the fast and slow components, and the accurate measurement of the time-of-flight.

Fast Timing

The fast component of the BaF_2 light pulse provides the excellent timing. The rise time of the pulse is slowed down to 1-2 ns and a decay of about 5 ns by the photomultiplier tube. This pulse provides a high-quality time reference for time-of-flight measurement. Our specification is that we be able to measure the time with a jitter of 0.2 ns FWHM or less, and a range of about 400 ns full scale. We must delay the time measurement for 500 to 600 ns, to give time for the external trigger logic to determine whether or not the event is useful and provide the reference time or common start signal. If a veto pulse occurs, which would be in a plastic scintillator of comparable speed to the fast component of the BaF_2, it will be measured with a similar precision, jitter and delay.

Fast Light Integration

The integrated fast component pulse provides pulse shape and pileup discrimination. The fast-to-slow ratio varies from ~0.1 for photons to ~0.04 for a-particles. Although the integral is much smaller than for the slow light, the fast collection time of the pulse, less than 10 ns, produces a significant pulse height. We typically integrate this pulse for 30 ns, to be sure of collecting all the pulse. The available fast pulse intensity ranges from about 200 pC to 500 pC. The resolution is about three times worse than that for the slow light, because of photon statistics.

Slow Light Integration

We use the slow component pulse for nuclear spectroscopy. The phototube bias is adjusted to give an amplitude of 4500 pC for the maximum energy pulse. The instantaneous pulse height is small and requires an integration time of between 1000 and 2000 ns for optimal resolution. To properly reconstruct electromagnetic showers, we must measure photon energies down to 0.25 MeV, a dynamic range of up to 400:1 at 100 MeV full scale. We require sufficient accuracy to obtain a resolution of not worse than $9\%/\sqrt{E}$, better than the resolution possible from BaF_2 crystals.

Other requirements

The large dynamic range which we require demands a low noise system, particularly in the slow light integration. The presence of such range also requires careful attention to cross-talk in the electronics. Clearly, if more than one detector shares the same analog chip, cross-talk of much less that 0.25% is required. The system will need individual thresholds in the discriminators, because the ratio of fast to slow pulse heights vary significantly from detector to detector. This

is a consequence of uncontrollable experimental factors, such as quality of the crystals and phototube coupling. Without individual thresholds, fast component gain adjustments will be required to assure that all discriminators fire at the same photon energy threshold. Of course, with such a system we need computer control of the thresholds, multiplexors, scalers and pulsers.

The level 1 trigger will determine if a useful amount of energy was deposited in any one detector or in the sum of all detectors. It may also determine if the photons were in coincidence with a particle or other detector signal external to the BaF_2 array.

Meeting the objectives

Analog signal processing

The integration of the analog pulses will be done with a charge integrating preamplifier. The integrated signal will be fed to a clocked analog memory unit (AMU). The AMU address will be advanced at 50 ns intervals in a ring buffer, to keep at least four samples of the integrated signal from the detector. When a pulse is detected by the logic array, the advancement will be stopped after the next advance, to give us a sample of the background and the integrated fast light pulse. After 1500 ns has passed, the AMU will be advanced to one more address to preserve the slow light integration. At that point, if an event signal is present, digitization occurs in which the required buffers are switched to the ADC's for digitization and subsequent readout. This system automatically provides self-gating for each detector. It has the additional advantage of eliminating 100 m of delay cable for each detector, required so that the common gate had time to be generated. This system is similar to that used by the WA-98 electronics[1], with adaptations for the two component nature of the BaF_2 scintillations. The quality of the preamplifier and AMU will have to be investigated carefully to assure that sufficient resolution, low-noise and stability are built in for the higher resolution BaF_2, compared with the Pb-glass detectors of the WA-98 application.

Timing and discrimination

The presence of valid pulses will be detected by comparators on the preamplifier chips, used to discriminate both the presence of any signal and the presence of an interesting signal, with enough energy to justify reading out the array. These discriminators may be leading edge or constant fraction. Many of the effects of leading edge discrimination can be eliminated by offline walk adjustment, but the effects on the trigger timing remain. The important quality of the detector discriminator is that it must be able to trigger on 0.25 MeV pulses. Given the small amount of charge in the fast component pulse, we will need to use nearly the full amplitude pulse from the detector in that discrimination. The stability of the discrimination in time and amplitude will be the important qualities to test.

---

[1] A. L. Wintenberg, T. C. Awes, C. L. Britton, Jr., M. S. Emery, M. N. Ericson, F. Plasil, M. L. Simpson, J. W. Walker, G. R. Young, and L. G. Clonts, "Monolithic Circuits for the WA98 Lead Glass Calorimeter," IEEE Nuclear Science Symposium, Norfolk, VA, Nov. 1994.

ACCOMPLISHMENT OF PHASE I PROJECT OBJECTIVES

Feasibility

The feasibility of implementing the BaF_2 detector signal processing electronics in custom CMOS monolithic integrated circuits was predicated on the recent experience of custom CMOS chip design with applications in high energy physics detectors. Many of the function blocks necessary for processing signals from barium fluoride detectors have been designed and characterized for this work. Going into the project, there was a large amount of literature pointing to the feasibility of this work. The key to successfully designing and producing chips relies upon a knowledge of the processes, accurate modeling and simulation capabilities, as well as experience prototyping function blocks that can be incorporated in more complex chip designs.

Phase I of this project has been very successful in giving us experience in designing and manufacturing chips. In all, four prototype chips have been designed and implemented. Additional computer-aided design tools have been acquired and configured to design, simulate, and layout these chips. The models used in the simulations were based upon the level 3 model parameters published by MOSIS. A representative listing of these parameters for the ORBIT 1.2 μm low noise analog CMOS process is included as Appendix C.

Architecture

In defining the architecture of the Phase I work, it became obvious that there were both immediate and long term architecture objectives. The block diagram of Figure 2 is a conceptual arrangement of the separate function blocks required in the final system. By prototyping each function block as a separate integrated circuit in "tiny chip" form, the performance of each block could be examined and refined before placing all circuitry on a final large chip. Test boards for the phase I work were designed to test only each individual chip and it remains to assemble all chips in a total system. The ultimate system architecture will combine multiple function blocks into a target chip set composed of two custom CMOS integrated circuits plus some programmable logic devices forming the control and trigger functions. The pulse height measurement system is event driven rather than sampling at a fixed frequency as in collider experiments. This concept has implications on the depth of the analog memory buffer required and the number of sample data points taken during the slow light component duration.

Function Blocks

Monolithic circuit blocks for Barium Fluoride signal processing have been designed and implemented in several prototype CMOS integrated circuits. All test chips created during Phase I were fabricated using the ORBIT Semiconductor 1.2-μm n-well CMOS process. These were

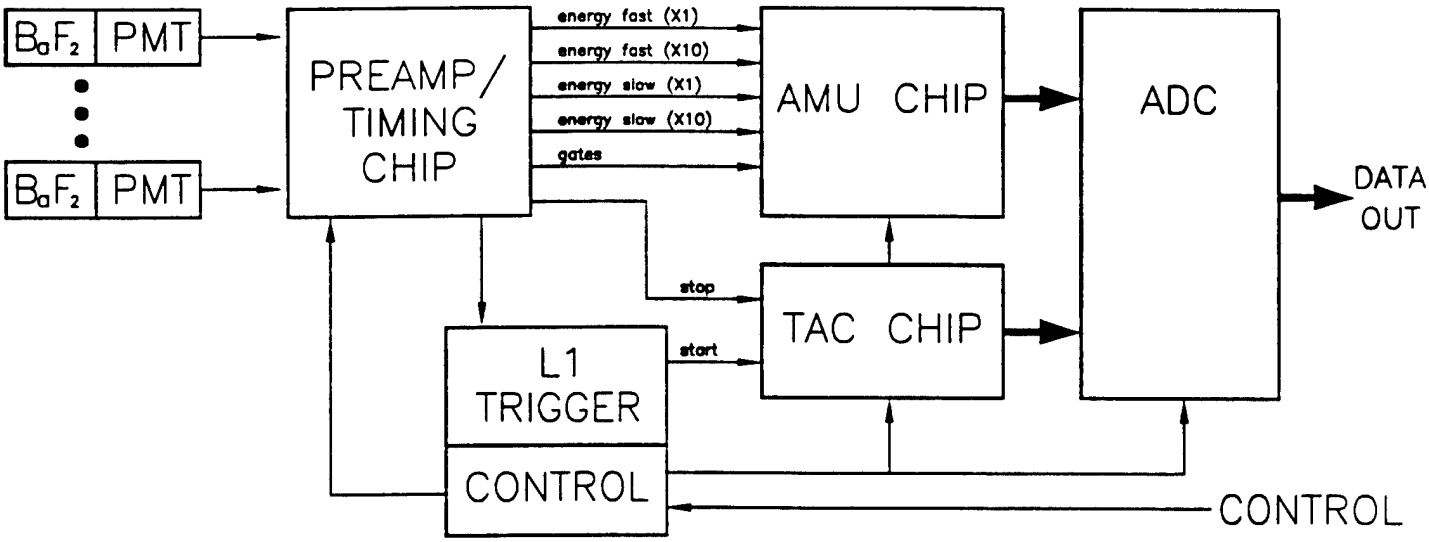


Fig. 2. Barium Fluoride Chip Set Block Diagram

implemented in tiny chips (2.2 mm x 2.2 mm) and housed in 40-pin dual-in-line packages. Prototyping runs were submitted through the MOSIS service of Marina del Rey, California. Prototyping services are offered through ORBIT directly at significantly higher cost but quicker turnaround and more parts, or through MOSIS which is less expensive, but has required a longer time frame.
Prototyping through MOSIS was chosen so that more chip designs could be afforded, although the slipped delivery schedule has impacted the testing aspect of this research. For example, the fabrication run scheduled to begin December 27, 1995 was held open until January 31, 1996. These chips were received 5 weeks later than planned, and while testing on these chips has continued, the weakness of the Phase I progress has been in the short testing time available after delivery of the chips. The major function block chips, the *baf2chip* and the *baf2r1 chip* were bench tested and results are included in this report. The amu_chip and tac_chip are not yet tested. A description of the four prototype chips produced is included beginning with the *baf2chip*, followed by the *amu_chip*, the *tac_chip*, and a refinement of the first chip, the *baf2r1 chip*. Photographs of the chips are included in Appendix B of this report.

baf2chip

The first prototype chip implemented, the baf2chip, includes four channels of charge-sensitive amplification followed by second and third stage amplifiers to provide gains of x1 and x10 outputs for each channel. Each input is also applied to a lower level discriminator circuit consisting of a comparator and two one-shot circuits which can be used as gating signals to sample the fast and slow components of the energy output. A block diagram of the baf2chip is shown in Figure 3. Using the dual output ranges extends the dynamic range of the system.

The integrating amplifier design is based upon a monolithic function block developed for lead-glass calorimetry by Dr. A. L. Wintenberg of Oak Ridge National Laboratory. The preamplifier features a p-channel differential input stage followed by an inverting stage with internal compensation added. The overall gain-bandwidth product of this integrating gain block is 70 MHz. The charge-sensitive gain is determined by using a 2-pF double poly capacitor in the feedback of each channel in parallel with a long channel FET. High megohm resistor values are not feasible to implement with standard CMOS processing, thus a long channel FET is used to provide a high impedance dc path from output to input for bias stability. A dc voltage applied to the long channel FET gate is adjusted to vary the effective feedback time constant of this stage, and can effectively adjust the equivalent feedback value from open to under 100-kΩ resistance.

The second and third amplifier gain blocks are similar to the first, using p-channel input devices and an inverting output stage. The output devices for these function blocks are larger, which provides higher open loop gain and higher output drive capability. Internal compensation of the second amplifier block stabilizes the circuit for a gain of two; the third gain block is compensated for a gain of ten. Feedback resistors on the second and third stages are implemented using on-chip polysilicon material with feedback values of 36 kΩ with 36 kΩ and 36 kΩ with 4 kΩ to give block gains of two and ten respectively.

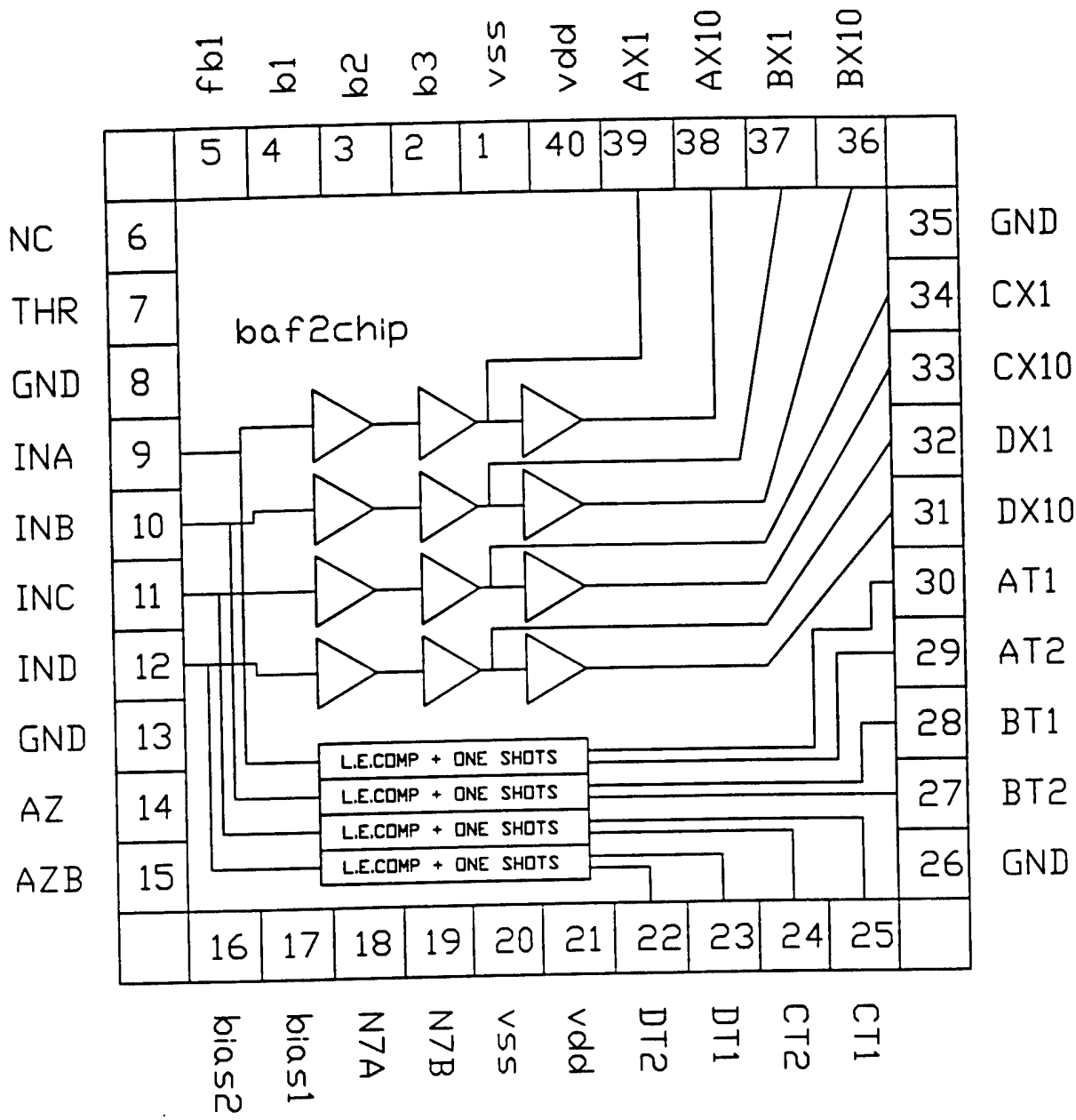


Fig. 3. Block diagram of baf2chip.

Leading edge discriminator circuits on each channel are designed to trigger on the leading edge of the fast component of barium fluoride scintillation signal. Some integration of the 600-ps decay signal from the photomultiplier tube (PMT) anode is inevitable because of the phototube characteristics and any cabling effects from PMT to the electronics module. In the case of the present barium fluoride experimental setup, the leading edge signals peak in approximately 2.5 ns which precludes using an arming comparator and zero crossing comparator scheme without substantially limiting the bandwidth of the signal which degrades the time resolution. Even though timing errors arising from walk because of signal amplitude variations can be corrected somewhat during post processing, the leading edge scheme employed in the first chip was intended to exemplify the implementation of comparator and one-shot function blocks, and not necessarily represent the final answer to timing circuitry issues.

PMT signals are terminated on board with a 50-Ω resistor creating a voltage at the chip input which is proportional to the current from the photomultiplier tube and thus the light output of the barium fluoride scintillator. This signal is differentiated on-chip through a 1-pF series capacitor with a 10-kΩ resistor to analog ground. The threshold of the four comparators is set by an externally applied negative dc voltage level. In this first chip, each channel comparator triggers both a short and a long pulsewidth monostable multivibrator. The width of each one shot is independently controlled by bias currents applied external to the chip. Typical pulse width values range from 20 ns to 200 ns and 150 ns to 1500 ns, respectively, depending on the external bias control settings.

An autozero mode has been added to the leading edge comparators to significantly reduce any input offset voltage of the discriminator circuit. During the autozero mode, each comparator is reconfigured to be a unity gain, linear amplifier. Analog switches connect each positive input to analog ground and tie each negative input to its comparator output thus forming a X1 buffer amplifier. The resulting output offset voltage is stored on a hold capacitor, C_H. This stored value is applied to the comparator input along with the external threshold after the autozero mode is completed.

Two schematics are shown in Figures 4a and 4b of the on-chip circuitry used to implement the one shot functions. Fig. 4a is a more detailed transistor level schematic of the one-shot circuit while Fig. 4b shows a simplified logic diagram of the function block. The one-shot circuit was used in both the *baf2chip* and the *baf2r1* chip following the comparators. The one-shot pulse widths are controlled by the current mirror formed with M12 and a second device common to one shot circuits in all channels. The capacitor, C1, was sized according to the pulse width required. Fine control of the output pulse width was provided by an external resistor and potentiometer on the test board.

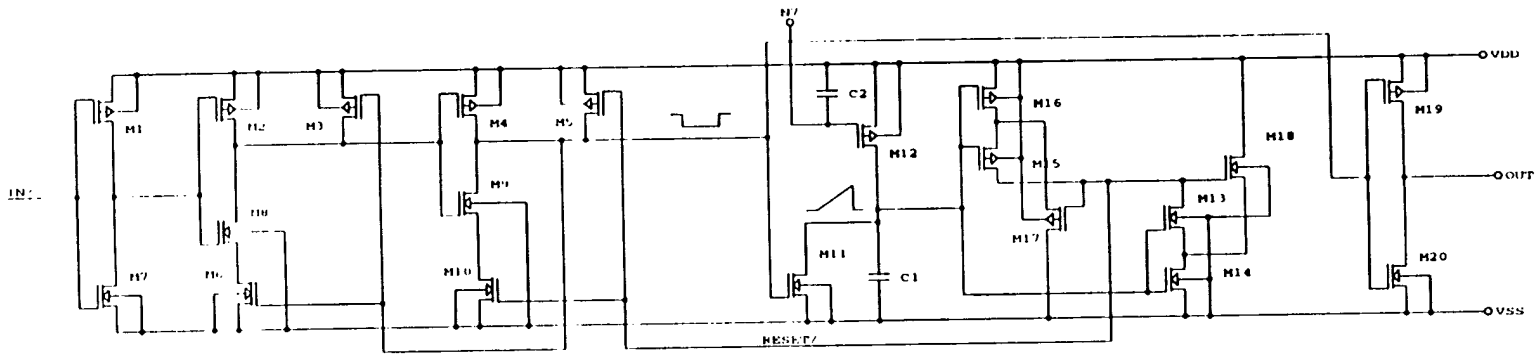


Fig. 4a. Transistor Level Schematic of One Shot Circuit

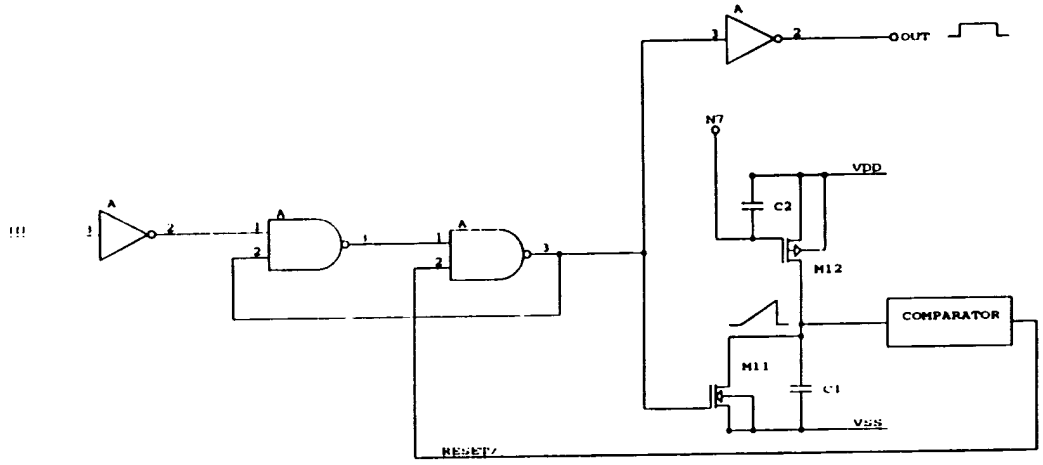


Fig. 4b. Simplified Block Diagram of One Shot Circuit

tac_chip

The time-to-amplitude converter chip was fabricated in a 12-channel configuration. Each channel has three main functional blocks: the logic elements comprising the digital control circuitry, the ramp generator circuit, and the unity gain buffer amplifier to drive the output. The tac_chip was designed to operate in a common start mode, and two common *start* signals are included, each of which controls six channels. The twelve *stop* signals are active on the falling edge. Complementary logic levels from this NAND-gate constructed flip-flop drive a differential p-channel pair that steer current either to the charging capacitor or to Vss, the most negative voltage rail. A second flip-flop discharges the ramp capacitor upon receiving a positive logic level *reset* signal. The capacitor is held in a discharge state until a subsequent *start* signal is received at which time the n-channel discharge transistor is turned off and the charging current is steered onto the capacitor by the differential pair.

The time-to-amplitude converter principle is based upon the charge integration of a fixed current source applied to a small double poly capacitor for a time duration set by the start and stop logic signals for each channel. The integration capacitor was sized to be $0.59\mu m^2$ or 0.3 pF. A full-scale time difference ranging from 250 to 1000 ns between start and stop signals can be translated into a full scale (4V) change in output voltage by applying 1.2 to 4.8 μA of charging current to this 0.3-pF capacitor. Current mirrors on chip are used to translate higher bias currents applied external to the chip to these lower value charging currents that define the ramp slopes.

The unity-gain buffer amplifier driving the output was implemented as a differential operational amplifier gain block with p-channel input devices. A series RC network was added internally to compensate the design to be unity gain stable. As in the analog memory chip, twelve buffer amplifiers are arrayed along the output side of the chip with supply voltages Vdd, Vss, and ground running vertically along the array, and a bias control line tied to all twelve readout amplifiers. One of the twelve units contains a diode-connected transistor, and that node is pinned-out externally so that a single pull-up resistor and potentiometer network could be added to determine the quiescent bias levels of all amplifiers.

amu_chip

The analog memory chip is organized in a 12-channel width by eight memory cells deep architecture. The components of the analog memory include analog switches, storage capacitors, buffer amplifiers, and a read/write decode logic circuit. The voltage signals applied to each channel are sampled differentially, as shown in the switch level schematic of Figure 5. Switch elements connect both the top and bottom side of the storage capacitor to the signal and input ground reference respectively during the analog write cycle. During the read cycle, a second set of switches connects the selected storage capacitor as the feedback component in an output amplifier circuit. A reset switch in the feedback of the readout amplifier is used to connect the output stage in a unity-gain configuration and can be used to discharge single storage capacitors or to monitor the readout amplifier offset voltage.

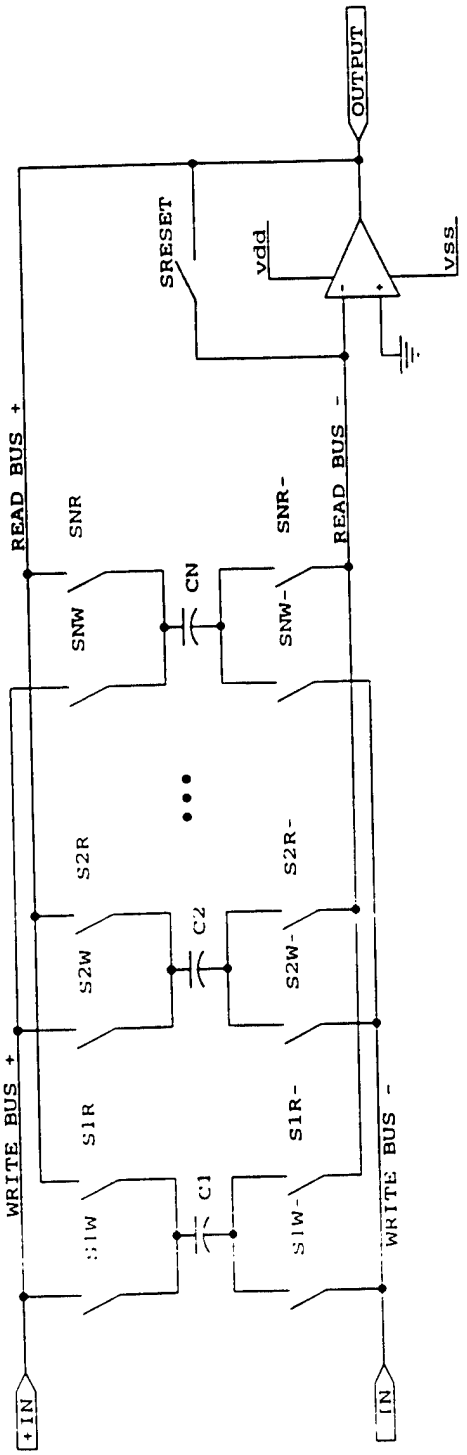


Fig. 5. Switch level schematic of the analog memory channel

All analog switches are implemented using complementary devices in parallel with sizes of 12-μm by 1.2-μm (p-channel) and 4.2-μm by 1.2-μm (n-channel) as shown in the transistor-level schematic of Figure 6. A double poly capacitor of value 2.75 pF was used for each storage cell measuring 21-μm by 96-μm. This value of storage capacitor is larger than might be needed for other comparable applications and directly increases the cell unit area; however, charge injection errors from the switch control lines are minimized as is the droop rate. Because the write time requirements are faster than the read time requirements, the switch pairs could be of different sizes. The designed write cycle will typically be a 35-ns sample period followed by a precisely timed hold. The read cycle hold time will be determined by the conversion time of the analog-to-digital converter which may typically be on the order of 10 μs. The accuracy of the analog memory should be at least 11 bits and, with a x10 additional gain, the dynamic range of the system is aimed to be at least 14 bits. These criteria are less stringent than other published designs such as for electromagnetic calorimetry for high energy physics detector applications.

The buffered analog readout amplifier for the *amu_chip* is the same design as described for the *tac_chip*. Twelve buffer amplifiers are arrayed along the output side of the chip with supply voltages Vdd, Vss, and ground running vertically along the array, and a bias control line tied to all twelve readout amplifiers.

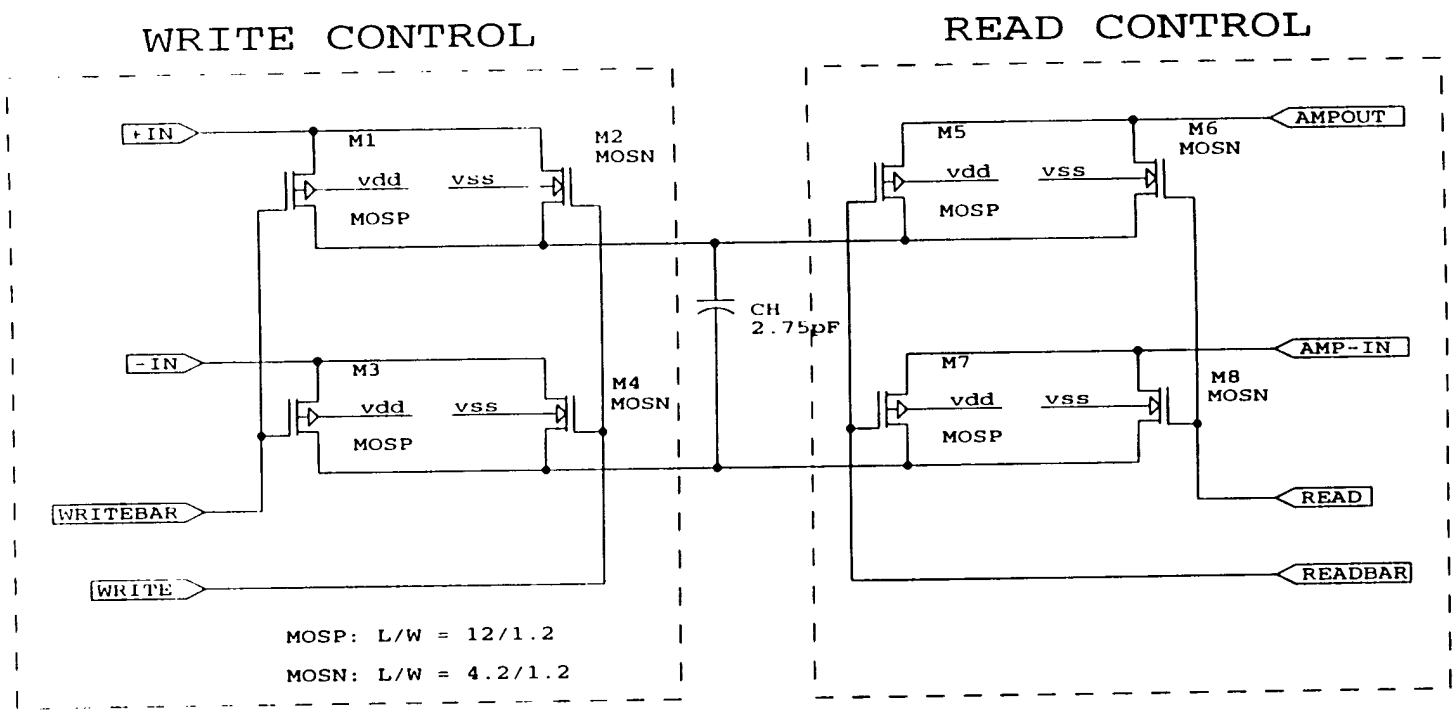


Fig. 6. Transistor level schematic of analog memory cell

baf2r1 chip

Dual Charge-Sensitive Amplifiers

The baf2r1 chip was designed and implemented in a 1.2-μm analog CMOS process as a refinement of the first prototype, the baf2chip. The charge-sensitive amplifiers used were reconfigured as two amplifier channels per input signal with fast and slow feedback time constants implemented in the first stage integrators. The long-channel feedback FET was shortened for the fast signal path to be only 10.2-μm long compared to 100-μm long for the slow signal path feedback element. As in the *baf2chip*, the following gain stages were configured for gains of 2 and 10 in both signal paths as in the first chip. Separate bias control for each of the three stages was provided external to the chip in order to adjust the gain-bandwidth of each type amplifier block. Figure 7 illustrates the block diagram of the baf2r1 chip housed in its 40-pin package.

Leading edge Discriminators

Timing information from each fast signal input is applied to a dual threshold comparator arrangement through a fast differentiation network composed of a 3.8 pF capacitor and a 5k resistor. Voltage threshold values, *thr1* and *thr2*, are brought to external pin connections in the prototype. In operation, the lower threshold magnitude is set slightly above the background noise level, and will trigger a stable one-shot circuit which is typically set for approximately 15 ns width. False triggering of this discriminator is expected. The second threshold magnitude is set above the noise level at an appropriate level and, if exceeded, arms the first output timing signal which occurs on the trailing edge of the first one shot. Thus, the timing information is attributable to the lower level threshold crossing delayed by the first one-shot pulse width. Three timing pulses are generated per channel: the first is an immediate leading edge signal delayed by the one-shot width just described. This first pulse then triggers two other adjustable delays of 1-1.5 μs and 200-400 ns which trigger fast narrow pulses at their trailing edges.

Level 1 trigger information is generated from the immediate output timing signals. System timing information from the level one trigger logic generates a common *start* signal to all time-to-amplitude converter channels. The second timing signal from each channel, which has been delayed by the adjustable 200-400 ns, individually sends a *stop* signal for each channel.

The immediate timing signal from each channel is also used to sample the fast integrator analog outputs. With the 600-ps fast light component of the barium fluoride scintillator, the fast integrated signal rise time is more dependent upon the response time of the input cabling scheme and the response of the active integrator stages than on the intrinsically fast signal itself. The width of the immediate timing pulse is chosen to sample all of the integrated fast light component and a minimal portion of the slow light component. Timing information can be later corrected for walk resulting from amplitude variations, and some post-processing refinement for gate width walk with large signals may be implemented.

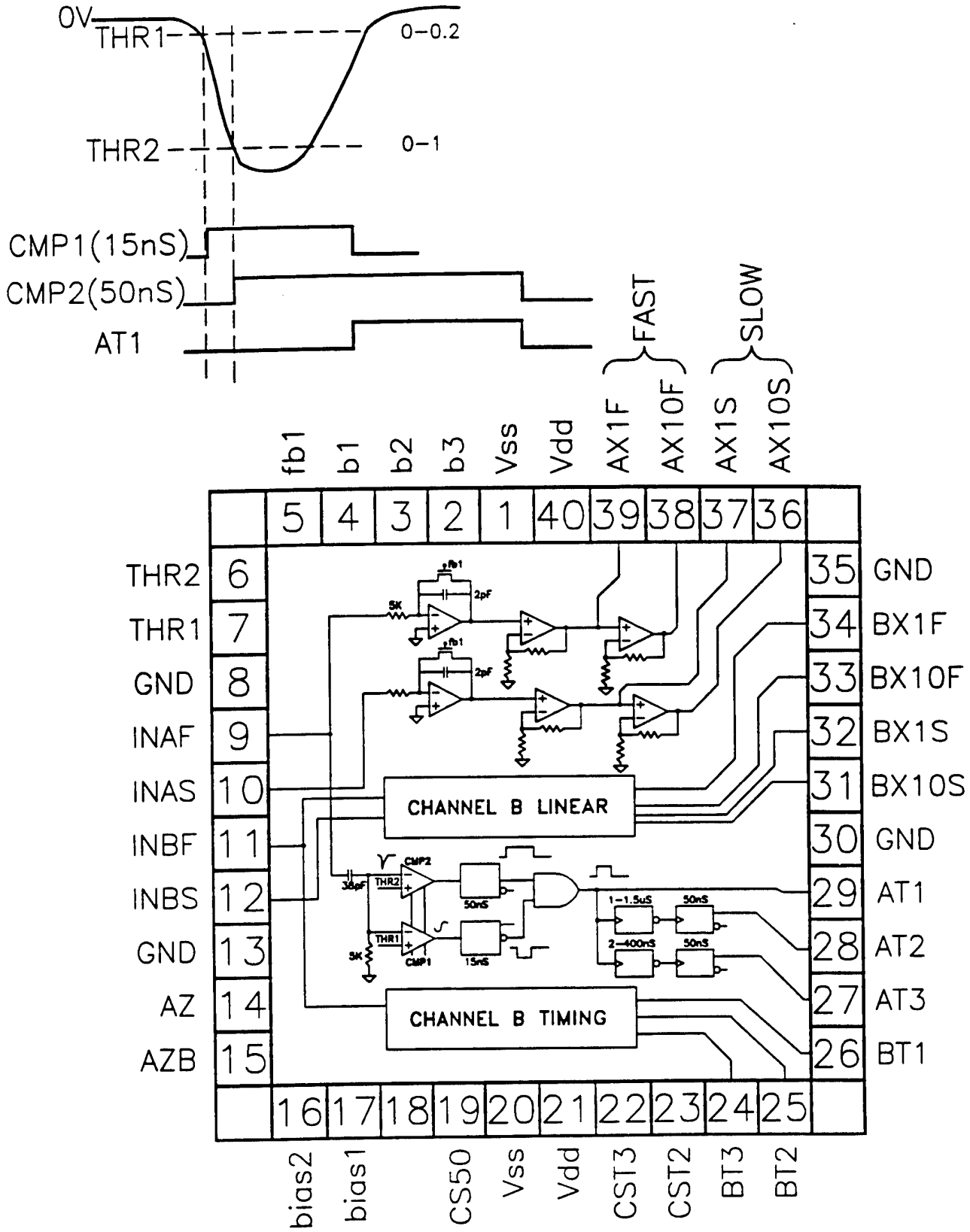


Fig. 7 Block diagram of the bat2r1 chip.

Performance and Cost

The economics of implementing monolithic circuitry for medium energy physics experiments must be lower than conventional approaches in order to be considered. In this section, costs of IC production are examined.

The integrated circuit costing rules used in the large physics experiments are based on factors such as die size, yield, fabrication cost, package cost, and testing. In large scale production, these costs ranged from $10 to $28 as reported in a GEM Electronics meeting in Dec. 1992. Shown below is a table from the Solenoidal Detector Collaboration (SDC) IC costing rules.

SDC IC Costing Rules						
Size	Area	Yield	Fab.	Pkg.	Test	Total
Tiny	6.8 mm^2	70%	$ 2.05	$ 1.00	$ 7.50	$ 10.55
Small	35 mm^2	65%	$ 11.17	$1.50	$ 8.00	$ 20.67
Medium	50 mm^2	60%	$ 17.65	$2.00	$ 8.50	$ 28.15

Table 1. Integrated circuit costing rules from the SDC experiment.

The costs associated with small scale production of integrated circuits for physics experiments that may have only 500 to 1000 channels will still be driven by the prototyping costs and will not require the number of chips resulting from a multi-wafer production run. For a 1000-channel experiment with either 4, 8, or 16 channels of electronics per chip depending on the chip size, a production run of 250, 125, or 63 completed chips is required. We expect that the signal processing for BaF_2 experiments can be incorporated in a chip set of two small size (21.6 mm^2) integrated circuits with a chip set cost per channel of $120. Hardware costs including printed circuit boards, enclosures, programmable logic interface chips, and connectors will still result in an additional cost per channel which is much less than the current $1200 per channel.

Small Scale Production Costs through MOSIS (FY96)						
Size	Area	Channels per chip	Yield	Fab.+Pkg.	(F+P)/Yield	Cost per channel
Tiny	4.8 mm^2	4	70%	$200	$286	$71.50
Small	21.6 mm^2	8	60%	$288	$480	$60.00
Medium	91 mm^2	16	50%	$875	$1750	$109.00

Table 2. Small scale prototyping costs through MOSIS assuming minimum quantity prices.

1 GEM Collaboration, Electronics Engineering Meeting, December 16 & 17, 1992, held at Princeton University, GEM TN-92-255, p. 207.

EXPERIMENTAL RESULTS

The Test Board

The test circuit for the baf2r1 chip was housed in a single width NIM module for convenient access during bench testing as well as portability to the detector array laboratory for tests with detectors. The NIM format provided an excellent ground plane configuration and quiet analog power supplies for testing purposes. A reduced copy of the schematic for the test board is included in Appendix A. The input and output circuits were designed to be representative of a final implementation in that input signals were connected through front panel Lemo connectors and terminated in 50 ohms. For testing purposes, all analog output signals were buffered through high speed unity gain Burr-Brown BUF600 integrated circuits. The logic output signals were buffered through Motorola MC10124 ECL level translators.

In order to encompass the input and output signal ranges yet retain a total supply differential of 5 volts, supply voltages of -1.25 volts and 3.75 volts were selected. The test board included voltage regulators to provide +5, +3.75, and -1.25 volts as well as a -5.2 volt line (designated VEE) derived through a 1N5406 diode from the -6.00 volt NIM supply. The anode current signal from the photomultiplier tube is applied across the input 50-ohm termination resulting in a negative-going pulse proportional in time to the anode current. A small fraction of the input current actually flows to the input summing node of the integrator stage through the 5k-ohm input resistor. The output of the integrator rises positively through a 2-pF feedback capacitor.

Stability of the operating point proved to be a problem in the preamp design. It was found that the long channel FET configuration for the integrating amplifiers did not provide a dc feedback path to stabilize the operating point, and any voltage applied to the gate control pin had no observable effect on the integrating amplifier time constant. The long channel FET's were sized to be 100-μm long by 1.2-μm wide to effect a high-megohm resistive feedback component for dc-stability purposes as opposed to a discrete high-megohm resistor which could not be fabricated on the CMOS chip. When it was found that the long-channel FET was essentially open circuited, several external dc path circuits were considered to proceed with testing. The most obvious was to connect a high-megohm resistor in parallel with the long-channel FET, but unfortunately, neither node was actually connected to an external pin. The input summing node was connected through a 5k-ohm resistor, and the output was available only after a second stage with gain of two. Nevertheless, a dc feedback path from the X1 outputs to each input could conceivably be equivalent to the on-chip long-channel FET and provide dc loop stability. Bench testing of this configuration resulted in severe low frequency oscillations at a few hundred Hertz. PSPICE simulations were run which showed good phase margin even at low frequencies. Alternate feedback paths were explored, with the one represented by the schematic drawing having passed both bench testing and PSPICE analysis.

The BUF600 unity gain buffers presented some crosstalk and oscillation problems on the test board even though the supply lines were well bypassed with low series inductance ceramic bypass capacitors at each chip. The high impedance input node of each buffer was terminated in 2k-ohms to ground in order to stabilize all channels simultaneously. In addition, output

series resistors of 47-Ω were included to back terminate each output line and to provide a less reactive load to each driver. The 2k-ohm load for each analog output from the baf2r1 chip presented a severe load for its output amplifiers. The 2k-ohm loading is not severe in the conventional practice of discrete printed circuit board design, but it represents a significant requirement in the design world of on-chip integrated circuit loads.

The matter of designing for conventional drive requirements *vs.* designing circuitry for on-chip drive or perhaps to design for off-chip drive of very moderate load requirements is an issue at the heart of monolithic design philosophy. One attraction of custom chip amplifier design is that the circuits may be less universal than the catalog offerings of commercial vendors. One may need the bandwidth, noise, and slew rate of an off-the-shelf integrated circuit, but may not want the power consumption or need the output drive capability. Carefully designed custom amplifiers can meet the exact requirements using less area and power than generic amplifiers found in discrete implementations. Severe drive criteria may be met, however, with custom designs, but one should not automatically assume that custom integrated circuits will perform just like their commercial counterparts unless drive requirements are built into the specification. Such was the case with the baf2r1 amplifiers which were designed to drive only a 10-pF, high impedance load. These design requirements are adequate for providing signals to an on-board analog memory circuit, but will not successfully drive a 50-ohm load. Thus, the BUF600 chips were added for test purposes.

Logic signals for the autozero function were generated on the test board using an LM555 oscillator with 74HCT4538 one shot circuits (U6, U7A & U7B). The autozero (AZ) and its inverse (AZB) are used to compensate for any dc input offset voltage resident on the comparator circuits, and are present for approximately 1.0 microsecond every 10 milliseconds. These functions could easily be placed on-chip, but were external in this case to provide easy access and control during the testing phase.

Bench Testing with Signal Generator

The *baf2r1* chip was tested in the NIM module configuration described above and detailed in Appendix A. Illustrated in the three parts of Fig. 8 are the input and responses for a fast light simulation using a BNC Model BL-2 pulser. Fig. 8a shows the pulser output for this test, which adequately models the rise of the fast light component from the BaF_2 scintillator adjusted for the response time of the photomultiplier tube and associated cabling. The *baf2r1* output shown in Fig. 8b shows a considerable amount of low frequency noise riding on the signal response. The rise time of the integrator output is on the order of 40 ns and appears to be exhibiting some large signal slew rate limitation in its response. Even with such a large signal and severe load resistance, however, the response time of the integrator is adequate to sample the fast light component at a time 50 ns after the pulse event. Fig. 8c shows the fast light component response after passing through a 1-μs shaping amplifier which removes a significant amount of the low frequency noise component from the signal. The baseline subtraction scheme envisioned for the signal processing of stored analog memory will likewise remove this low frequency component from the digitized signal.

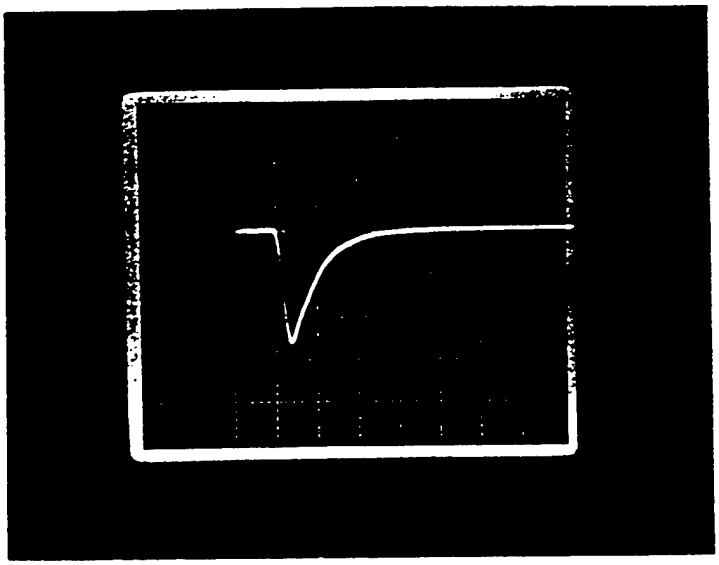


Fig 8a. BL-2 pulser output for fast light simulation using pulser settings of τ_R = 3 ns and τ_F = 10 ns.
Display is 0.5 V/div. and 20 ns/div.

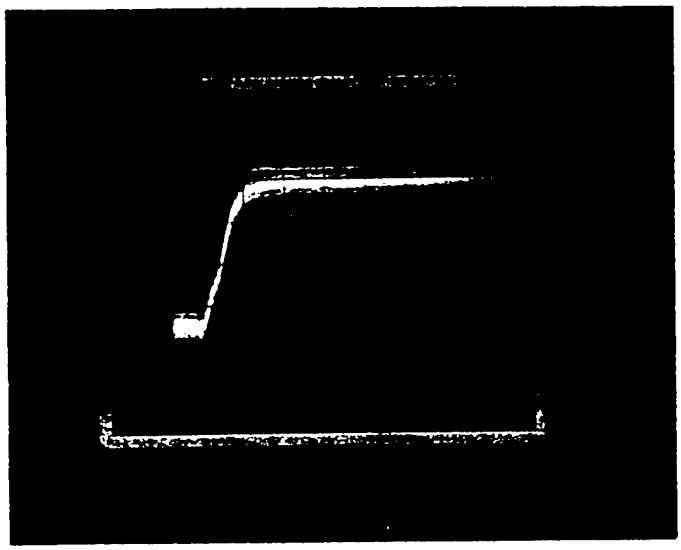


Fig 8b. *baf2r1* chip X1 output for fast light simulation.
Display is 0.5 V/div. and 50 ns/div.

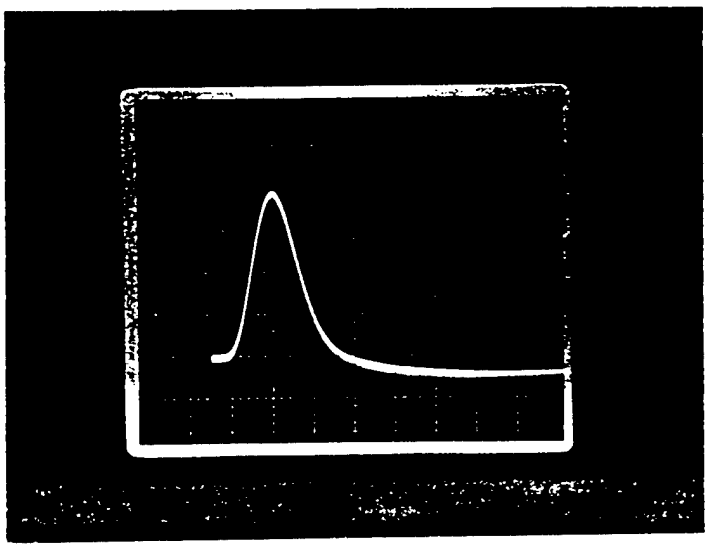


Fig 8c. *baf2r1* chip X1 output with 1-μs shaping for fast light simulation.
Display is 1.0 V/div. and 2 μs/div.

The waveforms shown in Figures 9a through 9c illustrate the system response to slow light simulations using the BNC Model BL-2 pulse generator. Figure 9a shows the pulser output representative of the slow time constant of the BaF_2 scintillator. A more precise simulation would have required an internal modification to the BL-2 pulser to set the decay time constant to 600 ns. The *baf2r1* pulse response shown in Fig. 9b again exhibits some low frequency noise and a decay time resultant from the external dc path added to the test circuit. The waveform of Fig. 9c results from passing the *baf2r1* output through a 1-μs shaping amplifier which has reduced considerably the low frequency noise component, as a baseline subtract scheme would perform.

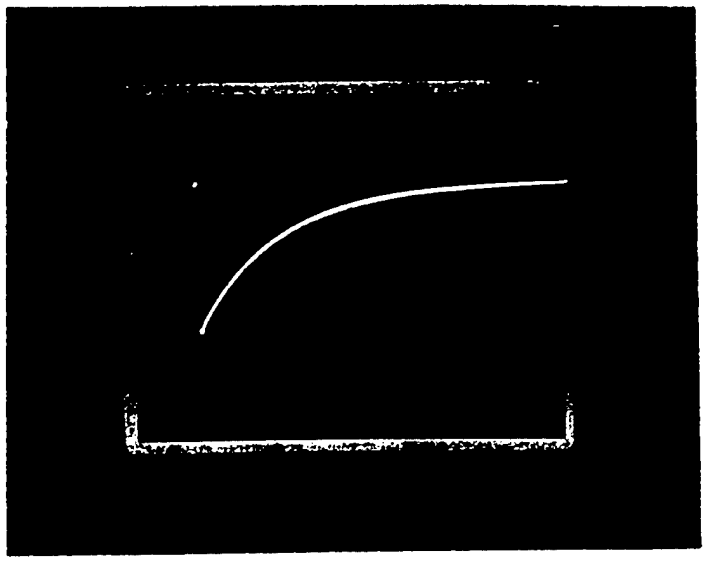


Fig 9a. BL-2 pulser output for slow light simulation using pulser settings of τ_R = 3 ns and τ_F = 300 ns. Display is 20 mV/div. and 200 ns/div.

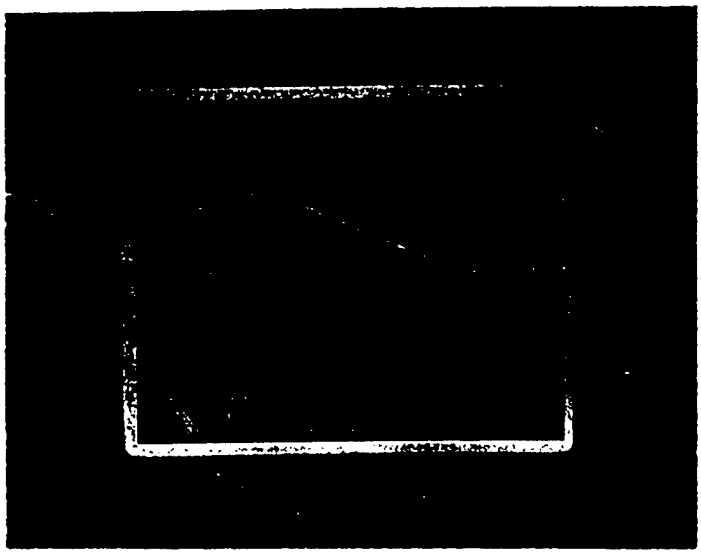


Fig 9b. *baf2r1* chip X1 output for slow light simulation.
Display is 0.5 V/div. and 2 μs/div.

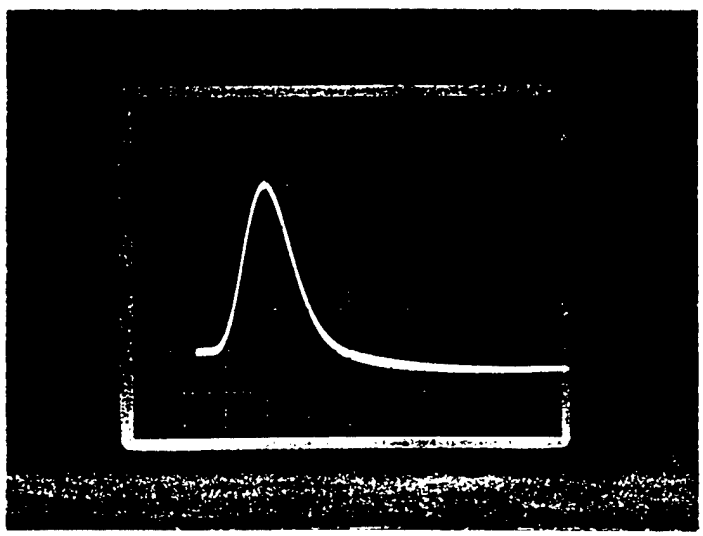


Fig 9c. *baf2r1* chip X1 output with 1-μs shaping for slow light simulation
Display is 1.0 V/div. and 2 μs/div.

Testing with a BaF_2 Detector and Sources

The *baf2r1* chip was tested with ^{137}Cs and ^{60}Co sources in a typical application using one of the BaF_2 detector/phototube base assemblies. An ORTEC 571 amplifier with 2-μs shaping followed the test device and a LeCroy Research Systems 3511 peak sensing ADC was used to digitize the peak amplitudes. Additionally, a ORTEC Model 113 preamp was substituted for the baf2r1 test chip to compare their responses.

The first system test result is shown in Fig. 10 with a tail pulse applied to the input of the *baf2r1* chip. The preamp output was applied to the ORTEC 571 shaping amplifier and the LeCroy Research Systems 3511 ADC as described above. The resultant full width half max (fwhm) shown is 7.3 channels with the peak at approximately 200 channels, for a noise induced width of 3.65% at fwhm.

Shown in Fig. 11a is the conventional ORTEC preamplifier and system response from a ^{60}Co source exhibiting a peak-to-valley ratio, P/V, of 353/253 or approximately 1.3. This low number was judged to be due in part to a poor detector. Additionally, warm temperatures in the laboratory contributed to this result. Nonetheless, the ^{60}Co peaks were resolved with this setup.

The system response of Fig. 11b was observed using the ^{60}Co source applied to our *baf2r1* test board. The gain of the shaping amplifier was adjusted slightly to match the system gain of the previous case. The peak-to-valley ratio is nondiscernable due to system noise contributions, however, the outside edges of each peak are moderately steep indicating that a modest improvement in noise performance would match the result of Fig. 11a. This improvement possibility will be discussed later in the conclusions.

The system responses to ^{137}Cs are shown in Figures 12a and 12b using the ORTEC 113 preamp and the *baf2r1* test board respectively. Arbitrary gain settings were chosen for these results. In the first case, the center occurred at channel 223 with a fwhm of 34 channels, or 15%; in the second, the center occurred at channel 158 with a fwhm of 26.8 channels for a percentage of 17%. Additionally, the lower level threshold setting for both cases of the *baf2r1* test chip was close to the noise level. This was due to the low frequency noise component in the preamplifier output, and improvements in this area must be made in order to utilize these circuits in any real system.

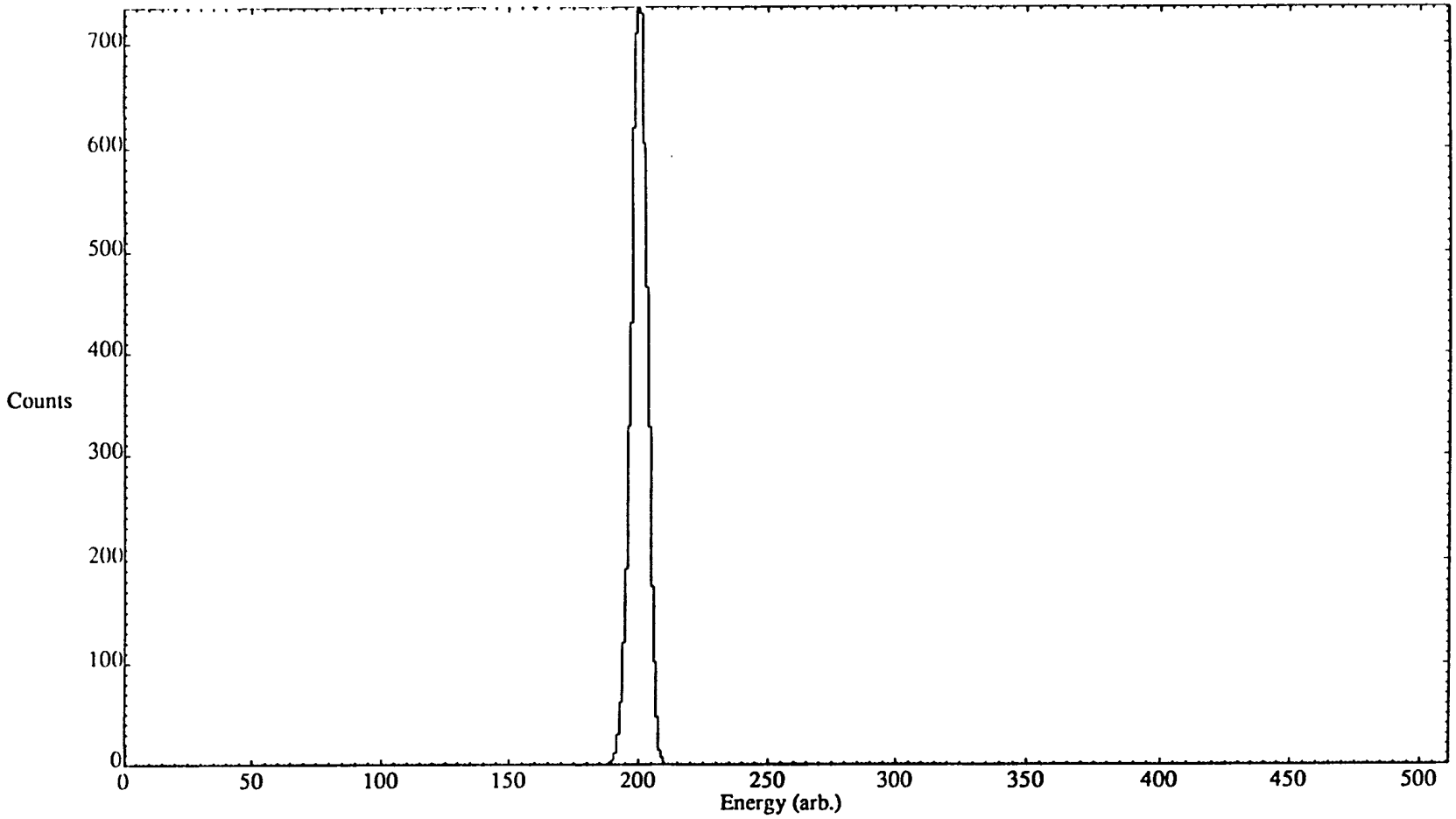


Fig. 10. System response of pulser applied to the baf2r1 test board followed by ORTEC 571 shaping amplifier and 3511 peak sensing ADC.

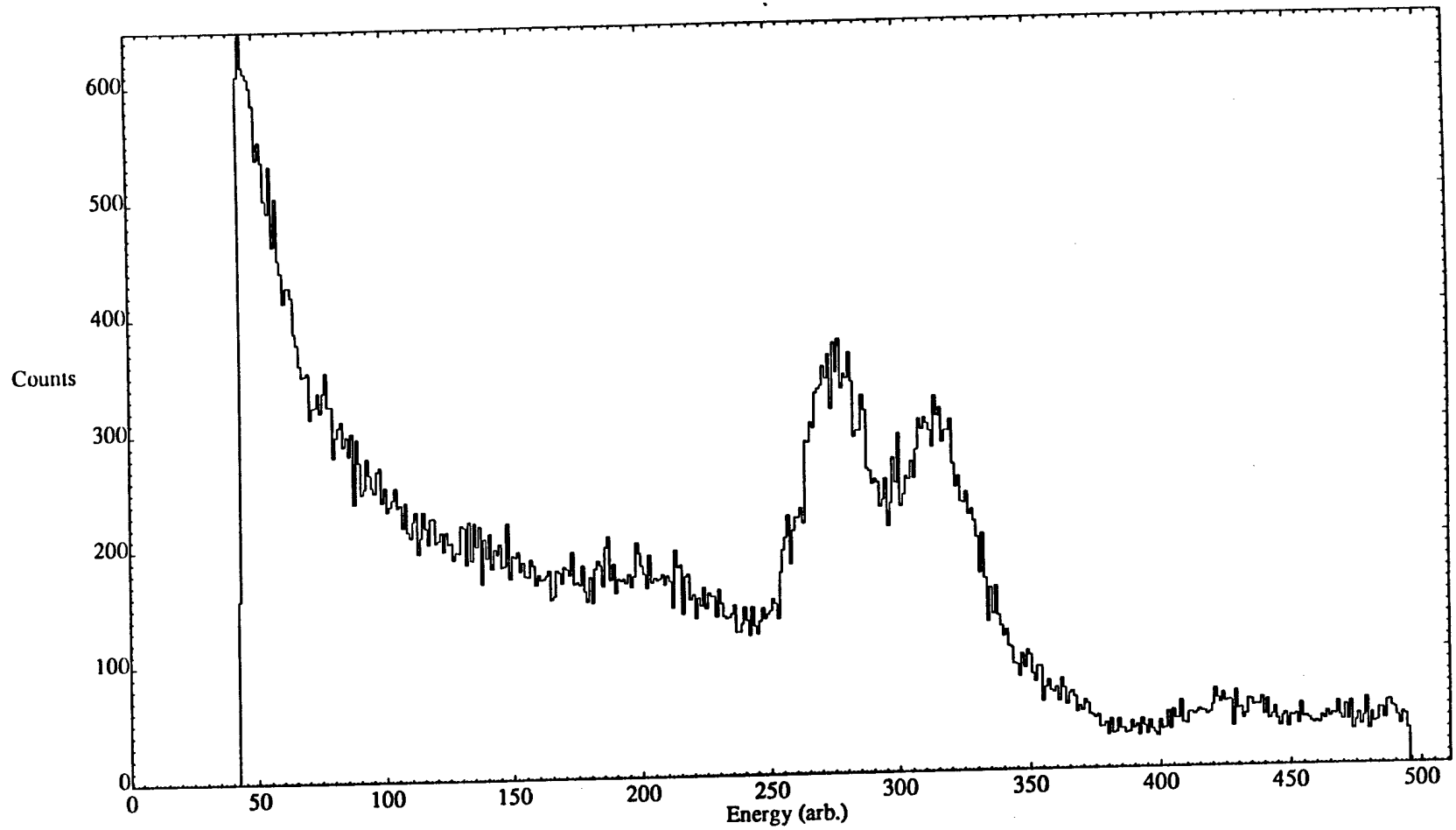


Fig. 11a. System response from a 60Co source using an ORTEC 113 preamplifier.

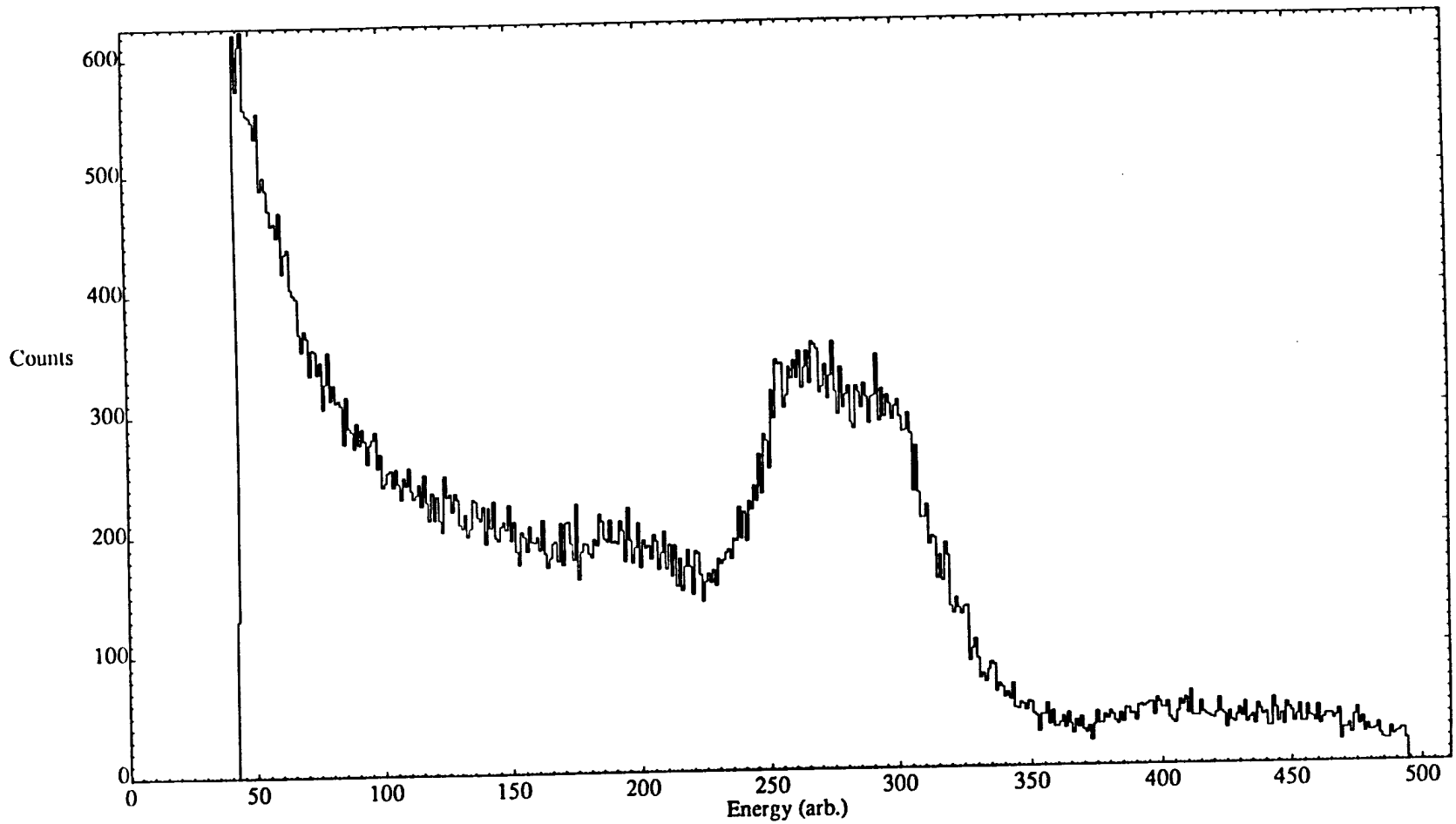


Fig. 11b. System response from a 60Co source using the baf2r1 test board.

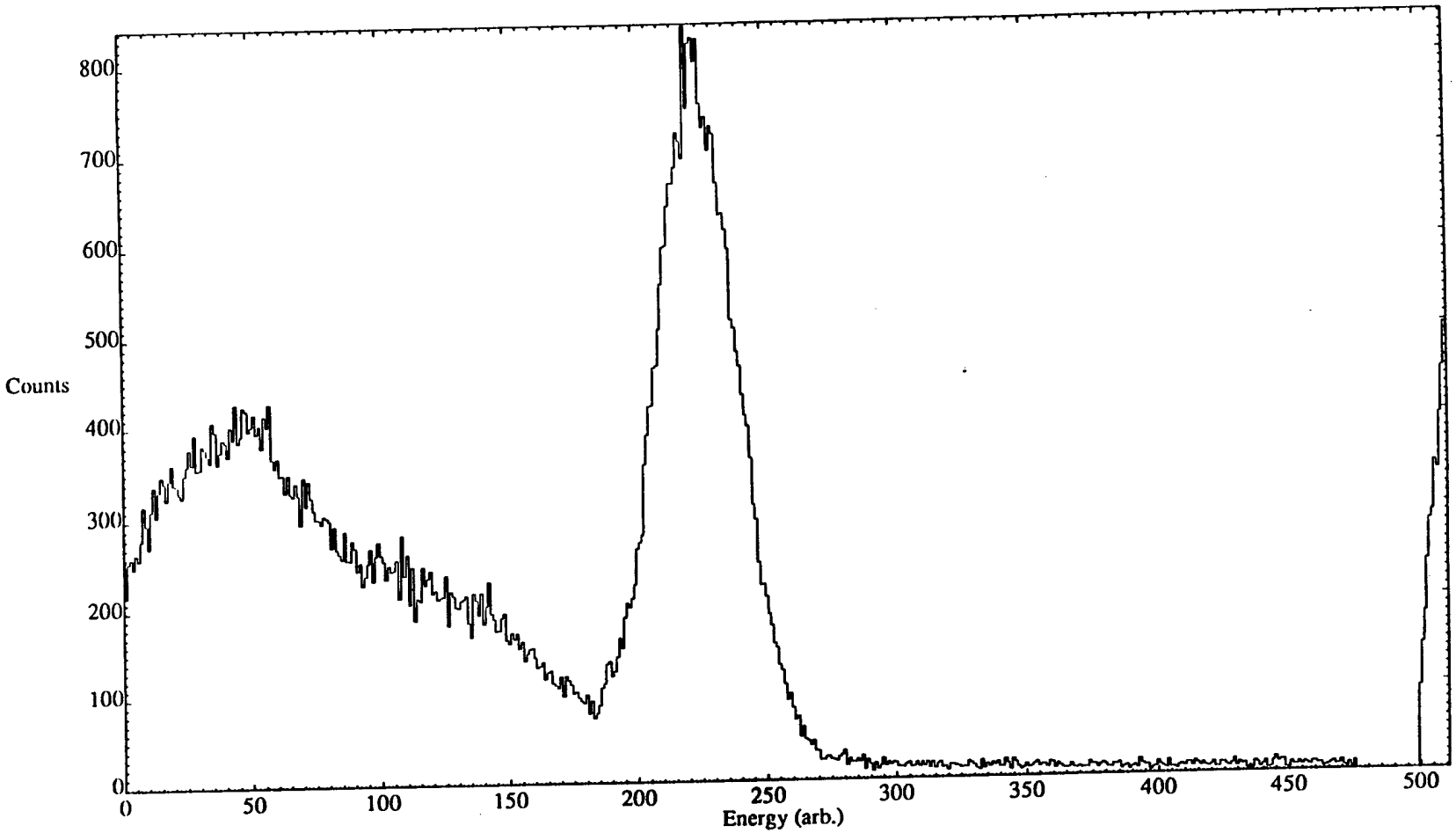


Fig. 12a. System response from a 137Cs source using an ORTEC 113 preamplifier.

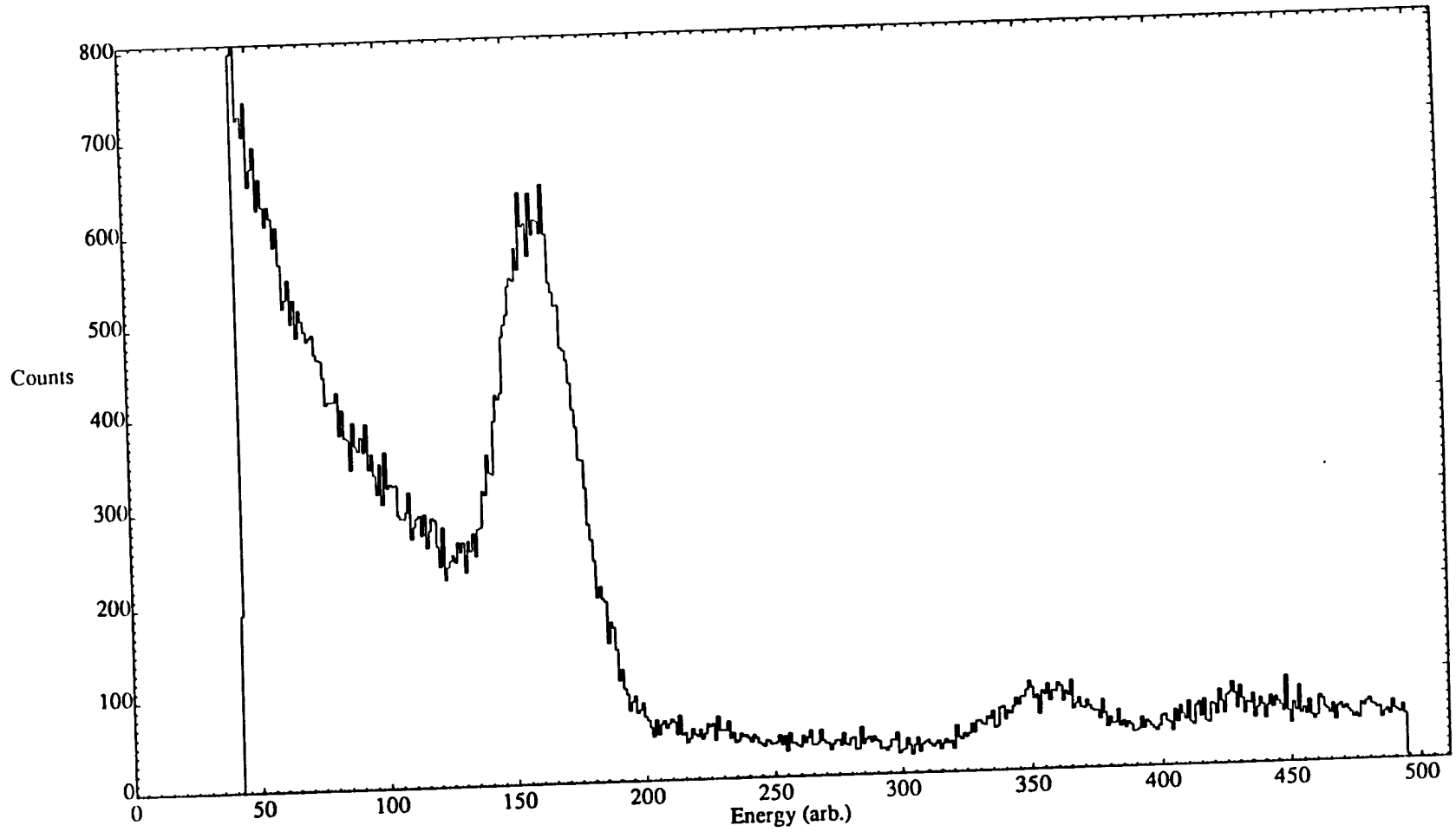


Fig. 12b. System response from a 137Cs source using the baf2r1 test board.

CONCLUSIONS

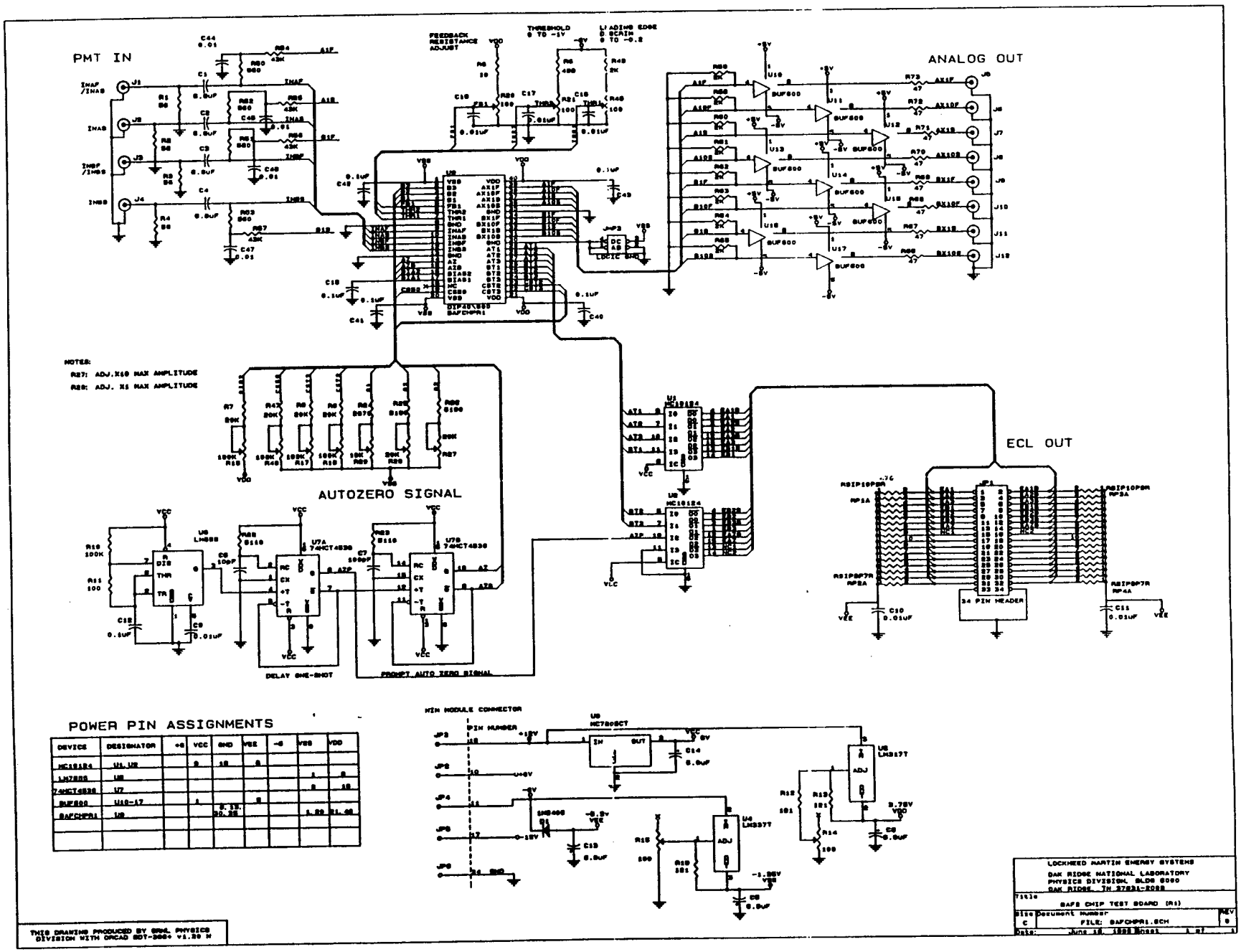
This Phase I research to examine the applicability of monolithic circuits to barium fluoride detectors used in nuclear physics experiments has resulted in the design, simulation, and prototyping of four CMOS integrated circuits. Test results have revealed a potential improvement in the processing of these signals as compared to the methods used in WA-98. The system topologies have been defined and many of the function blocks implemented in the first four chips.

Contacts have been made with researchers in the TAPS collaboration in Europe and that group of researchers is aware of and potentially interested in collaborating on any common elements of monolithic circuitry used in both experiments. We met with Dr. Rainer Novotny of the TAPS Collaboration at the onset of this project and have communicated with him on technical requirements.

The design of the baf2r1 integrator circuits is too noisy for the BaF_2 application intended. The device sizes used in the input amplifier function block can be modified for improved noise performance quite readily. Redesign of these integrator stages will also bring improvements in signal-to-noise using higher transconductance input devices resulting in a smaller Johnson noise voltage in future implementations. However, the overriding problem is in the circuit structure using a 50-ohm input resistance to ground with a 5-kΩ resistor then connected to the input summing node of the integrator. In essence, 99% of the signal current flows through the 50-Ω component and only 1% is applied to the integrator. A potential improvement of two orders of magnitude in signal-to-noise ratio is immediately possible by utilizing 100% of the anode current.

Appendix A

Schematic Diagram of baf2r1 Test Board



POWER PIN ASSIGNMENTS

DEVICE	DESIGNATOR	+6	VCC	GND	VEE	-6	VSS	VDD
MC10124	U1, U2		8	16	8			
LM7805	U8						1	8
74HCT4538	U7						8	16
BUF600	U10-17		4	8, 16, 20, 28	8			
SAFCHPR1	U9						1, 20	21, 40

THIS DRAWING PRODUCED BY ORNL PHYSICS DIVISION WITH ORCAD SDT-386+ V1.20 M

LOCKHEED MARTIN ENERGY SYSTEMS
OAK RIDGE NATIONAL LABORATORY
PHYSICS DIVISION, BLDG 6000
OAK RIDGE, TN 37831-6368

Title: SAFS CHIP TEST BOARD (R1)

Size: C | Document Number: FILE: SAFCHPR1.SCH | REV: 0

Date: June 18, 1998 | Sheet 1 of 1

Appendix B

Chip Photographs

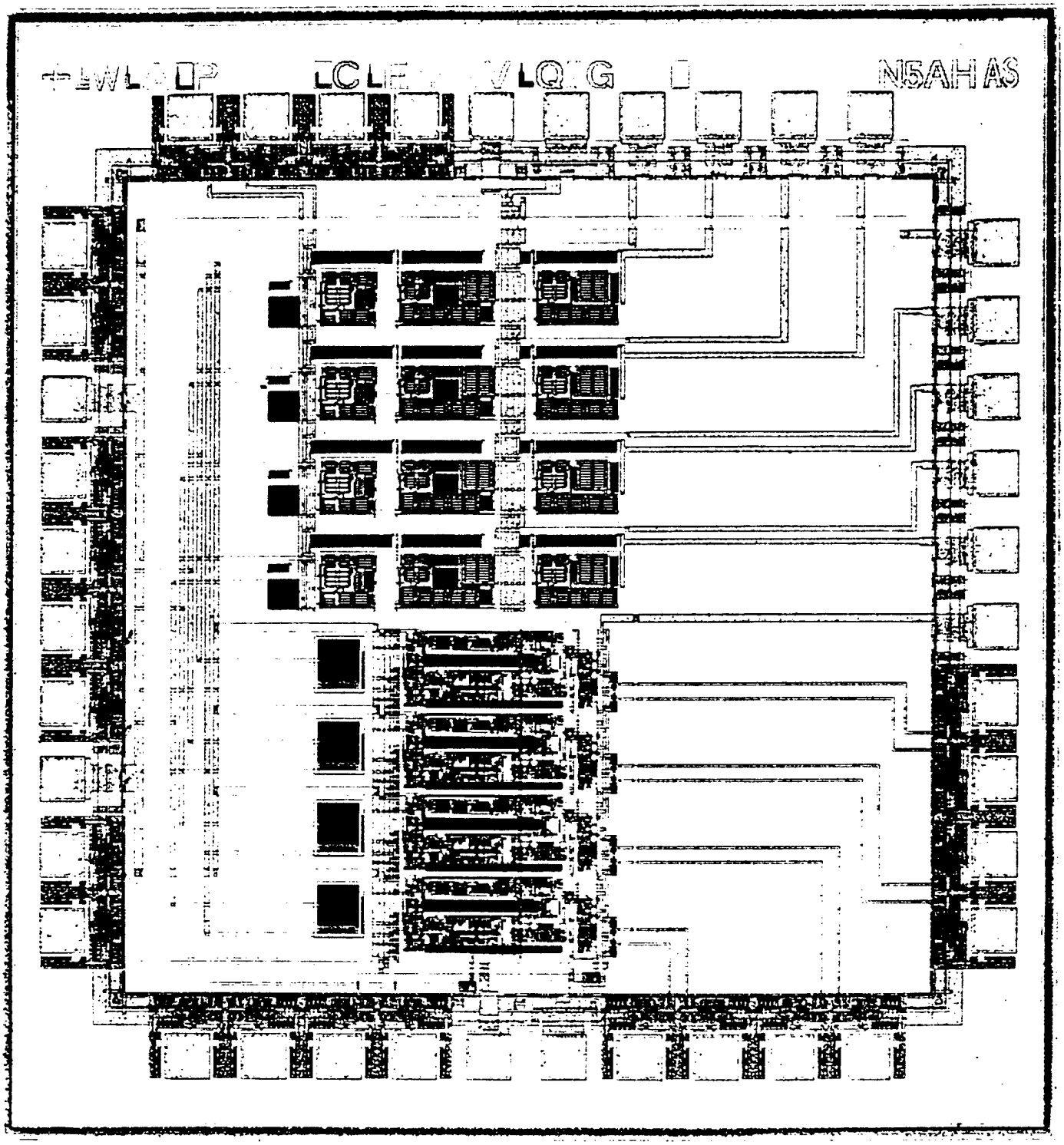


Fig. 13. Photograph of the *baf2chip*.

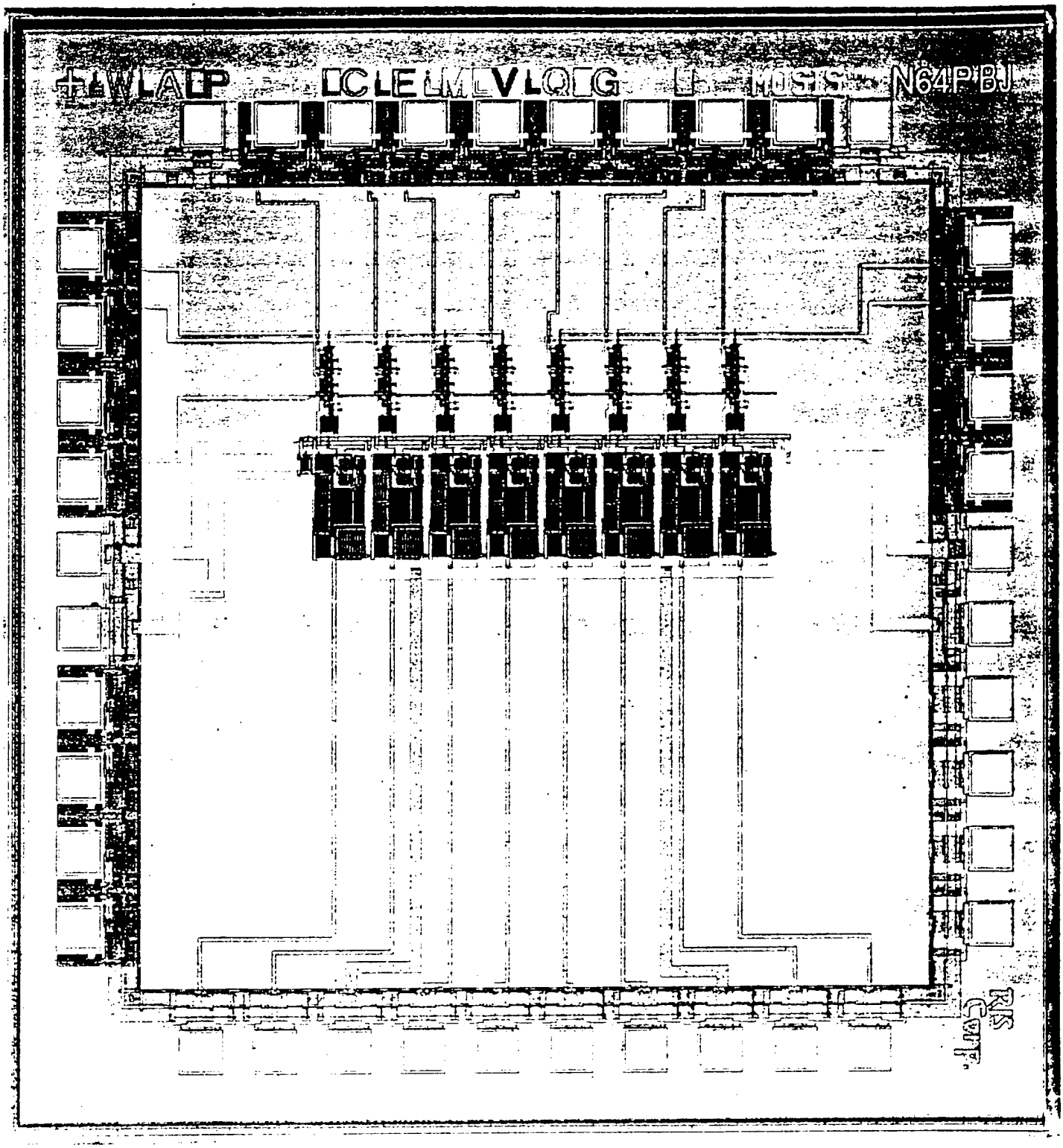


Fig. 14. Photograph of the *tac_chip*.

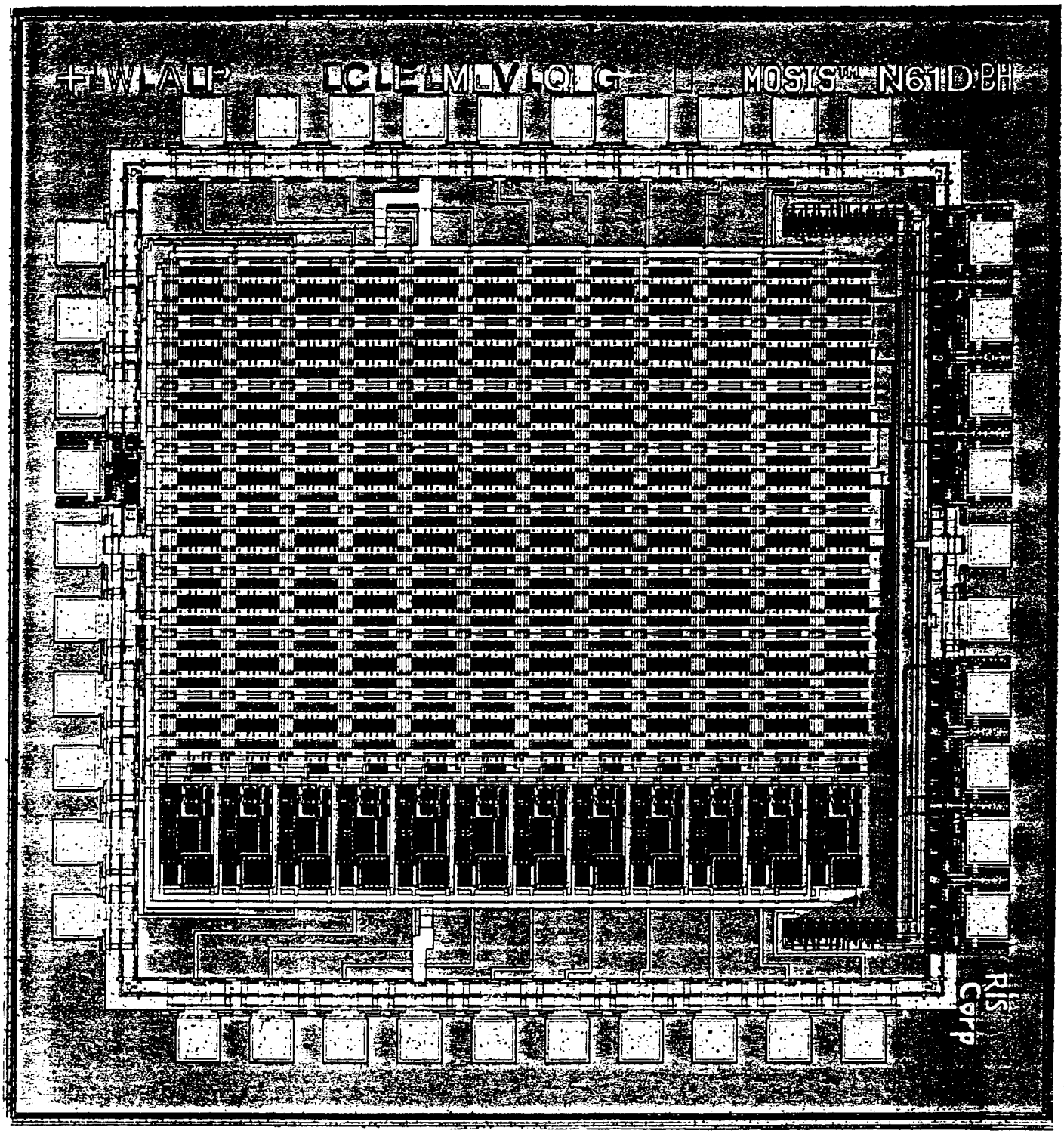


Fig. 15. Photograph of the *amu_chip*.

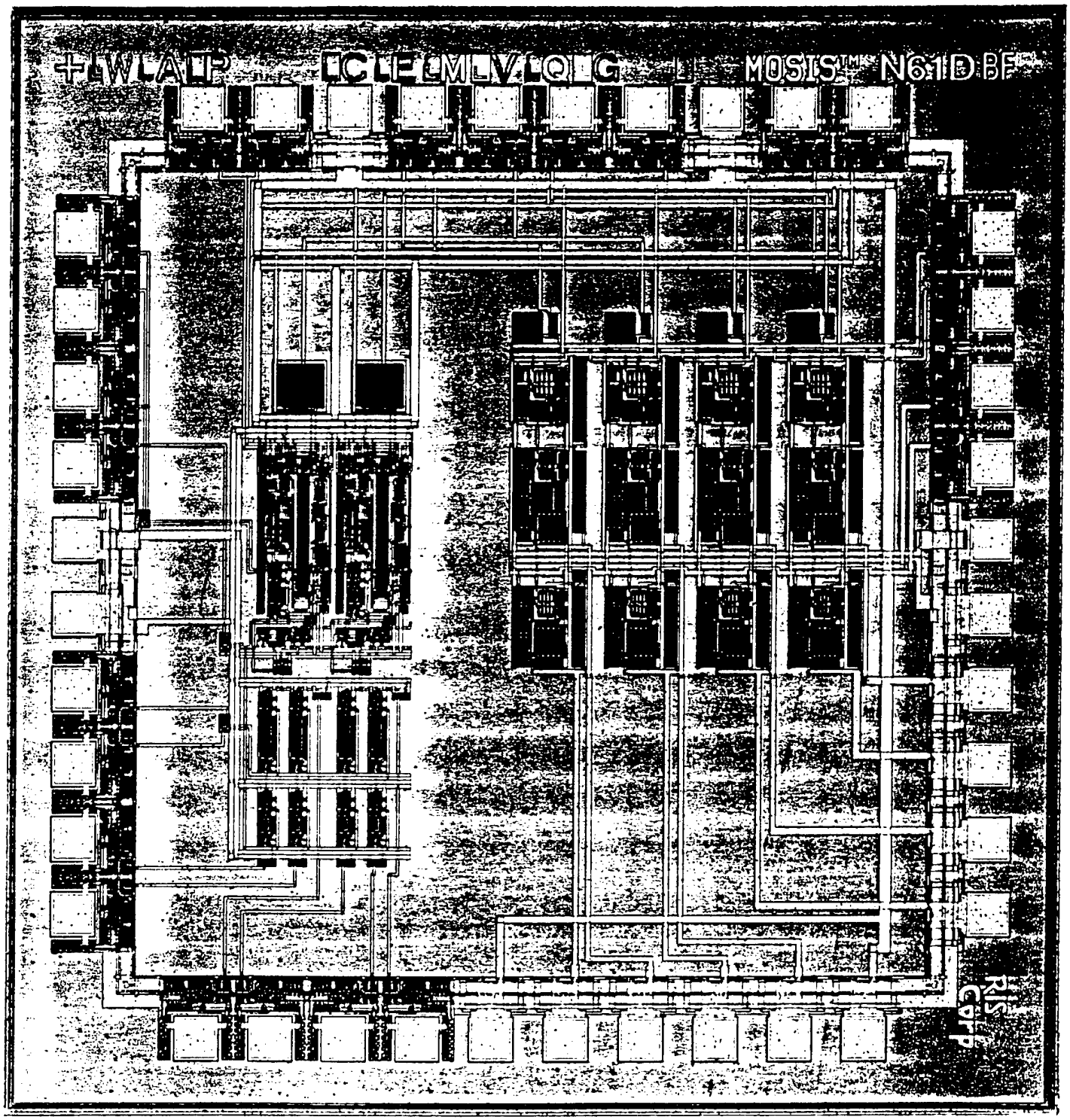


Fig. 16. Photograph of the *baf2r1* chip.

Appendix C

MOSIS Parametric Test Results
Bonding Diagram for *amu_chip*

MOSIS PARAMETRIC TEST RESULTS

RUN: N61D
TECHNOLOGY: SCN12

VENDOR: ORBIT
FEATURE SIZE: 1.2 microns

INTRODUCTION: This report contains the lot average results obtained by MOSIS from measurements of the MOSIS test structures on each wafer of this fabrication lot. The SPICE parameters obtained from similar measurements on a selected wafer are also attached.

COMMENTS: Orbit Semiconductor SCNA12.

TRANSISTOR PARAMETERS	W/L	N-CHANNEL	P-CHANNEL	UNITS
MINIMUM	1.8/1.2			
Vth		0.92	-0.95	Volts
SHORT	10.8/1.2			
Vth		0.85	-0.93	Volts
Vpt		15.0	-15.8	Volts
Vbkd		15.0	-15.9	Volts
Idss		208	-97	uA/um
WIDE	30/1.2			
Ids0		4.1	0.1	pA
LARGE	10.8/10.8			
Vth		0.94	-0.84	Volts
Vjbkd		15.5	-15.9	Volts
Ijlk		5.4	0.5	pA
Gamma		0.82	0.58	V^0.5
Delta length (L_eff = L_drawn-DL)		0.00	0.00	microns
Delta width (W_eff = W_drawn-DW)		0.00	0.00	microns
K' (Uo*Cox/2)		36.7	-12.7	uA/V^2

POLY2 TRANSISTORS	W/L	N-CHANNEL	P-CHANNEL	UNITS
MINIMUM	3.6/2.4			
Vth		1.03	-1.36	Volts
SHORT	7.2/2.4			
Vth		1.00	-1.33	Volts
LARGE	21.6/21.6			
Vth		0.97	-1.32	Volts
K' (Uo*Cox/2)		28.7	-9.7	uA/V^2

FOX TRANSISTORS	GATE	N+ACTIVE	P+ACTIVE	UNITS
Vth	Poly	>15.0	<-15.0	Volts

BIPOLAR PARAMETERS	W/L	NPN	UNITS
2X1	2X1		
Beta		132	
V_early		36.8	Volts
Vce,sat		0.2	Volts
2X2	2X2		
Beta		132	
V_early		34.9	Volts
Vce,sat		0.1	Volts
2X4	2X4		
Beta		130	
V_early		33.3	Volts
Vce,sat		0.1	Volts
2X8	2X8		
Beta		128	
V_early		32.1	Volts
Vce,sat		0.1	Volts
BVceo		---	Volts
BVcbo		28.9	Volts
BVebo		9.2	Volts

PROCESS PARAMETERS	N+DIFF	P+DIFF	POLY	POLY2	MTL1	MTL2	N_WELL	N\PLY	UNITS
Sheet Resistance	36.0	65.1	23.2	21.5	0.06	0.03	1358	1239	ohms/sq
Width Variation (measured - drawn)	0.14	-0.00	-0.20	-0.28	-0.20	-0.55			microns
Contact Resistance	41.7	135.3	12.7	12.6		0.05			ohms
Gate Oxide Thickness	239								angst.

COMMENTS: N\POLY is N-well under polysilicon.

CAPACITANCE PARAMETERS	N+DIFF	P+DIFF	POLY	POLY2	METAL1	METAL2	UNITS
Area (substrate)	487	433	66		38	17	aF/um^2
Area (poly)				470	60	26	aF/um^2
Area (poly2)					63		aF/um^2
Area (metal1)						37	aF/um^2
Area (N+active)			1442	1050	72	32	aF/um^2
Area (P+active)			1434	1047			aF/um^2
Fringe (substrate)	427	509			39	54	aF/um
Fringe (N+active)			31				aF/um
Fringe (P+active)			63				aF/um
Fringe (poly)					50	34	aF/um

CIRCUIT PARAMETERS			UNITS
Inverters	K		
Vinv	1.0	2.06	Volts
Vinv	1.5	2.26	Volts
Vol (100 uA)	2.0	0.38	Volts
Voh (100 uA)	2.0	4.48	Volts
Vinv	2.0	2.40	Volts
Gain	2.0	-17.02	
Ring Oscillator			
MOSIS (31-stage,5V)		55.13	MHz

N61D SPICE LEVEL3 PARAMETERS

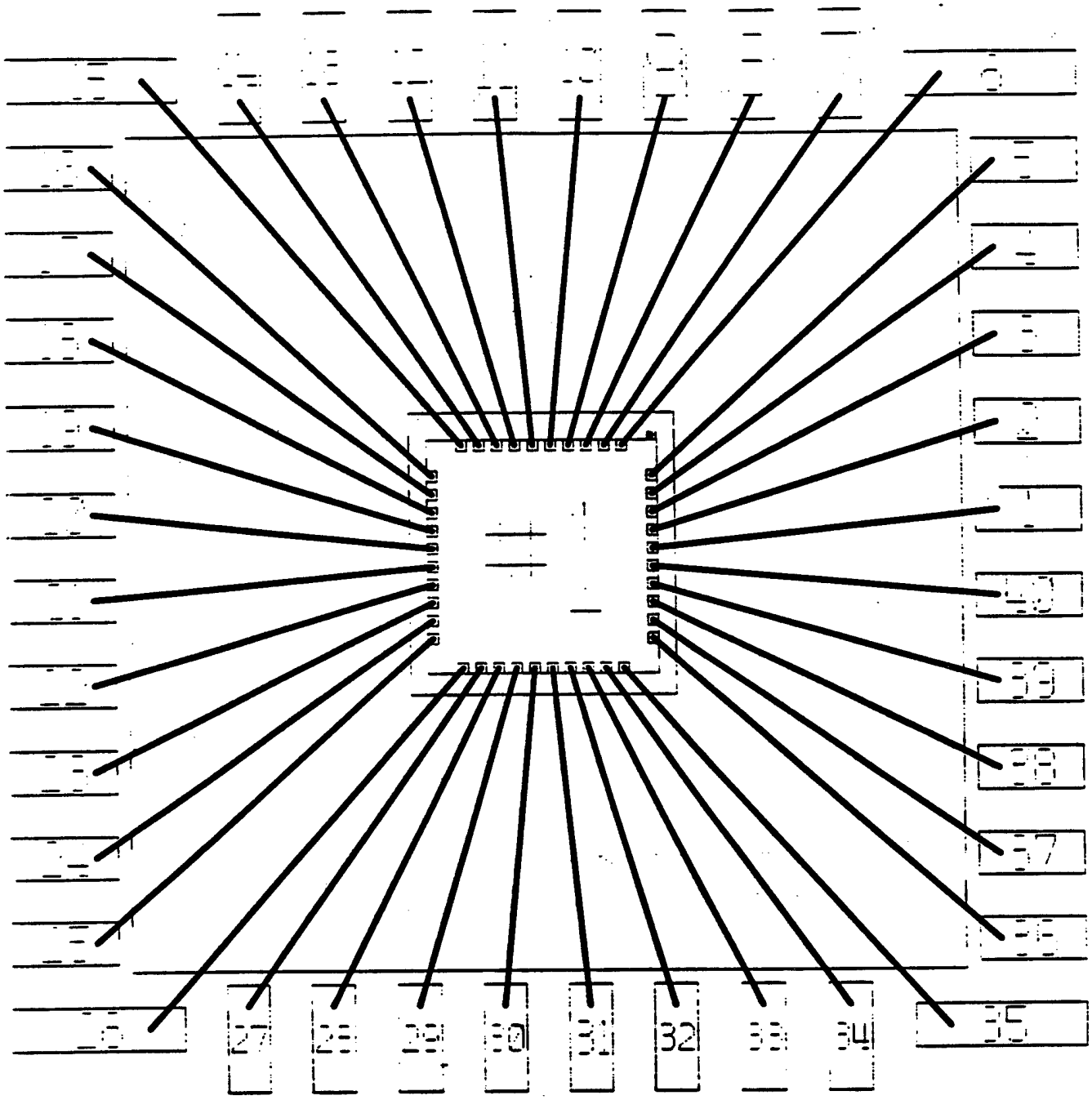
```
.MODEL CMOSN NMOS LEVEL=3 PHI=0.700000 TOX=2.3300E-08 XJ=0.200000U TPG=1
+ VTO=0.9286 DELTA=5.0960E-01 LD=1.0060E-09 KP=7.8281E-05
+ UO=528.2 THETA=8.7450E-02 RSH=6.4710E+01 GAMMA=0.9669
+ NSUB=6.1860E+16 NFS=5.9090E+11 VMAX=2.1530E+05 ETA=6.4490E-02
+ KAPPA=2.1440E-01 CGDO=2.2364E-10 CGSO=2.2364E-10
+ CGBO=2.6519E-10 CJ=4.24E-04 MJ=0.415 CJSW=7.89E-10
+ MJSW=0.524 PB=0.90
* Weff = Wdrawn - Delta_W
* The suggested Delta_W is 2.0000E-09
.MODEL CMOSP PMOS LEVEL=3 PHI=0.700000 TOX=2.3300E-08 XJ=0.200000U TPG=-1
+ VTO=-0.8647 DELTA=1.2060E+00 LD=9.3390E-10 KP=2.3742E-05
+ UO=160.2 THETA=7.6940E-02 RSH=3.1450E+02 GAMMA=0.4826
+ NSUB=1.5410E+16 NFS=7.1500E+11 VMAX=1.0260E+05 ETA=2.5210E-02
+ KAPPA=3.8690E+00 CGDO=2.0761E-10 CGSO=2.0761E-10
+ CGBO=2.6519E-10 CJ=3.84E-04 MJ=0.471 CJSW=8.08E-10
+ MJSW=0.413 PB=0.90
* Weff = Wdrawn - Delta_W
* The suggested Delta_W is 2.0000E-09
```

==========

N61D SPICE BSIM1 (Berkeley Level 4; HSPICE Level 13) PARAMETERS

```
NM1 PM1 DU1 DU2 ML1 ML2
*
*PROCESS=ORBIT
*RUN=n61d
*WAFER=01
*Gate-oxide thickness= 233 angstroms
*DATE=1-May-1996
*
*NMOS PARAMETERS
*
-8.59922E-01,-2.36515E-02, 7.84142E-02
 8.01704E-01, 0.00000E+00, 0.00000E+00
 1.14462E+00,-4.16409E-02, 1.94953E-02
 7.55041E-02, 2.30922E-02,-4.44841E-02
-3.59313E-03, 3.83416E-03, 1.51576E-03
 4.82214E+02,7.17420E-002,-1.74143E-001
 6.03686E-02, 1.18277E-01,-8.89839E-02
 2.30533E-02, 3.16754E-01,-4.09118E-02
 1.09271E+01,-2.04729E+01, 1.22035E+01
-1.98110E-04,-2.32745E-03,-2.99853E-03
 2.14355E-04, 3.58746E-04,-1.90108E-03
 2.95306E-03,-1.43989E-02, 6.27713E-03
-3.55797E-03,-2.95446E-03, 1.04138E-02
 4.91066E+02, 1.88769E+02,-3.10673E+00
 4.05140E+00,-2.59933E+01, 2.37579E+01
-1.18425E+00, 3.78951E+01,-7.04041E+00
 4.04278E-03, 3.72431E-02,-1.23680E-02
2.33000E-002, 2.70000E+01, 5.00000E+00
7.97432E-011,7.97432E-011,3.05969E-010
1.00000E+000,0.00000E+000,0.00000E+000
1.00000E+000,0.00000E+000,0.00000E+000
0.00000E+000,0.00000E+000,0.00000E+000
0.00000E+000,0.00000E+000,0.00000E+000
*
* Gate Oxide Thickness is 233 Angstroms
*
*
*PMOS PARAMETERS
*
-4.14077E-01, 3.87330E-01,-1.05142E-01
 7.06532E-01, 0.00000E+00, 0.00000E+00
 5.82676E-01,-2.91326E-01, 1.62737E-01
 5.27040E-03,-8.12134E-03, 4.75655E-03
-8.43609E-03, 3.10247E-02,-2.66251E-03
 1.79363E+02,-1.69825E-001,-1.13425E-001
 1.45840E-01, 6.63103E-02,-8.95823E-02
-1.41086E-02, 1.88193E-01, 2.00072E-02
 9.01668E+00,-3.01951E+00, 2.58643E+00
-8.90565E-04, 2.24760E-03,-5.74981E-03
 4.04294E-04, 2.64873E-04,-2.04038E-03
 7.65011E-03, 4.11718E-04,-2.09612E-03
 2.07099E-04,-3.20537E-04, 1.34303E-02
 1.89637E+02, 6.56670E+01, 1.38689E+01
 8.59408E+00,-7.34237E-01, 8.48262E+00
 2.65424E-01, 2.33396E+00,-4.14832E-02
-6.56420E-03,-1.76707E-02, 8.56354E-03
2.33000E-002, 2.70000E+01, 5.00000E+00
1.88765E-010,1.88765E-010,2.91509E-010
```

```
1.00000E+000,0.00000E+000,0.00000E+000
1.00000E+000,0.00000E+000,0.00000E+000
0.00000E+000,0.00000E+000,0.00000E+000
0.00000E+000,0.00000E+000,0.00000E+000
*
*N+ diffusion::
*
36,     4.2400e-04,     7.89e-10,     1e-08,     0.90
0.90,     0.415,     0.524,     0,     0
*
*P+ diffusion::
*
65.1,     3.84e-04,     8.08e-10,     1e-08,     0.90
0.90,     0.471,     0.413,     0,     0
*
*METAL LAYER -- 1
*
0.06,     2.6e-05,     0,     0,     0
0,     0,     0,     0,     0
*
*METAL LAYER -- 2
*
0.03,     1.3e-05,     0,     0,     0
0,     0,     0,     0,     0
```



NE10EH 2

144E-COMPATIBLE

PERIPHERALS EMULATOR

PIN OUT SHEETS

1-FEB-1996

DISTRIBUTION

1. S. Peter Rosen, Associate Director for High Energy and Nuclear Physics, Office of Energy Research, U.S. Department of Energy, Germantown, Maryland 20874-1290

2-3. Office of Scientific and Technical Information, P. O. Box 62, Oak Ridge, Tennessee 37831

4. Department of Energy-Work for Others

5. J. R. Beene

6. J. L. Blankenship

7. D. R. Hamrin, Laboratory Records - RC

8. Pam Gorman, ORNL Site Office

9. A. J. Luffman, Office of Science and Technology Partnerships

10-12. R. A. Todd, RIS Corp., 1345 Oak Ridge Turnpike, Suite 324, Oak Ridge, Tennessee 37832

13. C. A. Valentine, Office of Technology Transfer Business Office

14. R. L. Varner

Report Number (14) ORNL/M--6390

Publ. Date (11) 199802

Sponsor Code (18) DOE/ER, XF

UC Category (19) UC-400, DOE/ER