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Trigger Circuits for the PHENIX Electromagnetic Calorimeter *

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DISCLAIMER

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Abstract

Monolithic and discrete circuits have been developed to provide trigger signals for the PHENIX electromagnetic calorimeter detector. These trigger circuits are deadtimeless and create overlapping 4 by 4 energy sums, a cosmic muon trigger, and a 144 channel energy sum. The front end electronics of the PHENIX system sample the energy and timing channels at each bunch crossing (BC) but it is not known immediately if this data is of interest. The information from the trigger circuits is used to determine if the data collected is of interest and should be digitized and stored or discarded. This paper presents details of the design, issues affecting circuit performance, characterization of prototypes fabricated in 1.2 μm Orbit CMOS, and integration of the circuits into the EMCal electronics system.

I. INTRODUCTION

The PHENIX Electromagnetic Calorimeter (EMCal) is composed of a lead-scintillator calorimeter (PbSc) consisting of approximately 15,000 channels and a lead glass calorimeter (PbGl) which approximately 10,000 channels. The energy and timing channels are sampled by the front end module (FEM) at every bunch crossing (BC) (~106ns). This results in too much data to be digitized and archived, so only data of interest can be stored and the rest is overwritten. It is not possible to know beforehand if the data of the forthcoming BC will be of interest. This requires the data to be temporarily stored in fast analog memory units (AMUs) or digital memory units (DMUs) until the level-1 trigger logic (LVL-1) can decide if this data is of interest. Fast analog trigger circuits are needed to create analog sums and provide information to LVL-1 so that this decision can be made quickly [1]. The trigger circuits presented in this paper are based on preliminary work done for the WA98 lead glass calorimeter.[2]

A front end module (FEM) contains 144 channels of electronics that consists of a printed circuit board backplane with ten printed circuit boards (daughter cards) plugged in to the backplane. There are six ASIC cards, a trigger sum card, a heap manager card, a serial card, and a data output card. The ASIC cards have 24 channels of energy and timing electronics contained in six ASICs and the AMUs. The trigger sum card collects the summing data from the ASIC cards and sends this data to LVL-1. The heap manager controls the AMUs and contains the state machine for the ADCs on the ASIC cards. The data output cards formats the data from the ADCs and sends this data to the data collection module (DCM). The serial card is responsible for setting up the ASICs, DACs, and other programmable components on the other daughter cards.

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II. SYSTEM DESCRIPTION

A. Trigger Summing Scheme

The trigger tower summing scheme shown in Fig. 1 generates 2x2 sums that completely cover the detector and also generates overlapping 4x4 sums. A tower is composed of one scintillator, a photomultiplier tube and associated electronics. A 2x2 sum is the sum of the energy from four of these towers. The overlapping 4x4 sums are needed to increase efficiency of the detector. If an event of interest occurred and particles hit the detector at the boundary of four 2x2 sums, each 2x2 sum would have a small fraction of the total energy and it would look as if the event was not of interest. The overlapping 4x4 sums prevent this from happening. Each 2x2 sum is an index for a 4x4 sum. The 2x2 sum that is the lower-left element of a

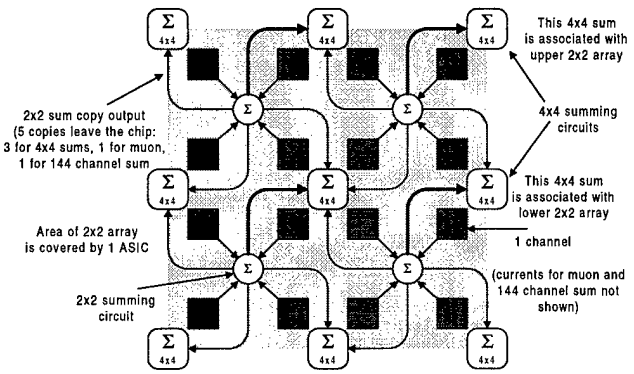

Figure 1. Trigger sum concept

4x4 sum is the "owner" of the 4x4 sum. When a 2x2 sum is formed, six copies of the signal are made. One of the copies is kept on chip to make its own 4x4 sum, three are sent to adjacent chips, one is used on chip for the cosmic muon trigger, and one is used to generate a 144 channel sum. A 2x2 sum is combined with three other 2x2 sums from adjacent chips to generate the 4x4 sum. Each 2x2 sum signal is used in forming four 4x4 sums.

B. 2x2 Sum Formation

An FEM processes signals from a 12 by 12 array (144 channels) of photomultiplier tubes. The signal from the PMTs in the detector are input to a discrete passive integrator. The resultant voltage is then amplified with a variable gain amplifier (VGA) that has adjustable gain and compensation. The VGA is used to equalize the gains of the multiple

photomultipliers.[3] This signal is then input to the 2x2 summing circuit shown in Fig. 2. The integrators are designed for a maximum four channel input of 250pc (~5GeV). The inputs to each channel of the trigger circuits are equipped with switches that can disable that channel by connecting the input to ground in the event of a faulty channel. There are alternating integrating units for generation of the 2x2 sums so

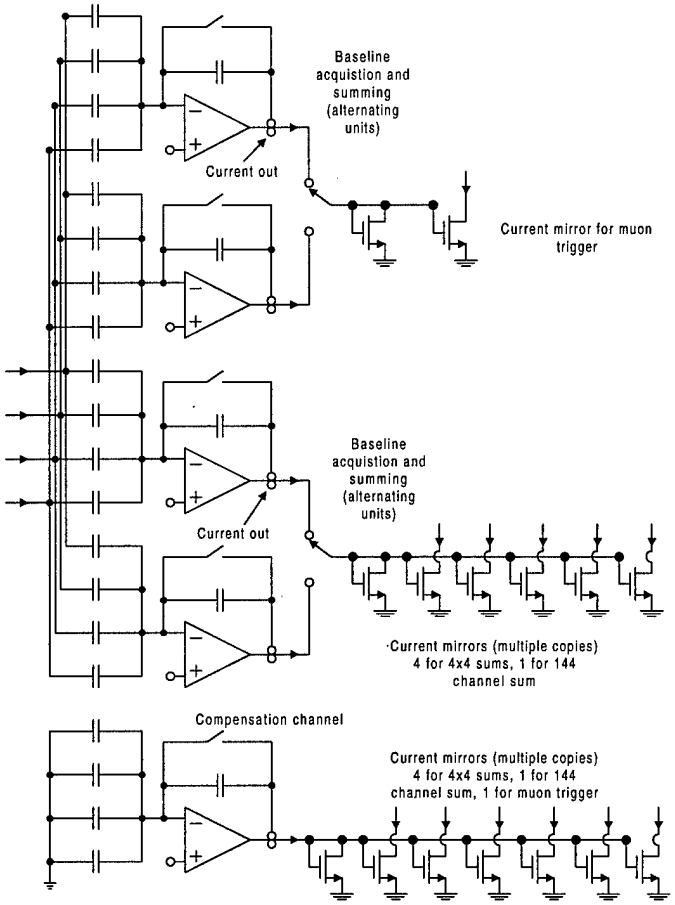

Figure 2. 2x2 current mode sum formation and copying

that the trigger circuits can be live for each BC. While one integrator is active, the other is acquiring baseline and the switching between integrators is synchronized with the BC. The signal is then converted to a current and multiple copies are made. The trigger signals must be routed across several printed circuit boards and they are connected to other backplanes using twisted pair cable. The resulting high capacitance and high probability of noise and crosstalk makes routing the signal as a voltage difficult. Making multiple copies of the trigger signals is also much easier in current mode. The current has a DC component of 1mA and is designed for a maximum 2x2 signal of 1mA which gives maximum current of 2mA for a maximum signal on one channel. Multiple copies of this current are made using current mirrors. Three of the 4x4 current sums must either go off the chip, on to the backplane and back on to another chip, or they are routed on to the backplane or they are connected to adjacent backplanes using 1m of twisted pair cable. This results in slow 4x4 sum formation due to the long signal routes and large parasitic capacitance. For this reason, the 2x2 sums are doubled resulting in a 2mA DC component and a 4 mA maximum.

The cosmic muon trigger must process much lower signal levels than the 4x4 sums. To reduce the dynamic range requirements of the integrators, another pair of alternating amplifiers with higher gain was added.

When a 4x4 sum is created, the DC component would be 8mA (4 x 2mA) and the maximum signal is 2mA. The compensation channel show in Fig. 2 is used to generate a DC current to subtract most of DC component from the 4x4 sum. The compensation channel is similar to the 2x2 summing channel. The inputs are grounded and the DC current is set to 90% of the DC current in the 2x2 summing channel. The compensation currents must be smaller than the DC currents in the 2x2 summing channels so that process variations could not cause the compensation currents to be larger than the DC component in the 2x2 currents and result in a negative baseline.

C. 4x4 Sum Formation

The 4x4 sum is formed using a diode-connected MOSFET as shown in Fig. 3. Signal currents and compensation currents are input from four separate chips where they are combined and converted to a voltage. A larger voltage is obtained using a

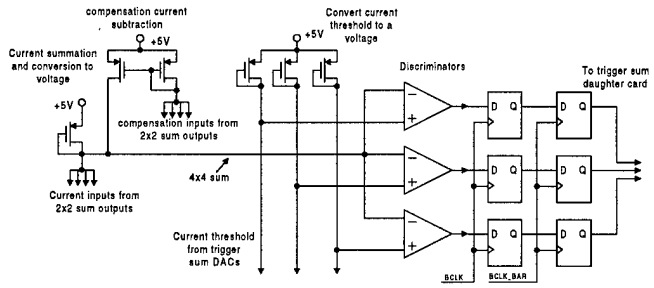

Figure 3. 4x4 sum formation and encoding

MOSFET with a smaller W/L but the resulting high resistance gives rise to speed issues which required the use of a larger W/L. The compensation current sum is mirrored and subtracted from the signal sum. Encoding of the 4x4 sum is accomplished with three current threshold discriminators. The current thresholds enable a linear adjustment of the threshold levels. The thresholds are set by three 6-bit current DACs. The 4x4 sum is linear to 400pC (8GeV) and the maximum threshold is 250pC (5GeV). At each BC the output of the discriminators are clocked into a register and sent off chip to the trigger sum daughter card. The muon bit formation, shown in Fig. 4, is similar to the 4x4 sum. There is a single current threshold that is set by a 6-bit DAC with the minimum threshold being <40MeV.

D. *144 Channel Sum Formation*

On each ASIC card a 24-channel signal current sum and a 24-channel compensation current sum is formed using discrete circuitry. These are the first two amplifiers shown in Fig. 5. On each FEM there are six 24-channel voltage sums that are input to the trigger sum daughter card to generate a 144-channel sum. An additional amplifier stage is needed to adjust for offsets due to process variations in the monolithic trigger

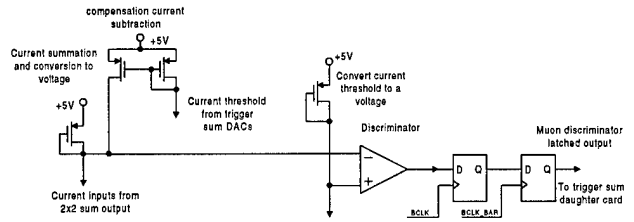

Figure 4. Muon bit formation

circuitry. This offset adjustment is accomplished using a 12-bit voltage DAC. The 144-channel energy sum is then digitized using an 8-bit 10 Mhz FADC. The 144 channel sum is designed to have a range of 0 to 25GeV so the resolution of the digitized sum is ~100MeV/bit. This information is used to generate a global sum representative of the total energy measured in the EMCal detector.

Two FPGAs are used as a data latch, buffer, and cosmic muon logic. The FPGAs latch the 8 bits for the 144-channel

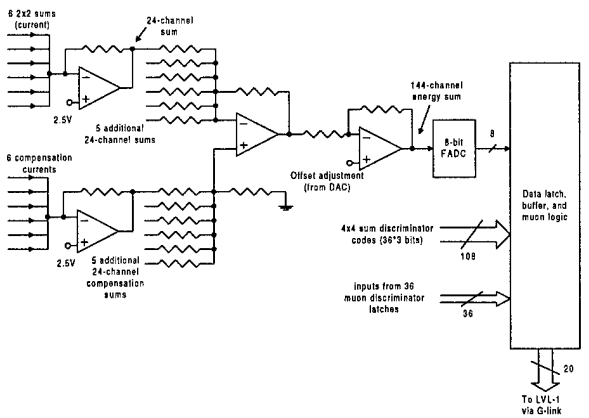

Figure 5. 144 channel sum formation

energy sum, the 108 bits from the 4x4 sums (36 * 3 bits) and the 36 bits from the muon discriminators. A programmable threshold is set for the muon logic and if the number of logic highs in the 36 muon bits exceeds the threshold, then a single muon bit is set high and sent to LVL-1. This trigger allows the use of cosmic muons to calibrate the detector. As shown in

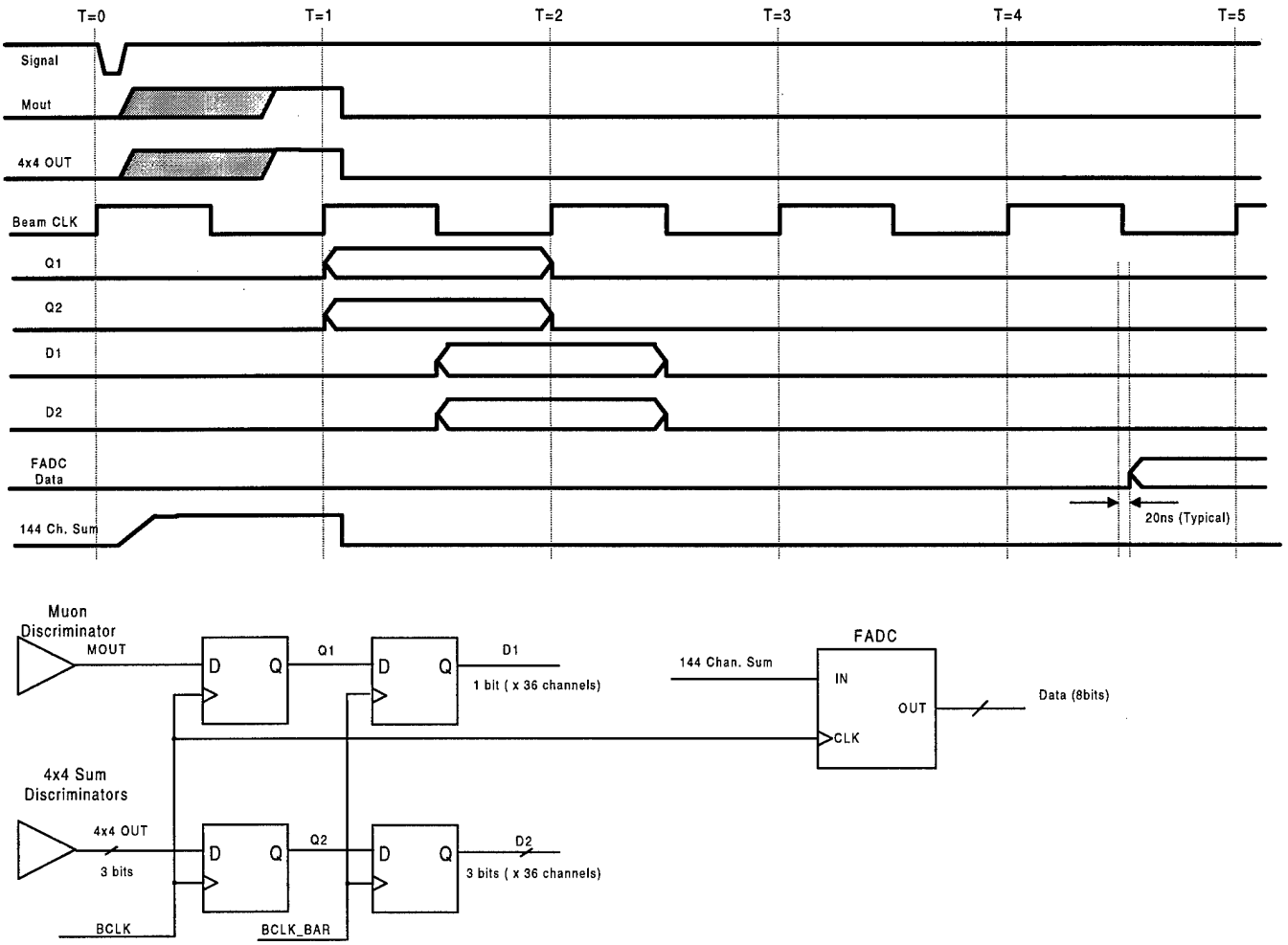

Figure 6. Trigger sum data timing diagram

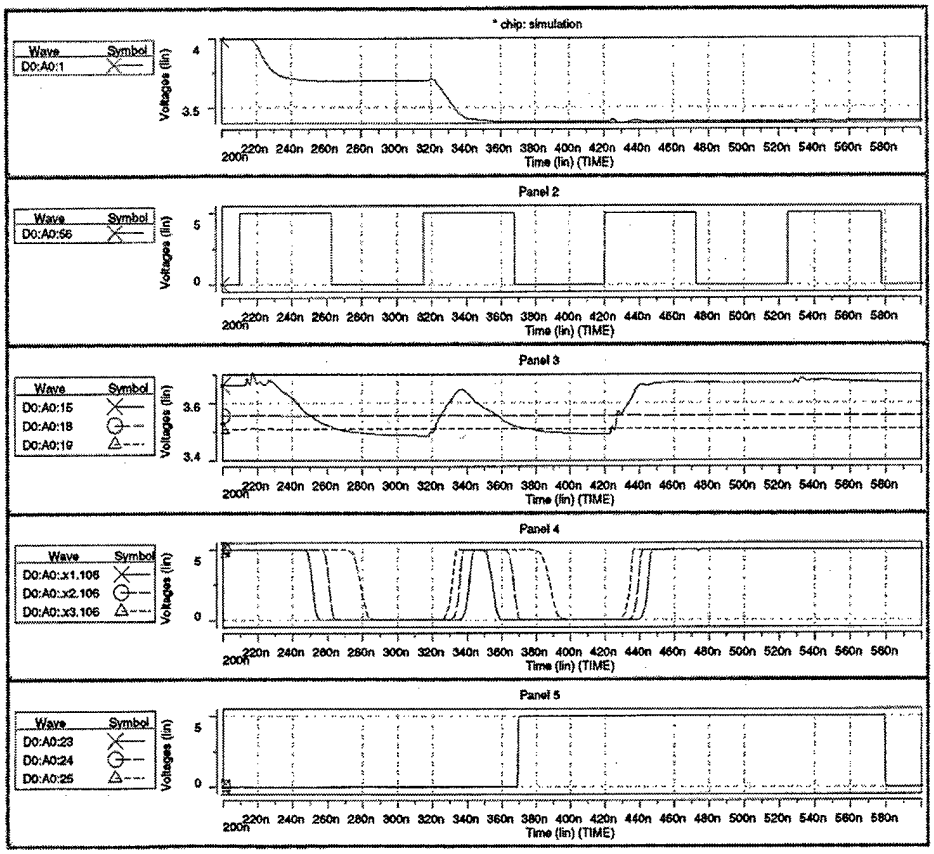

Figure 7. Monolithic trigger circuitry simulation

Fig. 6, the three sets of data do not arrive at the FPGAs at the same time, so the FPGA aligns the data to be sent to LVL-1. For each BC, a total of 117 bits must be sent to LVL-1 in 20 bit packets. This requires a 60 Mhz clock which is generated from the BC on the trigger sum daughter card using a PLL circuit.

III. RESULTS

Care was taken in the layout of the monolithic circuits to minimize clock noise on the analog sums while keeping area at a minimum. The smallest signal levels are at the inputs so all clock lines were routed away from this area. The switches for acquiring baseline and switching between the integrators are a source for charge injection so they were made as small as possible without sacrificing speed. To further minimize clock noise problems, several bypass capacitors were placed throughout the layout.

The most difficult requirement for the trigger circuitry was to make it live for every BC. The simulations of the 4x4 sum generation is shown in Fig. 7. The top panel is the trigger sum input from the VGA on two successive BC. Each signal corresponds to approximately 3 GeV. The 10 Mhz BC is shown in panel 2. Panel 3 shows the 4x4 sum after the compensation currents have been subtracted and converted to a voltage. The three thresholds are also shown. The output of the comparators are shown in panel 4. The comparators respond in approximately 10ns. The latched comparator outputs are shown in panel 6. There is a two BC delay from the time the signal arrives to when the trigger circuits provide the encoded 4x4 sums to the trigger sum daughter card.

The layout of the monolithic trigger circuitry is shown in Fig. 8. The circuits were fabricated in the Orbit 1.2 μm

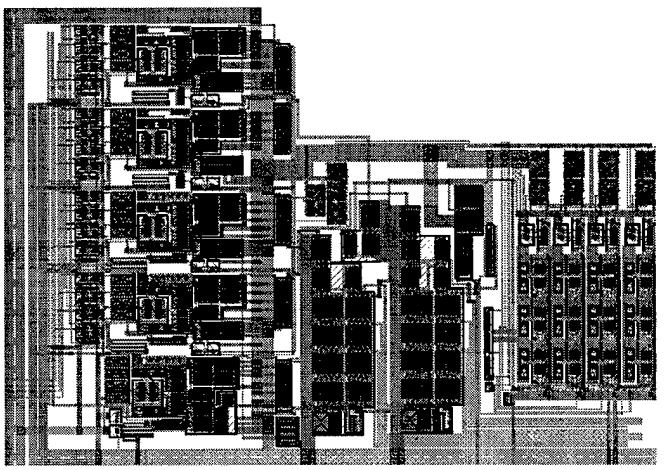

Figure 8. Monolithic trigger circuitry layout in 1.2 μm CMOS

CMOS N-well process. The circuit size is 962 μm x 1376 μm. The power DC power consumption is 160 mW.

IV. CONCLUSION

A prototype was fabricated in the Orbit 1.2 μm CMOS N-well process. The ASIC was tested and was fully functional but exhibited problems with clock interference and charge injection from the CMOS switches. Necessary layout changes

were made and the circuit was resubmitted. The circuits are presently being fabricated and will be tested upon arrival.

V. REFERENCES

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