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Summary

The overall mission of the Institute of Energy Conversion is the development of thin film photovoltaic cells, modules, and related manufacturing technology and the education of students and professionals in photovoltaic technology. The objectives of this four-year NREL subcontract are to advance the state of the art and the acceptance of thin film PV modules in the areas of improved technology for thin film deposition, device fabrication, and material and device characterization and modeling, relating to solar cells based on $CuInSe_2$ and its alloys, on a-Si and its alloys, and on CdTe.

$CuInSe_2$-based Solar Cells

High Bandgap $CuInSe_2$ Alloys

$CuInSe_2$ has a bandgap of 1.0 eV and most $Cu(InGa)Se_2$-based devices have absorber layers with $Ga/(In+Ga) \approx 0.25$ which gives a bandgap of 1.15 eV and results in devices with open circuit voltages < 0.65V. Higher Ga concentrations to increase the $Cu(InGa)Se_2$ bandgap result in a trade-off of higher open circuit voltage and lower short circuit current which may allow increased cell efficiency. Further, module performance should be improved due to lower resistive losses, thinner ZnO with less optical loss and/or greater interconnect spacing with reduced associated area-related losses.

We have previously demonstrated $Cu(InGa)Se_2$ solar cells with 15% efficiency for $Ga/(In+Ga) \leq 0.5$ or bandgap (Eg) ≤ 1.3 eV [101, 102]. With higher bandgap a decrease in cell efficiency was shown to be caused by poor collection of light generated minority carriers in the $Cu(InGa)Se_2$ absorber layers and in this report, we have expanded the characterization of $Cu(InGa)Se_2$ devices with increasing Ga content and bandgap. Further, we have begun to investigate other $CuInSe_2$-based alloy materials, $CuInS_2$ and $Cu(InAl)Se_2$, which may provide alternative means to achieve improved device performance with Eg > 1.3 eV.

Reduced $Cu(InGa)Se_2$ Deposition Temperature and Thickness

There are many technical issues which need to be addressed to effectively enable the transfer of $Cu(InGa)Se_2$ deposition and device fabrication technology from the laboratory to manufacturing scale. In general, these issues provide a means to reduce thin film semiconductor process costs. Shorter deposition time can be achieved with reduced film thickness and increased deposition rate. Thinner absorber films reduce the total amount of material used and allow faster process throughput. The minimum thickness of the $Cu(InGa)Se_2$ absorber layer may be determined by the nucleation of the film to form a continuous layer or by the film morphology. From a device perspective, the minimum thickness may be determined by the minority carrier diffusion length and optical absorption coefficient of the $Cu(InGa)Se_2$ or the ability to incorporate optical confinement.

Lower substrate temperature (T_{ss}) can lower processing costs by reducing thermally induced stress on the substrate, allowing faster heat-up and cool-down, and decreasing the heat load and stress on the entire deposition system. In addition, with lower substrate temperature, stress on the glass substrate can be reduced and alternative substrate materials, like a flexible polymer web, could be utilized.

We have addressed the need to improve process throughput by reducing the $Cu(InGa)Se_2$ thickness and deposition temperature. The approach during this work has been to first define a baseline process for $Cu(InGa)Se_2$ deposition by multisource elemental evaporation and solar cell fabrication. All other deposition parameters are then held fixed to determine the effects of varying either the substrate temperature or, by changing the deposition time, film thickness. Material

properties of the resulting Cu(InGa)Se_2 films have been characterized and their device behavior has been measured and analyzed.

Team Participation

IEC is a member of the National CIS Team under the NREL Thin Film Partnership Program. The CIS Team effort includes four working groups (WG). Of these, IEC has been a member of the Transient Effects WG and the New Junction WG, for which William Shafarman is the Group Leader.

New Junction

The New Junction WG has identified two tasks and IEC has contributed to work on each. The objective of the first task is to develop non-cadmium containing buffer layers. The priority is on vacuum processes which could potentially be incorporated in-line, and chemical bath deposition is not considered a primary option. The objective of the second task is to develop improved TCO layers to minimize losses for module fabrication and quantify the effect of TCO layers on module performance. This task is focusing on the high conductivity TCO layers.

Transient Effects

The $CuInSe_2$ thin film partnership program organized a transient effects team to determine if present I-V testing procedures can predict the daily output of $CuInSe_2$-based modules and cells under field conditions; and, if they cannot, to determine what new testing procedures are needed.

a-Si:H-based Solar Cells

The focus of a-Si research was on contacts and interfaces. This work was motivated by results from the previous year which showed that the electrical behavior of the n-layer/TCO contact was critical to incorporating a high performance TCO/Ag back reflector and achieving efficiencies over 10%.

Current-Voltage Characterization of TCO Contacts

We investigated the current-voltage-temperature dependence of the following contacts, where TCO refers to sputtered ITO or ZnO: TCO/a-Si i-layer, TCO/a-Si n-layer, TCO/µc-Si n-layer, textured SnO_2/a-Si n-layer and textured SnO_2/µc-Si n-layer. Regarding the contact between sputtered TCO and a-Si i-layers, ITO has a larger barrier compared to ZnO. Thus, ITO makes a better junction, hence poorer Ohmic contact, with a-Si i-layers. Also, sputtering ZnO in Ar/O_2 gives a higher barrier and more blocking contact with a-Si compared to sputtering ZnO in Ar or Ar/H_2. Thus, the barrier between ZnO and a-Si depends on the ZnO sputtering conditions. It is not known if this is an interfacial or bulk effect. Regarding the contact between sputtered TCO and a-Si or µc-Si n-layers, it was found that the µc-Si n-layers have nearly-Ohmic behavior with ITO, ZnO or SnO_2 contacts at $T > 25^{\circ}C$ unlike a-Si n-layers. The µc-Si n-layers have lower contact resistance than a-Si n-layers. JV behavior at $T > 25°C$ with the a-Si or µc-Si n-layers was nearly independent of the various sputtered TCO contacts. We found that the a-Si n/SnO_2 contact is more blocking at $T < 25°C$ than is the µc-Si n/SnO_2 contact. Thus, µc-Si n-layers are essential for good Ohmic contacts to TCO for either top or bottom contacts. Their high conductivity allows the decoupling of the electrical requirements for the contact from the optical requirements, and allows the device to achieve full benefit of an optical back reflector or other transparent contact without any additional electrical losses.

We also investigated the contact between the p-layer and various glass/TCO substrates for superstrate p-i-n cells as part of our on-going study of ZnO/p contacts and ZnO substrates in collaboration with R. Gordon at Harvard University. It was found that a new process for APCVD ZnO yields much better device performance than previous APCVD ZnO material, and that straightforward changes to the deposition of the p-layer, such as increasing the B dopant flow can give significant improvements in FF and V_{oc} of ZnO/p-i-n devices.

Effect of Interface on V_{oc}

In an effort to improve the stabilized V_{oc}, we attempted to duplicate studies from Penn State, NREL and elsewhere by modifying the initially deposited i-layer to include either hydrogen dilution or graded a-SiC. This resulted in only a small (~10 mV) improvement in initial V_{oc} and no improvement in degraded V_{oc} or efficiency. We conclude that without hydrogen dilution of the bulk i-layer we will not see gains reported by others with hydrogen diluted interface layers since the bulk degradation dominates.

Team Participation

IEC is a member of the National a-Si Team under the Thin Film Partnership Program. Steve Hegedus is the group leader of the Device Design and Interface team. Much of the work described above was performed as part of the teaming activities.

CdTe-based Solar Cells

Production of reliable and reproducible CdS window layers and contacts for stable, high performance CdS/CdTe solar cells are the key issues confronting development of thin-film CdTe solar cells. Meeting these objectives with manufacturing-compatible processes is crucial to satisfying the overall NREL program goals and requires an understanding of the controlling properties and mechanisms. IEC research in this phase was concentrated on: 1) quantifying and controlling CdS-CdTe interaction; 2) analyzing CdTe contact formation and properties; and 3) analyzing device behavior after stress-induced degradation. Through extensive interaction with the National CdTe R&D Team, the applicability of the results and processes to CdS/CdTe cells made by different techniques has been demonstrated, enabling a consistent framework to be used for understanding the relationship between device fabrication and operation.

Devices With Thin CdS

IEC demonstrated improved understanding and control of CdS diffusion by employing evaporated $CdTe_{1-x}S_x$ absorber layers and by modifying post-deposition treatments to anneal crystal defects prior to $CdCl_2$ delivery. Significant results include: 1) determining the effect of $CdTe_{1-x}S_x$ alloy composition on the effective CdS diffusion rate; 2) reducing CdS window layer consumption by 3X; 3) fabricating devices with $J_{sc} > 25$ mA/cm^2 with evaporated CdS layers; 4) determining device performance as a function of *final* CdS thickness; and 5) development of an all-vapor cell fabrication process.

Quantification of CdS-CdTe Interdiffusion

During Phase I, fundamental issues confronting fabrication of devices with ultra-thin CdS were investigated, allowing the CdS consumption process to be understood and controlled. Through teaming activity, the role of TCO properties was further elucidated. In particular: 1) measurement protocols were developed to analyze pinholes in the CdS layer and CdS diffusion into the absorber layer; 2) low-temperature equilibrium data points were added to the CdS-CdTe phase diagram; 3) CdS diffusion into CdTe-based absorber layers with a range of sulfur content was quantified; 4)

CdS diffusion in CdTe was examined for varying post-deposition treatment conditions; 5) the micro-crystal structure of the resulting absorber and absorber-window layer interface was examined by TEM for varying post-deposition treatment conditions; 6) a complete materials analysis with respect to interdiffusion in CdTe/CdS cells was made using CdTe/CdS furnished by six groups of the CdTe Team, leading to development of a phenomenological model of CdTe/CdS devices; and 7) TCO properties were identified which render the device structure more tolerant to complete CdS loss, leading to improvements in baseline efficiency of physical vapor deposited CdTe/CdS devices.

Contact to CdTe

A key chemical component of working CdTe contacts was clearly identified for the "wet chemical" fabrication processes typically employed and an alternative, all-vapor, method for fabricating low resistance contacts was developed. Measurement protocols using variations in light intensity and temperature during current-voltage measurements were employed to analyze the CdTe contact characteristics of devices made by different processes having different contacts. Coupled with the stress-induced degradation and recontacting studies being carried jointly with the CdTe Stability Team, a model is being formulated which links operational and stability aspects of CdTe/CdS cells.

Team Participation

IEC actively participated in the National CdTe R&D Team by fabricating contacts for the stability sub-team and devices for the CdS sub-team, analyzing films and devices for both sub-teams, reporting results through presentations and written reports, and hosting a full-day team meeting on April 30, 1997. In particular, devices were fabricated on different TCO to augment investigation of TCO/CdTe junction influence as d(CdS) is reduced. Contacts to CdTe were deposited and evaluated on CdTe/CdS samples from Solar Cells, Inc., using five different conductors, and from Golden Photon, Inc. A comprehensive x-ray diffraction analysis was performed on samples made by six groups within the team, and a full report was submitted at the April, 1997 team meeting.

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1. Introduction

Photovoltaic modules based on thin film systems of a-Si:H and its alloys, $CuInSe_2$ and its alloys, and CdTe are promising candidates to meet DOE long range efficiency, reliability and manufacturing cost goals. The commercial development of these modules is at different stages and there are generic research issues that need to be addressed.

- quantitative analysis of processing steps to provide information for efficient commercial scale equipment design and operation;
- device characterization relating the device performance to materials properties and process conditions;
- development of alloy materials with different bandgaps to allow improved device structures for stability and compatibility with module design;
- development of improved window/heterojunction layers and contacts to improve device performance and reliability; and
- evaluation of cell stability with respect to illumination, temperature and ambient and with respect to device structure and module encapsulation.

The critical issues that are being addressed under this four-year NREL program for the specific thin film materials system are discussed below.

1.1 $CuInSe_2$-based Solar Cells

$CuInSe_2$ has a bandgap of 1 eV and the devices typically have V_{oc} less than 0.5 V. This bandgap is about 0.5 eV less than required for a single junction device to have optimal efficiency for terrestrial applications. Further, the high J_{sc} of these devices reduces module performance because of higher cell spacing and series resistance losses, and because devices with low operating losses typically suffer larger fractional losses as the devices are operated under real PV module operating conditions (module operating temperatures of 50˚ to 60˚C) as compared to operation under standard measurement conditions (25˚C). Champion cells have been made with bandgaps of about 1.2 eV through the addition of Ga. It is desirable to further increase the bandgap from 1.4 to 1.6 eV for improved module performance.

Presently, most companies developing $CuInSe_2$ for modules form the $CuInSe_2$ films by the selenization of Cu/In films in either an H_2Se or Se atmosphere. Progress has been made in characterizing the chemical pathways to film growth and estimating the reaction rate constants. As the process evolves to include the $CuInSe_2$ alloys, characterization of the reaction chemistry and kinetics needs to be extended to the alloys. While reaction pathways have been identified that lead to the formation of near stoichiometric $CuIn_{1-x}Ga_xSe_2$ when the processing temperatures are limited to below 400˚C, all cells with record-level efficiencies were produced by reacting the absorber layers at temperatures above 500˚C. Such high processing temperatures limit the choice of substrate materials (e.g., lightweight Kapton foil) and make processing and substrate handling in general more difficult. It is presently not well understood why the champion cells had to be processed at such high temperatures.

1.2 a-Si:H-based Solar Cells

Amorphous silicon (a-Si) PV modules were the first thin-film PV modules to be commercially produced and are presently the only thin-film technology that had an impact on the overall PV markets. However, the efficiencies of these modules have not yet reached the levels that were predicted in the 1980s. To a significant degree this is due to the intrinsic degradation of a-Si under illumination. The amount of light-induced degradation can be limited to 20 to 30% in models

operating under prevailing outdoor conditions. Both material processing schemes and device design schemes have been developed to improve the stabilized solar cell efficiency of a-Si solar cells. The use of multijunction devices (allowing the use of thinner absorber layers in the component cells) and the use of employing light-trapping appear to be the most powerful device design schemes to improve stabilized device performance.

The US industry is currently using these approaches to build a-Si-based modules. The so-called substrate type devices are built on stainless steel foil, covered with a "back reflector." The superstrate devices are built on glass coated with transparent conductors (TCO). The texture and transparency of the TCO contacts are critical to improve light-trapping and J_{sc}. Reducing optical losses in the TCO will allow thinner i-layers to generate the same J_{sc}, thus improving stability.

The national amorphous silicon teams have broken down the optimization of stabilized cell performance into the individual high-, mid-, and low-bandgap component cells. However, the optimization of two-terminal dual or triple-junction cells has further requirements such as to minimize the electrical and optical losses in the internal p/n junctions. The p and n layers of a cell have to be optimized not only to result in optimum performance of the component cells, but also to give the lowest losses in multi-junction devices.

1.3 CdTe-based Solar Cells

Instability of CdTe-based solar cells and modules is commonly assumed to be related to the rear contact, especially if this contact is Cu-doped. There is a need to further develop a stable ohmic contact for CdTe compatible with monolithic integration technologies. New contacts must be tested and a method developed to rapidly characterize stability. It appears likely that the optimization of such a contact depends also on the details of the other layers used in the device (CdTe, CdS, SnO, type of glass).

The effects of high temperature processing, either during deposition or after film growth, and $CdCl_2$ treatments on the operation of the device are not well characterized. Of particular concern is the uniformity of large-area modules and the "robustness" of such processes. Questions concerning CdS-CdTe interdiffusion, O and Cl doping, and chemical reactions between $CdCl_2$ and CdTe need to be addressed quantitatively.

Although many researchers have produced devices with 12% efficiency, few have exceeded 14%. The challenge is to obtain high values for J_{sc} without loss of V_{oc}, and a good spectral response at short wavelengths ($\lambda < 500$ nm) without sacrificing the spectral response at longer wavelengths. It is important to understand which factors lead to cells in which such losses can be avoided. It has been established that cell parameters are sensitive to the details of the CdS/CdTe interface. Understanding the mechanisms in detail would accelerate device optimization, which is more and more realized to be an interactive process requiring the optimization of each layer in the device depending on all the other layers present.

1.4 Organization of the Report

This report is organized into three technical sections: $CuInSe_2$-based solar cells, a-Si:H-based solar cells, and CdTe-based solar cells. Each section describes the progress made in addressing the critical issues discussed above during phase I of the program. Based on the results of this phase, the statement of work for phase II was evaluated and modified accordingly.

2. $CuInSe_2$-based Solar Cells

2.1 High Bandgap $CuInSe_2$ Alloys

2.1.1 Introduction

$CuInSe_2$ has a bandgap of 1.0 eV and most $Cu(InGa)Se_2$ based devices have absorber layers with $Ga/(In+Ga) \approx 0.25$ which gives a bandgap of 1.15 eV and results in devices with open circuit voltages < 0.65V. Higher Ga concentrations to increase the $Cu(InGa)Se_2$ bandgap result in a tradeoff of higher open circuit voltage and lower short circuit current which may allow increased cell efficiency. Further, module performance should be improved due to lower resistive losses, thinner ZnO with less optical loss and/or greater interconnect spacing with reduced associated area related losses.

We have previously demonstrated $Cu(InGa)Se_2$ solar cells with 15% efficiency for $Ga/(In+Ga) \leq 0.5$ or bandgap (Eg) ≤ 1.3 eV [101, 102]. With higher bandgap a decrease in cell efficiency was shown to be caused by poor collection of light generated minority carriers in the $Cu(InGa)Se_2$ absorber layers. In this work we have continued characterization of $Cu(InGa)Se_2$ devices with increasing Ga content and bandgap. In addition, we have begun to investigate other $Cu(InGa)Se_2$ based alloy materials, $CuInS_2$ and $Cu(InAl)Se_2$, which may provide alternative means to achieve improved device performance with Eg > 1.3 eV.

2.1.2 $Cu(In,Ga)Se_2$ device analysis

As the bandgap of $CuInSe_2$ is increased by alloying with Ga or S, the loss in efficiency due to the decrease of light generated current with increasing voltage becomes important. The standard technique of quantifying this loss is to analyze spectral response measurements made as a function of applied voltage. Instead, it is shown how to determine the voltage dependence of the light generated current by an analysis of the current-voltage (I-V) measurements made at two different light intensities. By adding an I-V measurement at a third light intensity one can also determine if the analysis technique is valid ([103] and Appendix 1).

2.1.2.1 Experimental procedures

It has been demonstrated that the loss in efficiency of $Cu(In,Ga)Se_2$ solar cells with high Ga content is due to a decrease in fill factor, and to a lesser extent V_{oc} which is caused by a drop in the light generated current with increasing forward voltage [101, 102]. This type of loss mechanism is well known in amorphous silicon solar cells where I-V measurement and analysis techniques have been developed to determine the voltage dependence of the light generated current, J_L (V), [104, 105].

In most solar cells, it is possible to correct for parasitic resistive losses by measuring and subtracting the small shunt, R_{shunt}, and series resistance, R_{series}, losses from the measured J - V data. This then leaves the junction current, J_J (V'), and the voltage dependent light generated current, J_L (V'). If J_J (V') is independent of light intensity and J_L (V') is proportional to the light intensity, J_L (V') can be found by subtracting the corrected J-V data measured at two different light intensities. One can also determine if the assumptions are correct by using additional J-V measurements made at other light intensities to determine J_L (V') independently and comparing.

J-V measurements were made on $Cu(In,Ga)Se_2$ solar cells at four different light intensities: (1) full AM1.5 Global normalized to 100 mW/cm^2, (2) ~90% AM1.5G, (3) ~10% AM1.5G and (4) Dark. The reduced light intensities were achieved using neutral density screens. Two high light intensities (full & ~90%) and two low light intensities (~10% & dark) were chosen to give accurate

comparisons when subtracting the J'-V' data. R_{shunt} was determined from finding the minimum dJ/dV, usually from the dark data, in reverse voltage bias. R_{series} was found from the intercept of dV/dJ vs. 1/J. The lower light intensities, ~10% and dark, are used in the R_{series} determination in order to reduce interference from J_L (V) effects. After correcting all the data for these losses, the high intensity J'-V' data were subtracted from the low intensity data. Except for high forward voltage bias, the different subtractions are basically identical. This shows that the assumptions that J_J (V') is independent of light intensity and J_L (V') is proportional to the light intensity are valid.

2.1.2.2 Results

Table 2.1 shows the results of the previously described measurements and analysis when applied to various $Cu(In_{1-X}Ga_X)Se_2$ solar cells. The solar cells used for this analysis were chosen from two categories: (1) moderate Ga content ($X \approx 0.3$) and fairly high efficiency and (2) high Ga content ($X = 0.5 \rightarrow 0.7$) and high V_{oc}. As can be seen from this table, the J_L (V) losses, which varies from cell to cell, primarily affects FF and V_{oc} and hence Eff. However, unlike the best devices examined in References [101] and[102], these J_L (V) losses do not obviously increase with increasing Ga content.

Table 2.1 J-V parameters for various $Cu(In,Ga)Se_2$ devices measured and analyzed (see text).

Measured at AM1.5 Global @100mw/cm^2 T = 30 deg. C; Area = 0.13 cm^2				Derived Series and Shunt Resistances		Calculated AM1.5 Global J-V parameters without J_L (V) loss, i.e., $J_L = J_L$ (V)max.			
Eff (%)	V_{oc} (Volts)	FF (%)	J_{sc} (mA/cm^2)	R_{series} (Ω-cm^2)	R_{shunt} (kΩ-cm^2)	Eff (%)	V_{oc} (Volts)	FF (%)	J_{sc} (mA/cm^2)
High Efficiency $Cu(In_{1-X}Ga_X)Se_2$ $X \approx 0.3$									
13.9	0.606	68.8	33.2	0.2	1.7	15.1	0.635	71.0	33.5
13.6	0.631	72.1	29.8	0.1	2.5	14.2	0.644	73.6	30.0
12.8	0.583	67.8	32.4	0.0	0.7	13.7	0.607	69.4	32.6
12.8	0.605	68.2	31.0	0.0	1.7	13.5	0.626	69.3	31.1
12.6	0.612	66.2	31.1	0.5	1.4	14.5	0.637	71.9	31.7
12.5	0.596	63.9	32.9	0.4	1.1	14.6	0.621	70.3	33.3
High Voltage $Cu(In_{1-X}Ga_X)Se_2$ $X = 0.5 \rightarrow 0.7$									
7.9	0.764	60.4	17.0	0.0	5.0	10.0	0.792	71.2	17.7
6.9	0.734	61.6	15.3	0.4	2.0	9.4	0.760	76.2	16.2
10.1	0.732	74.4	18.5	0.0	5.0	10.6	0.736	76.6	18.8

It can be concluded that, by taking J-V measurements with at least three different light intensities, one can determine if it is correct to analyze these data for J_L (V) losses and, if correct, what the magnitude of these losses are.

2.1.3 $CuInS_2$

$CuInS_2$ has a bandgap of 1.53 eV and the $CuIn(SeS)_2$ system allows the bandgap to be varied continuously from 1.0 to 1.53 eV. $CuInS_2$ occurs as a single phase in the region slightly copper and sulfur rich of stoichiometric in the ternary phase diagram. Unlike $CuInSe_2$, which is single phase for Cu/In < 1, if the composition of $CuInS_2$ becomes at all indium rich, In_2S_3 precipitates to the surface of the film [106]. The growth of films with Cu/In > 1.1 followed by a KCN etch to remove segregated CuS from the surface is considered necessary for high efficiency devices. The CuS enhances the growth of the $CuInS_2$ resulting in larger grains [107]. The highest reported efficiency device for Cu/In precursors reacted in H_2S is 10.5% [108].

2.1.3.1 Experimental procedures

The objective of the work done in this contract phase was to develop a process to form single phase $CuInS_2$ from metal precursors in a sulfur atmosphere. This has been approached by upgrading the flowing H_2Se reactor to allow reaction of Cu/In precursors in H_2S. The IEC CVD reactor for selenization of metallic precursors in a quartz tube under flowing H_2Se was upgraded to allow reaction in any combination of H_2S and H_2Se to form $CuIn(SeS)_2$. Specifically, the system has pure H_2S, H_2Se(16%)/Ar, Ar, and Ar/O_2 gases available. Modifications to the reactor included adding the gas handling capability to add H_2S, an upgraded control panel to allow controlled simultaneous flow of H_2Se and H_2S and modifications to the safety systems. A schematic drawing of the system is shown in Figure 2.1. Safety features of the upgrade include the choice of a low pressure H_2S bottle stored within the reactor enclosure. A single point MDA TLD-1 H_2S gas detector was added to the reactor enclosure system. The two-stage packed column waste treatment system in place for the H_2Se is also effective to treat H_2S in the exhaust.

Experiments were performed to characterize the reaction of individual copper and indium precursor films on glass with the flowing H_2S. The samples were reacted in 2% H_2S for 90 minutes at various temperatures from 250 to 550˚C. EDS and XRD analysis were used to characterize the resulting films. The phases determined by XRD are summarized in Table 2.2.

2.1.3.2 Results

Indium samples had good adhesion, but the indium agglomerated into islands during reaction. This was minimized by applying a 20 minute heat treatment in dry air at 450˚C to each sample prior to reaction to convert the surface layer of the film to indium oxide. The film reacted in H_2S at 250˚C was identified as In_6S_7 with no other phases detected by XRD. In the films reacted at 350, 450, and 550˚C, the films contained a mixture of In_2S_3 and a second phase identified as $Na_2In_2S_4$. The amount of $Na_2In_2S_4$ present increased with increasing temperature. To verify the identification of $Na_2In_2S_4$, indium samples were prepared on SLG, 7059 and alumina substrates. These samples were reacted at 550˚C. The XRD scans for the samples on SLG and 7059 are shown in Figure 2.2. The $Na_2In_2S_4$ is present with some In_2S_3 on the SLG sample, while only In_2S_3 is found in the 7059 glass sample.

Cu films deposited on soda lime glass substrates resulted in single phase $Cu_{1.8}S$ when reacted at 350, 450, and 550˚C. Adhesion problems for films reacted at 250˚C prevented any characterization in that case. Cu films deposited on 7059 borosilicate glass substrates resulted in $Cu_{1.8}S$, $Cu_{1.93}S$, or an amorphous phase depending on the reaction temperature as shown in Table 2.2.

A set of Cu/In samples, with Cu/In ≈ 0.9, on soda lime and 7059 glass were also reacted at various temperatures and the phases determined by XRD are also listed in Table 2.2. The XRD measurements of the films on soda lime glass revealed $CuInS_2$ peaks with a small amount of $Na_2In_2S_4$. Films on 7059 glass had $CuInS_2$ with In_6S_7 and $Cu_{11}In_9$ at the lower temperatures as indicated below.

Table 2.2 Phases observed by XRD in Cu, In, and Cu/In precursor films on soda lime and 7059 glass substrate and reacted in H_2S at different temperatures.

Precursor	substrate	250˚C	350˚C	450˚C	550˚C
Cu	soda lime	poor adhesion	Cu1.8S	Cu1.8S	Cu1.8S
Cu	7059		Cu1.93S	Cu1.93S, Cu1.8S	amorphous
In	soda lime	In_6S_7	In_2S_3, $Na_2In_2S_4$	In_2S_3, $Na_2In_2S_4$	In_2S_3, $Na_2In_2S_4$
In	7059	In_6S_7, In_2O_3	In_2S_3, In_2O_3	In_2S_3, In_2O_3	In_2S_3, In_2O_3
Cu/In	7059	-	$CuInS_2$, $Na_2In_2S_4$	$CuInS_2$, $Na_2In_2S_4$	$CuInS_2$, $Na_2In_2S_4$
Cu/In	7059	$CuInS_2$, In_6S_7, $Cu_{11}In_9$	$CuInS_2$, $Cu_{11}In_9$	$CuInS_2$	$CuInS_2$

The reaction of Cu/In precursors, with Cu/In > 1, was performed at different H_2S concentrations from 0.125 to 3% in Ar. The films were reacted in the flowing H_2S/Ar at 450˚C for 90 min. The morphology of the resulting films changed with H_2S concentration as demonstrated by SEM micrographs of films reacted at 0.25% and 2% in Figure 2.3. The films all have an increase in the Cu/In ratio from the precursor to the reacted film attributed to loss of volatile In_xS_y species. This In loss could be minimized by reducing the ramp time from room temperature to reaction temperature. The In loss could also be minimized by holding the film at an intermediate temperature, e.g. 325˚C, for 10 minutes before ramping up to the final reaction temperature. This process yields a reproducible composition and morphology with Cu/In >1 which can be made single phase $CuInS_2$ with a post-deposition KCN etch.

Subsequent work will focus on the simultaneous reaction with H_2S and H_2Se to form single phase $CuIn(SeS)_2$ and allow control of the bandgap over the range 1.0 - 1.5 eV. Devices will be fabricated and characterized to supplement more detailed material characterization.

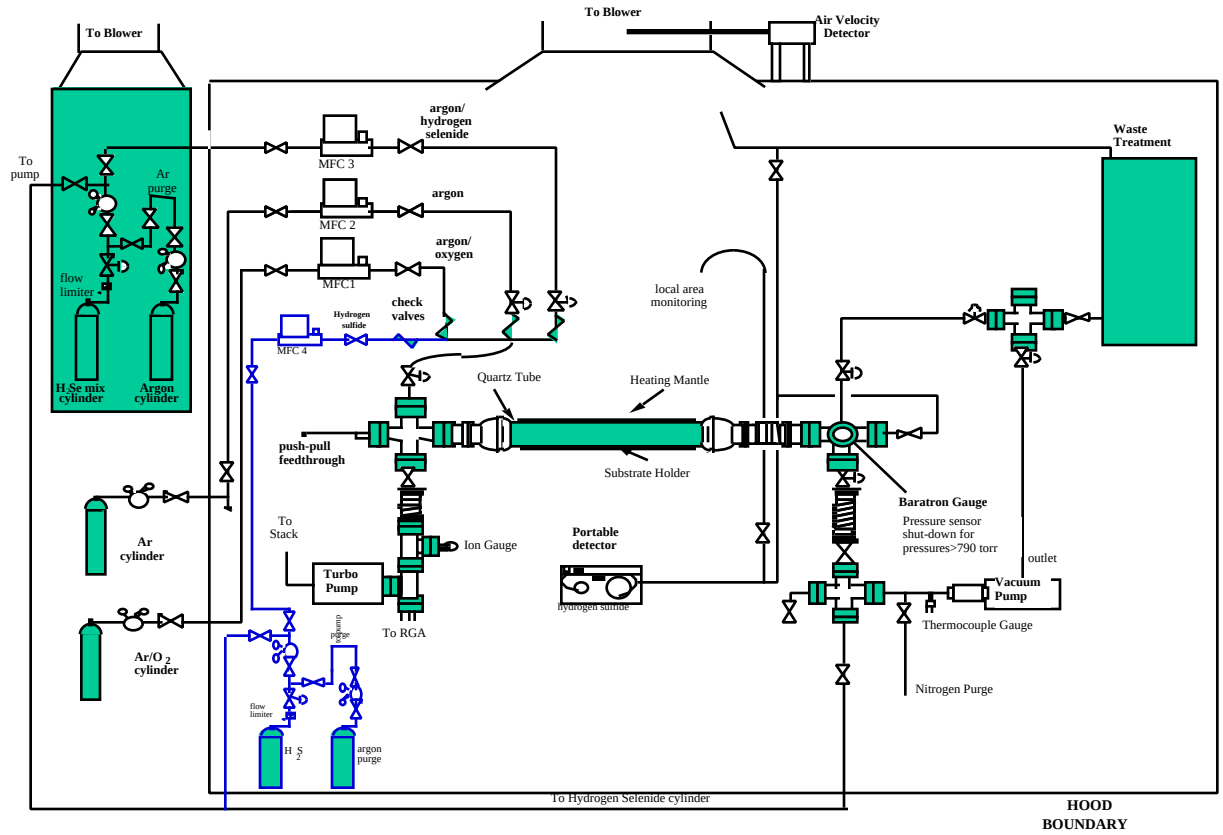


Figure 2.1 Schematic diagram of the H_2Se/H_2S CVD reactor including gas handling and waste treatment.

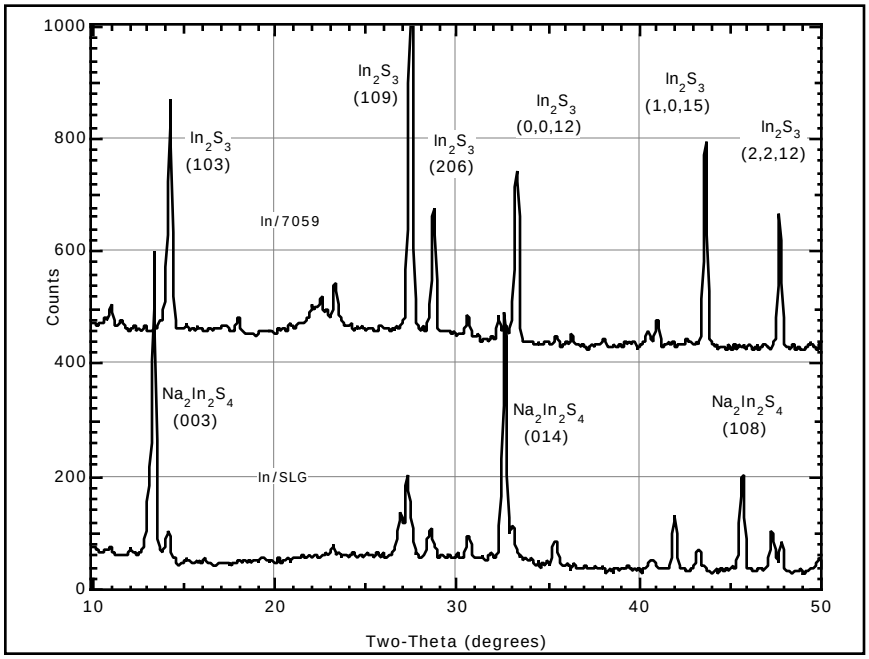
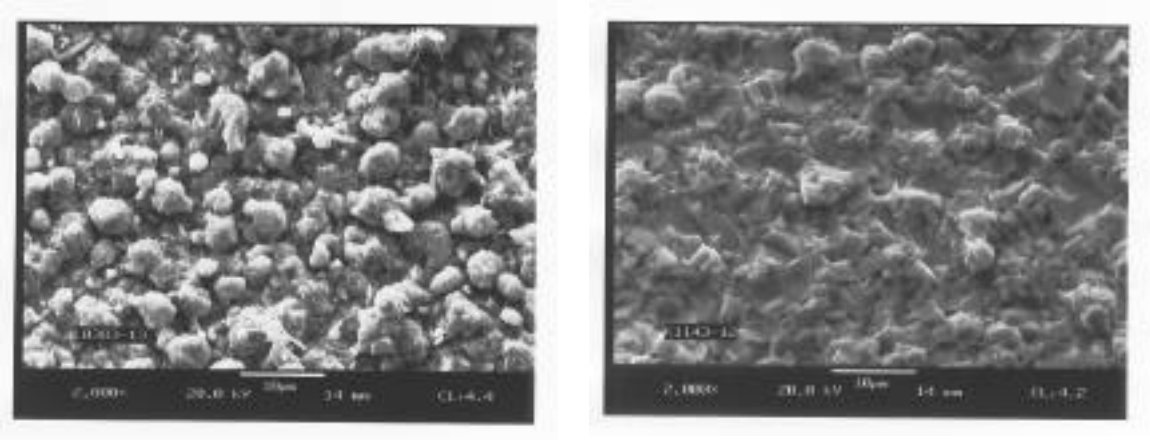


Figure 2.2 XRD scans of In films on 7059 (top) and soda lime (bottom) substrates after they were reacted in H_2S at 550˚C for 90 min.



2% H_2S concentration 0.25% H_2S concentration

Figure 2.3 SEM micrographs at 2000x magnification showing the change in morphology of Cu/In films reacted at different H_2S concentrations.

2.1.4 Cu(InAl)Se_2

The band gap of Cu(InAl)Se_2 can be varied from 1.0 eV to 2.7 eV by varying the Al/(Al+In) ratio from 0 to 1.0. This steep variation of band gap in this alloy system can be exploited to achieve the optimum band gap for an absorber of approximately 1.4 eV by replacing only 25 % of In by Al in $CuInSe_2$. In contrast, about 60% of In has to be replaced by Ga to obtain 1.4 eV in the Cu(InGa)Se_2 system. In analogy with Cu(InGa)Se_2, it may be preferable to replace as small an In content as possible in order to retain better device performance. Other practical advantages of using Al over other materials in current use for engineering the band gap, such as Ga and S, are the availability and ease of handling. Also, it is easier to sputter deposit Al than Ga.

Existence of a continuous solid solution for the $CuInSe_2$ - $CuAlSe_2$ system has been established in crystal-form [109, 110, 111] and in thin film-form [112]. Powder diffraction studies have showed that the lattice parameters vary linearly with 'x' in $CuIn_{1-x}Al_xSe_2$ [110, 111]. The energy gap (Eg) is almost linear with 'x'. The authors in Reference 111 have provided a relationship for the variation of Eg with 'x' as:

$$E_g(x) = E_g(0) + bx(1-x) + [E_g(1) - E_g(0)]x \qquad : b = 0.51 \qquad (2.1)$$

2.1.4.1 Experimental procedures

It was the goal of this work to obtain single phase Cu(InAl)Se_2 thin films by selenization of Cu-Al-In precursors. The Cu thickness was chosen to be 2500 Å to obtain a final selenized film thickness of approximately 2 µm. The precursors were deposited either by e-beam evaporation or by sputtering of individual elements on molybdenum coated soda lime glass substrates. There was no intentional heating of the substrates during the deposition of the precursors. The Al layer was buried under either the In or Cu layer because Al would rapidly oxidize during transfer of precursors to the selenization reactor and the oxide layer would be very stable. Two sets of precursors were prepared: one set with Al/(Al+In) ratios 0.15, 0.30, and 0.45 and another set with Al/(Al+In) ratios 0.05, 0.10, 0.15, and 0.20. Selenization was carried out at 450˚C to 550˚C

with a mixture of $H_2Se/Ar/O_2$ flowing. Selenized films were characterized by SEM, EDS and XRD.

2.1.4.2 Results

For the precursor stacking sequence Cu/Al/In only elemental phases Cu, Al and In were observed in the as-deposited state. The Al layer between the Cu and In layers prevents alloying of Cu and In. Al and In forms a eutectic and have very little solid solubility in each other. Cu-Al form a series of intermetallic compounds: Cu_9Al_4, $CuAl_2$, Cu_3Al_2, Cu_4Al and Cu_3Al. After annealing at 450˚C for 10 minutes the precursor with Al/(Al+In) ratio of 0.45 contain Cu_9A_{l4} and In, the precursor with Al/(Al+In) ratio of 0.30 contains Cu_9A_{l4}, Cu-Al solid solution and In, and the precursor with Al/(Al+In) ratio of 0.15 contain Cu-Al solid solution and In. These results indicate that Cu-Al alloys form preferably over Cu-In alloys.

Films obtained by selenizing Cu/Al/In precursors with Al/(Al+In) ratios 0.15, 0.30 and 0.45 at 450˚C for 90 minutes are non-uniform with In-rich regions. In-rich regions form during the ramp-to-reaction temperature due to the high surface mobility of In atoms. Due to preferential formation of Cu-Al alloys over Cu-In alloys, most of the In is present in the elemental form. Elemental In is able to diffuse rapidly on the surface to form islands of In. This non-uniformity in In distribution present after the ramp-to-reaction temperature gives rise to the compositional non-uniformity in the selenized films.

Films obtained by selenizing Al/Cu/In at 450˚C precursors with Al/(Al+In) ratios 0.15, 0.30 and 0.45 were also found to be non-uniform. XRD revealed that in all of the above selenized films $CuInSe_2$ phase was predominant with a signature of $CuAlSe_2$ phase in some films. Some unidentified peaks were also observed in few films. Spot EDS analysis on cross-sections suggests the presence of unreacted Cu-Al alloy at the Mo/film interface. Selenization at 500˚C yielded results similar to those observed at 450˚C. Al/Cu/In precursors selenized at 550˚C showed definite formation of $CuAlSe_2$ for Al/(Al+In) ratios 0.30 and 0.45. Films with Al/(Al+In) ratio of 0.15 did not show the presence of $CuAlSe_2$. To remove non-uniformity due to In agglomeration, the precursors were exposed to H_2Se during the ramp-to-reaction temperature. XRD scans of these films, however, did not show single phase $Cu(InAl)Se_2$. Figure 2.4 shows an XRD scan of a film obtained by selenizing an Al/Cu/In precursor at 550˚C for 90 minutes. The pattern reveals the presence of two distinct phases, $CuInSe_2$ and $Cu(InAl)Se_2$ with Al/(In+Al) ≈ 0.55. Even after post-selenization annealing at 600˚C for 60 minutes, a single phase $Cu(InAl)Se_2$ film was not obtained.

Al/Cu/In precursors with Al/(Al+In) ratios of 0.05, 0.10, 0.15 and 0.20 were selenized at 550˚C for 90 minutes with H_2Se flowing during the ramp-to-reaction temperature. Figure 2.5 shows the detailed XRD scans of the several characteristic peaks in the resulting films . The Al/(Al+In) ratios were chosen after realizing the difficulty in obtaining single phase at 550˚C for 90 minutes reaction time for higher Al/(Al+In) ratios of 0.30 and 0.45. Selenization at 600˚C was not attempted because soda-lime glass substrates soften and loose their mechanical integrity at this temperature. In Figure 2.5(a)-(d) the X-ray peaks shift to higher angles, i.e., to lower d-spacings, with increasing Al content in the films. Due to the overlap of the Se 'L' and Al 'K' X-ray energies, EDS compositional measurements of these films were not accurate. The X-ray peak positions of the film from the precursor with Al/(Al+In) of 5% indicates that this film contains $CuInSe_2$ to a large extent with very little or no Al dissolved in the $CuInSe_2$ phase. The other three films show a definite change in lattice parameter due to Al dissolution in $CuInSe_2$. In Figure 2.5(c), the peak shape of (312)/(116) changes from a doublet due to c/a ratio of a chalcopyrite structure different from 2.0 to a single peak due to a c/a ratio of 2.0. As the 'x' in $CuIn_{1-x}Al_xSe_2$ increases from 0 to 1.0 the c/a ratio of the resulting structure varies from 2.01 to 1.96.

In conclusion, single phase $Cu(InAl)Se_2$ films were obtained by selenizing stacked metallic layers of Al/Cu/In in H_2Se at 550˚C for 90 minutes.

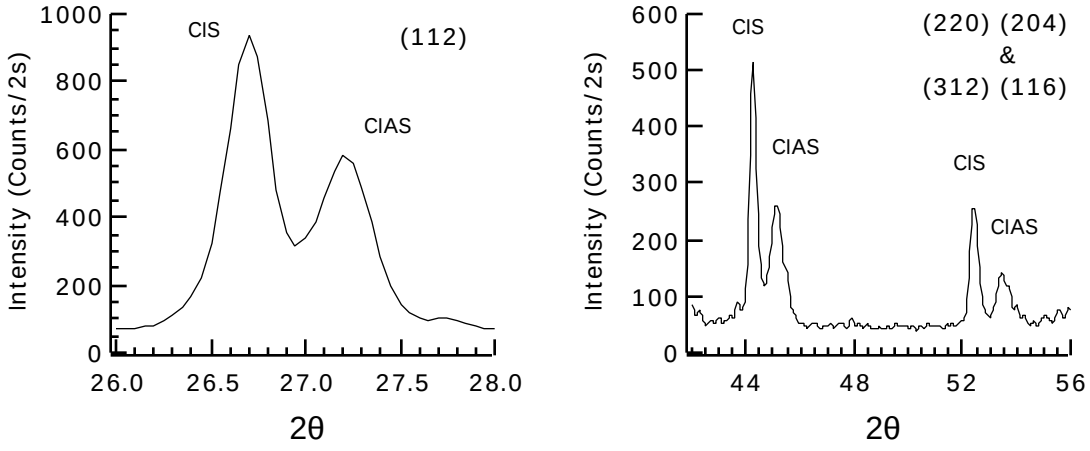


Figure 2.4 XRD pattern of a film obtained by selenizing Al/In/Cu precursor at 550˚C. The Al/(Al+In) ratio in the precursor is ≈ 0.45. CIS = $CuInSe_2$, CIAS = $CuIn_{1-x}Al_xSe_2$.

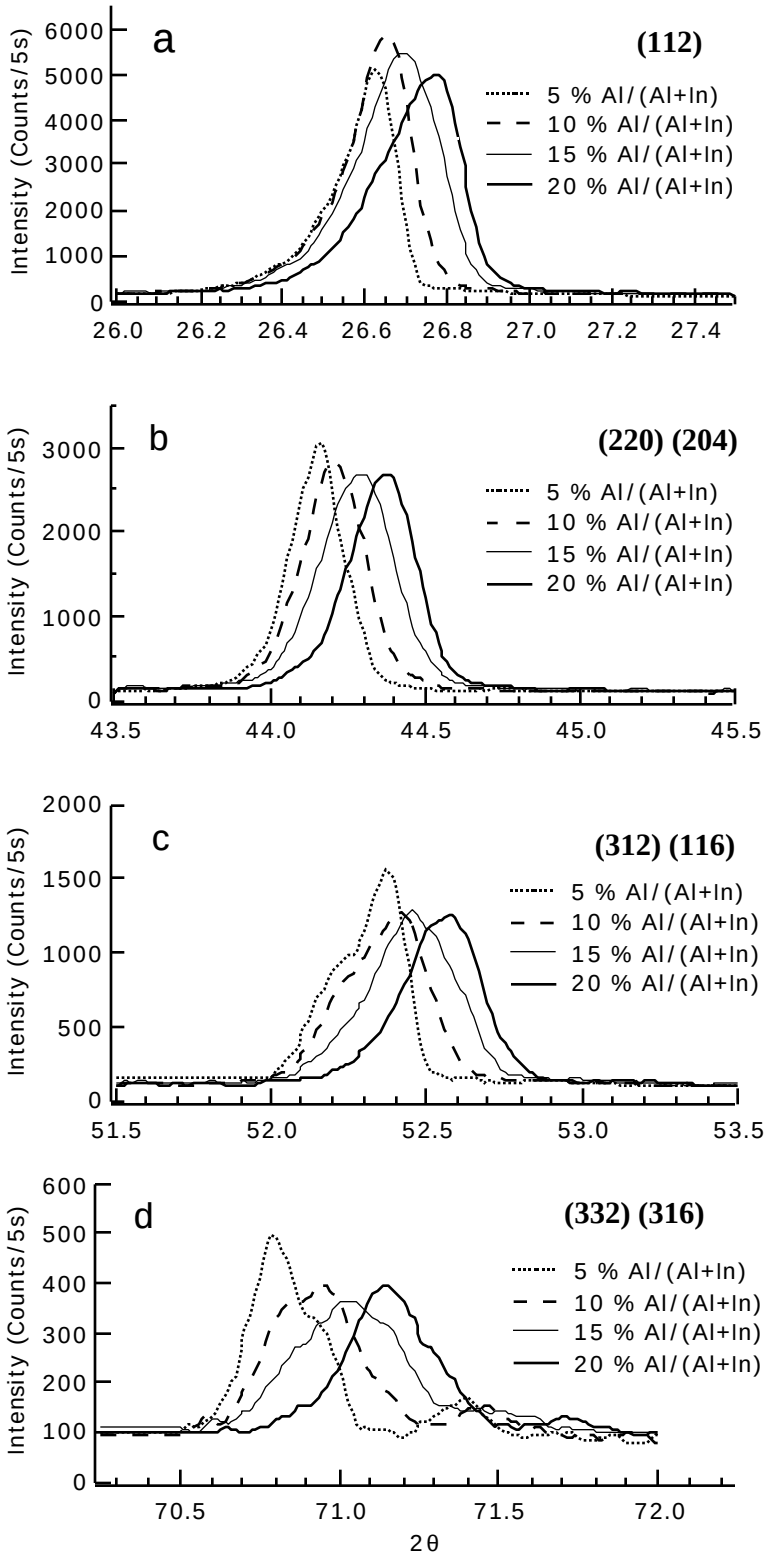


Figure 2.5 XRD plots of various peaks of a $CuIn_{1-x}Al_xSe_2$ films (from run L0393). The Al/Al+In) concentrations in the legends are intended ratios in the precursors.

2.2 Reduced Cu(InGa)Se_2 Deposition Temperature and Thickness

2.2.1 Introduction

There are many technical issues which need to be addressed to effectively enable the transfer of Cu(InGa)Se_2 deposition and device fabrication technology from the laboratory to manufacturing scale. In general, these issues provide means to reduce thin film semiconductor process costs. Shorter deposition time can be achieved with reduced film thickness and increased deposition rate. Thinner absorber films reduce the total amount of material used and allow faster process throughput. The minimum thickness of the Cu(InGa)Se_2 absorber layer may be determined by the nucleation of the film to form a continuous layer or by the film morphology. From a device perspective, the minimum thickness may be determined by the minority carrier diffusion length and optical absorption coefficient of the Cu(InGa)Se_2 or the ability to incorporate optical confinement.

Lower substrate temperature (T_{ss}) can lower processing costs by reducing thermally induced stress on the substrate, allowing faster heat-up and cool-down, and decreasing the heat load and stress on the entire deposition system. In addition, with lower substrate temperature, stress on the glass substrate can be reduced and alternative substrate materials, like a flexible polymer web, could be utilized.

In this work, we have addressed the need to improve process throughput by reducing the Cu(InGa)Se_2 thickness and deposition temperature. The approach during this work has been to first define a baseline process for Cu(InGa)Se_2 deposition by multisource elemental evaporation and solar cell fabrication. All other deposition parameters are then held fixed to determine the effects of varying either the substrate temperature or, by changing the deposition time, film thickness. Material properties of the resulting Cu(InGa)Se_2 films have been characterized and their device behavior has been measured and analyzed.

2.2.2 Experimental procedures

Cu(InGa)Se_2 films were deposited by thermal evaporation from four elemental sources. Details of the deposition, film characterization, and device fabrication are described in Reference 101. The baseline deposition process in this work is the same as described but with T_{ss} maintained constant through the entire deposition. The films are deposited with a Cu-rich first layer, deposited in 32 min. and followed continuously by an In-Ga-Se second layer deposited in 12 min. The fluxes of Ga and In are constant through the deposition time so there is no grading of the bandgap. A profile of the source and substrate temperatures are shown in Figure 2.6. This results in ~2.5 μm thick films with Ga/(In+Ga) ≈ 0.3 which gives a bandgap ~ 1.2 eV.

To study the effect of substrate temperatures, Cu(InGa)Se_2 films were deposited with T_{ss} from 600 to 350°C, maintaining fixed source effusion rates and deposition times. To study varying thicknesses, films were deposited with constant effusion rates and T_{ss}, and only the times adjusted.

The film thickness was determined by the mass gain after deposition and from cross-sectional micrographs and the films were characterized by scanning electron microscope (SEM) images, energy dispersive x-ray spectroscopy (EDS), x-ray diffraction (XRD). Secondary ion mass spectroscopy (SIMS) measurements were performed at NREL.

The Cu(InGa)Se_2 films were deposited on soda lime glass substrates with a sputtered 1 μm thick Mo layer. Complete solar cells were fabricated [101] with the chemical bath deposition of ~ 30 nm CdS followed by rf sputtered ZnO:Al with thickness 0.5 μm and sheet resistance 20 Ω/sq. Two different cell configurations were used. Cells with active area ≈ 0.13 cm^2 were fabricated by deposition of Ni bus bar/contact tabs and mechanical scribing to define cell areas. Cells with total

area ≈ 0.5 cm^2 were fabricated using a Ni/Al grid and 125 nm MgF_2 anti-reflection layer deposited by electron beam evaporation and, again, mechanical scribing to define cell areas. Devices were characterized by current-voltage (J-V) measurements at 28°C under 100 mW/cm^2 AM1.5 illumination.

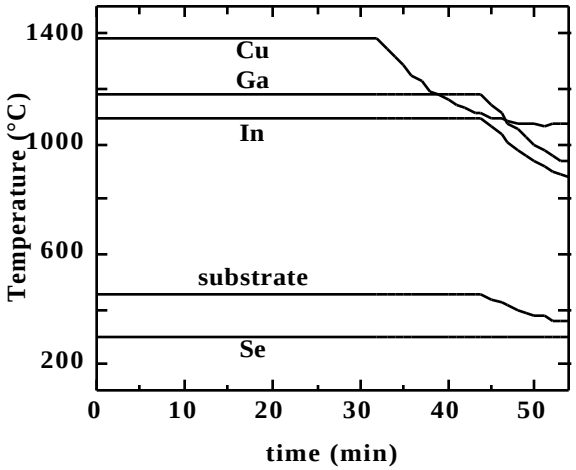


Figure 2.6 Deposition profile showing source and substrate temperatures for a standard run with T_{ss} = 450˚C.

2.2.3 Results: Deposition temperature

$Cu(InGa)Se_2$ films were deposited at varying T_{ss} with fixed effusion rates that were determined to give films of composition Cu/(In+Ga) ≈ 0.9 and Ga/(In+Ga) ≈ 0.3 when T_{ss} = 600°C. This required the total concentration of metals to be delivered to the substrate with ratios Cu/(In+Ga) ≈ 0.6 and Ga/(In+Ga) ≈ 0.3. Compositional analysis, by EDS, of the films is presented in Appendix 2. All films have Ga/(In+Ga) ≈ 0.3.

SEM micrographs show that the grain structure of the $Cu(InGa)Se_2$ films changes dramatically as T_{ss} changes. SEM micrographs of the top surface are shown in Figure 2.7 and cross sectional micrographs are shown in Appendix 2. These show columnar grains at T_{ss} = 600°C with typical grain size 1.5 - 2 μm. But the grains become smaller as T_{ss} decreases and for T_{ss} ≤ 450°C it appears that single grains do not grow continuously from the Mo to the top surface. In this case, current in a working device clearly would need to cross several grain boundaries. XRD measurements did not reveal any significant differences in the film orientation or compositional distribution at different substrate temperatures. All films have approximately random orientation of grains, comparable to a powder diffraction pattern. We have shown previously that this is determined by the orientation of the Mo film [113]. There is no peak broadening, indicating that the average grain size at the lowest T_{ss} is still greater than ~ 300 nm.

While the film deposited at T_{ss} = 600°C has the largest grains, the soda lime glass in this case is well above its softening point during the deposition which resulted in a curved substrate [114].

$Cu(InGa)Se_2$ have been shown to contain significant levels of Na impurities when deposited on soda lime glass substrates [115]. The Na is incorporated into the $Cu(InGa)Se_2$ by diffusion and is therefore expected to be temperature dependent. Depth profiles of the Na content measured by SIMS are shown at different T_{ss} in Appendix 2, Figure 3. The Na level varies by relatively little

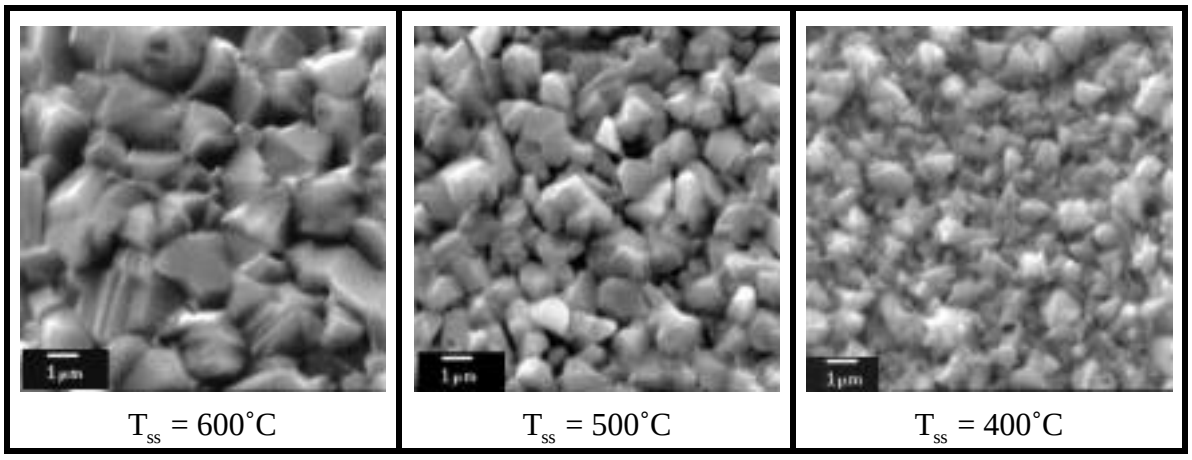
from 400 to 600°C and is actually highest for the lowest T_{ss}, though diffusion of Na is expected to increase with increasing T_{ss}. This may be explainable by Na diffusion along grain boundaries since there is a greater grain boundary density at the lower temperature. The SIMS profiles for Cu, Ga, In, Se, Mo, and Na are shown in Figure 2.8 for samples deposited at T_{ss} = 600, 500, and 400˚C. These profiles show that the Cu, In, and Ga are uniformly distributed from the front surface of the film to the Mo contact at all deposition temperatures.

Finally, solar cells were fabricated with films deposited at varying T_{ss} and the J-V parameters for the best cell achieved at each T_{ss} are listed in Table 2.3. The efficiency (η) decreases slowly as T_{ss} decreases from 550°C, but is still 12.8% at 400˚C and 10.9% at 350˚C. While there is some tradeoff in V_{oc} and J_{sc} which may be associated with variations in the Ga content and, therefore, bandgap of the $Cu(InGa)Se_2$, the biggest change is the fill factor. Further analysis of these devices is presented in Section 2.2.5.

The dependence of grain size with T_{ss} has been reported previously [116] and at high temperatures was attributed to the formation of copper selenide phases above ~525˚C which act as a "flux" for grain growth in the Cu rich film [117]. However, the films in this work show an increasing grain size with increasing T_{ss} over the entire temperature range. There is only a small drop-off in device performance with lower T_{ss} despite the decreasing grain size.

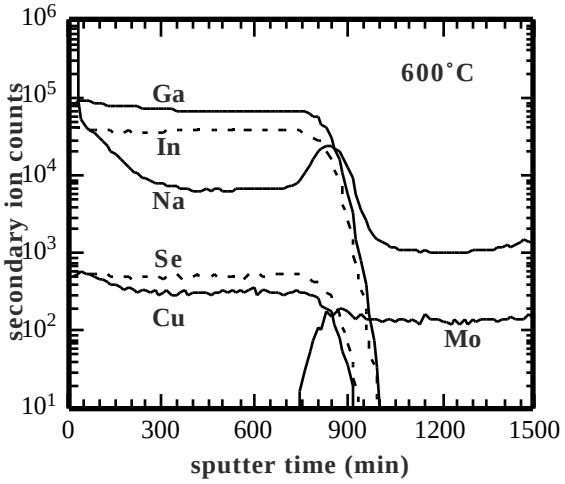
Table 2.3 J-V parameters with varying substrate temperature.

T_{ss} (°C)	V_{oc} (mV)	J_{sc} (mA/cm^2)	FF (%)	η (%)
600	0.596	31.2	67.4	12.5
550	0.583	34.3	71.8	14.4
500	0.606	32.5	70.0	13.8
450	0.605	32.6	68.4	13.5
400	0.606	32.5	64.8	12.8
350	0.561	33.2	58.6	10.9

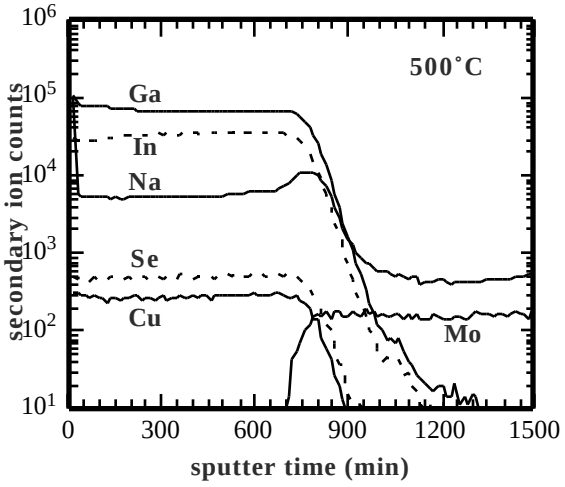


T_{ss} = 600˚C | T_{ss} = 500˚C | T_{ss} = 400˚C

Figure 2.7 SEM micrographs showing a decrease in grain size as T_{ss} decreases from 600 to 400˚C.



(a)



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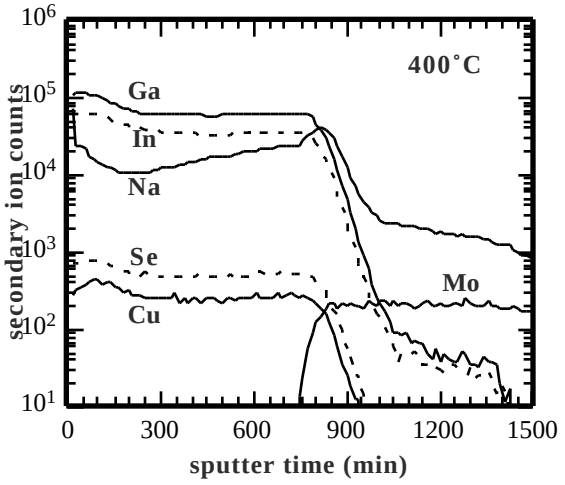


(c)

Figure 2.8 SIMS depth profiles of Cu, In, Ga, Se, Mo, and Na for films deposited with (a) T_{ss} = 600˚C, (b) 500˚C, and (c) 400˚C.

2.2.4 Results: Film thickness

Using the same effusion rates as above, the effect of thickness has been studied by changing the deposition times with T_{ss} = 450°C to give films with thickness (d) ranging from 2.5 to 1.0 μm as determined by mass gain of the substrate. The thickness estimated from SEM cross-sectional micrographs was ~ 0.2 μm thinner than that determined from the mass gain. The composition of these films was unchanged over the thickness range with all films having Cu/(In+Ga) ≈ 0.9 and Ga/(In+Ga) ≈ 0.3 and again, no difference in orientation or compositional distribution was observed by XRD.

Device results for different Cu(InGa)Se_2 thickness with this deposition process are shown in Table 2.4. With d ≥ 1.4 μm the devices have η ≈ 13%. There are no significant thickness related losses which might include effects of bulk series resistance or back surface recombination. For d = 1.0 μm, η decreases due to decreases in V_{oc}, J_{sc}, and FF. In addition, the J-V curves both in the dark and under illumination indicate an increased shunt conductance for the thinnest cells. SEM micrographs in Section 2.2.3 and Appendix 2 show that films deposited with T_{ss} < 500˚C have decreasing grain size and horizontal grain boundaries. This may lead to morphological defects which contribute shunt-like characteristics to the J-V behavior of the cells with thinner Cu(InGa)Se_2 layers.

Table 2.4 J-V parameters with decreasing Cu(InGa)Se_2 thickness for films deposited at T_{ss} = 450˚C.

d ± 0.2 (μm)	V_{oc} (mV)	J_{sc} (mA/cm^2)	FF (%)	η (%)
2.5	0.605	32.6	68.4	13.5
1.8	0.581	33.7	66.6	13.0
1.4	0.590	32.5	69.5	13.3
1.2	0.526	34.2	64.9	11.7
1.0	0.514	30.7	62.5	9.9

2.2.5 Device measurements and analysis

For the six evaporation runs made on which results were reported in Table 2.3, a total of 101 devices from 19 samples were processed and tested. Twenty-four samples of six cells each for a total of 144 devices were processed and tested from the 10 evaporation runs made at five different Cu(In,Ga)Se_2 thicknesses.

In addition, Table 2.5 and Table 2.6 show the averaged J-V parameters, along with their standard deviation, taken from the highest efficiency test for every sample processed from these evaporation runs. These results include cells with area ≈ 0.13 cm^2 tested on an active area basis, and cells with area ≈ 0.42 cm^2 tested on a total area basis. Furthermore, some cells have an MgF_2 anti-reflection layer. Although the samples were not processed at identical times or under identical conditions after the Cu(In,Ga)Se_2 evaporation runs, they still give an idea of the sample to sample variation, and the cell to cell variation within a sample, that can occur. There would have been an even wider variation if the heavily shunted or shorted devices not been excluded.

The statistical data shown in Table 2.5 and Table 2.6 show a great deal of overlap in the J-V parameters as a function of either thickness or substrate temperature. However, it can be seen that the averaged efficiency does fall off at the two lowest thicknesses (1.0 and 1.2 μm) and the lowest

substrate temperature (350˚C). In all of these cases there is a decrease in FF due to an increase in shunting behavior as shown in the values of $dJ/dV@J_{sc}$. The shunting behavior was also seen in the dark J-V characteristic. The shunting behavior could lead to a decrease in V_{oc} as well. This could be caused by the rougher and thinner $Cu(In,Ga)Se_2$ material. The loss in J_{sc} for thinner $Cu(InGa)Se_2$ cannot be explained by simple morphology.

It is necessary to improve the uniformity of device results within a single $Cu(In,Ga)Se_2$ evaporation run before more detailed differences can be seen.

Table 2.5 Statistics of all the device J-V parameters for each sample made into cells as a function of substrate temperature. Parameters were taken from the best average efficiency test. *Shorted or heavily shunted ($dJ/dV@J_{sc} \geq 25$ mS/cm^2) not included in the statistics.

Substrate	Average ± Standard Deviation						# of	total		
Temp.	Efficiency	J_{SC}	V_{oc}	FF	$dV/dJ@V_{oc}$	$dJ/dV@J_{sc}$	good	# of		
(˚C)	(%)	(mA/cm^2)	(V)	(%)	(Ω-cm^2)	(mS/cm^2)	cells*	cells	Test Date	Sample #
600	14.56±0.34	33.4±0.3	0.610±0.003	71.4±0.9	1.5±0.0	2.4±0.5	5	5	22-May-97	32774-32
600	12.41±1.09	31.9±0.9	0.600±0.010	64.9±5.4	2.0±0.3	2.4±1.3	4	6	22-May-97	32774-33
600	11.39±0.91	30.7±0.3	0.593±0.011	62.6±4.0	2.2±0.2	3.5±0.7	4	6	11-Apr-97	32774-23
600	10.69±0.55	28.7±0.3	0.625±0.009	59.6±2.6	2.8±0.3	3.8±0.4	5	6	12-Jun-97	32774-22
550	13.74±0.68	32.9±1.3	0.585±0.002	71.4±0.7	1.7±0.1	1.1±0.6	6	6	22-Sep-97	32808-32
550	11.47±0.48	29.3±0.4	0.566±0.009	69.2±0.9	1.9±0.0	1.5±0.9	6	6	16-Sep-97	32808-23
500	13.22±0.42	32.0±0.6	0.603±0.004	68.6±0.8	1.8±0.1	1.8±0.5	3	3	20-May-97	32773-32
500	12.78±0.20	30.2±0.1	0.606±0.002	69.9±0.9	1.8±0.0	2.3±1.1	6	6	18-Apr-97	32773-33
500	11.58±0.44	29.6±0.6	0.598±0.003	65.3±1.3	2.3±0.0	3.6±1.6	6	6	16-Apr-97	32773-23
450	12.85±0.51	31.3±0.9	0.600±0.006	68.5±1.0	1.9±0.1	1.8±0.6	6	6	19-Sep-97	32797-33
450	10.01±1.18	29.4±1.6	0.539±0.019	62.9±2.5	2.6±0.4	2.7±0.6	6	6	16-Sep-97	32797-23
400	13.09±0.69	34.4±0.6	0.603±0.004	63.0±3.2	2.1±0.1	7.0±3.6	6	6	22-May-97	32771-23
400	12.32±0.42	31.2±1.2	0.611±0.002	64.7±0.9	2.4±0.2	2.6±0.3	3	3	20-May-97	32771-23
400	12.15±0.39	31.6±0.9	0.585±0.003	65.8±0.8	2.3±0.0	2.7±1.2	4	5	12-Jun-97	32771-22
400	11.93±0.48	30.0±1.1	0.587±0.004	67.7±0.6	1.9±0.0	2.6±0.8	5	6	20-May-97	32771-33
400	11.78±1.40	32.0±0.9	0.576±0.008	63.7±5.0	2.1±0.3	4.1±1.7	2	4	11-Apr-97	32771-32
400	10.77±0.40	27.9±0.3	0.580±0.002	66.6±1.8	2.0±0.1	3.7±1.0	6	6	05-Jun-97	32771-13
350	10.56±0.21	33.4±0.8	0.557±0.013	56.8±1.2	2.5±0.1	5.7±0.2	2	3	20-May-97	32780-33
350							0	6		

Table 2.6 Statistics of all the device J-V parameters for each sample made into cells as a function of Cu(InGa)Se_2 thickness. Parameters were taken from the best average efficiency test. *Shorted or heavily shunted (dJ/dV @ $J_{sc} \geq 25$ mS/cm^2) not included in the statistics.

Thick-ness	Average ± Standard Deviation						# of good	total # of		
	Efficiency	J_{SC}	V_{oc}	FF	dV/dJ@V_{oc}	dJ/dV@J_{sc}				
(μm)	(%)	(mA/cm^2)	(V)	(%)	(Ω-cm^2)	(mS/cm^2)	cells*	cells	Test Date	Sample #
2.5	12.85±0.51	31.3±0.9	0.600±0.006	68.5±1.0	1.9±0.1	1.8±0.6	6	6	19-Sep-97	32797-33
2.5	12.39±0.54	32.1±1.3	0.572±0.004	67.6±0.9	1.8±0.0	2.3±1.0	5	6	28-Aug-97	32798-32
2.5	11.39±0.77	30.5±0.7	0.558±0.010	66.9±3.5	1.9±0.1	3.7±4.5	6	6	28-Aug-97	32798-23
2.5	10.01±1.18	29.4±1.6	0.539±0.019	62.9±2.5	2.6±0.4	2.7±0.6	6	6	16-Sep-97	32797-23
1.8	12.90±0.78	33.2±1.7	0.582±0.003	66.9±0.8	1.8±0.2	2.4±1.3	4	6	16-Sep-97	32800-23
1.8	11.78±1.90	33.1±1.4	0.552±0.008	64.3±8.4	1.9±0.4	6.0±7.8	5	6	16-Sep-97	32801-32
1.8	10.59±0.41	30.0±0.6	0.546±0.006	64.7±2.2	2.2±0.2	2.7±1.8	6	6	10-Sep-97	32800-13
1.8	10.55±0.12	29.4±0.2	0.522±0.001	68.6±0.4	1.9±0.0	2.0±0.7	5	6	5-Sep-97	32801-23
1.8	9.90±0.30	28.6±0.2	0.527±0.006	65.6±0.9	2.2±0.0	3.0±1.0	6	6	11-Sep-97	32801-13
1.8							0	6	5-Sep-97	32800-32
1.4	13.12±0.12	32.1±0.2	0.594±0.000	68.8±0.7	1.9±0.1	1.8±1.2	3	6	20-May-97	32777-32
1.4	11.42±0.41	31.5±0.3	0.558±0.005	65.0±1.8	2.2±0.0	3.1±1.8	5	6	16-Apr-97	32776-23
1.4	10.90±0.55	30.3±0.0	0.543±0.004	66.4±2.8	2.0±0.0	3.4±2.9	4	6	15-Apr-97	32777-23
1.4	10.25±2.42	31.3±0.7	0.528±0.033	61.2±11.4	2.7±1.3	4.8±6.7	6	6	16-Apr-97	32776-32
1.2	10.64±0.51	31.7±1.2	0.509±0.004	66.0±2.2	1.8±0.0	4.1±2.9	6	6	16-Sep-97	32802-23
1.2	10.50±1.00	31.7±2.4	0.525±0.005	63.0±2.1	2.1±0.2	5.5±1.8	6	6	19-Sep-97	32806-32
1.2	8.71±0.42	28.6±0.6	0.483±0.005	63.1±1.5	2.2±0.1	5.2±1.8	5	6	10-Sep-97	32802-13
1.2	8.17±0.76	28.0±0.6	0.479±0.011	61.0±5.2	2.5±0.2	7.0±6.6	6	6	12-Sep-97	32806-23
1.2	7.16±1.04	28.5±0.8	0.434±0.038	57.6±2.0	2.3±0.0	10.8±1.9	4	6	8-Sep-97	32802-32
1.0	9.10±0.62	28.8±1.4	0.507±0.009	62.3±3.1	2.7±0.6	5.6±2.1	6	6	16-Sep-97	32803-13
1.0	8.63±0.68	27.9±1.3	0.489±0.013	63.2±2.4	2.3±0.2	5.0±2.0	6	6	15-Sep-97	32805-23
1.0	8.46±0.63	29.3±1.4	0.482±0.007	60.0±4.3	2.1±0.2	7.6±1.7	6	6	8-Sep-97	32803-23
1.0	4.96±0.76	27.8±1.1	0.367±0.038	48.6±2.9	3.1±0.5	18.2±3.8	3	6	15-Sep-97	32805-32
1.0							0	6	8-Sep-97	32803-32

2.3 Teaming Results

2.3.1 Introduction

IEC is a member of the National CIS Team under the NREL Thin Film Partnership Program. The CIS Team effort includes four working groups (WG). Of these, IEC has been a member of the Transient Effects WG and the New Junction WG, for which William Shafarman is the Group Leader. The work done at IEC for each of these Working Groups is described below.

2.3.2 New junction results

The New Junction WG has identified two tasks and IEC has contributed to work on each. The objective of the first task is to develop non-cadmium containing buffer layers. The priority is on

vacuum processes which could potentially be incorporated in-line and chemical bath deposition is not considered a primary option. The objective of the second task is to develop improved TCO layers to minimize losses for module fabrication and quantify the effect of TCO layers on module performance. This task is focusing on the high conductivity TCO layers.

For the first task, IEC provided device fabrication and J-V and QE measurements for $Cu(InGa)Se_2$/ZnO samples provided by other team members. This included ZnO layers deposited by MOCVD at Washington State University (WSU), by dc reactive sputtering at University of South Florida (USF), and by rf sputtering from a $ZnO:Al_2O_3$ target. Samples were processed with and without a solvent/water rinse prior to ZnO deposition. These layers were deposited on $Cu(InGa)Se_2$ films provided by NREL and EPV. Device completion included deposition of our baseline ZnO:Al, deposition of Ni contacts or a Ni/Al grid, and mechanical scribing. IEC also did experiments to compare the effect of sputtering from a $ZnO:Al_2O_3$ target in different atmospheres.

A summary of the J-V tests on $Cu(InGa)Se_2$/ZnO cells completed at IEC is given in Table 2.7. In the table, R_{oc} is the slope dV/dJ at J = 0 and G_{sc} is the slope dJ/dV at V = 0. All measurements in this case are active area results with no AR layers on the cells. The results include a $Cu(InGa)Se_2$/ZnO device with the MOCVD i-ZnO from WSU on $Cu(InGa)Se_2$ deposited at NREL with 13.9% efficiency. J-V and QE curves for this device and a description of the process for the i-ZnO deposition for are described in [118]. The growth includes an initial growth step at 250˚C with flowing hydrogen. An additional set of 10 samples with the MOCVD i-ZnO on absorber layers from NREL and SSI, completed and tested at IEC, showed that this first step was necessary for good device performance [118].

Results shown in Table 2.7 where the i-ZnO layers were deposited by EPV in $Ar:O_2$ indicate shorted devices while i-ZnO deposited in $Ar:H_2$ gave up to $\eta = 9\%$. An experiment to determine whether the H_2 plays a beneficial role in this process or whether merely the absence of O_2 in the sputter gas is critical was addressed in a set of devices fabricated completely at IEC. Previous results with a high resistivity (~100 Ω-cm) ZnO buffer layer deposited by sputtering from the $ZnO:Al_2O_3$ target in Ar/O_2 with 2% O_2 gave shorted devices. Devices were fabricated with absorber films from a single deposition of evaporated $Cu(InGa)Se_2$ with $Ga/(In+Ga) \approx 0.25$. ZnO layers were sputtered in either pure Ar or $Ar:H_2$ with 4% H_2. All cells, including a control sample with a CdS buffer layer deposited by CBD, had a 0.5 μm thick ZnO layer sputtered in Ar as the primary TCO layer deposited on top of the buffer layer. In each case, the best device had $\eta = 8\%$ as shown in Table 2.8, while the control sample gave $\eta = 13\%$. The $Cu(InGa)Se_2$/ZnO samples had poor reproducibility over the 12 devices on two pieces with each buffer layer, primarily due to shunting in the dark and illuminated J-V characteristics. These preliminary results show no advantage to the presence of H_2.

Under the second task, "Improved TCO Layers," the New Junction WG has focused on an observed increase in ZnO sheet resistance when it is deposited on CdS. This was shown at IEC for different TCO materials deposited on glass and glass/CdS substrates. The samples include single layer low resistivity ZnO:Al, bi-layer high /low resistivity ZnO:Al, and ITO. The CdS was our standard CBD film deposited in a double dip to give thickness ~70 nm The average sheet resistance of each sample type is given in Table 2.9. In each case the resistance of the ZnO deposited on CdS is higher than that deposited on bare glass. Optical transmission and reflection of each sample were also measured at IEC. These samples were sent for FTIR, atomic force microscopy, and Hall effect measurements at the Universities of Florida and South Florida.

Two different experiments at IEC confirmed that the increase in ZnO resistance also occurs when the CdS/ZnO layers are deposited on $Cu(InGa)Se_2$. The sheet resistance of the ZnO in a complete glass/Mo/$Cu(InGa)Se_2$/CdS/ZnO structure was measured on working devices. This was done by fabricating devices with two separate Ni contact tabs deposited on the ZnO and measuring the J-V curve between them with a bias voltage maintained between the front of the device and the Mo back

contact. The tab-to-tab resistance does not change with the bias voltage confirming that there is no significant leakage through the device and the measured resistance is due to the ZnO. The sheet resistance is then given by

$$R_{sq} = R_{tab-to-tab}\left(\frac{l}{w}\right) \qquad (2.2)$$

where l = 0.52 cm is the cell width and w = 0.25 cm is the spacing between the contact tabs. On a typical device, #32744.32, for which the ZnO witness slide gave R_{sq} = 18 Ω/sq, the tab-to-tab measurement in the device gave R_{sq} = 29 Ω/sq, similar to the increase seen on the glass/CdS samples.

Table 2.7 J-V parameters for Cu(InGa)Se_2/ZnO devices completed and tested at IEC.

Cu(InGa)Se_2		i-ZnO		Best Cell					
pc. #	pre-rinse	source	process	V_{oc} (V)	J_{sc} (mA/cm^2)	FF (%)	eff (%)	R_{oc} (Ω-cm^2)	G_{sc} (mS/cm^2)
NREL 675-2	yes	WSU	MOCVD	0.529	33.1	55.6	9.7	2.3	10.
NREL 679-9	yes	WSU	MOCVD	0.524	33.5	69.5	12.2	1.6	1.
EPV 716-3-1	yes	WSU	MOCVD	shorted					
EPV 709-1-1	yes	WSU	MOCVD	0.411	33.5	62.5	8.6	1.5	6.
NREL681-5	-	WSU	MOCVD	0.267	25.4	32.7	2.2	6.4	50.
NREL 679-5	yes	WSU	MOCVD	0.581	34.5	69.2	13.9	1.9	2.
EPV 716-3-2	yes	WSU	MOCVD	0.426	37.1	61.0	9.6	1.5	6.
EPV 709-1-2	-	WSU	MOCVD	0.412	37.7	56.3	8.8	2.0	6.
NREL 681-4	yes	USF	react-sp	0.082	21.8	29.3	0.5	2.8	180
NREL 680-8	-	USF	react-sp	0.083	2.9	28.1	0.1	21.4	29
EPV 709-2-6	yes	USF	react-sp	0.085	24.3	28.1	0.6	2.8	225
EPV 709-1-5	-	USF	react-sp	0.115	18.8	29.6	0.6	4.3	120
EPV 709-2-1	yes	EPV	sput Ar:O_2	shorted					
NREL 680-3	yes	EPV	sput Ar:O_2	shorted					
EPV 709-2-4	-	EPV	sput Ar:O_2	shorted					
NREL 680-4	-	EPV	sput Ar:O_2	flaked off					
EPV 709-2-3	yes	EPV	sput Ar:H_2	0.127	23.9	33.3	1.0	3.0	96.
EPV 706-3-3	yes	EPV	sput Ar:H_2	0.107	22.5	32.9	0.8	2.8	112.
NREL 679-8	yes	EPV	sput Ar:H_2	0.386	26.4	45.5	4.6	3.7	16.
EPV 709-2-2	-	EPV	sput Ar:H_2	0.125	25.0	31.4	1.0	3.3	123.
NREL 679-4	-	EPV	sput Ar:H_2	0.501	29.2	62.0	9.1	2.1	2.

Table 2.8 Device results with ZnO buffer layers deposited on Cu(InGa)Se_2 in Ar and Ar:H_2 sputter gases.

pc. #	CdS	ZnO:Al deposition	V_{oc} (V)	J_{sc} (mA/cm^2)	FF (%)	η (%)
32814.21	CdS	Ar	0.560	31.1	73.2	12.7
32814.22	none	Ar	0.538	24.3	61.8	8.1
32814.11	none	Ar:H_2	0.488	26.1	61.2	7.8

Table 2.9 Sheet resistances of different TCO materials deposited on glass and glass/CdS substrates.

	R_{sq} (Ω/sq)	
TCO	on glass	on glass/CdS
bi-layer ZnO	18	25
single layer ZnO	26	35
ITO	20	30

2.3.3 Transient Effects

2.3.3.1 Introduction

The $CuInSe_2$ thin film partnership program organized a transient effects team to determine if present I-V testing procedures can predict the daily output of $CuInSe_2$-based modules and cells under field conditions; and, if they cannot, determine what new testing procedures are needed.

2.3.3.2 Initial Tests

As a start, it was decided to stress (with temperature, illumination and electrical bias) one of IEC's Cu(In,Ga)Se_2 devices for a period of hours and monitor its recovery.

This device stressed at a temperature of 80˚C with and without illumination (approximately 88 mW/cm^2) under various conditions of electrical bias (-0.5 V, 0.0 V, ~ maximum power, 0.0 mA/cm^2 and +30 mA/cm^2). After each stress, the illumination and voltage bias was removed and they were brought to room temperature in about 3 minutes. Their recovery was monitored by measuring and analyzing their J-V behavior at three different light intensities plus dark at logarithmically spaced time intervals.

The IEC Cu(InGa)Se_2 device (IEC-32702-32-7) was put through this stress sequence. Over the time it was stressed and monitored, the only significant change was the development of a shunt when held in reverse bias. The J-V results of these stress tests are shown in Figure 2.9 to Figure 2.16.

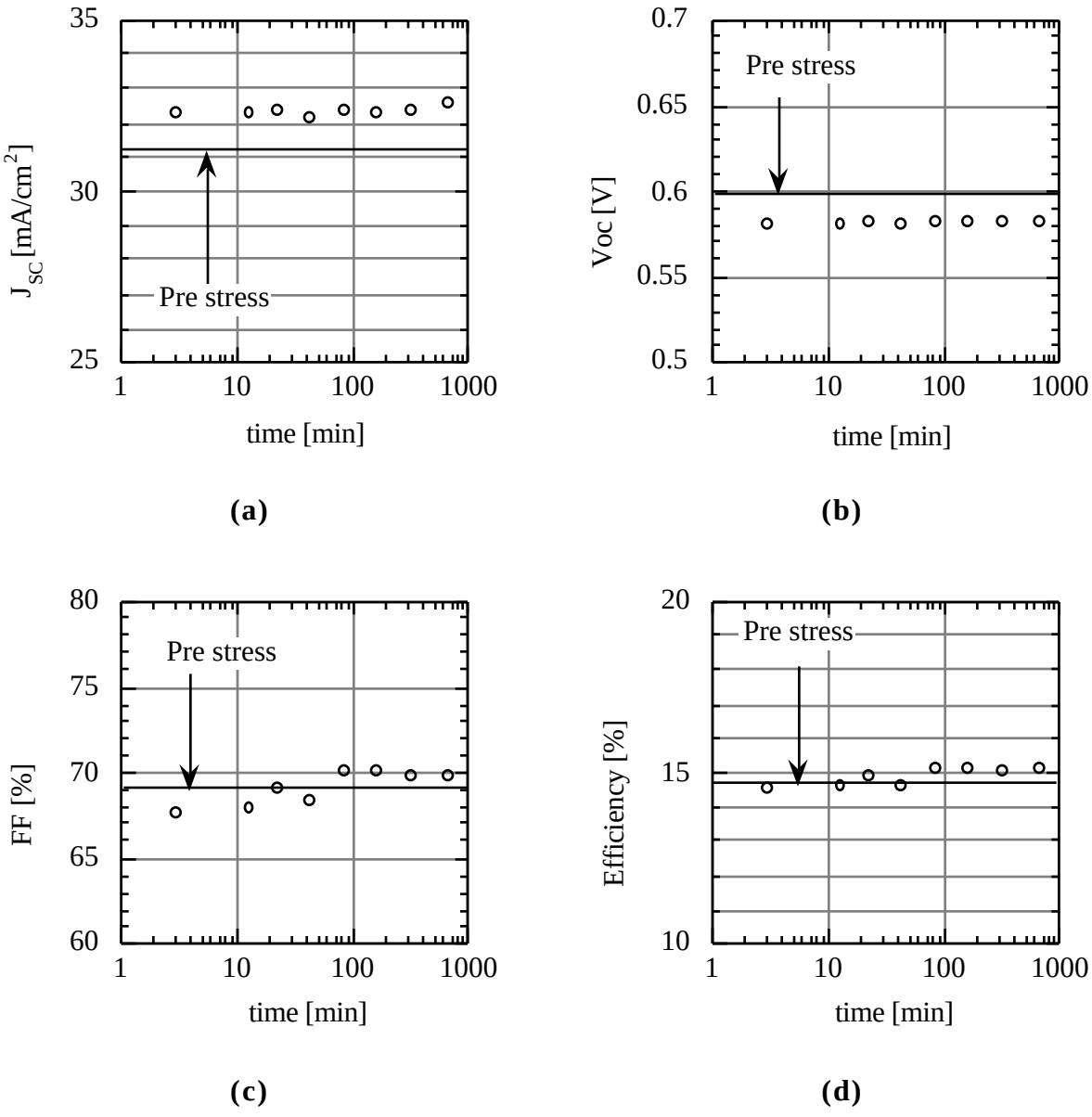


Figure 2.9 J_{sc}, V_{oc}, FF and efficiency vs. recovery time for device IEC-32702-32-7 after stress at a temperature of 80˚C, in the dark and 0 V for 12 hours.

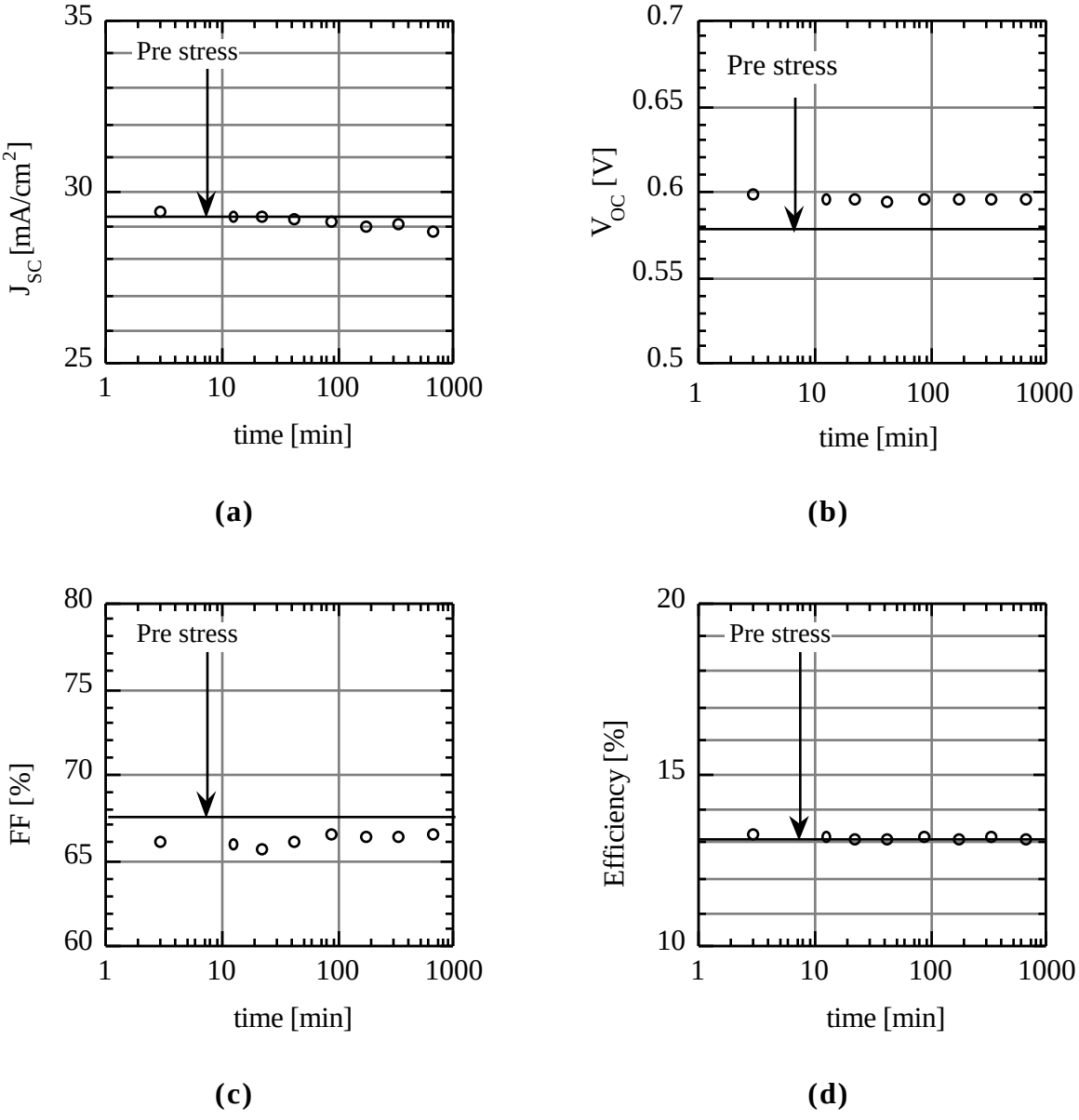


Figure 2.10 J_{sc}, V_{oc}, FF and efficiency vs. recovery time for device IEC-32702-32-7 after stress at a temperature of 80˚C, in the dark and at a forward current of 30 mA/cm^2 for 10 hours.

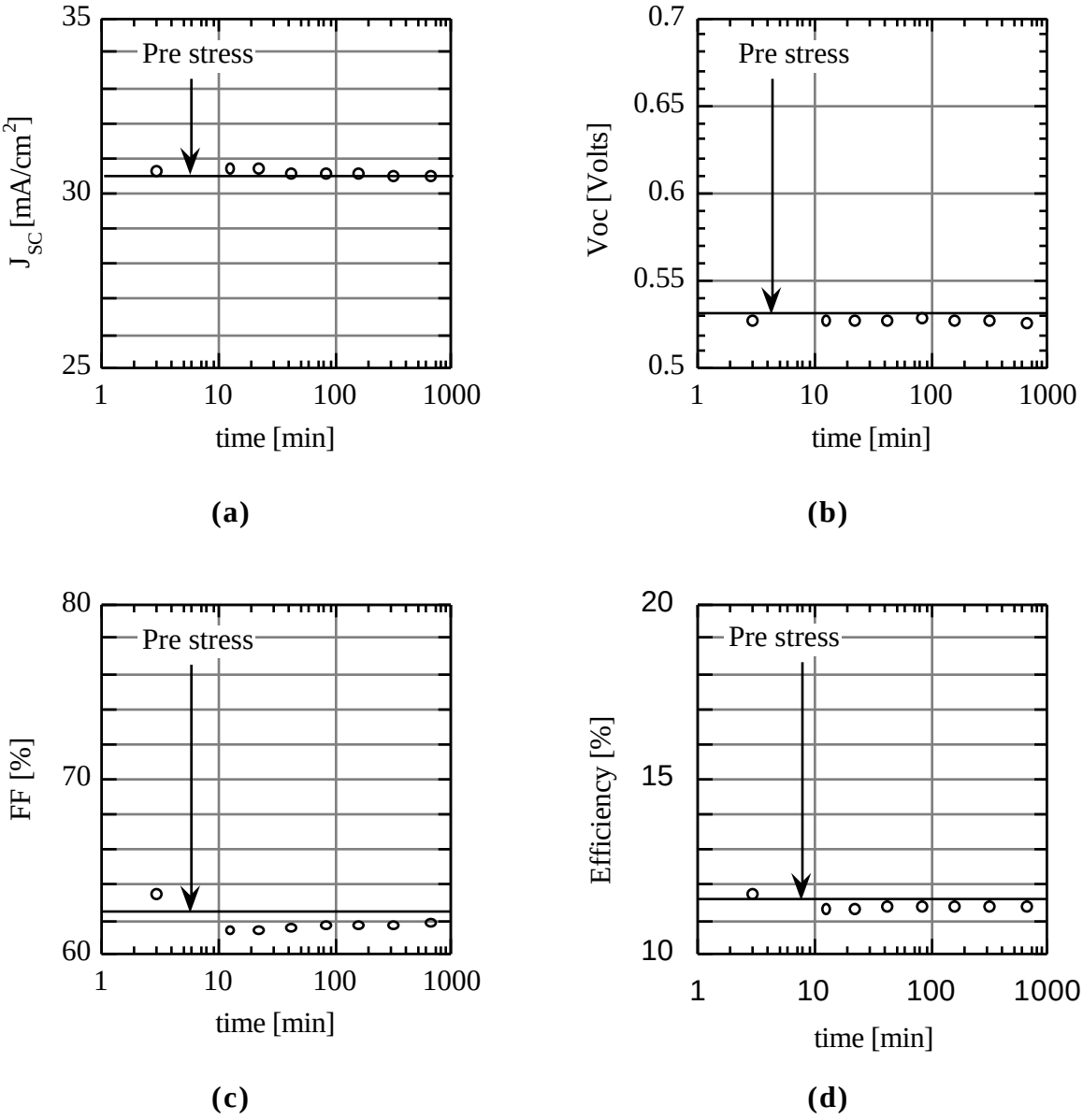


Figure 2.11 J_{sc}, V_{oc}, FF and efficiency vs. recovery time for device IEC-32702-32-7 after stress at a temperature of 80˚C, in the dark and at V = -0.5 V for 12 hours.[*]

[*] Still shunted from a previous stress test.

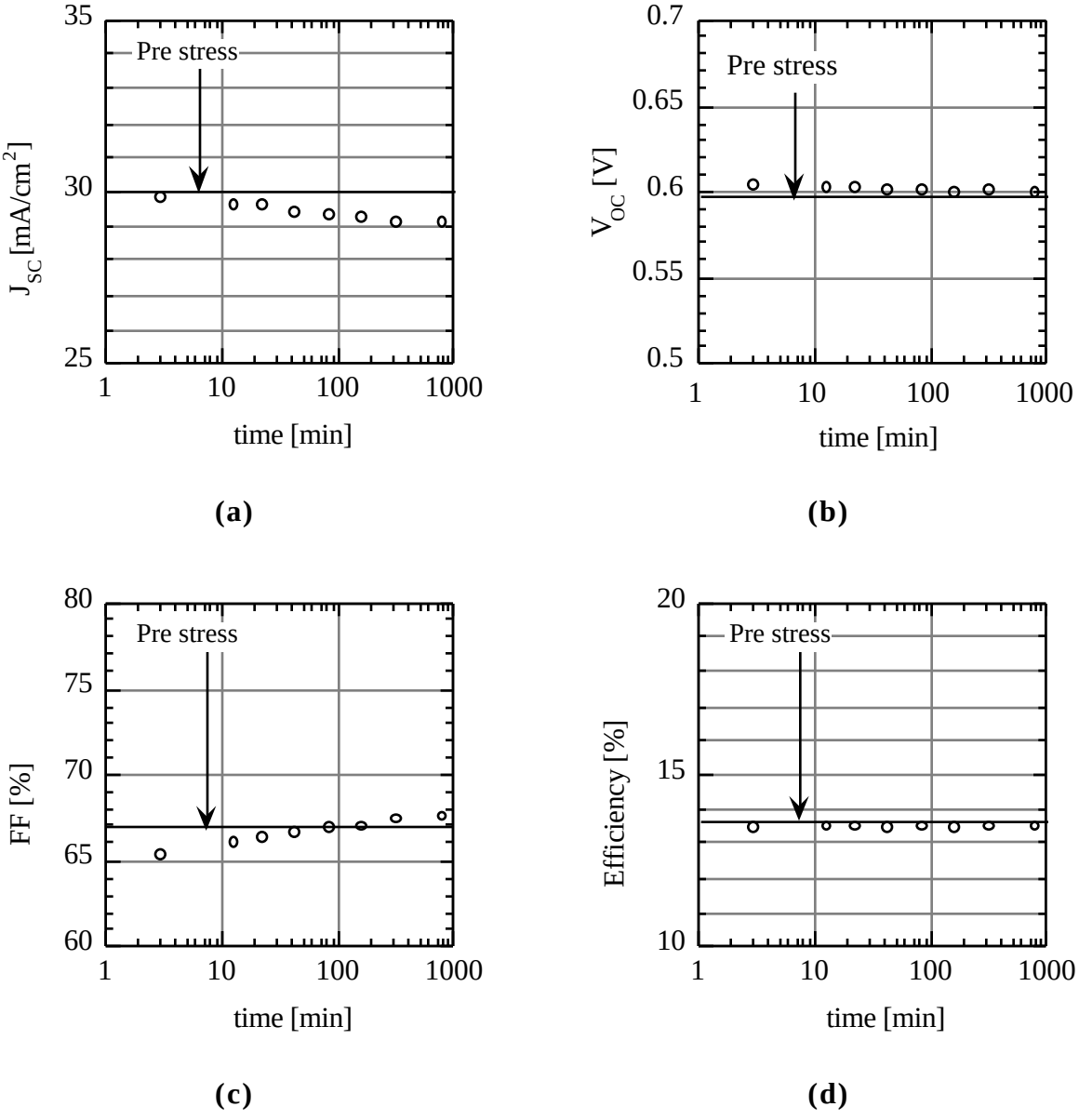


Figure 2.12 J_{sc}, V_{oc}, FF and efficiency vs. recovery time for device IEC-32702-32-7 after stress at a temperature of 80˚C, AM1 illumination and at a forward current of mA/cm^2 for 12 hours.

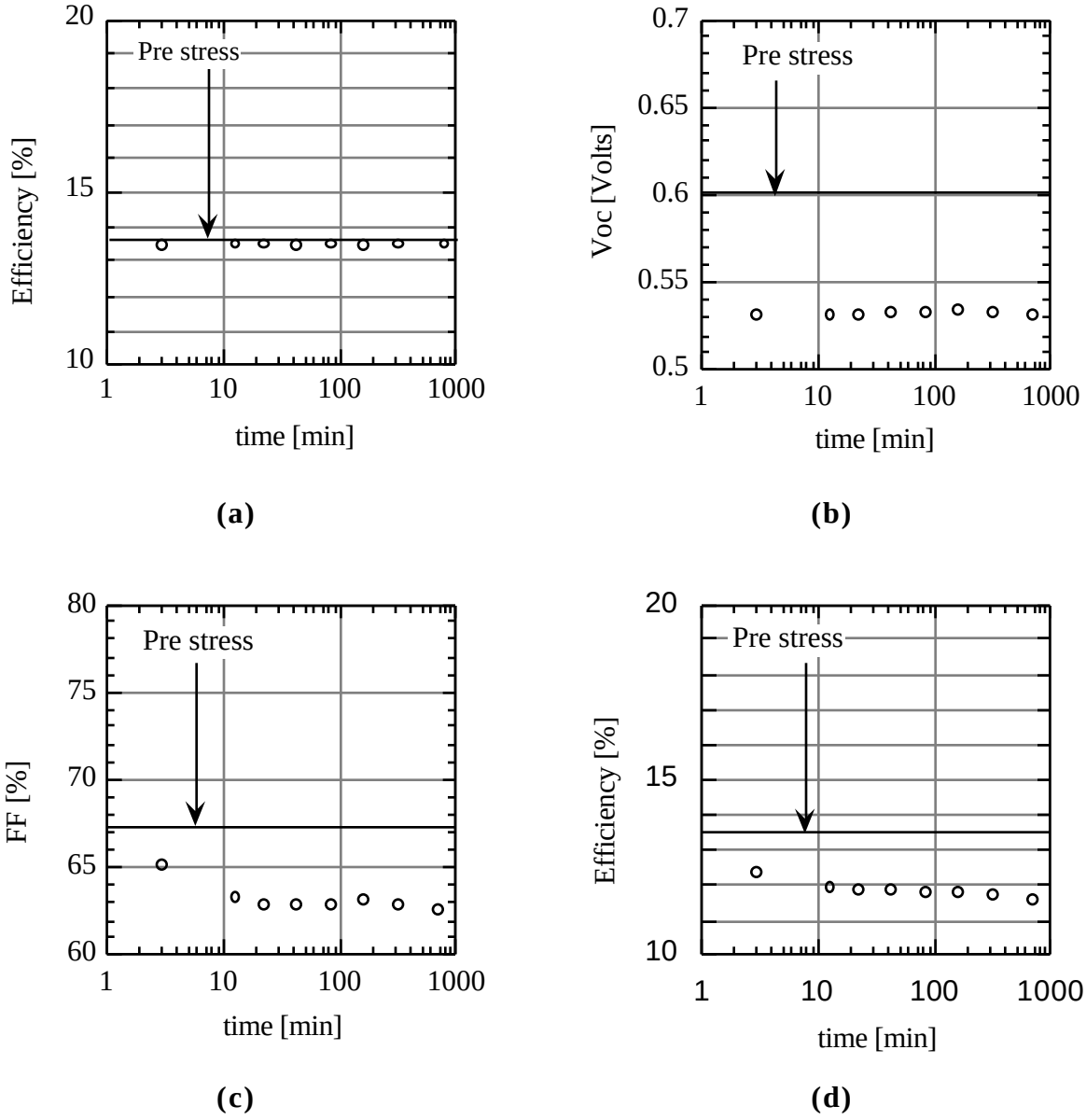


Figure 2.13 J_{sc}, V_{oc}, FF and efficiency vs. recovery time for device IEC-32702-32-7 after stress at a temperature of 80˚C, AM1 illumination and at V = -0.5 V for 12 hours.[*]

[*] Shunt developed during stress test.

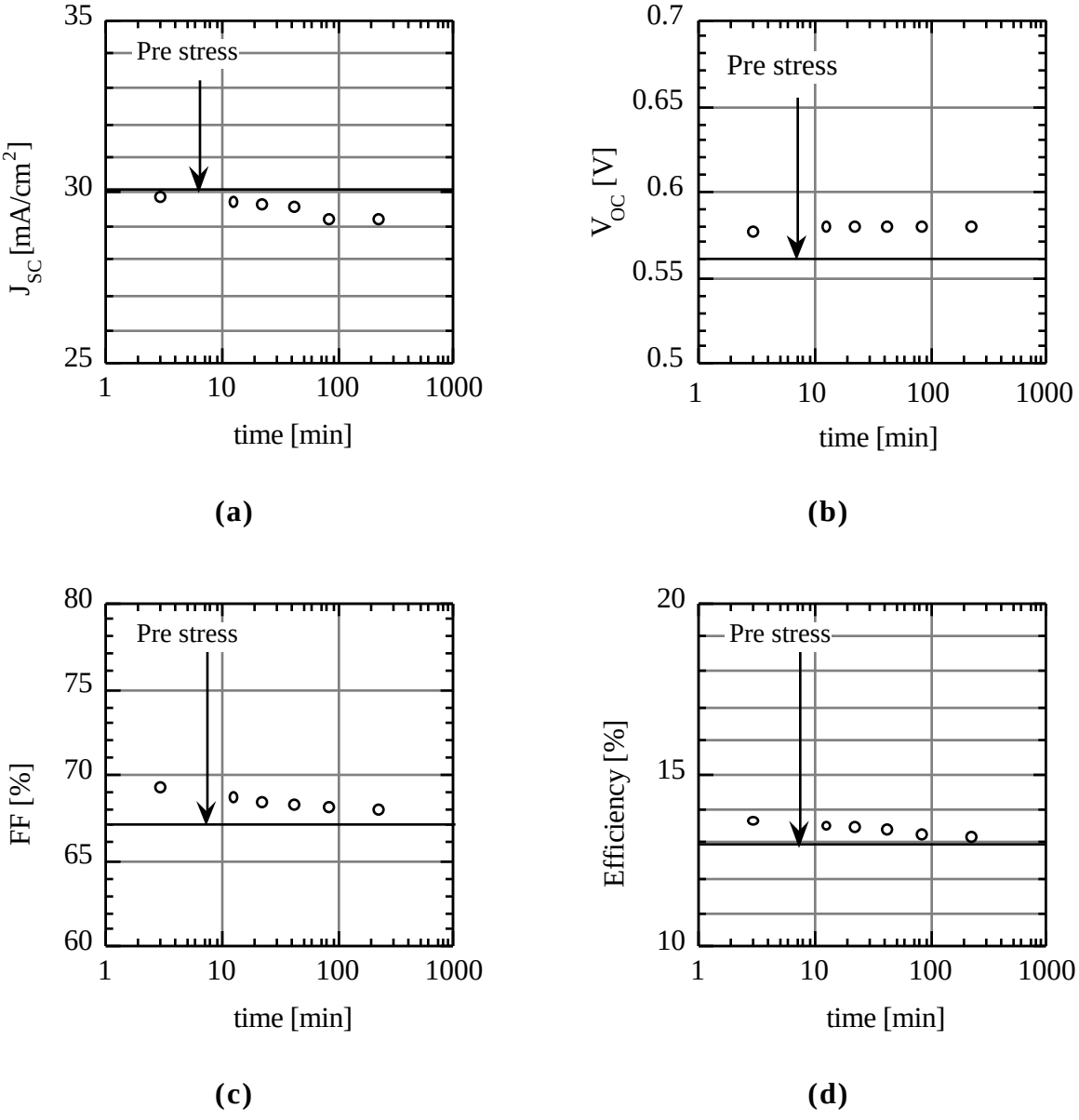


Figure 2.14 J_{sc}, V_{oc}, FF and efficiency vs. recovery time for device IEC-32702-32-7 after stress at a temperature of 80˚C, AM1 illumination and R_L = 12.6 Ω-cm^2 for 10 hours.

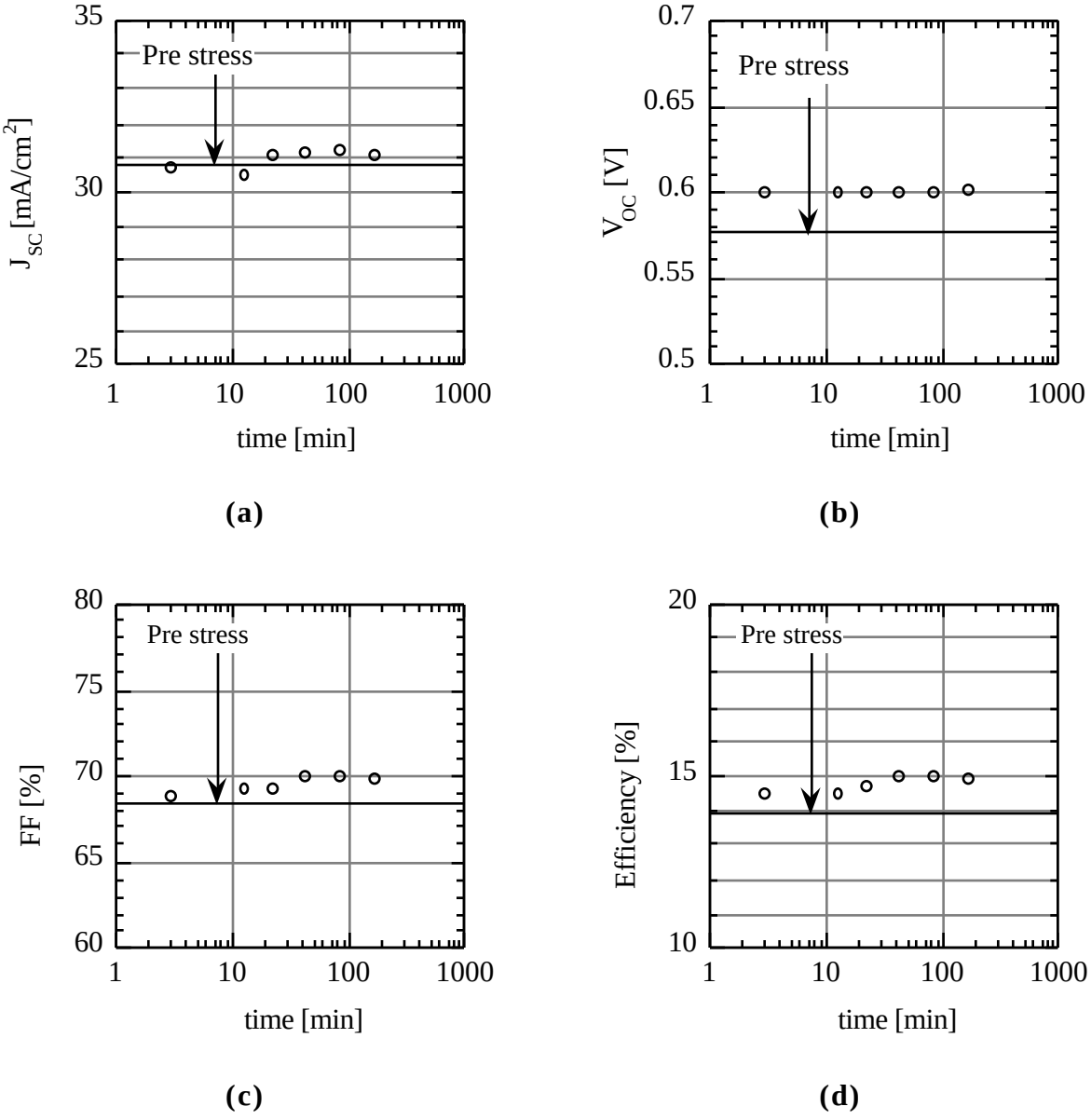


Figure 2.15 J_{sc}, V_{oc}, FF and efficiency vs. recovery time for device IEC-32702-32-7 after stress at a temperature of 80˚C, AM1 illumination and at V_{oc} for 8.5 hours.

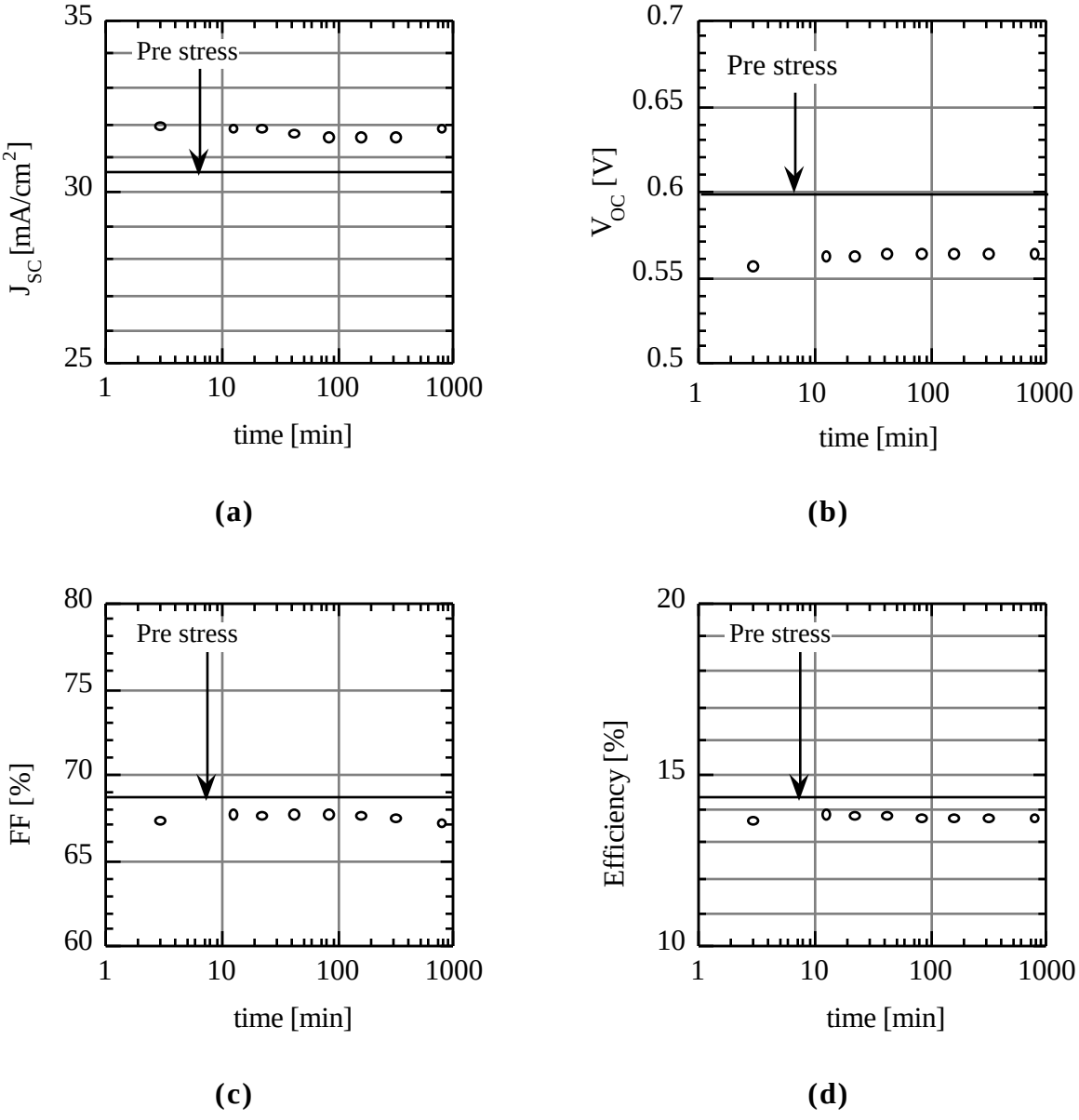


Figure 2.16 J_{sc}, V_{oc}, FF and efficiency vs. recovery time for device IEC-32702-32-7 after stress at a temperature of 80˚C, AM1 illumination and at J_{sc} for 11 hours.

2.3.3.3 Siemens Solar Industries Devices

Attempts have also been made to duplicate and analyze the transient behavior Siemens Solar Industries $CuInSe_2$-based devices undergo during lamination. This transient behavior is characterized by a loss in efficiency which slowly recovers if illuminated at open circuit conditions. The lamination cycle is replicated by subjecting the devices to a temperature of 85˚C for a period of 16 hours while unconnected in the dark. The recovery @ 25˚C under various conditions is being

monitored by periodically measuring and analyzing the J-V behavior at four different light intensities (including dark).

Figure 2.17 is a picture of a typical substrate supplied by Siemens Solar Industries. Each substrate contains two delineated solar cells with an approximate area of 1.0 cm^2. Figure 2.18 shows the transient effects of the lamination cycle (T = 85˚C, t = 16 hrs., Ill. = Dark) on the efficiency of one of these solar cells. The recovery illumination (except for J-V tests) is supplied by ELH lights and set to approximately 88 mw/cm^2.

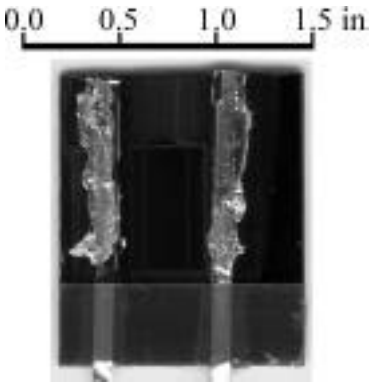


Figure 2.17 Picture of a Siemens Solar Industries substrate with two $CuInSe_2$-based solar cells (area ~ 1.0 cm^2).

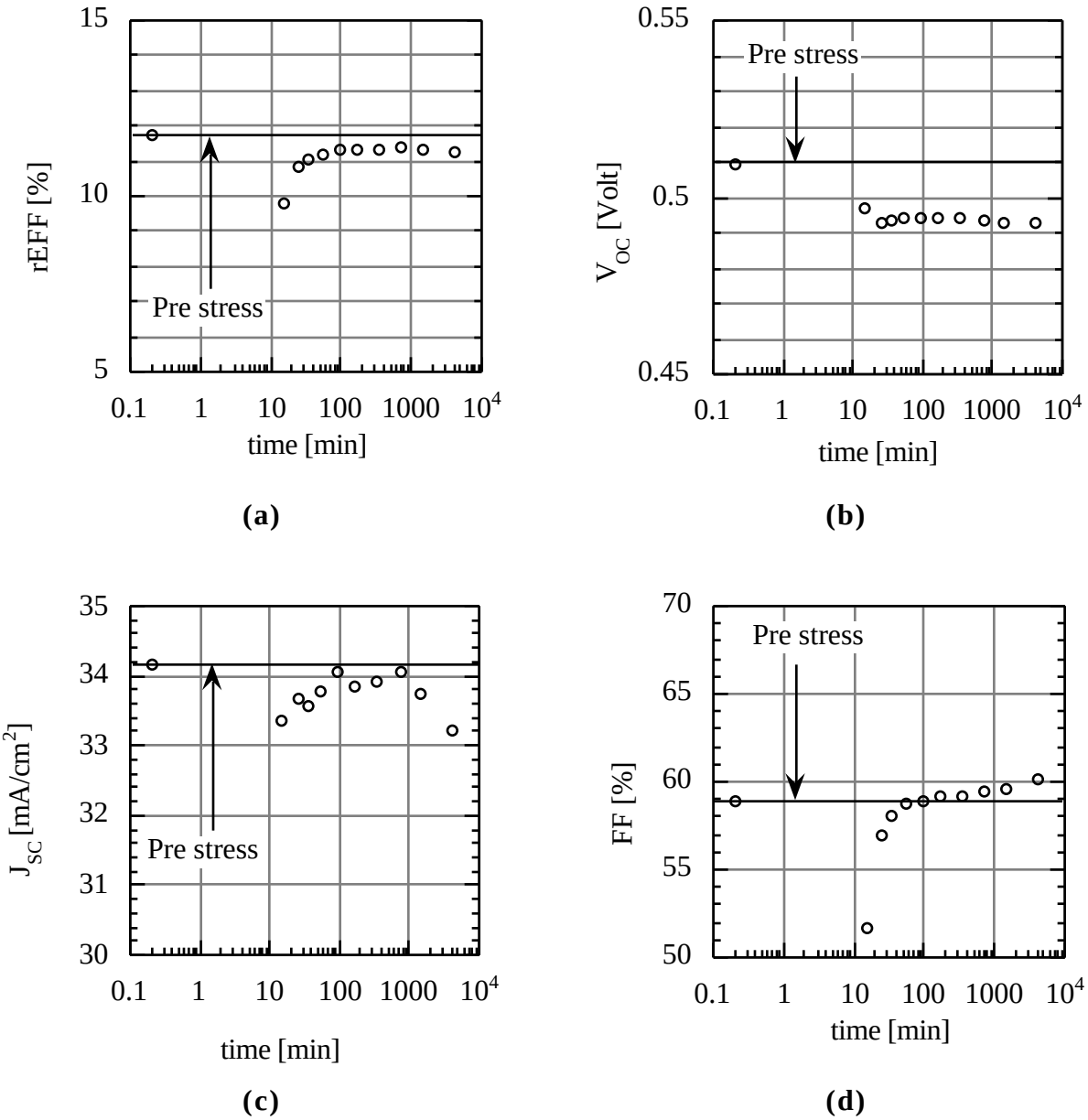


Figure 2.18 Efficiency, V_{oc}, J_{sc} and fill factor recovery under illumination at 25˚C of device SSI-255-F2 after being subject to a lamination cycle (see text).

The plots of J_{SC} and V_{OC} shown in Figure 2.18(b) & (c) demonstrate that this transient loss in efficiency is not due to either a change in light generated current or diode parameters.

Figure 2.18(d) shows that the transient loss in efficiency is largely due to a change in fill factor. As can be seen from the slope of the J-V curves (see Figure 2.19), the loss in fill factor is due to an increase in the series resistance (R_S).

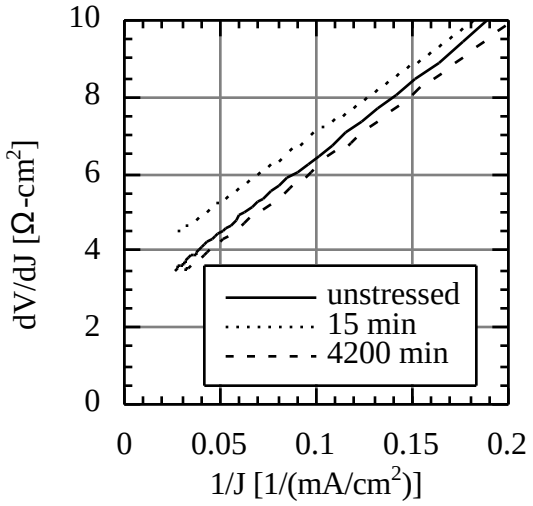


Figure 2.19 A plot of the slope of the J-V curve at various times during recovery (see text).

A plot of the transient behavior of the series resistance (R_S) is shown in Figure 2.20.

To determine whether this transient behavior in series resistance depends upon the type and intensity of illumination used during recovery, the devices were re-laminated and their recovery was followed in the dark and under "blue" and "red" illumination (Figure 2.24). The recovery of the series resistance (R_S) under the various illumination conditions is shown in Figure 2.21 to Figure 2.23.

The recovery data does suggest that the rate of recovery may be illumination and spectrally dependent. However, the interruption of illumination in order to make a complete set of J-V measurements obscures the results.

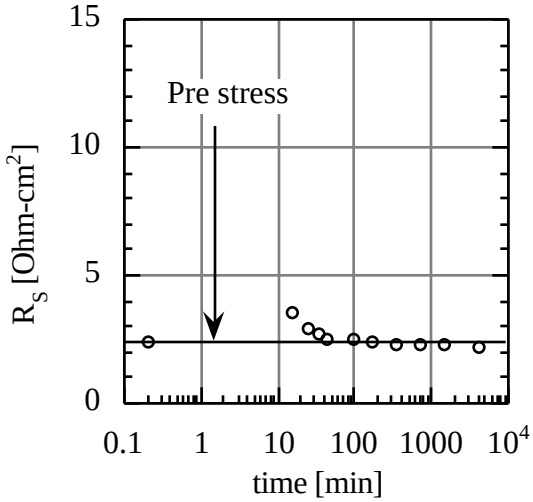


Figure 2.20 Series resistance recovery under illumination (see text).

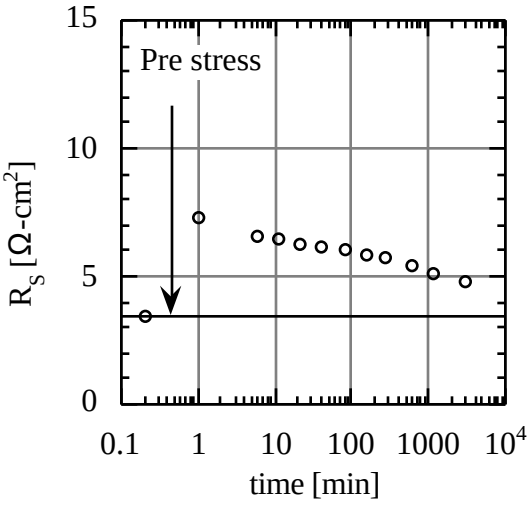


Figure 2.21 Series resistance recovery in the dark (except for J-V testing).

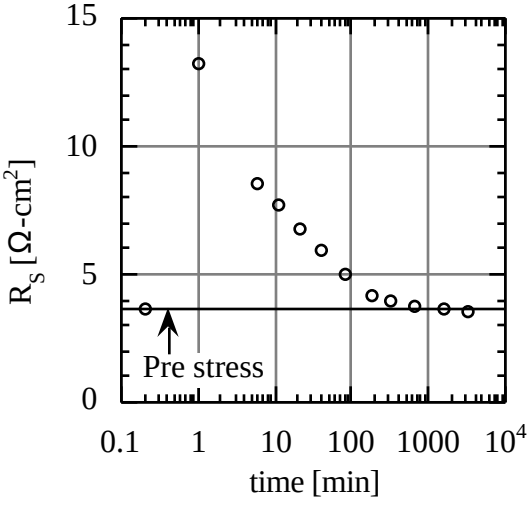


Figure 2.22 Series resistance recovery with "blue" light (except for J-V testing).

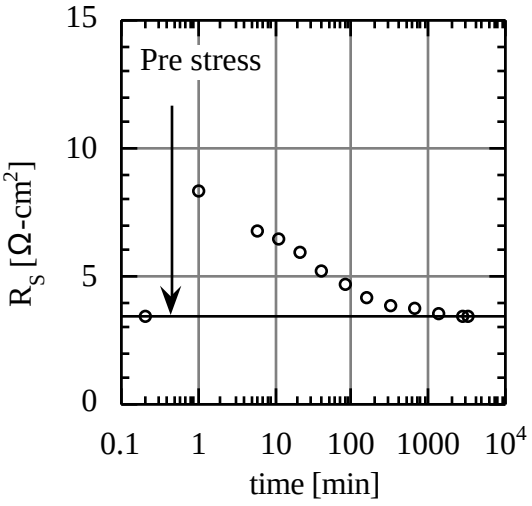


Figure 2.23 Series resistance recovery with "red" light (except for J-V testing).

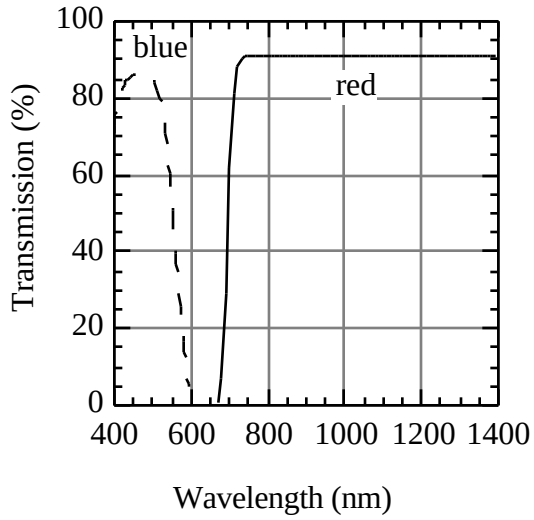


Figure 2.24 Transmission characteristics of the filters used to produce "blue" and "red" illumination.

2.3.3.4 Siemens Solar Industries Mini-modules

Similar experiments were also performed on SSI mini-modules. These 4 x 4" mini-modules consisted of 12 solar cells connected in series with an active area of ~ 50 cm^2. The same lamination cycle of heating the mini-modules to a temperature of 85˚C for a period of 16 hours while unconnected in the dark was used. The recovery @ 25˚C under various conditions is being monitored by periodically measuring and analyzing the J-V behavior while in the dark, under full illumination and under "red" light illumination. The I-V behavior of the mini-module recovering under full illumination had J-V measurements made at all four light intensities as the previous solar cells. The other two mini-modules only had dark J-V measurements made.

The basic J-V parameters of the mini-module during recovery under full illumination are shown in Figure 2.25.

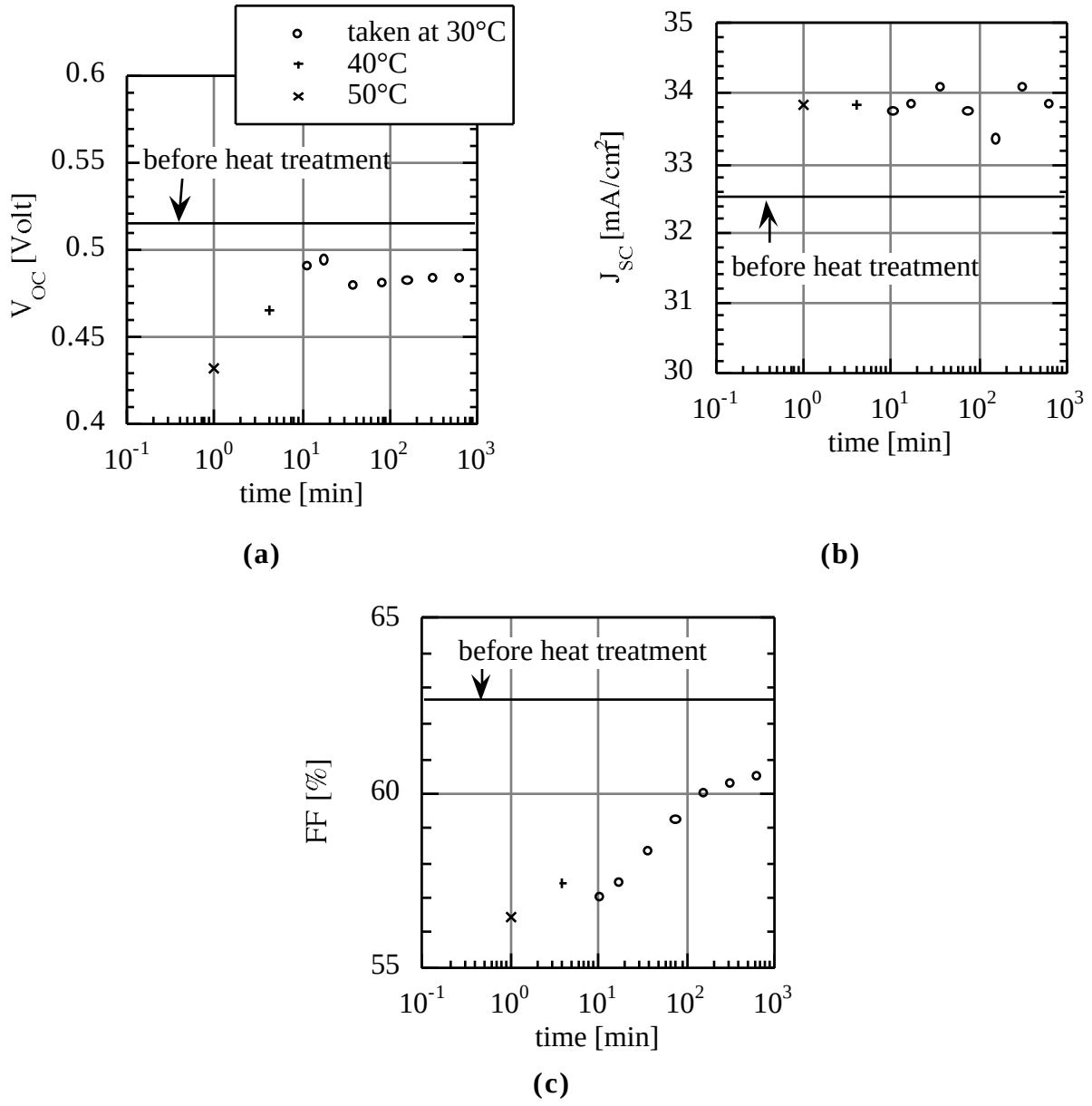


Figure 2.25 V_{oc}, J_{sc} and FF recovery under illumination at 30˚C of mini-module SSI-260-98 after being subject to a lamination cycle.

The mini-module recovery under illumination is similar to that of an individual solar cell. However, when the J-V data at different illumination intensities were analyzed, an unusual light dependent behavior in forward bias was noted (see Figure 2.26 to Figure 2.29). As can be seen, the a.c. resistance (or J-V slope) exhibits a dramatic and illumination dependent change at high forward currents. At present, we have no explanation for this. It has not been seen in any of the other solar cells or mini-modules we have tested.

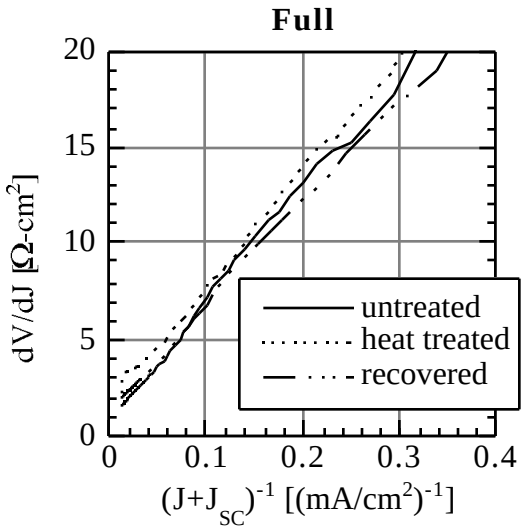


Figure 2.26 dV/dJ behavior of mini-module SSI-260-98 before and after lamination and after recovery at full illumination.

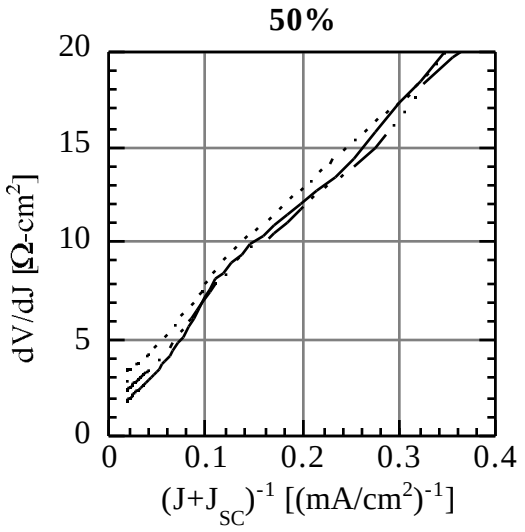


Figure 2.27 dV/dJ behavior of mini-module SSI-260-98 before and after lamination and after recovery at 50% illumination.

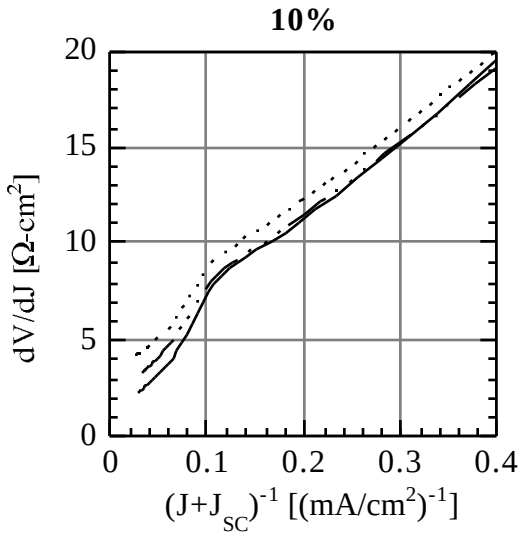


Figure 2.28 dV/dJ behavior of mini-module SSI-260-98 before and after lamination and after recovery at 10% illumination.

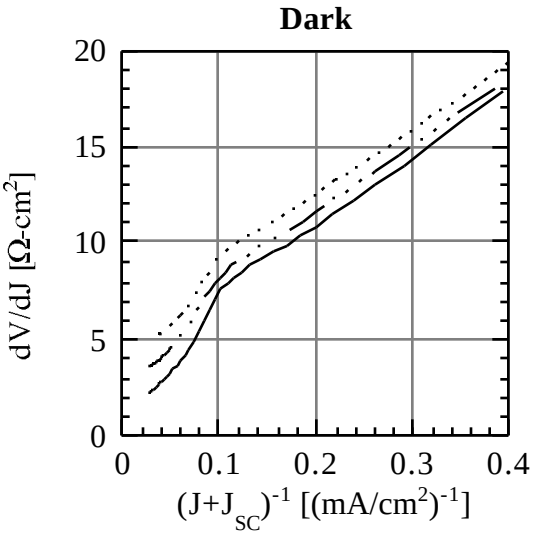


Figure 2.29 dV/dJ behavior of mini-module SSI-260-98 before and after lamination and after recovery in the dark.

The mini-modules recovered under dark and "red" illumination exhibited changes primarily in series resistance, R_S (the same as the solar cells). These changes are shown in Figure 2.30 to Figure 2.31. The transmission characteristics of the "red" filter is shown in Figure 2.32. In summary, the mini-module behavior, except for one with an unusual dV/dJ characteristic, is essentially the same as the individual solar cells.

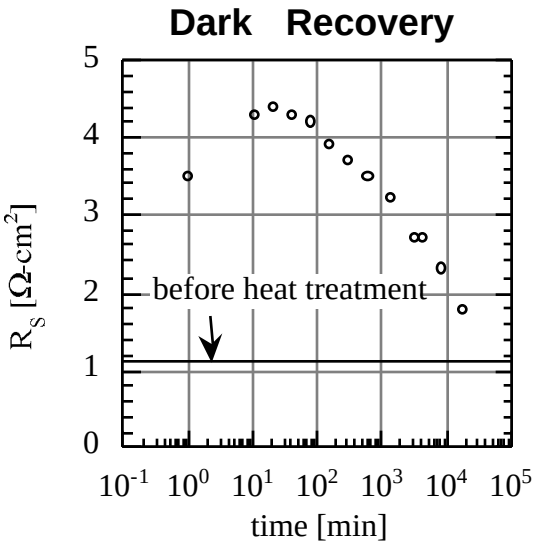


Figure 2.30 R_s recovery in the dark at 30˚C of mini-module SSI-260-108 after being subject to a lamination cycle.

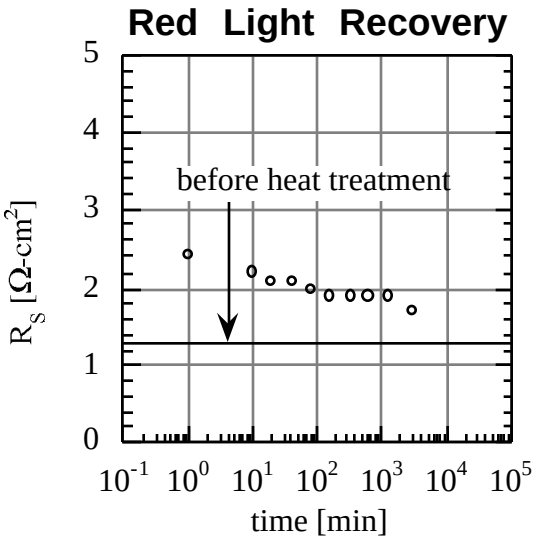


Figure 2.31 R_s recovery in "red" light at 30˚C of mini-module SSI-260-105 after being subject to a lamination cycle.

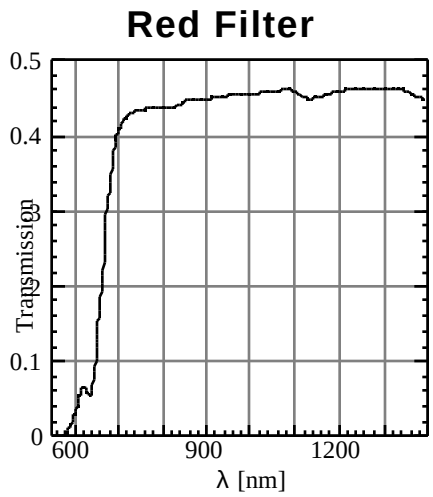


Figure 2.32 Transmission characteristics of the "red" filter used for the illumination of mini-module SSI-260-105.

2.3.3.5 Conclusions

In the SSI mini-modules, paralleling the transient behavior in FF caused by R_2 during the lamination cycle, Sites [119] has also found, from C-V measurements, a transient decrease in capacitance and conductance. The rate of recovery of the capacitance and conductance was also found to be dependent upon illumination.

Other groups [120, 121, 122] have noted similar behavior in Cu(In,Ga)Se_2 devices. These groups have suggested that the information is pointing to a persistent or long lived photoconductive effect in Cu(In,Ga)$(Se,S)_2$ semiconductors that is caused by the trapping of electrons in a high density of states below the conduction band which leads to p-type photoconductivity and long time constants. This is analogous to the defect photoconductivity that occurs in CdS.

3. a-Si:H-based Solar Cells

3.1 Summary

The focus of a-Si research was on contacts and interfaces. This work was motivated by results from the previous year which showed that the electrical behavior of the n-layer/TCO contact was critical to incorporating a high performance TCO/Ag back reflector and achieving efficiencies over 10% as described in Appendix 3. We investigated the current-voltage-temperature dependence of the following contacts, where TCO refers to sputtered ITO or ZnO: TCO/a-Si i-layer, TCO/a-Si n-layer, TCO/μc-Si n-layer, textured SnO_2/a-Si n-layer and textured SnO_2/μc-Si n-layer. Regarding the contact between sputtered TCO and a-Si i-layers, ITO has a larger barrier compared to ZnO. Thus, ITO makes a better junction, hence poorer Ohmic contact, with a-Si i-layers. Also, sputtering ZnO in Ar/O_2 gives a higher barrier and more blocking contact with a-Si compared to sputtering ZnO in Ar or Ar/H_2. Thus, the barrier between ZnO and a-Si depends on the ZnO sputtering conditions. It is not known if this is an interfacial or bulk effect. Regarding the contact between sputtered TCO and a-Si or μc-Si n-layers, it was found that the μc-Si n-layers have more nearly-Ohmic behavior with ITO, ZnO or SnO_2 contacts at T > 25˚C than do a-Si n-layers. The μc-Si n-layers have lower contact resistance than a-Si n-layers. JV behavior at T > 25°C with the a-Si or μc-Si n-layers was nearly independent of the various sputtered TCO contacts. We found that the a-Si n/SnO_2 contact is more blocking at T < 25°C than is the μc-Si n/SnO_2 contact. Thus, μc-Si n-layers are essential for good Ohmic contacts to TCO for either top or bottom contacts. Their high conductivity allows the decoupling of the electrical requirements for the contact from the optical requirements, and allows the device to achieve full benefit of an optical back reflector or other transparent contact without any additional electrical losses.

We also investigated the contact between the p-layer and various glass/TCO substrates for superstrate p-i-n cells as part of our on-going study of ZnO/p contacts and ZnO substrates in collaboration with Professor Roy Gordon at Harvard University. It was found that a new process for APCVD ZnO yields much better device performance than previous APCVD ZnO material, and that straightforward changes to the deposition of the p-layer such as increasing the B dopant flow can give significant improvements in FF and V_{oc} of ZnO/p-i-n devices.

In an effort to improve the stabilized V_{oc}, we attempted to duplicate studies from Penn State, NREL and elsewhere by modifying the initially deposited i-layer to include either hydrogen dilution or graded a-SiC. This resulted in only a small (~10 mV) improvement in initial V_{oc} and no improvement in degraded V_{oc} or efficiency. We conclude that without hydrogen dilution of the bulk i-layer we will not see gains reported by others with hydrogen diluted interface layers since the bulk degradation dominates.

3.2 PECVD system operational improvements

In order to be able to perform work required by the new Statement of Work, several modifications/upgrades have been made on the PECVD reactor. In addition, long neglected major maintenance has also been addressed. The major upgrade involved computer control of the deposition process. Ten mass flow controllers, the down-stream pressure control unit and the RF power were connected to a Macintosh computer via two analog and one digital Lab View interface boards. The software program controlling the deposition process has two parts. In the first part, any of the twelve process parameters can be set to desired values prior to actual deposition. During the deposition any of these twelve parameters can be set to have linear time dependence over ten time segments. As a result, a large number of time profiles can be approximated for all the parameters.

Four new mass flow controllers were installed enabling the addition of two new gases, TriMethylBoron (TMB) and CO_2, allowing the two other gases to be computer controlled.

In addition, a new load-lock mechanism has been designed. The earlier system consisted of two magnetically coupled feed-throughs, one for pushing substrates from load-lock No. 1 into the deposition chamber and the other one pulling them out to load-lock No. 2. This system did not allow the samples to be removed from the deposition chamber and reintroduced later. Such a flexibility is necessary in order to perform reactor conditioning to reduce cross-contamination and to increase system throughput. To that effect, two new magnetically coupled feedthroughs were purchased and a new feedthrough-to-chamber coupling mechanism was designed and constructed by a vacuum component manufacturer. The new, internally designed coupling mechanism not only allows the feedthrough to have a linear motion, but also makes it possible for the tip latching to the substrate to have an up-down motion necessary for gripping and releasing the substrate holder. Besides these system upgrades, the reactor and gas lines were leak-checked for vacuum integrity. The turbo molecular pump and the reactive gas flow pump have also been reconditioned and cleaned.

3.3 Device deposition conditions

The PECVD system and its operation were discussed in detail in last year's Annual Report [123]. A 15 minute a-SiC burying layer is deposited between each device run to seal in dopants and prevent cross-contamination. Deposition parameters for standard devices have changed slightly due to the continuous p-to-buffer transition. For example, the p-layer has been lengthened from 15 to 20 seconds. Previously, the plasma was turned off while the buffer conditions were established. Table 3.1 lists deposition parameters of our standard p-i-n cells, leading to baseline efficiencies of 9.0-9.5%.

Table 3.1 Deposition conditions of standard devices

Layer	p	graded-buffer	i	µc n
Time (min:sec)	0:20	0:25	30:00	6:00
Pressure (T)	0.2	0.2	0.2	1.0
Temperature (˚C)	150	150	175	175
RF Power (W)	20	20	7	50
SiH_4 (sccm)	20	30	20	2
H_2 (sccm)				200
CH_4 (sccm)	30	20 -> 7.5		
2% B_2H_6 in H_2 (sccm)	1.5			
‘				
2% PH_3 in H_2 (sccm)				2

All devices were deposited on Asahi Type U textured SnO_2 unless other substrates were specifically being investigated. All devices received back reflector contacts consisting of a sputtered 80 nm ZnO(Al) layer sputtered in Ar at 900 W at 3 mT followed by 500 nm evaporated Ag. The ZnO/Ag contacts were sputtered through a mask giving areas of 0.4 cm^2.

3.4 Devices with continuous plasma "soft start" p-layer

A critical requirement for device studies, especially those investigating intentional p-layer variations or TCO/p contacts, is a repeatable p-layer. This can be difficult due to variability in the plasma ignition and transients in pressure and plasma density. While only lasting a few seconds, these initial variations can be significant since the p-layer deposition is only ~20 seconds long. We investigated a "soft start" process in order to improve the deposition of reliable and reproducible p-layers. A plasma is first established for ~10 seconds with Ar at the same total flow and pressure as used for the p-layer deposition. Then the p-layer process gases are turned on and the Ar is turned off. Since the actual deposition time of the boron doped a-SiC layer may be slightly different when pre-establishing the plasma, a series of devices were deposited with increasing p-layer times from 18 to 27 seconds. Our previous standard p-layer was 20 sec long. Table 3.2 shows results from this series including two devices without soft-start, one deposited at the beginning (4719) and one at the end (4743) of the soft-start series.

The V_{oc} and J_{sc} of the devices with soft start are comparable to non-soft start runs (4719, 4743) but the FF is lower. Analysis of the dark JV data shows that the series resistance, obtained from the intercept of dV/dJ vs 1/J in the dark, is R_s = 1.6-2.0 Ω-cm^2 . This is typical of runs without the soft start, suggesting the poor FF is due to i-layer collection, not contact resistance problems. This was confirmed with bias dependent QE measurements which showed large voltage dependence at long wavelengths. We define a parameter X_c =[QE(0V)/QE(+0.5V)@700 nm]/ [QE(0V)/QE(+0.5V)@450 nm] as the ratio of the voltage bias dependence for red light to that of blue light. Figure 3.1 shows the voltage bias ratio QE(0V)/QE(+0.5V) vs wavelength for devices with and without soft start p-layers, from runs 4727 and 4743, respectively. The device with the soft start p-layer has greater voltage dependent collection losses at forward bias for red light. A value of X_c of 1.15-1.20 at 700 nm was found for the devices having the new soft start. In comparison, X_c is typically between 1.00-1.05 for previous devices like 4719 or 4743, as shown in Figure 3.1. Values of X_c greater than unity indicate poor collection of holes from the i-layer, such as from P or O contamination while X_c less than unity indicates poor collection of electrons, such as from B contamination or p-i interface problems. Therefore, it is concluded that low FF in the soft start series (runs 4727 to 4735 above) is not due to a poor SnO_2/p contact but poor hole collection in the i-layer, typically caused by P or O contamination. This is consistent with previous experience in our single chamber system where changing the plasma conditions of one layer has resulted in low FF of subsequently deposited devices due to apparent i-layer contamination. Based on these results, we decided not to use soft start conditions for subsequent device runs.

Table 3.2 Results from series with new "soft start" for different p-layer deposition times. All devices had ZnO/Ag contacts. R_{oc} is slope at V_{oc}, R_s is intercept of dV/dJ vs 1/J from dark diode (series or contact resistance). 4719-22 and 4743-22 were deposited without a soft start p-layer before and after the soft start series.

run/piece	p-layer (sec)	V_{oc} (V)	J_{sc} (mA/cm^2)	FF (%)	Eff. (%)	R_{oc} (Ω-cm^2)	R_s (Ω-cm^2)
4719-12	20	0.861	15.2	70.7	9.2	5.2	1.6
4731-22	18	0.828	15.6	62.4	8.1	6.3	1.6
4727-22	20	0.800	15.7	60.7	7.6	6.5	1.8
4729-22	22	0.860	15.1	64.0	8.3	6.8	1.7
4733-22	25	0.871	15.1	63.9	8.4	7.0	1.8
4735-22	27	0.868	15.4	64.6	8.6	6.7	2.0
4743-22	20	0.843	14.9	70.6	8.8	5.1	n/a

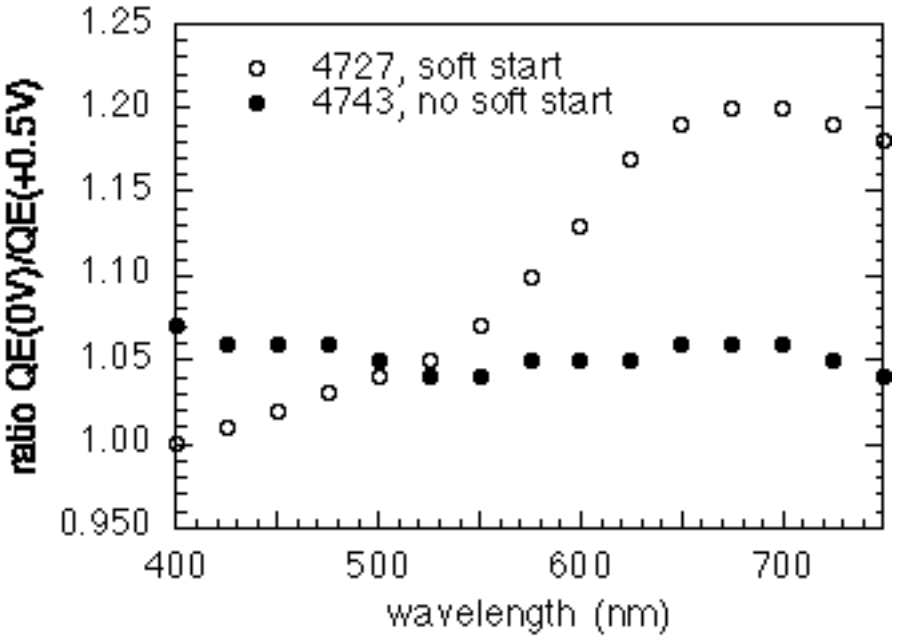


Figure 3.1 Voltage dependent QE ratio for devices with and without soft start p-layers. X_c is ratio of QE/(0v)/(+0.5V) at 700 nm to that at 450 nm. Run numbers refer to Table 3.2.

3.5 Effect of interface layers on V_{oc} and stability

The stability of devices with different initial i-layer conditions was studied. It has been reported by Penn State [124] and NREL [125] that p-i-n devices with H_2 diluted or C graded profiles in the i-layer near the p-layer (but distinct from the C graded buffer layer) have improved V_{oc} and stability

of p-i-n cells. Devices with structure of SnO_2/p-b-i_1-i_2-n/ZnO/Ag were deposited having 10-20 nm H_2 diluted or C graded i_1 regions. The 0.5 µm i_2 layers were deposited under standard conditions of pure SiH_4 at 175°C. Note that there was no H_2 dilution of the i_2 layers.

Table 3.3 shows that all of the devices studied, including the control cell without any i_1 layer, were in the initial efficiency range of 9.3-9.6%. Devices with a-SiC i_1 layers have 10-20 mV higher V_{oc}. After light soaking, all devices were between 5.2 and 5.5% efficiency. All parameters (V_{oc}, J_{sc}, FF) degraded similarly independent of i_1. The degraded V_{oc} values were within 10 mV of each other. A large amount of degradation was expected since the bulk of i-layer (i_2) is deposited under conditions known to have poor stability, namely low temperature with pure SiH_4 (no H_2 dilution). This is consistent with the lack of stabilization of the degradation even after 200 hours light exposure seen in Figure 3.2. We conclude that the degradation of the i_2 layer dominated the device stability and obscured any differences which might be due to different i_1 layers. H_2 diluted i-layers will be required for any further studies.

Table 3.3 Initial and light soaked performance of four p-b-i_1-i_2-n devices with different i_1 layers. All i_2 layers were 0.5 µm deposited without H_2 dilution. Light soaking for 200 hours at 25˚C under ELH lights @ 100 mW/cm^2. Light soaked values in ( ).

sample #	transition layer i_1	state	V_{oc} (Volts)	J_{sc} (mA/cm^2)	FF (%)	eff. (%)
4659-11	none	initial	0.857	15.8	69.7	9.5
		(200 hrs)	(0.813)	(13.2)	(48.6)	(5.2)
4670-21	ungraded a-SiC, 20 nm	initial	0.878	15.3	71.7	9.6
		(200 hrs)	(0.824)	(13.8)	(48.0)	(5.5)
4672-21	graded a-SiC, 10 nm	initial	0.865	15.4	72.3	9.6
		(200 hrs)	(0.815)	(13.3)	(50.8)	(5.5)
4696-22	H_2-diluted a-Si, 10 nm	initial	0.861	15.4	69.9	9.3
		(200 hrs)	(0.811)	(13.4)	(48.8)	(5.3)

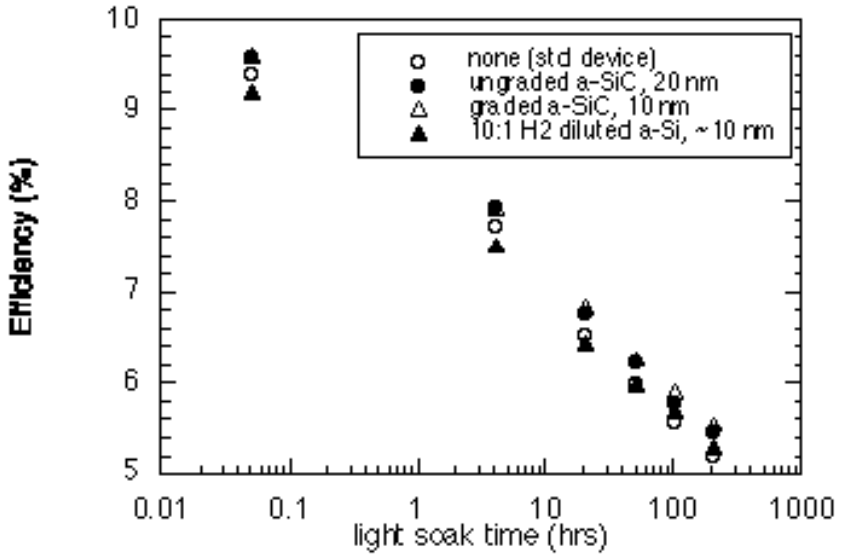


Figure 3.2 Stability of four devices with different i_1 layers during 200 hour light exposure. Note that there was no difference in degradation and that no stabilization occurs within 200 hours. The i_2 layer was not hydrogen diluted.

3.6 Effect of p-layer doping and alternate TCO substrates: ZnO and SnO_2/ZnO

Devices were deposited on various TCO substrates as part of an on-going study of the TCO/p contact. While the benefits of ZnO are well known, such as higher transmission and plasma-damage resistance [126, 127], difficulties in obtaining a low resistance and Ohmic ZnO/p contact are commonly reported [128, 129]. This is an area of focus for the NREL Multijunction Device Team.

A standard device was deposited on four different TCO substrates to study the influence of the bulk vs the surface of the TCO material. Three of the pieces were specially prepared substrates and one was standard Asahi SnO_2 as a control. One piece was APCVD ZnO from Prof. Gordon at Harvard. Another piece was Asahi SnO_2 coated with 100 nm of sputtered ZnO, while the third piece was 500 nm of sputtered ZnO, both prepared at IEC. Thus the three specially prepared substrates presented a ZnO surface for the p-layer contact. Results are shown in Table 3.4.

Table 3.4 Results for four devices deposited in run 4741 on different TCO substrates.

piece	TCO substrate	V_{oc} (V)	J_{sc} (mA/cm^2)	FF (%)	Eff. (%)	R_{oc} (Ω-cm^2)
-11	Asahi SnO_2	0.854	15.3	69.8	9.1	5.7
-12	Asahi SnO_2/ 100 nm sp ZnO	0.842	15.3	66.7	8.6	7.7
-21	500 nm sp ZnO	0.839	11.0	53.4	4.9	21.6
-22	APCVD ZnO	0.851	13.4	63.0	7.2	11.6

The control piece (-11) is typical. The -21 piece had no texture and -22 piece had very little texture (haze < 1%) which accounts for their lower J_{sc}. It is very surprising that the 100 nm of ZnO on top of SnO_2 gave a much better FF and R_{oc} compared to the single 500 nm ZnO layer. This suggests that either incomplete coverage of the SnO_2 allowed some SnO_2/p contact formation or that the contact is influenced by TCO properties deeper than 100 nm from the contact. Thus, textured SnO_2 coated with a thin sputtered ZnO layer may be a suitable substrate for p-layer studies with high H_2 dilution and high power since the ZnO may protect the underlying SnO_2 from damage while still giving a reasonable electrical contact.

The above results were obtained with our standard p-layer whose deposition was optimized for textured SnO_2 substrates. It is expected that the optimum p-layer for ZnO substrates will be different. The simplest improvement would be to increase the hole concentration. Three devices were deposited with the B_2H_6 flow in the p-layer of 1.5 (standard), 3.0 and 4.5 sccm to determine if increasing the p-layer conductivity could improve the ZnO/p contact. Substrates included ZnO from Harvard, and Asahi SnO_2. Figure 3.3 shows that the V_{oc} and FF of the ZnO were both significantly improved by doubling the B_2H_6 flow while the results on Asahi SnO_2 were relatively independent of B_2H_6 flow.

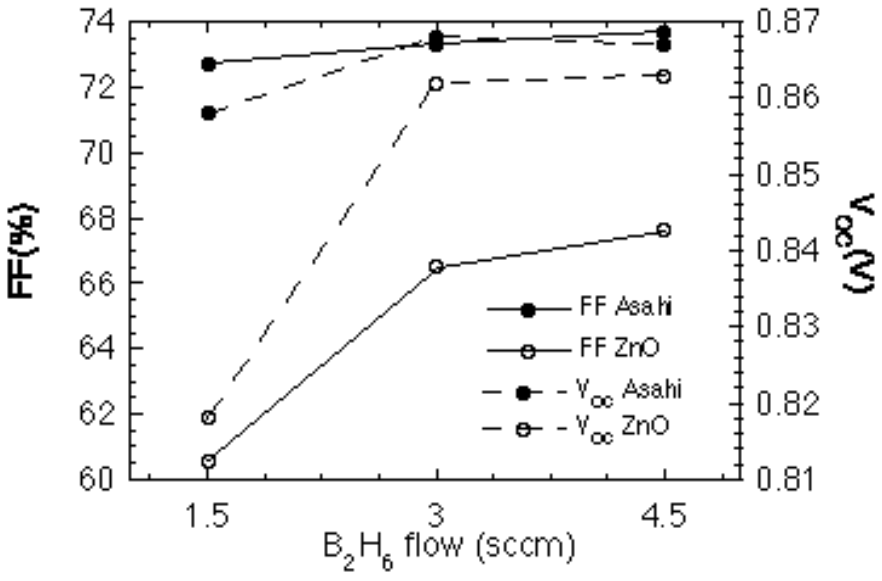


Figure 3.3 FF and V_{oc} for devices on SnO_2 (textured, Asahi) and ZnO (smooth, Harvard) for different B_2H_6 flows in the a-SiC p-layer.

3.7 Electrical and optical study of high performance TCO/metal back reflector

Results from last year indicated that it was necessary to optimize both the electrical and optical properties of the back reflector in order to obtain full benefit of the enhanced reflection. This lead to a study comparing the n-layer conductivity, sputtered TCO conditions, and effect of the reflective metal. Temperature dependent JV measurements indicated that the n/TCO contact was blocking electrons with an a-Si n-layer but not with a µc-Si n-layer. The n/TCO interface has a controlling influence on the electrical quality of the contact. ZnO was found to be better electrically and optically compared to ITO. These results are described in greater detail in Appendix 3.

3.8 Electrical characterization of sputtered TCO junctions on a-Si and µc-Si n and i-layers

Since the device results described above in Section 3.6 and in Appendix 3 indicated significant differences between a-Si and µc-Si layers and between ITO and ZnO, special test structures were fabricated to study these contacts and junctions in more detail. Four sets of depositions were made. Substrates were Asahi SnO_2 in all positions. Table 3.5 lists the layer thicknesses and Figure 3.4 shows the different device structures. From each run, one piece was contacted with a different sputtered TCO. Thus a total of four different sputtered TCO conditions were applied to pieces from a given run, leading to 16 different test devices. The four RF sputtered TCO layers used to contact pieces from each run are listed in Table 3.6. Three pieces were contacted with ZnO, sputtered with different atmospheres, and one with ITO. All sputtering was at 3 mT. Properties of the n-layers and sputtered layers are given in Appendix 3. Devices were measured from 100°C to -60°C in the dark (4685, 4686) and in light and dark (4687, 4688). Illumination was provided by ELH lamps adjusted to match the J_{sc} value obtained at 25°C under AM1.5 simulated light.

Table 3.5 Structure and thicknesses of a-Si and µc-Si layers in test structures used for sputtered TCO contact study.

a-Si run #	structure	a-Si n (nm)	µc-Si n (nm)	a-Si i (nm)
4685	glass/SnO_2/µc-Si n		200	
4686	glass/SnO_2/a-Si n	200		
4687	glass/SnO_2/µc-Si n/a-Si i		20	500
4688	glass/SnO_2/a-Si n/a-Si i	20		500

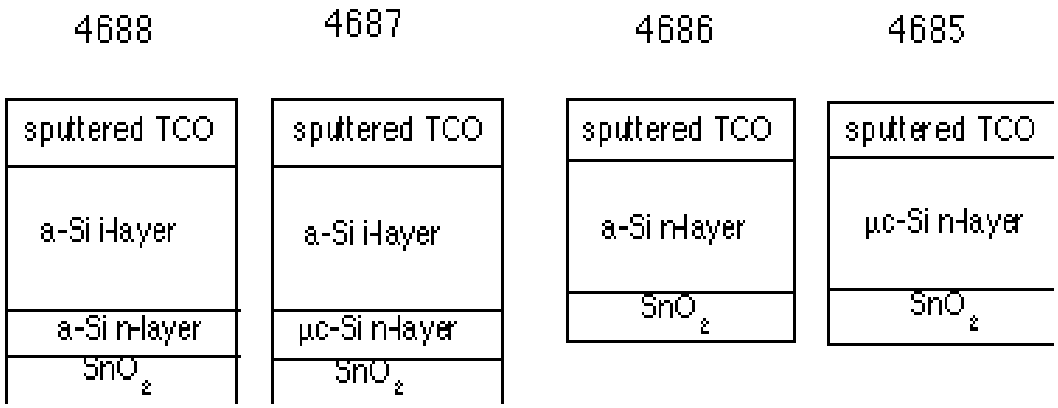


Figure 3.4 Four device structures (depositions 4685-4688) used to study sputtered TCO and SnO_2 contacts with a-Si and µc-Si i-layers and n-layers.

Table 3.6 Sputtered TCO layers used to contact each piece from runs 4685-4688. Balance of gas flow is Ar.

piece #	sputtered TCO	conditions (gas, RF)
-11	ZnO(Al)	Ar, 900 W
-12	ITO	0.9% O_2, 700W
-21	ZnO(Al)	1% H_2, 900W
-22	ZnO(Al)	0.2% O_2, 900W

Figure 3.5 and Figure 3.6 show the illuminated JV curves at 100, 25, and -60°C for glass/SnO_2/n-i/TCO devices with a-Si n-layer (4688-11) and µc-Si n-layer (4687-11). Both have ZnO top contacts sputtered in Ar. Note that the device with the a-Si n-layer has strong curvature beyond V_{oc} at and below 25°C, indicating a blocking contact between the a-Si n layer and the SnO_2. This significantly distorts the JV curve and lowers the FF even at 25°C. All devices from 4688 showed

this behavior while none of the devices from 4687 did, verifying that the blocking contact is between the SnO_2 and the n-layer, not the sputtered TCO and the i-layer. Therefore, no devices from 4688 were studied as a function of temperature. The blocking behavior of the a-Si n/SnO_2 interface provides key information for understanding results from 4686 pieces which also had a-Si n-layers deposited on SnO_2 as will be discussed below.

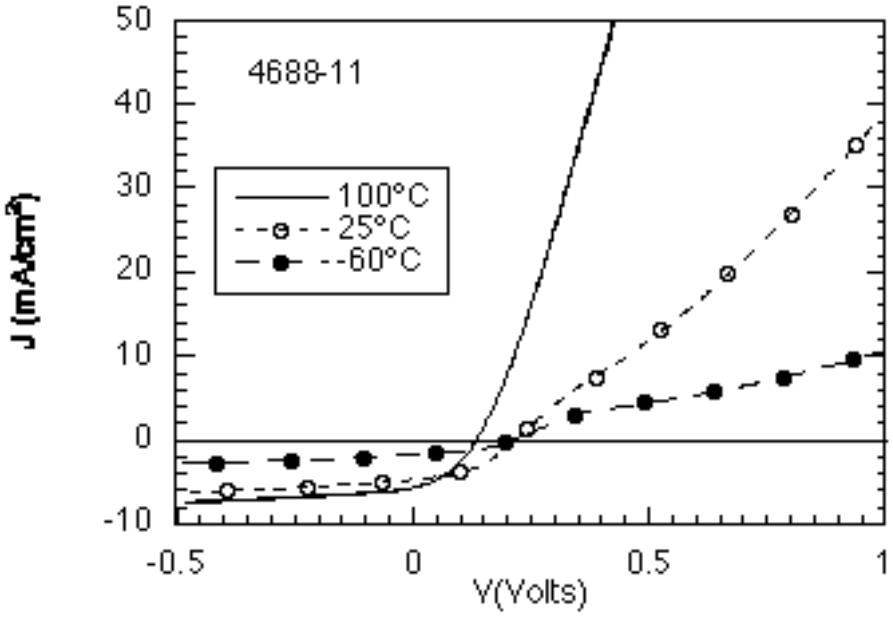


Figure 3.5 Illuminated JV curves at 100, 25, and -60˚C for glass/SnO_2/n-i/TCO devices with a-Si n-layer (4688-11).

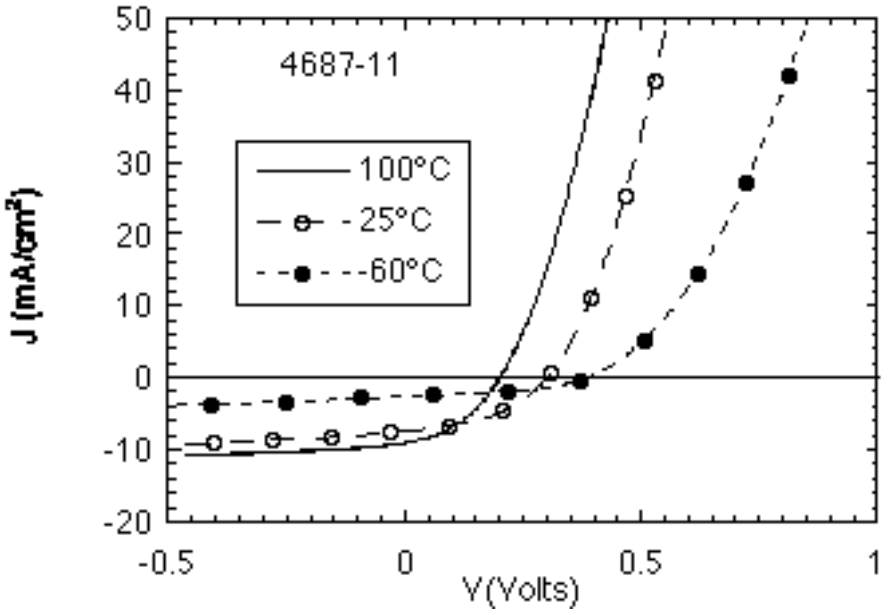


Figure 3.6 Illuminated JV curves at 100, 25, and -60˚C for glass/SnO_2/n-i/TCO devices with µc-Si n-layer (4687-11).

Figure 3.7 shows the JV curves in the light from all four sputtered TCO contacts on the 4687 pieces (glass/SnO_2/µc-Si n/a-Si i/sputtered TCO). Values of V_{oc}, J_{sc}, FF and R_{oc} are listed in Table 3.7. The two devices with TCO sputtered in Ar/O_2, either ITO or ZnO, have larger V_{oc} than the two devices with ZnO sputtered in Ar or Ar/H_2. It is surprising that FF as high as 57% were obtained without a p-layer. This indicates that the sputtered TCO provides a significant built-in voltage, hence electric field, in the i-layer. None of these devices show evidence of blocking contacts indicating the µc-Si n-layers provide Ohmic contact to the SnO_2 substrate.

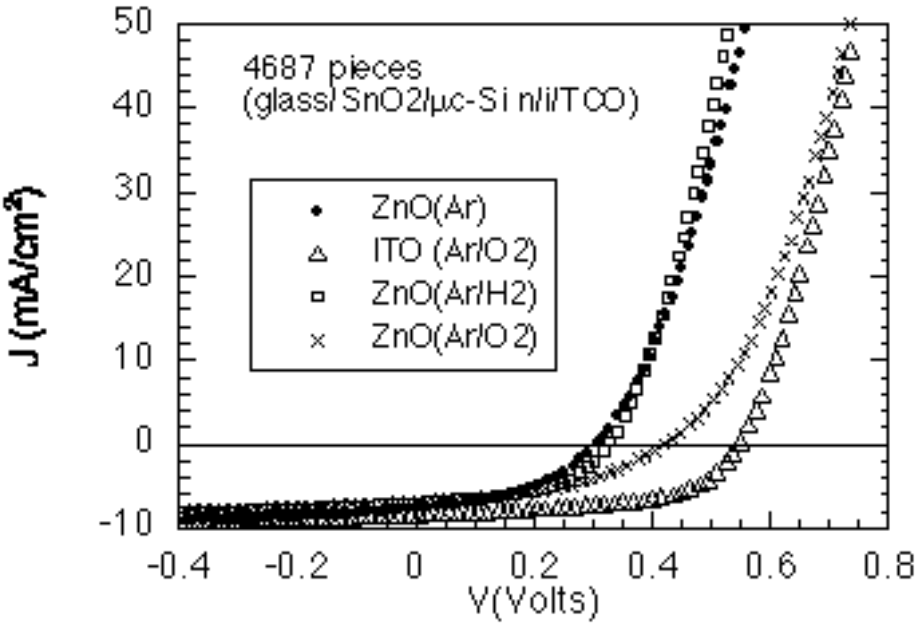


Figure 3.7 Illuminated JV curves at 25˚C for glass/SnO_2/n-i/TCO devices with µc-Si n-layers and four different sputtered TCO contacts.

Table 3.7 Illuminated JV parameters of glass/SnO_2/µc-Si n/a-Si/ i/sputtered TCO devices from 4687 under ELH light. V_{oc}, J_{sc}, FF and R_{oc} from measurement at 25˚C as shown in Figure 3.7, while V_{oc}/A, E_a, and J_{oo} from temperature dependence of Figure 3.8 and Figure 3.9.

piece #	sputtered TCO	Figure 3.8 V_{oc} (Volts)	J_{sc} (mA/cm^2)	FF (%)	R_{oc} (Ohm-cm^2)	V_{oc}/2 @ 0 K (Volts)	E_a (eV)	J_{oo} (mA/cm^2)
4687-11	ZnO(Ar)	0.29	7.5	46.4	11.0	0.38	0.24	6.1E2
4687-12	ITO (Ar/O_2)	0.53	8.1	57.4	8.8	0.50	0.47	3.6E3
4687-21	ZnO(Ar/H_2))	0.32	7.1	51.4	9.8	0.39	0.24	6.3E2
4687-22	ZnO(Ar/O_2)	0.42	6.9	45.0	21	0.45	0.37	1.0E4

Figure 3.8 shows the V_{oc} vs T from the same four devices from Figure 3.7. The intercept at T = 0 K is ($A*V_b$) where A is the diode A factor and V_b is the barrier. The A factors ranged from 1.5 to

2.5 over this temperature range for most of the devices. Assuming an average value of A = 2.0, the barriers between TCO and a-Si range from 0.5 eV for ITO sputtered in Ar/O_2 to 0.38 eV for ZnO sputtered in Ar. The two devices sputtered in Ar/O_2 mixtures have higher barriers than the two sputtered in Ar or Ar/H_2. ITO has the largest barrier with a-Si. The light JV data was analyzed at each temperature using the equation

$$J(V) = J_o \exp(-qV'/AkT) - J_{sc} + GV \quad (3.1)$$

with

$$V' = V - J*R_s \quad (3.2)$$

and

$$J_o = J_{oo} \exp(-E_a/kT) \quad (3.3)$$

where G is the shunt conductance, J_o is the diode recombination current, R_s is the series resistance and A is the diode factor. G is obtained from dJ/dV at reverse bias and R_s is obtained from the intercept of dV/dJ vs $1/(J + J_{sc})$. Figure 3.9 shows the temperature dependence of J_o. The activation energy E_a is obtained from the slope and J_{oo} from the intercept and is given in Table 3.7 along with other properties of the devices obtained from analysis of illuminated JV data as a function of temperature.

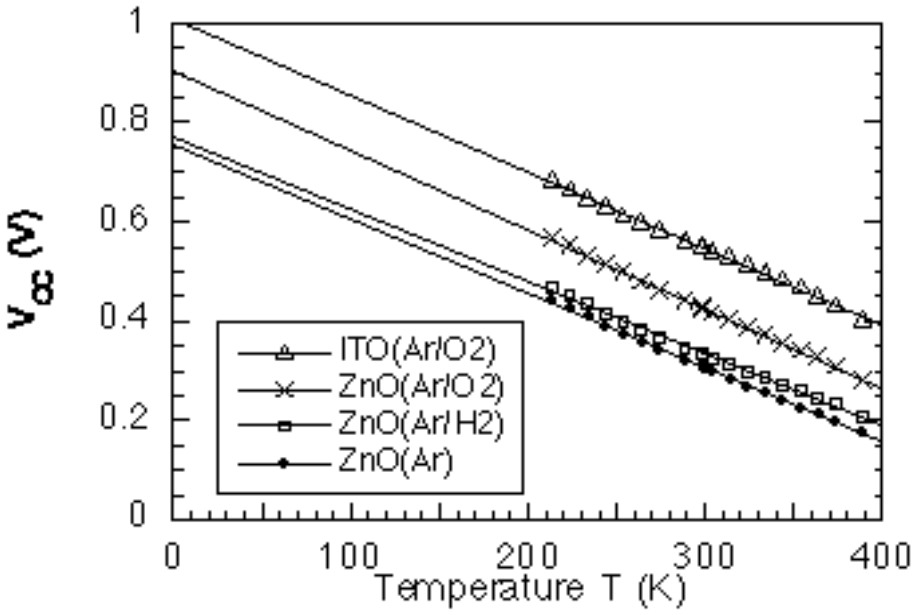


Figure 3.8 Temperature dependence of V_{oc} for four devices from Figure 3.7 with µc-Si n-layer.

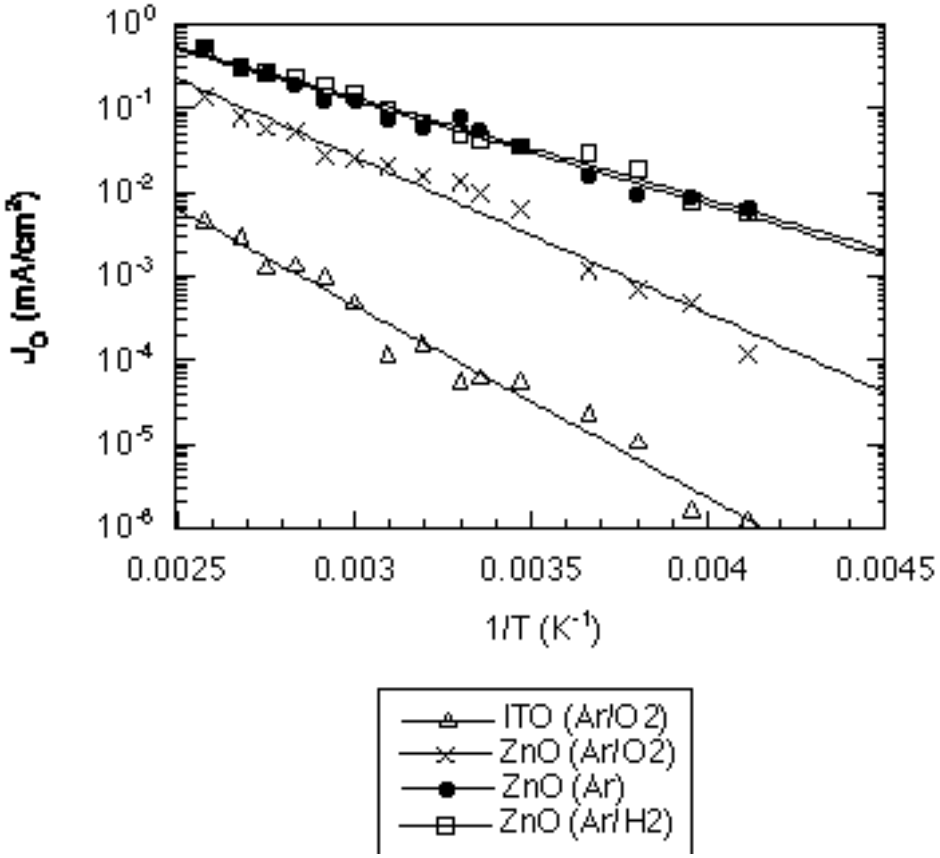


Figure 3.9 Temperature dependence of J_o for four devices from Figure 3.8 with µc-Si n-layer.

The temperature dependence of the series resistance obtained by analyzing the light JV data is shown in Figure 3.10 for the same four devices as shown in Figure 3.7 – Figure 3.9. At T greater than 15°C, the resistance is constant and equal to 1.3 Ohm-cm^2 for devices with TCO sputtered in Ar or Ar/H_2 and about 1.8 Ohm-cm^2 with TCO sputtered in Ar/O_2. Below this temperature the resistance is thermally activated with E_a ~ 0.08 eV for all four devices. Values of R_s = 1-2 Ohm-cm^2 are commonly found for standard p-i-n solar cells at 25°C.

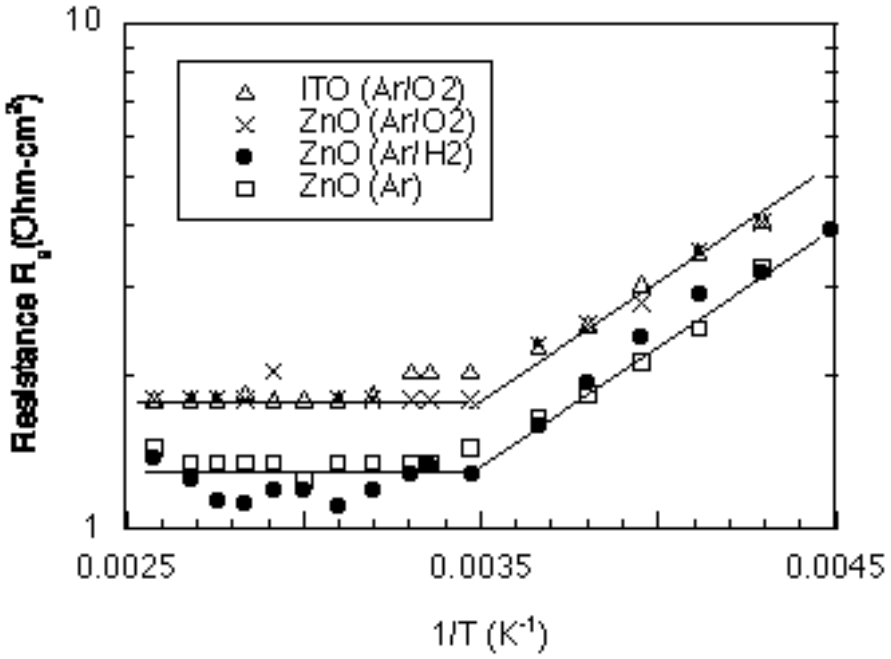


Figure 3.10 Temperature dependence of series resistance R_s from light JV of devices from 4687 (glass/SnO_2/µc-Si n/i/TCO). Lines are drawn to guide the eye. Activation energy for 1/T > 0.0036 K^{-1} is approximately 0.08 eV.

Further information about TCO contacts was obtained from analysis of the 4685 and 4686 devices consisting of single n-layer between two TCO contacts (see Figure 3.4). This work was originally motivated by our high efficiency solar cell results showing strong dependence of FF on the n/TCO back contact as discussed in Appendix 3. Since ITO, ZnO and SnO_2 are all supposedly degenerate n-type (n^+) TCO materials, Ohmic contacts and linear JV behavior was expected for these n^+ -n- n^+ device structures. Information about contacts and junctions between TCO and n-layers is useful for p-i-n and n-i-p solar cells and also flat panel displays. Both the a-Si and µc-Si n-layers were around 0.2 µm thick. Properties of the a-Si and µc-Si n-layers are given in Appendix 3. Note that forward bias refers to more positive bias on the ZnO or ITO sputtered contact relative to the SnO_2 contact. The top TCO/n contact and bottom n/SnO_2 contact are in series but can be separately identified by changing the voltage bias on the device. The sputtered top TCO/n contact is therefore limiting the current at reverse bias because it is reverse biased, while the n/SnO_2 is limiting at forward bias because it is reverse biased.

Figure 3.11 and Figure 3.12 compare JV curves at three temperatures for µc-Si n (4685) and a-Si n (4686) layers with the ZnO top contact (-11 pieces). These figures show the full range of JV behavior encountered. Both types of device had Ohmic JV behavior at 100°C. The a-Si device has some weak blocking behavior even at 25˚C. At -60˚C, both devices have poor conduction in forward bias indicating the n/SnO_2 is blocking. But the µc-Si device is very conducting in reverse bias while the a-Si device is still very blocking.

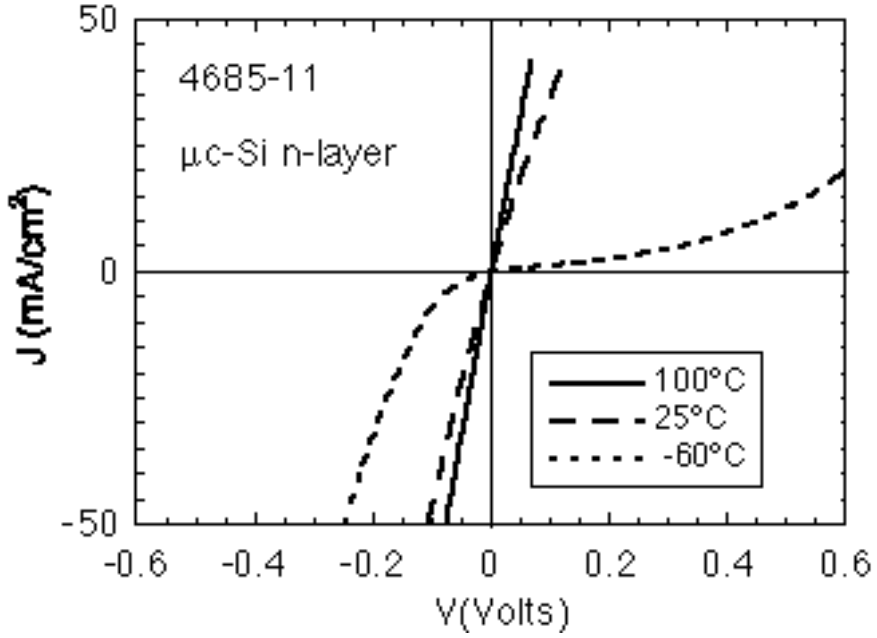


Figure 3.11 JV curves at 100, 25, and -60˚C for device with µc-Si n-layer (4685-11) and sputtered ZnO (Ar) contact. Device structure is glass/SnO_2/µc-Si n/ZnO.

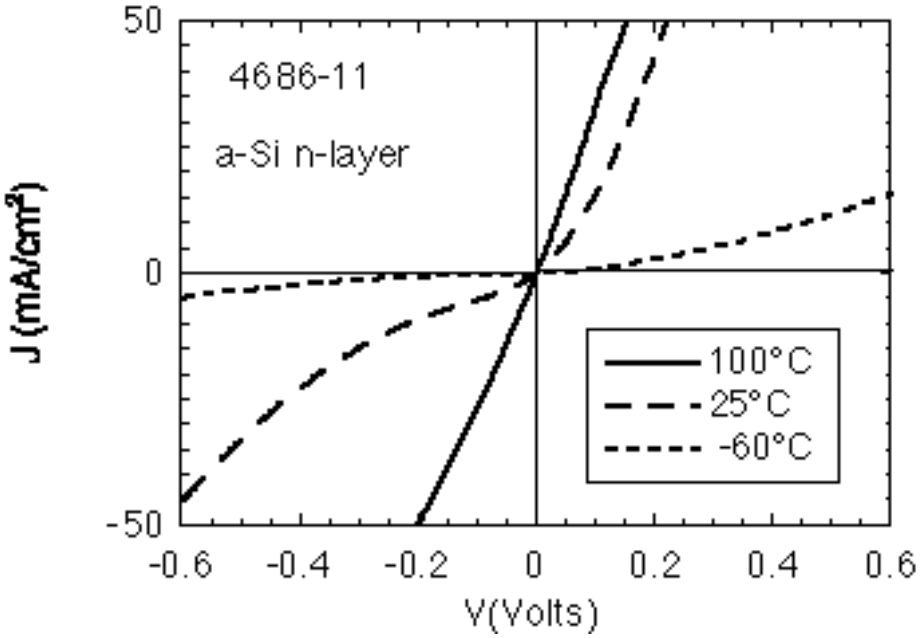


Figure 3.12 JV curves at 100, 25, and -60˚C for device with a-Si n-layer (4686-11) and sputtered ZnO (Ar) contact. Device structure is glass/SnO_2/a-Si n/ZnO.

In general, JV behavior on these n^+-n-n^+ structures was independent of the specific sputtered TCO contact for devices on µc-Si n-layers and only weakly dependent on sputtered TCO contact for devices with a-Si n-layers. However, results differ significantly between the µc-Si (4685) and a-Si (4686) n-layers as shown by Table 3.8 and Figure 3.13 and Figure 3.14. Table 3.8 shows the

slope at 0V for the eight n^+-n-n^+ devices. The resistances on the four µc-Si pieces are all similar, around 2 Ohm-cm^2, which is about a factor of 10 lower than for the four a-Si pieces. Note that bulk semiconductor resistance of either n-layer is less than 0.01 Ohm-cm^2. Thus the resistances in Table 3.8 must be dominated by contact and junction properties. Figure 3.13 and Figure 3.14 show the results at T = -60°C for all four sputtered TCO contacts on devices with µc-Si and a-Si n-layers, respectively. Blocking behavior is enhanced at low temperatures due to the lower probability of transport of thermally excited carriers over any barrier. Figure 3.13 also shows that the SnO_2/µc-Si n-layer contact is more blocking than the sputtered TCO/µc-Si contacts since these devices all have higher current flow when the SnO_2 contact is forward biased yet the sputtered TCO/µc-Si is reverse biased. Figure 3.14 shows that both SnO_2 and sputtered TCO contacts to the a-Si n-layer are blocking at low temperature since there is very little current flow in either polarity of bias. Also note that greater variation in the JV curves at forward bias is seen among the a-Si pieces (Figure 3.14) than among the µc-Si pieces (Figure 3.13), suggesting the higher conductivity of the µc-Si n-layer reduces sensitivity of the current transport to differences between the TCO bulk and interface properties. It effectively neutralizes any variability in the contact due to the TCO itself.

Table 3.8 Resistance dV/dJ at 0V in Ohm-cm^2 at 25˚C for glass/SnO_2/n-layer/TCO devices with µc-Si (4685) and a-Si (4686) n-layers.

sputtered TCO	µc-Si n-layer	a-Si n-layer
ITO (Ar/O_2)	2.6	18.1
ZnO (Ar)	2.5	10.4
ZnO (Ar/O_2)	2.5	20.8
ZnO (Ar/H_2)	1.9	16.7

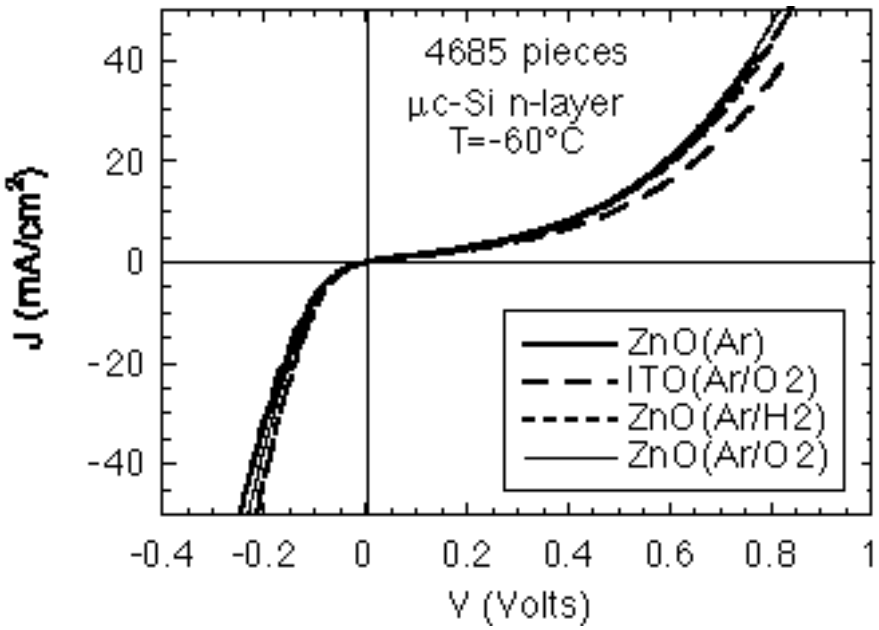


Figure 3.13 JV curves at -60˚C for devices with c-Si n-layer (4685 pieces) and sputtered TCO contacts.

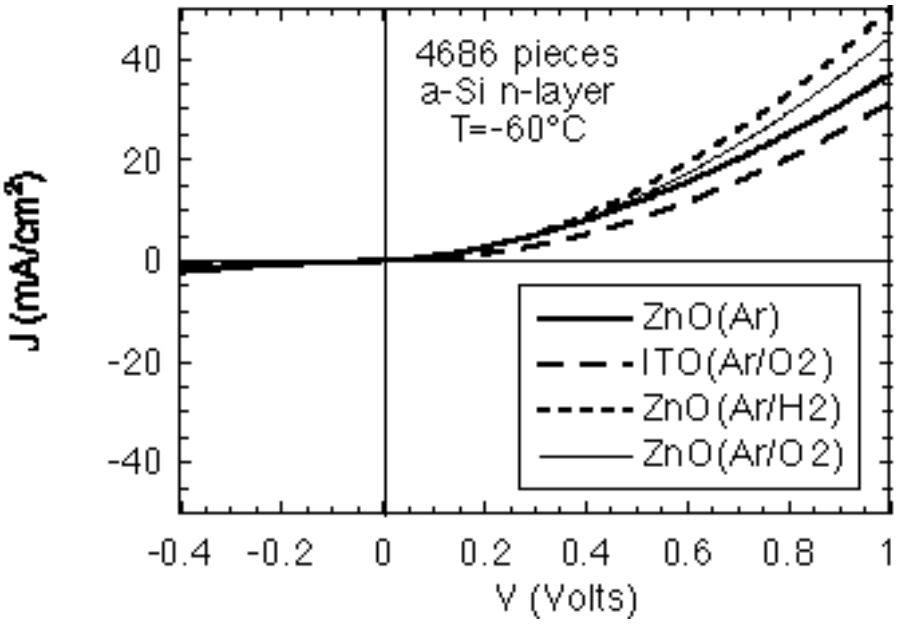


Figure 3.14 JV curves at -60˚C for devices with a-Si n-layer (4686 pieces) and sputtered TCO contacts.

To summarize, the µc-Si n-layers have more nearly-Ohmic behavior and lower resistance with sputtered ITO or ZnO contacts at T > 25˚C than do a-Si n-layers. JV behavior with various sputtered TCO contacts was essentially identical on µc-Si n-layers but has some dependence on the specific TCO for a-Si n-layers, especially at T < 0˚C. µc-Si n-layers are thus more tolerant by providing lower resistance, more uniform Ohmic contacts at T > 25°C with all of the TCO contacts investigated here. Regarding the bottom SnO_2 contact, measurements from the n-i devices (4687 and 4688, Figure 3.5 and Figure 3.6) as well as single n-layer devices (4685 and 4686, Figure

3.13 and Figure 3.14) indicate that the a-Si n/SnO_2 contact is more strongly blocking at 25° than the µc-Si n/SnO_2 contact. Thus µc-Si n-layers are essential for good Ohmic contacts to TCO for either top or bottom contacts. Their high conductivity allows the decoupling of the electrical requirements for the contact from the optical requirements, and allow the device to achieve full benefit of an optical back reflector or other transparent contact. More quantitative analysis of these contacts and their temperature dependence is in progress.

4. CdTe-based Solar Cells

4.1 Summary

Production of reliable and reproducible CdS window layers and contacts for stable, high performance CdS/CdTe solar cells are the key issues confronting development of thin-film CdTe solar cells. Meeting these objectives with manufacturing-compatible processes is crucial to satisfying the overall NREL program goals and requires an understanding of the controlling properties and mechanisms. IEC research in this phase was concentrated on: 1) quantifying and controlling CdS-CdTe interaction; 2) analyzing CdTe contact formation and properties; and 3) analyzing device behavior after stress-induced degradation. Through extensive interaction with the National CdTe R&D Team, the applicability of the results and processes to CdS/CdTe cells made by different techniques has been demonstrated, enabling a consistent framework to be used for understanding the relationship between device fabrication and operation.

4.1.1 Devices with Thin CdS

During phase I, IEC demonstrated improved understanding and control of CdS diffusion by employing evaporated $CdTe_{1-x}S_x$ absorber layers (see Appendix 4) and by modifying post-deposition treatments to anneal crystal defects prior to $CdCl_2$ delivery. Significant results include: 1) determining the effect of $CdTe_{1-x}S_x$ alloy composition on the effective CdS diffusion rate; 2) reducing CdS window layer consumption by 3X; 3) fabricating devices with $J_{sc} > 25$ mA/cm^2 with evaporated CdS layers; 4) determining device performance as a function of *final* CdS thickness; and 5) development of an all-vapor cell fabrication process.

4.1.2 Quantification of CdS-CdTe Interdiffusion

During phase I, fundamental issues confronting fabrication of devices with ultra-thin CdS were investigated, allowing the CdS consumption process to be understood and controlled. Through teaming activity, the role of TCO properties was further elucidated. In particular: 1) measurement protocols were developed to analyze pinholes in the CdS layer and CdS diffusion into the absorber layer; 2) low-temperature equilibrium data points were added to the CdS-CdTe phase diagram; 3) CdS diffusion into CdTe-based absorber layers with a range of sulfur content was quantified; 4) CdS diffusion in CdTe was examined for varying post-deposition treatment conditions; 5) the micro-crystal structure of the resulting absorber and absorber-window layer interface was examined by TEM for varying post-deposition treatment conditions; 6) a complete materials analysis with respect to interdiffusion in CdTe/CdS cells was made using CdTe/CdS furnished by six groups of the CdTe Team, leading to development of a phenomenological model of CdTe/CdS devices; and 7) TCO properties were identified which render the device structure more tolerant to complete CdS loss, leading to improvements in baseline efficiency of physical vapor deposited CdTe/CdS devices.

4.1.3 Contact to CdTe

A key chemical component of working CdTe contacts was clearly identified for the “wet chemical” fabrication processes typically employed and an alternative, all-vapor, method for fabricating low resistance contacts was developed. Measurement protocols using variations in light intensity and temperature during current-voltage measurements were employed to analyze the CdTe contact characteristics of devices made by different processes having different contacts. Coupled with the stress-induced degradation and

recontacting studies being carried jointly with the CdTe Stability Team, a model is being formulated which links operational and stability aspects of CdTe/CdS cells.

4.1.4 Team Participation

During phase I, IEC actively participated in the National CdTe R&D Team by fabricating contacts for the stability sub-team and devices for the CdS sub-team, analyzing films and devices for both sub-teams, reporting results through presentations and written reports, and hosting a full-day team meeting on April 30, 1997. In particular, devices were fabricated on different TCO to augment investigation of TCO/CdTe junction influence as d(CdS) is reduced. Contacts to CdTe were deposited and evaluated on CdTe/CdS samples from Solar Cells, Inc., using five different conductors, and from Golden Photon, Inc. A comprehensive x-ray diffraction analysis was performed on samples made by six groups within the team, and a full report was submitted at the April, 1997 team meeting.

4.2 Background

4.2.1 Framework Relating CdTe/CdS Fabrication Technologies

All polycrystalline CdTe-based thin-film devices are fabricated with the aid of post-formation treatments which transform weakly photoactive structures into efficient photoconverters. With emphasis on post-deposition processing, there is a wide latitude for CdS and CdTe deposition conditions that lead to >10% devices, but each "method" inherently possesses its own performance-limiting characteristics. Working through this space of processing conditions and establishing a unified framework for relating behavior is essential for allowing the existing body of data to be understood. Macroscopically, the fabrication technologies can be represented by a simple matrix with respect to film formation temperature and chloride chemistry (Table 4.1). The method of film formation and resultant properties determine the extent of change incurred during post-formation $CdCl_2$ treatment (Table 4.2).

Table 4.1 As-deposited methods and selected properties.

Deposition Temperature>>	**T < 300 C**	**T > 400 C**
Chloride Present During Film Formation	**Electrodeposition** 1. low mixing, 2. small grains	**Spray/Sinter** 1. high mixing, 2. large grains, porous
Chloride Absent During Film Formation	**Physical Vapor Deposition** 1. low mixing, 2. small columnar grains	**Close-Space Sublimation** 1. low mixing, 2. large grains

Table 4.2 Selected properties after treatment at ~400˚C.

Deposition Temperature>>	T < 300 C	T > 400 C
Chloride Present During Film Formation	**Electrodeposition** 1. Additional chloride not necessary, 2. Significant interdiffusion, 3. Grains coalesce	**Spray/Sinter** 1. Additional chloride not necessary, 2. No change, 3. No change
Chloride Absent During Film Formation	**Physical Vapor Deposition** 1. Chloride needed, 2. Interdiffusion controllable by thermal history, 3. Grains coalesce	**Close-Space Sublimation** 1. Chloride needed, 2. No change, 3. No change

It is apparent in Table 4.2 that macroscopic grain coalescence and interdiffusion do not occur after treatment of films that are deposited at T > 400˚C; in such films the function of $CdCl_2$ is simpler (i.e., limited to electronic modification) than in other films wherein significant structural changes accompany electronic modification. Comparison of high performance devices made by different methods should yield quantitative information about the performance and stability-limiting mechanisms in all CdTe-based cells and how they can be overcome. For example, grain size as a single parameter cannot be used as a predictor of high performance; rather, the grain boundary density during $CdCl_2$ treatment will affect the diffusion pathways for CdS consumption, and the CdS thickness uniformity resulting from the diffusion process will directly affect the device behavior.

At IEC, physical vapor deposition (PVD) is used to form the CdS and CdTe films. This deposition technique offers a low temperature approach for separating the effects of post-deposition processing on device performance [130, 131]. The PVD reactor permits single-phase CdTe films to be deposited at temperatures from ~150°C to ~400°C and two-phase films (CdTe + Te) to be deposited at temperatures below 150°C. This range of deposition conditions has permitted separation of deposition and post-deposition effects resulting in identification of critical relationships between post-deposition treatments, device structure and composition, and performance. Extrapolating information from these studies to devices made by wholly different deposition technologies has been made possible by interaction with other groups.

Recently, the NREL-sponsored National CdTe R&D Team effort has afforded access to devices prepared by five different technologies. Physical, chemical, optical and electronic characterization of these representative devices shows considerable variation in gross film properties, and yet performance in the 10 to 15% efficiency range is demonstrated. The primary difference in the performance among these devices is J_{sc}, which is controlled primarily by the CdS thickness. In the highest efficiency devices, the CdS is all-but eliminated during processing and J_{sc} is limited primarily by the optical properties of the superstrate/TCO combination, giving efficiencies from 14 to 16%. Achieving 20% conversion efficiencies will require increasing both V_{oc} and fill factor by manipulating the recombination mechanisms in the materials of the junction region.

A unified phenomenological model describing the geometrical, structural, and chemical situation of the devices can be established from known data. For recently fabricated samples, Table 4.3, Table 4.4, and Table 4.5 (presented at Team meetings in Crystal City, Lakewood, and Newark) summarize fabrication conditions and properties of CdS and CdTe films from seven facilities. Table 4.6 presents device results for representative samples of the different methods using the diffused-Cu plus etch contacting process at IEC, which gave comparable results to those obtained by the groups with their contacts. The highest conversion efficiencies have been demonstrated using CSS-deposited CdTe. A commonly observed trend found for low deposition temperature processes is reduced V_{oc} as CdS thickness is reduced [132, 133]; this was the impetus for generating a subsequent sample set and for assessing pinhole occurrence in CdS films.

Table 4.3 CdS deposition methods and film properties.

Group	CdS Depo Method	CdS Depo Temp (C)	Initial CdS Thk (nm)	CdS Treatment
USF	CBD	85	80	H_2
NREL	CBD	85	80	H_2
SCI	CSS	?	250	?
Gold Photon	Spray	?	1000	?
IEC	PVD	220	180	$CdCl_2$
U of Toledo	Sputter	?	160	?
CSM	CBD	85	180	?

Table 4.4 CdTe deposition methods and as-deposited film properties.

Group	CdTe Depo Method	CdTe Depo Temp (C)	CdTe Thk (um)	CdTe Grain Size (um)	CdTe Orient
USF	CSS	**600**	7	1.0	?
NREL	CSS	**600**	7	2.5	?
SCI	CSS	**550**	5	1.0	111
G Photon	Spray	**550**	10	5.0	220
IEC	PVD	**250**	5	0.2	111
U of Tol	Sputter	**200**	2	0.2	111
CSM	E-dep	**85**	2	0.2	111

Table 4.5 Film properties in finished device structures based on analysis performed by IEC for NREL CdTe - Thin CdS Team.

Group	Post Depo Treat?	Final CdS Thk (nm)	Final CdTe Grain Size (um)	CdTe Surface Morph	CdTe Cross Section @ Junction	Final CdTe Orient	Sulfur Dist
USF	Y	20	1.0	Dense, Faceted	Dense	Random	Graded, <1%
NREL	Y	20	2.5	Dense, Faceted	Dense	220	Graded, <1%
SCI	Y	200	1.0	Dense, Rounded	Dense	220	Graded, <1%
G Photon	Y	< 20	5.0	Porous, Faceted	Dense	220	Uniform,8%
IEC	Y	160	1.5	Dense, Rounded	Dense	Random	Graded, <1%
U of Tol	Y	160	0.3	Dense, Rounded	Dense	220	Graded, <1%
CSM	Y	160	1.0	Dense, Rounded	Dense	220	Graded, 1%

Table 4.6 Device results for representative samples of Table 4.3, Table 4.4 and Table 4.5, receiving contacts at IEC. NREL and Golden Photon results are based on published data.

Group	Sample #	V_{oc} (mV)	J_{sc} (mA/ cm^2)	QE @ (400 nm)	FF (%)	Eff (%)
USF	1075	843	24.3	0.6	70.6	14.5
NREL	Ref [134]	823	21.3	0.3	73.3	12.8
SCI	10304E2	808	16.8	0.05	67.8	9.2
G Photon	Ref [135]	793	24.2	0.9	63.7	12.2
IEC	40920.11	821	21.5	0.2	69.0	12.2
U of Tol	376.1	798	22.0	0.2	64.8	11.4
CSM	HT-1	765	19.2	0.1	65.7	9.7

Table 4.4 and Table 4.5 show that the $CdCl_2$ treatment recrystallizes films deposited at low temperatures, resulting in larger grains and reduced (111) orientation. The crystallographic properties of films deposited at high temperatures are not significantly altered by $CdCl_2$ treatment. In all cases, CdS thickness is reduced and is detectable by measuring the formation of $CdTe_{1-x}S_x$ and by comparing initial CdS optical data to short-wavelength QE data.

A striking contrast is noted between cells made by spray-deposition and the other high temperature processes, both in processing condition and cell result. In the spray-deposited cells, a very thick CdS layer is initially employed but is totally consumed as $CdTe_{1-x}S_x$ alloy

during CdTe processing, resulting in the high short-wavelength response. The J_{sc} has been maximized, but the resulting $CdTe_{1-x}S_x/SnO_2$ junction exhibits a slightly lower V_{oc} than other high temperature cells. On the other hand, CSS devices are fabricated by depositing CdTe directly onto ultra-thin CdS maintaining the thinnest possible layer, resulting in lower J_{sc} but retaining high V_{oc}. With most processing methods, when the CdS layer is kept thick, in the 0.2-0.5 µm range, high V_{oc} is obtained, but at the expense of J_{sc}.

For the low temperature CdTe deposition processes, controlling the interaction during the $CdCl_2$ processing is the key to optimization. This may be related to defects in as-deposited CdTe films which serve as diffusion paths for S, resulting in enhanced CdS consumption. Depending on type and density, residual defects may also limit V_{oc}. Recently, V_{oc} = 850 mV was achieved with low temperature PVD CdTe by incorporating a short, high temperature anneal prior to chloride processing [136]. TEM analysis of these films compared to unannealed but chloride treated films showed dramatically lower crystallographic defect density and uniformly thick CdS layer at the CdS-CdTe interface. Thus, V_{oc} and CdS consumption are related to defects which can be annealed out or minimized by high deposition temperature.

The existence of S in the CdTe absorber layer as $CdTe_{1-x}S_x$ raises questions about the electronic properties of $CdTe_{1-x}S_x$ alloys, the alloy compositional uniformity, and the alloy distribution in the junction region. Current research at IEC is focused on this aspect of the devices. It should be noted that, to a first order, spray-deposited films, containing up to x = 8% S after processing, show sufficiently comparable device behavior to cells with less S content to demonstrate equivalence in electronic properties. Further, PVD films deposited with S at the solubility limit for ~400°C processing temperatures have demonstrated similar device performance to those made with CdTe layers and offers a path for utilizing ultra-thin CdS window layers.

The CdTe/CdS device is represented as an n/p heterojunction in which the CdS layer serves as a buffer layer between the CdTe and the TCO, producing an inversion layer within the CdTe side of the device which minimizes the effect of interface recombination on the collected light-generated current [137]. Enhanced p-type doping at the grain boundaries reduces grain boundary recombination. Diode current in the devices is controlled by space-charge (Shockley-Reed-Hall) recombination in the $CdTe_{1-x}S_x$ absorber layer. Developing a *detailed* electronic model from this description requires an understanding of the effects of impurities such as oxygen, chlorine, and copper as well as the fundamental nature of the junction, the type, density, and role of defects, and the role of grain boundaries as both conduction paths and participants in the junction operation.

The problem can be represented in two physical dimensions as shown in Figure 4.1 and Figure 4.2 for evaporated films, and are based on TEM and XRD data previously reported [130, 131, 132, 136, 138]. In the as-deposited condition, there is heteroepitaxial coordination of the CdTe and CdS layers resulting in lattice strain at the interface. The relatively low deposition temperature results in a high density of incorporated non-grain boundary defects such as twin planes and dislocations. Treatment with $CdCl_2$ serves at least two functions: 1) provides thermo-chemical activation of atoms in each layer resulting in sufficient atomic mobility to anneal defects and coalesce grains, and 2) induces intermixing and solid-state diffusion resulting in thinning of the CdS layer and producing $CdTe_{1-x}S_x$ and $CdS_{1-y}Te_y$ in the junction region.

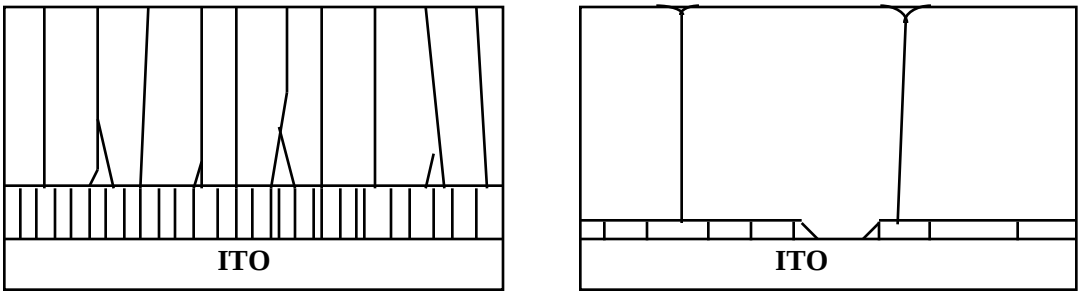


Figure 4.1 Schematic cross-sectional views of as-deposited (left) and $CdCl_2$-treated CdTe/CdS cells.

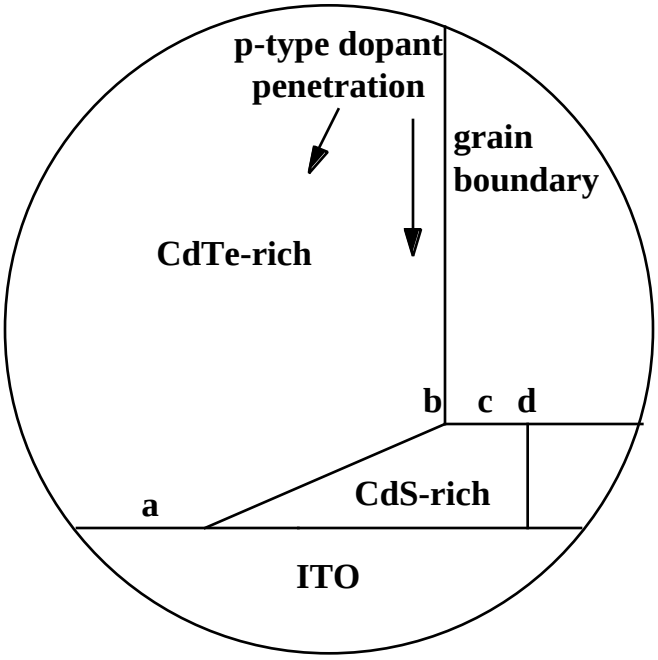


Figure 4.2 Schematic detail of the junction region in a CdTe/CdS device.

Figure 4.2 depicts an interface region in which there are parallel junctions between CdTe-rich and CdS-rich alloys and between CdTe-rich alloy and the TCO. In addition to these primary junctions, it is possible that the near-junction grain boundaries, both within CdS-rich and CdTe-rich alloys, can play an active role in controlling device behavior. For example, high grain boundary density coupled with penetrating chemical etchants could produce shunt paths through the CdTe layer. At this juncture, the microscopic distribution of chemical constituents, dopants, and defects within the schematic model of Figure 4.2 is not known, yet a phenomenological model relating processing conditions to "bulk" film properties and device output is within reach, based on the following conclusions from working devices:

· Interface region consists of $CdTe_{1-x}S_x/CdS_{1-y}Te_y$ [138, 139].

- CdS and $CdS_{1-y}Te_y$ result in parasitic optical losses at short wavelengths [138, 139] and act as a "dead" layer for current generation [140].

- Extent of Te alloy on CdS side depends critically on preparation and condition of CdS layer [139, 141].

- Distribution of S in absorber layer ranges from uniform to enrichment of grain surface [138, 142].

- Extent of S alloy on CdTe side depends critically on thermal/chemical history of CdTe layer [138, 143], chloride vapor concentration [144], and oxygen vapor concentration [144, 145].

- Effect of $CdCl_2$ treatment depends on the as-deposited "condition" of the CdTe film. From a crystallographic perspective, low temperature-deposited layers undergo significant reorganization while high temperature-deposited layers are minimally affected, a result of incorporated defects in films deposited at different base-pressures and temperatures. From an electronic perspective, the roles of the chemical constituents of the treatment ambient (oxygen and chlorine) must be further elucidated.

- Action of $CdCl_2$ at T below 568°C is via solid-vapor equilibrium with CdTe. Films containing excess Te second phase are converted to single phase films during treatment, i.e., $CdCl_2$ has a chemically compensating effect on CdTe stoichiometry based on thermodynamic equilibrium.

- Quantitatively similar materials and device results can be achieved by delivering chloride species as solid $CdCl_2$ or via vapor phase as $CdCl_2$, HCl, or Cl_2 [142, 144, 146, 147].

- To a first order, the properties of uniformly deposited Cd(TeS)/CdS and interdiffused CdTe/CdS junctions are similar, as demonstrated by devices made with *in situ* Cd(TeS) absorber layers [148].

- $CdTe_{1-x}S_x$ and $CdS_{1-y}Te_y$ are thermodynamic endpoints for the CdS-CdTe system; any process must cope with formation and distribution of these alloys.

- $CdCl_2$, O_2, Cu, and Te have coupled roles in controlling "conductivity" of the Cd(TeS) layer and formation of contacts thereupon [145, 149, 150, 151].

- Optically-limited J_{sc} obtained because grain boundaries are passivated during the chloride treatment, resulting in enhanced p-conductivity at grain boundaries [137].

- Optimal device performance obtained when a high temperature step is used in the process; the recombination mechanisms controlling V_{oc} and fill factor are thus linked to defect density in absorber layer.

- Low resistance back-contacts are facilitated by enhanced p-conductivity at the back surface [152]. Variations in back-contact processing can produce as-yet unexplained variations in V_{oc} which may be due to penetration of contacting agents along grain boundaries [153].

4.2.2 Critical issues

For the framework to be relevant to the overall goal of developing a successful low-cost thin-film photovoltaic module, the research needs to maintain focus upon the *critical* issues. During Phase I of this contract, research efforts were directed at the critical issues defined below for performance, stability, and manufacturability.

For polycrystalline thin-film CdTe/CdS solar cells, the *performance*-limiting issues are related to the fundamental quantities that determine built-in voltage, recombination, carrier transport, and Ohmic contact. With the present device structure, the *critical* performance-limiting issue is control of the CdS layer. To maximize the current density output, the CdS must be as thin as possible without producing junctions between the CdTe and the TCO. This is because the junction between CdTe and the available TCO materials exhibits a larger diode current than the junctions with CdS. Developments in TCO technology may eventually allow elimination of the CdS layer entirely, which will shift the focus towards the electronic properties of the CdTe layer. Another option for increasing the current density is to utilize photocarriers generated within the CdS layer; for these carriers to be collected the field must cross the interface, making the device susceptible to interface recombination.

The critical *stability*-controlling issues, while not fully definable, will relate to the infinitesimal nature of the CdS layer and to the robustness of the dopants and contacts. Minimization of CdS thickness to maximize current density may affect the sensitivity of the cell to thermal or electrical bias stresses, making the long-term stability of cells with ultra-thin CdS a critical issue. In addition, various dopant materials and chemical species are introduced into the cell structure at various phases of processing; their interaction and modification under stress conditions and over long periods of time must be fully understood in the context of stability.

The critical issue of *manufacturability* of CdTe/CdS thin-film devices is defined by the balance between maximum performance achievable at minimum processing and materials cost. Fully understanding and solving the critical issues of *performance* and *stability* will naturally lead to innovative options for low-cost processing. As a guiding philosophy, near-atmospheric vapor processes were sought to replace liquid chemical processes.

4.3 CdS-CdTe Interaction

4.3.1 Approach and Techniques

4.3.1.1 Film Deposition

The goals of identifying, quantifying and controlling the interaction between CdS and CdTe layers in thin-film device structures were achieved by:

1. Utilizing a baseline fabrication process for CdTe/CdS cells;

2. Establishing a measurement protocol for quantifying CdS properties and content in window and absorber layers;
3. Measuring CdS content in absorber layer before and after post-deposition treatments;
4. Correlating photovoltaic output of devices with resultant CdS window layer thickness;
5. Using (2) and (3) above to evaluate cells made with $CdTe_{1-x}S_x$ alloy absorber layers and with modified post-deposition treatments.

The baseline process is defined below:

1. Physical vapor deposition of CdS film onto ~200 nm ITO (20Ω/sq)/Corning 7059 glass.
2. $CdCl_2$ treatment @ 420°C for 10-20 min [141].
3. Physical vapor deposition of ~5 μm thick CdTe film onto treated CdS at T ~ 250°C.
4. $CdCl_2$ vapor treatment @ 420°C for 15 min in air [154].
5. Etch to produce Te excess.
6. Deposit Cu film with *in situ* heat treatment @ 200°C for 30 min [152].
7. Etch excess Cu away with bromine-methanol.
8. Apply carbon ink conductor, dry for 4-6 hours.

This baseline fabrication process allows the effects of individual processing steps to be altered and evaluated independent of other steps; for example, the copper doping step is separated from the application of the current-carrying conductor. New to the process in this contract year is performing the copper diffusion step within the copper deposition reactor.

Nine 1" x 1" samples, including one with an embedded thermocouple, are coated in each physical vapor deposition. The arrangement utilized within the bell jar to deposit the alloy absorber layers is shown in Figure 4.3. Deposition is obtained by dissociative evaporation of the CdTe and CdS powders within the effusion sources and free molecular flow from source to substrate in the vacuum at a base pressure of $\sim 10^{-6}$ Torr :

$$CdTe_s \text{ ---> } Cd_v + 1/2(Te_2)_v \qquad (4.1)$$

$$CdS_s \text{ ---> } Cd_v + 1/2(S_2)_v. \qquad (4.2)$$

The effusion rate (r_o) from the sources is a function of the pressure drop across the effusion orifice (P_1-P_2) and the effective gas phase molecular weight (M_{eff}):

$$r_o \sim (M_{eff}/RT)^{0.5}(P_1-P_2), \qquad (4.3)$$

where P_1 = gas pressure at orifice.

The incident flux (r_i) at the substrate, y units away, is a function of the angle (θ) from the center line:

$$r_i \sim (r_o \cos^{3/2}\theta)/y^2 \qquad (4.4)$$

At the substrate, the deposition rate depends on the component sticking coefficients and reaction rates. The composition of the deposit depends on the ratio of the effusion fluxes

and relative sticking coefficients (δ_{Cd}, δ_{Te}, δ_S). For typical deposition temperatures used to make $CdTe_{1-x}S_x$ [155]:

$$\delta_S < \delta_{Cd} < \delta_{Te}. \quad (4.5)$$

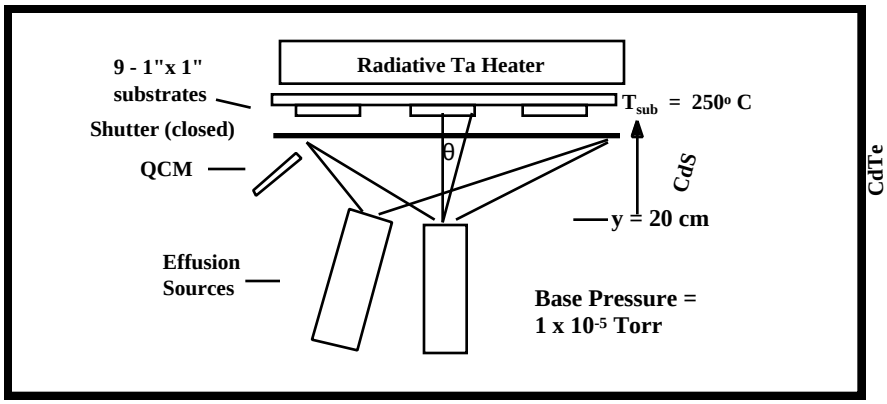


Figure 4.3 Schematic cross-section view of physical deposition system for $CdTe_{1-x}S_x$ absorber layers.

$CdTe_{1-x}S_x$ films were deposited as uniform layers and as stepped layers to investigate the rate of CdS consumption for different quantities and distributions of S within the absorber layer. The stepped layers were formed by depositing a ~1 μm uniform layer at the CdS interface and then shutting off the CdS source.

4.3.1.2 Film Characterization - CdS

Optical absorption and step profilometry measurements were used to determine initial CdS film thickness. Figure 4.4 shows the transmission, normalized for reflection, obtained from CdTe/ITO/7059 samples deposited during the present contract year. For the structures employed in this work, at constant ITO thickness, the CdS thickness is determined using:

$$d\ (cm) = 8 \times 10^{-6} \{\ln T(400nm) - 0.43\}. \quad (4.6)$$

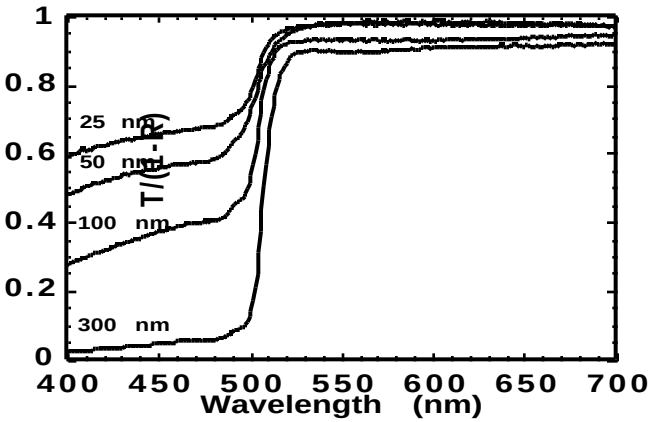


Figure 4.4 Measured optical transmission, normalized for reflection of CdS/ITO/7059 (samples from depositions 12148, 12157, 12176, and 12143).

A key concern raised in 1996, the drop in open circuit voltage experienced as CdS thickness, is reduced. The existence of localized and somewhat uniformly distributed discontinuities in the CdS layer after cell fabrication offers an explanation of this phenomenon by allowing for the existence of parallel diodes between CdTe/CdS and CdTe/ITO. The latter junction exhibits a higher diode current, J_o, and will exert a limiting influence on V_{oc} depending on the ratio of areas between the two types of junctions. Junctions between the CdTe and TCO could arise due to at least three sources: 1) pinholes present in as-deposited CdS films; 2) depletion of CdS due to diffusion into CdTe; and 3) breakdown of particulate residues, leaving exposed ITO. Particulates can also create hard shunt paths, reducing V_{oc} from increased shunt conductance. These phenomena are depicted schematically in Figure 4.5, and the equivalent circuit and circuit equation are shown in Figure 4.6.

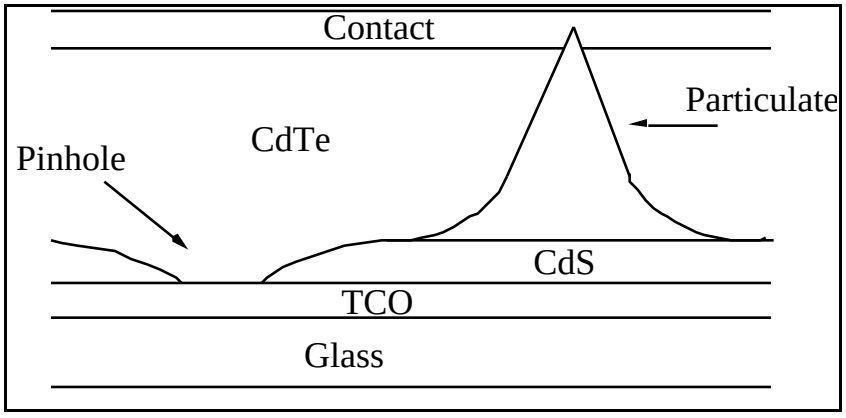
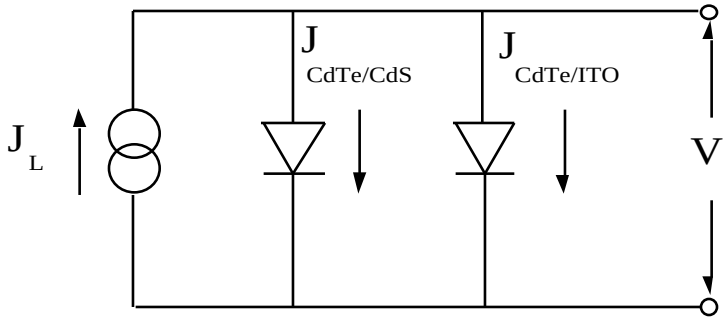


Figure 4.5 V_{oc}-limiting defects attributable to CdS and TCO processing.



$$V_{oc} = \frac{AkT}{q} \ln\left[\frac{J_L}{J_{o_{CdS}}(1 - F) + J_{o_{TCO}}(F)}\right]$$

Figure 4.6 Equivalent circuit and equation for parallel diodes between CdTe/CdS and CdTe/TCO.

To provide data for CdS films of different thicknesses made by different methods, films from different groups of the NREL National CdTe Team were microscopically surveyed for pinhole and particulate areal density using the following methodology:

1. Pinhole and Surface Particulate Area
   - A. Contrast-Enhanced Optical Microscopy
   - B. Survey > 1 cm^2 Area in 1 mm Wide Strips
   - C. Count Pinholes According to Size
   - D. Calculate Fractional Area (F)
2. Surface Particulate Height
   - A. High Magnification Microscopy (~800X)
   - B. Difference in Focus Plane from Basal Film to Tip of Particulate
3. CdS Film Thickness
   - A. Optical Transmission and Reflection
   - B. Measure in High Absorption Band (λ = 400 nm)
   - C. Correct for TCO Absorption
   - D. Calculate d(CdS) using α(400 nm)

Enhanced contrast optical microscopy was used for pinhole detection on thin CdS, made possible in transmission mode by rejection of unwanted E < Eg(CdS) light using a bandpass filter as shown in Figure 4.7. The optical transmission properties of both film and filter are shown in Figure 4.8. Low magnification photographs show the contrast enhancement obtained (Figure 4.9). At higher magnifications pinholes as small as 5 µm diameter can be detected on CdS films as thin as 50 nm. Tabulation of pinholes found on surveyed strips allows the pinhole area in as-deposited films to be determined, giving a degree of quality control to the window layer. Data for the IEC and NREL CdTe Team samples is shown in Table 4.7 below.

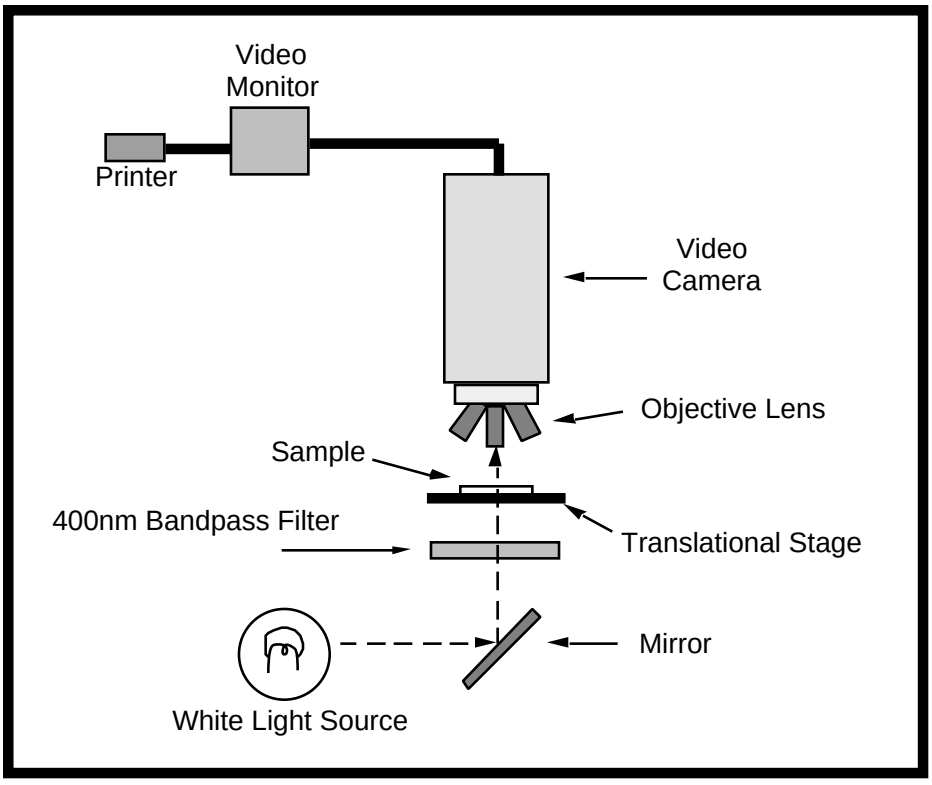


Figure 4.7 Optical arrangement used to survey CdS films.

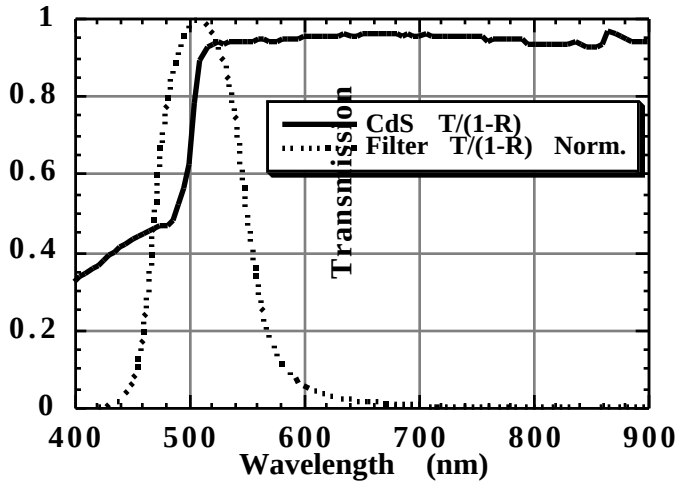
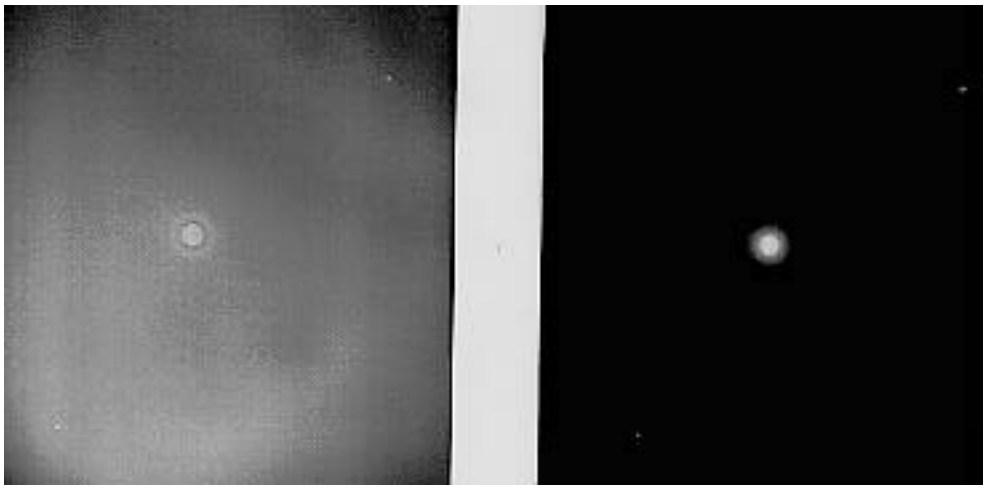


Figure 4.8 Optical transmission of CdS film and Corion 400 nm bandpass filter.



Unfiltered 80 X With 400 nm Bandpass Filter

Figure 4.9 Optical micrographs of pinholes in PVD CdS film 120 nm thick.

Table 4.7 Results of CdS film pinhole and surface particulate survey. Column definitions are as follows: TCO# = run #; d(CdS) = Thickness; Area h = area of pinholes in survey region; F_h = fractional area of pinholes; Area p = area of particulates in survey region; F_p = fractional area of particulates; F_h+F_p = sum of pinhole and particulate fractional areas.

Group	Sample ID	Superstrate	TCO #	CdS Method	d (CdS) (nm)	Area h (cm^2)	F_h	Area p (cm^2)	F_p	F_p+F_h
MRG	707	ITO/7059	92024	Sputter	225	5E-06	5E-06	3E-05	3E-05	3E-05
MRG	707	ITO/7059	92024	Sputter	225	1E-05	1E-05	5E-05	5E-05	7E-05
MRG	2080	ITO/7059	92024	Sputter	150	4E-06	4E-06	4E-05	4E-05	4E-05
MRG	2080	ITO/7059	92024	Sputter	150	9E-06	9E-06	2E-05	2E-05	3E-05
MRG	1080	ITO/7059	92024	Sputter	50	2E-05	2E-05	3E-05	3E-05	5E-05
UTol	CS 105	7059 no O2	N/A	Sputter	300	8E-05	8E-05	2E-04	2E-04	2E-04
UTol	UB 3	7059 no O2	N/A	Sputter	90	4E-06	4E-06	2E-04	2E-04	2E-04
UTol	CS 94	LOF no O2	Tec20	Sputter	50	2E-05	2E-05	2E-04	2E-04	2E-04
UTol	CS 95	LOF + O2	Tec20	Sputter	50	0E+00	0	2E-04	2E-04	2E-04
UTol	CD 92	LOF + O2	Tec15	Sputter	50	2E-05	2E-05	1E-04	1E-04	1E-04
NREL	A 208	SnO2/7059		CBD	106	1E-05	1E-05	5E-05	4E-05	5E-05
NREL	A 207	SnO2/7059		CBD	40	1E-05	1E-05	6E-05	6E-05	7E-05
CSM	3-12	SnO2/7059		Elec	~120	5E-05	3E-05	2E-06	1E-06	3E-05
CSM	28-11	SnO2/7059		Elec	~120	2E-05	5E-06	2E-06	6E-07	6E-06
IEC	12094.11	ITO/7059	92144	PVD	200	5E-06	5E-06	4E-06	4E-06	9E-06
IEC	12045.11	ITO/7059	91949	PVD	120	2E-05	2E-05	7E-06	7E-06	2E-05
IEC	12038.11	ITO/7059	91950	PVD	100	2E-05	2E-05	4E-06	4E-06	2E-05
IEC	12089.11	ITO/7059	92083	PVD	70	5E-05	5E-05	4E-06	4E-06	5E-05
IEC	12090.11	ITO/7059	92083	PVD	25	N/A	N/A	4E-06	4E-06	"4E-06"

Before microscopic examination, the pieces were ultrasonically rinsed in methanol and dried under forced argon. Films were surveyed in transmission mode with a bandpass

filter to enhance contrast. Particulates were included in the survey since they can lead to shunt paths as pinholes in CdS (formed via reaction during treatments) or spikes through the CdTe layer. Their vertical dimension (normal to film plane) was measured as: 5-10 μm on CDB and Sputtered films and < 5 μm on PVD films.

For the MRG and IEC cases, the samples were on 7059/ITO, with the ITO sputtered at IEC. The 70 and 25 nm cases were witness pieces to the set #2 samples. The NREL samples were witness pieces to those employed for cell fabrication in set #1. The University of Toledo samples were on different superstrates and sputtering conditions. The CSM samples were deposited at different pH and temperature conditions.

For the CSM samples, the number of surface particulates was very low (~1 per sample). The entire surface was surveyed (in 1 mm from the edges to discount edge, cutting, and tweezer effects). The sample 3-12 was deposited at pH = 2.65 and T = 80°C and had an order of magnitude greater density of pinhole area than sample 28-11, deposited at pH = 3.0 and T = 90°C. Sample 3-12 had over 30 pinholes, while 28-11 had only 9.

For the IEC samples made by PVD, the 25 Å case exhibited low optical contrast, making pinhole assessment difficult. For the other PVD samples, pinhole area increased with decreasing CdS thickness.

For the NREL CBD samples, the pinhole area was low but the particulate was high. EDS examination of the particulates revealed the presence of Sn, Al, Si, and Cl.

For all of the samples examined, the following short summary is given:

1. PVD: inverse correlation between pinhole area and CdS thickness; constant particulate area.

2. CBD: constant fractional pinhole and particulate area.

3. RF Sputtered: no trend in pinholes, constant particulate.

4. For PVD cells, pinhole density accounts for V_{oc} falloff with ITO; need more cell data on J_o of CdTe/SnO_2 cells to draw a firm conclusion.

The effect of the summed areal fractions on V_{oc} is shown in Table 4.8, using A-factors, JL, and J_o for the CdTe/CdS and CdTe/ITO junctions.

Table 4.8 Estimated drop in V_{oc} versus F for CdTe/CdS/ITO.

F (holes) (%)	V_{oc} (mV)	ΔV_{oc} (mV)
0	840	0
0.001	830	10
0.01	786	54
0.1	687	153
1	570	270
100	330	510

In the table, a fractional pinhole area of 1E-04 would produce a 60-70 mV drop in V_{oc} for a CdTe/CdS junction having V_{oc} = ~840 mV. Surveying every square cm of every sample is

not practical, but monitoring control or witness pieces can be a valuable tool for assessing performance of ultra-thin CdS before using it in a cell structure. In the future, we hope to combine CdS film transmission mapping with high resolution OBIC mapping to correlate the extent and uniformity of localized CdS defects with voltage output of the devices.

4.3.1.3 Film Characterization - CdTe and $CdTe_{1-x}S_x$

CdTe and $CdTe_{1-x}S_x$ film thicknesses were determined by mass gain of the superstrates after deposition. For uniform $CdTe_{1-x}S_x$ alloy films, the as-deposited composition was determined by energy dispersive x-ray spectroscopy (EDS), and wide-angle $\theta/2\theta$ scanning x-ray diffraction (XRD) and lattice parameter reduction [138]. Selected samples were analyzed in cross-section by transmission electron microscopy (TEM).

In devices, the CdS loss incurred during post-CdTe treatments was determined by measurement of the quantum efficiency from 400 to 450 nm, which is found to be limited by parasitic optical absorption in the CdS layer. In the device structure, the CdS layer essentially acts as a thickness-dependent optical filter for the high absorption region ($E > E_g$), since carriers which are generated in the CdS layer are not collected. For the present devices this assumption has been confirmed by selectively etching away the Te-rich layers and comparing the 400 nm to 450 nm optical transmission to the quantum efficiency as shown in Figure 4.10. In the case shown, the values at 400 nm differ by less than 2 relative percent, which translates to an error in CdS thickness of ±5 nm. For routine use with small area cells, care must be taken to minimize errors in the cell area used to compute the quantum efficiency to avoid larger deviations.

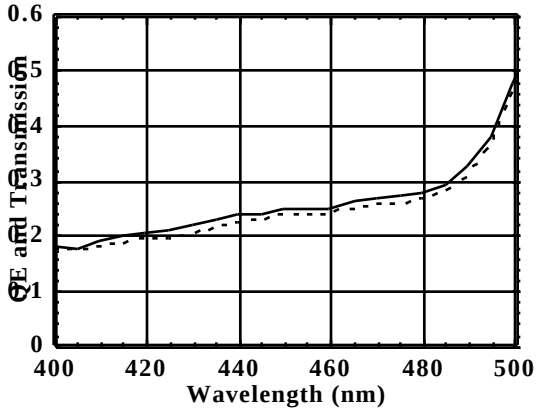


Figure 4.10 Short wavelength quantum efficiency of CdTe/CdS thin-film device (solid line) compared to CdS transmission (dotted line) after removal of Te-rich layers (sample 40992.31/12127.31).

The accumulation of CdS within the absorber layer after thermal and chemical treatments was determined by x-ray diffraction line profile analysis. XRD techniques yield lattice parameter variations in the layers producing the diffracted signal, which for the CdTe (511) or (531) peaks, is restricted to a depth of 3 μm. For glancing XRD techniques, in which the primary beam angle is fixed, the depth sampled is restricted to thinner surface layers. Similarly, EDS measurements give compositional data for ~0.5 - 1 μm from the exposed "back" surface. Obtaining compositional data near the junction region by these methods thus requires thinner absorber layers; in this work, access to the junction region was facilitated by etching the absorber layer in dichromate solution to a thickness of ~ 2 μm. In

devices, the long-wavelength fall-off of the quantum efficiency provides a measure of the bandgap, hence composition, in the junction region.

X-ray diffraction measurements of the $CdTe_{1-x}S_x$ absorber layer were made with Cu-kα x-rays using a Philips/Norelco θ-2θ scanning diffractometer (Bragg-Brentano parafocusing geometry) fitted with a diffracted-beam monochrometer. Data was acquired by step-scanning: in constant time mode for broad angular scans and constant count mode for detailed peak profile acquisition. This focusing geometry, while sampling crystal populations aligned with the substrate, is not ideal for examining ultra-thin CdS or interfacial layers because of the very low diffracting volume presented by the CdS film or interface at the high angles needed for good angular resolution. For this, an effort was initiated to evaluate glancing incidence diffractometry (hybrid Seehman-Bohlin parafocusing geometry) of CdS/CdTe structures in which the CdTe was chemically thinned to < 0.5 µm (samples prepared by Andreas Fischer and Al Compaan at the University of Toledo).

The limitations of the measurements and analyses are as follows. The x-ray sampling depth, defined as the film thickness contributing to detectable diffracted x-ray signal, is a function of the Bragg angle and varies from ~1 µm at $2\theta = 20°$ to ~4 µm at $2\theta = 80°$. Thus, devices with thick CdTe, > 3 µm, had to be thinned to access the interfacial region. Variability in CdTe/CdS sample area makes comparative intensities useless, so these have been avoided in the results section. A sample broad θ-2θ scan and corresponding Nelson-Riley-Sinclair-Taylor (NRST) fit is presented in Figure 4.11 and Figure 4.12. The error in the extrapolated "precision" lattice parameter, +/- 0.001 Å, is related to the step size and SNR of the peaks, which lead to errors in d-spacing. This translates to an absolute compositional error of +/- 0.3%. On narrow angle scans, detection of an alloy component depends on thickness and attenuation. For the diffraction system used, a SNR = 1 is obtained for the (511) peak of a CdTe film 20-30 nm thick.

On all data, standard spectral reductions to remove α_2 components, smooth data, and calculate lattice parameter were performed using software developed at IEC by Brian McCandless and Garth Jensen in 1996. Quantification of x-ray diffraction line profiles was achieved by Fourier deconvolution of the diffractometer instrument function from the measured profiles, using an annealed CdTe powder standard for the desired (hkl) reflection. The resulting profiles consisted of an angular distribution of intensities which were numerically integrated with respect to composition, yielding a net CdS content in $CdTe_{1-x}S_x$. The specific reduction steps used to determine film orientation, "bulk" absorber layer $CdTe_{1-x}S_x$ composition, and to infer compositional distribution are summarized below.

<u>$CdTe_{1-x}S_x$ Film Orientation and Bulk $CdTe_{1-x}S_x$ Composition</u>

- Acquire broad 2θ scan (20-90°, step = 0.05°, count for 2 or 4 seconds per step).
- Remove α_2 components and smooth (floating 3-point binomial).
- Index pattern with ICDD standard using most intense component of (hkl) peaks.
- Compute orientation parameter, p(111), by method of Harris [156] for fiber texture analysis. In this study, p(111) was computed using first 7 (hkl) peaks of the random pattern. Thus, p(111) = 7 indicates a perfectly (111) oriented film, p(111) = 1 indicates random orientation, and p(111) < 1 indicates dominance of a different orientation.
- Compute precision lattice parameter using Nelson-Riley-Sinclair-Taylor reduction [157, 158].

- Compute $CdTe_{1-x}S_x$ composition corresponding to lattice parameter using Vegard relation for the CdS-CdTe system: $x = 1.508 \times (6.481 - a_o)$ [138].

$CdTe_{1-x}S_x$ Compositional Distribution

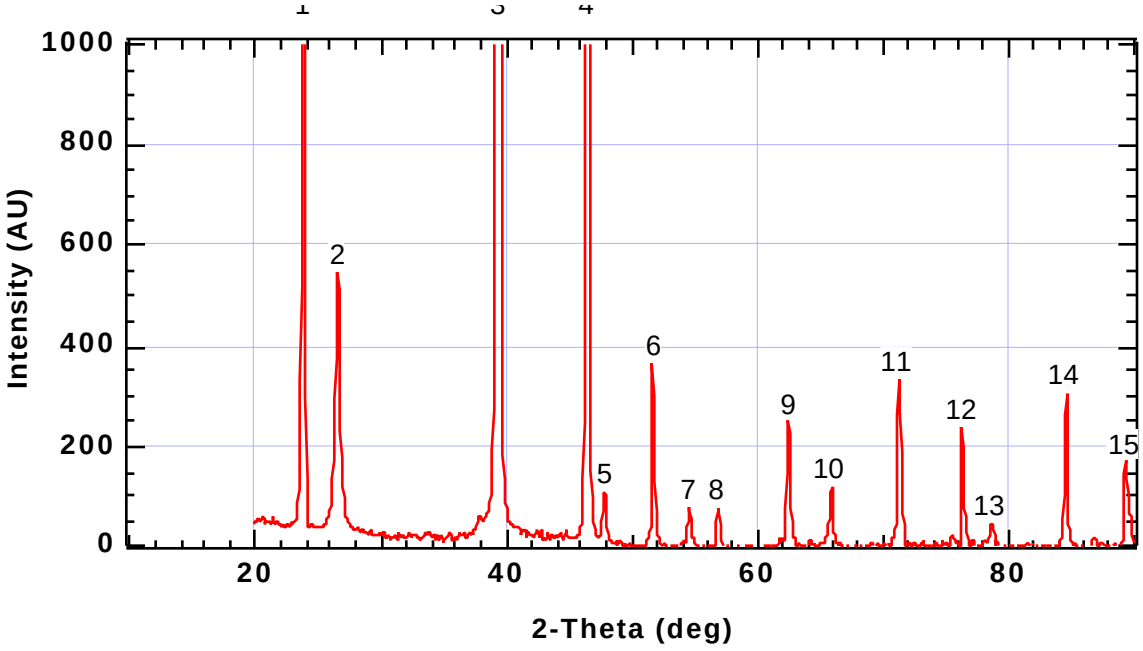
- Acquire narrow 2θ scan (step = 0.01°, constant count mode = 1000 counts per step) of high angle peak such as (511).
- Remove α_2 components and smooth (floating 3-point binomial).
- Normalize profile to most intense component.
- Fit CdTe side of profile to Pearson VII to determine HWHM [159]. For high angle peaks, such as CdTe (511), the presence of asymmetric components on high-angle side is interpreted as $CdTe_{1-x}S_x$ alloy [160] having composition given by: $x = 1.508 \times (6.481 - a_o)$ [138].
- Deconvolve instrument function [161]
- Estimate integrated CdS content.
- Determine equivalent CdS thickness.
- Compare to change in CdS thickness estimated from changes in the optical transmission of the CdS layer inferred from the device quantum efficiency at 400 nm as described above.

$CdS_{1-y}Te_y$ Compositional Distribution

- Acquire narrow 2θ scan with fixed incident beam angle.
- Remove α_2 components and smooth (floating 3-point binomial).

SCI5EB.TXT

alpha2 stripped, 3 pt. binomial smoothing, step=0.05°, 4 sec.



No.	2 theta	cnts	d (A)	
1	23.8	1186.7	3.7355	
2	26.55	550.08	3.3545	
3	39.3	6065.5	2.2906	
4	46.45	2001.3	1.9533	
5	47.85	113.02	1.8993	
6	51.7	369.84	1.7666	
7	54.6	82.795	1.6794	
8	56.85	80.235	1.6182	
9	62.45	254.04	1.4858	
10	65.85	121.48	1.4171	
11	71.25	336.77	1.3224	
12	76.35	239.00	1.2462	
13	78.6	47.640	1.2161	
14	84.55	307.14	1.1450	
15	89.4	173.33	1.0950	

Figure 4.11 Data Example 1 - Broad scan and peak table - SCI 005 after thinning to 2 µm.

SCI 005 - Extrapolated Lattice Parameter = 6.479 Å (x ~ 0.3%)

peak	TwoTheta	NRST	H	K	L	a
1	23.8	4.626	1	1	1	6.47011
2	39.3	2.611	2	2	0	6.47889
3	46.45	2.112	3	1	1	6.47845
4	56.85	1.591	4	0	0	6.47283
5	62.45	1.376	3	3	1	6.4768
6	71.25	1.098	4	2	2	6.47851
7	76.35	0.963	5	1	1	6.47584
8	84.55	0.777	4	4	0	6.47752
9	89.4	0.682	5	3	1	6.47864

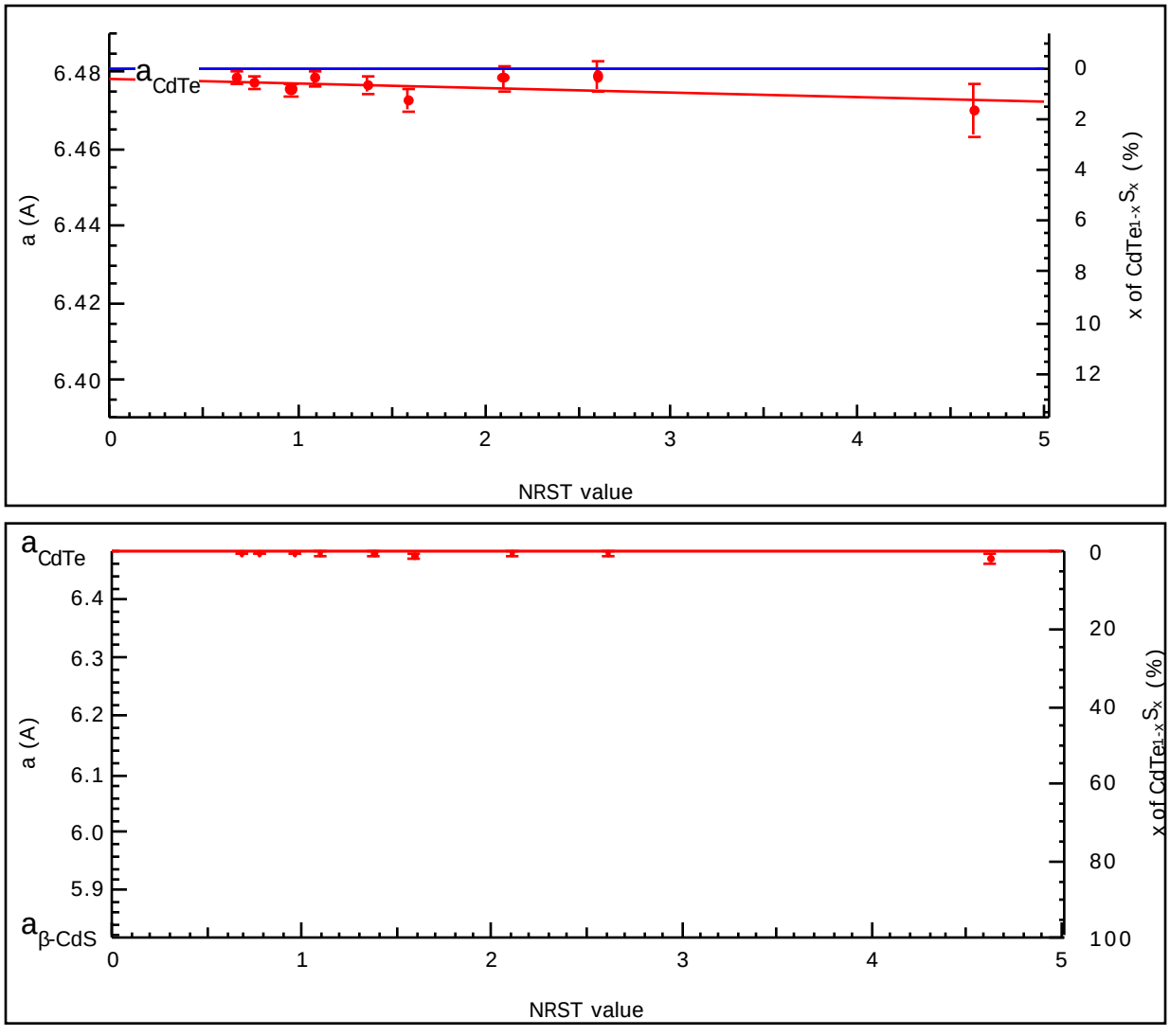


Figure 4.12 Data Example 2 - NRST reduction of $CdTe_{1-x}S_x$ peaks of Example 1.

4.3.2 CdS Window-Absorber Layer Interaction

The driving force for diffusion between CdTe and CdS layers is the chemical equilibrium for the CdTe-CdS system at the processing temperatures. In practice, the extent of diffusion by CdS into the CdTe layer has been shown to depend on the equilibrium condition [162] but also on kinetic controlling factors such as chloride and oxygen concentration in processing ambient and CdTe grain size prior to $CdCl_2$ treatment [154]. The equilibrium phase diagram for the CdTe-CdS system is shown in Figure 4.13, incorporating data points for 525°C determined during 1997 by lattice parameter reduction of $CdTe_{0.5}S_{0.5}$ films after heat treatment in argon for several hours.

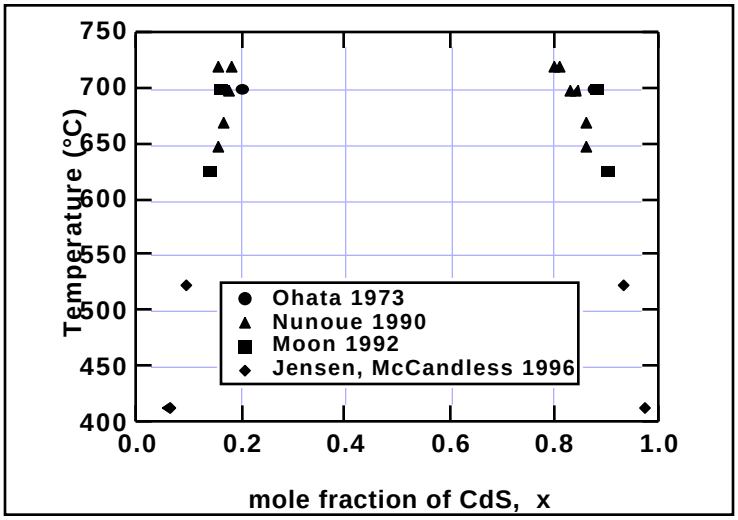


Figure 4.13 Equilibrium phase diagram for CdTe-CdS incorporating IEC data for films and powder and film data from References 163, 164, 165.

Alloying also changes the location of the absorption edge of the absorber layer, shifting it to lower energy for CdS mole fractions below ~0.28. The bandgap variation with alloy composition can be expressed:

$$Eg\ (eV) = 1.74x^2 - 1.01x + 1.51. \qquad (4.7)$$

This variation accounts for the observed shift in the long-wavelength falloff in quantum efficiency for different devices, allowing estimates of the CdS concentration in the junction region to be made.

On the CdTe-rich side of equilibrium, the location of the miscibility gap defines the upper limit of CdS incorporation which can exist for CdTe-CdS at thermal equilibrium. For CdTe absorber layer films of different thicknesses, the molar fraction of CdS incorporated as alloy can be expressed as an equivalent CdS layer thickness (Figure 4.14). Thus, measurement of the total mole fraction of CdS contained in the absorber layer after processing yields an equivalent CdS layer thickness that lost from the window layer. As described in Section 4.3.1, x-ray diffraction and optical techniques were employed to monitor the CdS distribution in the structure at different stages of processing. Figure 4.15 shows the x-ray diffraction (511) line profile and window layer optical transmission before and after cell fabrication. The loss in CdS thickness seen in the optical plot correlates with the total CdS taken up as $CdTe_{1-x}S_x$ alloy; analysis of the XRD line profile gives an equivalent d(CdS) = 48 nm, while the optical analysis gives Δd(CdS) = 55 nm.

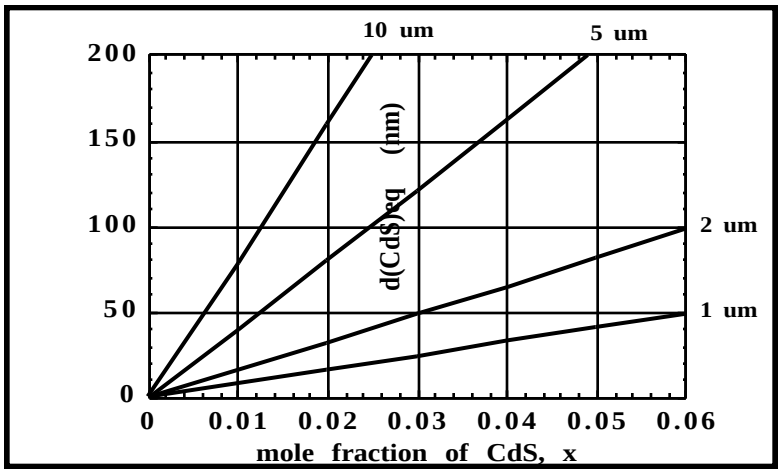


Figure 4.14 Equivalent CdS thickness versus molar fraction of CdS in $CdTe_{1-x}S_x$ for different total alloy film thicknesses. Single crystal densities were assumed in this approximation.

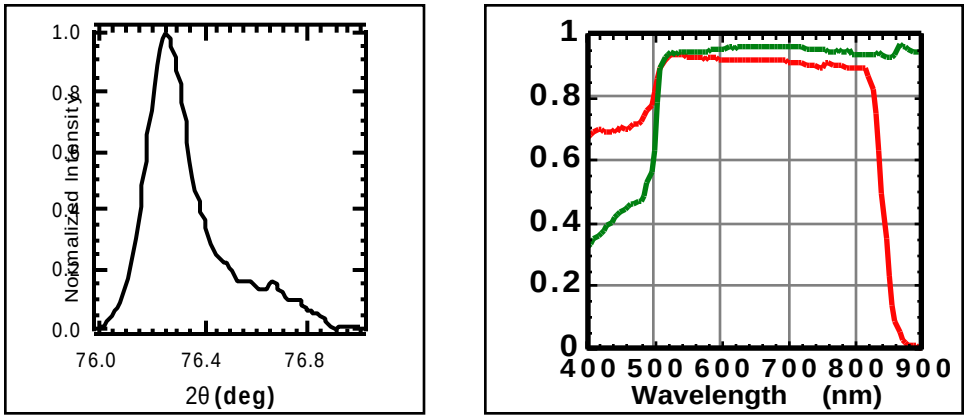


Figure 4.15 X-ray diffraction line profile of $CdTe_{1-x}S_x$ (511) after device processing (left) and optical transmission of CdS before processing and device quantum efficiency (right).

These measurement techniques were used to analyze samples fabricated by the members of the NREL CdTe Team. Devices were made with "thick" and "thin" CdS on TCO/glass superstrates provided by Chris Ferekides of the University of South Florida. The samples were selected from a larger group to give two CdS thicknesses: ~50 nm and ~130 nm. The J-V and QE characteristics of the devices were measured and reported by Jim Sites of Colorado State University. XRD analysis was performed at the Institute of Energy Conversion and selected samples were forwarded to the National Renewable Energy Laboratory for SIMS analysis, which was completed in April, 1997. The groups represented on the national team which participated in this and related XRD analyses are listed, with abbreviations, below:

Colorado School of Mines	CSM
Golden Photon, Incorporated	GPI
Institute of Energy Conversion	IEC
National Renewable Energy Laboratory	NREL
Solar Cells, Incorporated	SCI
University of South Florida	USF
University of Toledo	UT

The samples used in the study were from CdS Team "Set #1" and were fabricated on SnO_2/7059 superstrates provided by Chris Ferekides at the University of South Florida. Each participating team member was asked to prepare devices with "thick" and "thin" CdS using their standard process. Given that fabrication processes are constantly evolving, the findings herein apply to CdTe/CdS processed in the early 1996 period. Golden Photon did not participate in this particular study, but their standard material was provided privately for XRD analysis and constitutes a unique data set. The deposition processes and as-received film thicknesses represented in this study are listed in Table 4.9. On the CSM, IEC, and UT samples, sufficient CdTe area was available for performing XRD measurements; for the NREL, SCI, and USF samples, the back contacts were removed to provide sufficient exposed CdTe area for XRD analysis.

Table 4.9 Participating groups, deposition processes, and approximate film thicknesses for Set #1 samples used in x-ray diffraction study: CSS = close-space sublimation, ED = electrodeposition, EVD = elemental vapor deposition, PVD = physical vapor deposition, RFSD = rf sputter deposition.

Group	CdS Deposition Method	CdS Initial Thicknesses (nm)	CdTe Deposition Method	CdTe Thickness (μm)
CSM	CBD	70 and 150	ED	2
IEC	PVD	50 and 110	PVD	4-5
NREL	CBD	90 and 140	CSS	7-8
SCI	CSS	60, 100, 150	EVD	4-5
USF	CBD	75 and 105	CSS	7-8
UT	RFSD	40 and 140	SD	2

Table 4.10 summarizes the methods used to reduce the CdTe layer thickness and the XRD measurements performed on each sample. Final thicknesses were checked by profilometry.

Table 4.10 Summary of sample identification, preparation and XRD measurements performed.

Group/Sample #	d_i (CdS) nm	d(CdTe) µm	XRD Broad	Scan (511)	Thinning Technique	XRD Broad	Scan (511)
CSM 655	70	2	√	√	none	n/a	n/a
CSM 651	150	2	√	√	none	n/a	n/a
IEC 913.13	50	4 - 5	√	√	dichromate	√	√
IEC 913.12	110	4 - 5	√	√	dichromate	√	√
NREL A85	90	7 - 8	√	√	dichromate	√	√
NREL A84	140	7 - 8	√	√	dichromate	√	√
SCI 001	60	4 - 5	√	-	dichromate	-	√
SCI 002	60	4 - 5	√	√	bromine-methanol	√	√
SCI 004	100	4 - 5	√	√	bromine-methanol	√	√
SCI 005	150	4 - 5	√	-	dichromate	-	√
SCI 006	150	4 - 5	√	√	bromine-methanol	√	√
USF 8-14A-14	75	7 - 8	√	√	mech + dichromate	√	√
USF 8-14A-16	105	7 - 8	√	√	mech + dichromate	√	√
UT 306	40	2	√	√	none	n/a	n/a
UT 304	140	2	√	√	none	n/a	n/a

4.3.2.1 $CdTe_{1-x}S_x$ Film Orientation and Bulk $CdTe_{1-x}S_x$ Composition

The orientation parameter, lattice parameter and value of x in $CdTe_{1-x}S_x$ for samples before and after thinning to ~2 µm are shown in Table 4.11. To compare all samples at equivalent CdTe thickness, refer to the "Thinned" column.

Table 4.11 Orientation and CdTe1-xSx composition from broad XRD scans before (Initial) and after thinning (Thinned) CdTe layer to 2 µm.

Sample	d_i (CdS) (nm)	Orientation Parameter p(111)		Lattice Parameter (Å) +/- 0.001 Å		x in $CdTe_{1-x}S_x$ (%) +/- 0.3%	
		Initial	Thinned	Initial	Thinned	Initial	Thinned
CSM 655	70	n/a	0.1	n/a	6.476	n/a	0.7
CSM 651	150	n/a	0.3	n/a	6.470	n/a	1.6
IEC 913.13	50	0.7	0.7	6.479	6.478	0.3	0.4
IEC 913.12	110	0.7	0.8	6.479	6.478	0.3	0.4
NREL A 85	90	0.5	1.0	6.479	6.479	0.3	0.3
NREL A84	140	0.7	0.8	6.480	6.480	0.2	0.2
SCI 002	60	0.4	0.3	6.477	6.480	0.6	0.2
SCI 004	100	0.3	0.3	6.479	6.479	0.3	0.3
SCI 005	150	0.3	0.2	6.478	6.479	0.4	0.3
USF 14	75	1.2	1.6	6.480	6.476	0.2	0.7
USF 16	105	1.1	1.3	6.478	6.480	0.4	0.2
UT 306	40	n/a	0.3	n/a	6.475	n/a	0.9
UT 304	140	n/a	0.5	n/a	6.477	n/a	0.6

In all but the USF films, p(111) is less than 1, indicating preferential orientation of a different plane, which was the (220) in all cases. The USF films exhibited p(111) slightly

greater than 1, indicating slight (111) preferred texture. In general, the orientation parameter was similar for each group of samples and at all thicknesses. With respect to "bulk" S composition determined by the Nelson-Riley reduction of all (hkl) 2θ values, the CSM and UT samples exhibited the smallest lattice parameter and therefore highest S compositions. Within each group, there does not appear to be any correlation between the CdS thickness and the "bulk" S content derived from the shift in lattice parameter.

4.3.2.2 $CdTe_{1-x}S_x$ Compositional Distribution

Narrow angle diffraction scans yielded similar profiles for all high-angle (hkl) peaks, allowing a single (hkl) peak to be used to estimate CdS uptake by the CdTe film. Figure 4.16 shows the profiles obtained for the (422), (511), (440), and (531) peaks of IEC film 913.12. Taking into account angular divergence, the peaks exhibited similar profiles, allowing any one to be used for comparative purposes from sample to sample. Figure 4.17 to Figure 4.22 show the (511) profiles for all of the samples. In the CSM case, the (440) is also shown due to an unidentified peak overlap in the (511) profile.

Estimates of the equivalent CdS film consumed during processing for each sample is shown in Table 4.12 and is summarized graphically in Figure 4.23. These estimates are based on interpretation of XRD peak profiles and changes in the optical transmission of the CdS layer inferred from the device quantum efficiency at 400 nm. There is reasonable agreement between the values obtained from the XRD profiles and from the short wavelength quantum efficiency. For several cases, the quantity of CdS diffused into and alloyed with the CdTe film is greater for thicker CdS films. This may merely reflect the concentration of species available for diffusion.

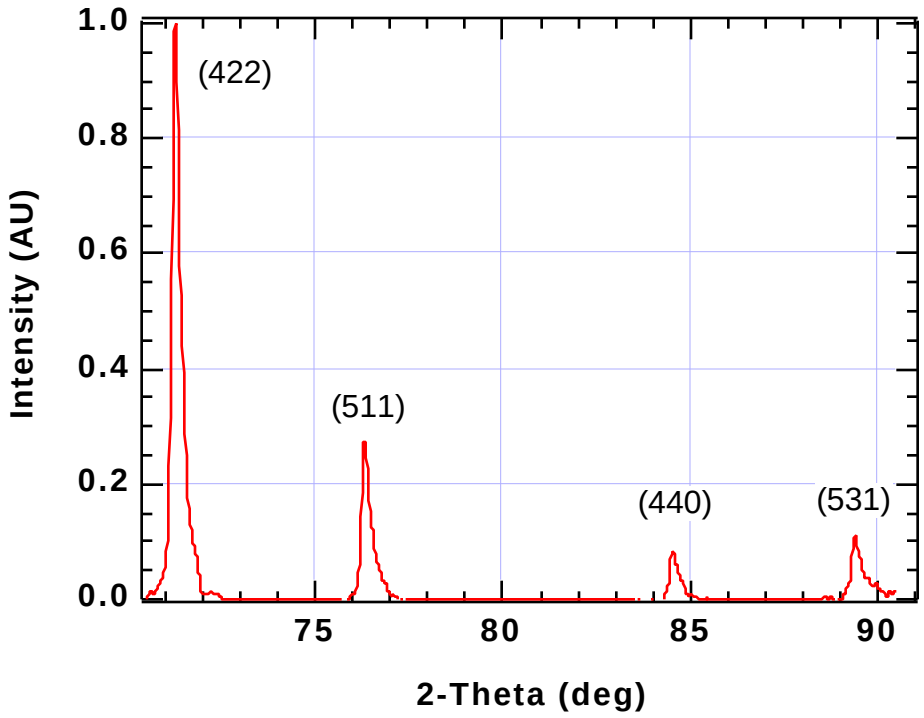


Figure 4.16 Narrow angle XRD peaks of different (hkl) for IEC sample 913.12 after thinning to 2 µm.

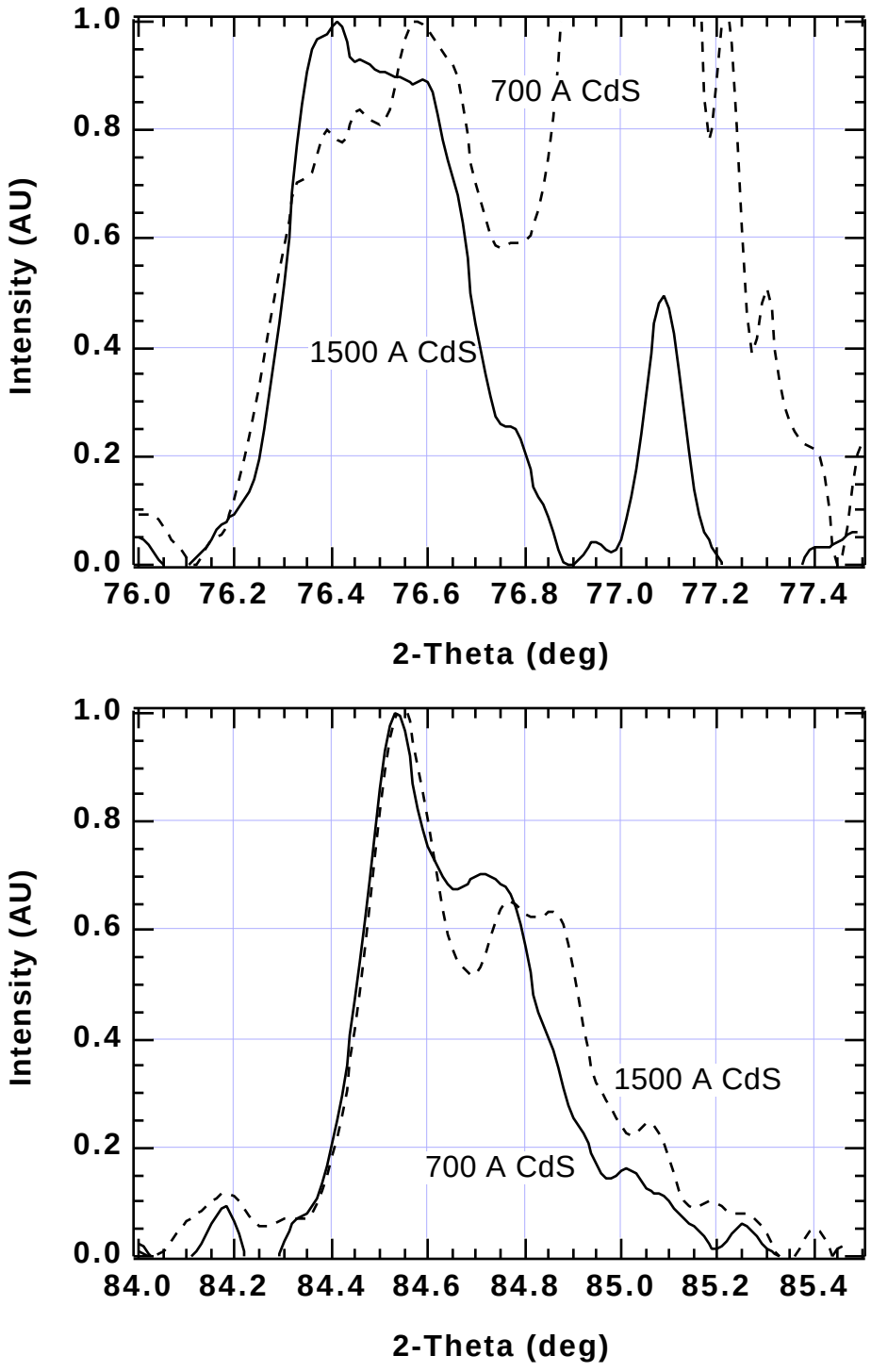


Figure 4.17 Narrow angle (511) (top) and (440) (bottom) XRD peak profiles for CSM samples with different CdS thickness.

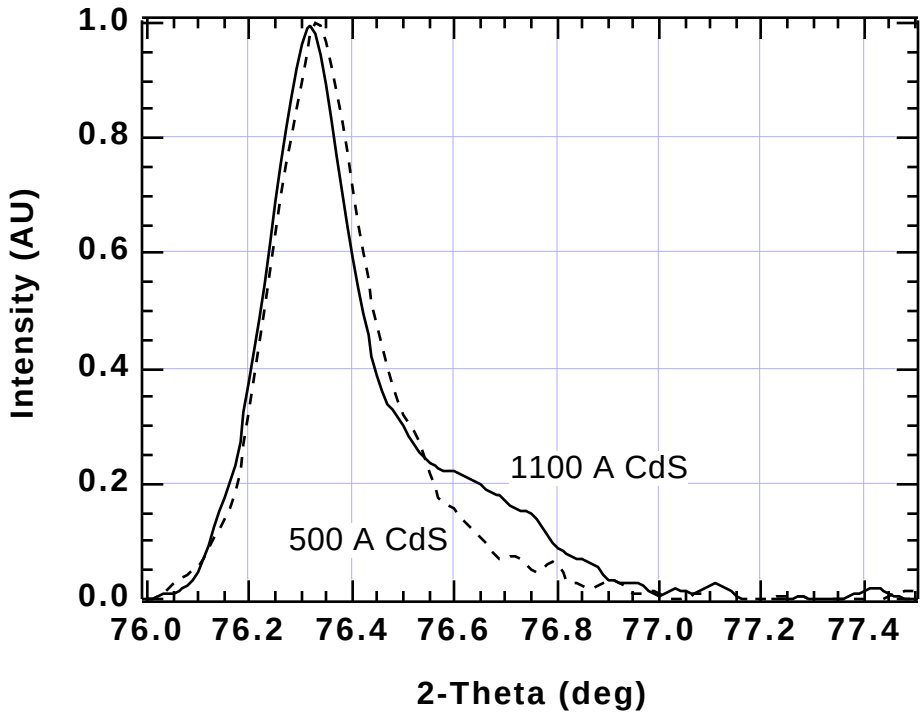


Figure 4.18 Narrow angle (511) XRD peak profiles for IEC samples with different CdS thickness after thinning the CdTe layer to ~2 µm.

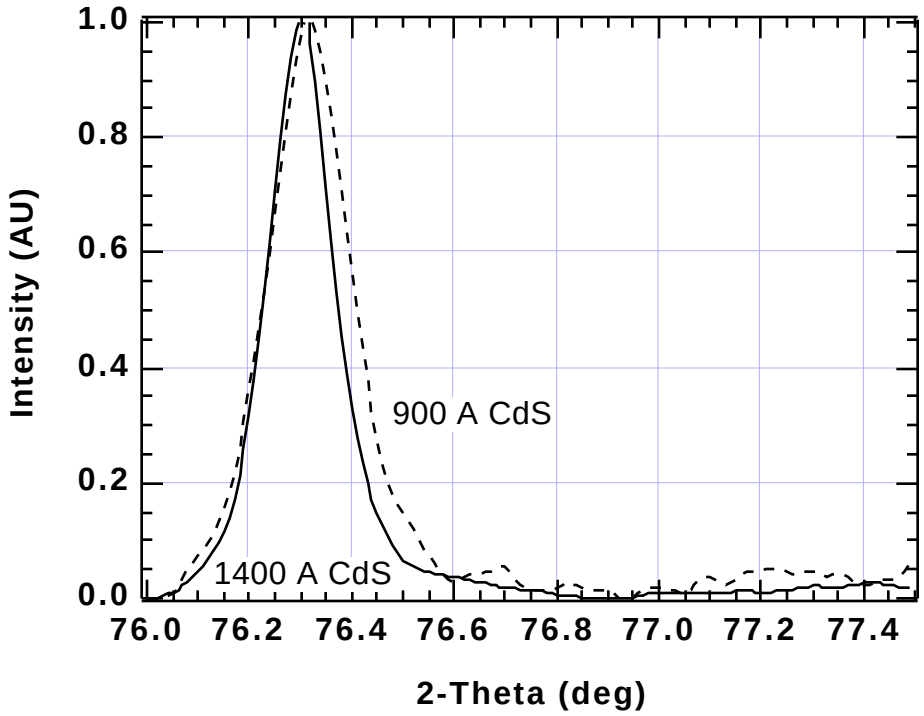


Figure 4.19 Narrow angle (511) XRD peak profiles for NREL samples with different CdS thickness after thinning the CdTe layer to ~2 µm.

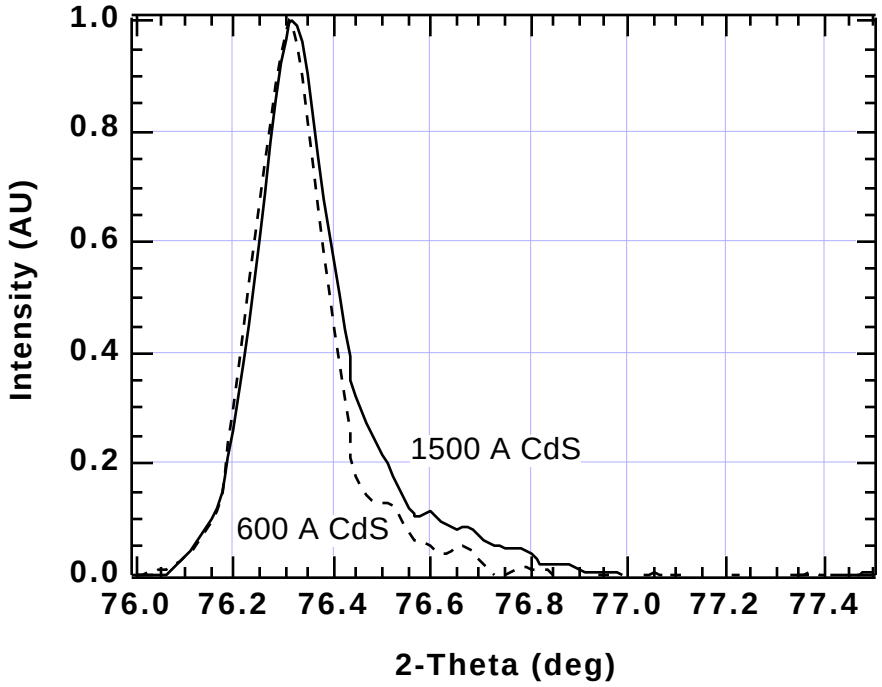


Figure 4.20 Narrow angle (511) XRD peak profiles for SCI samples with different CdS thickness after thinning the CdTe layer to ~2 μm.

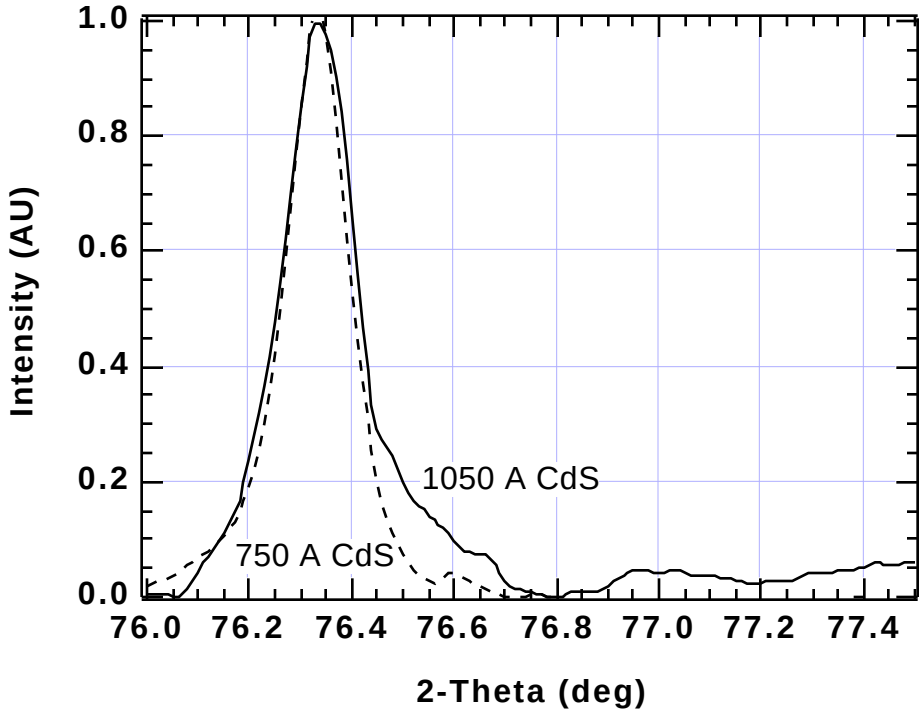


Figure 4.21 Narrow angle (511) XRD peak profiles for USF samples with different CdS thickness after thinning the CdTe layer to ~2 μm.

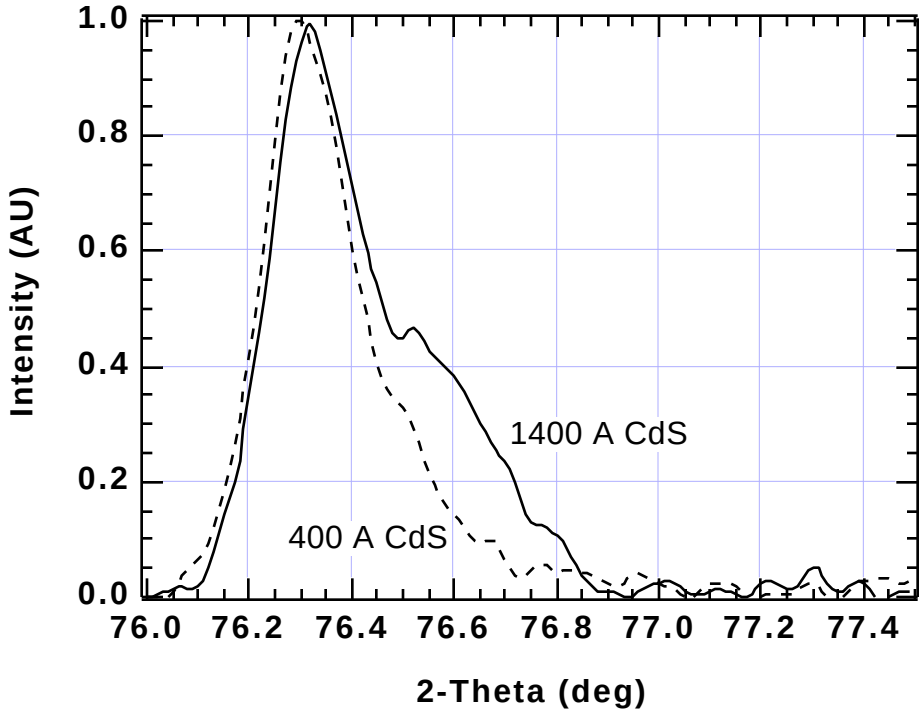


Figure 4.22 Narrow angle (511) XRD peak profiles for UT samples with different CdS thickness.

Table 4.12 Summary of CdTe peak profile and estimate of CdS uptake by CdTe film. The instrument HWHM for CdTe is 0.06˚. Determinations made by analysis of XRD peak profiles are compared to those made by change in CdS transmission. Composition of the doublet component is indicated in parentheses in atomic percent.

Sample	d(CdS) Initial (nm)	XRD Profile Shape	HWHM (511) (deg)	XRD Equiv d(CdS) (nm)	Δd(CdS) from QE(400nm) (nm)
CSM 655	70	doublet (1.9 %)	0.10	43	41
CSM 651	150	doublet (3.5 %)	0.10	47	54
IEC 913.13	50	tail	0.10	32	32
IEC 913.12	110	tail	0.10	55	80
NREL A85	90	tail	0.09	12	9
NREL A84	140	tail	0.09	11	27
SCI 002	60	tail	0.08	27	19
SCI 005	150	tail	0.08	30	21
USF 14	75	tail	0.07	9	11
USF 16	105	tail	0.09	17	
UT 306	40	tail	0.10	32	22
UT 304	140	doublet (2.5 %)	0.10	62	90

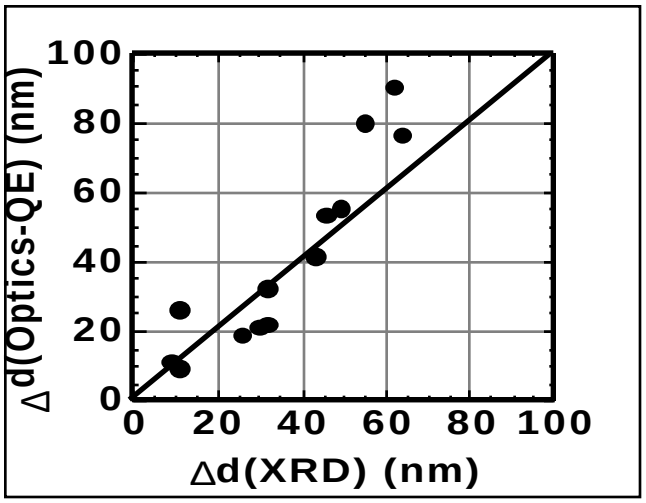


Figure 4.23 Change in CdS thickness derived from optical methods compared to that derived from X-ray diffraction measurements.

In Table 4.12, occurrence of a doublet indicates the presence of a discreet layer at the composition given in parentheses. The doublet structure can be seen in the preceding figures. Modeling of CdS-CdTe diffusion at IEC by Rajesh Venugopal in 1996 for PVD structures treated at different temperatures, times and $CdCl_2$ concentration showed that such bimodal distributions cannot be described by simple grain boundary and volume diffusion, even taking into account concentration-dependent diffusion coefficients [166]. To account for such distributions in the XRD profile it is necessary to invoke a two- or multiple-step diffusion process in which CdS is transported into the CdTe bulk quickly in the initial stages of heat treatment. For the CSM samples, the doublet data was taken from the (440) peak because the (511) peak was not clearly resolved from an unidentified adjacent peak. The presence of a doublet component in the CSM and UT samples correlates with their higher "bulk" S compositions shown in Table 4.11. The HWHM values are all very similar but are higher for the CSM, IEC, and UT cases. From the equivalent CdS thickness loss estimate, Table 4.12 and Figure 4.23 show that there is reasonable agreement between the XRD and optical methods, showing that more CdS was consumed in the CSM, IEC, and UT processes.

This can be understood by recognizing that the CSM, IEC, and UT structures were fabricated by depositing the CdTe at relatively low temperatures, below 300°C, which produces CdTe films with small grains, hence high grain boundary density. The other samples had CdTe deposited at high temperature, greater than 500°C. All of the samples have received a $CdCl_2$ treatment at around 400°C. For CdTe films deposited at low temperature, this treatment is known to promote dramatic recrystallization, hence mobility of the Cd, Te, and S atoms, resulting in enhanced interfacial diffusion. High temperature during CdTe growth produces large-grain films with lower defect density, resulting in little interaction during the chloride treatment. For the low temperature deposited films, the interaction can be minimized by performing a high temperature recrystallization before the chloride treatment may offer a means to reduce interdiffusion [167, 168]. The high temperature approach can be used to enhance performance in cells made by low deposition temperature processes, but there is still measurable CdS loss that puts a lower limit on the starting CdS thickness that can be used.

For the high temperature processes, limits in J_{sc} also appear to arise from effects due to $CdS_{1-y}Te_y$ formation in the window layer. In the quantum efficiency plots for these devices [169], the collection from 450 nm to 600 nm for the NREL and USF cells is lower than expected based on a CdS window layer. This effect is likely due to the presence of a graded $CdS_{1-y}Te_y$ layer that formed during CdTe deposition or during $CdCl_2$ treatment as observed for PVD cells [141]. More work, as described in the next section, is needed to address this problem.

4.3.2.3 $CdS_{1-y}Te_y$ Compositional Distribution

It has been previously shown that treatments of the CdS prior to CdTe deposition are necessary to minimize formation of $CdS_{1-y}Te_y$, which reduces the CdS bandgap, adding to the parasitic absorption of blue-green light [141]. In devices with ultra-thin CdS, this effect may be negligible, but as a control issue for squeezing the most out of the device in a repeatable process, the chemical interaction on the CdS side of the device cannot be ignored. In analyzing such thin CdS layers, θ-2θ XRD measurements (Bragg-Brentano) yield diffracted CdS signals that are too low to obtain compositional profiles of the high angle peaks needed. Increased signal can be achieved, however, by fixing the incident beam at a glancing angle and preparing the specimens for this type of analysis.

For this experiment 2 µm CdTe/0.2 µm CdS structures were sputter-deposited at the University of Toledo on quartz glass. The CdS was *not* treated prior to CdTe deposition. The CdTe/CdS structures were heat treated with $CdCl_2$ treatment at 320°C and 380°C in air. After heat treatment, the CdTe layer was thinned in bromine-methanol solution. The thinning procedure yielded a tapered CdTe-CdS interface around the sample edges and a maximum CdTe layer thickness of < 0.5 µm, which was sufficiently thin to permit the glancing incidence technique to be used to sample both CdTe and CdS layers simultaneously; the resulting thickness profiles are shown in Figure 4.24.

Bragg-Brentano $\theta/2\theta$ XRD scans with Cu x-rays only revealed the CdS (002) reflection at $2\theta = 26.6°$. Wide angle diffraction at 4° fixed incident angle revealed CdS (002) and (004) reflections; the (004) peaks were rescanned at smaller step size and slower scan rate to improve angular resolution and SNR. The Cu k_α x-ray penetration depth at 4° is ~450 nm in CdTe, which means that the CdS XRD signal was primarily obtained from the thinner half of the samples. Figure 4.25 shows that both shape and location of the peaks are different for the two films. For the film treated at 320°C, the peak is broadened towards $CdS_{1-y}Te_y$ and has a majority component at y = 0. The film treated at 380°C has further broadened and has shifted to y = 2.5% with a tail extending to ~3%. The upper limit of these plots, ~ 3%, agrees very well with the compositions determined by Raman spectroscopy at University of Toledo of the exposed interface. Both measurements directly confirm the diffusion of CdTe into CdS during heat treatment with $CdCl_2$. The XRD result demonstrates the potential of using glancing incident beam diffraction as a tool for evaluating the interdiffusion on the CdS side of the CdTe/CdS device. An extension of this approach will be to further thin the CdTe layers in the sample set and examine the microcomposition of the window layer.

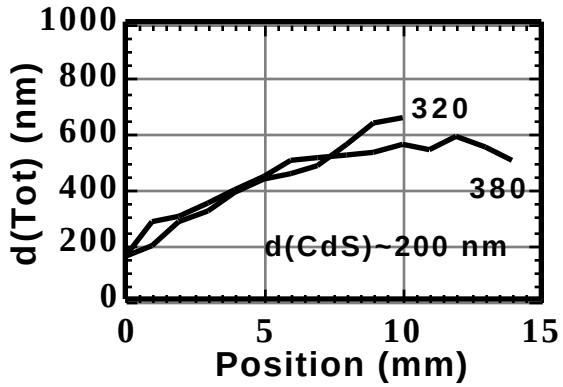


Figure 4.24 Total thickness profile of CdTe/CdS on quartz thinned with 0.05% Br_2-Ch_3OH.

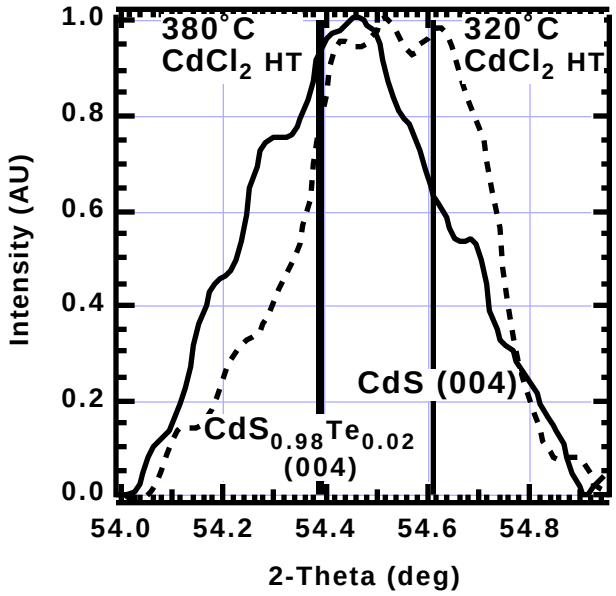


Figure 4.25 Glancing incidence XRD of CdS (004) on $CdCl_2$-treated CdTe/CdS/Quartz with CdTe thinned to profile shown in Figure 4.24; 4˚ incidence Cu-k_α.

In summary:

· The techniques of thin-film x-ray diffraction and optics are effective for assessing the interfacial chemistry of the CdTe-CdS alloy system in solar cells.

· All device structures exhibited measurable alloying between CdS and CdTe in the absorber layer. Enhanced CdS diffusion was found in devices having CdTe deposited at low temperature, T < 300°C compared to those having CdTe deposited above 500°C. This is understood by noting the dramatic recrystallization that occurs during chloride treatment of films deposited at low temperatures; films deposited at high temperatures do not undergo significant recrystallization during chloride treatment and hence absorb less CdS. In the case of sintered CdTe films, the process is carried out in the presence of chloride which results in significant CdS-uptake during CdTe film formation.

· In some of the low temperature-deposited structures the XRD profiles indicate a multi-step mixing process. The profiles of high temperature-deposited CdTe are consistent with grain boundary and volume diffusion.

· In general, the quantity of S in $CdTe_{1-x}S_x$ was greatest for the thickest CdS films, simply because more CdS was available to diffuse.

· The diffusion of CdTe into CdS needs to be examined, especially with respect to devices with CdTe deposited at high temperature.

· No correlation was found between crystallographic orientation and CdS diffusion into CdTe.

In the next phase of research, the kinetics of the CdS-CdTe intermixing and the sensitivity to the chemical environment during post-deposition treatments will be investigated.

4.3.3 Devices with $CdTe_{1-x}S_x$ Absorber Layers and Modified Post-Deposition Treatment

4.3.3.1 Preparation of Films - Absorber Layer Composition

To varying degrees, all CdTe/CdS devices contain $CdTe_{1-x}S_x$ in the junction region. Thus, it follows that direct formation of alloy absorber layers should reduce CdS loss during high temperature processing; such devices would be expected to exhibit similar performance and behavior to those in which the alloy was formed by diffusion, adding the expected benefit of reduced CdS diffusion during high temperature processing. Another approach, tested in combination with alloy absorber layers, was modification of the heat treatment to include a high temperature step to anneal crystallographic defects in the films. These defects are expected to act as pathways for diffusion.

$CdTe_{1-x}S_x$ alloy films were deposited over a wide range of composition, but primarily near the 400°C solubility limit for CdS in CdTe = 5.8%. Spatial compositional variation within each deposition made each sample unique with respect to composition. For a substrate temperature of 250°C, the film composition of the central (22) sample was a linear function of the ratio of the average CdS/CdTe effusion rates (Figure 4.26) used during deposition.

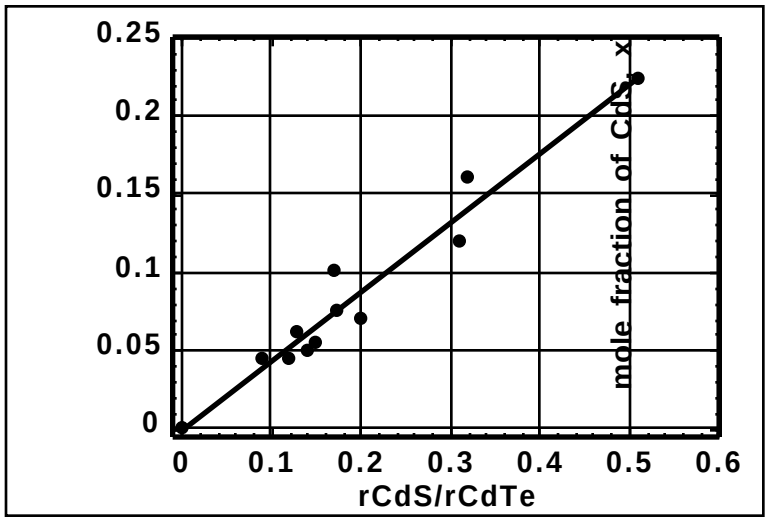


Figure 4.26 Molar fraction, x, of CdS in $CdTe_{1-x}S_x$ films versus effusion rate ratio of CdS and CdTe evaporation sources. Molar fraction determined by EDS measurement of central piece in substrate array.

X-ray diffraction and optical transmission measurements were also used to monitor CdS composition within the films. In general, compositions derived from precision lattice parameter correlated well with EDS measurements (Table 4.13).

Table 4.13 Composition of $CdTe_{1-x}S_x$ absorber layers determined by EDS and XRD methods.

Sample	x(EDS)	x(XRD)
40872.31	22.2	26.0
40988.22	6.8	6.2
41030.22	5.4	5.5
41015.22	5.4	5.4
40991.22	4.4	3.1

The optical absorption edge was measured on as-deposited $CdTe_{1-x}S_x$/CdS/ITO/glass samples before device processing to monitor run-to-run variations in film properties. Selected absorption data over the range of compositions is shown in Figure 4.27.

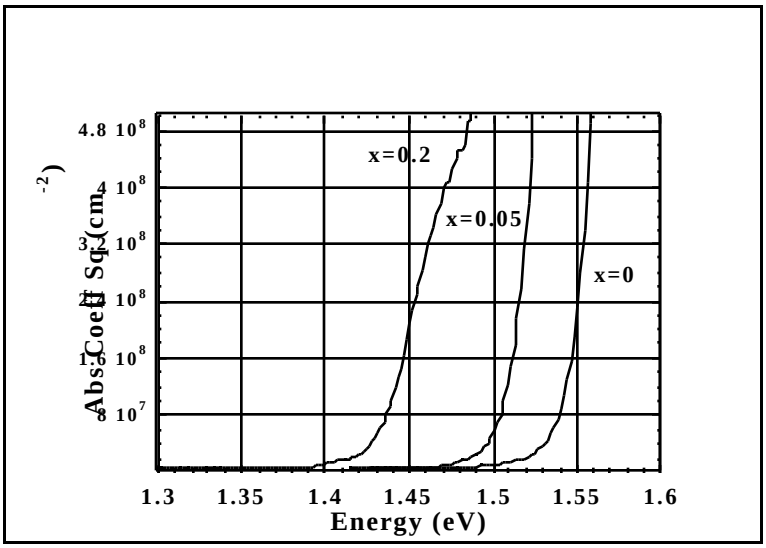


Figure 4.27 Absorption coefficient squared versus energy for selected $CdTe_{1-x}S_x$ films on CdS/ITO window layers over the range of as-deposited composition indicated.

The absorption edge energy of all samples measured approximately followed the parabolic function determined for $CdTe_{1-x}S_x$ films on *glass* as shown in Figure 4.28:

$$Eg\ (eV) = 1.74x^2 - 1.01x + 1.51. \qquad (4.8)$$

In some cases, the absorption edge shape deviated from those shown in Figure 4.27, suggesting non-uniform CdS distribution through the alloy layer. In these cases, assigning a single absorption edge energy is somewhat arbitrary, leading to significant deviations from Equation 4.8.

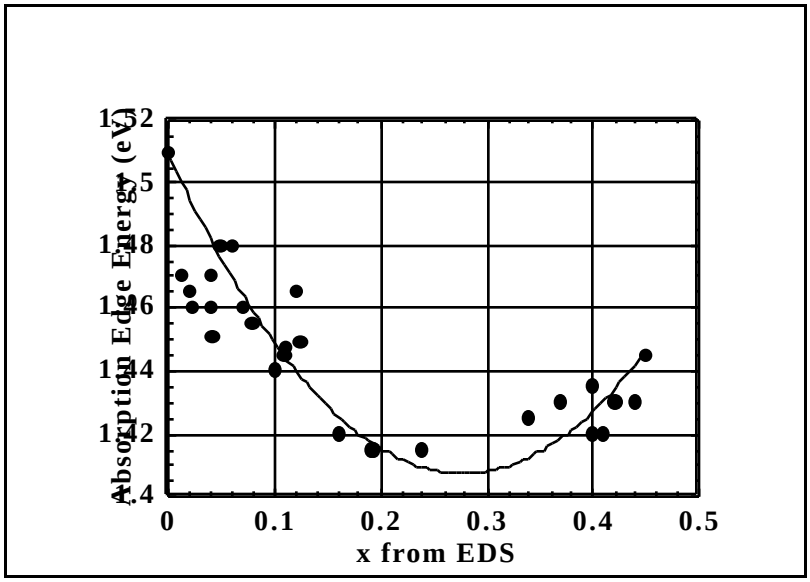


Figure 4.28 Absorption edge energy versus molar fraction, x, of CdS in $CdTe_{1-x}S_x$ for alloy layers on CdS/ITO. The solid line represents the function in Equation 4.8.

4.3.3.2 Heat Treatment of Alloy Absorber Layer Films

The presence of CdS throughout the $CdTe_{1-x}S_x$ absorber layer with x up to 0.06 did not measurably alter the recrystallization process or surface chemistry obtained after $CdCl_2$ treatment, allowing the same post-deposition processes to be used in all device configurations. For samples with as-deposited CdS content greater than 0.06, a single phase was measured after deposition, but two phases, Te-rich cubic $CdTe_{0.94}S_{0.06}$ and S-rich hexagonal $CdS_{0.97}Te_{0.03}$, were detected after $CdCl_2$ treatment (Figure 4.29). Glancing incidence XRD, Auger (measured at NREL) , and XPS (measured at NREL) measurements indicated that S-rich $CdS_{1-y}Te_y$ was distributed throughout the film, with the greatest portion segregated to the free surface of the sample. This intriguing result dictates that for devices, where uniform Te-rich phase is desired, studies of uniform layers must be restricted to films with CdS compositions *less* than the miscibility gap concentration.

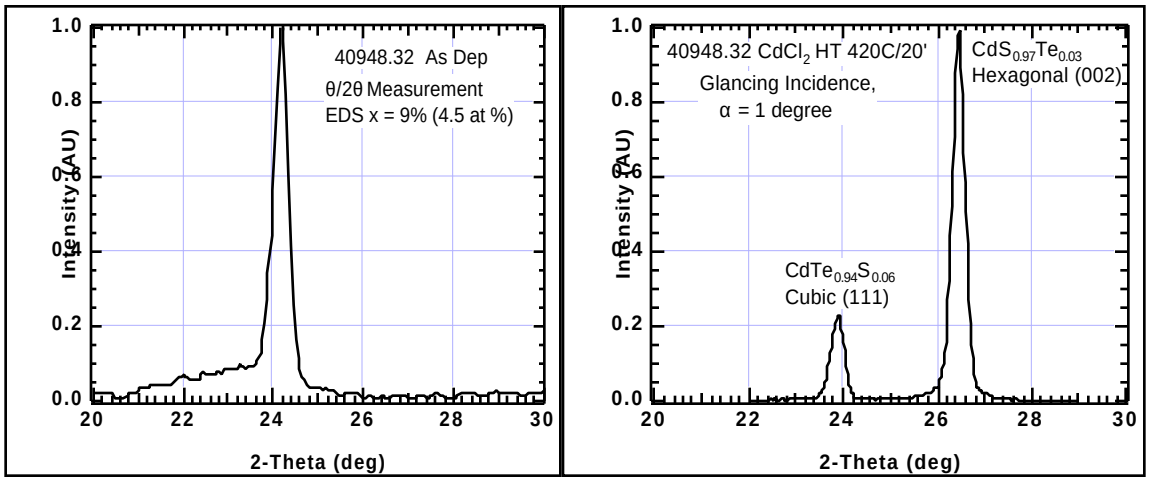


Figure 4.29 XRD spectra of single phase as-deposited $CdTe_{0.91}S_{0.09}$ and the same sample after heat treatment with $CdCl_2$ at 420˚C in air.

Using uniform layers with x < 6%, dramatic evidence for the retarding of CdS diffusion into a $CdTe_{0.95}S_{0.05}$ layer under conditions of high $CdCl_2$ concentration was found. This is apparent in the XRD line profiles of 2.5 µm thick samples (Figure 4.30). With *CdTe* absorber layers, this $CdCl_2$ treatment produced a broadened multi-modal distribution signifying the presence of several discreet regions different compositions, equivalent to a CdS layer 110 nm thick. With the $CdTe_{0.95}S_{0.05}$ layer and the *identical* $CdCl_2$ treatment, a single sharp line profile centered on the Bragg angle for x = 0.05 was obtained, having a small tail extending to x = 0.06, indicating a gain of an equivalent CdS thickness of less than 10 nm.

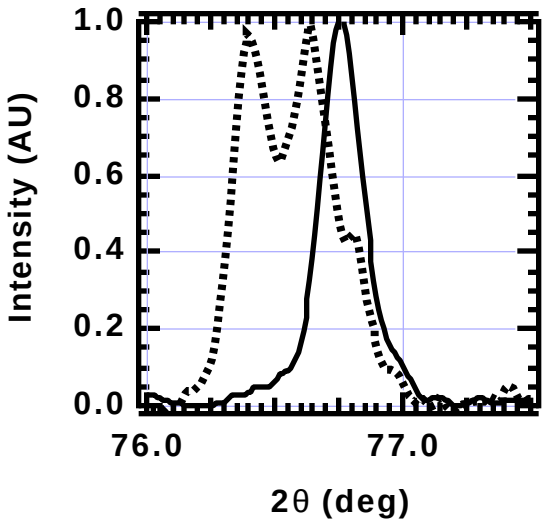


Figure 4.30 XRD (511) line profile of 2.5 µm CdTe/0.2 µm CdS (dotted) and 2.5 µm $CdTe_{0.95}S_{0.05}$/0.2 µm CdS (solid) after $CdCl_2$ treatment with high $CdCl_2$ concentration.

The retarding of CdS-CdTe interdiffusion during post-deposition processing by using alloy absorber layers was verified by EDS and XRD measurements for numerous samples. Structures of $CdTe_{0.96}S_{0.04}$ /CdS/ITO (x < solubility limit) were treated under conditions known to alter the extent of interdiffusion in CdTe/CdS/ITO samples. In some cases, a high temperature anneal (HTA) at 580°C was performed prior to $CdCl_2$ vapor treatment as described in References [136, 168, 170]. The EDS and XRD data do not reveal significant CdS uptake by the $CdTe_{1-x}S_X$ films. The materials analysis results for CdTe/CdS/ITO and $CdTe_{0.96}S_{0.04}$/CdS/ITO are compared in Table 4.14 for three treatment conditions. High-resolution XRD profiles for the three treatment methods are shown in Figure 4.31.

Table 4.14 Treatment conditions and materials data for 2.5 µm thick absorber layers on CdS/ITO after $CdCl_2$ processing at 420˚C for 30 minutes in air. The third sample in each group received a high temperature anneal (HTA) at 600˚C for 15 minutes prior to $CdCl_2$ vapor treatment.

Film Type	Treatment	AGS (µm)	EDS x ±0.3 (%)	XRD a_o (Å)	XRD x ±0.3 (%)	XRD Profile	XRD p(111)
CdTe	$CdCl_2$:MeOH	1.0	1.0	6.475	1.0	Multi	0.5
CdTe	Vapor $CdCl_2$	1.0	0.5	6.477	0.5	Asymm	1.0
CdTe	HTA + $CdCl_2$	2.0	<0.3	6.479	0.3	Asymm	1.0
$CdTe_{1-x}S_x$	$CdCl_2$:MeOH	1.1	4.8	6.446	5.3	Symm	1.1
$CdTe_{1-x}S_x$	Vapor $CdCl_2$	1.0	4.0	6.456	5.3	Symm	1.0
$CdTe_{1-x}S_x$	HTA + $CdCl_2$	1.9	5.4	6.444	5.6	Symm	0.6

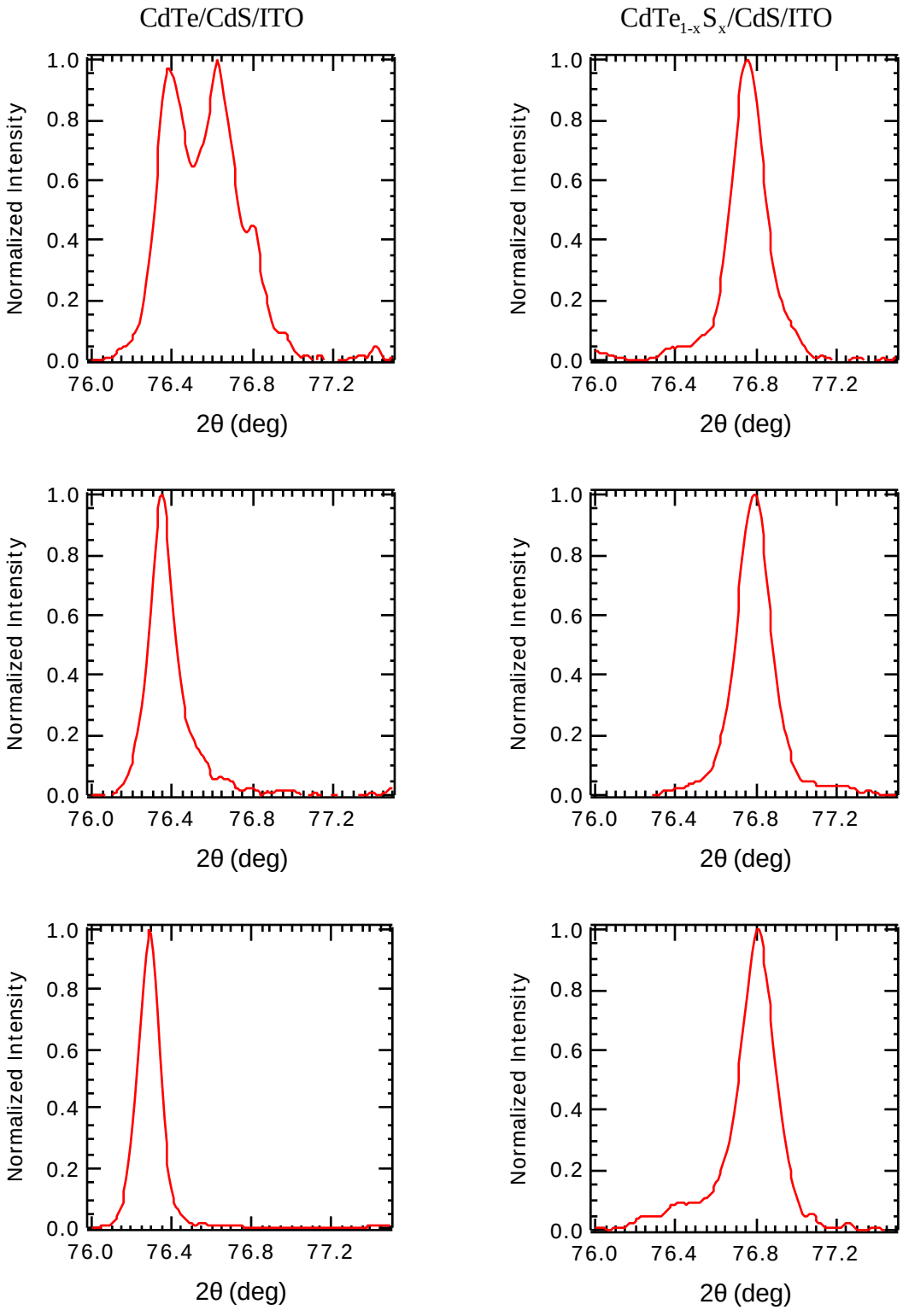


Figure 4.31 X-ray diffraction line profiles for $CdTe_{1-x}S_x$ after chloride processing at 420˚C for 30 minutes in air. Top = $CdCl_2$:MeOH; Middle = $CdCl_2$ vapor; Bottom = HTA + $CdCl_2$ vapor.

In Table 4.14, the average grain size (AGS) was determined by SEM, which showed uniform surface grain morphology with no residue on vapor-treated samples. Sulfur composition was measured by energy dispersive x-ray spectroscopy (EDS) at 20 kV. Comparison with as-deposited $CdTe_{1-x}S_x$ layers shows a drop in the S content after $CdCl_2$ treatment for the film treated with HTA prior to $CdCl_2$ vapor, due to CdS vaporization from the surface during the HTA step. Last month it was reported that films with x > solubility limit undergo phase segregation, with the S-rich phase on the surface. The precision lattice parameter, a_o, is determined from the Te-rich component of the XRD (hkl) line profiles; the three treatments chosen result in different S incorporation and asymmetry in line profile for *CdTe* films but constant lattice parameter and peak shape for $CdTe_{1-x}S_x$ films.

The retarding effect obtained by using as-deposited $CdTe_{1-x}S_x$ layers is also borne out by analysis of the devices. Table 4.15 shows the change in CdS thickness after $CdCl_2$ treatment for pure CdTe, stepped alloy, and uniform alloy absorber layers for different initial CdS thicknesses. Comparing the devices with ~200 nm CdS, it is readily seen that the uniform alloy layer reduced CdS loss by more than 2X. The stepped layer was less effective, showing that the presence of the alloy *near* the solubility limit in the junction area is not sufficient to stop CdS diffusion. In the temperature-time regime used to make device quality material, the quantity of CdS consumed is thus related to the deviation in absorber layer composition from the miscibility gap composition. Notice that the difference between the film compositions, x = 0.05, and the solubility limit, x = 0.06, allows a theoretical maximum of ~50 nm of CdS to be incorporated into a 5 μm thick alloy film. Thus, optimal control of the quantity of CdS consumed during $CdCl_2$ is achieved by depositing the alloy absorber layer with composition as close as possible to the solubility limit for the processing temperature used.

Table 4.15 also shows device J-V data for cells with different alloy configurations. The device J_{sc} increases as CdS *final* thickness is reduced. The V_{oc} is relatively constant with CdS thickness until the final CdS thickness falls below 75 nm. It is possible that non-uniform CdS consumption produces regions of complete CdS loss which results in formation of parallel junctions between the absorber and TCO layers.

Table 4.15 CdS thickness from optical and QE data compared to device J-V parameters for different alloy configurations.

As-deposited Structure	Initial d(CdS) (nm)	Final d(CdS) (nm)	Δd(CdS) (nm)	V_{oc} (mV)	J_{sc} (mA/cm^2)	FF (%)
CdTe	200	60	140	753	22.0	59.2
Stepped Alloy	220	125	95	776	22.0	67.4
(at junction	90	30	60	435	23.1	60.9
x = 0.05)	50	20	30	412	25.0	60.0
Uniform Alloy	190	130	60	792	21.2	66.3
(x = 0.05)	105	75	30	769	22.6	60.0
	70	50	30	623	24.0	61.2

These results are graphically depicted for devices made with different alloy absorber layer configurations in Figure 4.32 and Figure 4.33. In Figure 4.32, the fall-off in V_{oc} is shown for initial and final CdS thickness on the same cells. Samples with uniform alloy absorber

layers exhibited the least change in CdS thickness. It is apparent from the convergence of all devices onto the fall-off line for final CdS thickness that a fundamental mechanism which is independent of absorber layer configuration or composition dominates the devices with d(CdS) less than 100 nm. The open circles provide a significant clue; these are for devices made with bi-layer SnO_2 superstrates consisting of Libbey-Owens-Ford SnO_2/glass over-coated with high resistivity SnO_2 by Golden Photon, Inc. More will be reported on this topic in the next section. Figure 4.33 shows that the J_{sc} values for this device group approach those predicted based on window layer optical transmission and a uniform 5% collection loss.

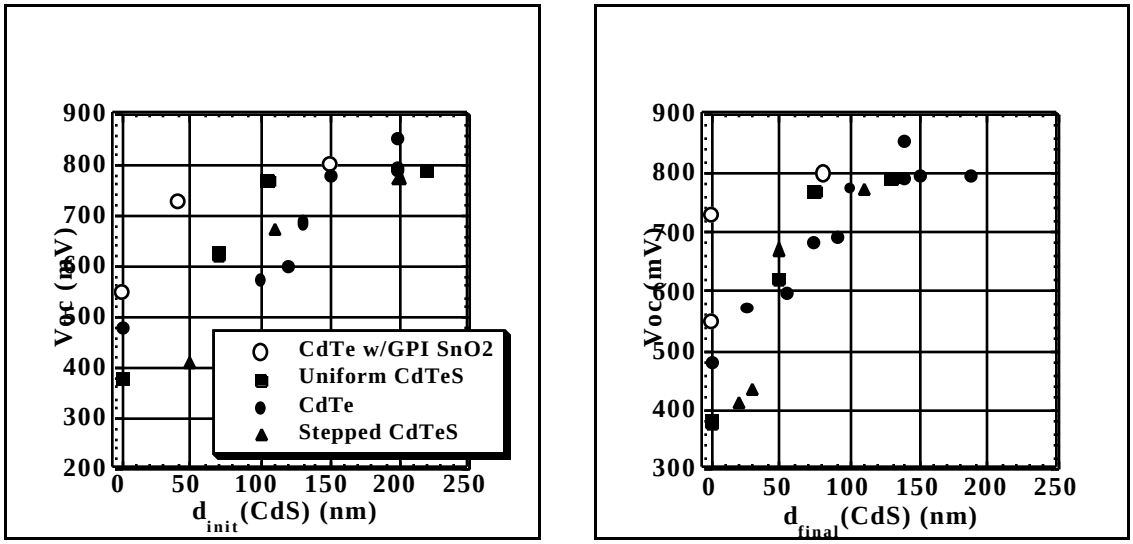


Figure 4.32 V_{oc} versus CdS thickness for different alloy absorber layer configurations. Filled markers are for devices on ITO/7059. Open circles are for devices with bi-layer SnO_2 superstrates, to be discussed in the next section.

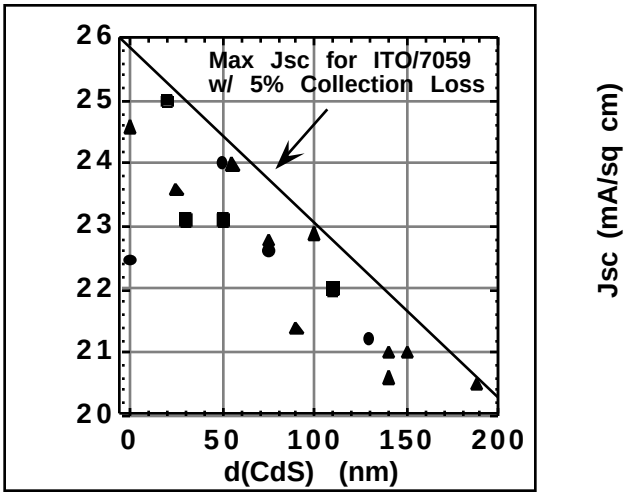


Figure 4.33 J_{sc} versus final CdS thickness in the devices of Figure 4.32.

4.3.3.3 Modified Post-Deposition Heat Treatment

The diffusion of CdS into CdTe can also be controlled by reducing the number of available diffusion pathways, which may be the single explanation needed to account for differences in devices deposited by high and low deposition temperatures. In the CdTe/CdS structures, the primary pathways are grain boundaries and crystallographic defects. Annealing the film at T > 550°C prior to chloride treatment enhances grain size, reduces crystallographic defects, and retards diffusion of CdS into CdTe [136, 168, 170]. As-deposited CdTe films have 200 nm wide columnar grains. An increase in grain size to 500 nm prior to delivery of $CdCl_2$ will reduce the total grain boundary area by ~5X, which will have a significant effect on the grain boundary diffusion rate. The final structure can exhibit grains with lateral extent greater than 5 μm, i.e., an aspect ratio greater than 1 (Figure 4.34).

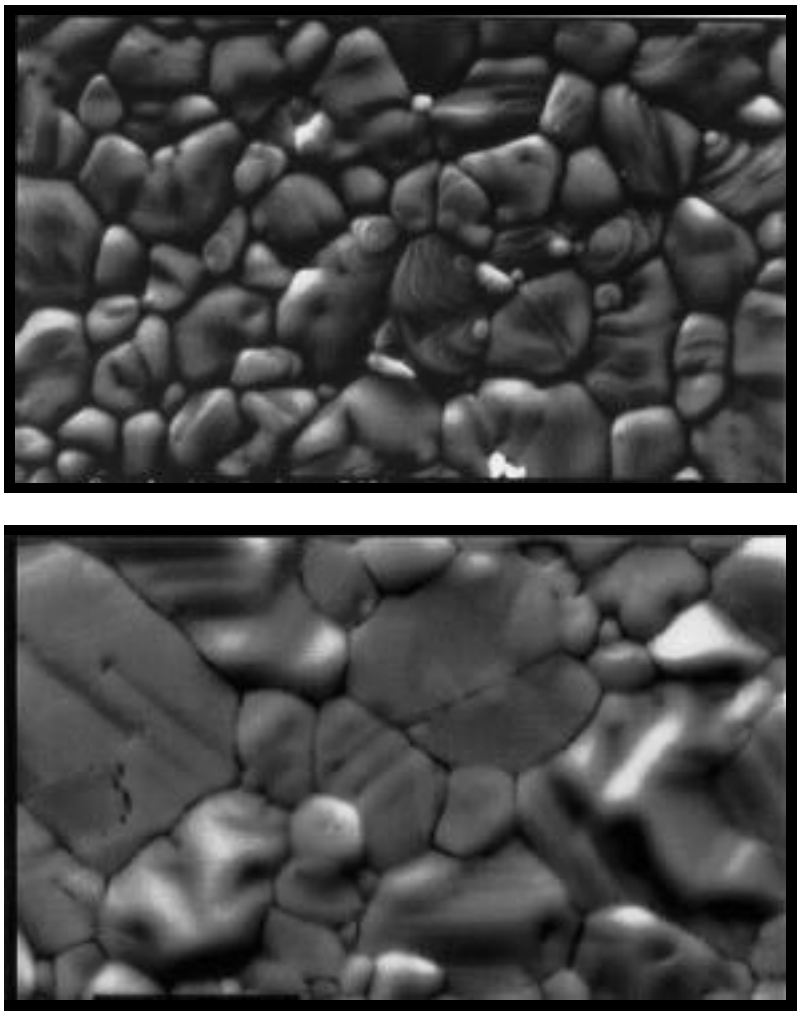


Figure 4.34 SEM photographs of $CdCl_2$ treated CdTe/CdS – no anneal (top) and HTA (bottom) prior to $CdCl_2$ treatment.

The effect of the anneal step is also demonstrated by the XRD line profiles of CdTe/CdS samples with 2.5 μm thick CdTe treated with $CdCl_2$ vapor and treated with a 580°C anneal for 10 minutes prior to $CdCl_2$ vapor treatment (Figure 4.35). The lateral grain size doubled

after the anneal; after $CdCl_2$ treatment the grain size increased to the usual value of ~ 3 μm (aspect ratio of ~1). The XRD line profile is a sharp, instrumentally-limited profile with a very small tail, corresponding to an equivalent CdS thickness of less than 10 nm. The sample which received no anneal exhibits a broad asymmetrical profile which corresponds to an equivalent CdS thickness of 100 nm. TEM cross-section micrographs of $CdCl_2$ treated samples with and without an anneal are shown in Figure 4.36; the annealed sample exhibits a dense, uniform CdS layer after processing whereas the sample receiving $CdCl_2$ treatment only exhibits a discontinuous CdS layer after processing plus residual crystallographic defects in the absorber layer.

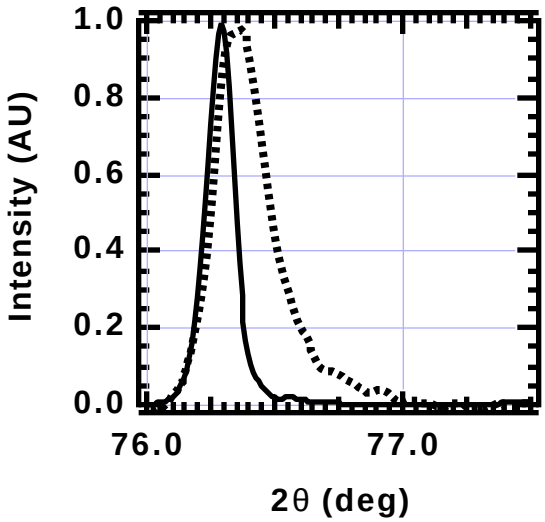


Figure 4.35 XRD (511) line profile of 2.5 μm CdTe/0.2 μm CdS after $CdCl_2$ vapor treatment (dotted) and after anneal in argon at 580˚C for 10 minutes followed by $CdCl_2$ treatment (solid).

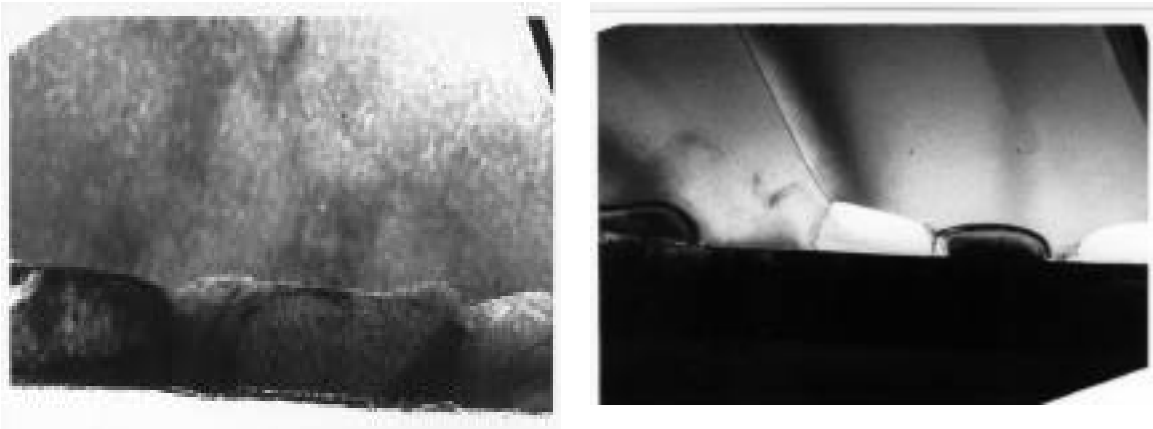


Figure 4.36 Cross-sectional TEM images of CdTe-CdS interface region on $CdCl_2$-treated samples with anneal (left) and without anneal (right) prior to chloride treatment.

The effect of changes in post-deposition processing on the change in CdS thickness and on the device J-V behavior is shown in Table 4.16. The samples were chosen to represent the initial CdS thickness at which a drop in V_{oc} has been observed for PVD samples processed with standard $CdCl_2$ treatment. Use of the anneal step reduced the CdS loss by 2X and yielded higher V_{oc} and FF for the final CdS thicknesses shown. Devices with V_{oc} > 850 mV and conversion efficiencies of PVD devices greater than 12% have been fabricated using this treatment method. This data suggests that the explanation of the differences in performance between devices made by high temperature and low temperature processes lies in the density of the CdS layer and residual defects in the absorber layer which are not completely removed by $CdCl_2$ treatment.

Table 4.16 CdS thickness from optical and QE data and device parameters for different heat treatments.

Method	Initial d(CdS) (nm)	Final d(CdS) (nm)	Δd(CdS) (nm)	V_{oc} (mV)	J_{sc} (mA/cm^2)	FF (%)
$CdCl_2$ Only	180	100	80	775	22.9	67.0
Anneal + $CdCl_2$	180	150	30	795	21.0	70.0
$CdCl_2$ Only	160	90	70	690	21.4	50.8
Anneal + $CdCl_2$	160	140	40	790	20.6	70.6
Anneal + $CdCl_2$	130	115	15	705	21.5	57.9

Given that CdS diffusion into the absorber layer of CdTe-based superstrate thin-film solar cells is a limiting factor for fabrication control and device performance, it has been shown that CdS loss can be reduced by depositing absorber layers having CdS content near the solubility limit for the processing temperatures used or by reducing diffusion pathways in the absorber layer by using a recrystallization step prior to $CdCl_2$ treatment. Use of denser CdS layer or of a densification step, combined with these techniques is expected to further extend control over the CdS diffusion and improve device performance with ultra-thin as-deposited CdS layers in PVD devices. Use of alternative TCO superstrate structures, having a high resistivity layer in contact with CdS, may offer control of junction properties if parallel diodes exist between CdTe/CdS and CdTe/TCO.

The results of this work can be readily summarized:

- Primary device junction is $CdTe_{1-x}S_x/CdS_{1-y}Te_y$.
- Te-S distribution is non-homogeneous in absorber layer.
- CdS loss via interdiffusion is a performance-controlling mechanism in superstrate CdTe/CdS devices, especially for:

  Fabrication processes having diffusion-enhancing properties (high chloride concentration during deposition, sub-micron grains, etc);

  CdTe/TCO junctions exhibiting high J_O.

- CdS-CdTe interdiffusion is reduced by:

$CdTe_{1-x}S_x$ alloy absorber layer (minimize chemical driving force);

Thermal history (minimize grain boundary volume).

· Role of TCO/Absorber junction ==> Alternative TCO.

4.3.4 Influence of TCO

The parallel diode representation of the CdTe/CdS/TCO devices discussed in Section 4.3.1 leads to the conclusion that a sufficient density of spatial discontinuities in the CdS layer will result in a significant fraction of device area comprised of CdTe/TCO junctions. For CdTe/ITO, the junction is characterized a diode current, J_o, one to two orders of magnitude higher than that measured for CdTe/CdS junctions. Obviously, one approach is to minimize extrinsic discontinuities such as pinholes in as-deposited CdS films. In this phase of the contract, pinholes were characterized and techniques were established to select or eliminate CdS/ITO/glass structures for CdTe depositions (see Section 4.3.1 above). In Section 4.3.3, it was further shown by TEM that the non-uniform depletion of CdS during post-deposition chloride treatment can be minimized by use of an anneal at T > 550°C.

Another approach, however, assuming that CdTe/TCO junctions always exist in devices when d(CdS) is less than 100 nm, is improvement of the CdTe/TCO junction itself. Without a specific junction model for CdTe/TCO, however, it is difficult to suggest *a priori* how to improve the junction, i.e., reduce J_o. It is also unclear that the CdTe/TCO junction will behave similarly to a CdTe/TCO junction in which a trace quantity of CdS was present prior to treatment. The work of Golden Photon provided an existence proof for devices in which the CdS layer was completely consumed. According to a patent on spray processed devices, a low conductivity tin oxide layer is formed on top of the current-carrying high conductivity tin oxide layer [171]. Such devices exhibit high J_{sc} and V_{oc}, yet the quantum efficiency indicates no detectable CdS layer remaining.

As part of the activity of the CdTe Team, several experiments were conducted to explore the effect of alternative TCO's: 1) Use TiO_2/SnO_2; TiO_2 has an optical bandgap of 3 eV, and 2) use TCO's over-coated with low conductivity layers. Specifically, IEC fabricated cells on: a) Harvard Nb-doped TiO_2 on SnO_2 made at the University of South Florida (USF); b) USF, SnO_2; and c) bi-layer SnO_2 made by Golden Photon, Inc (GPI).

TiO_2/SnO_2/Glass was rinsed with methanol and dried with flowing argon prior to CdS deposition. Target figures for CdS thickness were 20 nm and 150 nm. CdS films were $CdCl_2$ vapor treated prior to CdTe deposition. CdTe was deposited 5 µm thick. All structures received high temperature anneal (600°C for 15 minutes) followed by $CdCl_2$ vapor treatment. Diffused copper plus etch process with graphite paste contacts were used to make contact to the devices. J-V tests with forward and reverse voltage sweep were made with xenon simulator at AM 1.5 conditions at 25°C. The best cell obtained for each case is shown in Table 4.17.

Table 4.17 Device fabrication conditions and J-V results using alternative TCO.

Sample	TCO	d_i(CdS) (nm)	V_{oc} (mV)	J_{sc} (mA/cm^2)	FF (%)	R_{oc} (Ω-cm^2)	G_{sc} (mS/cm^2)
984.21	TiO_2/SnO_2	160	751	22	61	6	2
984.11	TiO_2/SnO_2	30	364	23	42	7	9
985.13	TiO_2/SnO_2	0	563	23	49	7	5
984.12	SnO_2	30	392	24	50	4	5

The TiO_2 had little effect on the performance of the PVD cells. The best cells were obtained on the piece with the thickest CdS, as found for SnO_2 or ITO TCO's. The voltage of the devices with *no* CdS was surprisingly high and may be an effect of the TCO not experiencing the $CdCl_2$ vapor treatment. In a subsequent experiment with niobium-doped TiO_2 films, the CdTe deposition incurred a substrate control thermocouple failure which resulted in only 3 µm film thickness. Also, the samples were plagued by delamination during $CdCl_2$ treatment. Thus, the comparative aspect of the doped TiO_2 experiment to baseline results was not possible. In spite of these problems, devices were completed and tested. The significant result of this sample set was blocking forward bias J-V characteristic not seen on the previous set with TiO_2 (40984 - presented above). The second set, which reached a much higher deposition temperature than set 40984, exhibits the same blocking characteristic near V_{oc} as found by the other team members, suggesting an influence of the CdTe deposition temperature on the interaction between the TiO_2 and the CdS/CdTe. Linear forward bias behavior has only been obtained on samples having the CdTe deposited at ~250°C. Aside from the blocking characteristic, which does not occur on samples with ITO or bare SnO_2, no other systematic difference in performance was found for this sample set.

4.3.5 Conclusion

For the GPI superstrates, encouraging results were obtained with respect to V_{oc}. The J-V data showed substantial V_{oc} gains for the ultra-thin CdS compared to any other PVD devices that have been made with such thin CdS on single layer ITO/7059, SnO_2/7059, or SnO_2/SL glass (Figure 4.32). As a reference, the best previous device we have made with *ultra-thin* evaporated CdS (d ~ 50 nm) utilized a $CdTe_{0.95}S_{0.05}$ alloy absorber layer and gave: V_{oc} = 623 mV; J_{sc} = 24.0 mA/cm^2; FF = 61.2%; for Eff = 9.1%. The cells in the present experiment have CdTe absorber layers, which with ITO typically yields V_{oc} no greater than 400 mV for d(CdS) ~ 50 nm. The present devices yield: V_{oc} = 715 mV; J_{sc} = 24 mA/cm^2; FF = 65%; for Eff = 11.1%. Thus, the properties of the GPI SnO_2 bilayer are well-suited for the PVD process. Additional samples with the GPI SnO_2 and with bi-layer ITO will be processed in 1998 and will be electrically characterized.

4.4 CdTe Contacting in Device Structures

4.4.1 Introduction

The most delicate feature of the CdTe/CdS device is believed to be the low loss back contact. Low resistance contacting methods typically involve use of Te-rich interfaces or p-type semiconductors such as HgTe or ZnTe, or thin layers including small amounts of Cu. Some devices subjected to stress testing or life testing display high series resistance and/or

evidence of a reverse diode, both characteristics which could be attributed to the back contact. What will be presented is an attempt to summarize and construct a simple working hypothesis of the important points gleaned from the stress tests and measurements done at IEC. Some of the details of these tests and measurements have been previously published [172 & 173].

4.4.2 Physio-chemical Analysis of Contact Operation

Forming low resistance Ohmic electrical contacts to p-type CdTe can be accomplished by many techniques [152]. For single crystals of CdTe, the CdTe conductivity and the work function of the contact material are critical, and for crystals with sufficient conductivity, doped to $> 10^{14}$ cm^{-3}, high work function materials such as gold and carbon are effective. For polycrystalline thin-films, however, the physical and chemical state of the grain and intergranular surface are substantially different from single crystal cases. For example, in thin-film devices, obtaining high internal quantum efficiency requires various treatments with oxygen and halogens to establish appropriate junction properties. Thus, while the interior of a given grain may be sufficiently p-doped, its surface may be composed of a complicated structure of oxides and halides. It is even possible that the reaction chemistry between the film and ambient (halogen-oxygen) treatment could produce Cd excess at the back surface, reducing p-type conductivity. Also, enhanced p-type doping along grain boundaries (normal to the CdS-CdTe interface) is required to minimize minority carrier recombination for carriers generated outside the space-charge region [137].

It is therefore necessary to "undo" the surface condition brought about by the junction-forming treatments to permit formation of Ohmic contacts. Over the past decade, IEC has employed a copper diffusion step to dope along grain boundaries, coupled with one or more etch steps to remove excess Cd, produce Te excess, and remove excess Cu metal [152]. This year, the crystalline phase composition of the surface of CdTe was measured in working devices, revealing the presence of Cu_2Te (Figure 4.37). Thus, the chemistry of the steps used to form contacts to CdTe can be written:

$$CdTe + Br_2 \Longrightarrow Te + CdBr_2 \quad (\Delta G_{rxn} = -48 \text{ kcal/mol}) \qquad (4.9)$$

$$CdTe + 2\,Cu + Br_2 \Longrightarrow Cu_2Te + CdBr_2 \quad (\Delta G_{rxn} = -59 \text{ kcal/mol}) \qquad (4.10)$$

Note that the reaction product $CdBr_2$ is soluble in methanol. If the etch is performed prior to Cu deposition, the reaction to form Cu_2Te is spontaneous:

$$Te + 2\,Cu \Longrightarrow Cu_2Te \quad (\Delta G_{rxn} = -12 \text{ kcal/mol}) \qquad (4.11)$$

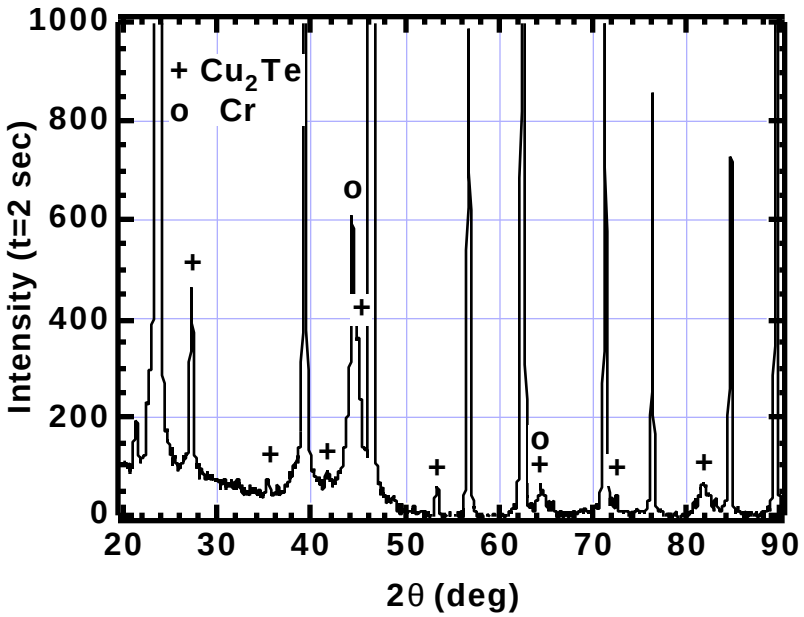


Figure 4.37 Glancing incidence (4˚) x-ray diffraction pattern of CdTe device through thin chromium metal contact showing Cu_2Te phase.

Signatory electrical characteristics which are encountered, such as forward bias curvature, light-to-dark crossover, and high series resistance (R_{oc} > 8 ohm-cm^2), are indicative of a combination of insufficient p-type doping or existence of a blocking primary contact to CdTe. By using a brief etch in hydrazine prior to Cu deposition, substantially more Te excess is formed, resulting in a more tolerant process. Recent cell results for CdTe/CdS and CdTeS/CdS junctions obtained using hydrazine etch are listed in Table 4.18. Also listed are results for a representative cell fabricated with CdTe/CdS from Solar Cells, Inc. and contacted at IEC using the same process with carbon conductor.

Table 4.18 Device fabrication steps and J-V results for cells with hydrazine etch prior to copper deposition.

Sample	Absorber	d (CdS) (μm)	High Temp Step	V_{oc} (mV)	J_{sc} (mA/cm^2)	FF (%)	Eff (%)	R_{oc} (Ω-cm^2)
929.21	CdTe	0.19	Y	789	21.7	70.6	12.1	3.8
978.22	CdTe	0.20	Y	795	21.5	68.4	11.7	3.8
934.11	$CdTe_{0.96}S_{0.04}$	0.25	Y	760	20.7	60.3	9.5	5.1
948.231	$CdTe_{0.94}S_{0.06}$	0.18	N	710	19.0	65.5	8.8	5.5
2D3.3	SCI	~0.24	Y	821	19.7	73.2	11.8	4.3

As the R_{oc} and FF values show, the contact process is moderately well-optimized for structures with CdTe and CdTeS and for CdTe/CdS from SCI. The devices exhibited no J-V retrace hysteresis and no crossover between dark and light traces.

4.4.3 Electronic Analysis of Contact Operation

We have found that most of the changes in the J-V characteristic due to stress conditions can be divided into two broad categories: (1) a "blocking contact," "rollover" or "leaky diode" appears in the J-V behavior in forward current bias (we define this as the occurrence of a minimum in the dV/dJ characteristic for J > 0); (2) an overall "shift" of the J-V characteristic to a lower voltage (this usually becomes apparent in a log J vs. V plot) which can also be accompanied by an increase in series resistance (in the illuminated J-V characteristic this results in a change in V_{oc} and in FF with little or no change in J_{sc}); and (3) both changes occur together.

Analysis of contacts to CdTe in working devices was carried out to elucidate the nature of "blocking contact" behavior which onsets at low temperature and which develops after stressing of cells at open circuit at 100°C. The J-V testing of unstressed cells was carried by varying the testing temperature to determine the activation energy of the blocking behavior and by varying the illumination intensity to separate out the photoconductive effects in the CdTe. To do these analyses, a simple equivalent circuit model incorporating a back diode was used, and the corresponding current equations were solved to separate the contact resistance. Results for a baseline cell completed using wet contact chemistry show: linear V_{oc} versus T (J = 0 bias point not affected by contact); V_{oc} at 0 K = 1.43 Volt; and activation energy for series resistance of 0.3 eV as shown in Figure 4.38 and Figure 4.39.

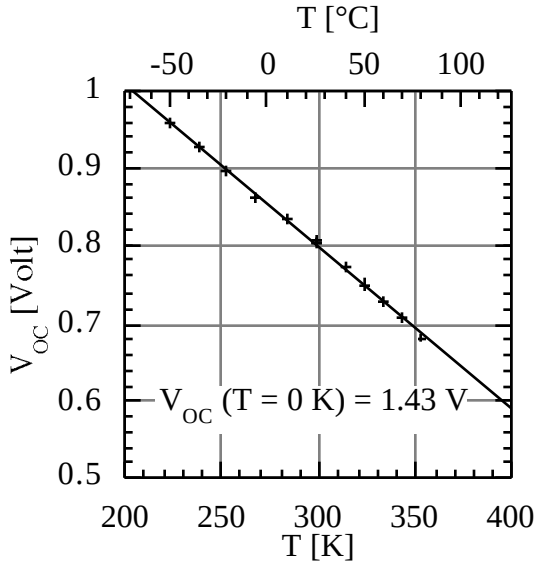


Figure 4.38 V_{oc} vs T for device #40929-21-5 at AM1.5G.

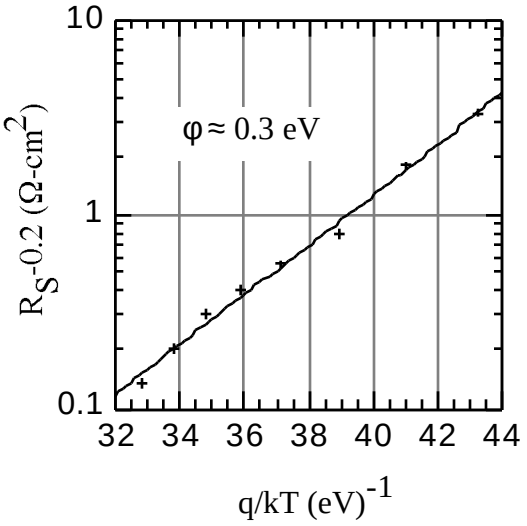


Figure 4.39 Series resistance versus 1/T for the same device shown in Figure 4.38.

4.4.4 Stress Testing and Analysis

Cells completed with IEC contacts on CdS/CdTe by Solar Cells, Inc. were stressed at Colorado State University (100°C, 2 suns, 6 weeks) and were returned to IEC. The before and after stressing J-V behavior is shown in Figure 4.40 and Figure 4.41.

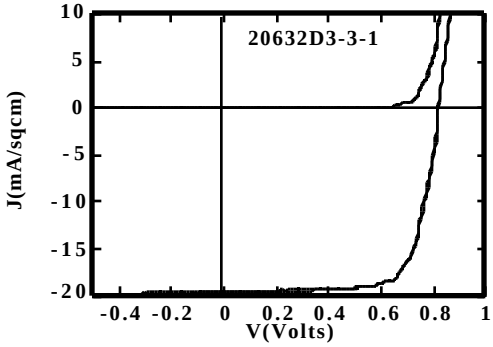


Figure 4.40 J-V behavior of SCI cell with IEC carbon contact before stressing.

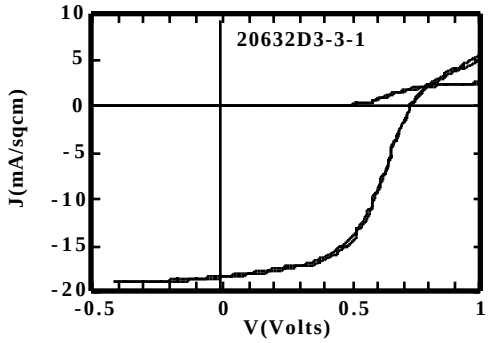


Figure 4.41 J-V behavior of same cell after stress at 100˚C, 2 suns, 6 weeks @ V_{oc}.

These cells then had their contacts removed and re-applied to help separate the location in the structure of whatever effect is responsible for the change in J-V behavior.

After being returned to IEC, one device was recontacted by lifting off the original carbon contact, re-etching the surface in 0.01% bromine-methanol for 2 seconds, and reapplying the carbon contact. The J-V data are shown in Table 4.19 and Figure 4.42 for the initial, stressed, and recontacted conditions.

Table 4.19 Device results for device # SSI 20632D3-3-1.

	Eff (%)	FF (%)	V_{OC} (Volts)	J_{SC} (mA/cm^2)	R_{OC} (Ω-cm^2)	G_{SC} (mS/cm^2)	Test Date
Initial	11.79	73.3	0.8192	19.65	4.4	0.0 Dark 0.4 AM1	Feb 28
After Stress @ CSU (100˚C, 2 suns, 6 weeks, V_{OC})	7.17	53.6	0.7273	18.39	20.2	0.0 Dark 2.4 AM1	Nov 12
Contacts Removed & Reapplied	9.08	62.2	0.7308	19.98	4.7	0.0 Dark 1.2 AM1	Nov 20

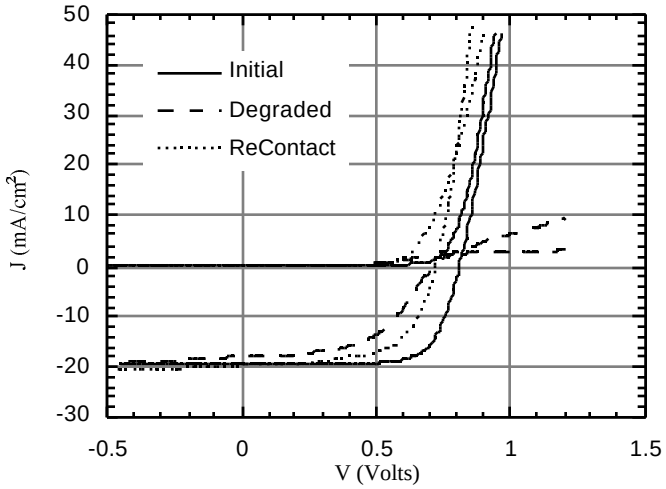


Figure 4.42 Summarized J-V behavior of device # SSI 20632D3-3-1.

The initial dark I-V characteristic of the device can be represented by a simple diode and resistor

$$J = J_0 \exp[(V-R_sJ)/V_0] \qquad (4.12)$$

and is shown in Figure 4.43 and Figure 4.44. After degradation the dark I-V exhibits a "blocking contact" behavior with a diode behavior similar to before degradation (Figure 4.44). The results of the model fit are shown separately in Table 4.20. After the previous C contact lifted, CdTe etch and new C contact applied, the dark I-V "blocking contact" behavior is reduced but the main diode behavior is unchanged (Figure 4.44).

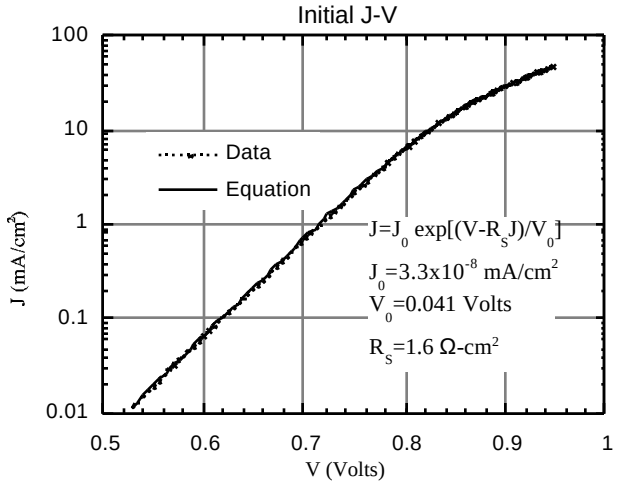


Figure 4.43 Dark J-V data and equivalent circuit fit for before degradation.

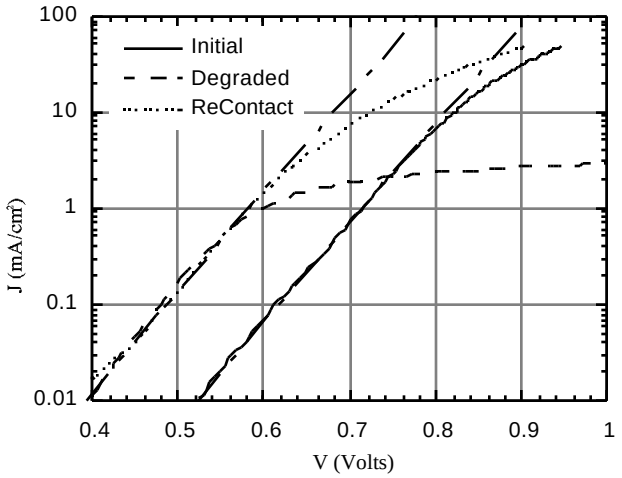


Figure 4.44 Summarized dark J-V data and equivalent circuit diode parameters.

Table 4.20 Diode parameters of the straight line fits shown in Figure 4.44.

	V_0 (Volts)	J_0 (mA/cm^2)
Initial	0.041	3.3×10^{-8}
After Stress @ CSU (100˚C, 2 suns, 6 weeks, V_{OC})	0.041	8.0×10^{-7}
Contacts Removed & Reapplied	0.041	8.0×10^{-7}

Figure 4.45 shows the J-V slope (dJ/dV) in reverse and low forward voltage of the J-V curve in the three conditions. The initial illuminated I-V behavior shows the normal "displaced" dark I-V curve with a small amount of $J_L(V)$ behavior. After degradation the illuminated I-V is dominated by the $J_L(V)$ behavior. After previous C contact lifted, CdTe etch and new C contact applied, the $J_L(V)$ behavior is essentially unchanged. This data can be interpreted as a reduction in the p-type doping of the CdTe layer by the stress condition, manifested in a lower junction voltage and development of a blocking contact. Re-contacting restores most of the contact portion of the degradation but does not affect the main junction.

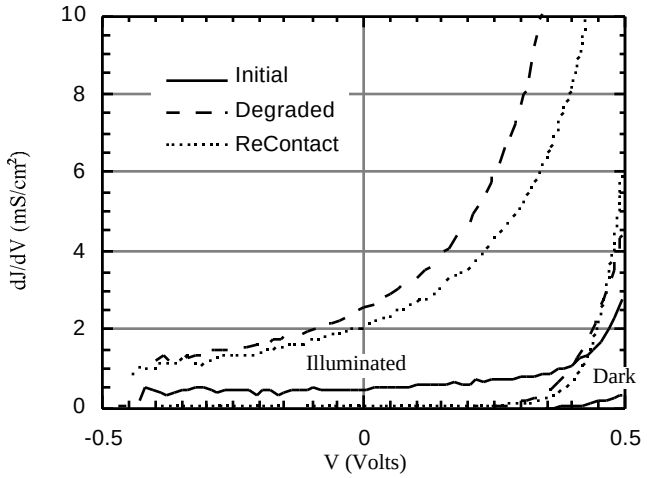


Figure 4.45 Summarized dJ/dV behavior of device # SSI 20632D3-3-1.

4.4.5 Operational Model

It is possible to look at the observations as resulting from a single mechanism. If a dopant (or compensating material) is activated by temperature and affected by an electric field (i.e., charged), it can account for the basic J-V behaviors. Under forward electrical bias it would accumulate at the contact, giving rise to the blocking contact behavior. Its concentration would also be depleted in the bulk and junction areas, thereby causing the J-V shift and increased series resistance. When reverse electrical bias is applied, it would move toward the metallurgical main junction, whose behavior is already "blocking." This would still reduce its concentration in the rest of the CdTe, giving rise to only the J-V shift and increased series resistance.

If the p-type dopant is accumulating at the contact during forward bias stress, it should be possible to remove it, and redope and recontact the device. To test this, we are exposing contacted and uncontacted material to temperatures of about 100˚C under illumination (@ V_{oc}). When the contacted material exhibits the blocking contact and J-V shift behavior, one uncontacted piece will be etched and contacted, and another will be etched, doped and recontacted. We expect to see the etched and contacted piece behave as if it were etched and recontacted (i.e., at room temperature, the blocking contact behavior disappears, but the J-V shift remains), while the etched and doped sample should appear as the normal initial I-V behavior.

5. Abstract

This report describes results achieved during phase I of a four-phase subcontract to develop and understand thin film solar cell technology associated to $CuInSe_2$ and related alloys, a-Si and its alloys and CdTe. Modules based on all these thin films are promising candidates to meet DOE long-range efficiency, reliability and manufacturing cost goals. The critical issues being addressed under this program are intended to provide the science and engineering basis for the development of viable commercial processes and to improve module performance. The generic research issues addressed are: 1) quantitative analysis of processing steps to provide information for efficient commercial scale equipment design and operation; 2) device characterization relating the device performance to materials properties and process conditions; 3) development of alloy materials with different bandgaps to allow improved device structures for stability and compatibility with module design; 4) development of improved window/heterojunction layers and contacts to improve device performance and reliability; and 5) evaluation of cell stability with respect to illumination, temperature and ambient and with respect to device structure and module encapsulation.

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Appendix 1

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DETERMINING THE VOLTAGE DEPENDENCE OF THE LIGHT GENERATED CURRENT IN $CuInSe_2$ - BASED SOLAR CELLS USING I-V MEASUREMENTS MADE AT DIFFERENT LIGHT INTENSITIES

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ABSTRACT

As the bandgap of $CuInSe_2$ is increased by alloying with Ga or S, the loss in efficiency due to the decrease of light generated current with increasing voltage becomes important. The standard technique of quantifying this loss is to analyze spectral response measurements made as a function of applied voltage. Instead, it is shown how to determine the voltage dependence of the light generated current by an analysis of the current-voltage (I-V) measurements made at two different light intensities. By adding an I-V measurement at a third light intensity one can also determine if the analysis technique is valid.

INTRODUCTION

It has been demonstrated that the loss in efficiency of $Cu(In,Ga)Se_2$ solar cells with high Ga content is due to a decrease in fill factor, and to a lesser extent V_{oc} which is caused by a drop in the light generated current with increasing forward voltage [1 and 2]. This type of loss mechanism is well known in amorphous silicon solar cells where I-V measurement and analysis techniques have been developed to determine the voltage dependence of the light generated current, $J_L(V)$, [3 and 4].

ANALYSIS

In most solar cells, it is possible to correct for parasitic resistive losses by determining (eq. 1 & 3) and subtracting (eqs. 2 & 4) small shunt, R_{shunt}, and series resistance ,R_{series}, terms from the measured J and V respectively.

$$1/R_{shunt} = G_{shunt} \approx (dJ/dV)_{min.} \quad (1)$$

$$J' = J - V/R_{shunt} \quad (2)$$

$$R_{series} \approx \lim_{1/J \to 0} (dV/dJ) \quad (3)$$

$$V' = V - JR_{series} \quad (4)$$

Which then gives the junction current, $J_J(V')$, and the voltage dependent light generated current, $J_L(V')$, (eq. 5). If $J_J(V')$ is independent of light intensity and $J_L(V')$ is proportional to the light intensity, $J_L(V')$ can be found by subtracting the J-V data measured at two different light intensities (1 &2) with the same spectral content (eq. 6).

$$J'(V') = J_J(V') - J_L(V') = J_J(V') - \eta(V')J_{L_{max}} \quad (5)$$

$$J_{21}(V') \equiv J'_2(V') - J'_1(V') = \eta(V')\left[J_{L1_{max}} - J_{L2_{max}}\right] \quad (6)$$

It is then possible to determine if the assumptions are correct by taking the difference between more than two light intensities and comparing the results. i.e.

$$\eta(V') = \left[J_{21}(V')\right] / J_{21}(V')_{max.} \quad (7)$$

and:

$$\eta(V') = \left[J_{31}(V')\right] / J_{31}(V')_{max.} \quad (8)$$

EXPERIMENTAL PROCEDURE

J-V measurements were made on $Cu(In,Ga)Se_2$ solar cells at four different light intensities: (1) full AM1.5 Global normalized to 100 mW/cm^2, (2) ~90% AM1.5, (3) ~10% AM1.5 and (4) dark (Figure 1). The reduced light intensities were achieved using neutral density screens. Two high light intensities (full & ~90%) and two low light intensities (~10% & dark) were chosen to give accurate comparisons when subtracting the J'-V' data. R_{shunt} was determined from finding the minimum dJ/dV ,usually from the dark data, in reverse voltage bias (Figure 2). R_{series}

was found from the intercept of dV/dJ vs. 1/J (Figure 3). The lower light intensities, ~10% and dark, are used to in the R_{series} determination in order to reduce interference from $J_L(V)$ effects. Figure 4 shows the dark J-V data with and without corrections for the parasitic resistance losses (eqs. 2 & 4). After correcting all the data for these losses, the high intensity J'-V' data were subtracted from the low intensity data (eqs. 5 & 6). The normalized results of this subtraction are shown in Figure 5. As can be seen from Figure 5, except for high forward voltage bias, the different subtractions are basically identical. This shows that the assumptions that $J_J(V')$ is independent of light intensity and $J_L(V')$ is proportional to the light intensity are valid. Finally, Figure 6 compares the full intensity J-V data assuming that $J_L(V)$ was independent of voltage i.e. $J_L(V)=J_L(V)max$.

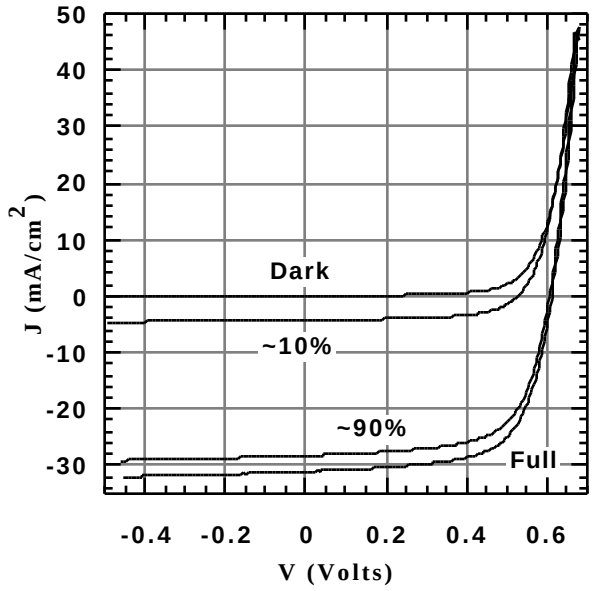

Figure 1 J-V measurements for a $Cu(In,Ga)Se_2$ solar cell measured at various light intensities under an AM1.5Global spectrum (the J-V parameters for this device are underlined and bolded in Table 1).

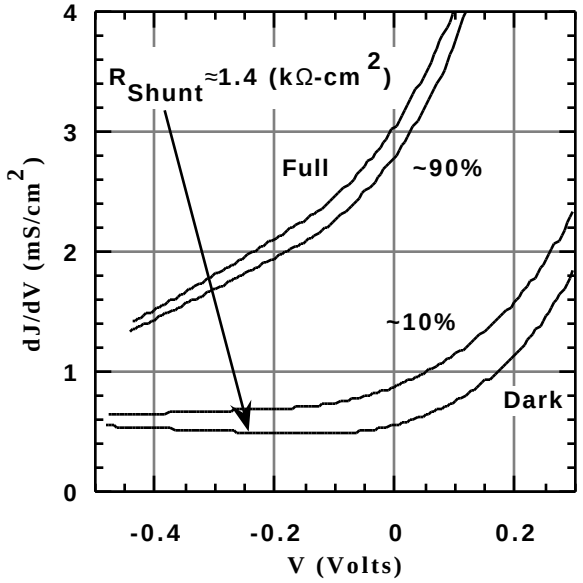

Figure 2 dJ/dV data for the solar cell shown in Figure 1

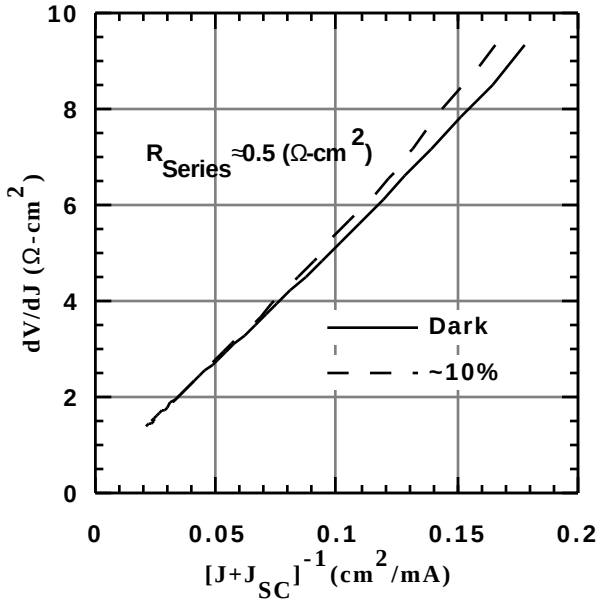

Figure 3 dV/dJ data for the solar cell shown in Figure 1

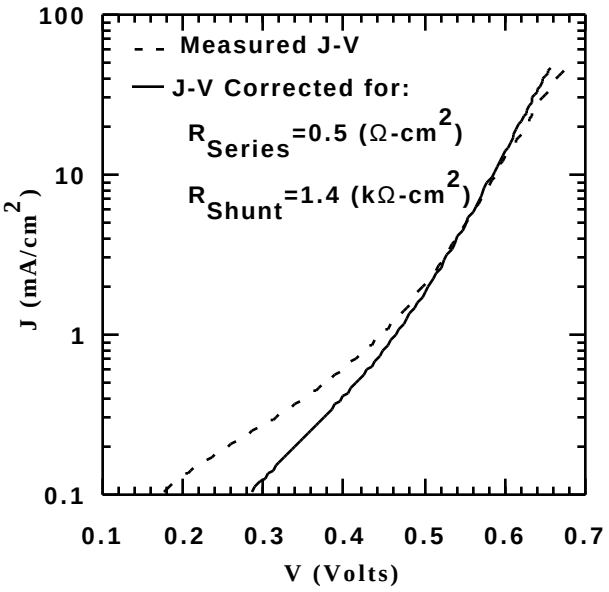

Figure 4 Dark J-V data, with and without resistance corrections data for the solar cell shown in Figure 1.

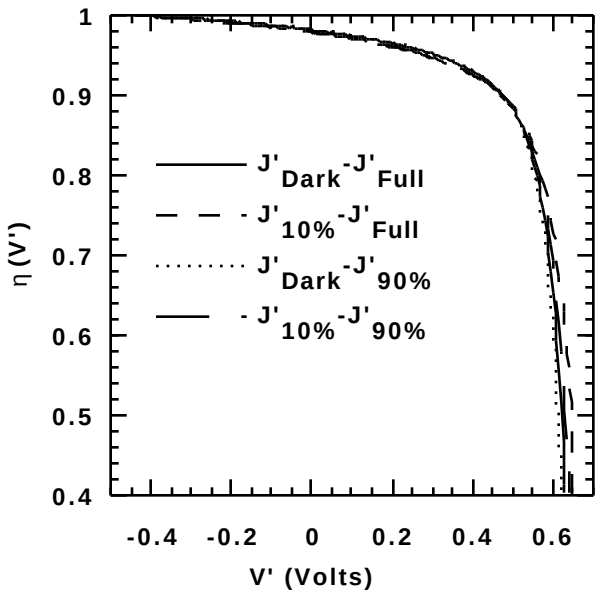

Figure 5 Normalized $J_L(V')$ data for the solar cell shown in Figure 1

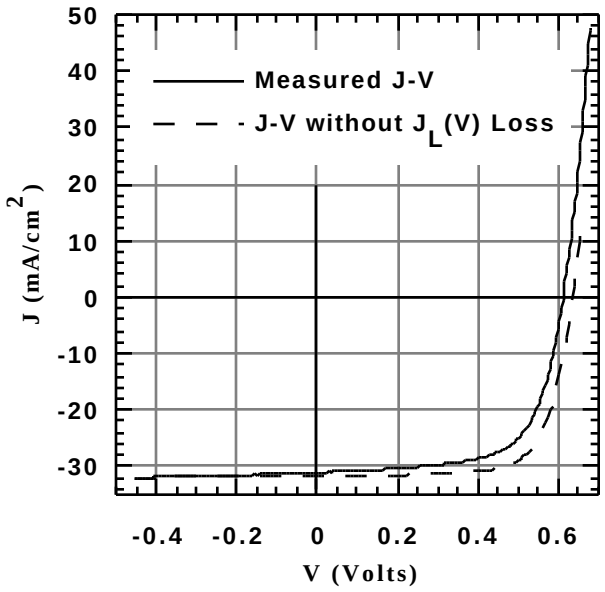

Figure 6 J-V data, with and without $J_L(V)$ losses, for the solar cell shown in (the J-V parameters for this device are underlined and bolded in Table 1).

RESULTS AND CONCLUSIONS

Table 1 shows the results of the previously described measurements and analysis when applied to various $Cu(In_{1-X}Ga_X)Se_2$ solar cells. The solar cells used for this analysis were chosen from two categories: (1) moderate Ga content (X≈0.3) and fairly high efficiency and (2) high Ga content (X=0.5 –> 0.7) and high V_{oc}. As can be seen from this table, the $J_L(V)$ losses, which varies from cell to cell, primarily affects FF and V_{oc} and hence Eff. However, unlike the best devices examined in references 1 and 2, these $J_L(V)$ losses do not obviously increase with increasing Ga content.

It can be concluded that, by taking J-V measurements at least three different light intensities, one can determine if it is correct to analyze these data for $J_L(V)$ losses and, if correct, what the magnitude of these losses are.

ACKNOWLEDGEMENTS

The authors would like to thank J. Laker and the technical staff of the Institute of Energy Conversion. This work was supported by the National Renewable Energy Laboratory under subcontract #XAK-7-17609-01.

Measured at AM1.5 Global @100mw/cm^2 T = 30 deg. C; Area = 0.13 cm^2				Derived Series and Shunt Resistances		Calculated AM1.5 Global J-V parameters without $J_L(V)$ loss i.e. $J_L = J_L(V)max.$			
Eff (%)	V_{oc} (Volts)	FF (%)	J_{sc} (mA/cm^2)	R_{series} (Ω-cm^2)	R_{shunt} (kΩ-cm^2	Eff (%)	V_{oc} (Volts)	FF (%)	J_{sc} (mA/cm^2)
High Efficiency $Cu(In_{1-X}Ga_X)Se_2$ X≈0.3									
13.9	0.606	68.8	33.2	0.2	1.7	15.1	0.635	71.0	33.5
13.6	0.631	72.1	29.8	0.1	2.5	14.2	0.644	73.6	30.0
12.8	0.583	67.8	32.4	0.0	0.7	13.7	0.607	69.4	32.6
12.8	0.605	68.2	31.0	0.0	1.7	13.5	0.626	69.3	31.1
12.6	**0.612**	**66.2**	**31.1**	**0.5**	**1.4**	**14.5**	**0.637**	**71.9**	**31.7**
12.5	0.596	63.9	32.9	0.4	1.1	14.6	0.621	70.3	33.3
High Voltage $Cu(In_{1-X}Ga_X)Se_2$ X = 0.5 –> 0.7									
7.9	0.764	60.4	17.0	0.0	5.0	10.0	0.792	71.2	17.7
6.9	0.734	61.6	15.3	0.4	2.0	9.4	0.760	76.2	16.2
10.1	0.732	74.4	18.5	0.0	5.0	10.6	0.736	76.6	18.8

Table 1 J-V parameters for various $Cu(In,Ga)Se_2$ devices measured and analyzed (see text). Note: The bolded and underlined device parameters are for the example used in figures 1 - 6.

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Appendix 2

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EFFECT OF REDUCED DEPOSITION TEMPERATURE, TIME, AND THICKNESS ON $Cu(InGa)Se_2$ FILMS AND DEVICES

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ABSTRACT

This paper will address the ability to reduce process costs for multisource evaporation of $Cu(InGa)Se_2$ by reducing the deposition temperature and film thickness and increasing the deposition rate. Substrate temperature (T_{ss}) is varied from $600 \geq T_{ss} \geq 350$°C using fixed elemental fluxes. The grain size decreases over the entire range but Na incorporation from the soda lime glass substrate doesn't change. Solar cell efficiency decreases slowly for $550 \geq T_{ss} \geq 400$°C. At T_{ss} below 400°C there is a change in composition attributed to a change in the re-evaporation of In and Ga species in the growing film. Device performance is shown to be unaffected by reducing the film thickness from 2.5 to less than 1.5 µm. Finally, a kinetic reaction model is presented for the growth of $CuInSe_2$ by multisource elemental evaporation which provides quantitative predictions of the time to grow $CuInSe_2$ films as a function of substrate temperature and delivery rate.

INTRODUCTION

There are many technical issues which need to be addressed to effectively enable the transfer of $Cu(InGa)Se_2$ deposition and device fabrication technology from the laboratory to manufacturing scale. In general, these issues provide means to reduce thin film semiconductor process costs. Shorter deposition time, with reduced film thickness and increased deposition rate, is a primary means to lower costs by increasing throughput and can enable reduced size of the deposition zone in an in-line process. For films deposited by multisource evaporation the deposition time will depend on the delivery rate to the substrate and the film growth rate. Understanding the effect of delivery rate and temperature on the film growth requires the quantitative knowledge of the reaction chemistry and kinetics.

Thinner absorber films reduce the total amount of material used and allow faster process throughput. The minimum thickness of the $Cu(InGa)Se_2$ absorber layer may be determined by the nucleation of the film to form a continuous layer. From a device perspective, the minimum thickness is limited by the optical absorption coefficient of the $Cu(InGa)Se_2$ or the ability to incorporate optical confinement. If the absorber layer becomes too thin, so that the minority carrier diffusion length becomes comparable to the thickness, then V_{oc} may be reduced by back surface recombination at the $Mo/Cu(InGa)Se_2$ interface.

Soda lime glass has been used as the substrate for most high efficiency $Cu(InGa)Se_2$ solar cells but often deforms at the substrate temperatures used for these devices. Additional effort and cost to control this for a large area deposition would be difficult for a manufacturing process. With lower substrate temperature (T_{ss},) alternative substrate materials, like a flexible polymer web, can be utilized. In addition, lower T_{ss} can lower processing costs by reducing thermally induced stress on the substrate, allowing faster heat-up and cool-down, and decreasing the heat load and stress on the entire deposition system.

This paper will address the need to improve process throughput by reducing the $Cu(InGa)Se_2$ thickness and increasing the deposition rate, and the effect of reducing deposition temperature. Baseline processes for $Cu(InGa)Se_2$ deposition by multisource elemental evaporation and solar cell fabrication are defined. All other deposition parameters are then held fixed to determine the effects of varying either the substrate temperature or, by changing the deposition time, film thickness. Characterization of the resulting $Cu(InGa)Se_2$ films and their device behavior will be presented. Finally, a chemical reaction model for the growth and kinetics of $CuInSe_2$ is presented to evaluate the effect of substrate temperature and delivery rate of elemental species to the substrate and to predict the minimum times to form the film.

EXPERIMENTAL PROCEDURES

$Cu(InGa)Se_2$ films were deposited by thermal evaporation from four elemental sources. Details of the deposition, film characterization, and device fabrication are described in Ref. 1. The baseline deposition process in this work is the same as described in Ref. 1 but with the T_{ss} maintained constant through the entire deposition. The films are deposited with a Cu-rich first layer, deposited in 32 min., and followed continuously by an In-Ga-Se second layer deposited in 12 min. The fluxes of Ga and In are constant through the deposition time so there is no grading of the bandgap. This results in ~2.5 µm thick films with $Ga/(In+Ga) \approx 0.3$ which gives a bandgap ~ 1.2 eV.

To study the effect of substrate temperatures, $Cu(InGa)Se_2$ films were deposited with T_{ss} from 600 to 350°C, maintaining fixed source effusion rates and deposition times. To study varying thicknesses, films were deposited with constant effusion rates and T_{ss}, and only the times adjusted.

The film thickness was determined by the mass gain after deposition and the films were characterized by scanning electron microscope (SEM) images, energy dispersive x-ray spectroscopy (EDS), x-ray diffraction (XRD). Secondary ion mass spectroscopy (SIMS) measurements were performed at NREL.

The $Cu(InGa)Se_2$ films were deposited on soda lime glass substrates with a sputtered 1 µm thick Mo layer. Complete solar cells were fabricated [1] with the chemical bath deposition of ~ 30 nm CdS followed by rf sputtered ZnO:Al with thickness 0.5 µm and sheet resistance 20 Ω/sq. A Ni/Al grid and 125 nm MgF_2 anti-reflection layer were deposited by electron beam evaporation. Cells were delineated by mechanical scribing to give areas ~0.5 cm^2. Devices were characterized by current-voltage (J-V) measurements at 28°C under 100 mW/cm^2 AM1.5 illumination.

RESULTS

Substrate Temperature

$Cu(InGa)Se_2$ films were deposited at varying T_{ss} with fixed effusion rates that were determined to give films of composition Cu/(In+Ga) ≈ 0.9 and Ga/(In+Ga) ≈ 0.3 when T_{ss} = 600°C. This required the total concentration of metals to be delivered to the substrate with ratios Cu/(In+Ga) ≈ 0.6 and Ga/(In+Ga) ≈ 0.3. The difference in the relative Cu and In compositions can be attributed to the re-evaporation of In and Ga from the surface of the growing film. The In and Ga form volatile intermediate binary species while no volatile Cu-Se species are formed [2]. The compositions of films deposited with T_{ss} varying from 600 to 350°C are plotted in Fig. 1. The composition is independent of T_{ss} except for T_{ss} ≤ 400°C when the ratio Cu/(In+Ga) decreases. At T_{ss} = 350°C, the Cu/(In+Ga) ratio is comparable to that delivered to the substrate during growth. The relative Ga content of the films remains unchanged which suggests that films lose Ga and In at similar rates. The temperature dependence of the composition will, in general, depend on Cu/(In+Ga) flux ratio [3] and the Se flux.

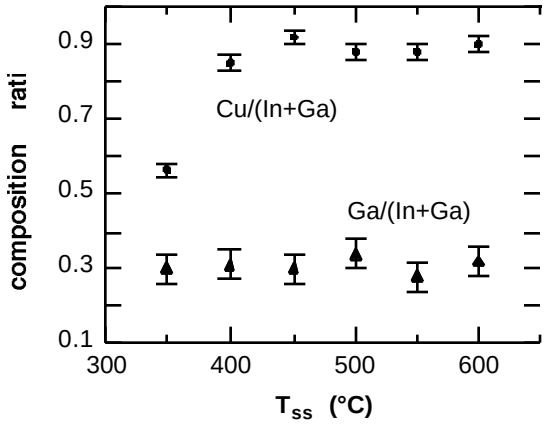

Fig. 1. The T_{ss} dependence of the composition ratios Cu/(In+Ga) and Ga/(In+Ga).

SEM micrographs show that the grain structure of the $Cu(InGa)Se_2$ films changes dramatically as T_{ss} changes. The cross sectional micrographs in Fig. 2 show columnar grains at T_{ss} = 600°C with typical grain size 1.5 - 2 µm. But the grains become smaller as T_{ss} decreases and for T_{ss} ≤ 450°C it appears that single grains do not grow continuously from the Mo to the top surface. In this case, current in a working device clearly would need to cross several grain boundaries. XRD measurements did not reveal any significant differences in the film orientation or compositional distribution at different substrate temperatures. There is no peak broadening, indicating that the grain size at the lowest T_{ss} is still greater than ~ 300 nm.

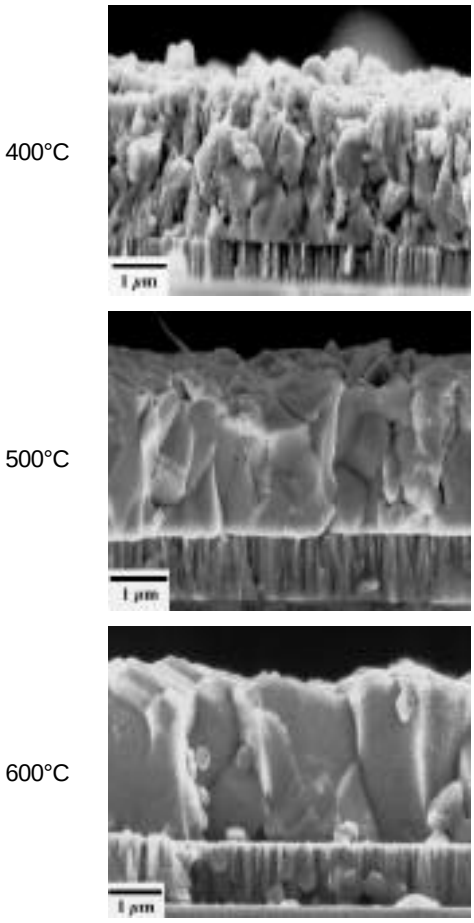

Fig. 2. Cross-sectional micrographs of $Cu(InGa)Se_2$ films deposited at different T_{ss}.

While the film deposited at T_{ss} = 600°C has the largest grains, the soda lime glass in this case is well above its softening point during the deposition which resulted in a curved substrate.

$Cu(InGa)Se_2$ have been shown to contain significant levels of Na impurities when deposited on soda lime glass substrates [4]. The Na is incorporated into the $Cu(InGa)Se_2$ by diffusion and is therefore expected to be temperature dependent. Depth profiles of the Na content measured by SIMS are shown at different T_{ss} in Fig. 3. The Cu and Mo levels for T_{ss} = 500°C are shown for reference to indicate the position of the $Cu(InGa)Se_2$/Mo interface. The

Na level varies by relatively little from 400 to 600°C and is actually highest for the lowest T_{ss}, though diffusion of Na is expected to increase with increasing T_{ss}. This can be explained by Na diffusion along grain boundaries since there is a greater grain boundary density at the lower temperature.

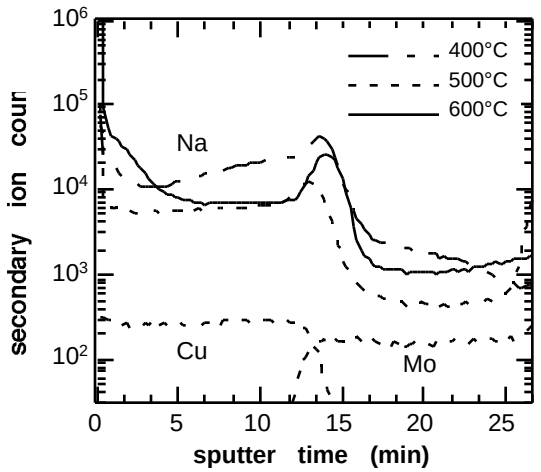

Fig. 3. SIMS profiles showing the Na content of $Cu(InGa)Se_2$ films deposited at different T_{ss}.

Finally, solar cells were fabricated with films deposited at varying T_{ss} and the J-V parameters are listed in Table 1. The efficiency (η) decreases slowly as T_{ss} decreases from 550°C, but is still 12.8% at 400°C. While there is some tradeoff in V_{oc} and J_{sc} which may be associated with variations in the Ga content and, therefore, bandgap of the $Cu(InGa)Se_2$, the biggest change is the fill factor. With T_{ss} = 350°C the $Cu(InGa)Se_2$ films with Cu/(In+Ga) ≈ 0.6 had η = 7.0%, but a film deposited with the Cu effusion rate adjusted to give Cu/(In+Ga) ≈ 0.9 gave η = 10.9%.

Thickness

Using the same effusion rates as above, the effect of thickness has been studied by changing the deposition times with T_{ss} = 450°C to give films with thickness (d) ranging from 2.5 to 1.0 µm. The composition of these films was unchanged over the thickness range with all films having Cu/(In+Ga) ≈ 0.9 and Ga/(In+Ga) ≈ 0.3 and again, no difference in orientation or compositional distribution was observed by XRD.

Table 1. J-V parameters with varying substrate temperature.

T_{ss} (°C)	V_{oc} (mV)	J_{sc} (mA/cm^2)	FF (%)	η (%)
600	0.596	31.2	67.4	12.5
550	0.583	34.3	71.8	14.4
500	0.606	32.5	70.0	13.8
450	0.605	32.6	68.4	13.5
400	0.606	32.5	64.8	12.8
350	0.557	23.2	54.2	7.0
350*	0.561	33.2	58.6	10.9

* Cu effusion rate adjusted to give Cu/(In+Ga) ≈ 0.9

Device results for different $Cu(InGa)Se_2$ thickness with this deposition process are shown in Table 2. With d ≥ 1.4 µm the devices have η ≈ 13%. There are no significant thickness related losses which might include effects of bulk series resistance or back surface recombination. For d = 1.0 µm, η decreases due to decreases in V_{oc}, J_{sc}, and FF. In addition, the J-V curves both in the dark and under illumination indicate an increased shunt conductance for the thinnest cells.

Table 2. J-V parameters with decreasing $Cu(InGa)Se_2$ thickness for films deposited at T_{ss} = 450°C.

d ± 0.2 (µm)	V_{oc} (mV)	J_{sc} (mA/cm^2)	FF (%)	η (%)
2.5	0.605	32.6	68.4	13.5
1.8	0.581	33.7	66.6	13.0
1.4	0.590	32.5	69.5	13.3
1.2	0.526	34.2	64.9	11.7
1.0	0.514	30.7	62.5	9.9

Growth Time

A chemical reaction analysis of the growth and kinetics of $CuInSe_2$ has been previously developed based on the species formed by the reaction of Cu/In precursors in H_2Se and Se vapor [5,6]. This required identification of the species present in the film versus time and at different reaction temperatures and quantitative determination of their concentrations by XRD and atomic absorption spectroscopy. This analysis has not been completed for the growth of $CuGaSe_2$ or $Cu(InGa)Se_2$ because of difficulty quantitatively measuring the elemental Ga and binary Ga selenide phases.

The reaction pathway leading to the formation of $CuInSe_2$ by selenization which was used to model the measured species concentrations was:

$$2\,Cu_xIn_y + (x+y)\,Se \rightarrow x\,Cu_2Se + y\,In_2Se$$
$$2\,In + Se \rightarrow In_2Se$$
$$In_2Se + Se \rightarrow 2\,InSe$$
$$2\,InSe + Cu_2Se + Se \rightarrow 2\,CuInSe_2$$

The rate constants and activation energies for each of these reactions were determined by fitting the concentrations to a detailed set of kinetic equations [6].

This analysis can be used to predict the growth of $CuInSe_2$ by three source elemental evaporation if modified to include a rate of delivery term for the elemental species. It is assumed that the reaction proceeds from elemental species, since the reaction time to form a Cu/In alloy is long, and that there is an unlimited continuous supply of Se. Finally, it is assumed there is no direct reaction of

In + Cu + 2 Se → 2 CuInSe$_2$. since there was no evidence of this reaction in analysis of the selenization experiments. These assumptions and modifications lead to the following proposed reaction pathway for the multisource evaporation:

2 Cu + Se → Cu$_2$Se
2 In + Se → In$_2$Se
In$_2$Se + Se → 2 InSe
2 InSe + Cu$_2$Se + Se → 2 CuInSe$_2$

Using the rate constants and activation energies determined previously [6], this model was used to predict the time to form $CuInSe_2$ as a function of substrate temperature and delivery rate. This has been completed for 2 cases and the results are shown in Fig. 4 at T_{ss} = 600, 500, and 400°C. Case 1 models a process similar to that described above which deposits a 2 µm thick film with the Cu delivered to the substrate in 30 min. and the In delivered in 40 min. while maintaining a constant T_{ss}. Case 2 in Fig 4. shows the theoretical limiting case when the Cu and In are delivered instantaneously at time equal to zero. An intermediate case, with the metals delivered at 5 times the rate in case 1 was also calculated and the curves (not shown) fall in between cases 1 and 2 as expected. These $CuInSe_2$ formation curves provide quantitative predictions for film growth time as a function of delivery rate and substrate temperature.

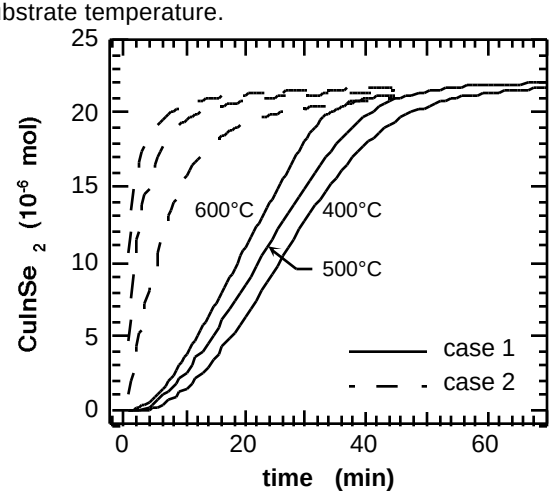

Fig. 4. Model predictions for the molar concentration of $CuInSe_2$ versus time for different T_{ss} and delivery rate (cases 1 and 2 defined in text).

DISCUSSION AND CONCLUSIONS

The $Cu(InGa)Se_2$ grain size decreases as T_{ss} decreases from 600 to 400°C but there is little change in the incorporation of Na from the glass substrate. The dependence of grain size with T_{ss} has been reported previously [7], and at high temperatures was attributed to the formation of copper selenide phases above ~525°C which act as a "flux" for grain growth in the Cu rich film [8]. However, the films in this work show an increasing grain size with increasing T_{ss} over the entire temperature range. There is only a small drop-off in device performance with lower T_{ss} despite the decreasing grain size. The ability to fabricate cells with $\eta \approx 13$ % at $T_{ss} \leq 450$°C allows flexibility in the choice of substrate materials and process design which can potentially lead to lower costs.

The absorber thickness can also be reduced to minimize materials use and deposition times. With the baseline process in this work there was no fall-off in device performance with the absorber layer thickness reduced to ~ 1.5 µm.

Increased growth rate and reduced thickness are critical means to increase throughput. Experimental verification of the effect of growth rate and time on device performance still need to be established, although, using a similar deposition process, a 13% cell efficiency with a deposition time of 10 min. was demonstrated in Ref. [9]. The kinetic reaction model presented here for $CuInSe_2$ film growth by elemental evaporation provides a quantitative prediction of the effect of T_{ss} and delivery rate on the film growth rate. This provides necessary information to design a manufacturing process and commercial scale deposition equipment. Experimental measurements of the concentrations of reaction species versus time in the growth of $CuInSe_2$ by evaporation are needed to provide the verification of the growth model and assumptions. This will require rapid substrate quenching to provide the necessary time resolution.

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Appendix 3

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IMPROVING PERFORMANCE OF SUPERSTRATE p-i-n a-Si SOLAR CELLS BY OPTIMIZATION OF n/TCO/METAL BACK CONTACTS

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ABSTRACT

A comprehensive study of the n-layer and back contact for superstrate (glass/textured SnO_2/p-i-n/TCO/metal) a-Si solar cells is presented. In particular, the difference between a-Si and µc-Si n-layers are compared. These results show that the efficiency can be improved from 7% to 10% (absolute) by optimizing the back contact layers to incorporate a good optical back reflector. A rectifying contact is formed between the TCO and a-Si n-layer which reduces FF. A µc-Si n-layer eliminates the blocking n/TCO contact. Results suggest that the n/TCO interface has a controlling influence. ZnO gives ~1 mA/cm^2 higher J_{sc} compared to ITO. The best contacts are µc-Si/ZnO/metal.

INTRODUCTION

Most a-Si solar cell research has focused on the i-layer, p-layer, and p/i and TCO/p interfaces. The n-layer and its contact has received relatively little attention. However, the n-layer and its contact can have a significant influence on performance [1,2]. We have performed a comprehensive study of the n-layer and back contact for superstrate a-Si solar cells. The goal is to determine the optimum contact having high back reflection and low absorption which is needed for high J_{sc}, along with low contact resistance which is needed for high FF. This work identifies and separates the critical roles of the n-layer conductivity, the TCO and the metal layer. As a result of this effort, we succeeded in fabricating a device having 10.4% efficiency, verified at the National Renewable Energy Laboratory (NREL), having parameters: V_{oc}=0.880 V, J_{sc}=16.2 mA/cm^2, and FF=72.7%.

DEVICE FABRICATION

Single junction a-Si solar cells were deposited in a single chamber plasma CVD system with the configuration of glass/textured SnO_2/p-b-i-n/TCO/metal. The textured SnO_2 was Asahi type U. The p and b (buffer) layers were a-SiC. There was no H_2 dilution of the p, b, or i-layers. The i-layers were 0.5 µm thick. All devices analyzed in this paper had identical p-b-i layers. The only differences were the types of n-layer, a-Si or µc-Si, and the back contacts. Film properties of the two types of n-layers are shown in Table 1. The µc-Si n-layer has a significantly lower activation energy and lower resistivity compared to the a-Si. Deposition conditions and properties of the ITO and ZnO films used as back TCO contacts are shown in Table 2. Metal contacts typically 0.5 µm thick of Ag, Ti(25Å)/Ag and Al were evaporated either directly on n-layers or on ZnO. The electrical and optical behavior of the back contacts have been studied using temperature dependent current voltage (J-V) measurements in the light and dark, and quantum efficiency (QE) and reflection measurements.

Table 1. Gas flow rates (sccm) and properties of the a-Si and µc-Si n-layers

n-layer	H_2/SiH_4	ρ(Ω-cm)	E_A (eV)	E_{04} (eV)
a-Si	0/30	1000	0.30	1.90
µc-Si	200/2	1	0.05	2.05

Table 2. Sputtering conditions and properties of ITO and ZnO TCO layers.

TCO layer	% O_2 in Ar	resistivity (Ω-cm)	avg. absorption λ =l500-900 nm
ZnO:Al	0	6 E-4	0.011
ZnO:Al	0.2%	10 E-4	0.006
ITO	0.9%	4 E-4	0.012

J-V RESULTS AND ANALYSIS

Table 3 shows the results from a series of devices having either a-Si or µc-Si n-layers with either Ti/Ag, ITO/Ag, or ZnO/Ag back contacts. The ITO and ZnO layers were ~70 nm. The a-Si n-layers make very poor contacts with either ITO or ZnO as indicated by the low FF and high R_{oc} (dV/dJ at open circuit). Figure 1 shows the J-V curves for the four devices in Table 1 with a-Si n-layers. The device with the Ti/Ag metal contact is the only one with a "normal" J-V curve, having high FF and low R_{oc}. The non-ideal curvature around V_{oc} , characterized by large R_{oc} in Table 3, occurs for all three a-Si n-layer devices with a TCO/Ag contact. The curvature is greater for ZnO (Ar/O_2) than for ITO (Ar/O_2), and it is greater for ZnO (Ar/O_2) compared to ZnO (Ar). Table 2 indicates the ITO and ZnO resistivities differ by only a factor of 2. This suggests that a critical role of the sputtering atmosphere may be to

influence interfacial not bulk properties. The µc-Si n-layers have much higher FF and lower R_{oc} with a TCO/Ag contact. However, the a-Si or µc-Si n-layers have equivalent FF and R_{oc} with a metallic Ti/Ag contact, in agreement with [1]. Devices with µc-Si n-layers also have 10-15 mV higher V_{oc} and 0.5 to 1 mA/cm^2 higher J_{sc} for a given contact. Table 3 shows that higher J_{sc} is due to higher red QE, presumably due to lower absorption losses in the µc-Si n-layer. Devices with ITO have about 1 mA/cm^2 lower J_{sc} compared to devices with ZnO, for either type of n-layer. Reasons for this difference in J_{sc} between ITO and ZnO are unclear since they have the same index of refraction and, from Table 2, similar absorption.

The dark and illuminated J-V characteristics of all of the devices in Table 3 were measured from T=100°C to -50°C, and analyzed as described elsewhere [3-5]. Figure 2 shows V_{oc} vs T for four of the devices in Table 3, two with a-Si and two with µc-Si n-layers, each pair with different contacts. Identical behavior is seen for all devices with an intercept of V_{oc}(0 K)=1.70±.01 V, equal to the i-layer absorber bandgap, indicating that the Fermi level in the n-layer has no effect on the temperature dependence of the recombination [5].

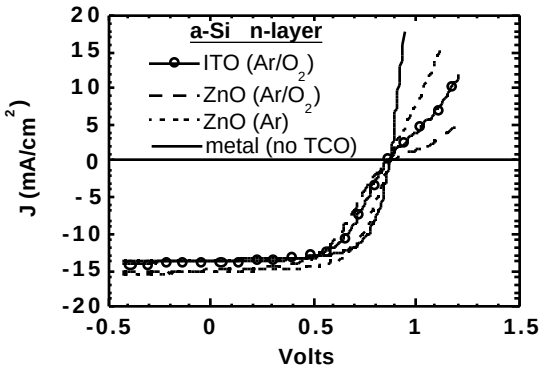

Figure 1. Illuminated J-V curves at 28°C for 4 identical devices with a-Si n-layers but different back contacts. Results are in Table 3.

Table 3. Cell performance of glass/SnO_2/p-i-n/TCO/Ag devices with either a-Si or µc-Si n-layers.

back contact	TCO sputter gas	n-layer	V_{oc} (V)	J_{sc} (mA/cm^2)	FF (%)	R_{oc} (Ω/cm^2)	Eff. (%)	QE@ 700nm
Ti/Ag	none	a-Si	0.871	13.5	70.3	5	8.3	0.28
Ti/Ag	none	µc-Si	0.881	14.1	70.4	5	8.7	0.35
ITO/Ag	Ar/0.9% O_2	a-Si	0.853	13.8	60.0	23	7.0	0.47
ITO/Ag	Ar/0.9% O_2	µc-Si	0.867	14.9	70.2	5	9.1	0.53
ZnO/Ag	Ar/0.2% O_2	a-Si	0.874	14.9	52.4	60	6.8	0.52
ZnO/Ag	Ar/0.2% O_2	µc-Si	0.889	16.2	68.0	5	9.8	0.61
ZnO/Ag	100% Ar	a-Si	0.872	15.0	64.0	13	8.5	0.52
ZnO/Ag	100% Ar	µc-Si	0.887	16.2	68.6	5	9.9	0.61

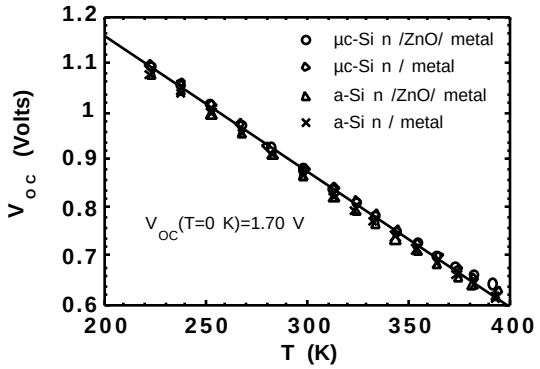

Figure 2. Temperature dependence of V_{oc} for two devices with a-Si n-layers and two devices with µc-Si n-layers, each with metal and TCO/metal contacts.

Although not shown, the curvature around V_{oc} becomes very large at lower temperatures for the devices with a-Si n-layers with TCO/Ag contacts. R_{oc} at -50°C exceeded 100 Ω/cm^2 for all three devices with a-Si n/TCO contacts. This drastic change in shape does not appear with µc-Si n / TCO / Ag or with a-Si n /Ti/Ag contacts where R_{oc} at -50°C was around 30 Ω/cm^2.

Figure 3 shows the dark J-V curves for three devices from Table 3 at three temperatures. At 100°C, they all appear very similar, having an expected exponential voltage dependence. At 25°C, the device with the a-Si n-layer with TCO/Ag contact shows a significant current limiting mechanism causing deviation from the exponential voltage dependence. At -50°C, all three devices show some high current limitation, with the µc-Si n-layer having the least.

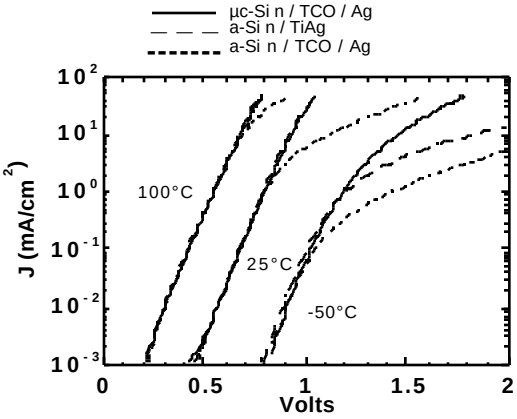

Figure 3. Dark J-V curves at 100, 25, and -50°C for devices with a-Si or µc-Si n-layers.

The dark J-V data has been analyzed with the following equations [5] by assuming the device consists of a diode in series with a resistance, or

$$J(V) = J_O \exp\{V-(J*R)/AkT\} \text{ with} \quad (1)$$
$$J_O = J_R \exp(-E_A/kT), \text{ then} \quad (2)$$
$$dV/dJ = R + \{AkT/q*(1/J)\}. \quad (3)$$

Analysis of the exponential region of the log J vs V curves in the dark (figure 3) gives A and J_o. The temperature dependence of J_o gives E_A and J_R from equation 2. The dark diode properties in the exponential region were independent of the contacts for all devices in Table 3 with E_A ~0.73 eV and J_R ~2-6E5 mA/cm^2. The diode A factors are A~2 for T>25°C, and increase at lower temperature. Combining A=2 with the intercept of V_{oc}(0 K)=E_G/q from Figure 2 confirms that space charge recombination is the dominant current mechanism [5] in all devices despite having such differently shaped light and dark J-V curves.

In order to determine whether the sub-exponential currents seen at high bias and low temperatures are due to a series resistance, the J-V data was analyzed by plotting dV/dJ vs 1/J. Figure 4 shows dV/dJ vs 1/J for the data at 25°C from Figure 3. If the model assumed by equation 1 applies, such a graph will be linear with the intercept of R and the slope of AkT/q as shown in equation 3. Figure 4 shows that the a-Si n-layer with a metal contact, and the µc-Si n-layer with a TCO/Ag contact have such linear relation, with R=1 Ω-cm^2 and A=2. These values are consistent with many other a-Si devices we have studied [4] and indicates that the n-layer and contact do not contribute to the series resistance when properly matched and processed. However, the device with the a-Si n-layer and TCO/Ag contact has very non-linear behavior, exhibiting non-ohmic current limitation even at 25°C attributable to the contact.

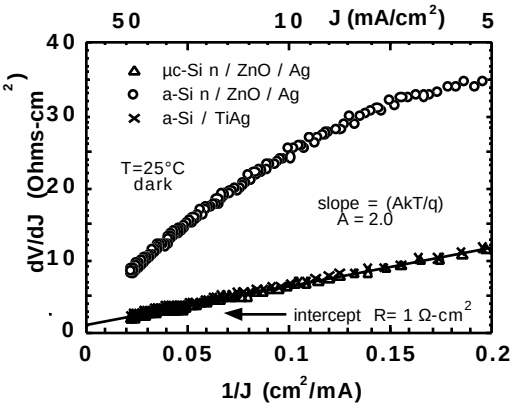

Figure 4. dV/dJ for same three devices in Figure 3 at 25°C.

DISCUSSION OF n/TCO BLOCKING CONTACT

Taken together, data on these devices suggests the low FF and large curvature at V_{oc} is due to a blocking contact at the a-Si n-layer/TCO contact. This barrier impedes electron injection at forward bias. A high density of interface states can cause a rectifying contact to form at the n/TCO interface by pinning the Fermi level causing band bending in the n-layer. A barrier E_n of 0.6 eV has been reported between SnO_2 and an a-Si n-layer [6]. Simulations of the n/contact interface found that increasing E_n from 0.6 to 0.8 eV resulted in a large decrease in FF from >70% to <60% without affecting

other parameters [7], consistent with results presented here. However, in all devices studied here, the n-layers were sufficiently doped to screen the i-layer from this second junction so it had no effect on the built-in potential, recombination or field in the i-layer.

Recent work on measuring and simulating J-V(T) in a-Si devices also finds that s-shaped curvature around V_{oc} becomes more pronounced at lower temperatures [8]. They concluded that the J-V curvature in the light [8] and sub-exponential J-V in the dark at V>1 V [9] is due to the p/TCO contact potential of 0.5 eV limiting hole injection. Our results show these effects can also be due to a barrier at the n/TCO contact limiting electron injection.

OPTICAL PROPERTIES OF BACK CONTACT

The optical role of ZnO and Ag was investigated by depositing ZnO layers from 0 to 200nm on devices with µc-Si n-layers, evaporating Ag, testing the devices, then etching away the Ag, and retesting the devices with only the ZnO contact. Figure 5 shows the QE at 700 nm for these samples with ZnO/Ag and, after Ag etching, just ZnO contacts. The QE decreases slightly with increasing ZnO thickness beyond 70 nm, probably due to absorption in the ZnO of light which has been reflected by the Ag contact. Without the Ag contact, the QE is independent of ZnO thickness since QE enhancement is only due to light which has been reflected at the Si/ZnO interface. Light which passes through the Si/ZnO interface is lost without the metal backreflector. Figure 5 shows that the QE is enhanced with a thin ZnO layer compared to the QE with Ti/Ag or Al contacts. These results are consistent with recent back reflector studies which model the optical role of a dielectric layer between the metal and the Si [10]. It is concluded that the dielectric layer enhances reflection back into the Si and reduces the amount of light incident on the metal contact, where significant absorption losses occur [10].

CONCLUSIONS

The n-layer and its contact can have a profound impact on the performance of a-Si devices, increasing efficiency from 7% to 10%. A µc-Si n-layer with a ZnO/metal contact is critical for high efficiency. The µc-Si n-layer creates an Ohmic contact with the TCO layer at T>25˚C, while the a-Si n-layer/TCO contact is blocking. Variations in device performance due to different TCO materials and sputtering conditions are much larger than expected based on bulk TCO properties, suggesting the Si/TCO interface may dominate the junction formation. ZnO/Ag is a better back reflector than ITO/Ag.

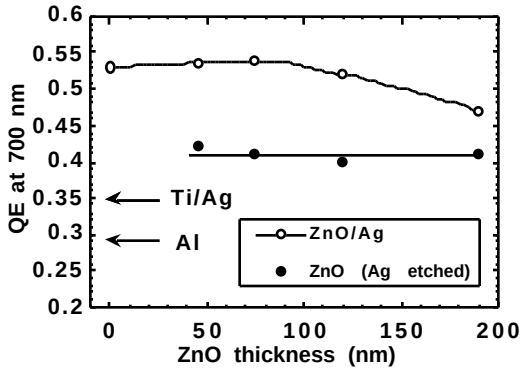

Figure 5. QE@700 nm for devices with ZnO/Ag contacts before and after etching Ag. Values for Al and Ti/Ag contacts also shown.

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Appendix 4

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$CdTe_{1-x}S_x$ ABSORBER LAYERS FOR THIN-FILM CdTe/CdS SOLAR CELLS

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ABSTRACT

Fabrication of high efficiency superstrate CdTe/CdS solar cells results in diffusion of CdS into the CdTe layer. Control of this diffusion is critical for processing cells with ultra-thin CdS layers. Two approaches are presented for retarding the diffusion of CdS into the CdTe-based absorber layer during chloride treatment of superstrate thin-film CdTe/CdS solar cells. One approach utilizes as-deposited $CdTe_{1-x}S_x$ alloy absorber layers with x near the thermodynamic limit of CdS-CdTe alloys to reduce the driving force for CdS diffusion. The second approach employs an anneal at T > 550°C prior to chloride heat treatment to reduce diffusion pathways near the absorber-window layer interface. X-ray diffraction, optical, and quantum efficiency measurements were used to quantify changes in CdS thickness and absorber layer composition.

INTRODUCTION

In fabricating high efficiency superstrate CdTe/CdS solar cells, intermixing of the CdTe and CdS layers occurs either during film growth or during post-deposition processing. The CdS thickness is reduced and can result in formation of CdTe/TCO junctions, reducing V_{oc} and imposing a low limit to the CdS thickness that can be employed for controllably fabricating uniform high efficiency devices over a large area. This paper presents approaches for controlling CdS diffusion.

Achieving the maximum conversion efficiency from CdTe-based thin-film devices and transferring successful research-scale fabrication processes to manufacturing-scale processes are ultimately limited by the effects of treatments on the CdS window layer and the resulting junction with the transparent conductive oxide (TCO). The high CdS absorption coefficient and 2.4 eV bandgap result in parasitic photon losses at wavelengths below 550 nm, necessitating ultra-thin (< 50 nm) CdS films in the final device for maximum current density (J_{sc}). Junctions between CdTe and the TCO such as In_2O_3:Sn (ITO) or SnO_2 have higher dark current density (J_o) and more voltage-dependent collection than those with CdS, resulting in lower open-circuit voltage (V_{oc}) and fill factor (FF). Thus, obtaining high conversion efficiency depends critically on maintaining a uniform CdS layer of the minimum possible thickness or reducing J_o in the CdTe/TCO junction, making control of the CdS layer thickness during processing of superstrate cells a critical issue.

A recent analysis by the present authors of CdTe/CdS devices fabricated by 7 participating groups of the CdTe team sponsored by the National Renewable Energy Laboratory (NREL) showed that a measurable degree of CdS-CdTe interdiffusion exists in all high efficiency devices made by electrodeposition, sputter deposition, physical vapor deposition (PVD), and close-space sublimation. The highest efficiency cells have been made with CdTe deposited by close-space sublimation on CdS deposited by chemical bath deposition [1]. Such devices, with CdTe absorber layers deposited at high temperature exhibit less interdiffusion than those deposited at low temperature. In an extreme example of the interdiffusion process, spray-deposited samples were found to be fully saturated with CdS as a result of near-complete consumption of the CdS window layer during absorber layer formation. As a tool for investigating post-deposition processing, the PVD process permits separation of individual effects which can occur during post-deposition steps, facilitated by the low deposition temperatures and the chemically pure deposition environment.

At typical PVD deposition temperatures, from 200 to 300°C, the as-deposited CdTe/CdS/TCO structure exhibits abrupt interfaces with sub-micron grain sizes. When these structures are subjected to heat treatment in the presence of chloride species, such as $CdCl_2$, several simultaneous changes occur, including significant atomic rearrangement resulting in CdS-CdTe mixing and formation of $CdTe_{1-x}S_x$ alloys on the absorber side of the device, limited by the solid solubility of CdS in CdTe at the treatment temperature [2-4]. The extent and mechanism of the mixing during heat treatment depends on the chloride concentration [5], oxygen concentration in the ambient [6], and the temperature-time profile [3,6,7].

Efforts to model the x-ray diffraction line profiles in 2- and 3-dimensions using a classical grain boundary and bulk approach do not agree with measured profiles for many cases [3,5]. A chemical mixing processes that may involve intermediate liquid components such as $CdTeCl_4$ and $CdSCl_4$ must be invoked to account for the measured profiles [5]. Recently, it was demonstrated that reduced interdiffusion and a qualitative match to expected profiles was obtained using $CdCl_2$ vapor treatments wherein delivery of chloride was delayed with respect to the heated CdTe/CdS/TCO structure, presumably due to a slight degree of recrystallization before reaction with chloride species [6,7].

In this paper, two approaches are presented for further controlling the CdS diffusion into the absorber layer of CdTe-based superstrate cells deposited by physical vapor deposition. One approach utilizes as-deposited $CdTe_{1-x}S_x$ absorber layers with x near the thermodynamic limit of CdS-CdTe alloys to reduce the driving force for CdS diffusion as proposed in [8]. The second approach employs an anneal at T > 550°C prior to chloride heat treatment to reduce diffusion pathways near the absorber-window layer interface.

EXPERIMENTAL

CdS, CdTe, and $CdTe_{1-x}S_x$ films were deposited onto In_2O_3:Sn (ITO) coated Corning 7059 glass by PVD from binary powder CdS and CdTe sources using boron nitride effusion cells. CdS films from 50 nm to 220 nm thick were deposited at 220°C at a deposition rate of 4 Å/s. As-deposited CdS film thickness was determined by optical absorption at 400 nm of the CdS/ITO/glass structure, calibrated for CdS by step profilometry, and are shown ± 5 nm. Prior to absorber layer deposition, the CdS layers were heat treated with $CdCl_2$ to increase their transmittance and to reduce the diffusion of CdTe into CdS during cell processing [9]. The CdS film thickness in completed devices was estimated from the quantum efficiency at 400 nm, calibrated by the optical absorption of selected films from which the absorber layer had been removed.

CdTe and $CdTe_{1-x}S_x$ films 5 µm thick were deposited at 250°C and deposition rates of ~8 Å/s. The S composition in the $CdTe_{1-x}S_x$ films was controlled by the relative temperatures, hence effusion rates, of the individual CdTe and CdS sources and was measured after deposition by energy dispersive x-ray spectroscopy (EDS) and x-ray diffraction (XRD) [10]. Three device configurations were fabricated: CdTe/CdS; CdTe/$CdTe_{0.95}S_{0.05}$/CdS (stepped); and $CdTe_{0.95}S_{0.05}$/CdS (uniform). The actual compositions are shown rounded to 0.01 to simplify presentation; all devices reported in this paper had CdS composition less than the solubility limit, x = 0.06, for the minimum processing temperature of 420°C. In the stepped configuration, the alloy layer constituted approximately one fourth of the total absorber layer thickness.

Evaluation of the effect of heat treatment temperature-time profile on interdiffusion, grain size, and device performance was carried out only on CdTe/CdS structures. The samples were annealed at T > 550°C for 4 minutes to 30 minutes in argon prior to $CdCl_2$ treatment.

Devices were fabricated by post-deposition $CdCl_2$ vapor treatment at 420°C in air followed by contacting with the diffused copper plus etch process described in Reference [11]. Current-voltage (J-V) and quantum efficiency (QE) measurements were used to characterize devices. J-V parameters were measured at 100 mW/cm^2 at 25°C with an Oriel xenon simulator.

ANALYSIS

After heat treatment, composition was measured by EDS of the surface and XRD through the bulk using Cu-k_α x-rays. Grain size was determined using the method of Heyn [3] applied to scanning electron microscopy (SEM). In selected cases, Auger depth profilometry (AES) and X-ray photospectroscopy (XPS) measurements were made at the National Renewable Energy Laboratory. Narrow-angle XRD scans of the CdTe and $CdTe_{1-x}S_x$ (511) peak with Cu $k_{\alpha 2}$ components removed were used to determine the intensity distribution of lattice parameters in the samples after treatment. The total CdS content in the treated film was determined from this distribution and was compared to the change in CdS thickness estimated from optical and quantum efficiency measurements. To facilitate detection of phases in the CdS-absorber interface region, samples ~2.5 µm thick are required. Typically, these were produced by using a polishing etch in bromine-methanol to thin the treated samples. In Reference [3] it was determined that identical profiles are obtained from thinner as-deposited samples under the same post-deposition treatment conditions as thicker samples which have been thinned, allowing the use of thin companion, or witness, samples for evaluation of a range of treatment conditions.

Examples of the XRD and optical-QE analyses used to assess interdiffusion on CdTe/CdS structures are depicted in Figures 1 and 2, respectively, for a sample treated with $CdCl_2$ vapor. In Figure 1, the (511) XRD line profile exhibits a strong peak at x = 0 with a tail extending to the solubility limit at x=0.06. Fourier analysis of the profile to remove instrumental broadening followed by integration of alloy component peaks yields an equivalent CdS layer thickness to account for the S content of the absorber layer, in this case 48 nm. In Figure 2, the transmission of the as-deposited CdS film, normalized for reflection, is shown

with the quantum efficiency of the device of Figure 1, made on the same CdS film. From the change in the short wavelength response, it is estimated that the CdS window layer lost 55 nm. The cell fabrication process did not affect the sharpness of the CdS transmission edge, since the CdS film was $CdCl_2$ treated prior to CdTe deposition, which prevents formation of S-rich $CdS_{1-y}Te_y$ as described in Reference [9]. Figure 3 shows reasonable agreement between the results of the XRD and optical methods for a range of samples.

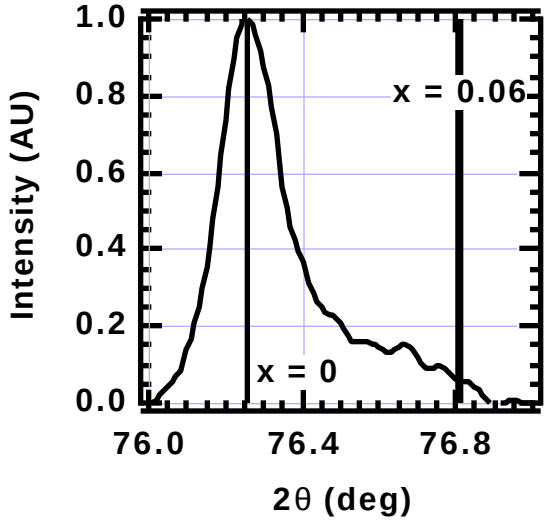

Figure 1. XRD (511) line profile of $CdCl_2$-treated 2.5 µm CdTe/70 nm CdS, showing a net gain of ~48 nm of CdS into the CdTe layer by formation of $CdTe_{1-x}S_x$ alloys.

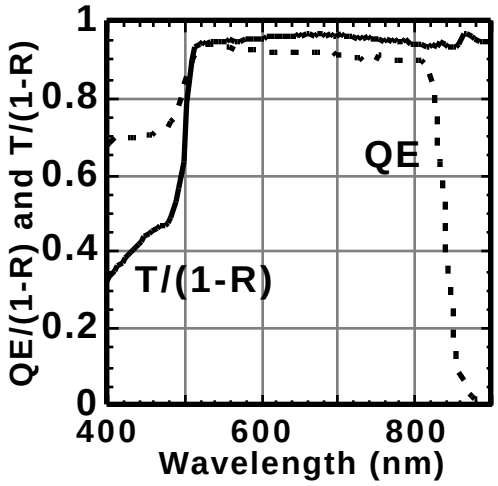

Figure 2. Optical transmission of 70 nm thick CdS film and quantum efficiency of completed device of Figure 1, showing a net loss of ~55 nm of CdS from the window layer.

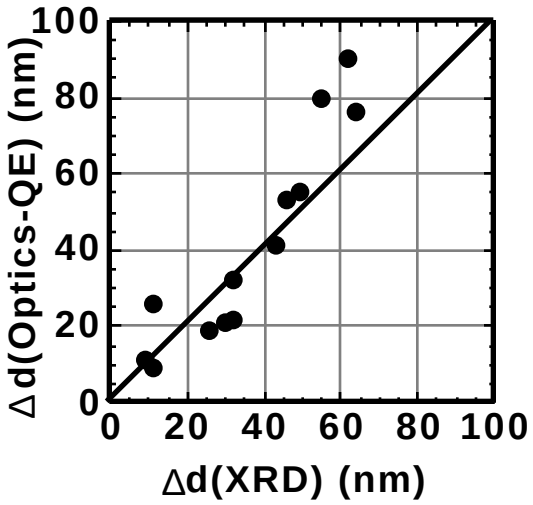

Figure 3. Comparison of XRD and optical methods: change in CdS thickness from transmission and quantum efficiency data versus equivalent CdS thickness to account for compositional XRD line profile broadening.

RESULTS: ABSORBER LAYER COMPOSITION

The presence of S throughout the $CdTe_{1-x}S_x$ absorber layer with x up to 0.06 did not measurably alter the recrystallization process or surface chemistry obtained after $CdCl_2$ treatment, allowing the same post-deposition processes to be used on all device configurations. For samples with as-deposited CdS content greater than 0.06, two phases, Te-rich cubic $CdTe_{0.94}S_{0.06}$ and S-rich hexagonal $CdS_{0.97}Te_{0.03}$, were detected by XRD. Glancing incidence XRD, Auger, and XPS measurements indicated that the $CdS_{1-y}Te_y$ was distributed throughout the film, but was primarily segregated to the free surface of the sample.

Dramatic evidence for the retarding of CdS diffusion into a uniform $CdTe_{0.95}S_{0.05}$ layer under conditions of high $CdCl_2$ concentration is seen by comparing the XRD line profiles of 2.5 µm thick samples in Figure 4. With CdTe absorber layers, this $CdCl_2$ treatment produced a broadened multi-modal distribution signifying the presence of several discreet regions having different compositions, equivalent to a CdS layer 110 nm thick. With the uniform $CdTe_{0.95}S_{0.05}$ layer and the identical $CdCl_2$ treatment, a single sharp line profile centered on the Bragg angle for x = 0.05 was obtained, having a small tail extending to x = 0.06, indicating a gain of an equivalent CdS thickness of less than 10 nm.

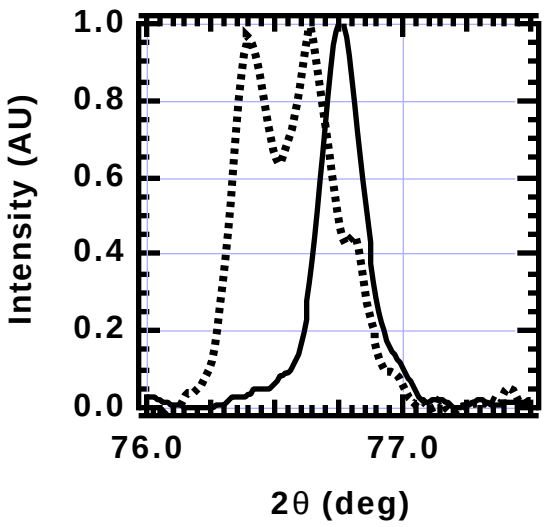

Figure 4. XRD (511) line profile of 2.5 µm CdTe/0.2 µm CdS (dotted) and 2.5 µm $CdTe_{0.95}S_{0.05}$/0.2 µm CdS (solid) after $CdCl_2$ treatment with high $CdCl_2$ concentration.

The retarding effect of the $CdTe_{1-x}S_x$ absorber in as-deposited structures is also borne out by analysis of the devices. Table 1 shows the change in CdS thickness after $CdCl_2$ treatment for pure CdTe, stepped alloy, and uniform alloy absorber layers for different initial CdS thicknesses. Comparing the devices with ~200 nm CdS, it is readily seen that the uniform alloy layer reduced CdS loss by more than 2X. The stepped layer was less effective, showing that the presence of the alloy near the solubility limit in the junction area alone is not sufficient to stop CdS diffusion. Notice that the difference between the film compositions, x = 0.05, and the solubility limit, x = 0.06, allows a theoretical maximum of ~50 nm of CdS to be incorporated into a 5 µm thick alloy film. Thus, optimal control of the quantity of CdS consumed during $CdCl_2$ is achieved by depositing the alloy absorber layer with composition close to the solubility limit for the processing temperature. Table 1 also shows that the J_{sc} increases as CdS final thickness is reduced. The V_{oc} is relatively constant with CdS thickness until the final CdS thickness falls below 75 nm. We speculate that non-uniform CdS consumption produces regions of complete CdS loss which result in parallel junctions between the absorber and the TCO.

RESULTS: POST-DEPOSITION HEAT TREATMENT

CdS diffusion is also controllable by reducing the number of available diffusion pathways. In the CdTe/CdS structures, the primary pathways are grain boundaries and crystallographic defects. Annealing the film at T > 550°C prior to chloride treatment enhances grain size, reduces crystallographic defects, and retards diffusion of CdS into CdTe [7,12]. As-deposited CdTe films have 200 nm wide columnar grains. As Table 2 shows, the mean lateral grain size doubled after the anneal; after $CdCl_2$ treatment the grain size increased to the usual value of 3 µm. An increase in grain size to 500 nm should reduce the total grain boundary area by ~5X, which will have a significant effect on the grain boundary diffusion rate. This is demonstrated by the XRD line profiles of CdTe/CdS samples with 2.5 µm thick CdTe treated with $CdCl_2$ vapor and treated with a 580°C anneal for 10 minutes prior to $CdCl_2$ vapor treatment (Figure 5).

Table 1. CdS thickness from optical and QE data and device parameters for different alloy configurations.

As-deposited Structure	Initial d(CdS) (nm)	Final d(CdS) (nm)	Δd(CdS) (nm)	Voc (mV)	Jsc (mA/cm^2)	FF (%)
CdTe	200	60	140	753	22.0	59.2
Stepped Alloy	220	125	95	776	22.0	67.4
	90	30	60	435	23.1	60.9
	50	20	30	412	25.0	60.0
Uniform Alloy	190	130	60	792	21.2	66.3
	105	75	30	769	22.6	60.0
	70	50	30	623	24.0	61.2

Table 2. Mean grain size of 2.5 µm CdTe/0.2 µm CdS obtained with different treatments.

Treatment	Temp (°C)	Time (min)	Mean Grain Size (μm)
None	-	-	0.2
Anneal	550	10	0.3
Anneal	550	30	0.8
Anneal	580	10	0.5
Anneal	600	4	1.0
Anneal + $CdCl_2$	550 420	30 20	0.8 3.0
$CdCl_2$ Only	420	20	3.0

The XRD line profile is a sharp, instrumentally-limited profile with a very small tail, corresponding to an equivalent CdS thickness of less than 10 nm. The sample which received no anneal exhibits a broad asymmetrical profile which corresponds to an equivalent CdS thickness of 100 nm. Space limitations preclude showing TEM cross-section micrographs of $CdCl_2$ treated samples with and without an anneal; the annealed sample exhibits a dense, uniform CdS layer after processing whereas the sample receiving $CdCl_2$ treatment only exhibits a discontinuous CdS layer after processing plus residual crystallographic defects in the absorber layer [12].

Table 3 shows CdS thickness and device parameters for samples with and without the anneal step. The samples were chosen to represent the initial CdS thickness at which a drop in V_{oc} has been observed for PVD samples processed with standard $CdCl_2$ treatment [13]. Use of the anneal step reduced the CdS loss by 2X and yielded higher V_{oc} and FF for the final CdS thicknesses shown. Devices with V_{oc} > 850 mV and conversion efficiencies of PVD devices greater than 12% have been fabricated using this treatment method. The TEM and device data together suggest that an explanation of the differences in performance between devices made by high temperature and low temperature processes lies in the density of both films, and of defects in the absorber layer which are not completely removed by $CdCl_2$ treatment.

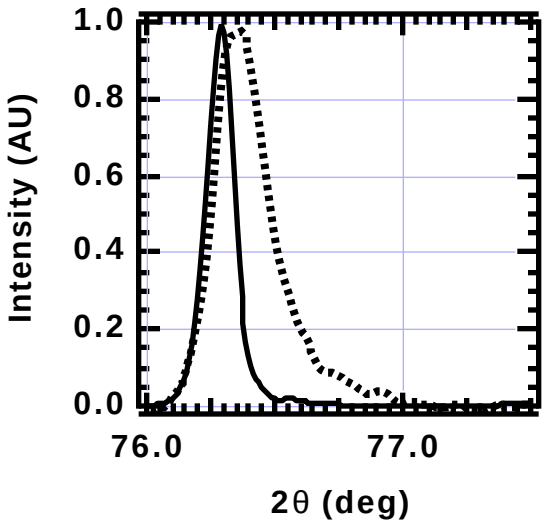

Figure 5. XRD (511) line profile of 2.5 μm CdTe/0.2 μm CdS after $CdCl_2$ vapor treatment (dotted) and after anneal in argon at 580°C for 10 minutes followed by $CdCl_2$ treatment (solid).

CONCLUSIONS

CdS diffusion into the absorber layer of CdTe-based superstrate thin-film solar cells is a limiting factor for fabrication control and device performance. The CdS loss can be reduced by depositing absorber layers having CdS content near the solubility limit for the processing temperatures used or by reducing diffusion pathways in the absorber layer by using a recrystallization step prior to $CdCl_2$ treatment. Use of denser CdS layer or of a densification step, combined with these techniques is expected to further extend control over the CdS diffusion and improve device performance with ultra-thin as-deposited CdS layers.

Table 3. CdS thickness from optical and QE data and device parameters for different heat treatments.

Method	Initial d(CdS) (nm)	Final d(CdS) (nm)	Δd(CdS) (nm)	Voc (mV)	Jsc (mA/cm^2)	FF (%)
$CdCl_2$ Only	180	100	80	775	22.9	67.0
Anneal + $CdCl_2$	180	150	30	795	21.0	70.0
$CdCl_2$ Only	160	90	70	690	21.4	50.8
Anneal + $CdCl_2$	160	140	40	790	20.6	70.6
Anneal + $CdCl_2$	130	115	15	705	21.5	57.9

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13. ABSTRACT *(Maximum 200 words)*
This report describes results achieved during phase I of a four-phase subcontract to develop and understand thin-film solar cell technology associated with $CuInSe_2$ and related alloys, a-Si and its alloys, and CdTe. Modules based on all these thin films are promising candidates to meet DOE long-range efficiency, reliability, and manufacturing cost goals. The critical issues being addressed under this program are intended to provide the science and engineering basis for developing viable commercial processes and to improve module performance. The generic research issues addressed are: 1) quantitative analysis of processing steps to provide information for efficient commercial-scale equipment design and operation; 2) device characterization relating the device performance to materials properties and process conditions; 3) development of alloy materials with different bandgaps to allow improved device structures for stability and compatibility with module design; 4) development of improved window/heterojunction layers and contacts to improve device performance and reliability; and 5) evaluation of cell stability with respect to illumination, temperature, and ambient and with respect to device structure and module encapsulation.

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