DOE/JPL/954356-5

SILICON-ON-CERAMIC COATING PROCESS

Silicon Sheet Growth Development for the Large-Area Silicon Sheet and Cell Development Tasks of the Low-Cost Silicon Solar Array Project

Quarterly Report No. 8, December 28, 1977—March 28, 1978

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April 20, 1978
Date Published

Work Performed Under Contract No. NAS-7-100-954356

Honeywell Corporate Material Sciences Center
Bloomington, Minnesota

U.S. Department of Energy

Solar Energy

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DOE/JPL/954356-5
Distribution Category UC-63b

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Period Covered 12/28/77-3/28/78

Published April 20, 1978

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The JPL Low-Cost Silicon Solar Array Project is sponsored by the U. S. Department of Energy and forms part of the Solar Photovoltaic Conversion Program to initiate a major effort toward the development of low-cost solar arrays. This work was performed for the Jet Propulsion Laboratory, California Institute of Technology, by agreement between NASA and DOE.

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CONTENTS

ILLUSTRATIONS

TABLES

SUMMARY

The objective of this research program is to investigate the technical and economic, feasibility of producing solar-cell-quality sheet silicon. We hope to do this by coating one surface of carbonized ceramic substrates with a thin layer of large-grain polycrystalline silicon from the melt.

Beginning the middle of February 1978, we expanded our program to include activities funded by the Task VI Cell Development Group of the Low-Cost Silicon Solar Array (LSSA) program at the Jet Propulsion Laboratory. This work is directed toward the solution of unique cell processing/design problems encountered within the silicon-on-ceramic (SOC) material due to its intimate contact with the ceramic substrate. Beginning next quarter, we will issue two separate quarterly reports. One will report on progress of the total effort; the other will identify the activities specifically funded by the Cell Development Group. The Cell Development Quarterly Report will be a replication of cell development information contained within the total Task II and Task VI Quarterly Report.

During the past quarter, we demonstrated significant progress in several areas:

- An antireflection (AR) coating facility was put in place. Results to date indicate a 33 percent average increase in cell performance using an 800Å silicon monoxide (SiO) coating.
- Further fabrication of active area cells yielded the best performance to date, namely, 9.5 percent conversion efficiency (AR-coated) on a 1-cm^2 active area cell.
- Our first slotted substrate cells were fabricated (base contact on back of substrate); best performance to date is 4.3 percent (uncoated) on a 5-cm^2 cell. (Slot spacing and widths were not optimized for cell performance).

Results and accomplishments during the quarter can be summarized as follows:

- Thermal shock resistance and fracture toughness measurements were completed on both Honeywell and Coors ceramic substrates. The range in values for the different materials is small.
- The proper adhesive was found, enabling us to carry out SOC adhesion tests.
- Coors determined that the thermal expansion coefficient of mullite

can be closely matched with silicon without increasing the cost of the mullite material.

- A new, experimental, dip coater design was 80 percent completed. This will be used to study methods for increasing the throughput of our SOC process without sacrificing thickness.

- The dip coater consistently yielded material capable of solar-cell quality material. Our best-performing cells were produced after the latest cleaning of the dipper, indicating our contamination problem is solved.

- The problem of the silicon spalling off of some ceramic substrates was identified as a loss of porosity and roughness as a result of the dipping.

- The overheating problems in the continuous coater were resolved. Thermal gradients existing within this coater caused substrate breakup. This condition is currently being modified by the addition of preheaters and afterheaters.

- Light-beam-induced current (LBIC) measurements indicated minority carrier diffusion lengths (L_D) of 14 to 22 μm within grains of SOC cells.

- An experiment where three different base dopings (N_A) were used in successive dippings was carried out to establish a correlation between N_A and J_{sc}. No correlation was established, in that the N_A range was too narrow.

- A new fabrication procedure was adopted for processing slotted substrate cells (removing the base contact from the top). The best performance to date is 4.3 percent on a 5-cm^2 cell.

- Our processing techniques yielded some cells with low fill factors ($\sim$0.60). This will be improved during the next quarter.

- Work began in the novel device development area. The first structures investigated were the integral optical coupler and P-N junction formation using doped carbon as a diffusion source.

- Ammonia borane (NH_3BH_3) mixed with carbon resin showed promise as a P^+ dopant source.

- An exact theoretical analysis was made of the solar-cell electrode design geometry effect on cell performance. This analysis yielded electrode design criteria needed to design cells for maximum performance.

INTRODUCTION

This research program began on 21 October 1975. Its purpose is to investigate the technical and economic feasibility of producing solar-cell-quality sheet silicon by coating inexpensive ceramic substrates with a thin layer of polycrystalline silicon. The coating methods to be developed are directed toward a minimum-cost process for producing solar cells with a terrestrial conversion efficiency of 12 percent or greater.

By applying a graphite coating to one face of a ceramic substrate, molten silicon can be caused to wet only that graphite-coated face and produce uniform thin layers of large-grain polycrystalline silicon; thus, only a minimal quantity of silicon is consumed. A dip-coating method for putting silicon on ceramic (SOC) has been shown to produce solar-cell-quality sheet silicon. This method and a continuous coating process also being investigated have excellent scale-up potential which offers an outstanding cost-effective way to manufacture large-area solar cells. The dip-coating investigation has shown that, as the substrate is pulled from the molten silicon, crystallization continues to occur from previously grown silicon. Therefore, as the substrate length is increased (as would be the case in a scaled-up process), the expectancy for larger crystallites increases.

A variety of ceramic materials have been dip-coated with silicon. The investigation has shown that mullite substrates containing an excess of SiO_2 best match the thermal expansion coefficient of silicon and hence produce the best SOC layers. With such substrates, smooth and uniform silicon layers 25 cm^2 in area have been achieved with single-crystal grains as large as 4 mm in width and several cm in length. Crystal length is limited by the length of the substrate. The thickness of the coating and the size of the crystalline grains are controlled by the temperature of the melt and the rate at which the substrate is withdrawn from the melt.

The solar-cell potential of this SOC sheet silicon is promising. To date, solar cells with areas from 1 to 10 cm^2 have been fabricated from material with an as-grown surface. Recently, an antireflection (AR) coating has been applied to our SOC cells. Conversion efficiencies greater than 9 percent have been achieved without optimizing series resistance characteristics. Such cells typically have open-circuit voltages and short-circuit current densities of 0.51 V and 20 mA/cm^2, respectively.

The SOC solar cell is unique in that its total area is limited only by device design considerations. Because it is on an insulating substrate, special consideration must be given

to electrical contact to the base region. To date, this has been done using an interdigital electrode pattern. One method which offers considerable promise is to place small slots in the substrate parallel to the crystalline growth direction and contact the base region by metalizing the silicon that is exposed through the slots on the back side of the substrate. Smooth, continuous coatings have been obtained on substrates which were slotted in the green state prior to high-temperature firing. Initial cell results indicate a 4.3 percent conversion efficiency (no AR coating) on a 5-cm^2 cell. This cell was not optimized for device performance.

Development efforts are continuing in such areas as improvement in growth rate, reduction of progressive melt contamination, and optimiziation of electrical contacts to the base layer of the cell. The investigation has shown that mullite substrates, to a limited extent, dissolve in molten silicon. The impurities from the substrate are believed to adversely affect solar-cell conversion efficiency. A special type of graphite coating on the substrate has shown a potential for inhibiting this dissolution of mullite. Should these coatings prove to satisfactorily isolate the substrate from the melt in a cost-effective manner, improved solar-cell performance should be attained. An alternate method for reducing substrate dissolution is to reduce the contact area the substrate makes with the silicon melt. Therefore, a silicon coating facility has been constructed which is designed to coat large (10-cm x 100-cm) substrates in a continuous manner. It is expected that this new facility will not only improve the growth rate, but also minimize the silicon melt's contact with the substrate. This should reduce the rate at which the melt becomes contaminated. This new facility will also permit a study of possible continued grain growth by accommodating the use of longer substrates. It should also reveal problems that are likely to be encountered in a scale-up process.

TECHNICAL DISCUSSION

SUBSTRATE CHARACTERIZATION (B. Koepke and K. Wuori)

During the past quarter, most of the efforts concerning substrate characterization were concerned with determinations of the fracture toughness and thermal shock resistance of Coors and Honeywell Ceramic Center substrates and with devising a means to quantitatively measure the adhesion of the silcon layer to the ceramic substrate. Some important data were received from Coors on low-thermal-expansion substrate compositions which are also reported in this section.

Fracture Toughness Testing

Fracture toughness is a measure of the resistance of a material to fast, catastrophic fracture. Fracture toughness is usually given as the critical stress intensity factory, K_{IC}, in units of $MNm^{-3/2}$ (meganewtons meter $^{-3/2}$). Further discussion of K_{IC} and techniques used to measure it were given in the Quarterly Report No. 7 and will not be repeated here.

K_{IC} measurements have now been made on all experimental substrate materials. These data are listed in Table 1. Six measurements were made on each Coor composition and five have been run on the Honeywell material.

Table 1. Fracture Toughness of Mullite Substrates

Code	Material	K_{IC} ($MNm^{-3/2}$)
---	MV20*	1.98 ± 0.23
A	S1SI	2.39 ± 0.31
B	High-mullite	2.22 ± 0.06
D	Glass-property modification	2.37 ± 0.26
E	Open-porosity	2.17 ± 0.23
F	High-purity	2.23 ± 0.23
G	Electrically-fused	2.11 ± 0.28
H	Reducing-fire	2.30 ± 0.31

*Honeywell Ceramics Center

The fracture toughness of all the materials supplied by Coors was about the same, with the open-porosity and electrically-fused modifications being lowest. As noted in Quarterly Report No. 7, all substrate compositions except the electrically fused mullite survived the dipping process. The failure of the electrically-fused mullite composition was more likely due to its high thermal expansion and high alumina/silica ratio rather than its slightly lower K_{IC} value.

As noted in Quarterly Report No. 7, the K_{IC} measurements made on the MV20 were from a batch that had a tendency to fracture during dipping. The fracture toughness of this material is somewhat lower than that of the other substrate materials as might be expected. At this time, we have not measured K_{IC} on other batches of MV20.

To summarize, the range in fracture toughness of all substrates used in this study was found to be small. We will complete these measurements during the next quarter by measuring K_{IC} on other batches of MV20.

Thermal Shock Measurements

Thermal shock measurements were completed on the substrate materials. The method used is attributed to Hasselman[1] in which the room temperature fracture strength (usually in bending) of samples quenched from elevated temeratures is measured as a function of quench temperature. When the quenching stresses are sufficient to propagate locallized flaws in the ceramic, the room temperature strength decreases abruptly. The quench temperature causing the decrease in strength is an indication of how much thermal shock the material can withstand. Higher critical quench temperatures imply greater thermal shock resistance.

An example of a thermal shock resistance measurement for Coors S1SI material is shown in Figure 1. In this material the critical quench temperature is 290°C. The room temperature fracture strength and critical quench temperatures for the experimental substrate materials are listed in Table 2.

The Coors substrates exhibited lower thermal shock resistance and higher room temperature strength than the MV20. The higher strengths reflected, no doubt, smaller flaw sizes due to the increased homogeneity resulting from cold pressing and firing. The increased thermal shock resistance of the MV20 substrates is suggested to result from the lower thermal expansion of these materials. The thermal expansion of MV20 is 0.495 percent from room temperature (R.T.) to 1000°C, while all Coors compositions, except the high-silica modification (not tested to date) and high-mullite modification, were above 0.5 percent.[2] It should be mentioned here that the room temperature strengths measured during the thermal shock measurements correlated well with those reported in the Silicon-on-Ceramic Process Second Annual Report.

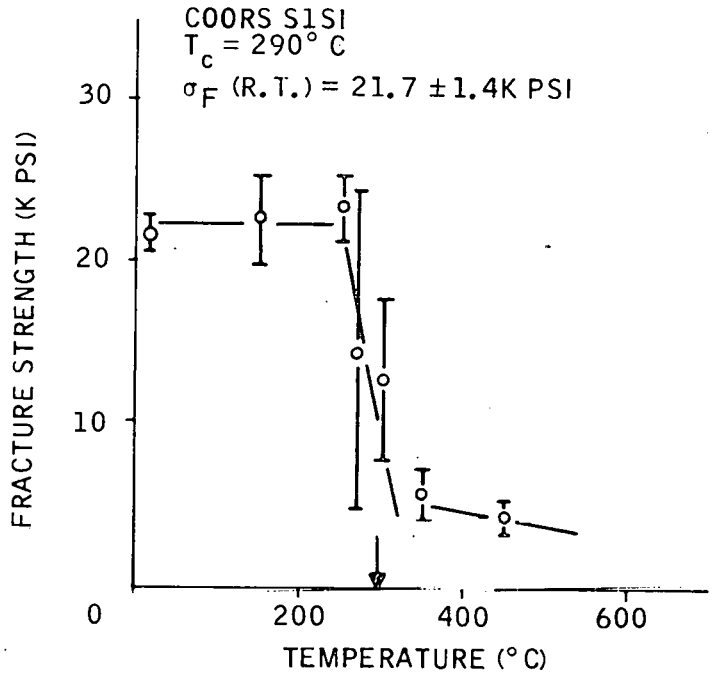


Figure 1. Thermal Shock Resistance of Coors S1SI Mullite Material

Table 2. Room Temperature Fracture Strength and Critical Quench Temperatures for Honeywell and Coors Substrate Materials

Code	Material	Strength (kpsi)	Critical Quench Temperature (°C)
Series 7-50	MV20	15.0 ± 2.7	340
Series 7-300	MV20	13.8 ± 2.3	340
A	S1SI	21.7 ± 1.4	290
B	High-mullite	21.0 ± 1.6	290
D	Glass-property modification	21.1 ± 1.4	285
E	Open-porosity	17.1 ± 1.8	275
F	High-purity	19.4 ± 0.9	285
G	Electrically-fused	16.4 ± 6.5	225
H	Reducing-fire	22.3 ± 1.5	280

In summary, little variation was observed in the thermal shock resistance of the Coors substrates. The MV20 material had superior thermal shock resistance but lower strength. The superior thermal shock resistance of the MV20 is attributed to the lower thermal expansion of this material. Our general experience has been that all substrates, with the exception of the electrically-fused mullite, have the thermal shock resistance and strength required to survive the dipping process.

Measurements of the Adhesion of SOC Substrates

In Quarterly Report No. 7, our initial attempts to measure the fracture energy of the SOC interface were reported. In those tests, a slotted, modified double-cantilever beam specimen was used. The slot was coated on each side with carbon and the specimen dipped to fill the slot with silicon. The sample was designed to fracture along the silicon-ceramic interface by offsetting the silicon-filled slot so that one edge of the slot coincided with the centerline of the specimen. Difficulties were encountered with completely filling the slot with silicon and with fracture occurring predominantly through the silicon. The two successful tests that were run yielded values of K_{IC} of 1.65 and 1.95 $MNm^{-3/2}$ These values are reasonable when compared with Table 1 and imply that the silicon is mechanically adhering to the ceramic but over only a fraction of the surface.

In view of the marginal success of this technique, we have also been attempting to measure adhesion by the technique of Becher, et al.[3,4] This technique is another modification of the double-cantilever beam geometry in which a steel beam is cemented to the silicon. The steel beam is then loaded as a cantilever beam, and fracture occurs at the silicon-ceramic interface as shown in Figure 2. The biggest problem with this geometry, of course, is finding a cement strong enough to withstand the testing loads. Preliminary tests run during the past quarter identified a suitable adhesive. The adhesive, Buehler Epo-Kwick, Epoxy No. 20-8128, is an epoxy used for mounting metallurgical specimens. Figure 3 is a photograph of a specimen before and after testing. The silicon coating is ground off part of the surface as shown in the top photo. The specimen after testing is shown in the bottom photo. Fracture has occurred entirely at the silicon-ceramic interface. A jig is being fabricated that will allow us to apply this technique to quantitatively measure the fracture energy and to determine the adhesion as a function of parameters related to carbon deposition processes. These measurements will be made during the next reporting period.

Development of Low-Thermal-Expansion Substrates

Under a separate contract, J. Sibold and D. Wirth at Coors are developing experimental substrate materials that exhibit improved thermal compatibility with silicon. Some of

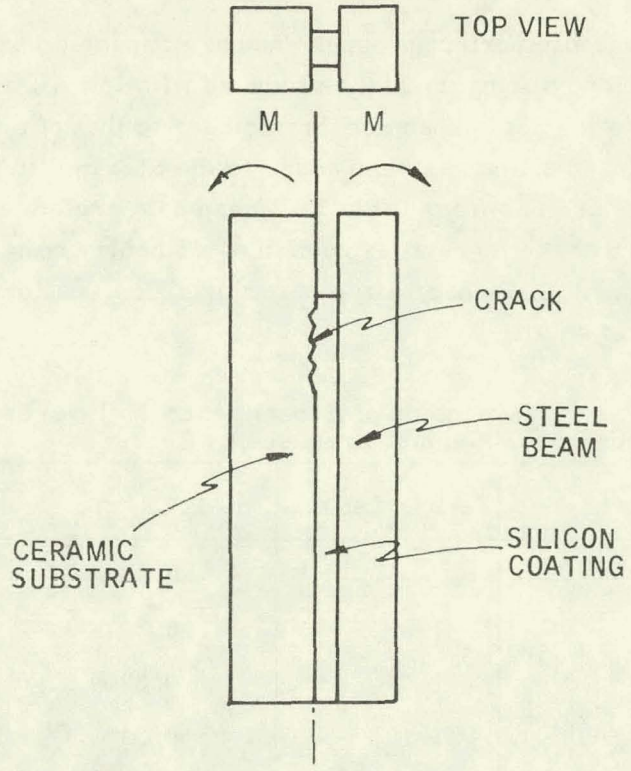


Figure 2. Constant-Moment, Double-Cantilever Beam Fracture Mechanics Specimen

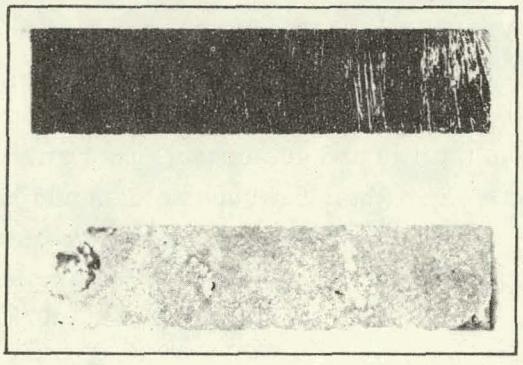


Figure 3. Photograph (Magnification 2x) Showing Untested (Top) and Tested (Bottom) Modified Double-Cantilever Beam Specimens Used to Measure Adhesion of SOC Substrate. In the tested specimen, the silicon layer has been completely removed.

their recent results show important progress and are repeated here. A number of experimental mullite compositions are being produced with low Al_2O_3/SiO_2 ratios with the intention of driving the thermal expansion down closer to that of silicon. To do this, naturally-occurring fused silica has been added to the S1Si mullite composition in varying amounts. The results are shown in Table 3. These data are quite encouraging and show, as one might expect, that the thermal expansion of a fireclay refractory decreases as the silica content increases. Since naturally-occurring silica is a low-cost material, the overall price change is small.

Table 3. Thermal Expansion of Experimental Mullite-Based Ceramic Substrate Materials Produced by Coors

Material	Al_2O_3/SiO_2	$\Delta\ell/\ell\Delta$ (R. T. to 700°C)	$\Delta\ell/\ell\Delta$ (R. T. to 1000°C)
Silicon		0.26	0.40
MV20	1.2*	0.307	0.495
SlSI	1.47*	0.320	0.520
SlSI + 10% excess SiO_2	1.18†	0.310	0.505
SlSI + 12.5% excess SiO_2	1.12†	0.305	0.485
SlSI + 15% excess SiO_2	1.07†	0.295	0.470
SlSI + 17.5% excess SiO_2	1.02†	0.290	0.450
60% fused mullite + 40% fused silica	0.874†	0.250	‡

* Coors chemical analysis.

† Calculated from raw materials.

‡ Not measured.

By adding 17.5 percent silica, the thermal expansion dropped 9 percent. The composition containing 60 percent fused mullite and 40 percent fused silica had a lower thermal expansion than the silicon. We feel the ideal substrate should have a thermal expansion equal to or slightly greater than silicon, since the residual stress in the silicon layer, if one exists, will be compressive. We have received samples of the 60 percent mullite, 40 percent silica material and will dip them in the near future. Samples of the other compositions are forthcoming.

SHEET SILICON GROWTH (R. B. Maciolek, J. D. Heaps, R. I. George, L. D. Nelson, and D. J. Sauve)

General Discussion

During the past quarter, the SOC coating effort was divided into three interrelated tasks, as follows:

1) Providing state-of-the-art SOC layers for cell fabrication and device evaluation studies.

2) Performing SOC growth studies with the objective of optimizing the growth velocity, stress-relieving the silicon coating, improving the silicon ceramic bond, and reducing the coating's series contact resistance.

3) Developing a continuous SOC coating technique capable of providing uniform coatings of large-grain silicon on large-area (1000 cm^2) substrates.

The coating effort was modified principally to provide more highly controlled, variable free sheet silicon to the cell fabrication and device evaluation portion of the program. In the past, the first two tasks above relied on the existing dip coater for their experimental procedures. Satisfying the objectives of the second task required constant modification of the dip coater. Occasionally, some of these modifications adversely affected the quality of the silicon coatings being used for device studies. The design of a new experimental dip coater, which is discussed below, is about 80 percent completed and will be constructed early in the next quarter to satisfy the needs of the second task. The existing dip coater has now been cleaned and all of its internal furnace parts have been replaced to provide the highest-purity sheet silicon possible for cell fabrication. Once the experimental dip coater is completed, the existing dip coater will be used exclusively to provide state-of-the-art SOC coatings for device studies.

Experimental Dip Coater

A new experimental dip coater is being designed to perform SOC growth studies. In the interest of saving time, its design, where practical, copies the existing coater. Changes in the design are being made, however, to accommodate increased versatility and improved accessibility. The growth chamber is being enlarged to provide sufficient space for adding "cold fingers" to increase the temperature gradient of the substrate above the melt. By removing the latent heat more rapidly, it should be possible to increase the

growth rate for a given coating thickness. The design will also permit the use of two types of heating elements. One type will be identical to that in the existing coater and the second type will allow us more freedom in altering the temperature gradient above the surface of the melt. Use of the identical heater will assure us that for certain experimental applications the new coater will be able to duplicate the results of the existing coater.

Toward the end of the quarter, Drs. Barry Koepke and David Zook visited Dr. J. D. Verhoeven of Iowa State University to discuss our solidification studies. Dr. Verhoeven is a recognized expert in solidification. He has since visited our laboratory to discuss methods for increasing SOC growth velocity. He reviewed the design of the new coater and suggested ways for modifying and measuring the temperature gradient within the ceramic substrate being dip-coated. In his opinion, the horizontal SCIM coating method offered greater flexibility toward improvement in growth velocity.

Growth Experiments

Following the cleanup process performed on the existing dip coater, a purity level run was made where no substrates were dipped into the melt. Resistivity measurements made on samples taken from the solidified melt indicated variations of resistivity from 100 to 1000 ohm-cm. These measurements were comparable to the highest purity levels we have previously measured. It should be remembered, however, that most common metallic impurities are electrically inactive in silicon, but do provide devastating recombination sites. Nevertheless, past results have shown some correlation between carrier purity of various melts and the performance of solar cells fabricated from the material of these melts.

Approximately 140 substrates were dip-coated during the quarter. No problems were experienced with breakage of either the nonslotted or the slotted substrates during dip-coating. Because the interiors of the slots were not coated with carbon, they did not fill with silicon, thus reducing the chance of substrate breakage due to thermal expansion differences. The decision not to fill the slots results from the fact that electrical contact can be made to the cell's base layer through the slot opening whether it is filled or not; thus, there is little reason for consuming additional silicon which only adds to the series resistance of the cell.

Many of the substrates coated were supplied by Coors Refractory Co. To date, the various compositions of Coors dip-coat-size substrates have been supplied to us with a thickness of approximately 3 mm as opposed to the Honeywell-fabricated MV20 substrates which are typically 2 mm thick. It has been observed that for a given set of growth

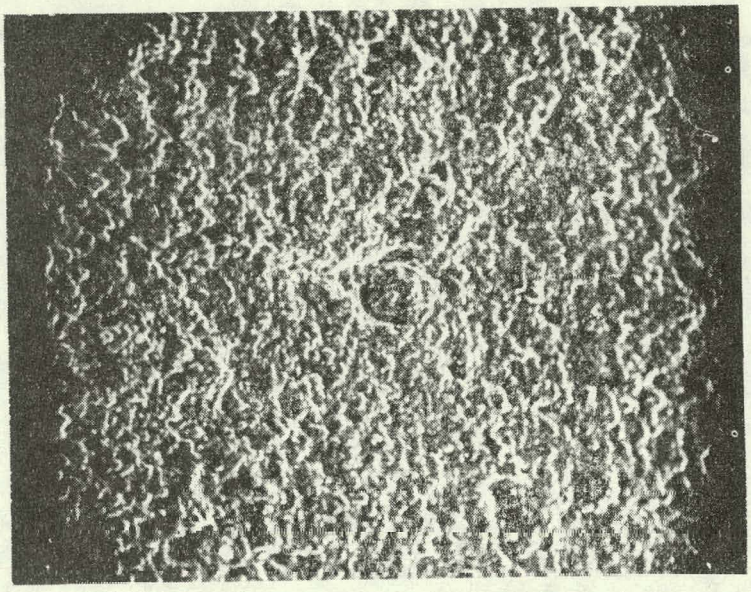
parameters, layers coated on Honeywell substrates are thicker than those coated on Coors substrates. This is believed to result from the greater temperature gradient within the thinner substrate. This conclusion is further supported by the fact that dip-coat-size samples prepared from two thinner (0.5 mm and 1.0 mm) Coors substrates also had correspondingly thicker layers for similar growth parameters.

Mullite and other substrates have been coated with a thin glassy carbon (GC) film prepared in-house. This is being done to investigate the possibility of using this approach to provide a dopant source for our basic layer contact interface. Substrates were dipped and the wetability of silicon was found to be excellent. Silicon adherence has been demonstrated on a coating as thin as 6.7×10^{-5} cm. In dippings with thicker layers, the silicon has been observed to wet at a level which is slightly higher than the melt level. In one experiment, a graphite substrate, which would normally dissolve in molten silicon, was coated on both sides with several thin layers of the GC and dipped. The carbon remained intact. This indicates that the dissolution of the GC film is only slight and that it might be an excellent barrier to inhibit diffusion of impurities from the mullite, as well as provide a means for doping the basic layer at the ceramic interface P^+.

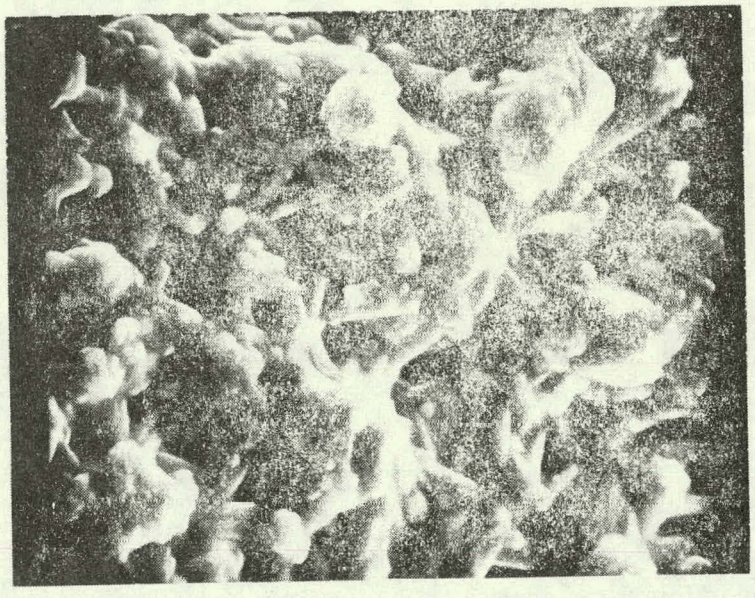
Grooved (partially slotted) substrates have been successfully dip-coated with silicon and show that very little disruption of the growth occurs when the grooves are parallel to the surface of the melt. Care was taken to see that Dag carbon did not run into the grooves. Closer spacing and wider grooves could be used. The spacing and groove width were chosen for present convenience. The process offers the advantage of contacting the back of the silicon, spanning the entire back surface. Very good contact geometry can be obtained. The main disadvantage at the present is the need for a means of ohmic contact to the back of the silicon in the grooves. The aluminum paste technique suggested by John Scott-Monck of JPL for BSF solar cells may be a means by which a back contact can be made.

SOC Bonding Study

It has been observed that occasionally the silicon coating will spall off the ceramic substrate either immediately after growth or during diffusion. In an effort to solve this problem, we have begun examining the nature of the surfaces of the ceramic substrates. It was recognized early in the program that the texture of the ceramic surface played an important role in the bonding of the silicon to the ceramic. It was found that the silicon flowed into the surface pores and in effect locked the silicon to the ceramic. It was thought that one way to alter the texture of the ceramic surface would be to etch it. However, as can be seen from Figures 4, 5, and 6, which are scanning electron microscope (SEM) photomicrographs of undipped and dipped MV20 mullite, etching only alters the surface to the extent that the glass matrix is dissolved. It appears that the difference in the rate of attack between the glass and mullite is too great for etching to effectively create pits in the surface to promote bonding.

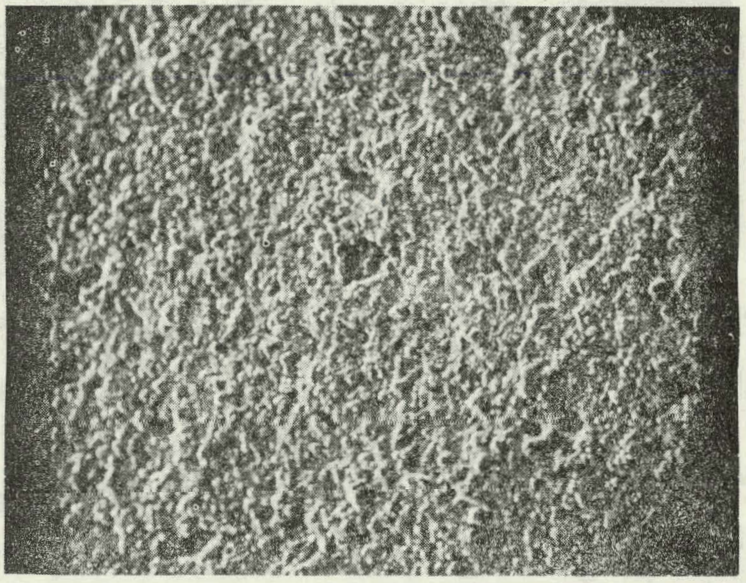


a) SEM (200x)

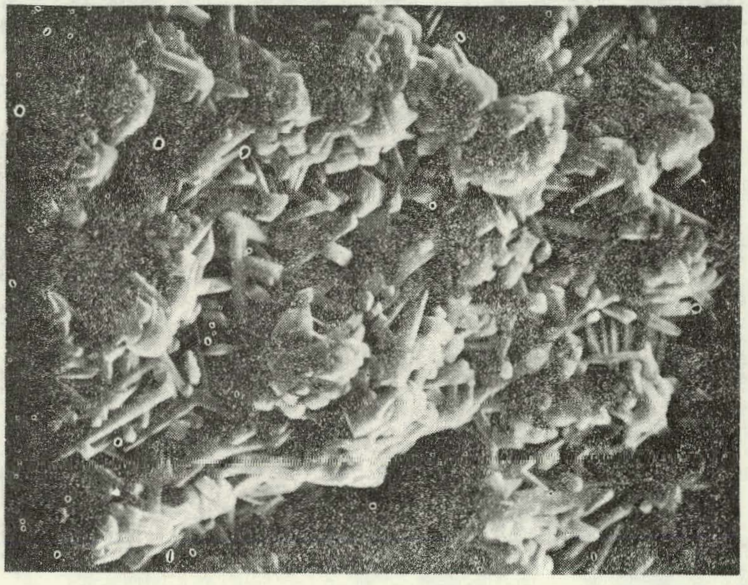


b) SEM (2000x)

Figure 4. Photomicrographs (SEM 200x and 2000x) of As-Fired Surface MV20 Mullite

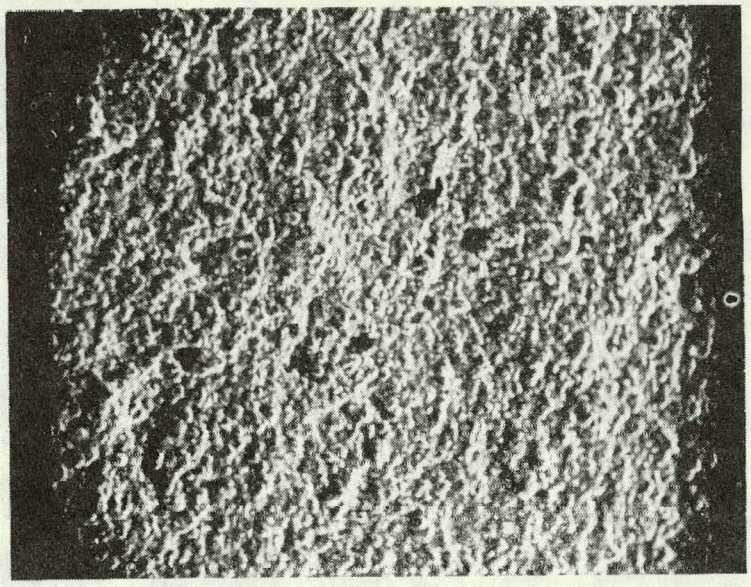


a) SEM (200x)



b) SEM (2000x)

Figure 5. Photomicrographs (SEM 200x and 2000x) of Etched (15 Seconds) MV20 Mullite



a) SEM (200x)

b) SEM (2000x)

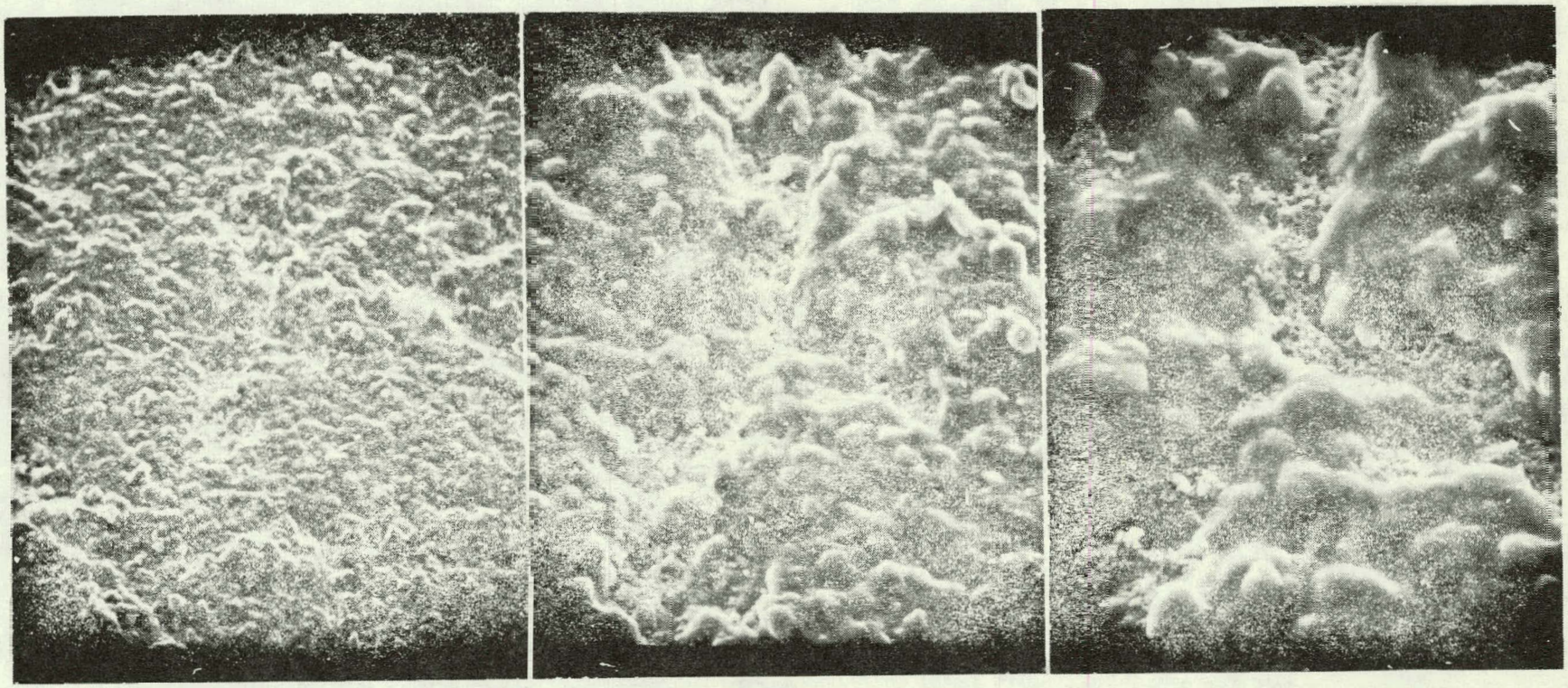
Figure 6. Photomicrographs (SEM 200x and 2000x) of Etched (60 Seconds) MV20 Mullite

To see what effect the actual dipping has on the surface of the ceramic, we examined the uncoated, back side of a sample. The result is shown in the SEM photomicrographs of Figure 7. It appears that the surface roughness is actually reduced, as both the glass and mullite phases have melted and flowed. Samples of the various ceramics were examined before and after dipping using scanning electron microscopy. The results shown in the following photomicrographs are in agreement with the observations made last month, namely, that the mullite melts and flows to some extent upon being dipped in the molten silicon. We hypothesize that the silicon reacts chemically with the mullite, producing a glassy phase which is immiscible with molten silicon. This is reasonable since silicon does not wet SiO_2. The dipped samples are the back sides of the substrates that were not carbon-coated and simply show the thermal effects of being dipped in molten silicon. Figure 8 is a photomicrograph of the very first batch of McDanel MV20 mullite and in the SOC experiments before dipping. Figure 9 is a photomicrograph of the same material after dipping. Note retention of some roughness and porosity, which is considered necessary for the silicon to adhere to the substrate. Figures 10 and 11 are photomicrographs of the latest batch of MV20 before and after dipping. The porosity retention appears to be less than that observed in the first batch. Figures 12 and 13 show a Coors mullite, S1SI, before and after dipping. The resultant surface after dipping is fairly smooth. The very porous material on the surface is silicon oxide that was vapor-deposited on the surface after dipping. Figures 14 and 15 show a high-mullite formula modification of S1SI before and after dipping. The structure is not very porous before dipping but develops a very finely porous surface after dipping. Figures 16 and 17 show an S1SI formulation in which the glass properties were modified. The surface after dipping is comparable to that of the standard S1SI. Figures 18 and 19 show an attempt at open-porosity modification of S1SI. The photographs indicate that there wasn't much porosity before or after dipping. A high-purity version of S1SI is shown in Figures 20 and 21. Again, the surface after dipping appears similar to that of the standard S1SI. Figures 22 and 23 show samples of an electrically-fused mullite body, prepared by Coors, before and after dipping. Note the uniform porosity before and after.

Finally, Figures 24 and 25 show samples of the Coors mullite from 1-meter-long substrates. Some roughness and porosity was lost as a result of dipping. This study indicates porosity in the ceramic is important to good silicon adhesion and will be modified in certain compositions by contact with the silicon melt.

Continuous Coating Process

During the quarter, the 24-kW power supplies, which were temporarily loaned to us, were replaced by the 45-kW supplies originally ordered. Initial operational testing of the continuous (SCIM) coater at the power levels achievable with these larger supplies uncovered numerous overheating problems. The most serious overheating problems were related to contact resistance between the heating elements and their electrodes.



a) SEM (200x)

b) SEM (500x)

c) SEM (1000x)

Figure 7. Photomicrographs (SEM 200x, 500x, 1000x) of Ceramic Dipped in Molten Silicon but not Coated

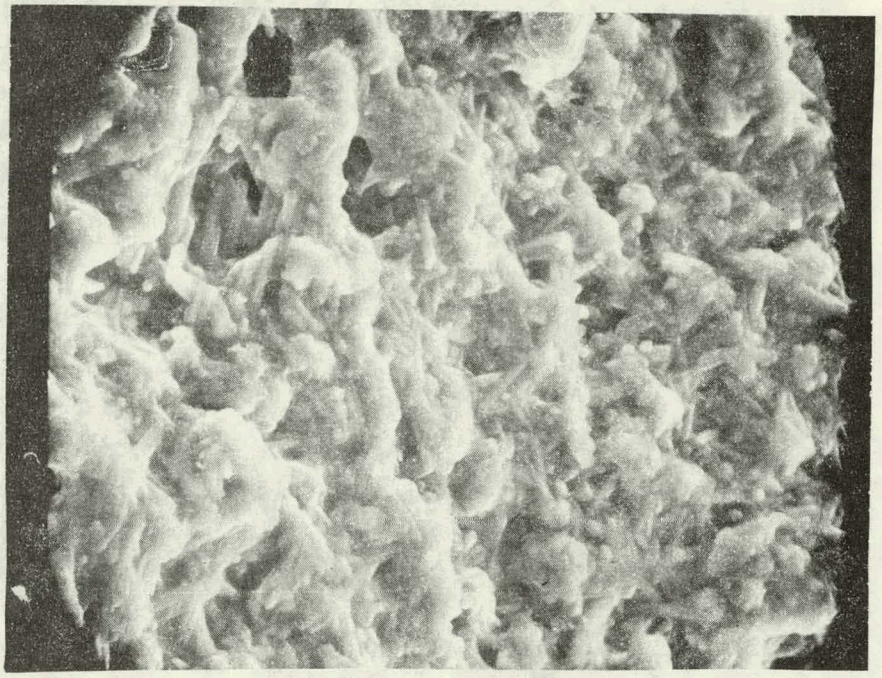


Figure 8. Photomicrograph (SEM 1000x) of MR27, Not Dipped

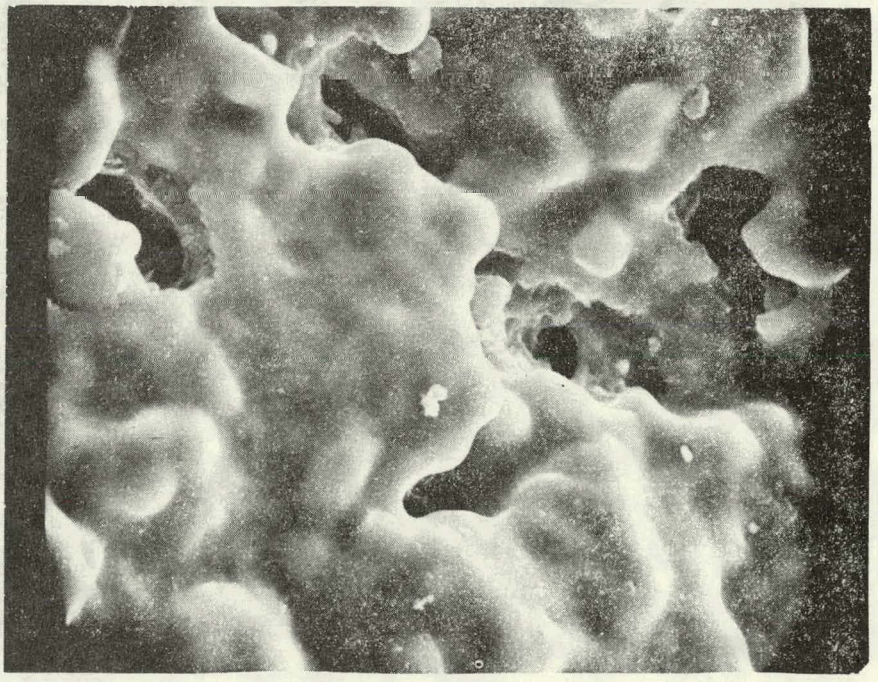


Figure 9. Photomicrograph (SEM 1000x) of MR27, Dipped

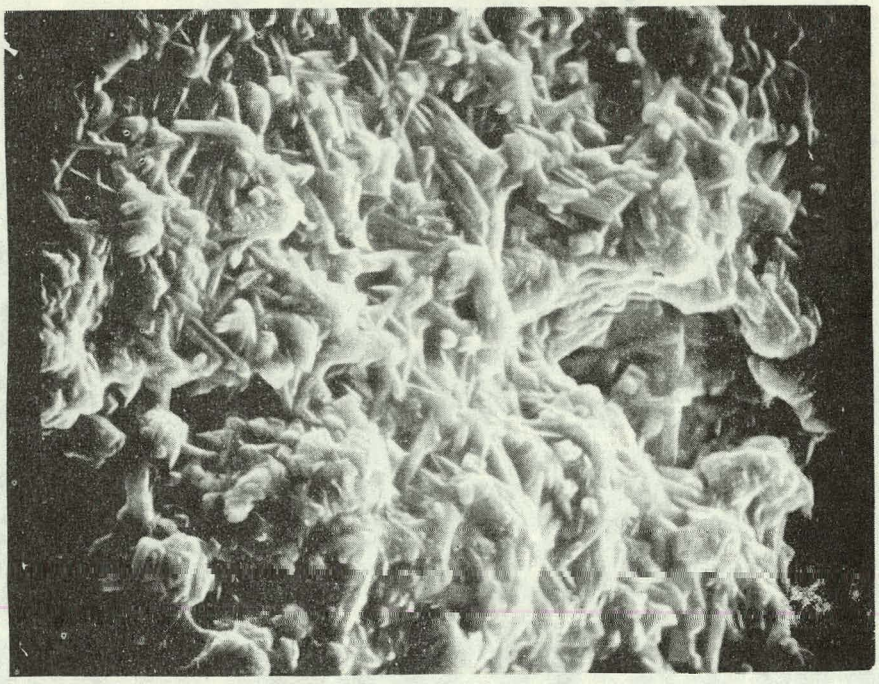


Figure 10. Photomicrograph (SEM 1000x) of Most Recent Batch of MV20, Not Dipped

Figure 11. Photomicrograph (SEM 1000x) of Most Recent Batch of MV20, Dipped

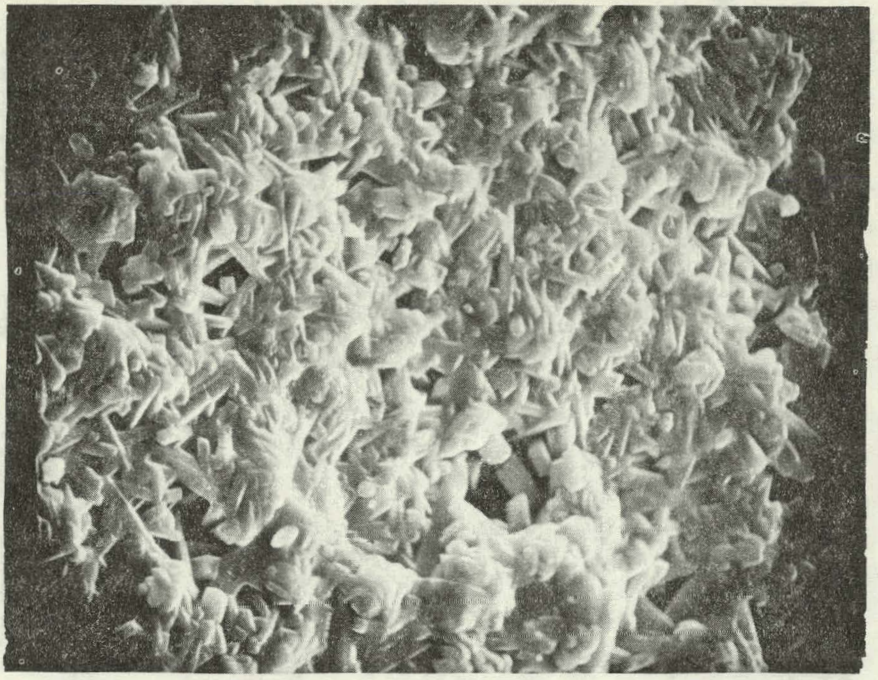


Figure 12. Photomicrograph (SEM 1000x) of Coors S1SI, Not Dipped

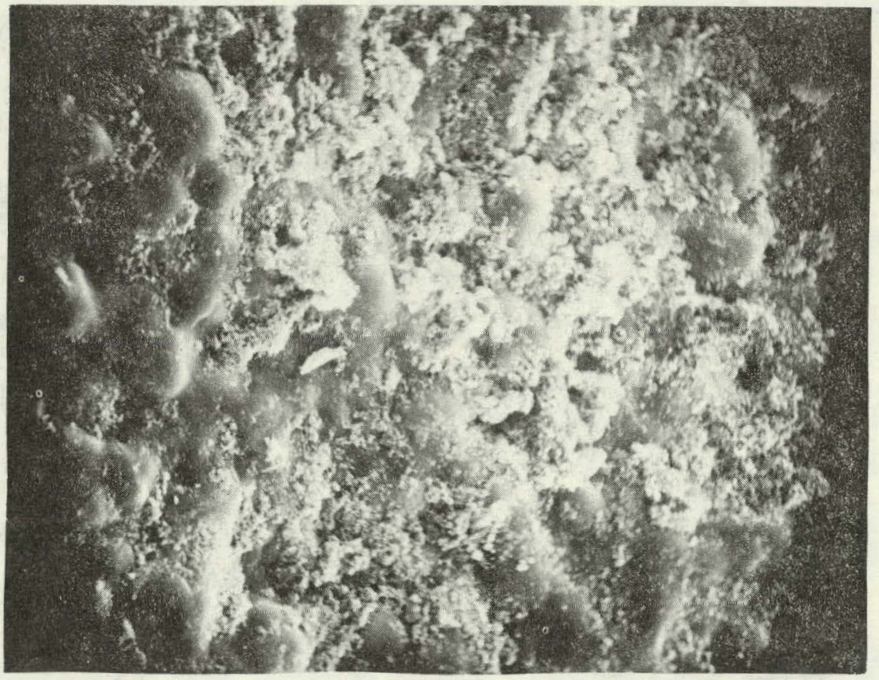


Figure 13. Photomicrograph (SEM 1000x) of Coors S1SI, Dipped

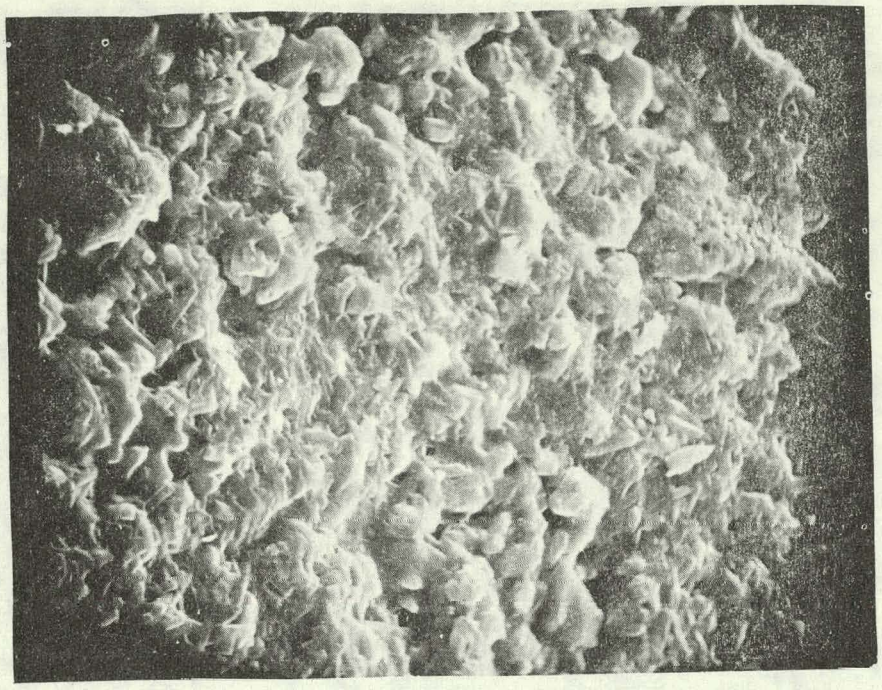


Figure 14. Photomicrograph (SEM 1000x) of Coors S1SI (High Mullite), Not Dipped

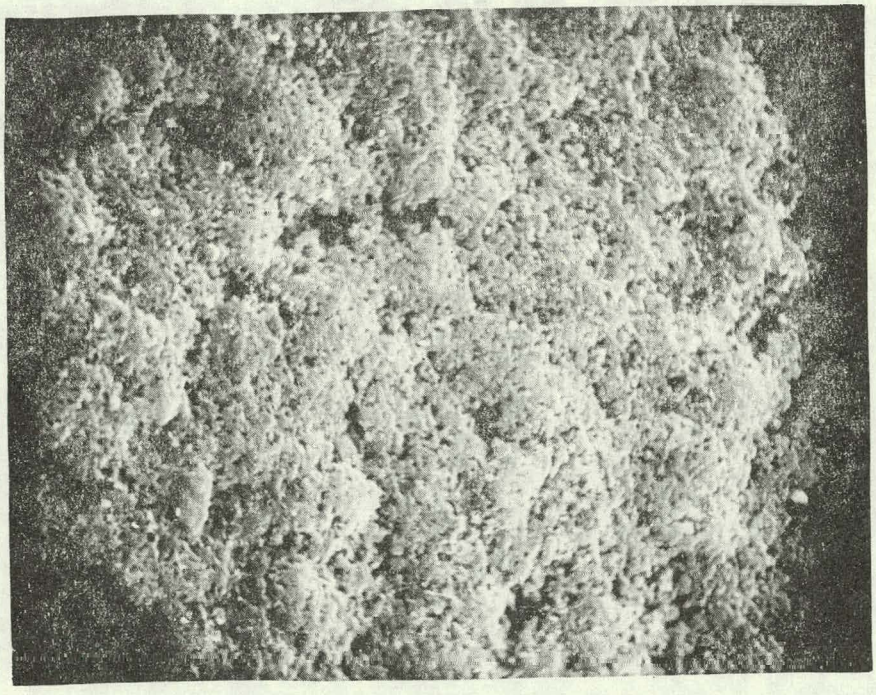


Figure 15. Photomicrograph (SEM 1000x) of Coors S1SI (High Mullite), Dipped

Figure 16. Photomicrograph (SEM 1000x) of Coors S1SI (Glass Property Modification), Not Dipped

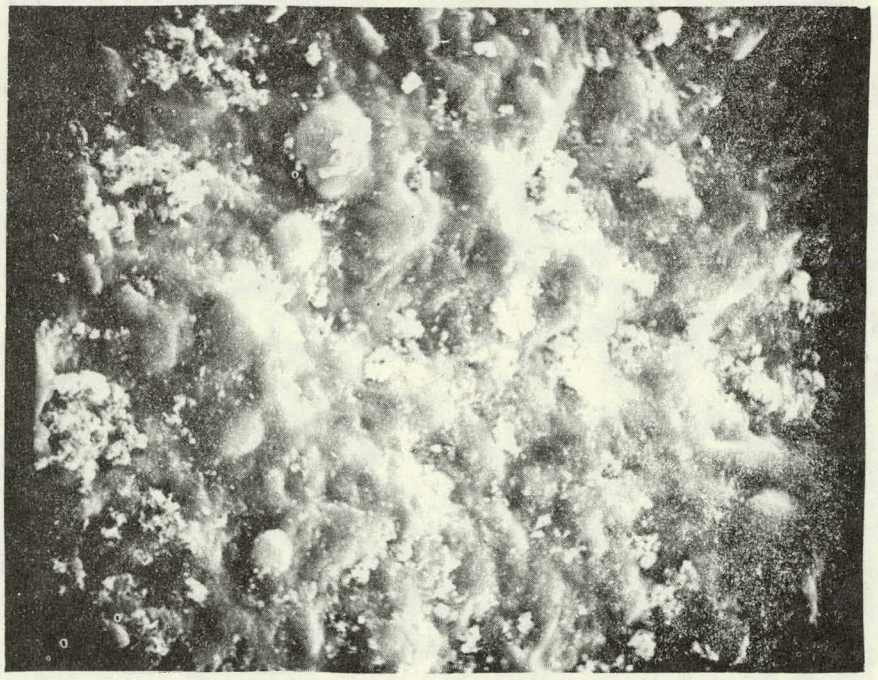


Figure 17. Photomicrograph (SEM 1000x) of Coors S1SI (Glass Property Modification), Dipped

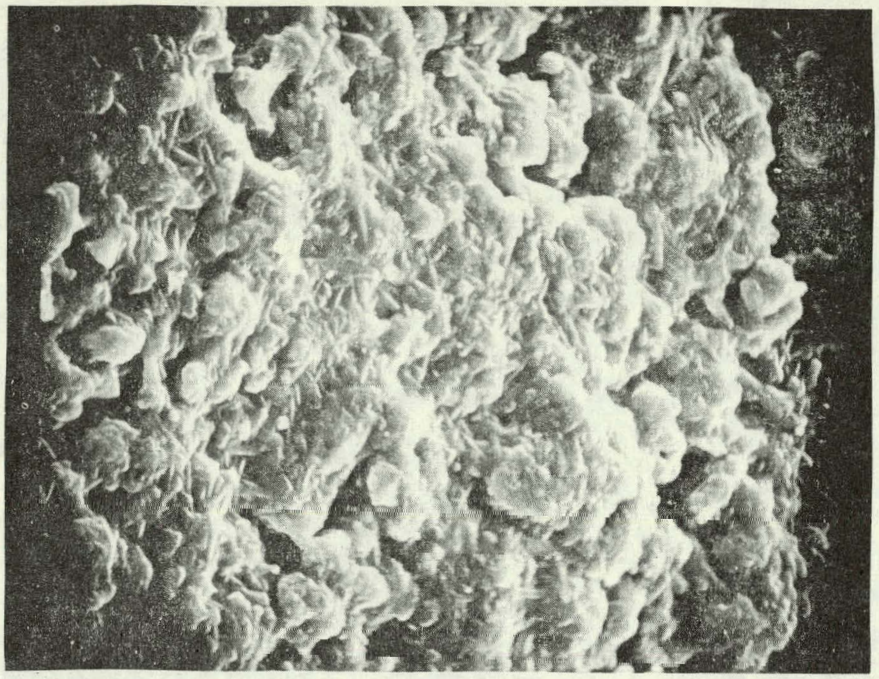


Figure 18. Photomicrograph (SEM 1000x) of Open-Porosity Modification of S1SI, Not Dipped

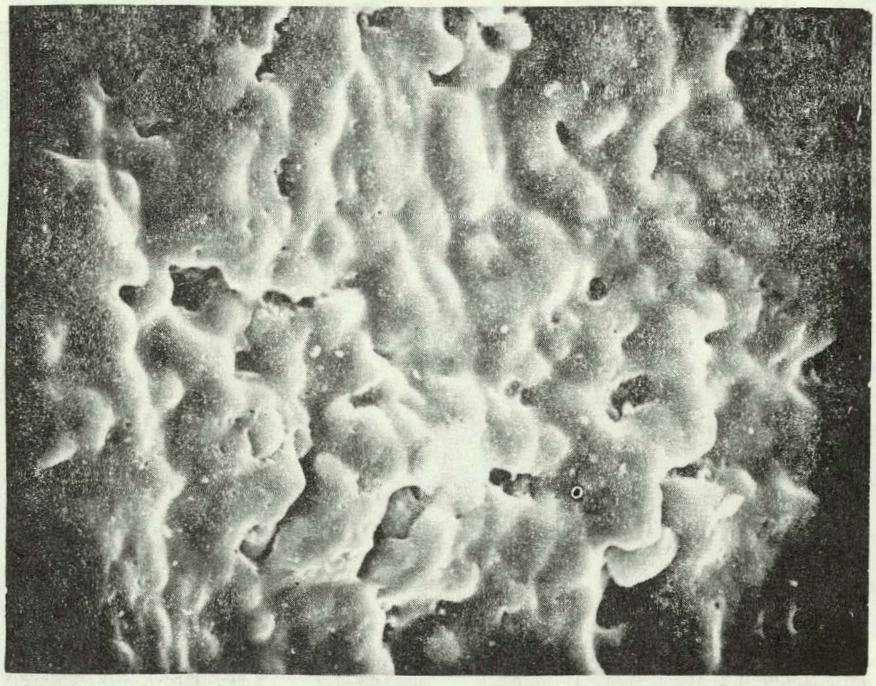


Figure 19. Photomicrograph (SEM 1000x) of Open-Porosity Modification of S1SI, Dipped

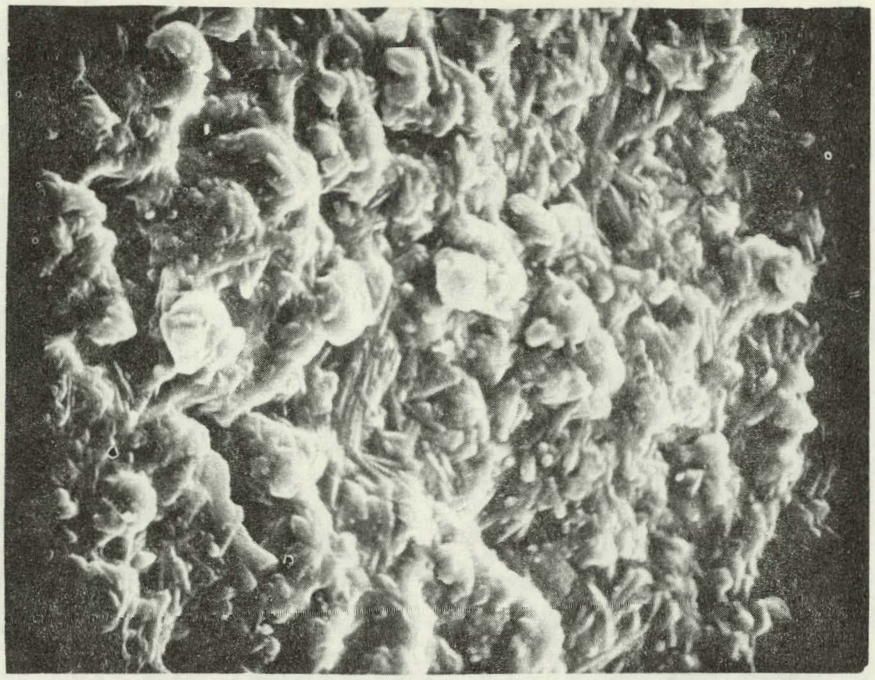


Figure 20. Photomicrograph (SEM 1000x) of High-Purity S1SI, Not Dipped

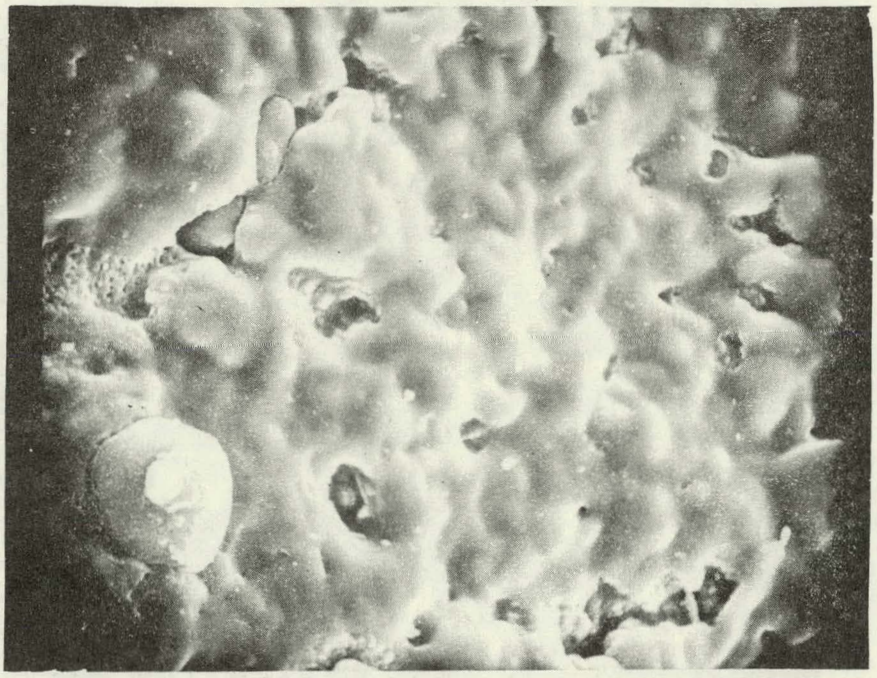


Figure 21. Photomicrograph (SEM 1000x) of High-Purity S1SI, Dipped

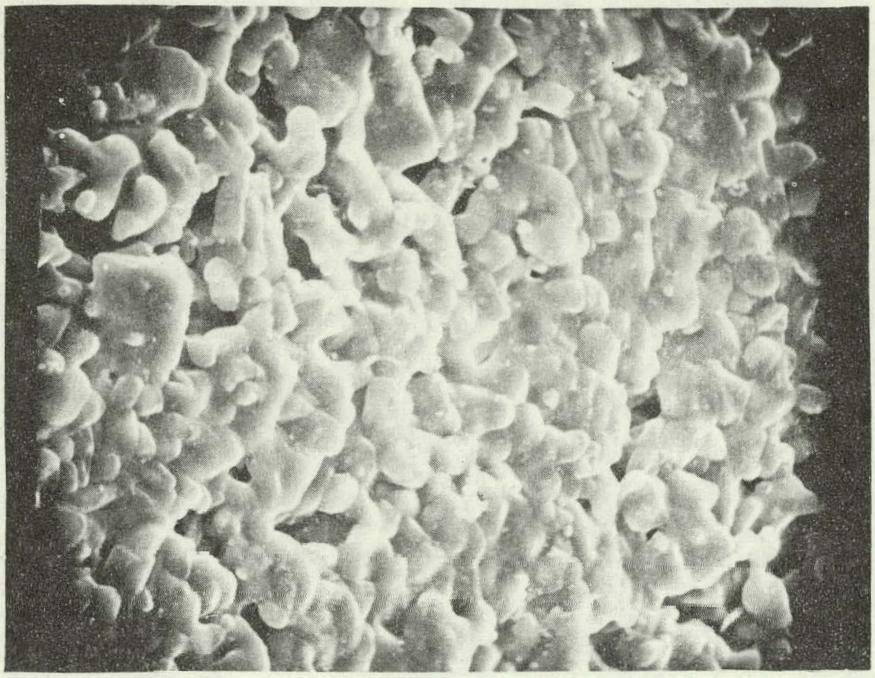


Figure 22. Photomicrograph (SEM 1000x) of Elcctrically-Fused Mullite, Not Dipped

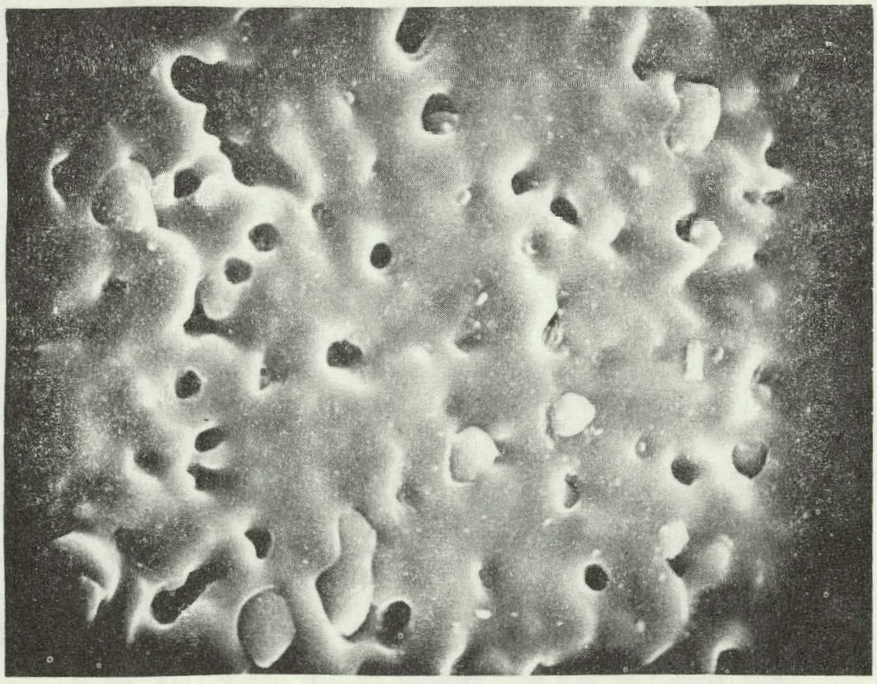


Figure 23. Photomicrograph (SEM 1000x) of Electrically-Fused Mullite, Dipped

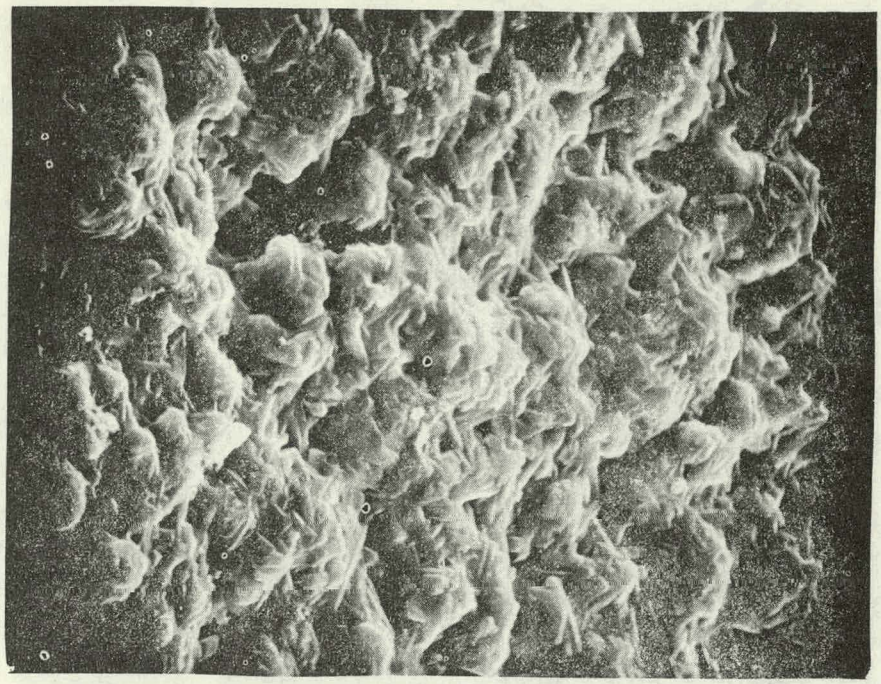


Figure 24. Photomicrograph (SEM 1000x) of Coors Mullite, 1-Meter-Long Substrate, Not Dipped

Figure 25. Photomicrograph (SEM 1000x) of Coors Mullite, 1-Meter-Long Substrate, Dipped

These particular problems were solved by replacing the stainless-steel mounting screws with larger-diameter graphite screws. Additional heating-element insulators containing carbon felt were also added, where needed, to increase the efficiency of the growth chamber.

Two attempts to silicon-coat large (100 cm x 10 cm x 0.1 cm) mullite substrates furnished by Coors failed. The failures were primarily due to substrate breakage. During the first attempt, one end of the large substrate shattered as it was slowly (0.05 cm/sec) entering the substrate heater (see Figure 26). This presumably was a result of the large thermal gradient at the entrance port of this heater.

Two further problems became evident during this run. First, after the silicon charge had melted and the silicon level was being satisfactorily elevated by the quartz displacer, it was observed that the molten silicon did not flow along the quartz trough. This is necessary, of course, to form a meniscus column over which the substrate passes. After increasing the temperature, silicon did eventually flow into the trough. Observations following the run indicated that this flow did not take place, however, until the quartz trough was near its melting point and had subsequently vitrified, allowing the silicon to wet it. The second problem resulted from a superheated region in the trough heating zone. As shown in Figure 26, the surfaces of one portion of both the trough and melt heaters face each other. As a result, these surfaces radiate their energy to each other, causing a higher temperature to be attained in this region. This problem was anticipated, and the walls in this portion of both heaters were made thicker to lower the power density. It is quite apparent, now, that they were not made sufficiently thick. This superheated region eventually melted a portion of the quartz trough, allowing molten silicon to flow between these two heating elements. It was necessary to replace these heating elements and, after doing so, a graphite cap was placed over the two heaters to more uniformly distribute the heat. Also, an additional plate of graphite was cemented to the offending wall of the trough heater to further lower the power density in this zone. Lastly, a moat was machined around the periphery of the above cap to trap molten silicon should there be future runover problems.

The second attempt to silicon-coat a large substrate again failed because of substrate breakage. In this run, one end the substrate was positioned within the substrate heater prior to applying power to the coater. Understandably, this would not solve the thermal gradient problem, but it may be possible to demonstrate the SCIM coating concept on a smaller section of substrate in this manner. Unfortunately, when the substrate heater reached a temperature of approximately 750°C, the substrate broke up in an explosive manner, removing any possibility of silicon coating.

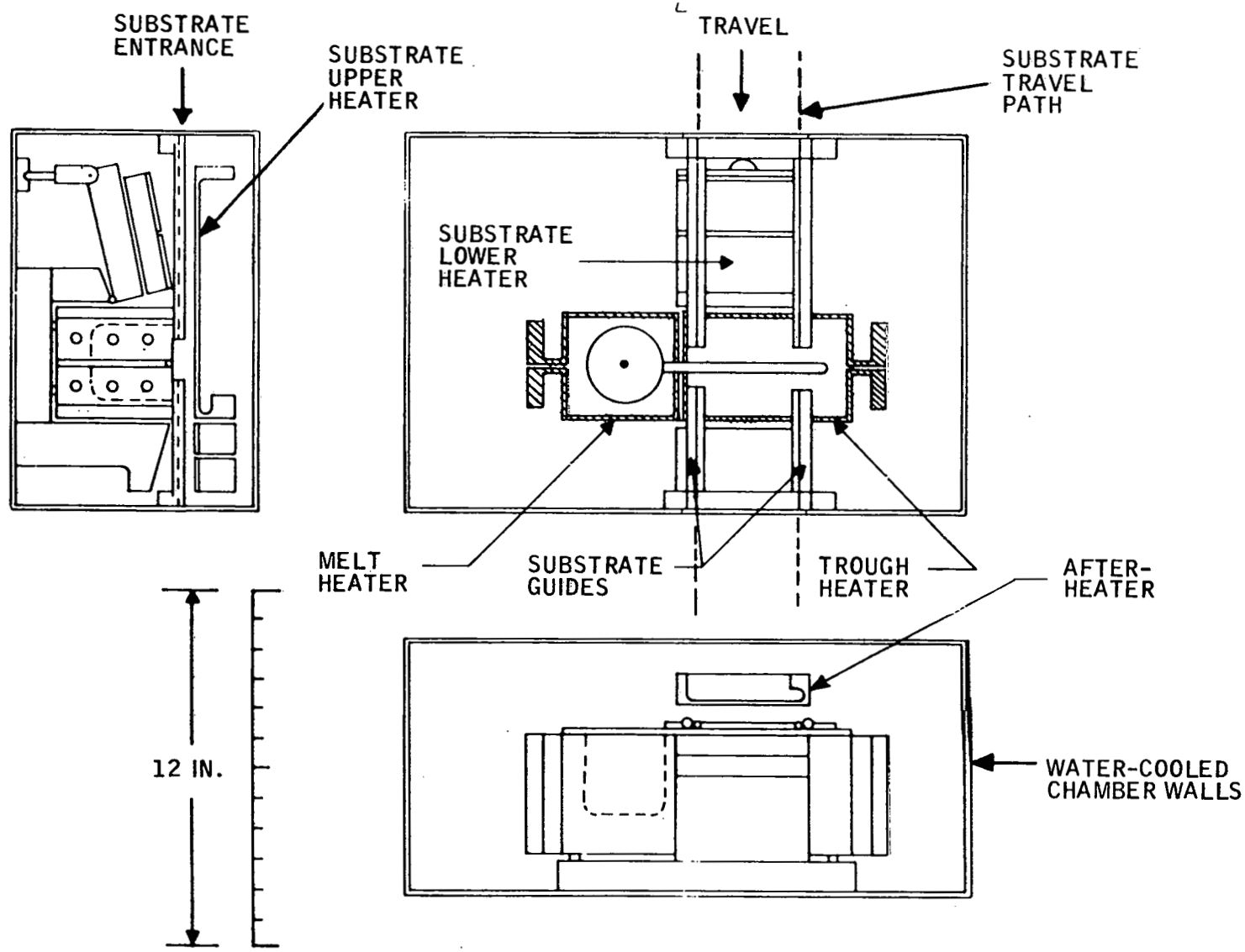


Figure 26. Modified Heating-Element Arrangement in Coating Chamber of SCIM Coater. (Substrate upper heater and after-heater not shown in plan view.)

It becomes obvious that the substrate must experience a less severe temperature gradient if large substrates are to be successfully silicon-coated. To gain insight regarding the acceptable thermal gradient and thermal shock that Coors large substrates will endure, a substrate was passed through a heated (910°C) belt furnace. It was allowed to travel first at a very slow rate and then at the furnace's maximum rate. The substrate endured both passes. At temperatures above 750 to 800°C, mullite should be sufficiently plastic to accommodate larger thermal gradients; therefore, the major emphasis will be to properly adjust the temperature gradient below this temperature.

A thermal profile of the belt furnace is shown in Figure 27. Also shown is the maximum temperature gradient (dT/dx) and thermal shock (dT/dt) the substrate encountered. By way of comparison, a temperature profile was made of the path along which the substrate passes through the silicon coating furnace. The measurements were initially attempted by cementing three transversely-oriented thermocouples (TC) to a thin (0.020 inch)-substrate-size sheet of stainless steel. The three TCs were to indicate transverse temperature differences along the path, and the stainless sheet's function was to simulate the thermal effects of the substrate. As the stainless sheet entered the coating furnace, it warped badly, and the profile run was discontinued. Later it was learned that the thermal conductivity of stainless steel does not closely match that of mullite. Their values are 16.3 W/m°K and 2.5 W/m°K, respectively. Since no other material could be found that was capable of withstanding 1400°C, the TCs were supported by the alumina TC tubing alone in the profile runs that followed. The results of these runs are shown in Figure 28.

Action is being taken to reduce the maximum values of dT/dx and dT/dt by adding a pre-heater and afterheater at the entrance and exit ports of the coating furnace chamber. If such heaters are 12 inches long and provide a linear gradient from room temperature to 700°C, the maximum values of dT/dx and dT/dt would be those shown in Figure 29. Based on the data acquired by passing the substrate through the belt furnace (see Figure 27), these modified values of dT/dx and dT/dt should be acceptable.

MATERIAL CHARACTERIZATION AND EVALUATION (D. Zook, T. Schuller, and R. Hegel)

LBIC Measurements

Ten diodes were measured for uniformity, spectral response, and minority carrier diffusion length (L_D). Table 4 gives the L_D results. Within grains, typical L_D values are 14 to 22 μm at "good" spots.

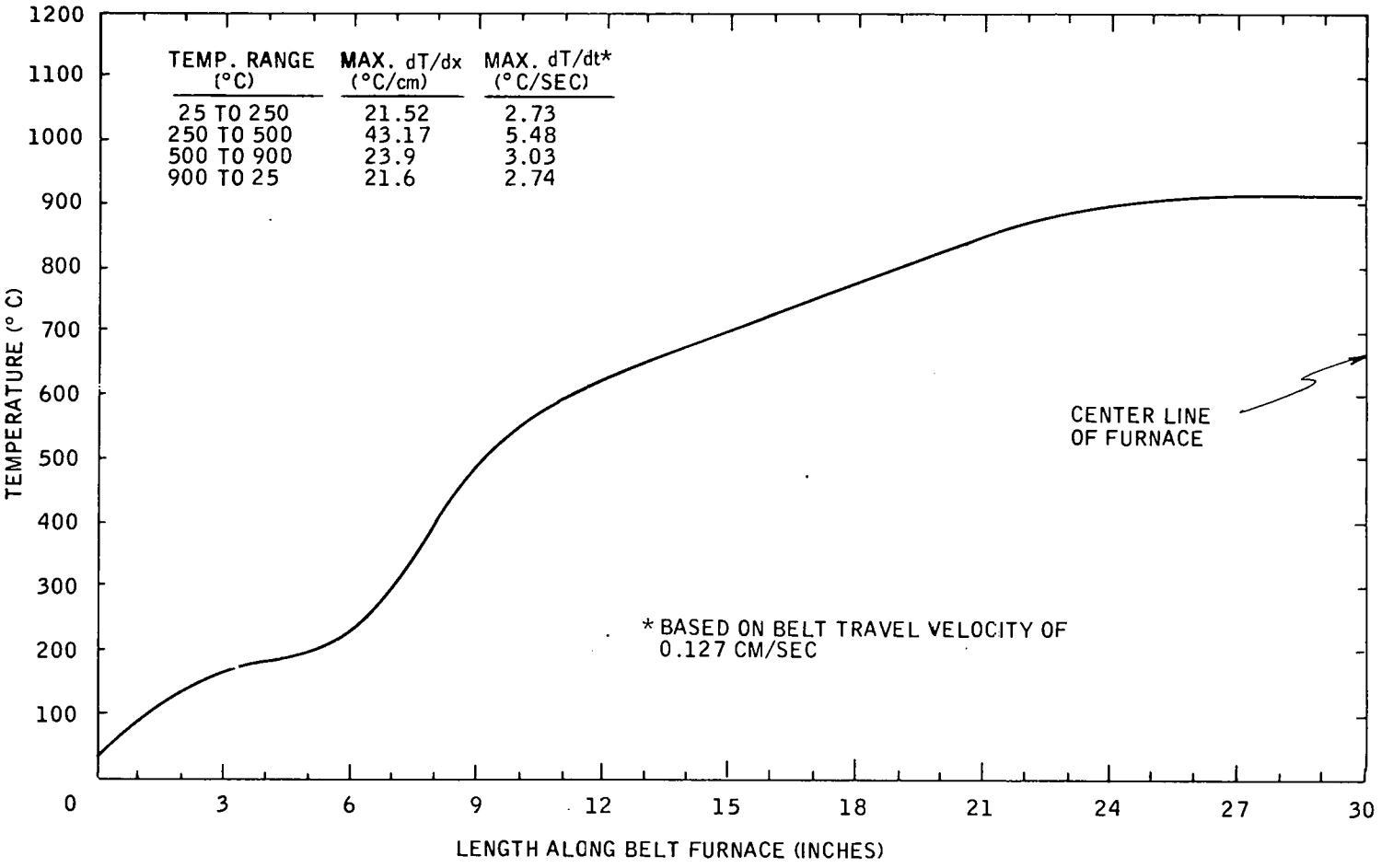


Figure 27. Temperature Profile of First Half of Belt Furnace

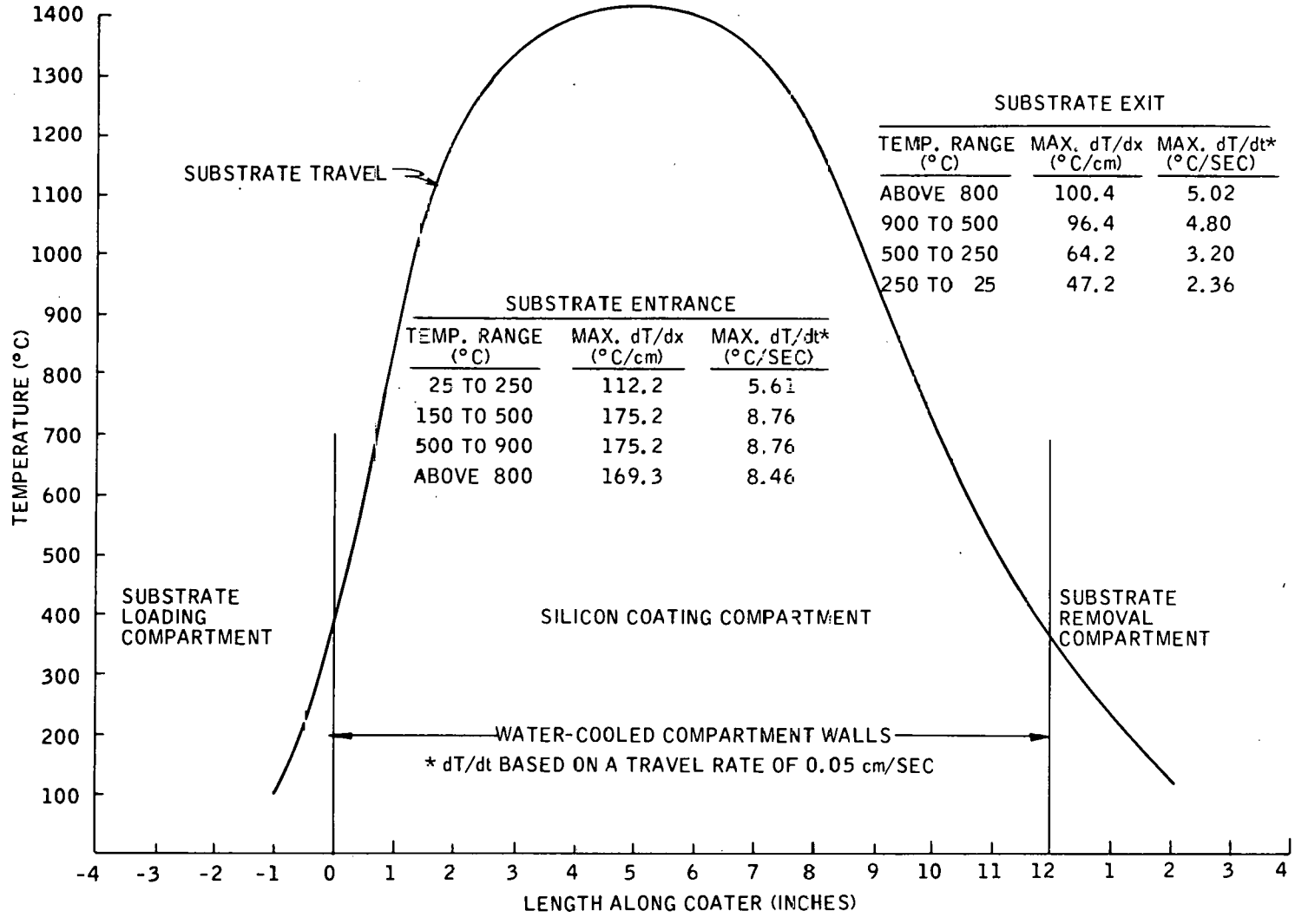


Figure 28. Temperature Profile of Silicon Coating Furnace

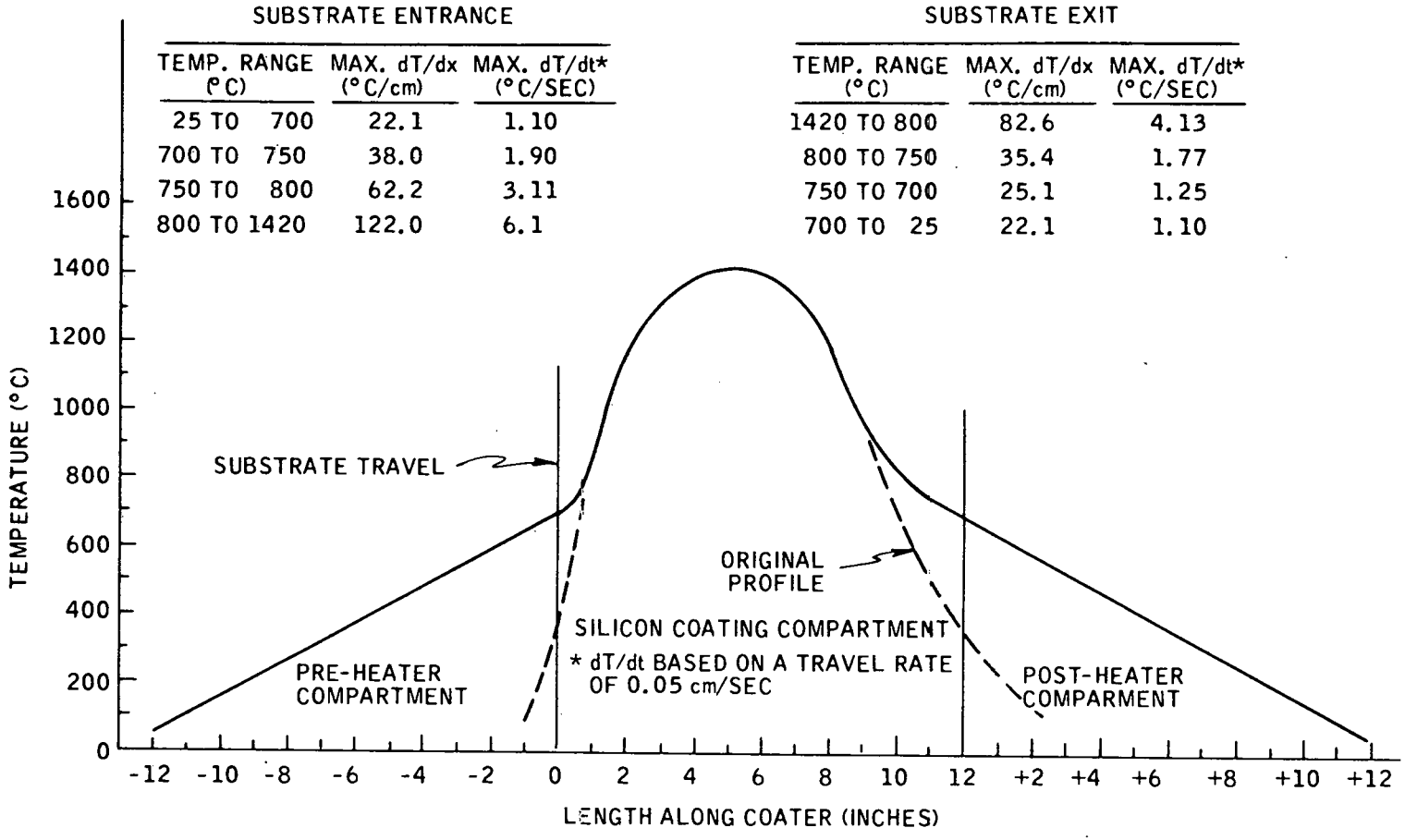


Figure 29. Estimated Temperature Profile of Silicon Coating Furnace after Planned Modification

Table 4. Diffusion Length (L_D) Values for SOC Cells

Cell	L_D (μm)	Comments
85-7-2-P9-B5	18	Good spot
	10	Bad spot (probably dirty)
85-7-2-P9-A6	14	Good spot
	6	Bad spot
P20-A6	340	Single-crystal cells, poor fit to data
P20-B5	305	
96-4B-P21-3	22	Good spot
	2	Bad spot
96-4B-P21-1	18	Good spot
	4	Bad spot
94-3A-P24-3	29	Good spot
	17	Bad spot
94-3A-P24-5	38	Good spot
	9	Bad spot
104-24A-P25-A5	22	Good spot
	4	Bad spot
104-2B-P25-2	16	Good spot
	12	Average spot
	3	Bad spot

A scan of diode 94-3A-P24-5 was examined in more detail in an effort to correlate the minima in current response with observed features. Micrometer readings were taken at the position of each minima, then the scan was repeated and a visual observation was made using reflected light. At each minima there is an observable boundary which scatters light significantly. This result suggests that it may be possible to characterize the crystallinity of the material by measuring scattered light.

In deriving the values of L_D, the stress-relieved (SR) literature values of α were used. The "good" and "bad" spots were chosen at representative regions where the current response appeared to be uniform.

For our convenience in measurement, a second LBIC system is being set up in our own laboratory, using essentially the same setup as in the original system.

Device Performance (D. Zook. B. Grung, R. Hegel, T. Heisler, S. Znambroski)

Summary of Solar Cell and Photodiode Performance -- During the period, no significant modifications in fabrication procedures were made. The possibility of using a thick sputtered silver film to replace both the nickel film and the indium solder was investigated, but was not found to be feasible. A number of cells were fabricated, with the results shown in Table 5. Several significant conclusions can be drawn:

- Cells which have been etched with Wright's to show twin boundaries and dislocations do not appear to suffer any loss of performance. This is good because diodes made on etched substrates can then be used for LBIC measurements, and the response can be correlated with dislocation densities.

- Three different base dopings (N_A) were used in the cells evaluated. A correlation between doping and short-circuit current (J_{sc}) would indicate the effect of doping on lifetime, but such a correlation is not obvious from the data.

- There are wide variations in the base sheet resistance (ρ_{sb}) as indicated by the four-point probe method. These variations appear to be too large to be explained as thickness variations and may be due to mobility variations. At any rate, there does seem to be some correlation between ρ_{sb} and the cell fill factor (FF).

- A new pattern with total area of 4 cm^2 and active area of 2.77 cm^2 was made up, using a closer electrode spacing than the previous pattern. Because of the variations in ρ_{sb}, there was no noticeable improvement in FF.

- Dip run 104 was the first run made after the new heating elements were installed and the system was thoroughly cleaned. Cell 104-7B-P25 showed the best performance to date for an uncoated 1-cm^2 cell. This indicated that the contamination problem was solved. One note of caution, is in order, however, because these cells appeared to have an unusually black color, and may have had some type of inadvertent AR coating which accounted for their better performance. This is being investigated.

- It is significant that cells made from dip 104-23 were about as good as those from 104-7, this indicated that cumulative contamination of the melt by the mullite did not occur.

Table 5. Summary of Cell and Diode Performance

Diode	Base ρ_{sb} (Ω/□)	N_A ($10^{16}cm^{-3}$)	Number of Diodes (avg)	Active Area (cm^2)	ρ_s (Ω/□)	V_{oc} (V)	J_{sc} (mA/cm^2)	FF	Eff. (%)	Max. Eff. (%)	Comments
P21	---	---	14	0.078	39	0.53	24.8	0.724	9.5	9.9	
P22	---	---	14	0.078	39	0.54	24.7	0.719	9.7	10.4	
P24	---	---	14	0.078	41	0.53	25.8	0.684	9.4	10.2	Single-crystal control cells
P25	---	---	14	0.078	---	0.53	27.5	0.692	10.1	10.6	
P26	---	---	1	1.05	---	0.54	23.6	0.613	7.9	7.9	
86-5A-P21	66-152	1.2	1	2.4	42	0.48	13.7	0.564	3.7	3.7	
86-7A-P21	112-141	1.2	1	1.0	42	0.47	18.4	0.532	4.6	4.6	Sample reworked Seeded growth
86-7B-P21	112-141	1.2	6	0.078	42	0.35	23.8	0.564	4.6	5.6	
91-4B-P19	103-235	1.2	7	0.078	---	0.47	19.6	0.638	6.0	7.2	
91-6B-P19	63-235	1.2	7	0.078	53	0.30	19.9	0.476	2.8	4.8	
91-9A-P19	192, 310	1.2	1	1.0	---	0.46	20.0	0.533	4.9	4.9	
93-3A-P22	43-88	1.2	1	1.05	43	0.38	17.7	0.628	4.0	4.0	Seeded growth etched surface
93-3B-P22	42-88	1.2	14	0.078	43	0.46	22.1	0.610	6.2	8.3	Sample reworked
93-6-P22	27-64	1.2	1	2.9	42	0.40	14.6	0.401	2.4	2.4	
94-3-P24	75-170	0.9	1	3.085	50	0.513	21.04	0.551	6.05	6.05	Seeded growth etched surface
94-3A-P24	75-170	0.9	6	0.084	50	0.50	24.6	0.657	8.1	9.0	
95-3A-P24	136-411	0.9	1	1.05	51	0.50	20.8	0.487	5.0	5.0	
95-3B-P24	136-411	0.9	6	0.084	51	0.47	22.4	0.582	6.1	7.15	
95-4A-P24	87-263	0.9	6	0.085	42	0.48	23.3	0.640	7.15	7.8	
96-4A-P21	101-271	0.9	1	1.05	44	0.48	17.7	0.628	5.4	5.4	
96-4B-P21	101-271	0.9	7	0.078	44	0.43	17.7	0.548	4.4	6.2	
97-6-P24	80-143	0.9	7	0.078	49	0.42	21.7	0.473	4.4	7.8	
104-2A-P25	180-485	0.6	1	1.05	49	0.48	19.8	0.508	4.9	4.9	
104-2B-P25	180-485	0.6	7	0.078	49	0.47	21.1	0.602	6.0	6.0	
104-3A-P25	113-375	0.6	14	0.078	53	0.48	20.5	0.606	5.9	6.6	
104-7A-P25	68-140	0.6	1	3.08	45	0.51	22.6	0.523	6.0	6.0	Sample reworked
104-7B-P25	68-140	0.6	1	1.05	45	0.51	21.8	0.654	7.2	7.2	
104-9A-P25	150-338	0.6	1	2.47	52	0.50	21.0	0.435	4.5	4.5	
104-9B-P25	150-338	0.6	14	0.078	52	0.49	22.5	0.656	7.2	8.1	
104-24A-P25	44-62	0.6	14	0.078	71	0.40	20.1	0.551	4.7	8.0	Material defects
104-24B-P25	44-62	0.6	13	0.080	71	0.48	19.7	0.644	6.1	7.3	
104-24C-P25	44-62	0.6	13	0.080	71	0.49	19.7	0.625	6.7	7.9	
105-2A-P26	62-153	1.2	1	2.77	52	0.50	19.3	0.541	5.2	5.2	
105-2B-P26	62-153	1.2	1	1.05	52	0.50	18.7	0.654	6.1	6.1	
105-2C-P26	62-153	1.2	7	0.078	52	0.49	18.5	0.675	6.5	7.0	
105-7A-P26	256-542	1.2	1	2.77	49	0.48	15.7	0.541	4.1	4.1	
105-7B-P26	256-542	1.2	1	1.05	49	0.47	14.8	0.463	3.2	3.2	
105-7C-P26	256-542	1.2	7	0.078	49	0.43	15.6	0.415	2.9	2.9	

CELL DEVELOPMENT (B. Grung, D. Zook, R. Hegel, and T. Heisler)

Slotted Cell Development

Solar cells were fabricated on five slotted substrates. The best cell (see Table 6) had an efficiency of 4.3 percent (uncoated) and an active area of 5 cm^2. Neither the slot widths nor the spacings were optimized for device performance. This preliminary result indicates clearly the technical feasibility of the slotted substrate approach.

Table 6. Summary of Cell Performance on Slotted Substrates (Without AR Coating)

Diode	Base ρ_s ($\Omega/\square$)	N_A ($10^{16}cm^{-3}$)	Number of Diodes (avg)	Active Area (cm^2)	ρ_s ($\Omega/\square$)	V_{oc} (V)	J_{sc} (mA/cm^2)	FF	Eff. (%)	Max. Eff. (%)	Comments
P-28	---	---	1	1.05	---	0.54	24.9	0.60	8.0	8.0	Single crystal control cells
P-29	---	---	1	13.1	34	0.56	27.6	0.53	8.1	8.1	
P-29B	---	---	1	13.1	34	0.56	26.9	0.58	8.6	8.6	
105-4-P27	50-200	1.2	1	5.07	58	0.47	17.8	0.51	4.3	4.3	Slotted substrates
108-12-P28	90-220	1.2	1	8.9	57	0.36	13.8	0.29	1.5	1.5	
108-13-P28	70-230	1.2	1	10.38	48	0.45	13.2	0.37	2.2	2.2	
109-10-P29	75-130	0.6	1	12.2	43	0.48	18.8	0.38	3.4	3.4	
109-12-P29	30-90	0.6	1	13.1	31	0.34	15.3	0.26	1.3	1.3	

A new fabrication procedure was required for the slotted substrates because the base contact was removed from the top surface of the solar cell and added to the back surface. The new fabrication procedure is as follows:

1) Perform phosphorus diffusion for 20 minutes at 85°C. This diffusion forms the n^+ emitter region of the completed solar cell. After the phosphorus diffusion, the resulting heavily-doped silicon-dioxide layer is then removed by hydrofluoric (HF) etch.

2) Sputter-deposit platinum on the back surface. The platinum is used to form an ohmic contact to the lightly-doped base region.

3) Bake for 2 hr at 100°C. This bake removes any residual liquids (i.e., water) that remain in the porous ceramic substrate after the previous process steps. Without this bake, the silicon may spall off the substrate during the subsequent high-temperature process, as was demonstrated during our first attempt to fabricate solar cells on slotted substrates.

4) Sinter for 30 minutes at 600°C. This forms a platinum-silicide ohmic contact to the base region.

5) Sputter-deposit nickel on both the top and bottom surfaces. On the top surface, the nickel is selectively etched to form the contact grid to the n^+ emitter region. On the bottom surface, the nickel provides a good electrical connection to the thin platinum-silicide layer.

6) Indium-solder the deposited nickel. This completes the ohmic contacts to the emitter and base regions of the solar cell.

7) Plasma-etch the outer regions of the solar cell. This defines the total area of the solar cell, which was between 5 to 10 cm^2 for the preliminary cells on slotted substrates.

The cells fabricated by the above process show considerable potential, as has been noted. New, higher-efficiency cell configurations are being designed and fabricated at the present time.

Antireflective Coatings (B. Grung and R. Hegel)

A total of 21 solar cells having antireflective (AR) coatings have been fabricated using our new coating system. The average efficiency increased by approximately 33 percent. The measured characteristics for SOC solar cells are given in Table 7; the corresponding characteristics for single-crystal solar cells are given in Table 8. Up to this point, no attempt has been made to optimize the coating conditions.

The fill factors of all 21 solar cells were less than 0.60. With our processing techniques, we should be able to produce fill factors greater than 0.70. During the next quarter, we will try to determine the cause for the low fill factors.

The new AR coating system is a diffusion-pumped evaporation system with a silicon-oxide evaporation source from Vacuum Atmospheres Company. This is a design with which we had good experience in coating manganese-bismuth films. The thickness is monitored with an Inficon thickness monitor. The nominal thickness we have used is 800Å, which gives the desired deep blue color.

Table 7. Antireflection Coating Enhancement of Cell Performance (SOC Material)

SOC Cell	Area (cm^2)	V_{oc}	J_{sc}	FF	% Eff.	Percent Increase
91-10F-P19 (before)	1.05	0.485	16.62	0.567	4.57	27
(with AR)		0.494	20.76	0.565	5.80	
96-4A-P21 (before)	1.05	0.493	18.18	0.641	5.75	22
(with AR)		0.498	21.71	0.649	7.02	
R1720-59 (before)	1.05	0.510	19.05	0.701	6.81	36
(with AR)		0.519	25.71	0.696	9.29	
75-15-PH9-01 (before)	3.08	0.506	18.18	0.448	4.13	29
(with AR)		0.512	22.04	0.473	5.34	
65-7F-66 (before)	1.05	0.514	18.38	0.682	6.45	47
(with AR)		0.521	28.33	0.621	9.5	
104-7A-P25 (before)	3.08	0.51	23.0	0.51	5.8	21
(with AR)		0.51	30.0	0.46	7.0	
105-7A-P26 (before)	2.80	0.47	16.0	0.53	4.0	43
(with AR)		0.48	22.0	0.54	5.7	
105-7B-P26 (before)	1.05	0.46	15.0	0.46	3.1	29
(with AR)		0.47	19.0	0.46	4.0	
105-2B-P26 (before)	1.05	0.50	18.0	0.65	6.0	30
(with AR)		0.51	25.0	0.61	7.8	
106-2B-P26 (before)	1.05	0.49	17.0	0.60	5.2	42
(with AR)		0.50	25.0	0.58	7.4	
106-9A-P26 (before)	1.05	0.45	16.0	0.43	3.3	42
(with AR)		0.47	22.0	0.44	4.7	
						Average Increase = 34%

After the AR coatings, the appearance of the single-crystal cells was quite uniform in color. However, there were large variations in appearance of the SOC cells after AR coating and some of them did not have the required blue color. The reasons for the variation are not clear, and those with poor appearance were not included in the averages.

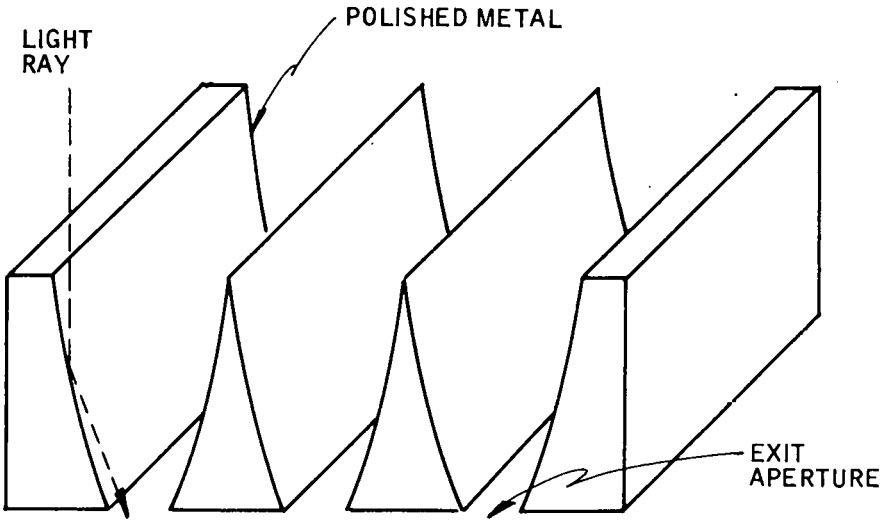
Table 8. Antireflection Coating Enhancement of Cell Performance (Single-Crystal Material)

Single-Crystal Diodes	Area (cm^2)	V_{oc}	J_{sc}	FF	% Eff.	Percent Increase
P21 - 1B (before)	0.0525	0.541	26.5	0.745	10.68	43
(with AR)		0.567	33.5	0.805	15.31	
P21 - 5B (before)	0.045	0.545	27.1	0.748	11.06	25
(with AR)		0.562	33.3	0.739	13.85	
P21 - 6A (before)	0.045	0.556	26.4	0.747	10.99	48
(with AR)		0.555	37.1	0.789	16.26	
P21 - 2A (before)	0.045	0.558	26.0	0.756	10.98	32
(with AR)		0.554	36.9	0.710	14.53	
P22 - 1B (before)	0.0525	0.546	25.9	0.755	10.67	21
(with AR)		0.542	33.52	0.708	12.87	
P22 - 5B (before)	0.045	0.543	26.0	0.733	10.35	13
(with AR)		0.543	33.6	0.640	11.66	
SC - 71A (before)	1.05	0.543	23.62	0.615	7.89	39
(with AR)		0.55	33.3	0.599	10.98	
94-3 (before)	3.1	0.50	21.0	0.56	5.9	25
(with AR)		0.51	27.0	0.54	7.4	
P-26 (before)	1.05	0.54	23.0	0.62	7.7	40
(with AR)		0.55	37.0	0.54	10.8	
						Average Increase = 33%

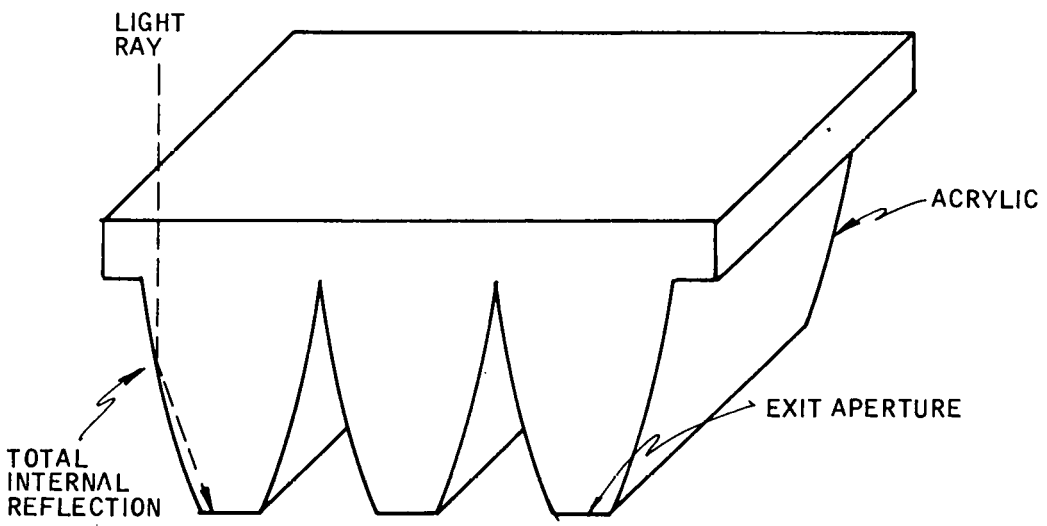
Novel Device Development (B. Grung, D. Zook, and S. Znameroski)

Our objective is to develop novel devices using the SOC substrates fabricated at Honeywell. At the outset, we plan to investigate 1) the benefits of combining an integral optical coupler with a high-voltage cell structure, and 2) the feasibility of forming a pn junction by using doped carbon as the diffusion source. The first was suggested by G. Turner and the second by Li-Jen Cheng of JPL.

The integral optical coupler is a concentrator device having a concentration ratio in the range of 2 to 10. This device is based on the compound parabolic concentrator devices developed by Winston, et al. The integral optical coupler can have two forms as illustrated in Figure 30. The first form involves reflections from a metal surface; the second form involves total internal reflections. In both devices, the solar cell material is located primarily in the regions directly below the exit apertures.



a) COMPOUND PARABOLIC CONCENTRATOR



b) DIELECTRIC COMPOUND PARABOLIC CONCENTRATOR

Figure 30. Integral Optical Coupler

The high-voltage cell is illustrated in Figure 31. This cell is fabricated as follows. Carbon stripes are deposited on the ceramic substrate. The substrate is then dipped so that the carbon stripes are perpendicular to the surface of the melt. The resulting silicon stripes are then used to form the completed structure. The integral optical coupler and the high-voltage structure can be easily combined as shown in Figure 32. For this figure, the integral optical coupler is a cylindrical, trough-like dielectric compound parabolic concentrator having a concentration ratio of 3. As compared with a conventional SOC solar cell structure, the combined device structure has two novel features. First, it allows efficient collection of incident light even though all metal contacts are located on the top surface. That is, the incident light is concentrated primarily on the solar cell material. Second, the combined device can produce an output voltage in the range of 5 to 10 volts.

Doped carbon is being developed as a diffusion source for forming pn junctions. If this source proves to be feasible, then several novel devices, such as the tandom cell, will be investigated at a later point.

CONDUCTIVE INTERFACE DEVELOPMENT

Diffusions from Doped Carbon

During the quarter, attention was directed to the formation of a p^+ back region for the SOC cells. The inaccessibility of the back region or ceramic side of the silicon makes it impossible to use conventional diffusion methods. New diffusion processes are now under investigation. One such process, which we shall refer to as a doped-carbon process, makes use of the carbon layer as a dopant source. Dopants such as boron or aluminum are either incorporated in the carbon or in a layer between the carbon layer and the ceramic.

To date, two diffusion sources have been tried using the doped carbon method on single-crystal wafers with a glassy carbon (GC) film. The first incorporated the use of a mixture of amorphous boron (400Å average particle size) and a GC polymer. This mixture was spin-coated into the surface of an n-type silicon wafer and diffused at 1000°C for 4 hours. A p-type surface of 135 Ω/□ sheet resistivity resulted. The other doping source was ammonia borane (NH_3BH_3). The dopant was mixed with the carbon resin, was coated on a p-type wafer of 131 Ω/□ sheet resistivity and was diffused at 1100°C for 40 minutes. This resulted in a p-type surface of 4.8 Ω/□ after carbon removal, indicating significant diffusion had occurred.

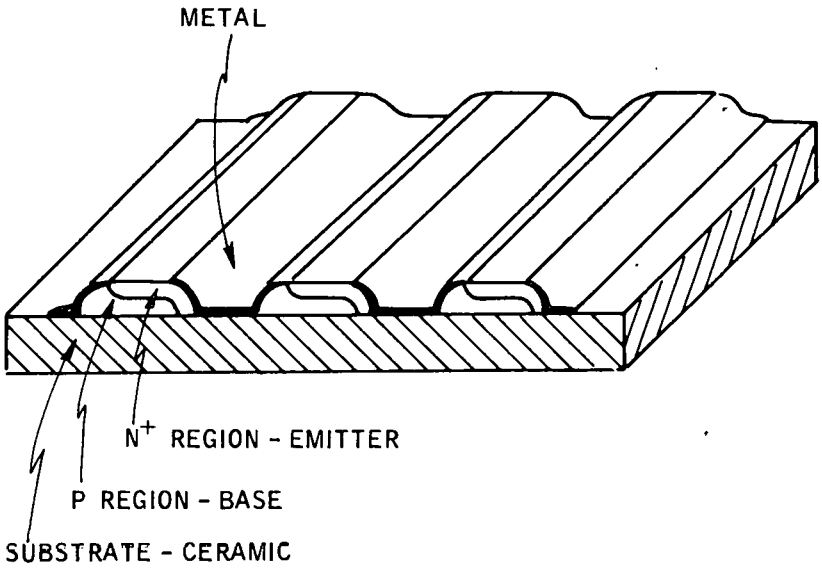


Figure 31. High-Voltage Cell

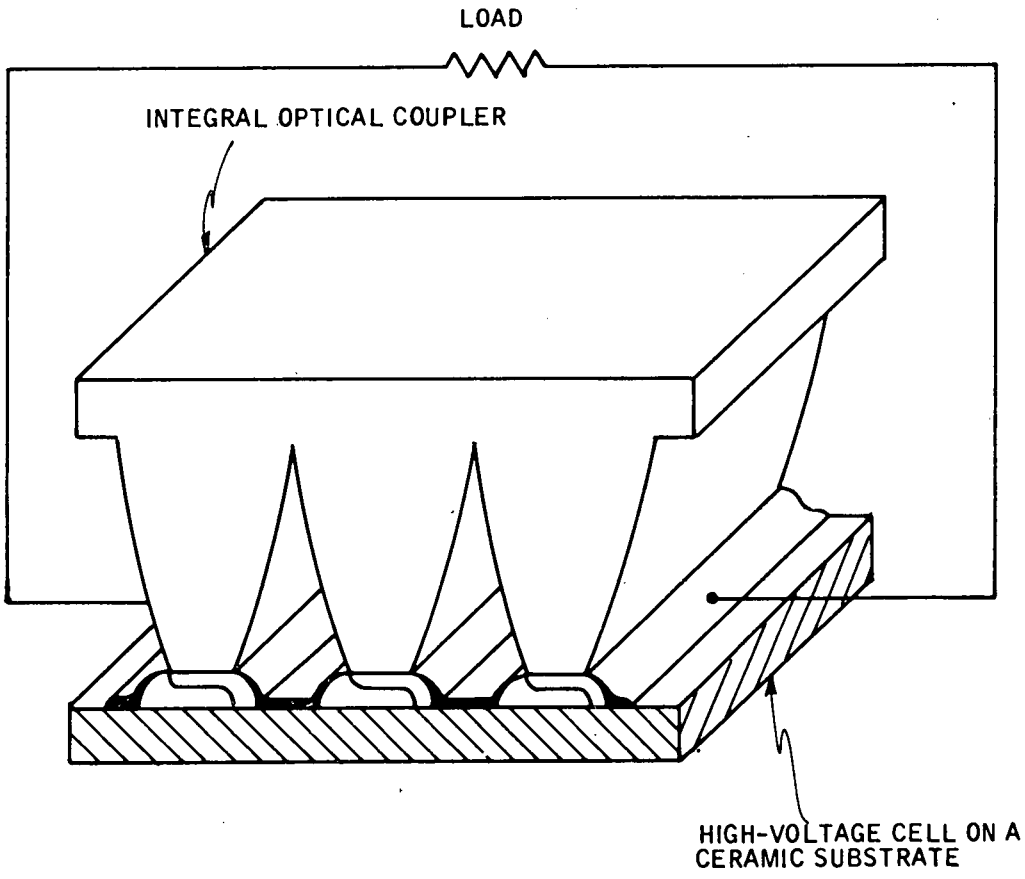


Figure 32. Combined Integral Optical Coupler/High-Voltage Cell Device

The use of ammonia borane as a dopant is very promising. The above diffusion process has been repeated with slight modifications of conditions and resulted in very similar results. One such modification was to take a GC-coated wafer (wafer ρ_s = 135 Ω/□), coat the carbon surface with a film of the doped polymer, and diffuse. This resulted in a p-type diffused surface of 6.7 Ω/□ after carbon removal. The surface concentration (C_s) for a diffused wafer from an ammonia borane polymer mixture was calculated to be approximately 10^{21} atoms/cm^3, so that the diffusion appears to be the same as conventional methods using oxide sources to produce p^+ layers.

SILICON-ON-CERAMIC SOLAR CELL OPTIMIZATION (S. B. Schuldt)

The solar cell electrode geometry is one aspect of the total solar cell design analysis which should help to determine maximum cell efficiency subject to practical limits on design parameters. Optimization of solar cell electrode geometry requires specification of the equivalent circuit parameters, since these have a contributing impact upon the efficiency of the cell. This report deals in particular with the striped grid electrodes and the collecting electrode at right angles to them. The collecting electrode gathers current not only from the grid electrodes but also directly from the active cell areas. Hence, the equivalent circuit must account for a division of the photogenerated current, i_n into a portion, i_c, to the collecting strip, and i_G to the grid strips. An exact analysis is made here which shows that a previous model[5] overestimates i_c compared with i_G. Also, equivalent resistance and power dissipation are rigorously determined from the analysis.

A solar cell consists of repeated rectangular unit fields, each surrounded on three sides by metal strips, as shown in Figure 33. The equivalent circuit for the diffused layer of any one unit (for the base layer also, if similar back geometry is used) is shown in Figure 34. Current WSJ_n generated by the sunlight flows through R_c and R_G to ground. R_c represents the resistance of the diffused region for carriers flowing to the top contact strip, and R_G is the resistance of the diffused region for carriers flowing to the two grid strips. Figure 34 is an essential part of a larger equivalent circuit considered by Handy.[5]

The problem is to determine

$$P = (i_c + i_G)^2 \qquad R = i_n^2 R \tag{1}$$

where P is the electrical power dissipation per unit field in the diffused layer. Another important quantity is $\bar{V}$, the potential with respect to ground, averaged over the unit field area. In the proof shown at the end of this discussion, it is shown that

$$P = i_n \bar{V} \tag{2}$$

so that an equivalent definition of R from (1) and (2) is

$$R = \bar{V}/i_n \tag{3}$$

The quantity V has further significance[6] as the correct parasitic voltage in the lumped model of the solar cell junction. The resistances R_c and R_G have no special interest, since the important quantities, i_c, i_G, R, $\bar{V}$, and P, are determined without them.

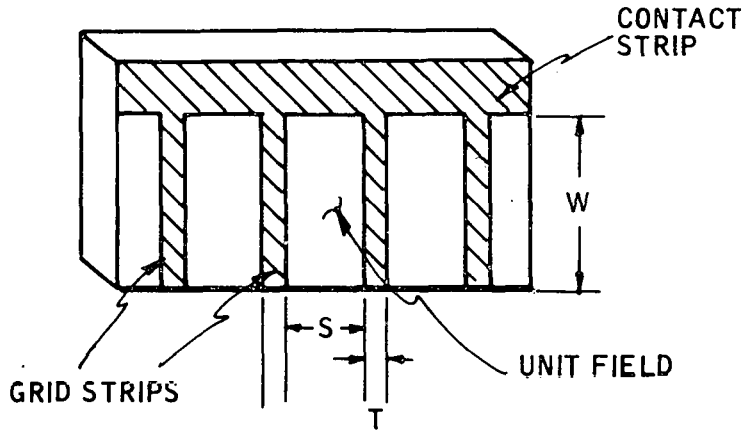


Figure 33. Solar Cell Representation. Usually the unit field includes a grid strip and has area (S + T) x W. In this report, the unit field is S x W.

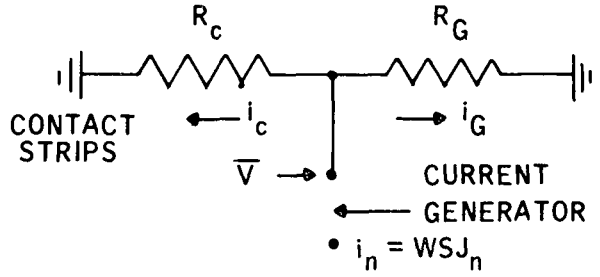


Figure 34. Lumped Equivalent Circuit Model for the Diffused Layer of Unit Field

The present analysis is exact, and begins with a calculation of the potential, V(x, y), at all points in the unit field (Figure 35). The items of interest are obtained from this potential as follows. Let $R_{\square}$ be the sheet resistance (ohms per square):

$$i_c = (1/R_{\square}) \int_{-S/2}^{+S/2} \partial V/\partial y(x, o)dx \tag{4}$$

$$i_G = i_n - i_c \tag{5}$$

$$V = (1/WS) \int_{-S/2}^{+S/2} dx \int_{o}^{W} V(x, y)dy \tag{6}$$

The potential itself satisfies the equation

$$(1/R_{\square}) (\partial^2/\partial x^2 + \partial^2/\partial y^2) V(x, y) + J_n(x, y) = 0 \tag{7}$$

which follows from local conservation of current and Ohm's law. Boundary conditions are V = 0 at the three metal sides and $\partial V/\partial y = 0$ at the open end. The solution is $[J_n(x, y) = J_n = \text{constant}]$:

$$V(x, y) = R_{\square} J_n S^2 \cdot \left\{ 1/2 \left[1/4 - (x/S)^2 \right] - 4 \sum_{n=1}^{\infty} (-)^{n+1}/[(2n-1)\pi]^3 \cos \frac{(2n-1)\pi x}{S} \cosh \frac{(2n-1)\pi y - W)}{S} \operatorname{sech} \frac{(2n-1)\pi W}{S} \right\} \tag{8}$$

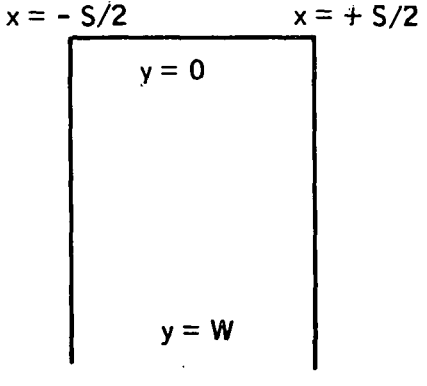


Figure 35. Coordinates of the Unit Field

Results

The normalized contact strip current and effective resistance were calculated from Equations (4), (6), and (8). The results, which depend only on the ratio S/W, are given to good approximation by simple linear forms if $S/W \lesssim 0.5$, a condition which covers all configurations of practical interest. Letting $R_o = 1/12\ R_\square\ S/W$ represent the resistance of the unit field with the two grid strips but no contact strip,[7] we find

$$i_c/i_n \cong 0.2714\ S/W \tag{9}$$

$$R/R_o \cong 1 - 0.3151\ S/W \tag{10}$$

For example, let $J_n = 30\ mA/cm^2$, $R_\square = 50\ \Omega/\square$, $S = 0.5$ cm, and $W = 2$ cm:

$i_n = (30)(0.5)(2) = 30.0$ mA

$i_c = (0.2714)(0.5/2)(30) = 2.04$ mA

$R_o = (1/12)(50)(0.5/2) = 1.042$ ohms

$R = [(1.042)(1 - 0.3151)(0.5/2)] = 0.960$ ohm

$V = (30)(0.960) = 28.8$ mV

$P = (30)(28.8) = 864\ \mu W$

Comparison with Handy Model[5]

Handy assumed that i_c originates in a triangular region whose base is the contact strip (Figure 36). He proceeded to develop a relationship for the half-angle, θ, based on continuity of voltage between the two regions at the apex of the triangle. According to this representation, the fractional current to the contact strip is

$$i_c/i_n = (S/4W) \cot \theta. \tag{11}$$

The actual boundaries which separate the origins of i_c and i_G were determined from the exact model and are shown in Figure 37. This is the path of steepest ascent of $V(x, y)$, beginning at the metalization corners.

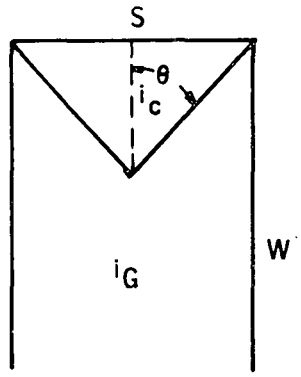


Figure 36. Geometry Assumed by Handy for Separation Between i_c and i_G

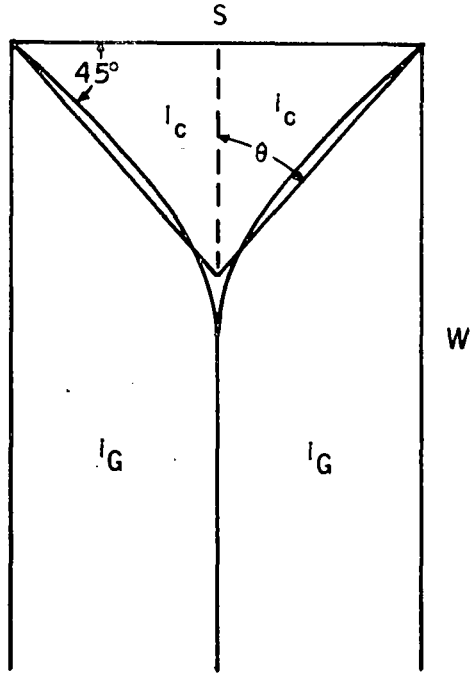


Figure 37. Exact Current Boundaries (cf Figure 32) Determined By Steepest Ascent of V(x, y) Starting at the Corners. The emergence angle is 45 degrees. Boundaries approach each other asympototically. The triangle of area equal to the i_G region has an apex half-angle, θ, which is constant at 42°39' for S/W ≤ 0.5. Hence, the calculation of circuit parameters is much simpler than in Handy's approximate model, which produces a variable θ.

The boundaries emerge from the corners at a 45-degree angle but then curve so that they approach each other tangentially. The boundary shape is practically independent of the ratio S/W in the range $S/W < 0.5$, and this accounts for the simplicity of expressions (9) and (1). In fact, the triangle with area equal to the i_c region has a constant $\theta = 42°39'$ over this range. Handy's θ is not constant, as seen from Table 9. His angles are smaller, meaning that his model overestimates current to the contact strip.*

Table 9 also includes i_c/i_n and $1 - R/R_o$. Gradual departures from linearity are evident in the range of S/W above 0.5, where the equivalent half-angle θ begins to increase beyond 42°39'. The quantity $1 - R/R_o$ represents the fractional decrease in resistance due to the contact strip. The same quantity gives the fractional decrease in $\overline{V}$ and the fractional decrease in P.

Table 9. Equivalent Circuit Parameters According to Exact Model. Both the exact (θ) and Handy's (θ_H) equivalent half-angles are included.

S/W	i_c/i_n	$1 - R/R_o$	θ	θ_H
0.2	0.05428	0.06302	42°39'	35°56'
0.4	0.10855	0.12605	42°39'	36°17'
0.6	0.16282	0.18906	42°39'	37°25'
0.8	0.21694	0.25190	42°40'	38°16'
1.0	0.27041	0.31396	42°45'	39°11'
1.2	0.32237	0.37416	42°56'	40°10'
1.4	0.37189	0.43141	43°16'	41°15'
1.6	0.41825	0.48480	43°43'	42°24'
1.8	0.46100	0.53382	44°18'	43°39'
2.0	0.50000	0.57827	45° 0'	45° 0'

Proof of $P = i_n\overline{V}$

Local power dissipation density, P_D is given by

$$P_D = \vec{J} \cdot \vec{E} \text{ watts/cm}^2, \tag{12}$$

where $\vec{J}$ is vector sheet current density (amp/cm) and $\vec{E}$ is the electric field:

*It appears that there is a further problem in Handy's model. He defined the effective resistance as $R = V_{max} / I_n$, where V_{max} is the potential appearing at the apex of the triangle (Figure 36). Then $P = i_n^2$ and $R = i_n V_{max}$, which is at variance with the result proved in the proof that follows.

$$\vec{J} = -\frac{1}{R_\square} \text{grad}\, \vec{V} \text{ (2-dimensional)} \tag{13}$$

$$\vec{E} = -\text{grad}\, \vec{V} \tag{14}$$

Hence,

$$P_D = \frac{1}{R_\square} \left|\text{grad}\, V\right|^2$$

and

$$P = \iint \frac{1}{R_\square} \left|\text{grad}\, \vec{V}\right|^2 dA \tag{15}$$

where the integration is over the area of the unit field.

A mathematical identity enables us to write

$$\iint \left|\text{grad}\, \vec{V}\right|^2 dA = \int V (\text{grad}\, \vec{V}) \cdot \vec{n}\, ds = \iint V \Delta V\, d\Lambda \tag{16}$$

where $\Delta = \partial^2/\partial x^2 + \partial^2/\partial y^2$ and the single integral is around the perimeter of the field. The first integrand on the right is zero everywhere on the perimeter due to the boundary conditions (either V is zero or $\text{grad}\, \vec{V} \cdot n$ is zero). In the second integral, $\Delta V = R_\square J_n$ from Equation (7). It follows that

$$\iint \left|\text{grad}\, \vec{V}\right|^2 dA = R_\square J_n \iint V\, d\, A \tag{17}$$

Substitution into Equation (15) gives

$$P = J_n \iint V\, d\, A = W\, S\, J_n\, \bar{V} = i_n\, \bar{V}. \tag{18}$$

CONCLUSIONS

From work performed during this quarter, we conclude that:

- The fracture toughness and thermal shock resistance of mullite substrates varies little between Coors material and Honeywell-processed material. These appear to be good quality control indicators for substrate selection.
- Substrate characterization tests for mullite suitability for silicon coatings will be deemphasized. Our knowledge is fairly complete in terms of understanding the necessary mechanical parameters of the substrate.
- We have eliminated the contamination problem which previously plagued the dip coater. Our SOC material is providing better cell performance than ever.
- A coater dedicated to increasing the throughput without sacrificing thickness is a necessity.
- Silicon layers will spall off of ceramic substrates which do not have a porous surface.
- The continuous coater (SCIM) will have to contain preheaters and afterheaters to provide the thermal gradient necessary to safeguard against large substrate thermal fracture.
- Light-beam-induced current (LBIC) will be the standard method for determining L_D values.
- Cells etched with Wrights etch to show twin boundaries and dislocations do not suffer loss of performance. This indicates that a correlation between performance and dislocation densities can be obtained.
- Slotted substrate cells are technically feasible and show great promise for reaching high conversion efficiency. The best to date is 4.3 percent (uncoated), 5-cm^2 area.
- Our antireflection (AR) coating technique improves performance by approximately 33 percent. The best to date is 9.5 percent, 1-cm^2 active area.
- Ammonia borane (NH_3BH_3), when mixed with carbon resin, shows promise as a P^+ diffusion source for the silicon at the ceramic interface.

RECOMMENDATIONS

To date, activity has been carried out in two areas of the program to gain a more fundamental understanding of the parameters necessary for successful SOC coating. These areas are: 1) the understanding of the mechanical/thermal properties of mullite, and 2) the evaluation of various carbon layers strictly from the standpoint of silicon adhesion to ceramic.

We now have a good base of fundamental knowledge concerning these areas. In the interest of providing greater emphasis in the area of coating throughput versus thickness optimization, we recommend a deemphasis in substrate characterization and carbonization (mechanical property analysis) activity.

NEW TECHNOLOGY

The incorporation of ammonia borane (NH_3BH_3) with a carbon resin to provide a diffusion source for the base layer of our SOC cell represents an important new development. This could provide a means for creating a conductive layer at the ceramic-silicon interface, minimizing the series resistance within the SOC cell and improving the overall cell performance.

PROJECTION OF FUTURE ACTIVITIES

Future activities are projected as follows:

- A dedicated coater will be built to maximize our coating rate for 100-μm layers.
- Slotted substrate cells will be fabricated with various slot widths and spacing to optimize our SOC cell performance.
- AR coating techniques will be refined to improve performance of SOC cells.
- The cause of our low fill factors will be determined and processing of our cells improved to eliminate this problem.
- New device design activity will begin on the integral optical coupler for use with a high-voltage cell structure.
- Substrates will be dipped into silicon containing various concentrations of boron to investigate L_D versus N_A versus series resistance considerations.
- The temperature gradient at the entrance and exit ports of the SCIM coater furnace chamber will be modified to prevent substrate breakage.
- Experimental Coors substrates having thermal expansion coefficients closely matched to silicon will be dipped.
- LBIC will be used to evaluate material before processing to determine L_D.
- Work will continue to determine usefulness of ammonia borane/carbon resin as P^+ diffusion source.
- Device modeling activities will concentrate on incorporating material parameters in theoretical analysis.
- Active area and total area solar cells will be fabricated to determine material and processing limitations to cell performance.
- Coating/solidification consultation will be carried out with Dr. J. Verhoeven of Iowa State University to determine definitive coating experiments leading to maximum throughput.

Updated versions of the Program Plan, Program Labor Summary, and Program Cost Summary are presented in Figures 38, 39, and 40, respectively.

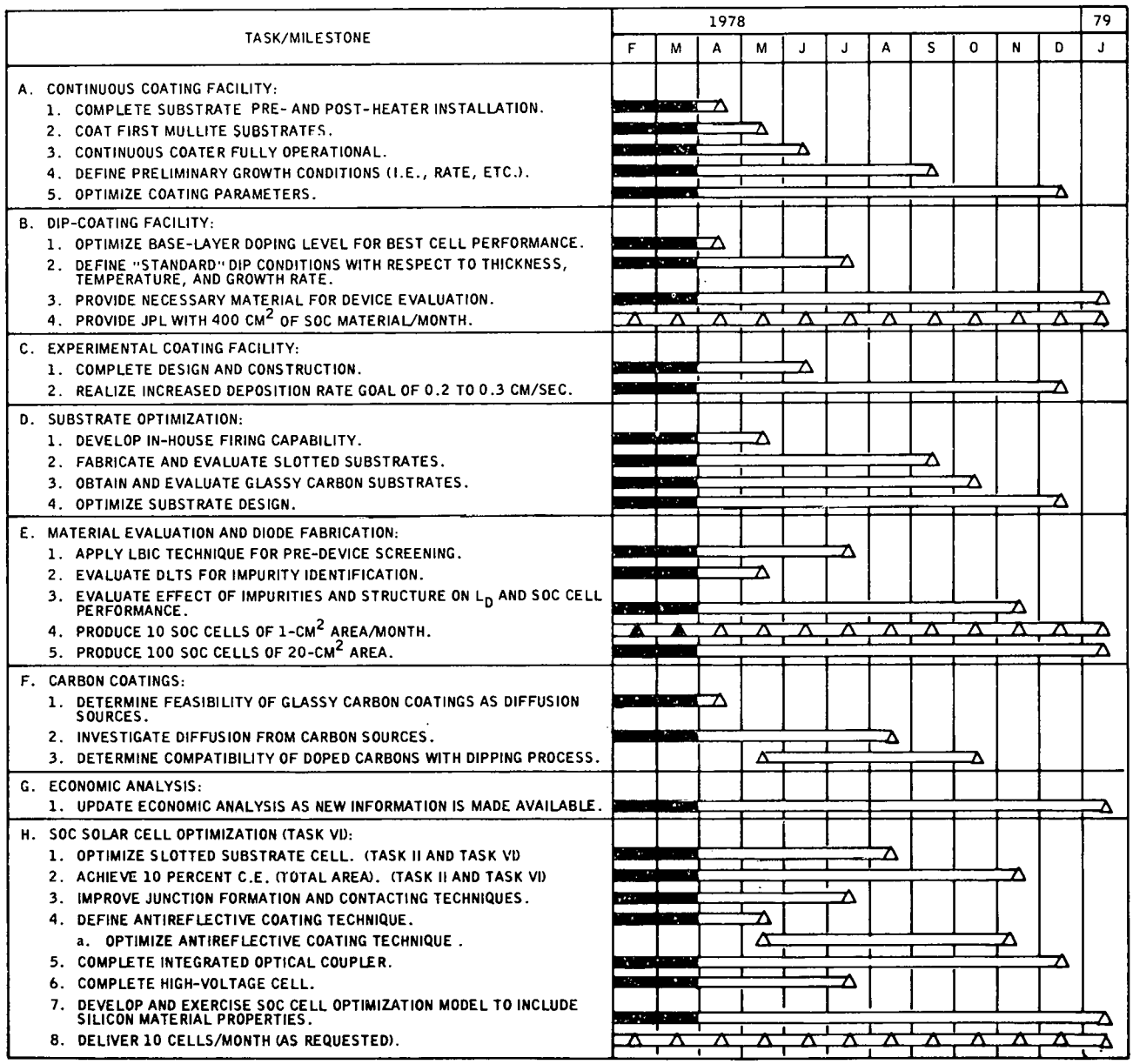


Figure 38. Updated Program Plan

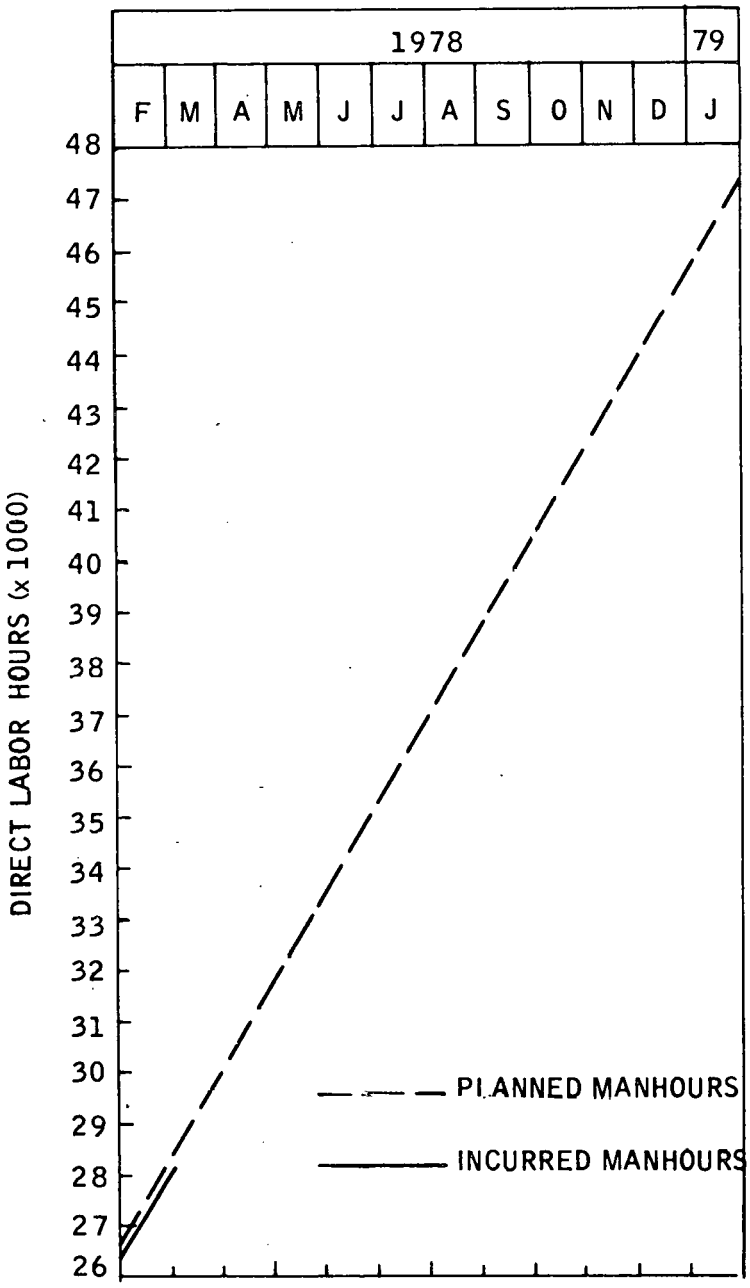


Figure 39. Updated Program Labor Summary

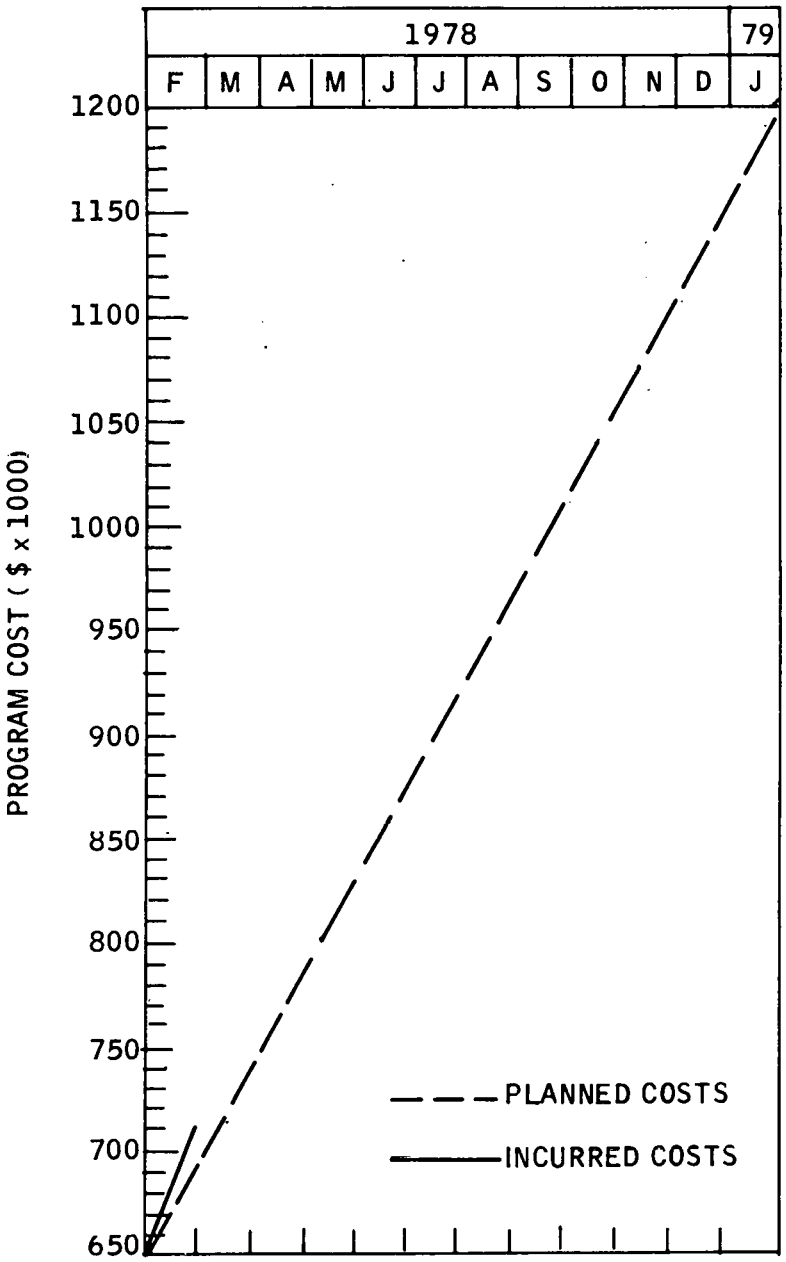


Figure 40. Updated Program Cost Summary

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*U.S. GOVERNMENT PRINTING OFFICE: 1978-740-306/4317. Region 4.