SELECTIVE, DEEP Si TRENCH ETCHING WITH DIMENSIONAL CONTROL

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ABSTRACT

The recent development of a high-aspect ratio Si etch (HARSE) process[1] has enabled the fabrication of a variety of Si structures where deep trench etching is necessary. The HARSE process relies on the formation of a sidewall etch inhibitor to prevent lateral etching of the Si structures during exposure to an aggressive SF_6/Ar plasma etch chemistry. The process yields highly anisotropic profiles with excellent dimensional control for high aspect ratio features. In this study, Si etch rates and etch selectivities to photoresist are reported as a function of chamber pressure, cathode rf-power, ICP source power, and gas flow. Si etch rates > 3 μm/min with etch selectivities to resist > 75:1 were obtained. Lateral dimensional control, etch selectivities to SiO_2 and Si_3N_4, and aspect ratio dependent etching (ARDE) will also be discussed.

Keywords: high-aspect ratio silicon etching, inductively coupled plasma etching, aspect ratio dependent etching, dimensional control.

1. INTRODUCTION

Pattern transfer into Si has been very successful by both wet chemical and plasma etch techniques.[2-6] However, the fabrication of deep, high-aspect ratio Si structures has been limited due to low etch selectivity to photoresist masks, slow etch rates, or poor lateral dimensional control. For example, wet chemical etching is typically fast, often exceeding several μm/min, but can be isotropic, crystallographic, and difficult to control. Reactive ion etching (RIE) of Si in either chlorine or fluorine based plasmas can yield anisotropic, non-crystallographic, highly directional etching but at rates typically < 0.5 μm/min. High-density plasma (HDP) etching including electron cyclotron resonance (ECR) etching and inductively coupled plasma (ICP) etching can result in rates > 2.5 μm/min with anisotropic profiles (at temperatures < 0°C) but aspect ratios that are typically ≤ 10:1. Another disadvantage of RIE and HDP deep etching of Si is the low selectivity to photoresist (and thus the need for hard masks) due to the high ion energies necessary to achieve high etch rates and anisotropic profiles. The recent development of a high-aspect ratio Si etch (HARSE) process has resulted in anisotropic profiles at room temperature, etch rates > 3.0 μm/min, aspect ratios > 30:1, and good dimensional control.[1] Additionally, the HARSE process has shown etch selectivities of Si to photoresist > 75:1 thereby eliminating the process complexity of hard etch masks for features deeper than 100 μm.

The HARSE process (patented by Robert Bosch GmbH)[1] relies on an iterative ICP-based deposition/etch cycle in which a polymer etch inhibitor is conformally deposited over the wafer during the deposition cycle. The polymer deposits over the resist mask, the exposed Si field, and along the sidewall. During the ensuing etch cycle, the polymer film is preferentially sputtered from the Si trenches and the top of the resist mask due to the acceleration of ions (formed in the ICP plasma) perpendicular to the surface of the wafer. Provided the ion scattering is relatively low, the polymer film on the sidewall is removed at a much slower rate, thus minimizing lateral etching of the Si. Before the sidewall polymer is completely removed, the deposition step is repeated and the cycle continues until the desired etch depth is obtained. In this study we report Si etch results using the HARSE process as a function of pressure, cathode rf-power, ICP source power, and gas flow. These results are compared to Si etch results obtained in a SF_6/O_2-based ICP plasma.

2. EXPERIMENTAL

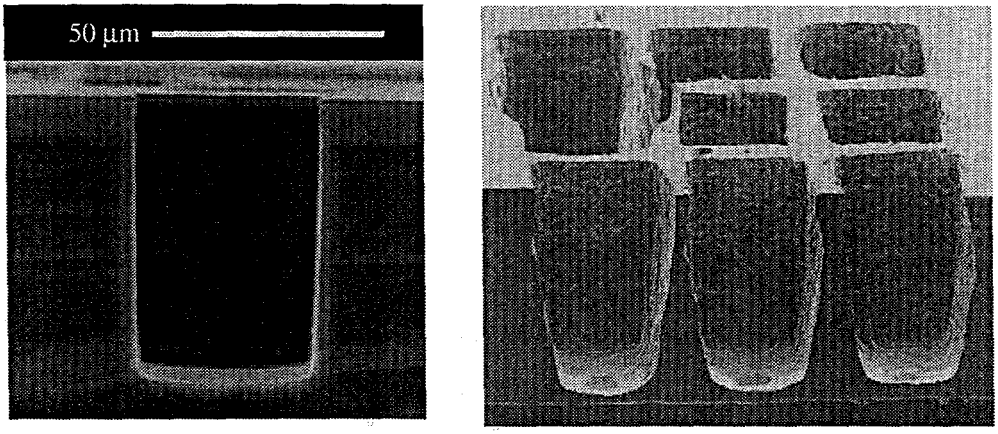
Si wafers were patterned with AZ-4330 photoresist, which was spun on to a thickness of approximately 3.4 μm. The Si etch results were obtained in a load-locked Plasma-Therm SLR 770 ICP etch system with a Plasma-Therm 2 MHz ICP source. Energetic ion bombardment was provided by superimposing an rf-bias (13.56 MHz) on the sample. Samples were mounted with a low vapor pressure thermal paste onto a 6 inch Si wafer carrier that was coated with approximately 1 μm of thermal SiO_2 to minimize loading effects. The Si wafer carrier was clamped to the cathode and cooled to 20°C with He gas. Process

gases were introduced through an annular region at the top of the chamber. Si etch rates were calculated from the depth of the etched feature measured with an Alpha Step stylus profilometer following removal of the photoresist. Samples were exposed to the plasma for 10 minutes and all depth measurements were taken on 20 μm wide features in a minimum of three positions. Each sample was approximately 1 cm^2. Selectivities were reported as the ratio of Si etch rate to resist erosion rate. The resist erosion rate was calculated from the depth of the resist measured with the profilometer before and after exposure to the plasma relative to the depth of the Si removed during the etch. Etch profile and morphology were evaluated using a scanning electron microscope (SEM).

3. HARSE RESULTS

3.1 HARSE versus ICP etch comparison

As stated earlier, Si can be etched in an ICP SF_6-based plasma at relatively high rates, however good dimensional control and smooth etch morphology can be difficult to achieve. In Figure 1, SEM micrographs show Si vias etched by (a) the HARSE process and (b) an ICP-generated SF_6/O_2 plasma. The via etched using the HARSE process was approximately 40 μm wide and etched to a depth of approximately 70 μm while the vias etched in the ICP were 50 μm wide and etched to a depth of approximately 150 μm. The HARSE etch conditions were 23 mTorr pressure, 100 sccm SF_6, 40 sccm Ar, 875 W ICP source power, 6 W cathode rf-power with a corresponding dc-bias of –25 to –50 V, and 20°C substrate temperature. The ICP etch conditions were 5 mTorr pressure, 50 sccm SF_6, 10 sccm O_2, 10 sccm Ar, 500 W ICP source power, 250 W cathode rf-power with a corresponding dc-bias of -350 V, and -40°C substrate temperature. Due to the high dc-bias used in the ICP, the etch selectivity of Si to photoresist was typically ≤ 2:1; therefore, a Ni mask was used to achieve etch depths > 25 μm. The ICP etch rate was approximately 1 μm/min. The HARSE process used a photoresist mask due to etch selectivities > 75:1. The high etch selectivity observed in the HARSE process is attributed to the deposition of the sidewall polymer etch inhibitor, which also deposits on the resist. Despite ion bombardment of the surface, the deposited polymer significantly reduces the erosion rate of the resist. Additionally, lower dc-biases in the HARSE process (≤ -50 V as compared to -350 V in the ICP) significantly reduce the resist erosion rate. The HARSE process yielded an etch rate of approximately 2.0 μm/min with highly anisotropic etch profiles, good dimensional control, and smooth etch morphologies. The sidewall polymer etch inhibitor deposited in the HARSE process eliminated lateral etching of the Si resulting in via widths which were essentially identical at the top and bottom of the feature. However in the ICP, lateral etching of the Si was observed due to the absence of a sidewall polymer resulting in poorly controlled via profiles. The sidewall profile was concave with a much wider opening at the top of the via than that obtained at the bottom. Additionally, the sidewall was much rougher than that achieved using the HARSE process. The lateral Si etching observed in the ICP was somewhat surprising due to the low process pressure (2 mTorr) which reduces ion scattering and sidewall sputtering and the low substrate temperature (-40°C) which lowers the volatility of the etch products.



(a) (b)

Figure 1. SEM micrographs which show Si vias etched by (a) the HARSE process and (b) an ICP-generated SF_6/O_2 plasma. The via etched using the HARSE process was approximately 40 μm wide and etched to a depth of approximately 70 μm while the vias etched in the ICP were 50 μm wide and etched to a depth of approximately 150 μm.

DISCLAIMER

3.2 Etch rates and selectivity

In order to evaluate the HARSE process for device application, etch parameters were studied as a function of chamber pressure, cathode rf-power, ICP source power, and SF_6 flow rate. In Figure 2, Si etch rates and etch selectivity of Si to photoresist are shown as a function of pressure while the cathode rf-power, ICP source power, gas flows, and substrate temperature remained constant. Plasma conditions change quite dramatically as a function of pressure, in particular the mean free path decreases, the collisional frequency increases, and the residence time of the reactive species increases as the pressure is increased. This typically results in changes in both ion energy and plasma density which strongly influences the etch properties. Si etch rates increased as the pressure was increased from 15 to 20 mTorr, suggesting a reactant limited regime at low pressures. Above 20 mTorr, the Si etch rate was relatively independent of pressure. Selectivity of Si to photoresist was typically > 50:1 with a maximum of approximately 95:1 at 25 mTorr. Etch profile and morphology were relatively independent of pressure.

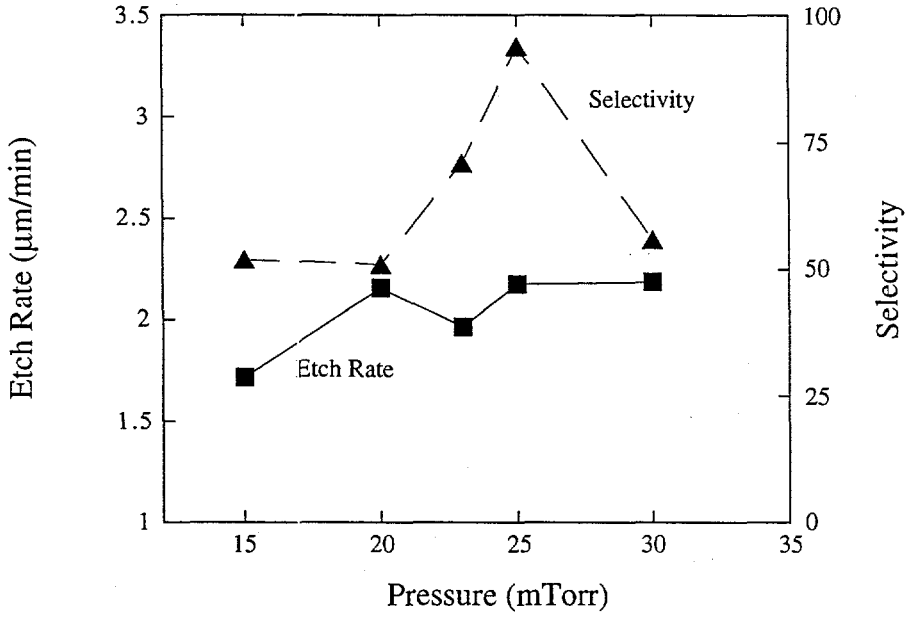


Figure 2. Si etch rates and etch selectivity of Si to photoresist as a function of pressure in the HARSE process.

Etch characteristics normally show a strong dependence on ion energy and plasma density. Ion energies influence the physical component of the etch whereas plasma density can affect both the physical and chemical components of the process. In Figure 3, Si etch rates and etch selectivity of Si to photoresist are plotted as a function of cathode rf-power while all other plasma parameters were held constant. Si etch rates increased monotonically by almost a factor of 3 as the cathode rf-power increased. Since cathode rf-power is closely related to dc-bias and ion bombardment energy, higher etch rates at higher ion energies implies more efficient bond breaking of the Si surface bonds and improved sputter desorption of the etch products (i.e. SiF_x) from the surface. As the ion bombardment energy increased so did the sputtering efficiency of the polymer in the Si field which was deposited during the deposition cycle of the HARSE process. Under low rf-power conditions, the polymer may not sputter as efficiently thereby increasing the etch initiation time and reducing the Si etch rates. Despite faster Si etch rates, the etch selectivity decreased quite dramatically as the cathode rf-power increased due to faster sputter rates of the polymer and faster erosion rates of the resist.

Dimensional control and etch profile were strongly dependent on cathode rf-power. Under low cathode rf-power conditions, the etch profile was positively tapered. At moderate cathode rf-powers, the profile was highly anisotropic. Finally, under high cathode rf-power conditions, the profile became re-entrant. This trend can be observed in Figures 4 and 5. In Figure 4, SEM micrographs show Si posts etched at (a) 8 and (b) 25 W cathode rf-power. At 8 W, the etch profile was highly anisotropic at an etch depth of approximately 23 μm. At 25 W, the etch depth was approximately 30 μm and a

prominent re-entrant profile was observed. The re-entrant profile observed under high rf-power conditions was attributed to more ion scattering at the base of the feature and higher sputter removal rates of the polymer from the Si sidewall.

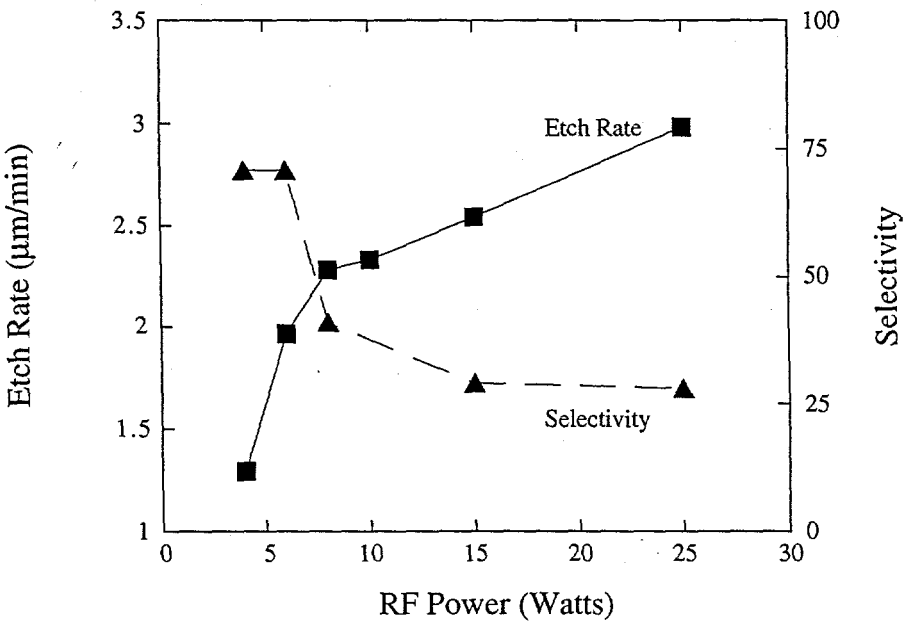


Figure 3. Si etch rates and etch selectivity of Si to photoresist as a function of cathode rf-power for the HARSE process.

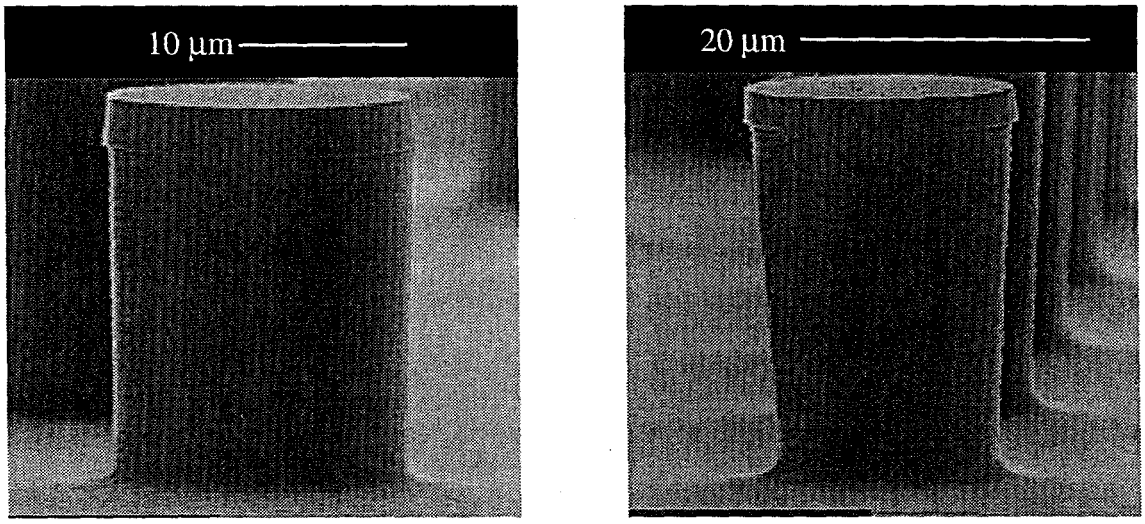


Figure 4. SEM micrograph of Si posts etched at (a) 8 W and (b) 25 W cathode rf-power. The re-entrant profile observed at 25 W cathode rf-power was attributed to increased ion scattering and sputter removal of the sidewall polymer.

In Figure 5, Si trenches 15 to 20 μm wide were etched approximately 70 μm deep. In Figure 5a, the HARSE process was run at 6 W cathode rf-power for 30 minutes. The etch rate was approximately 2 μm/min at a dc-bias of approximately -50 V. The trench profile showed a positive taper and significant roughness at the bottom while the sidewall at the top remained smooth. The rough etch morphology at the bottom of the trench was attributed to inefficient sputter

removal of the deposited polymer due to ineffective ion transport. In Figure 5b the standard etch was run for 20 minutes followed by a more aggressive etch (8W cathode rf-power and 22% longer etch cycle) for 5 minutes and then completed with the standard process for another 5 minutes. The etch was approximately 15 μm deeper than the single step etch with an etch rate of approximately 2.5 μm/min. The etch was highly anisotropic with a slight foot at the base of the sidewall and a smooth sidewall morphology throughout the feature. At higher rf-power, the increased ion bombardment energy improved the sputter removal of the deposited polymer from the bottom of the trench and allowed chemical etching at the base of the Si trench. Therefore it is critical to optimize the sputter removal rate of the polymer from the base of the feature.

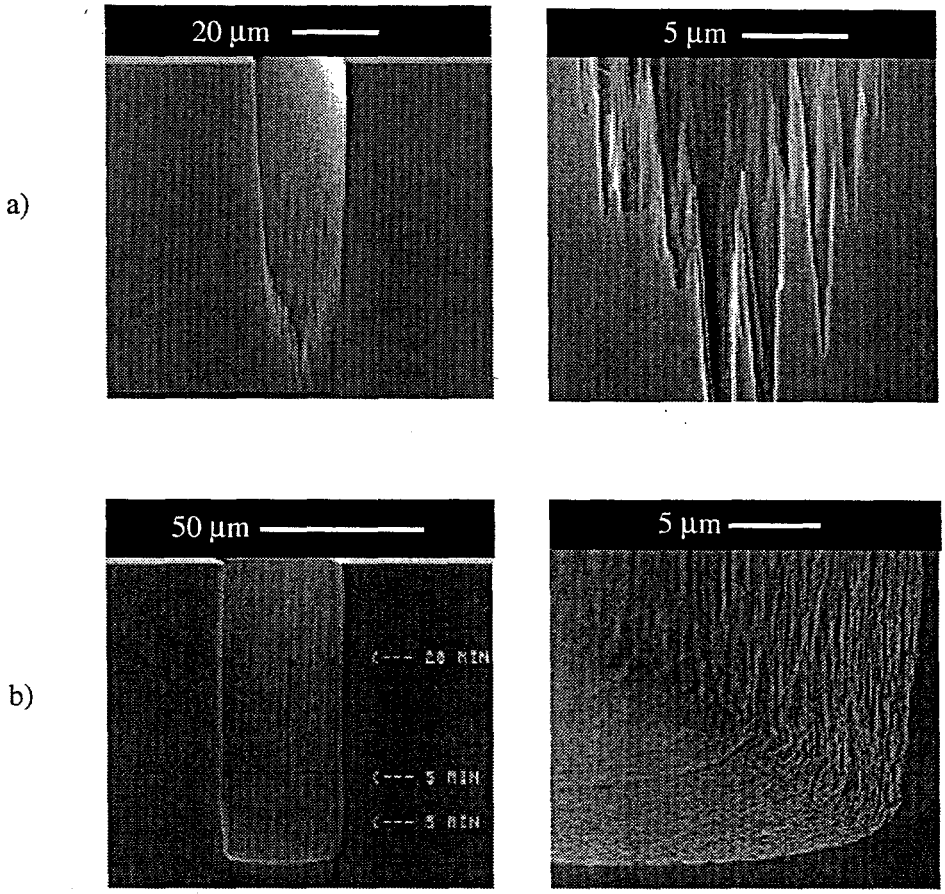


Figure 5. SEM micrograph of Si etched with a) single step HARSE process (6W cathode rf-power) and b) a three-step process with an aggressive step (8W cathode rf-power) to increase the sputter desorption at the base of the trench.

As a function of increasing plasma density or ICP source power, etch rates typically increase due to 1) higher concentrations of reactive species which increases the chemical component of the etch mechanism and 2) higher ion flux which increases the sputter desorption component of the etch mechanism. The effects of ion energies and plasma densities are more obvious for HDP systems, since ion energies and plasma densities can be more effectively decoupled as compared to RIE. In Figure 6, the Si etch rates increased by approximately 30% as the ICP source power increased. The etch selectivity data was less consistent ranging from approximately 55:1 to 90:1. The low selectivity observed at 800 W ICP source power is not understood. Etch profiles were slightly re-entrant and rough under low ICP source power conditions.

Si etch rates are also expected to increase with higher SF_6 flow rates due to the strong chemical component of the Si etch mechanism and higher concentrations of reactive F. In Figure 7, Si etch rates and selectivity to photoresist are plotted as a function of SF_6 flow rate. Si etch rates increased as the SF_6 flow rate increased from 60 to 120 sccm implying a reactant limited etch regime at low flow rates. However at 150 sccm SF_6 the etch rate decreased significantly indicating a diffusion limited regime. The etch selectivity was quite low (< 50:1) except at 80 sccm where the selectivity was >120:1. Etch profile and morphology were essentially independent of SF_6 flow rates.

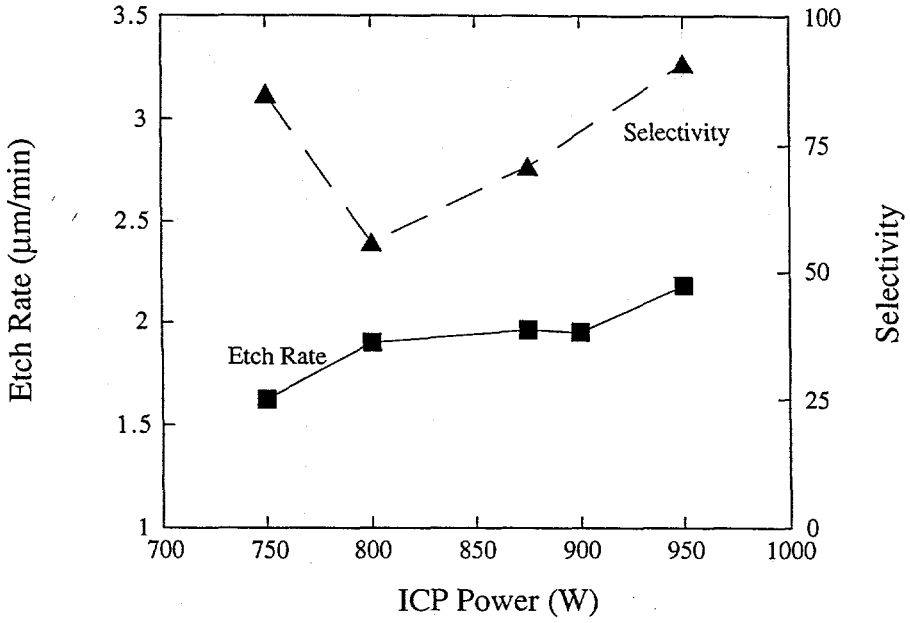


Figure 6. Si etch rates and etch selectivity of Si to photoresist as a function of ICP source power for the HARSE process.

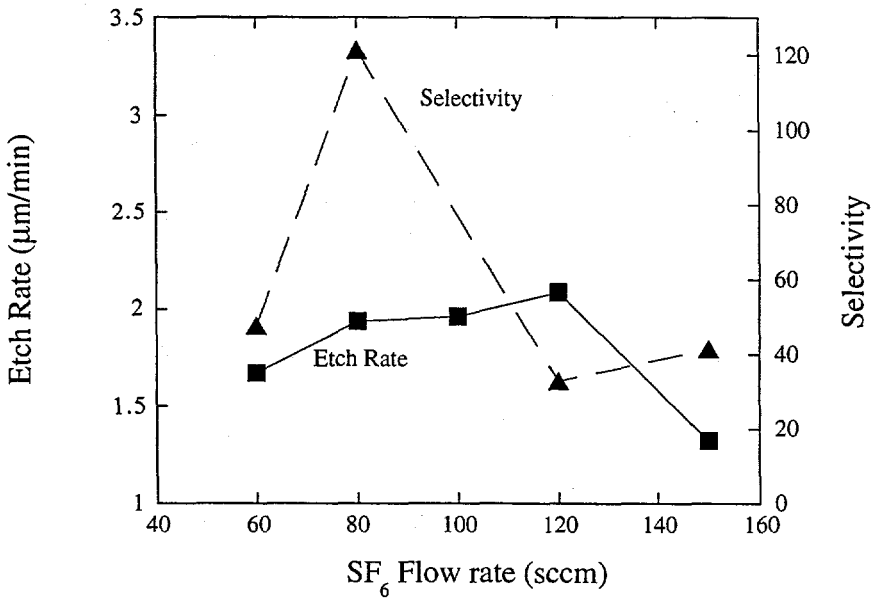


Figure 7. Si etch rates and etch selectivity of Si to photoresist as a function of SF_6 flow rate for the HARSE process.

3.3 Aspect ratio dependent etching (ARDE)

The observation that smaller diameter vias and narrower trenches etch more slowly than larger diameter vias and wider trenches is often referred to as aspect ratio dependent etching (ARDE) or RIE lag.[7] An example of ARDE is shown in Figure

8 for 1 and 3.5 μm wide trenches. The etch depth for the 1 μm trenches was approximately 7.5 μm while the 3.5 μm trenches were etched to a depth of approximately 9.5 μm. The difference in etch depth is attributed to transport of reactants and etch products into and out of the trenches.[7] As lateral dimensions decrease or the etch depths increase it becomes more difficult for the reactive etch species to reach the bottom of the trench and more difficult for etch products to be removed. Ayon and coworkers have observed improved ARDE effects for the HARSE process under high SF_6 flows conditions.[8] They attributed this observation to a reduction in etch product species that contribute to redeposition.

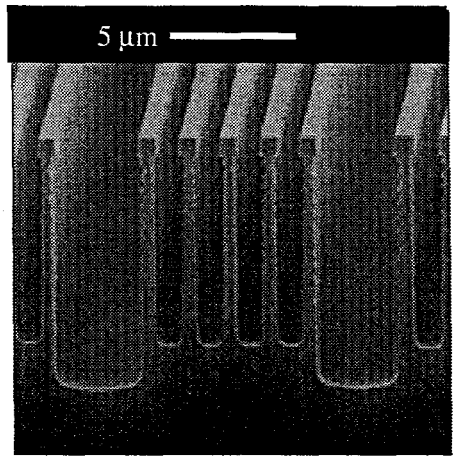


Figure 8. SEM micrograph of Si HARSE etch which demonstrates ARDE. The 1 μm wide trenches were etched to an approximate depth of 7.5 μm while the 3.5 μm trenches were etched to a depth of approximately 9.5 μm.

In Figure 9, Si etch depths are plotted as a function of via diameter for the HARSE process (23 mTorr pressure, 100 sccm SF_6, 40 sccm Ar, 850 W ICP source power, 8W cathode rf-power, and 20°C substrate temperature) at 30, 60, and 90 minute plasma exposure times. As expected, the etch depths increased as a function of time. Also, as the via diameters increased from 10 to 300 μm, the etch depth typically increased independent of etch time. This was attributed to improved transport of reactants into the via and etch products out of the via as the diameter increased. Above 300 μm via diameter, the etch depth remained relatively constant independent of diameter for the 30 and 60 minute etches with only a slight increase for the 90 minute etch.

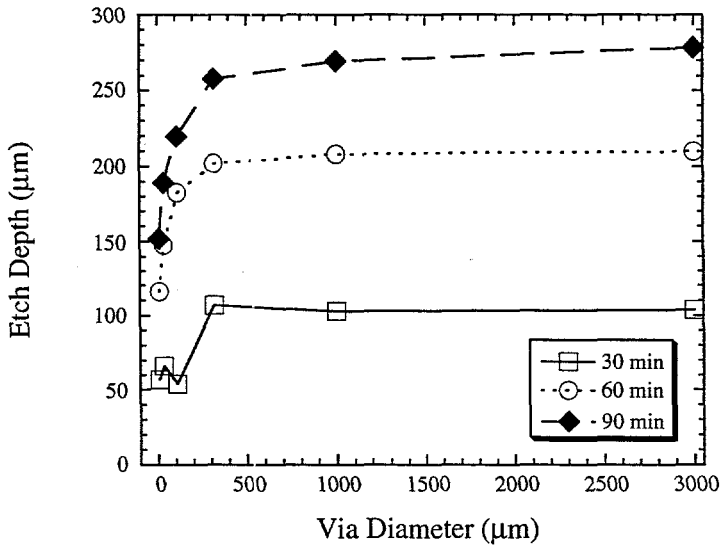


Figure 9. Si etch depths plotted as a function of via diameter for 30, 60, and 90 minute HARSE etch times.

3.4 Etch selectivities

Selective etching of one material over another is critical in the fabrication of microelectronic and photonic devices to accurately stop on defined layers for subsequent processing steps, for example the formation of ohmic and gate contacts. For high aspect-ratio silicon structures, selective etching is important in the fabrication of membrane-based devices where the etch process must stop on a thin film layer typically < 1 μm thick. Etch selectivities of Si to several films exposed to the HARSE process are shown in Table 1. HARSE etch conditions were 23 mTorr pressure, 100 sccm SF_6, 40 sccm Ar, 850 W ICP source power, 8W cathode rf-power with a corresponding dc-bias of –25 to –50 V, and 20°C substrate temperature. As mentioned earlier, the high etch selectivity of Si to photoresist simplifies the process sequence for deep high-aspect ratio features by eliminating the need for hard masks. The high etch selectivities of Si to either SiO_2 or Si_3N_4, makes them excellent candidates for the membrane-based structures including flexural plate wave (FPW) devices and micromachined valves, pumps, and heaters.

Material	Etch Rate (Å/min)	Selectivity to Si
Si	25,000	
Polysilicon	5334	4.7:1
LPCVD Si_3N_4	295	85:1
LPCVD SiO_2	90	275:1
Thermal SiO_2	90	275:1
Photoresist	250	100:1

Table 1. HARSE etch rates and selectivity to Si.

A schematic diagram of a membrane-based device is shown in Figure 10. Initially, a thermal SiO_2 or low stress low pressure chemical vapor deposition (LPCVD) Si_3N_4 film is deposited on the frontside of the wafer. All frontside processing (metallization, etch, etc.) is completed and protected with photoresist. The Si via etch mask is then applied using a thick photoresist (AZ 4903) and aligned to the frontside membrane features using backside alignment techniques. The wafer is then exposed to the HARSE process (where 400 to 650 μm of Si is removed) and etched to the SiO_2 or Si_3N_4 membrane which is typically ≤ 1 μm thick. The results of this process sequence are demonstrated in Figure 11. The SEM micrograph shows a 400 μm wide Si via etched to a depth of approximately 685 μm at an etch rate of 3.5 μm/min. Due to the high etch selectivity of Si to SiO_2 (see Table 1), the etch essentially stops on the thermal SiO_2 layer which was 0.6 μm thick. The via was highly anisotropic and maintained the dimensions of the mask, however the sidewall morphology was somewhat rough due to vertical striations and a slight Si foot was observed at the base of the sidewall. Ayon and co-workers have also observed a foot at the base of many of their features.[8] Altering the deposition cycle of the HARSE process, they have been able to significantly reduce the foot dimesions. The features observed at the bottom of the via in Figure 11a were frontside metal features which could be seen through the transparent thermal SiO_2 film.

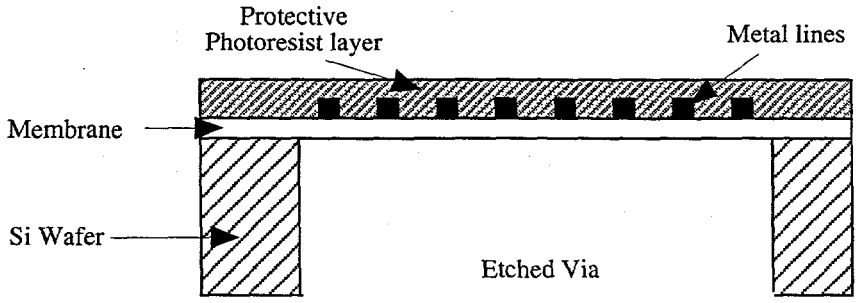
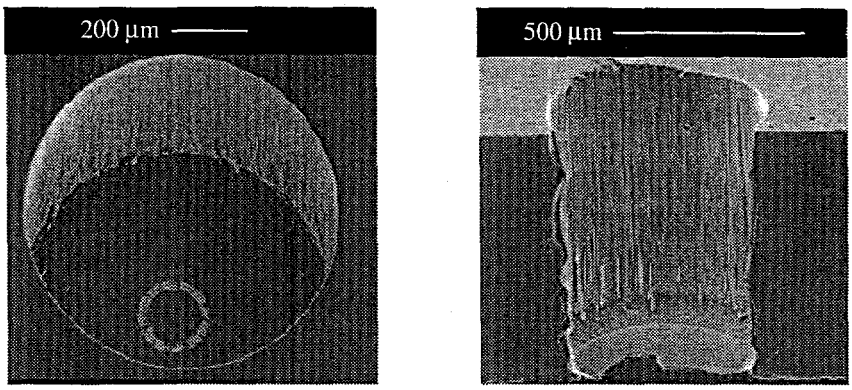


Figure 10. Schematic of a membrane based device with a HARSE via, a thin film membrane, frontside metal lines, and a protective photoresist layer.



(a) (b)

Figure 11. SEM micrographs of a Si via HARSE etched to a depth of approximately 685 µm to a thin thermal SiO_2 layer which acts as an etch stop. The via diameter was approximately 400 µm.

5. CONCLUSIONS

Etch rates ranging from 1 to 3.5 µm/min with highly anisotropic profiles and smooth etch morphologies were demonstrated for several HARSE process conditions. Si etch rates, profiles, dimensional control, and morphologies were strongly dependent on cathode rf-power. As the cathode rf-power or ion energy increased, the etch rate increased due to more efficient sputter removal of the polymer, more efficient bond breaking of the Si bonds, and more efficient sputter desorption of the etch products from the surface. Under low cathode rf-power conditions the etch profile was positively tapered due to inefficient sputter removal of the polymer; became highly anisotropic at moderate cathode rf-power; and was re-entrant under high cathode rf-power conditions due to ion scattering and sputter removal of the polymer from the Si sidewall. Si etch characteristics were much less dependent on chamber pressure, ICP source power, and SF_6 flow rate. The HARSE process operated at room temperature and showed etch selectivities of Si to resist > 75:1 thus eliminating the need for hard masks. Etch selectivities for Si to SiO_2 were 275:1 and to Si_3N_4 were 85:1 thus enabling the fabrication of membrane-based devices. ARDE was observed for small vias and trenches but was less significant for large features (≥ 300 µm).

6. ACKNOWLEDGMENTS

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