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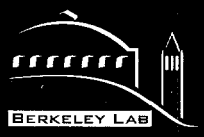

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Porosity in Collapsible Ball Grid Array Solder Joints

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Materials Sciences Division
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M.S. Thesis

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by

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Abstract

Ball Grid Array (BGA) technology has taken off in recent years due to the increased need for high interconnect density. Opposite to all the advantages BGA packages offer, porosity in collapsible BGA solder joints is often a major concern in the reliability of such packages. The effect of pores on the strength of collapsible BGA solder-joints was studied by manufacturing samples with different degrees of porosity and testing them under a shear load. It was found that the shear strength of the solder joints decreased in a linear fashion with increasing porosity. Failure occurred by internal necking of the interpore matrix. It was confirmed that entrapment of flux residues leads to porosity by manufacturing fluxless samples in a specially made furnace, and comparing them with samples assembled using flux. Also, contamination of Au electrodeposits (in substrate metallization) was determined to cause significant porosity. It was found that hard-Au (Co hardened Au) electrodeposits produce high degrees of porosity even in the absence of flux. Finally, increasing the time the solder spends in the molten state was proven to successfully decrease porosity.

DEDICATED TO

María Andreina

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1. Introduction

1.1. General Background

The following is a short overview of the most relevant aspects of electronic packaging as they relate to the topic of this thesis. It begins with the definition of the broad concept of electronic packaging. Next, a few basic facts about solder and its role in electronic packaging are given. The reliability issues surrounding solder are presented next. Last, a description of Ball Grid Array technology is given, as it covers the specific solder joints studied for this work.

1.1.1. Packaging Technology

A package, in general, provides a "box" or protection for a given object. In the electronic industry a package usually has the following functions:

a) protects the silicon (or GaAs) die from environmental and mechanical damage,
b) provides electrical communication between the different devices,
c) dissipates the heat generated by the circuit,
d) provides a robust structure for handling and assembly, and
e) provides a shield from external electromagnetic radiation and interference.

The package has to accomplish all these functions and at the same time be compact (to be able to build small and light devices), reliable, and low cost. This combination of requirements makes packaging a challenging and interesting subject from an engineering point of view.

The electronic package is a hierarchical interconnection structure that allows a central processing unit (CPU) to communicate with memory and input/output (I/O) units such as the display, keyboard, and data storage devices. In general, packaging integrates[1]:

a) chips into single-chip modules (SCM) or multichip modules (MCM), known as a first level package,
b) components (SCMs, MCMs) on a card or printed circuit board that may be referred to as second level package, and

c) PCB assemblies, cables, power supplies, cooling systems, and peripherals into a mother board, frame or a box, which is called a third level package.

In the packaging process, the chip or (I/C) device is separated from its wafer and packaged on a carrier (first level). At this point the chip is protected from mechanical and chemical damage, so it can be tested and handled in the next manufacturing step. Next the package is assembled (usually soldered) onto a card or board (second level). Finally this card is assembled onto a "mother" board (third level).

In the chip-level or first level packaging, the IC device is connected to its carrier in one of three ways: wire bond, flip-chip, or tape automated bond (TAB). Wire bonding is done by first bonding the back of the die to the carrier with an adhesive, and then the chip pads are bonded to the carrier pads with gold or aluminum wires. For the flip chip package, the chip's pads face downward and are attached to the carrier with gold or solder bumps. In the tape automated bond (TAB), flat metal fingers provide an interconnection between chip pads and the leads on the carrier tape.

The second level packaging (in surface mount technology, SMT) is usually accomplished in one of two ways, with peripheral leads (leaded packages), or an area array. In both cases, a low melting temperature (< 350 °C) solder alloy is used to attach the package to the card or the board. The melting temperature of the solder has to be lower than the melting temperatures of the package and the board (plastic). Also, transistors on the Si Chip are based on high differences in concentration of dopants over very short distances, diffusion at high temperatures could ruin the whole circuitry by driving dopants from high to low concentration areas.

The most popular leaded packages are the Quad Flat Pack (QFP), Very Small Outline Package (VSOP), and Small Outline Integrated Circuit (SOIC). The most common area array packages are the Leadless Ceramic Chip Carrier (LCCC), Pin Grid Array (PGA), Ball Grid Array (BGA), and Tape Automated Bonding Ball Grid Array (TBGA).

The focus of this work is on Ball Grid Array packages, specifically on BGA packages with collapsible solder joints[i], such as Plastic Ball Grid Array packages (PBGA).

1.1.2. Solder in Electronic Packaging

Solder is commonly defined as a fusible alloy with a melting temperature below 400 °C. Sn-Pb is the most widely used alloy system in the electronic packaging industry. Other popular alloy systems are Sn-Ag, Sn-Sb, Sn-Bi, Sn-In, Sn-Pb-Ag, Sn-Pb-Bi, Sn-Pb-In, Sn-Ag-Sb, Pb-In, Pb-Ag, and Pb-Sb[2]. Solder is fabricated into various forms and shapes including bars, ingots, wire, powder, paste, preform, and ball.

The solder joints in a PBGA package are usually produced with eutectic Sn-Pb solder. Because of its common usage, eutectic 63 Sn-37 Pb was chosen to investigate the reliability of collapsible BGA solder joints. Another reason to choose eutectic Sn-Pb is because it is the most studied and well-characterized solder alloy system. Eutectic Sn-Pb is the most widely used solder due to its good combination of low melting temperature, good mechanical properties, and it readily forms intermetallic compounds (bonds) with Cu and Ni. In the Sn-Pb phase diagram, the eutectic composition (63 Sn- 37 Pb) has a liquidus temperature of 183 °C.

In the process of soldering, a joint is produced by the formation of an intermetallic compound between the two materials to be soldered. In the case of a Sn-Pb solder-joint, an intermetallic forms between the Sn in the solder and the substrate material. The substrate materials ordinarily found in BGA packages are Cu and Ni. The reason these materials are used as substrates or pad metallizations is that all of them form intermetallic compounds with Sn. Table 1.1.2-1 shows the compositions of the intermetallic compounds Sn forms with Cu and Ni. In addition, Au is also a very common substrate metallization material, but for different reasons. When Ni metallization is used, a thin layer of Au is needed to protect the Ni from oxidation. The amount of Au used is kept as low as possible to prevent Au embritelment from the formation of brittle Au-Sn intermetallics[3].

[i] Collapsible joints are those in which the solder ball melts (collapses) during reflow, such as the joints in PBGAs, TBGAs, and CSPs. Non-collapsible solder joints are those that do not melt during reflow like the

Substrate Metallization	Intermetallic Compounds Formed with Sn
Cu	Cu_6Sn_5, Cu_3Sn, Cu_4Sn
Ni	Ni_3Sn_4

Table 1.1.2-1. *Intermetallic compounds formed between tin and most common BGA pad metallizations*[1,2]

In order to be able to form an intermetallic layer between the solder and the substrate, one must first remove the oxide layer from the surfaces of the solder and the substrate metallization. To remove these metal oxides one uses what is called a "flux." A flux is basically an organic solution that is active only at temperatures close to the melting temperature of the solder in question. Fluxes are designed to dissolve the oxide layer at high temperatures to reduce the length of time the clean surfaces are exposed to the atmosphere (oxygen) prior to the formation of the intermetallic compound (wetting).

1.1.3. Solder Reliability

A solder joint is subjected to strains from many sources. For example, temperature gradients caused when the device is powered ON can lead to a variety of tensile and/or shear strains on the solder. Ambient temperature fluctuations cause temperature fluctuations on the package and the board, which is also a source of strain. Vibration due to in-service conditions can also impose strains on the solder, as well as handling during manufacturing, deformation due to water absorbed by the package and/or board, etc.

Thermal excursions are usually the most critical source of strain; they are common for every device, and they occur in a cyclic fashion leading to a metallurgical phenomenon called creep-fatigue[i]. These thermal excursions might be caused either by Joule heating[ii] (internal) or by changes in the ambient temperature. Because solder usually joins two

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high-Pb solder balls on a Ceramic BGA.

[i] Creep-fatigue is usually defined as the combined effect of cyclic loading and deformation at high homologous temperatures.

[ii] Joule Heating is an increase in temperature due to an increase in current density.

materials with different coefficients of thermal expansion (CTE), a cyclic strain is imposed on the solder.

Solder in electronic packaging is always liable to be strained to greater or lesser degree depending on the device and/or the working environment. Fatigue and creep-resistance of the solder alloy are usually referred to as the most critical factors affecting the in-service reliability of solder joints. Normally, in the solder community, reliability is strictly linked with fatigue and creep for the reasons just described. It is certainly very important to understand and improve the fatigue and creep resistance of solder in order to be able to make more reliable solder joints. But to take advantage of all the valuable knowledge gathered through the years on the optimal microstructural configuration of different solder alloys, we must gain tight control of the processing of such joints. Processing defects can, for example, shadow the improved fatigue resistance of a finer grained solder. Or the presence of a thick intermetallic layer may produce a brittle failure at very low strains. Lastly, as will be shown in the following sections of this work, the presence of pores can considerably deteriorate the mechanical strength of the solder joint by providing a path for easy crack formation and rapid propagation.

1.1.4. Ball Grid Array and Flip Chip Technologies

IBM first introduced the area array concept in 1962 as the Controlled Collapsed Chip Connection (C4) method[4]. The C4 method was originally developed to place the contact in the back of the die in the form of solder bumps by evaporating a fixed composition of lead tin solder with the help of a mask. Today, this process has been modified by different companies, and in general is called Flip-Chip. Ball Grid Array (BGA) technology was developed later (in the 1980's) based on the C4 concept. This time the contacts were placed on the back of the chip carrier as solder balls or solder bumps.

The semiconductor industry's fast trend of both increasing the number of transistors per die, and shrinking the device's size by the early 1990s forced smaller and smaller spacing on peripherally leaded packages to a point where yield and throughput were becoming difficult tasks for many chip manufacturers[6]. Peripheral leaded packages at 0.4 mm pitch (center to center lead spacing) and below were difficult to handle, and usually have very

low manufacturing yields. The industry's reaction to this situation was to adopt first Pin Grid Array (PGA) Technology, and later BGA technology, which places the contacts (I/Os) on the backside of the package rather that at the periphery. BGA technology allowed the packaging industry to incorporate high pin counts (>250) without major manufacturing changes[5].

The BGA is a cost-effective, high I/O surface mount package. It utilizes an array of solder balls on the underside of the package to provide a high interconnection density. The BGA offers significant advantages over conventional leaded plastic packages[6]. One of them is that the solder bumped BGA can be attached with extremely low solder-joint defect levels. Another advantage of BGAs over their leaded counterparts is the elimination of lead inspection, and lead straightening.

The most common types of BGA packages are the plastic ball grid array (PBGA), ceramic ball grid array (CBGA), tape automated bonded grid array (TBGA), and chip-scale package (CSP), shown in Figure 1.1.4-2. From a solder perspective, PBGAs, CSPs, and TBGAs are equivalent in the sense that all of them use eutectic (63 Sn-37 Pb) lead-tin solder to produce a "collapsible solder joint." In the case of CBGAs, a "non-collapsible" high melting point solder ball (90Pb/10Sn) is joined to the ceramic chip carrier and the board by eutectic lead tin solder paste.

Along with any new technology comes a series of questions and uncertainties. For example, there are some disadvantages and open questions associated with BGA packages, specifically with respect to the reliability of their solder joints. Area array solder interconnects are less compliant than the conventional peripheral leaded joints[2]. This reduced compliance, where all the strain is taken up by the joints rather than the leads, is often linked with early failures under thermo-mechanical stress. This makes collapsible BGA joints particularly susceptible to defects such as poor wetting, insufficient solder, foreign contamination, and pores.

1.2. Effect of Porosity on the Solder Joint Strength

Before the implementation of BGA and Flip-Chip packages, solder was mainly used to "glue" the package's leads to the board. In this case, most of the mechanical strain (produced by the coefficient of thermal expansion (CTE) mismatch between the package and the board) is alleviated by the elastic deformation of the lead. BGAs eliminate the leads and substitute them with solder balls or solder bumps. Solder in BGAs, therefore, provides the only mechanical and electrical link joining the package to the board. As a consequence, any solder-joint defect in a BGA package becomes much more important and detrimental to the reliability of the device.

Pores are a common defect in collapsible BGA solder joints. In particular, porosity is more severe in BGA packages than in traditional leaded packages, presumably due to the increased difficulty of outgassing (due to the geometrical constraint of a "sandwiched" solder joint). Traditionally, pores have been believed to weaken the solder joint. The frequent occurrence of large pores on BGA packages has led to questions about the role of such defects on the reliability of BGA packages[7].

Pores are often referred as to voids in the electronic packaging literature. The word "pore" was chosen in this work to designate the spherical cavities found in solder joints after solidification. The reason pore was chosen is that traditionally "pore" is used to designate the cavities left in a metal casting due to entrapped gas or solidification shrinkage. On the other hand, it is common to use void to designate the empty space or cavity formed during service, after the part has been manufactured. In any case, the word pore in this work has the same meaning as the word void in some of the solder literature.

Pores have been reported to affect the mechanical properties of joints[8]. Xie, Chan, and Lai showed that pore-free, specially made joints had 20% higher average shear strength than a joint containing pores[9]. They also reported that the average fatigue life of pore-free, specially made joints increased up to 150% from the normal joints containing pores. According to Der Marderosian et al., the fatigue lives of a leadless chip carrier's joints are dramatically affected by the presence of bubbles[10]. Liu and Mei pointed out that

sometimes a crack in a solder joint consists of various pores of different sizes connected by some major macrocrack, and they speculated that pores might be the initial damage mode of SMT solder joints[11].

In contrast, recently some researchers have reported the opposite, that pores do not affect the reliability of PBGA solder joints[12]. Consequently, a controversy has apparently developed regarding the effect of pores on the reliability of PBGA packages. Banks, et al., concluded that pores caused no negative effect on PBGA board level reliability[12]. Furthermore, their results showed that PBGA solder joints with pores (up to 24% of the pad area) had 16% better reliability than joints without pores. The authors base these conclusions on a set of experiments in which they tested PBGA samples with various degrees of porosity and compared their performance under thermal cycling with a control set of pore-free PBGA packages. The packages with porosity were assembled using standard solder paste. The pore-free packages were assembled using paste flux and solid solder balls. Pore detection was done using X-ray inspection and metallographic cross-sectioning. Hopefully, the results presented in this thesis work will help clarify the question of the role of pores on the reliability of collapsible BGA solder joints.

Before trying to come up with inspection standards and part rejection criteria, therefore, it is important to first understand the influence of pores on the mechanical properties of collapsible BGA solder joints. The present work addresses this issue by manufacturing samples with different degrees of porosity and testing them under a shear load.

1.3. Pore Formation

Pores that are commonly observed in many metal castings such as steels and aluminum alloys are also observed in surface mount (SMT) solder joints. In general, pore formation in metals is caused in the solidification process by one of three reasons: solidification shrinkage, entrapped gases, and dissolved gases[13]. Additional reasons specific to soldered joints are printed circuit board outgassing, and contamination of the parts. Several techniques have being developed over the years to eliminate pores in structural alloys. Techniques such as directional solidification, addition of oxygen and nitrogen getters, and ar-

gon bubbling have, among others, proven to work for the aluminum and steel industries[13]. Unfortunately, the situation is more complex for SMT solder joints, as there always exists a source of entrapped gases (flux), and additionally, it is extremely difficult to control solidification direction/rate in small (4-30 mil) solder joints. The complexity of the problem in the case of SMT solder joints partially explains why we still have pores in most SMT solder joints.

Most of the research on porosity on solder joints seems to agree that pores are formed due to entrapped flux residues[9,14,2]. Other possible causes often found in the literature are solidification shrinkage of the eutectic Pb/Sn solder (about 4%), outgassing of the printed circuit board, and moisture. Pad metallization contamination is not usually considered as a possible cause for porosity in solder joints. Few researchers have reported this; for instance, Kramer reported an increase of porosity with increasing Au thickness in eutectic Sn/Pb creep samples[3,15]. Recently, Bulwith pointed out that large concentrations of pores could be created when soldering to plated layers having organic materials in them[16].

A simple way of determining if the flux is responsible for porosity is to make a solder joint without using flux. However, flux is necessary to remove the oxide layer from the copper pad, and the tin oxide from the surface of the solder, and thus making a fluxless solder joint is not trivial. The inherent difficulty of fluxless soldering can be understood on the basis of two thermodynamic equations, which govern wetting[17]. The first equation is the Young-Dupre equation, which describes the driving force for wetting in terms of the contact angle θ and the surface energies:

$$\cos(\theta) = \frac{(\gamma_{sv} - \gamma_{sl})}{\gamma_{lv}}$$

Where γ_{sl}, γ_{lv}, and γ_{sv} are the respective surface energies of the solid-liquid, liquid-vapor, and solid-vapor interfaces. The other equation is the Gibbs relation, which states that any spontaneous change that occurs at an interface must lower the interfacial energy:

$$\Delta\gamma \leq 0$$

The oxidation of the Cu pad reduces the γ_{sv}, increasing the contact angle θ, and thus lowering the driving force for wetting. The addition of a thin Au coating would protect the Cu from oxidizing and also provide a low contact angle surface between the molten solder and the pad. Then, when assembling a fluxless joint on a Cu substrate, a Au coating assures that when the solder melts and quickly dissolves the Au layer, a clean, oxide-free Cu surface is exposed. In industry, a layer of Ni is deposited on top of the Cu and then Au is deposited on top of the Ni. Also, in industry there is no need to coat the Cu with a layer of Au, the oxide Cu forms is readily dissolved by the flux.

This work involved both flux and fluxless soldering with different pad metallizations to confirm the sources of porosity on collapsible BGA solder joints. A fluxless experiment (samples assembled without using flux) was designed to compare with a commercial reflow process (with flux) and therefore confirm the effect of flux as the primary cause of pore formation in SMT solder joints. A second set of fluxless experiments were designed to test the effect of different substrate's metallizations (hard-Au and soft-Au) on pore formation in the absence of flux.

1.4 Reducing Porosity

Since everyone seems to agree that entrapment of flux residues is the primary cause of pores in collapsible BGA solder joints; most of the research on how to reduce porosity has focused on flux evaporation control[7,18]. The basic conclusion from these efforts is that one must optimize the reflow profile for each specific flux, and each specific soldering job. The recommendations and guidelines given by these authors certainly provide a very good start on reducing porosity.

Another way to reduce porosity, in theory, would be to increase outgassing by increasing the time the solder stays in the molten state. This method would potentially reduce porosity regardless of its source (such as metallization contamination). A series of experi-

ments were designed to study the effect of increasingly longer times at the molten state on porosity.

2. Experimental Procedure

2.1. General procedures

Commonly, BGA solder joints are studied using commercial BGA packages assembled onto PCB boards, and for some cases this might be the best approach. But, if one wants, for example, to directly study the mechanical strength of the solder joint, it is important to know that when a load is applied the deformation is taking place only at the solder joint and not in the substrate material. Test samples were designed to reproduce solder joints typical of a BGA package, but on a rigid substrate; these samples are referred to as *BGA Samples* in this work. BGA samples were assembled and tested in shear. Porosity was characterized mainly by analyzing fracture surfaces using a Scanning Electron Microscope (SEM), and additionally by analyzing cross-sections of untested and tested soldered joints on the optical microscope. Energy Dispersive Spectroscopy (EDS) was used to determine composition of the intermetallic phases formed. NIH Image analysis software was used to calculate pore diameter and pore-fraction from SEM micrographs.

2.1.1. BGA Substrates

The BGA substrates consisted of two copper coupons (6.6 cm x 2.2 cm x 0.16 cm) with a land pattern array on one face as shown on Figure 2.1.1-1. The pad array was created by applying a liquid photo-imageable solder mask (EPIC 200 Series) covering the surface of the copper coupon, but leaving open an array of 9 x 9 circular pads. The solder mask was around 25 μm (1 mil) thick for all the samples. The pad array was made out of 9 x 9 circular pads of 0.66 mm (26 mils) in diameter, spaced at 1.27 mm (50 mils) pitch as shown in Fig. 2.1.1-1.

2.1.2. Pad Metallization

Three different substrate metallizations were used: copper, hard gold over copper and soft gold over copper. The copper metallization was automatically produced by the way BGA samples were made. The underlying copper was exposed through circular openings on the solder mask. Electroplating hard and soft Au on the copper coupons after solder mask layout produced the gold metallization.

Both hard-Au and soft-Au coatings used in this work are electroplated from an acid gold bath. A hard-Au coating is produced from an acid gold process that produces a cobalt hardened gold deposit, with a composition of 99.7-99.9% Au and 0.1-0.3% Co. In this work, "soft Au" was used to designate an acid pure gold process that produced a gold electrodeposit of 99.9+% purity, termed soft gold because it has the lowest harness of the gold electrodeposits. Both Au electrodeposits were between 1.52 μm and 2.54 μm thick, which corresponds to 0.15% to 0.38% of the solder volume.

2.1.3. *Assembly of Shear Samples*

When applicable, a thin layer of RMA flux was applied to the pad array of both copper coupons. Then, with the help of a custom-built vacuum pick-up device (shown in Figure 2.1.3-1), a set of 25 spheres was placed on top of the pads of one of the copper coupons. Two pieces of wire (0.5 mm or 20 mils in diameter) were then placed on both sides of the pad array to serve as spacers during reflow. Next, the second copper coupon was placed on top of the one with the spheres and the spacers on it. The assembly sequence is shown in Figure 2.1.3-1. Finally, the two copper coupons with the spheres and the spacers in between were clamped with binder clips and placed in the reflow furnace.

2.1.4. Shear Testing

Shear testing was carried out using a custom-built load frame shown in Figure 2.1.4-1. This load frame consists of a stepper motor, a 30:1 reduction box, and a screw driven micro actuator. The strain rate for all the shear tests was 10^{-4} s^{-1}. The samples were placed in the friction grips and tightened. Figure 2.1.4-2 shows a BGA sample under a shear load. The strain was measured by a 1-inch extensometer placed between the two grips as shown in Figure 2.1.4-1. A PC computer collected the load and strain data through a data acquisition card.

2.1.5. Microscopy

A TOPCON 20 KeV scanning electron microscope was used for the SEM work. The sample preparation for scanning electron microscopy (SEM) analysis of the fracture surfaces consisted of:

a.) Careful cleaning of the samples in an ultrasonic cleaner using acetone to remove volatile residues from the surfaces. (This step was not used when flux and polymer residues were investigated).

b.) Platinum or carbon coating of the sample to avoid "charging" under the electron beam. The samples were coated in an *Edwards Sputter Coater S150 B.*

For cross-section analysis, the BGA substrates were mounted in a room-temperature mounting material. Then, they were precisely sliced using a Struers ACUTONE 5 high-speed diamond saw. Care was taken not to heat up or deform the samples while mounting or cutting them; the mounting epoxy hardens at room temperature, and high-pressure lubricant jets lubricate the saw. All samples were ground with successively finer silicon carbide paper down to 600 grit. Very little pressure was applied during grinding to avoid "smearing" of the solder. The samples were then polished by hand using 1.0 μm alumina suspension in distilled water until all the scratches from the grinding stage disappeared. The final polishing step was done using a suspension 0.05 μm alumina in distilled water until the surface of the solder joint appeared smooth under the optical microscope at 400x. For SEM analysis of the cross-sections, the samples were coated with either platinum or carbon as described earlier.

2.1.6. Image Analysis

SEM micrographs were scanned using a UMAX vista S8 scanner. NIH Image software version 1.58 was used to obtain pore diameter, pore size distribution and pore-fraction from the SEM images of the fracture surfaces.

2.2. Effect of Porosity on the Solder Joint Strength

In order to achieve different levels of porosity, BGA samples, *with bare-Cu metallization,* were assembled *using flux* and different reflow profiles. Different degrees of porosity were obtained by controlling heating rates and holding times. Slow heating rates and short hold times produced the highest degrees of porosity. Faster heating rates and longer hold times were used to produce less porosity (see Table 2.2-1). The porosity obtained after a particular reflow profile was not 100% predictable. The suggestions given by

Hence et al., were helpful in achieving different levels of porosity[18]. All the samples were assembled with 0.762 mm (30 mils) eutectic (63 Sn-37 Pb) solder balls, RMA flux and a joint height of 0.5 mm (20 mils).

Porosity Level	Heating Rate	Holding Time at 150°C	Holding Time Above 190°C	Peak Temperature (°C)	Flux
Low	FAST	LONG	LONG	220	RMA
Medium	FAST	SHORT	SHORT	220	RMA
High	SLOW	SHORT	SHORT	220	RMA

Table 2.2-1. *General guidelines followed to obtain different degrees of porosity.*

All BGA samples were tested under a shear load in a custom-built load frame (Fig. 2.1.4-1). The strain rate for all shear tests was 10^{-4} s^{-1}. The joints in all of the tested samples were identical in terms of joint height, number of balls, and solder composition. SEM micrographs of the fracture surfaces of the tested samples were scanned and analyzed using NIH-Image software to determine the fraction of pad area covered by pores.

2.3. Pore Formation

Three different configurations of BGA samples were assembled, and are described in Table 2.3-1. Set 1 was assembled using BGA substrates with bare copper pads and RMA flux. Set 2 was assembled using BGA substrates plated with soft gold over copper without flux. Set 3 was assembled with BGA substrates plated with hard gold over copper, and no flux. All three sets used 0.762 mm (30 mils) eutectic Sn/Pb solder balls and a joint height of 0.5 mm (20 mils).

BGA Sample Set	Pad Metallization	Flux	Solder Composition	Spacer Diameter (mils)
1	Bare Cu	RMA	63Sn-37Pb	20
2	Soft-Au/Cu	NO	63Sn-37Pb	20
3	Hard-Au/Cu	NO	63Sn-37Pb	20

Table 2.3-1. *Description of BGA samples for pore formation experiments.*

Samples from set 1 were manufactured following the reflow profile indicated by the flux manufacturer. The second and third set of samples, soft-Au/Cu with no flux, and hard-Au/Cu, were reflowed in a custom-built furnace, shown in Figure 2.3-1. This furnace is a sealed glass tube with gas inlets and outlets, and two commercial 500-Watt lamps, modified to fit around the glass tube, produce the heat. This furnace was designed to achieve very high heating rates (up to 350° C/min), under a vacuum (1 μATM) or an inert atmosphere.

The reflow profile used for sets 2, and 3 was a single ramp from room temperature to 340° C at about 350 °C/min, with a hold at 340°C for 2 min. All the samples from sets 1, 2, and 3 were cooled at air. After testing the samples from sets 1, 2 and 3 under a shear load, the corresponding fracture surfaces were analyzed using a scanning electron microscope (SEM).

2.4. Reducing Porosity

To investigate reducing the porosity of collapsible BGA solder joints, two configurations of BGA samples were assembled. Set 4 was assembled using bare-Cu pads, and RMA flux (see Table 2.4-1). Set 5 was assembled using hard-Au/Cu pads and RMA flux (see Table 2.4-2). To follow the evolution of porosity it is desirable to start with high degrees of porosity. The reason hard-Au coating was used instead of soft-Au for this experiment is because it produced considerably larger degrees of porosity. Sets 4, and 5 were reflowed up to 3 times using a conventional reflow profile. This means that they were held above the melting temperature of the solder for increasingly longer times. All of the samples were tested under shear with a strain rate of 10^{-4} s^{-1}.

Sample	Time above 190°C	# of Reflow Cycles
1-Cu	4 min.	1
2-Cu	8 min.	2
3-Cu	12 min.	3

Table 2.4-1. *Time above 190 °C and number of reflow cycles for samples from set 4 (assembled on* bare Cu pads).

Sample	Time above 190°C	# of Reflow Cycles
1-Au	4 min.	1
2-Au	10 min.	2
3-Au	15 min.	3
4-Au	27 min.	6

Table 2.4-2. *Time above 190 °C and number of reflow cycles for samples from set 5 (assembled on* hard-Au/Cu pads).

3. Results and Discussion

3.1. Effect of Porosity on the Solder Joint Strength

The data collected from testing samples with different degrees of porosity (all of them assembled on bare-Cu metallization and using flux) shows that the joint strength decreases as the porosity near the interface increases. Figure 3.1-1 is a plot of maximum shear stress versus effective area; it shows a linear relationship between the pore-free area fraction and the strength of the solder-joint. All the samples tested for Figure 3.1-1 fractured in a ductile mode as evidenced by their fracture surfaces. Figure 3.1-2 shows SEM micrographs of the fracture surfaces of these specimens. These micrographs are representative of samples with high, medium, and low degrees of porosity. For all levels of porosity shown, the solder joints failed through the bulk of the solder in a ductile fracture mode; none of them failed through the intermetallic layer.

It is important to note that the plot in Figure 3.1-1 specifically shows the influence of **pores near the interface** on the resulting shear strength. The effective area in Figure 3.1-1 refers to the pore-free area fraction of pad on a fracture surface. Unfortunately, the information obtained from a technique such as X-ray radiography[i] can not be interpreted in the same way. If pores are located in the center of the joint, X-ray radiography will detect them and include them in the porosity calculation. The effective area calculated from the fracture surfaces in the plot on Figure 3.1-1 shows the area covered by pores at the plane of the crack. If the pore area were to be calculated from an X-ray image, it is unlikely that a clear relationship between porosity and the mechanical strength of the joint would be found. The reason is that most x-ray techniques give a quantification of porosity throughout the volume of the solder and no distinction of location in the vertical direction.

All the samples tested for Figure 3.1-1 fractured in a ductile mode. The pores affected the ductile fracture by providing an easier, weaker path for the crack to propagate. Ductile fracture surfaces in metals are formed by microvoid nucleation, growth and

[i] In X-ray radiography, a source of x-rays is directed to the sample, some are absorbed and some pass through the sample and are picked-up by the detector. The resulting output is a gray scale image that represents differences in either density or thickness of the material.

coalescence[19]. The last part of this process, microvoid coalescence, occurs by localized internal necking of the intervoid matrix at the weakest sheet of microvoids. Therefore, pre-existing pores will speed up this process by skipping the nucleation and, in some cases, the growth stages. The pores present in the fracture surfaces remained spherical and had a smooth surface, which was indicative of no significant growth. The only deformation of the pores observed was a sharp increase in the void diameter at the fracture surface for some medium and large pores, which was indicative of very localized deformation (Figure 3.1-3).

The weakest sheet of micro-pores, or the weakest path for a crack to propagate, is determined by the pore diameter and spacing, and by the strain distribution within the sample. For a BGA or a Flip-Chip solder joint, the strain reaches a maximum along the interface. It has been shown through Moiré interferometry experiments that shear strain is almost constant at the center of the solder ball, but is 66% higher at the top right and bottom left corners[20]. Corbin showed, using Finite Element Analysis, that the plastic strain distribution within a eutectic solder ball had a maximum strain of 4.3% at the lower left corner, followed by 1.0-1.5% at the upper right corner, and 0.5-1.0% at the other two corners[21]. Therefore, the "weakest" sheet of pores has to be carefully defined. We have to account for the distance between the pores, the diameter of the pores, and the location of the pore in a non-uniform strain field.

A crack propagates naturally through the easiest (weakest) path it finds in the material. In this case, where the pores are located near the interface in a collapsible BGA solder-joint, this path forms by connecting such pores. Figure 3.1-3 shows a cross-sectional view of a solder joint after a shear test, where a crack runs along the interface and connects all the pores. This was observed in all the samples shown in Figure 3.1-1.

Because the stress is high near the edges, the crack always forms and propagates there regardless of the existence of pores. Figure 3.1-4 shows a cross-section of a BGA sample with a pore-free interface, in which it can be seen how the crack also starts very close to the interface, and propagates through the solder. Compared to the high pore-content joint

in Figure 3.1-3, the pore-free interface shown in Figure 3.1-4 had a crack with a more random path, which was dictated by the solder's microstructure[i]. For example, if we assume that the crack in Figure 3.1-4 starts at the right hand side of the joint, we see that stops at a Pb-rich dendrite (softer phase). Therefore, the presence of pores in this high stress-area (near the interface) allows easier crack propagation by internal necking of the interpore matrix

Another interesting result that emerges from the analysis of Figure 3.1-3 is that the crack did not go through the center of the large pores. Instead, it sectioned the pores near the interface. This phenomenon was observed in most of the samples tested for Figure 3.1-1. Fracture surfaces like that in Figure 3.2-5 show huge pores on the pad side, where a very shallow and large hole is observed. On the pad side, not shown, however we see a very deep hole indicating that the crack sectioned the pore very close to the interface rather than at the center of the pore. Figure 3.1-5 is a schematic representation of a crack in a sample with pores, and it shows how huge pores are sectioned near the solder-substrate interface.

After comparing the results just described with those reported by Banks et. al., it became evident that we should treat separately the case in which pores are on the interface and the case where the pores are in the center of the joint. As mentioned earlier, the stress distribution is significantly higher at the interfaces. Results from samples with porosity created by different sources point towards the conclusion that the case where the pores are farther away from the interface is much less severe. This is in agreement with Liu et al., where they report that the maximum stresses occur when the pores are near the top or the bottom interfaces.

Figure 3.1-6 shows that if one is not looking for them, small pores could easily be missed by a conventional pore detection method such as metallographic cross-sectioning. At a first look at the cross-section of the BGA sample in Figure 3.1-7, no pores were found.

[i] In this case, the solder's microstructure refers only to the chemical and physical distribution of the Sn, Pb, and Cu atoms (phases, and grain structure), and does not include the pores.

But after the fracture surfaces revealed (under the SEM) a high porosity all over the interface, a closer look (at 1000x) at the cross-section revealed a series of black circles where the pores were expected to be. It was then determined that such circles are in fact the same pores as the ones on the fracture surface. They appeared as black circles in the cross-sections because the slicing, grinding and polishing pushed the soft solder inside the pores. The most probable answer to this argument would be that X-ray radiography would not suffer from this problem, and it is true. But in this specific case, the X-ray radiography equipment available today would be very likely to miss pores below 25 μm in diameter, and certainly would not be able to detect pores in the order of 10 μ in diameter.

It appears that the controversy over the effect of pores on the reliability of BGA solder joints has its roots in the mistake of underestimating small pores, and characterizing porosity by pore diameter and pore area fraction alone. This work shows that pores (even 10-50 μm in diameter) located near the interface considerably deteriorate the strength of collapsible BGA solder joints. How close the pores are to the interface seems to be more important than the pore diameter or the pore population.

From the results just presented, it seems logical to define a solder joint inspection criterion that takes into account both pore diameter and total porosity, and pays special attention to the location of the pores, even accounting for very small ones located at the interface. More specifically, since the effect of pores on solder-joint strength is expected to strongly depend on their location with respect to the interface, inspection should first determine the location of the pores and then set specific criteria in terms of porosity allowed for that specific location. Further testing would be needed in order to define a precise and clear solder joint inspection criteria for porosity.

3.2. Pore Formation

Pores were observed at both interfaces in the samples assembled on bare Cu pads using flux (set 1). Porosity levels were virtually indistinguishable from the lower to the upper interfaces for the samples from set 1. Figure 3.2-1 shows a typical fracture surface for the samples from set 1. The average pore diameter of samples from set 1 was 16 μm, and

pores covered 30% of the pad area (calculated from SEM micrographs of the fracture surfaces. The pore size distribution is given in Figure 3.2-2. Most pores had a diameter between 5 μm and 25 μm.

Fluxless samples were manufactured using Au/Cu substrate metallization. The pad metallization of the first set of fluxless samples, set 2, was soft-Au on top of the Cu. The samples from set 2 had very little porosity; pores covered just 0.5% of the pad area (measured from the fracture surface), and the average pore diameter was 10 μm. Not all the solder joints had pores, and the ones that did had few very small pores. For samples from set 2, no significant difference in porosity levels between the lower and the upper interfaces was observed. Figure 3.2-3 is an SEM micrograph of a typical fracture surface from a sample from set 2. Figure 3.2-4 is a histogram showing the pore size distribution for samples from set 2, indicating that when no flux was used almost no porosity was obtained. This agrees with the results reported by other authors.

On the other hand, fluxless samples assembled on Cu pads plated with hard-Au, set 3, had enormous amounts of porosity. The fracture surfaces from set 3 showed many large pores at the upper interface, and small and medium pores at the lower interface. Figure 3.2-5 shows the fracture surfaces and the corresponding histograms for the upper and lower interfaces of a sample representative of set 3. The pores found at the upper interface (Figure 3.2-5 a), had an average diameter of 40 μm, and covered 35% of the pad area. The pores at the lower interface (Figure 3.2-5 b) covered just 18% of the pad area, and the average pore diameter was 28 μm.

It has been documented that a polymer is codeposited at the cathode with all hard Au, and in lesser quantities, with soft Au deposits that are plated from acid cyanide systems[22]. This polymer, trapped between the pad and the molten solder, is expected to become gaseous (evaporate) during reflow and produce pores. This explains the presence of large pores in the samples from set 3.

A residue with globular shape and around 2 μm in diameter was found inside some of the big pores on the fracture surfaces from set 3. Figure 3.2-6 is a SEM micrograph of that residue. Although, no chemical analysis was performed on these residues, the fact that this residue was found only in samples assembled on hard-Au plated pads leads me to believe that this residue could be the condensed polymer that produced the pore that it sits in.

Entrapment of flux residues during reflow has been widely recognized as the single most important cause of pores in solder joints[18]. By analyzing the results from sample set 1, and set 3 it was confirmed that, in fact, flux residues are responsible for pore formation in solder joints. For samples from set 1, assembled on bare-Cu pads using flux, porosity between 20% and 40% was observed at the pad area. On the other hand, virtually no porosity was observed (0.5% of pad area) for samples from set 2 assembled without flux.

It was also observed that even when no flux is used (set 3), it is possible to obtain considerable porosity (30% of pad area) in the solder joints. It seems evident that the source of these pores, created in the absence of flux, was the contamination of the Au metallization. Based on a study by Munier the contamination of the Au electrodeposits comes from a polymer of undetermined composition that is co-deposited during the plating process [22].

3.3. Reducing Porosity

Figure 3.3-1 shows the results from the shear tests as well as the results of the analysis of the fracture surfaces for the samples from set 5 (hard-Au/Cu substrate metallization, using flux). For these samples from set 5, the strength of the solder joint increased with increasing number of reflow cycles.

Figure 3.3-2 is a plot of the maximum shear stress versus time spent above melting temperature for the samples from set 4 (bare-Cu metallization). For these samples, as the number of reflow cycles increased the shear strength of the joint decreased, Figure 3.3-2.

The success in increasing the shear strength of the samples from set 5 (with hard-Au metallization) is due to the continuous decrease in porosity with an increasing number of reflow cycles, as shown in Plot (B) of Figure 3.3-1. On the other hand, the reason samples from set 4 (with bare-Cu metallization) were weaker as the time at peak temperature increased was not pore coalescence, but rather an excessive growth of the intermetallic layer. The fracture surfaces of the samples from set 4 showed a mix of brittle and ductile fracture modes after the second and third reflow cycles. All the samples from set 5, however, fractured in a ductile mode through the solder. The effect of the intermetallic layer growth on the fracture mode for bare-Cu samples is shown in Figures 3.3-3 and 3.3-4. Here, after the first reflow cycle the samples from set 4 and the samples from set 5 (bare-Cu and hard-Au metallization) fractured in a ductile mode through the solder. But after an extreme holding time of 120 min at 200°C the sample from set 4 (Fig. 3.3-4) fractured in a brittle mode through the ε phase (Cu_5Sn_6) of the intermetallic layer, and the sample from set 5 (Figure 3.3-3) still fractured in a ductile mode through the solder.

From the results in Figure 3.3-1 it can be inferred that pores do have a tendency to leave the solder, but the kinetics of the process appears to be very slow. After the first reflow cycle, large pores were found at the upper interface while fewer, smaller pores were found at the lower interface (Figure 3.3-5). Subsequent reflow cycles drove the small pores upward from the lower interface to the upper interface forming increasingly larger pores at the upper interface. Figure 3.3-5 and 3.3-6 show the evolution of the pores at the lower and upper interfaces for samples reflowed 1 and 2 times. Figure 3.3-7 shows the extreme case, were a sample was held at 200°C for 120 min. In Figure 3.3-7 almost no porosity is observed at the lower interface, and only one big pore was observed at the upper interface.

Holding the solder-joints assembled on hard-Au pads above 190°C successfully decreased porosity and therefore improved the strength of the joints assembled on hard-Au/Cu pads (Figure 3.3-1). By holding the solder in a molten state the pores have a better chance of escaping, and presumably time would allow smaller pores to move and eventually coalesce to form larger pores which move faster and are more likely to escape.

Just the coalescence of two pores into a larger one decreases the pad-area covered by pores. First, the contribution of any two pores to the pore area is the sum of their respective areas, but if they coalesce the diameter of the resulting pore is at least 63% less than the sum of the diameters of the original pores[i]. In the extreme case where a small pore and a big pore coalesce, the net effect is almost like getting rid of the small one, because the increase in diameter respective to the larger pore is very small. For example, two pores of 25 μm in diameter with a combined area of 982 μm^2 coalesce and form a pore of 31.5 μm in diameter with an area of 779 μm^2, effectively reducing the pore-area fraction by 20.6%. And a pore of 10 μm in diameter and a pore of 250 μm in diameter coalesce and form a pore of 250.05 μm in diameter.

[i] Since the volume is conserved, the volume of the two original pores has to equal the volume of the pore formed. Then the radius of the final pore (r_3) is related to the radius of the original pores (r_1, and r_2) in the following way: $r_3 = (r_1^3 + r_2^3)^{1/3}$.

4. Conclusions

From this work, five major conclusions can be drawn:

1) The shear strength of collapsible BGA solder joints decreased in a linear fashion with increasing porosity. Pores located close to the interface were found to be connected by a single crack after failure under a shear load indicating that pores provide a weak path for the crack to propagate.

2) Pores are formed due to two principal factors; the entrapment of flux residues (commonly accepted), and pad metallization contamination. Even in the absence of flux, considerable porosity was obtained on samples reflowed in substrates with a hard-Au metallization. Thus, it is important to keep in mind that pad metallization contamination can cause porosity depending upon the specific conditions of the plating bath.

3) Porosity was successfully decreased by subjecting the solder joints to increasingly longer times above the melting temperature of the solder. Long hold times proved to drive the pores from the lower to the upper interface, coalesce, and escape the solder. This was possible only on samples assembled on Au/Cu pads where the intermetallic layer showed no excessive growth even after 120 min at 200 °C. Then, in addition to reflow profile optimization, controlling the metallization contamination and prolonging times at molten state are a simple and industrially viable way to reduce porosity.

4) A pore inspection criterion, based on the results from this work, has to account for the location, size, and total fraction of pores, giving special attention to the cases in which pores are located near the interface. Also, the inspection technique has to be able to detect pores down to around 10 μ in diameter.

5) In general, there is no reason why these findings would not apply to Flip Chip solder joints, where the occurrence of pores is common too[14]. Although the solder composition is different (usually 90 Pb-10 Sn), and the size of the joint is considerably smaller (100-150 μm in diameter), Flip-Chip joints have the same basic geometry and shape.

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Figures

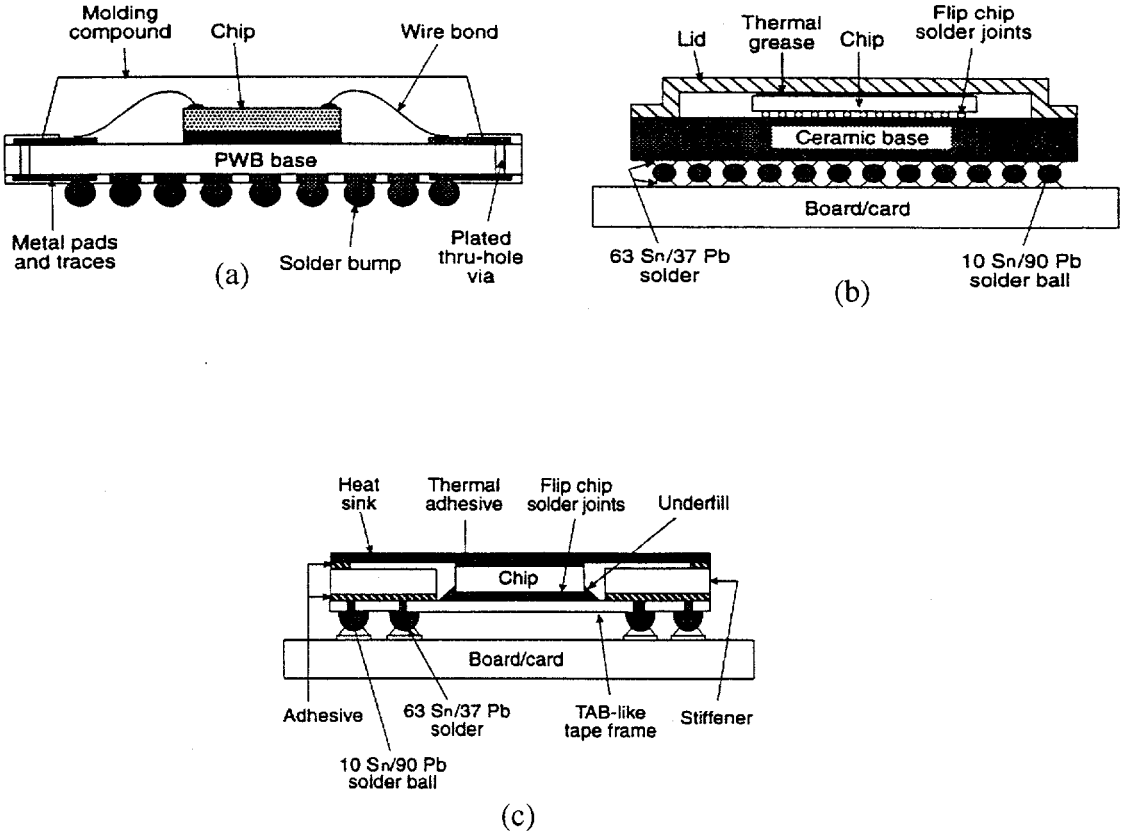


Figure 1.1.4-2. *Schematic illustration of a) Plastic Ball Grid Array (PBGA), b) Ceramic Ball Grid Array (CBGA), and c) Tape Automated Bond Ball Grid Array (TBGA). Taken from Ball Grid Array and Flip Chip Technologies: Their Histories and Prospects by Bruce M. Romanesco.*

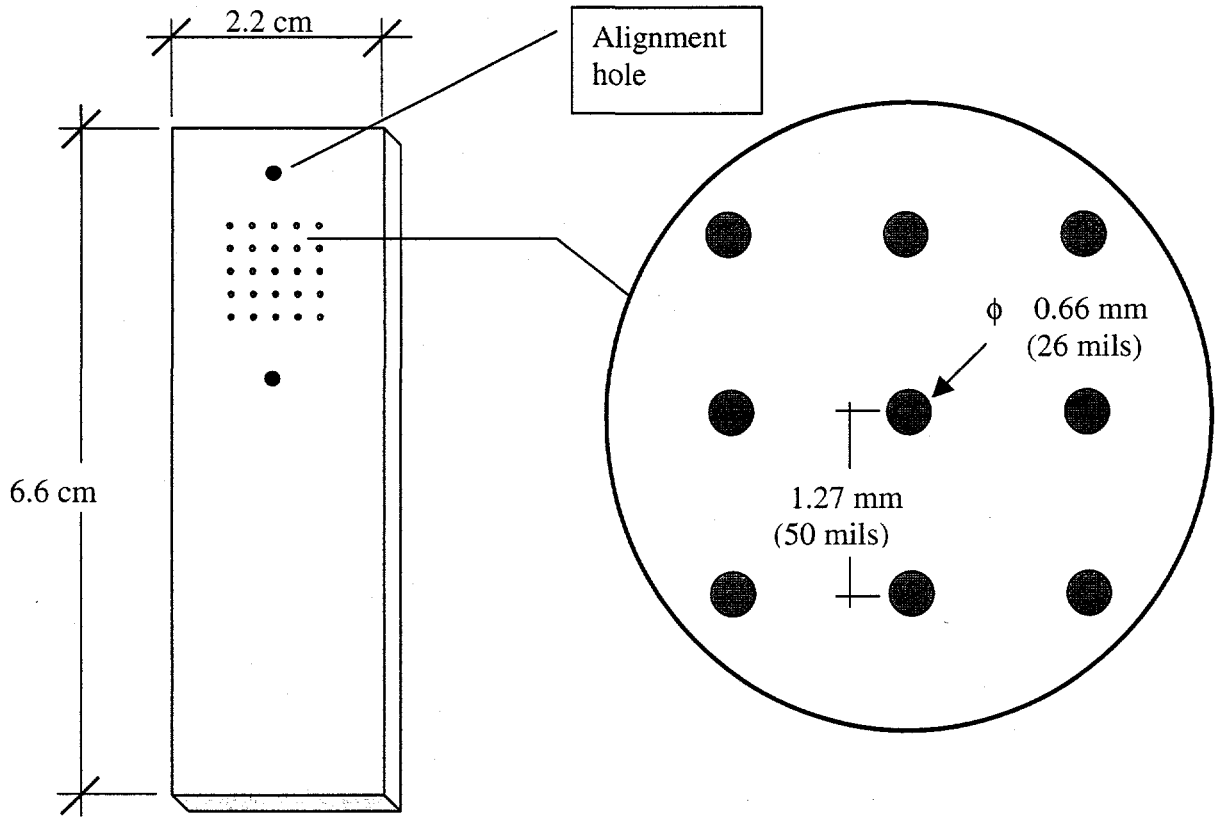
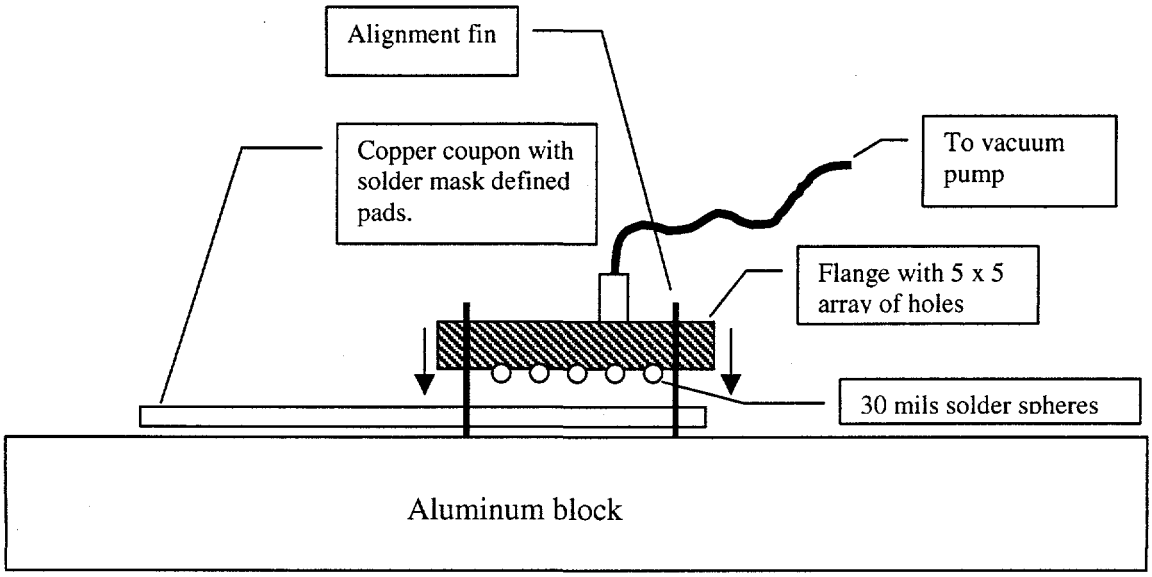
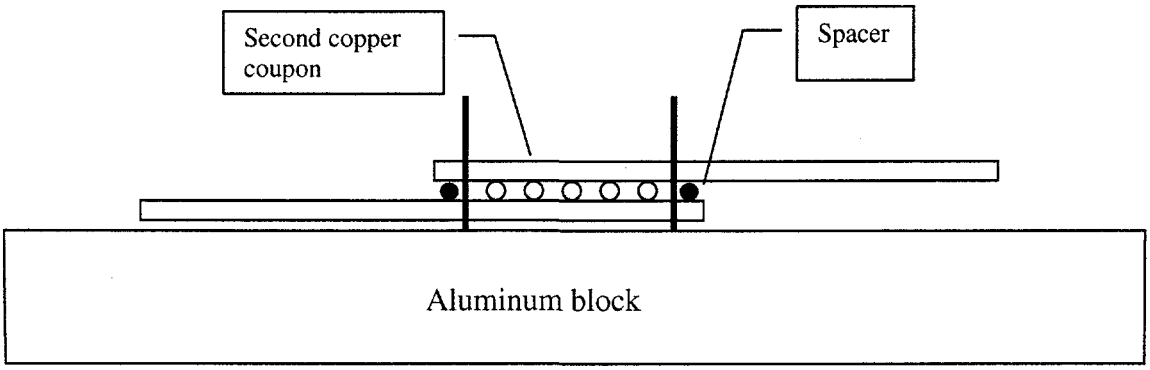


Figure 2.1.1-1. *Schematic illustration of a BGA sample*



(A)



(B)

Figure 2.1.3-1*. Assembly of BGA samples. A) Solder balls are placed on the coupon's pads with the vacuum pick-up device, B) The spacers are placed and the second copper coupon slides on top of the solder balls.*

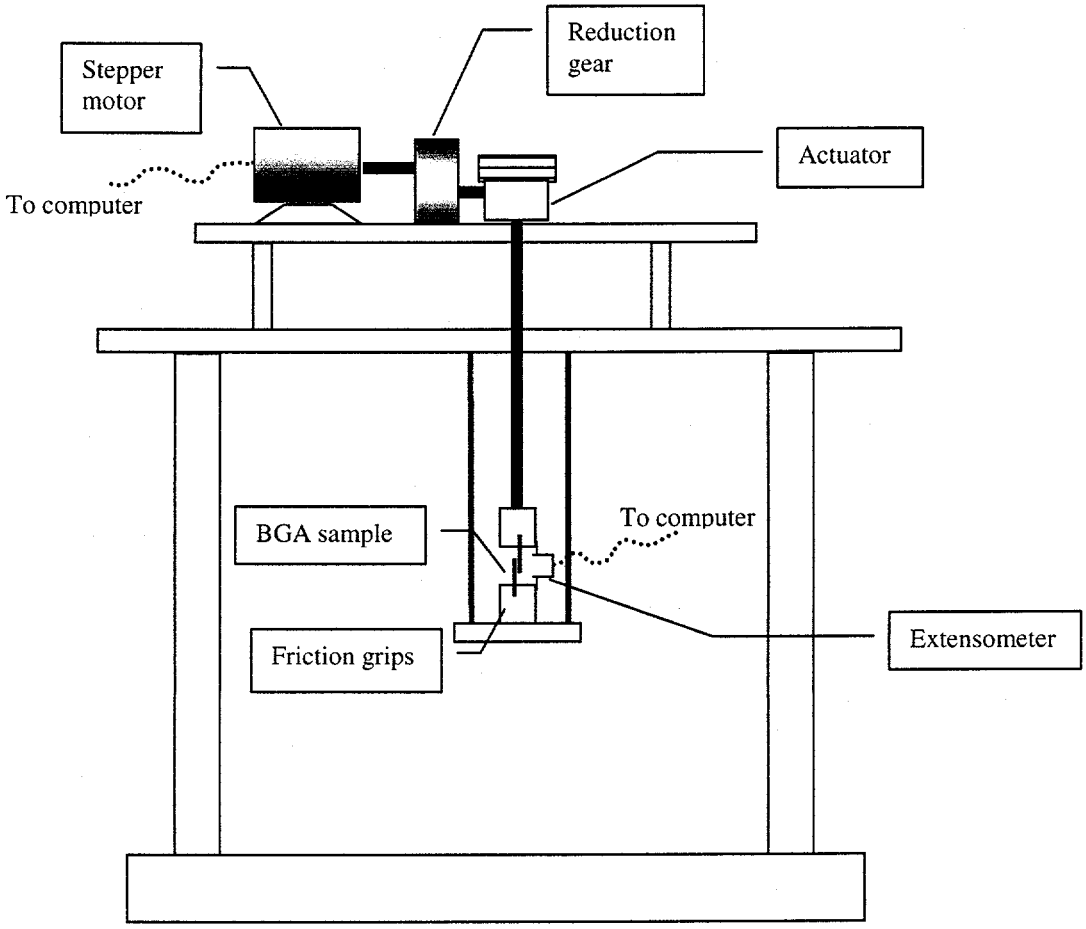


Figure 2.1.4-1. *Schematic illustration of the load frame used to test BGA samples in shear.*

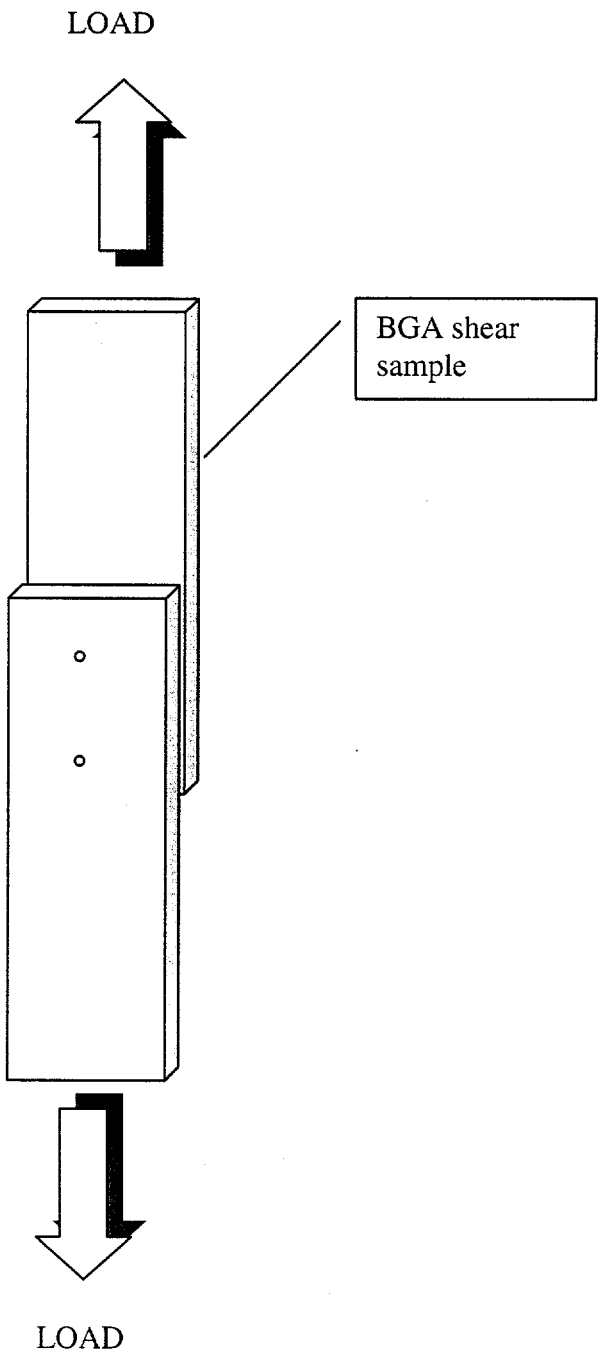


***Figure 2.1.4-2**. Schematic representation of a shear sample.*

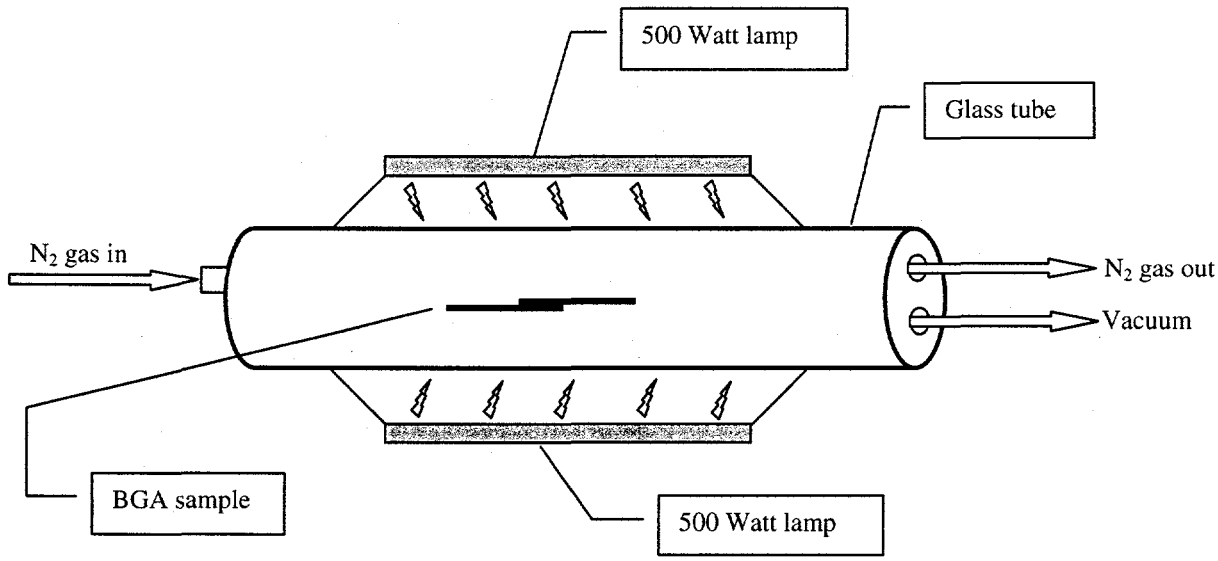


Figure 2.3-1. *Schematic illustration of the vacuum-furnace.*

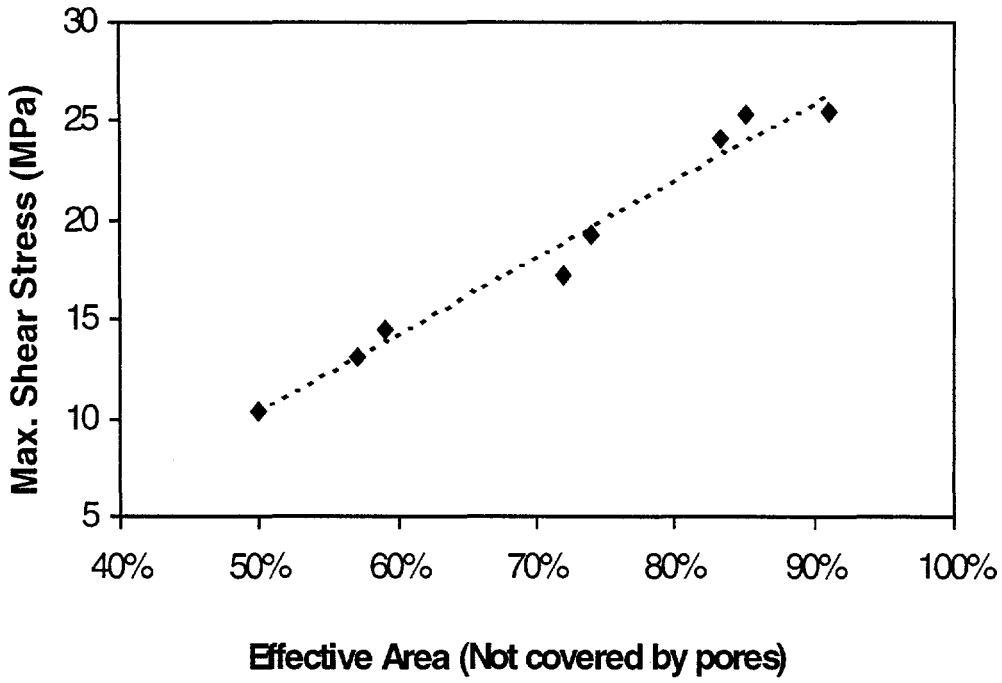


Figure 3.1-1. *Solder joint strength versus effective area (area not covered by pores), for samples assembled on bare-Cu metallization and using flux.*

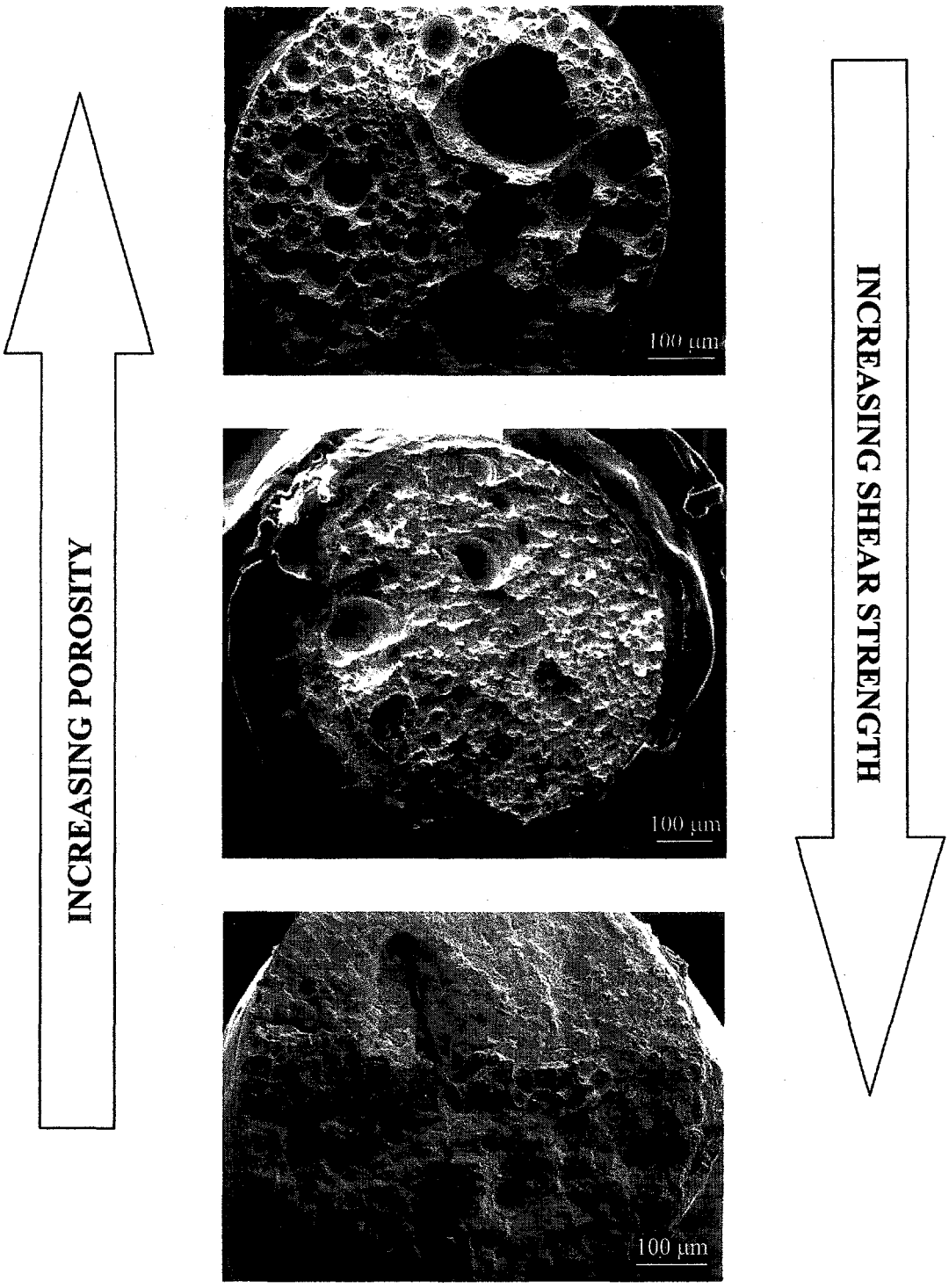


Figure 3.1-2. *SEM micrographs showing fracture surfaces of samples with different degrees of porosity.*

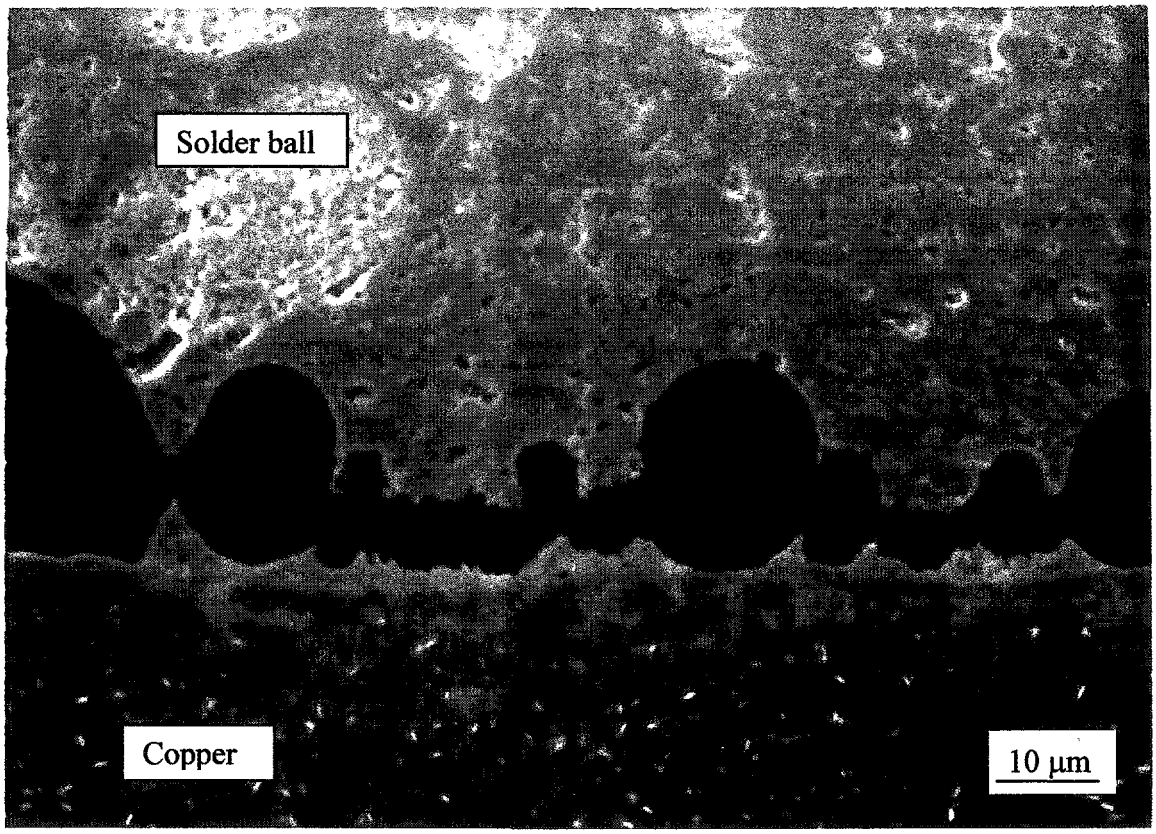


Figure 3.1-3. *SEM micrograph of cross-sectioned BGA solder joint after shear test, showing a crack connecting the pores close to the interface.*

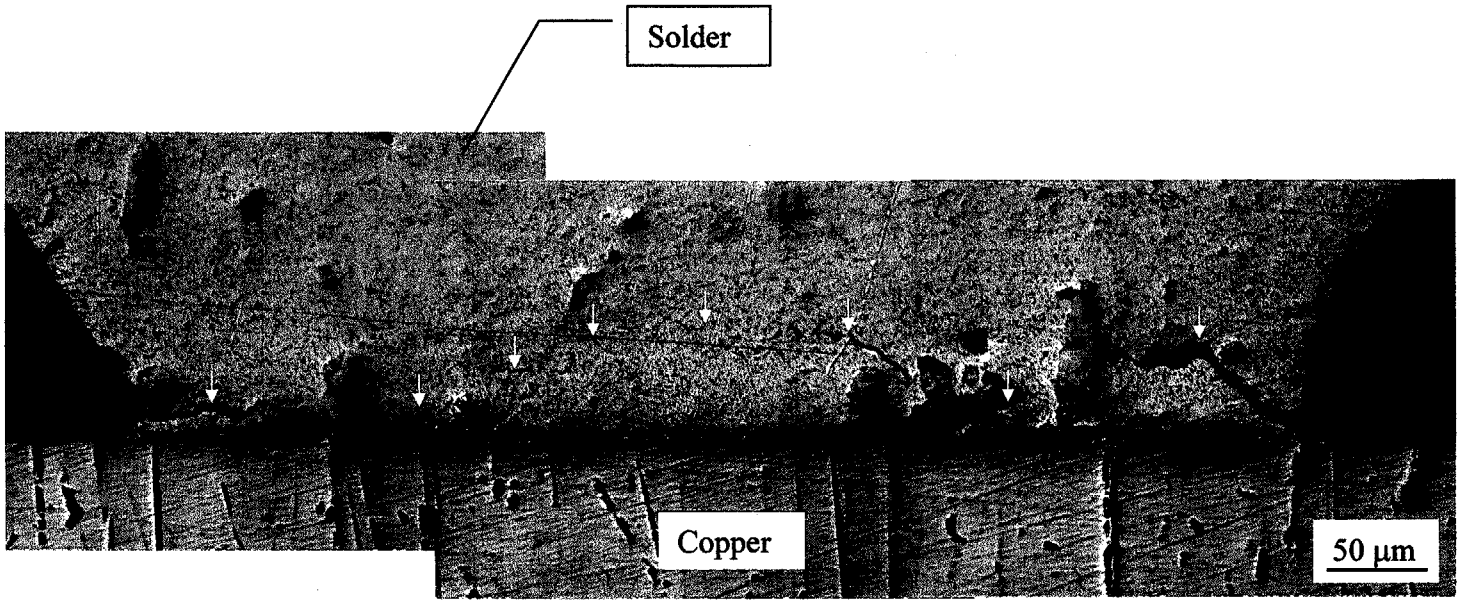


Figure 3.1-4. *Optical micrograph of a cross-sectioned BGA sample showing a crack running in pore-free interface. The white arrows indicate the path of the crack.*

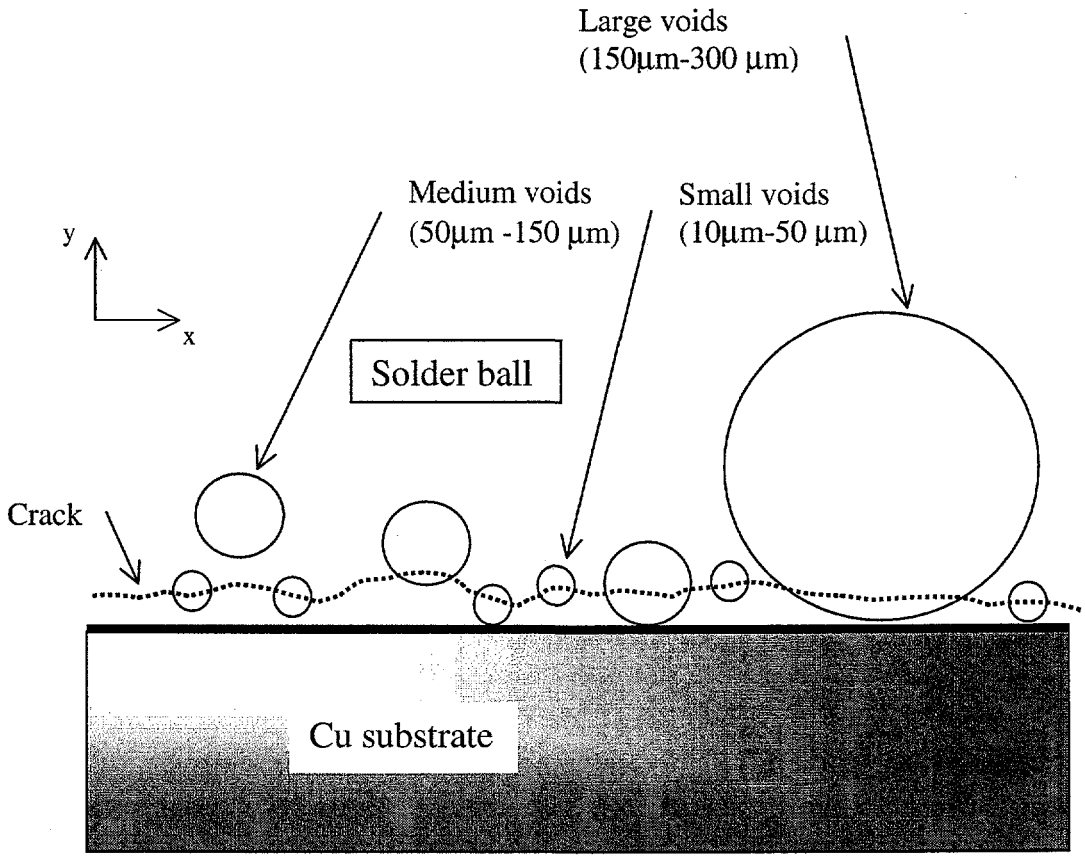


Figure 3.1-5. *Schematic representation of a crack in a sample with pores on the interface. Shows how a crack sections different pores depending on size and location with respect to the interface.*

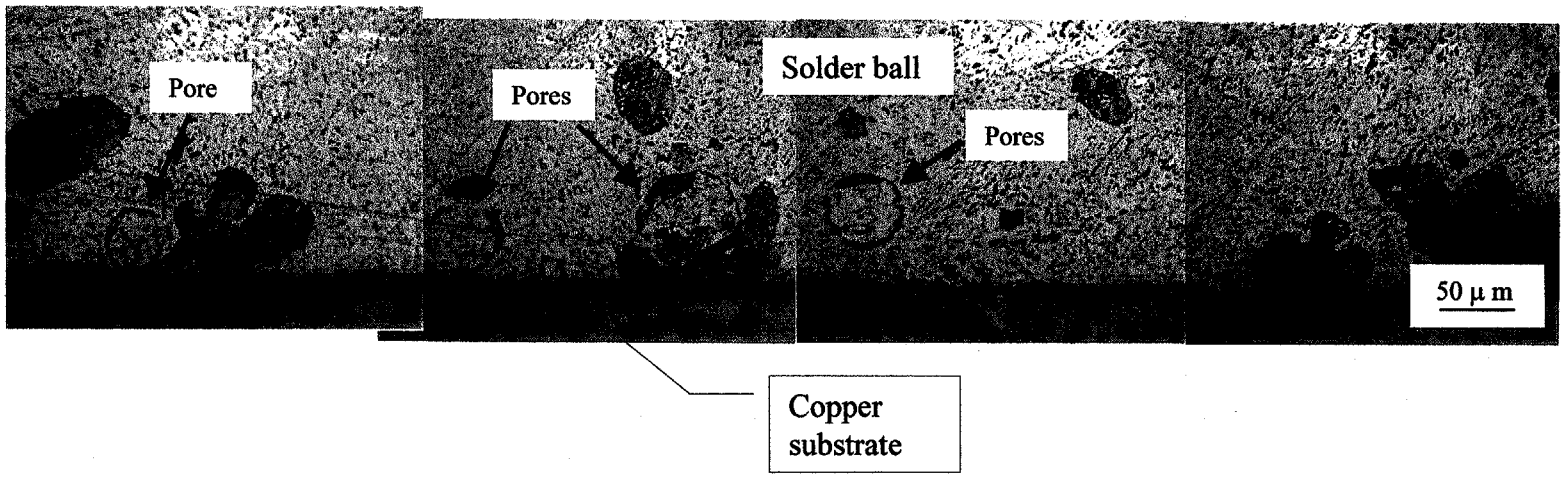
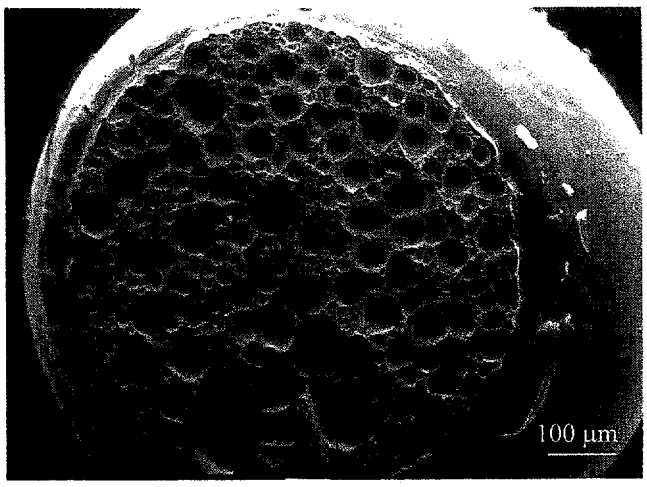
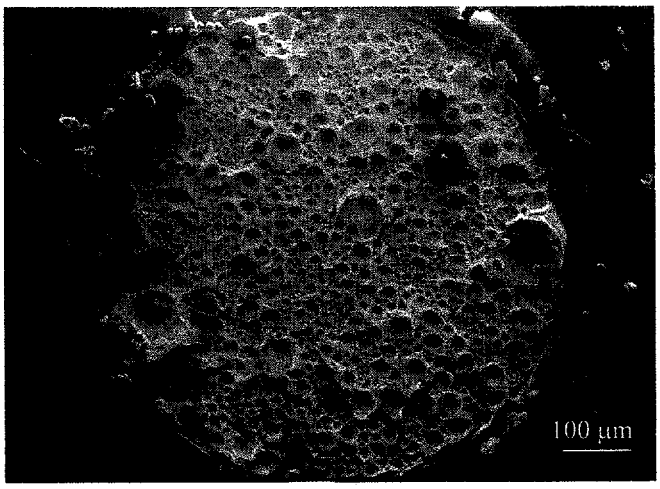


Figure 3.1-6. *Optical micrograph of a cross-sectioned BGA sample showing the outline of small pores close to the interface.*



(A)



(B)

Figure 3.1-7. *Fracture surfaces from the sample in the previous figure (Figure 3.1-6). A) Ball side, B) Pad side.*

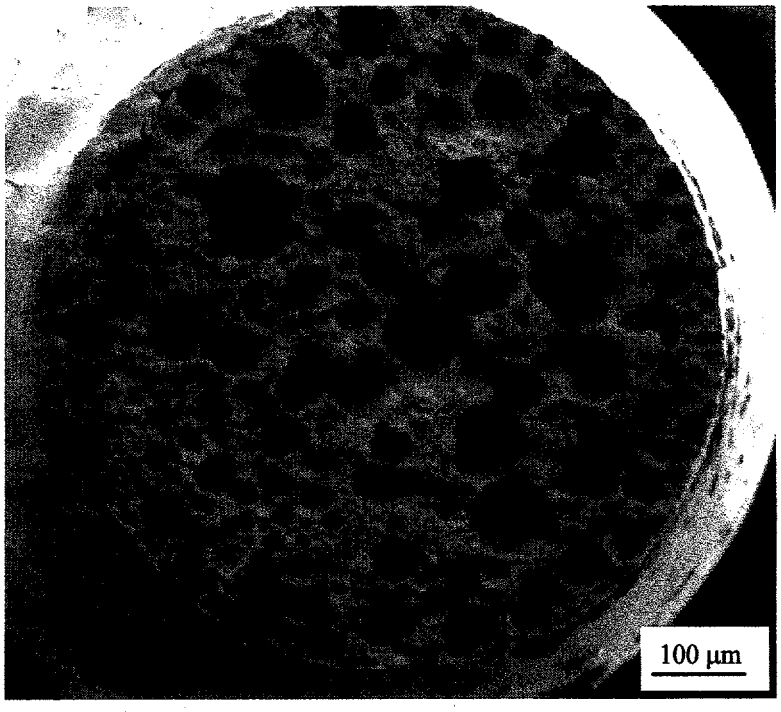


Figure 3.2-1 *SEM micrograph of the fracture surface of a BGA sample reflowed on bare-Cu pads with RMA flux (set 1).*

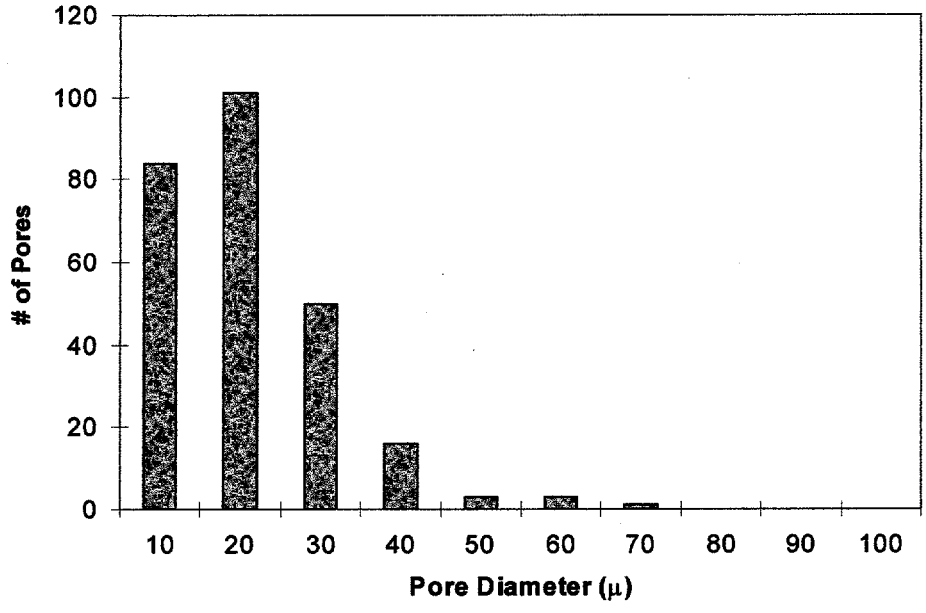


Figure 3.2-2 *Pore diameter histogram for a sample from set1*

Figure 3.2-3. *SEM micrograph of the fracture surface of a BGA sample assembled on soft Au/Cu pads and no flux (set 2).*

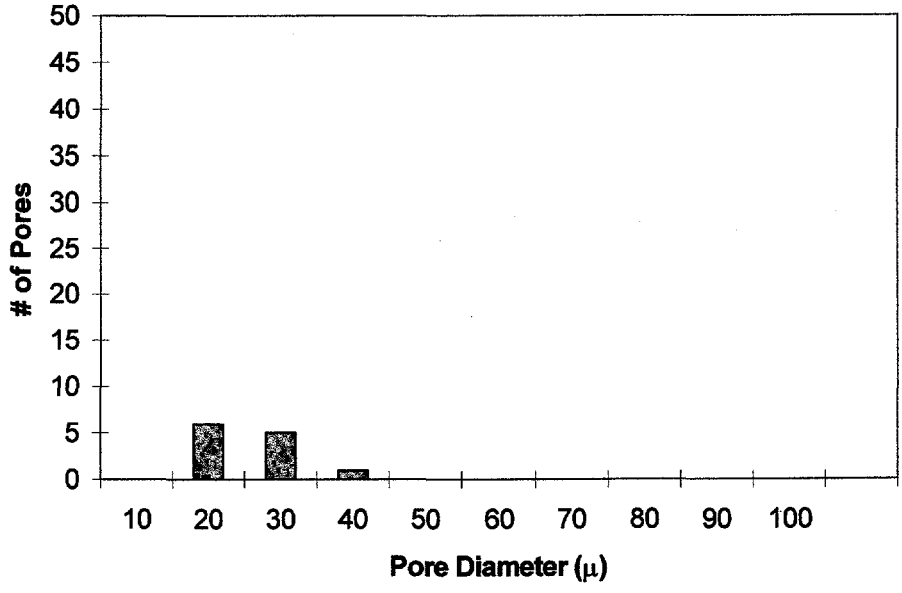
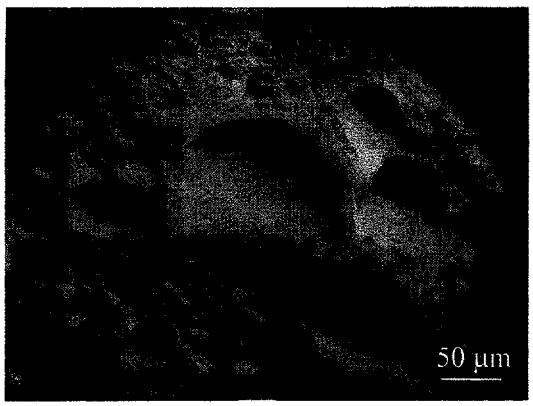
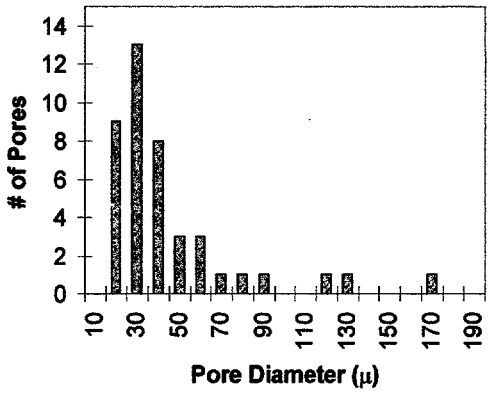
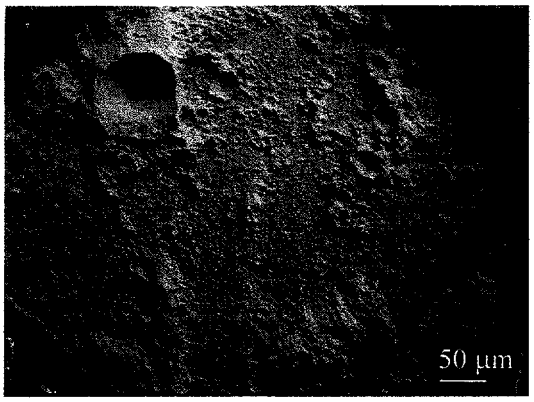


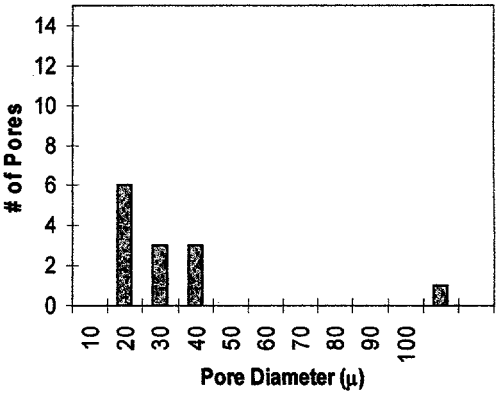
Figure 3.2-4. *Pore diameter histogram for a sample from set 2.*





(a: Upper Interface)





(b: Lower Interface)

Figure 3.2-5. *SEM micrograph of the fracture surface and histogram of pore content for samples from set 3 (hard-Au without flux). a) Upper interface of the joint, b) Lower interface.*

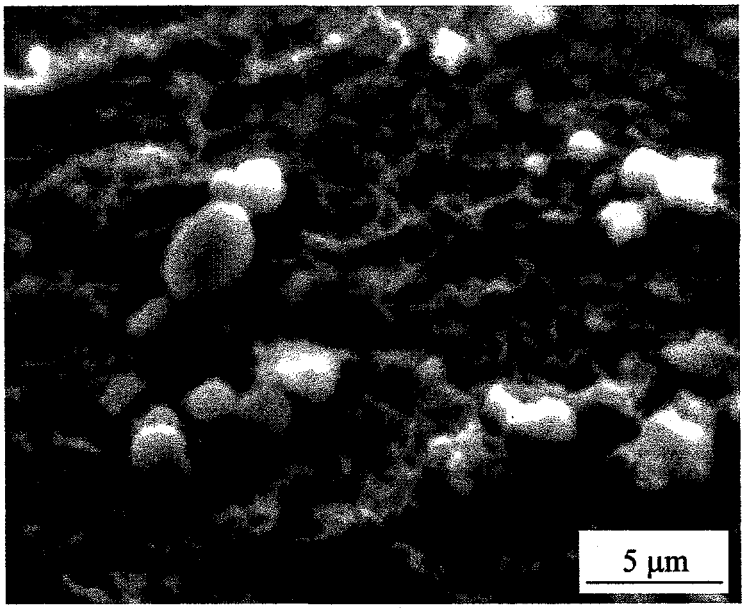


Figure 3.2-6. *SEM micrograph of presumed polymer residue inside a pore on a sample reflowed on hard –Au/Cu pads.*

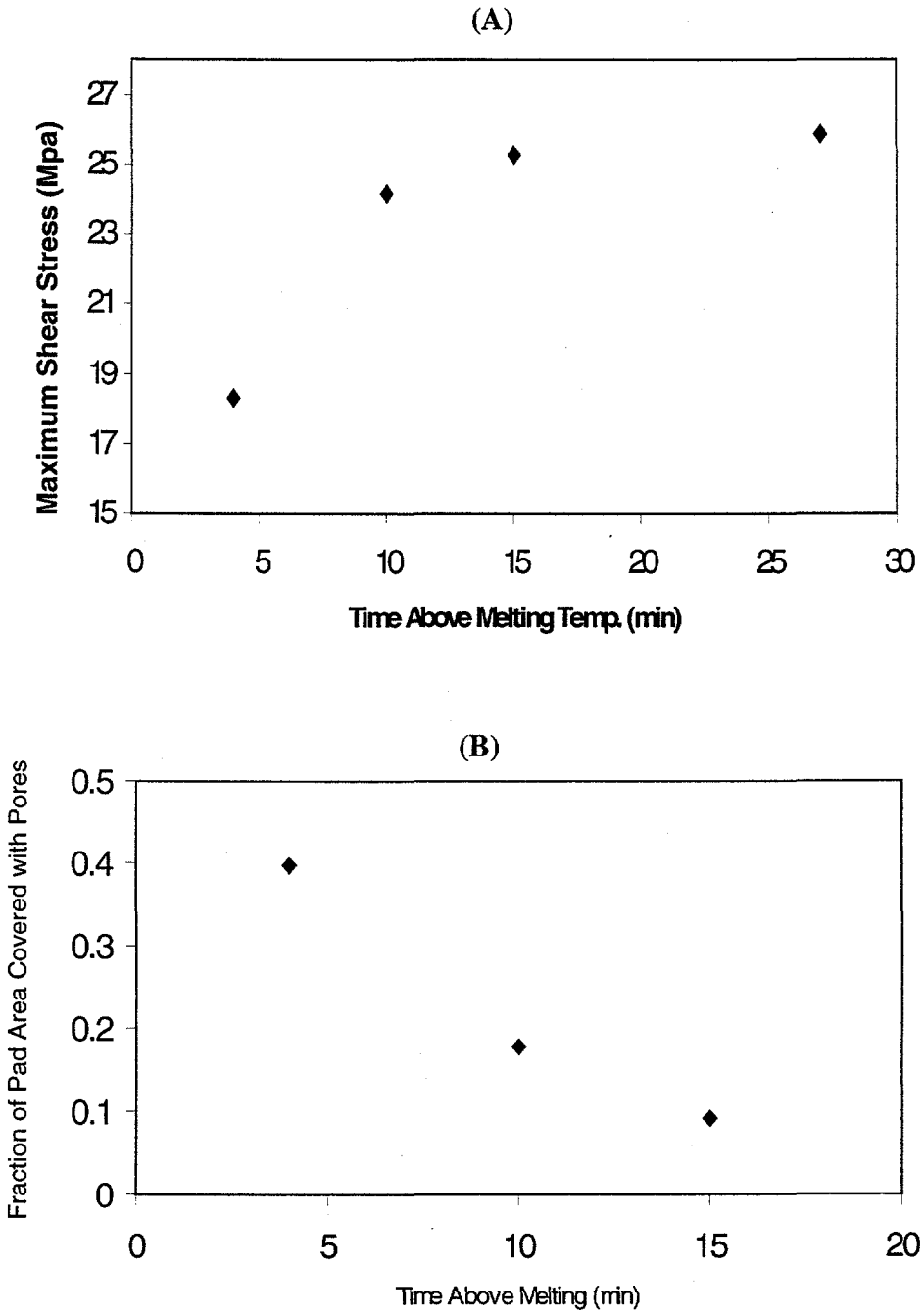


Figure 3.3-1. *Plots for samples assembled on hard-Au/Cu pads with flux. A) Maximum shear stress for samples held above melting temperature for different times. B) Fraction of the pad area covered by pores after being held for different amounts of time above melting temperature.*

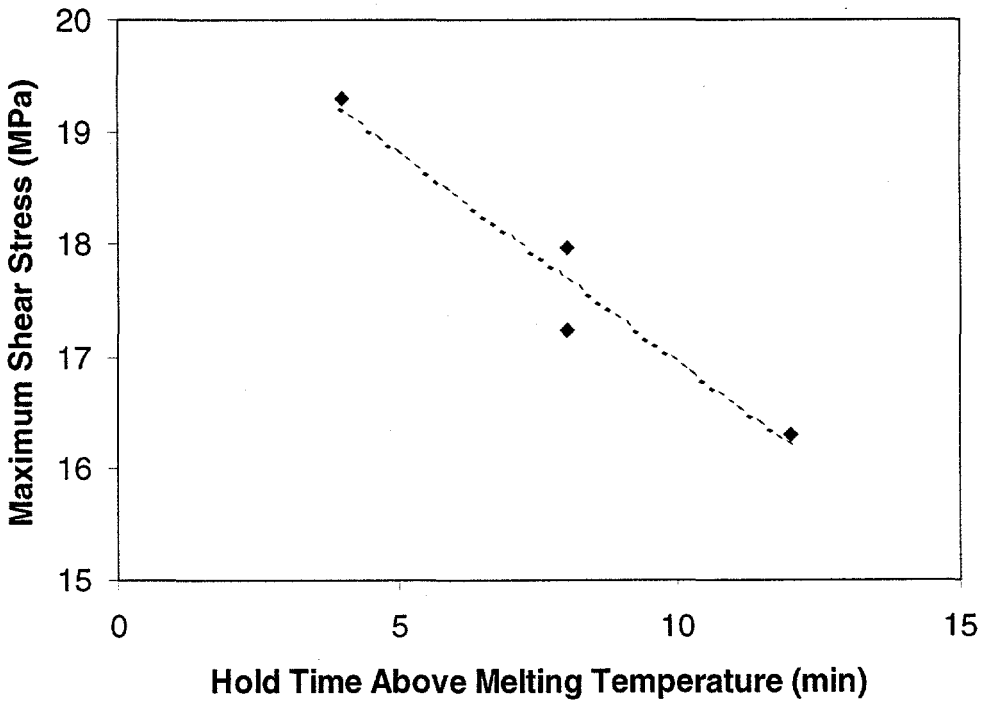
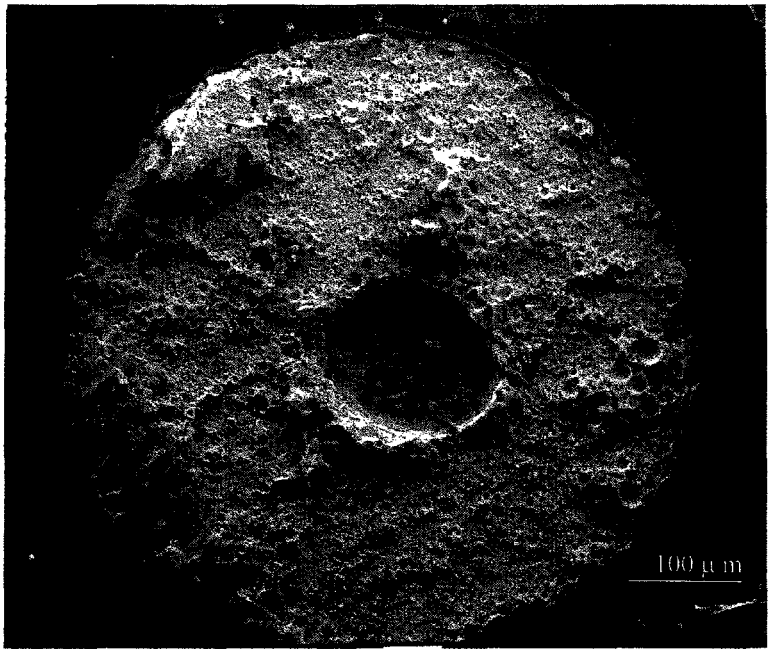
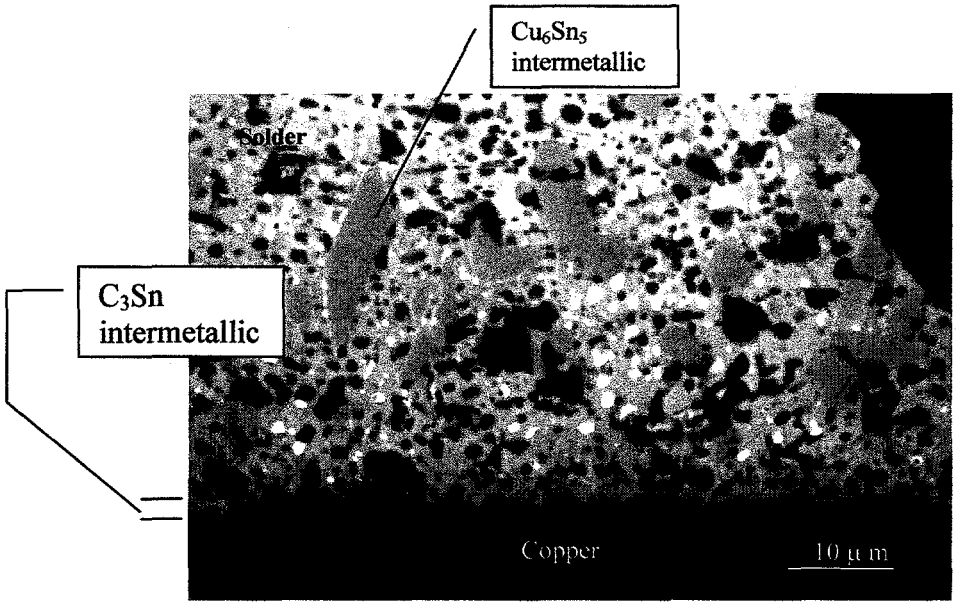


Figure 3.3-2. *Plot for samples reflowed on bare Cu pads using flux. The plot shows the maximum shear stress for each sample after being held above melting temperature for different times.*



(A)



(B)

Figure 3.3-3. *A) Secondary electron image from the fracture surface of a tested sample from set 5 (hard-Au metallization) heat-treated at 200 ℃ for 120 min. B) Backscattered image of its corresponding cross-section, showing the intermetallic layer as well as the intermetallic that detached from the interface.*

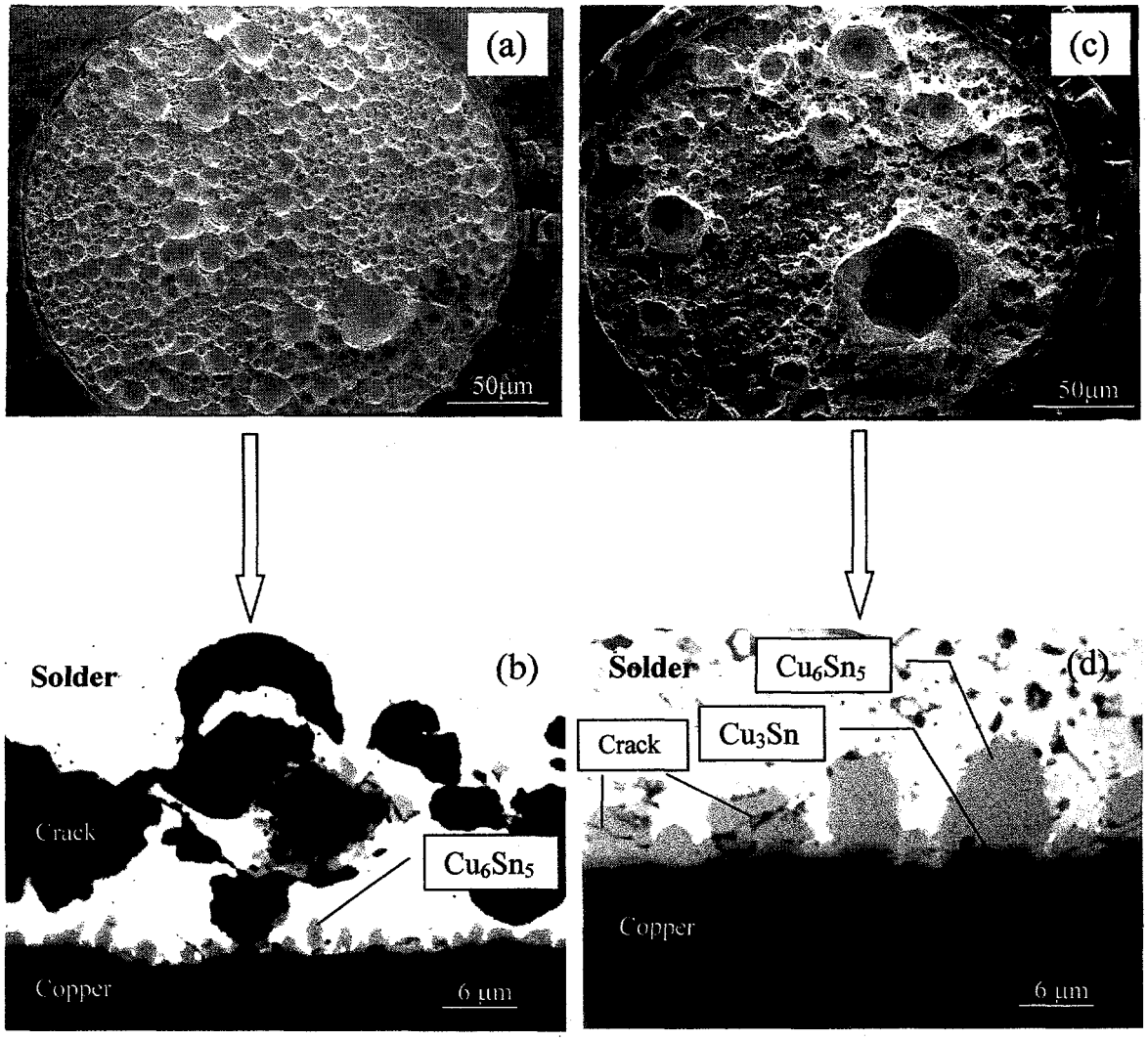
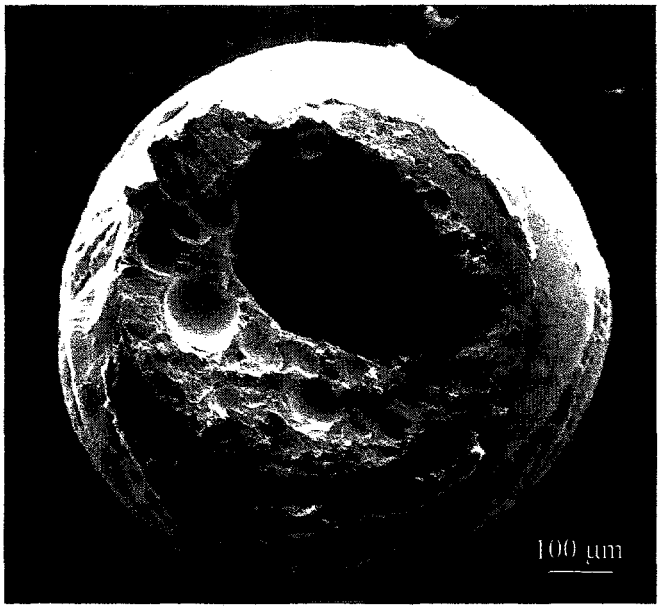
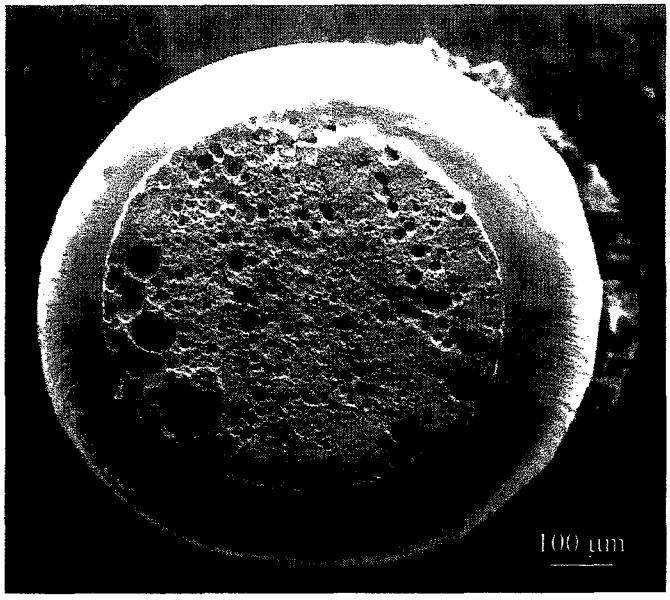


Figure 3.3-4. *a) Secondary electron image from the fracture surface of a tested bare-Cu sample after 1 reflow cycle, and b) the backscattered image of its corresponding cross-section. c) Secondary electron image from the fracture surface of a tested bare-Cu sample held above melting temperature for 120 min, and d) the backscattered image of its corresponding cross-section.*

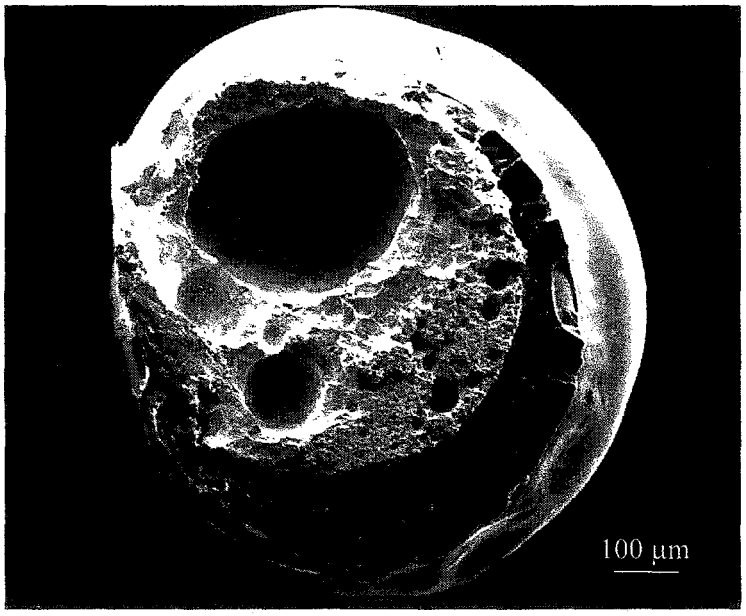


UPPER INTERFACE

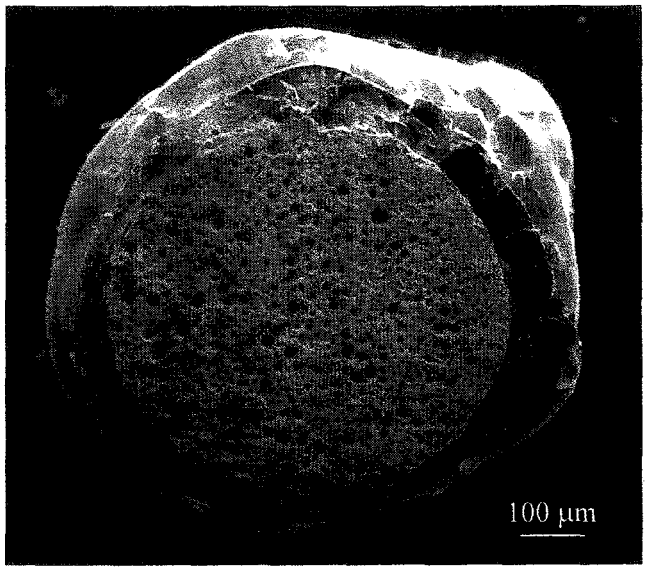


LOWER INTERFACE

Figure 3.3-5. *Fracture surfaces for BGA sample 1-Au (hard-Au/Cu pads using flux). This sample corresponds to the first data-point (4 min) in Figure 3.3-1.*

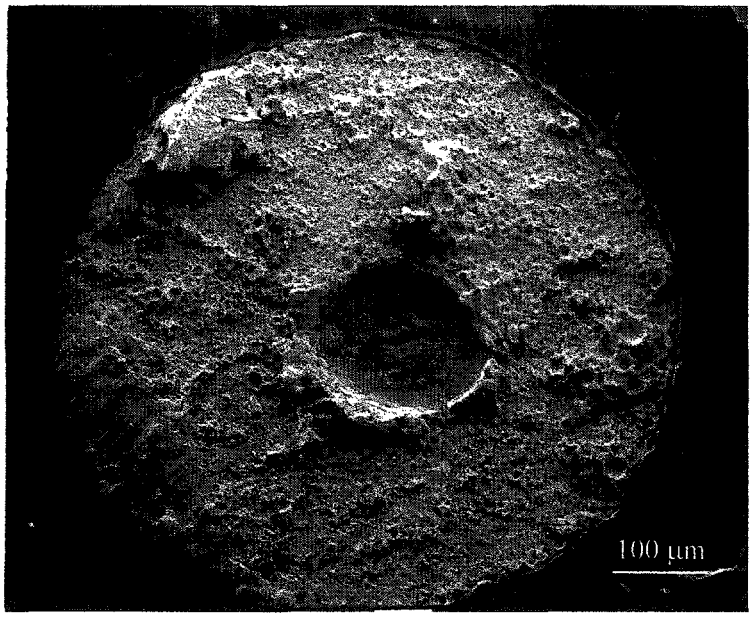


UPPER INTERFACE

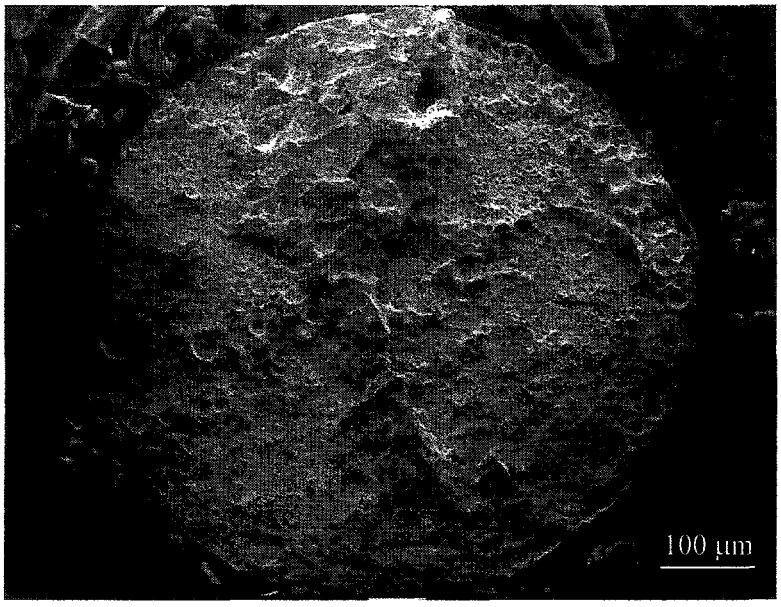


LOWER INTERFACE

Figure 3.3-6. *Fracture surfaces for BGA sample 2-Au (hard-Au/Cu pads using flux). This sample corresponds to the second data-point (10 min) in Figure 3.3-1.*



UPPER INTERFACE



LOWER INTERFACE

Figure 3.3-7. *Fracture surfaces for BGA sample 1-Au (hard-Au/Cu pads using flux). This sample corresponds to the sample heat treated at 200 °C for 120 min.*