CONCURRENT DESIGN OF AN RTP CHAMBER AND ADVANCED CONTROL SYSTEM

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ABSTRACT

A concurrent-engineering approach is applied to the development of an axisymmetric rapid-thermal-processing (RTP) reactor and its associated temperature controller. Using a detailed finite-element thermal model as a surrogate for actual hardware, we have developed and tested a multi-input multi-output (MIMO) controller. Closed-loop simulations are performed by linking the control algorithm with the finite-element code. Simulations show that good temperature uniformity is maintained on the wafer during both steady and transient conditions. A numerical study shows the effect of ramp rate, feedback gain, sensor placement, and wafer-emissivity patterns on system performance.

INTRODUCTION

Rapid thermal processing (RTP) is an emerging technology for some thermal manufacturing steps in integrated circuit fabrication process flows. The extent that existing methods (e.g., batch furnaces) will be displaced by single-wafer technology depends on the ability of RTP systems to accurately control wafer temperature during processing. The task of achieving uniform and repeatable temperature relies on design of the lamp housing and reaction chamber, the temperature control system, and the temperature sensors. For optimal performance, an integrated approach to equipment design, control-system design and sensor implementation is essential.

Temperature control of RTP systems is a topic that has received considerable study over the past several years. Control strategies incorporating internal nonlinear physically based models [1,2] along with approaches using empirically derived linear models [3] have been demonstrated as feasible methods for meeting the performance requirements for single wafer processing. A common element in each of these approaches is that the control design relies upon experimental data obtained from the reactor to be controlled. By waiting until the reactor fabrication has been completed to begin control system design, the burden of achieving acceptable closed-loop behavior is placed entirely on the controller. The system closed-loop behavior, however, is dependent on both the hardware design and the controller design.

It has been demonstrated that the design process for RTP control can proceed using detailed physically based models instead of hardware [4]. This eliminates the need for pre-existing hardware to begin controller development. By beginning the controller design while the reactor

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development is still in the conceptual stage, both control and hardware design parameters can be adjusted to optimize closed-loop performance.

We have developed a nonlinear physically based finite-element thermal model of CVC Products' (CVC) RTP chamber that can be linked with arbitrary process control algorithms. This model has been applied to the concurrent development and optimization of both the hardware design and the advanced control system design for the CVC RTP chamber. A preliminary temperature controller was developed using system response data generated with the model. Linking this controller with the finite-element RTP model has created a "virtual" environment to test the hardware design under closed-loop (feedback) control. This software capability has several advantages over the standard approach that requires hardware to be built prior to beginning the controller design. The product development time is reduced by allowing both the hardware design and the controller design to progress in parallel. In addition, performance of both the hardware and controller are evaluated simultaneously. Critical design features such as the lamp configuration, the wafer support, or placement of the sensors can be tested using closed-loop simulation thus allowing design iterations to occur on paper and not with actual hardware.

SYSTEM DESCRIPTION

The CVC RTP reactor is an axisymmetric design with five independently controlled lamp zones that heat the back side of a 200 mm wafer. Figure 1 shows a schematic representation of the reactor geometry. Each lamp zone contains an array of tungsten-halogen bulbs arranged in a circular pattern. Between each lamp zone is a radiation partition which limits "cross-talk" between the zones for improved control characteristics. The wafer rests face-up on a support that is attached to a rotation mechanism. Reactant gases are delivered through a multi-zone showerhead manifold from the top of the reactor. The face of the showerhead is polished for high reflectivity, creating a condition that approaches the behavior of a black-body cavity, and thereby reduces the sensitivity of the system to wafer front-side emissivity variations. A quartz window separates the lamp housing from the reaction chamber and the wafer. The chamber walls are water cooled. Deposition of reactants on the wafer back side and the window during processing is prevented by the wafer support ring. The reaction chamber is designed with a Modular Equipment Standards Committee (MESC) compatible interface.

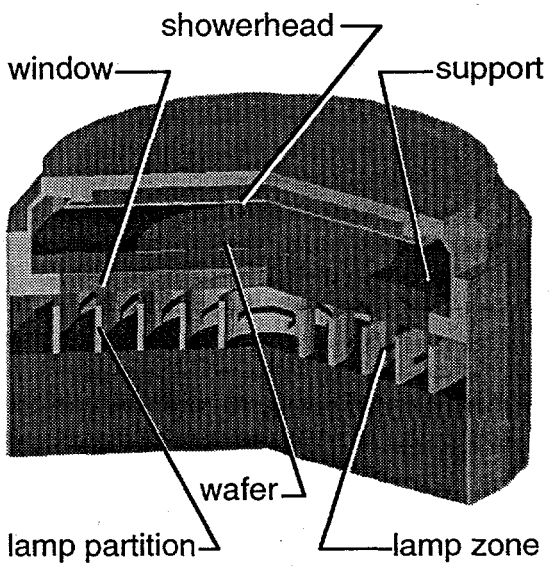

Figure 1. Model of a rapid-thermal-processing (RTP) reactor

THERMAL MODEL

We have developed a finite-element thermal model for design and evaluation of the CVC RTP system using the Sandia-developed TACO software [5]. Radiant heat exchange between enclosure surfaces is based on the net radiation method [6]. View factors for the enclosure radiation exchange are computed using the VIEWC software [7]. The thermal simulations for this RTP system have approximately 1000 elements and 400 radiation surfaces. The model includes the silicon wafer, lamps, semi-transparent window, chamber walls, and showerhead gas injector. Heat is removed from the model through convective boundary conditions that account for air cooling inside the lamp housing and for water cooling on the outer chamber walls. Heat input to

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the model is through volumetric heat generation (W/m^3) in the lamp zones. An annular ring approximation is used to represent the discrete lamps of each zone. The heat generation is controlled independently for each lamp zone. A more detailed description of the model and its application to the design of the CVC RTP reactor are discussed by Spence, et al. [8] and Kee, et al. [9].

CONTROLLER DESIGN

System Identification

The availability of a thermal model of the CVC RTP reactor provides us with the opportunity to begin controller design before the hardware has been fabricated. Using the model in place of the actual hardware, temperature responses at five discrete radial points on the wafer are predicted for a series of excitation signals to the control inputs (lamp zone powers) of the simulation. The temperature response points are chosen to correspond with the location of the pyrometers. Due to the nonlinear behavior of the system, it is important to characterize the system over the entire operating range (i.e., 500 °C to 1100 °C). Obtaining system response data at numerous operating temperatures through a series of open-loop simulations is a very time-consuming process. We are able to expedite the system identification process by performing the step-test simulations in two stages. First, one set of response data is obtained at a nominal operating temperature. Using these data, a simple (yet stable) controller is designed for the system. This controller is programmed to drive the simulation under closed-loop operation to a specified temperature then switch to an open-loop step test sequence. Following the open-loop test sequence, the controller switches back to closed-loop operation and takes the system to the next temperature where the open-loop step-test is repeated. With this controller driving the simulation, a complete system identification is done automatically. This controller is designed with an interface that allows the test sequence parameters (i.e., test temperatures, step size and duration, ramp rate between temperatures) to be easily varied. Figures 2a and 2b show the control inputs and the system response for an automated test sequence. The power excursions between each of the open-loop test sequences in Fig. 2a are a result of the closed-loop controller as it drives the simulation to the next test temperature.

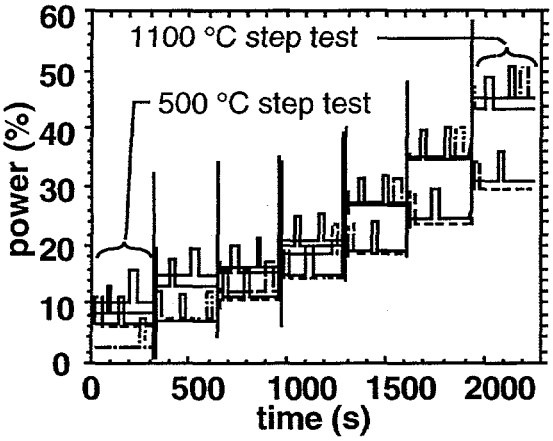

Figure 2a. Lamp powers for an automated system identification for temperatures from 500 °C to 1100 °C.

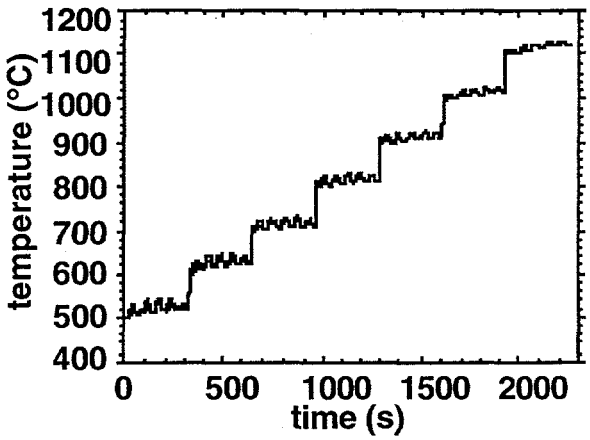

Figure 2b. Temperature response at wafer for excitation signal shown in Fig. 2a.

Linear Control Model

The response data we obtain from the finite-element simulations is used to develop a control model of the RTP system. Using the state-space approach, the process is represented by a system

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of first-order differential equations. The least squares method is used to derive a plant model of the form

$$\dot{x} = Ax + Bu \quad (1)$$
$$y = Cx + Du \quad (2)$$

where x is the state vector, u is the input (power) vector, and y is the measured output (temperature) vector. The control model is developed in two stages. First a high-order model (i.e., 20 - 60 states) is developed. Next, a reduced-order model is obtained by eliminating the unimportant modes thereby reducing the number of states in the high-order model. The reduced linear model for our system has 5 states. Figures 3a and 3b show how the linear models compare with the nonlinear finite-element model in predicting the wafer response to a step change in the power of the center lamp zone. The plots show that both the 5-state and the 38-state linear models are in good agreement with the finite-element model. Reducing the model from 38 states to 5 states generates a minimal decrease in accuracy.

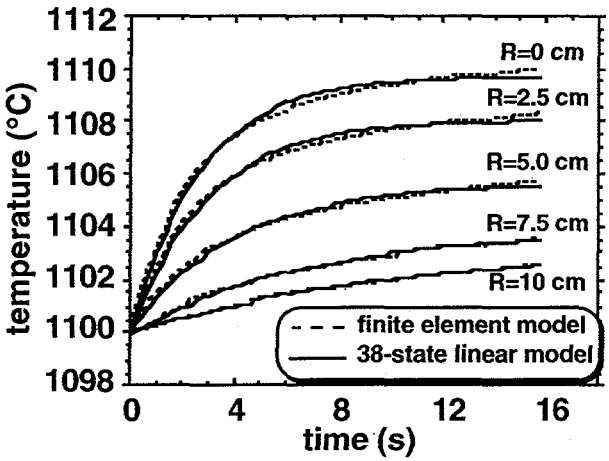

Figure 3a. Comparison of FE model and 38-state linear model in predicting response to a step change in power of the center lamp zone.

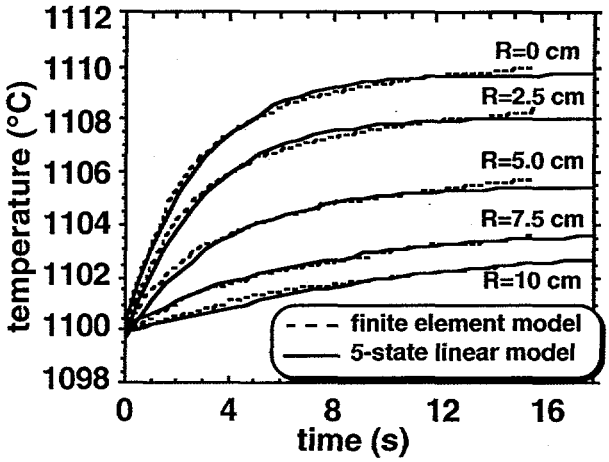

Figure 3b. Comparison of FE model and 5-state linear model in predicting response to a step change in power of the center lamp zone.

Design Process

We have designed a linear quadratic Gaussian (LQG) controller for the CVC RTP reactor. The LQG control strategy is well suited for RTP because of its applicability to multivariable and time-varying systems [10]. The control design process is separated into two parts: a linear-feedback controller (regulator), and a state estimator which gives estimates of the states from the observed outputs. The regulator is designed to drive the states of the system while maintaining them within specified limits. The design of the regulator requires an optimal gain matrix, K_r, to be computed that minimizes a specified cost function, V. The cost function is expressed as the integral [11]

$$V = \int_0^\infty \left[x^T(\tau)Q(\tau)x(\tau) + u^T(\tau)R(\tau)u(\tau) \right] d\tau \quad (3)$$

where Q and R are symmetric weighting matrices. The goal in designing the regulator is to minimize system response to noise or disturbances while avoiding saturation of the control signals. This balance is achieved through a somewhat trial-and-error process of selecting the weighting matrices (Q and R) that give the desired performance.

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Since the regulator requires that all states of the system be available, an estimator (i.e., Kalman filter) is also required. The goal is to find an estimate of the state vector which minimizes the error between the actual state vector $\boldsymbol{x}$ and the estimated state vector $\hat{\boldsymbol{x}}$. An optimal state-estimator gain matrix is calculated for the dynamic system. This gain matrix is derived by minimizing the expected mean square of the error between the measured output, $\boldsymbol{y}$, and the output from the estimator, $\hat{\boldsymbol{y}}$. The estimator model accounts for the fact that there may be some process noise within the system model itself as well as some noise inherent in the device used to measure the outputs. The resulting state equation for the estimator is [12]

$$\dot{\hat{\boldsymbol{x}}} = (\boldsymbol{A} - \boldsymbol{K}_e\boldsymbol{C})\hat{\boldsymbol{x}} + \boldsymbol{B}\boldsymbol{u} + \boldsymbol{K}_e\boldsymbol{y} \tag{4}$$

where $\boldsymbol{K}_e$ is the optimal state-estimator gain matrix. Combining the equations for the plant, the regulator, and the estimator results in the following equation for the LQG controller [12]:

$$\dot{\hat{\boldsymbol{x}}} = (\boldsymbol{A} - \boldsymbol{K}_e\boldsymbol{C})\hat{\boldsymbol{x}} + (\boldsymbol{K}_e\boldsymbol{D} - \boldsymbol{B})\boldsymbol{u} + \boldsymbol{K}_e\boldsymbol{y} \tag{5}$$

where

$$\boldsymbol{u} = -\boldsymbol{K}_r\hat{\boldsymbol{x}}. \tag{6}$$

Figure 4 shows a schematic of the process we use for controller design. The optimization loops represent the iterative process used to adjust the control design parameters (i.e., weighting matrices). At the first level, the control parameters are optimized using the high-order linear model to represent the plant. Next, the controller is linked with the finite-element model. At this level, both the control parameters and the hardware design can be modified to optimize closed-loop performance. The final step is to optimize the controller on the actual plant (i.e., the RTP reactor).

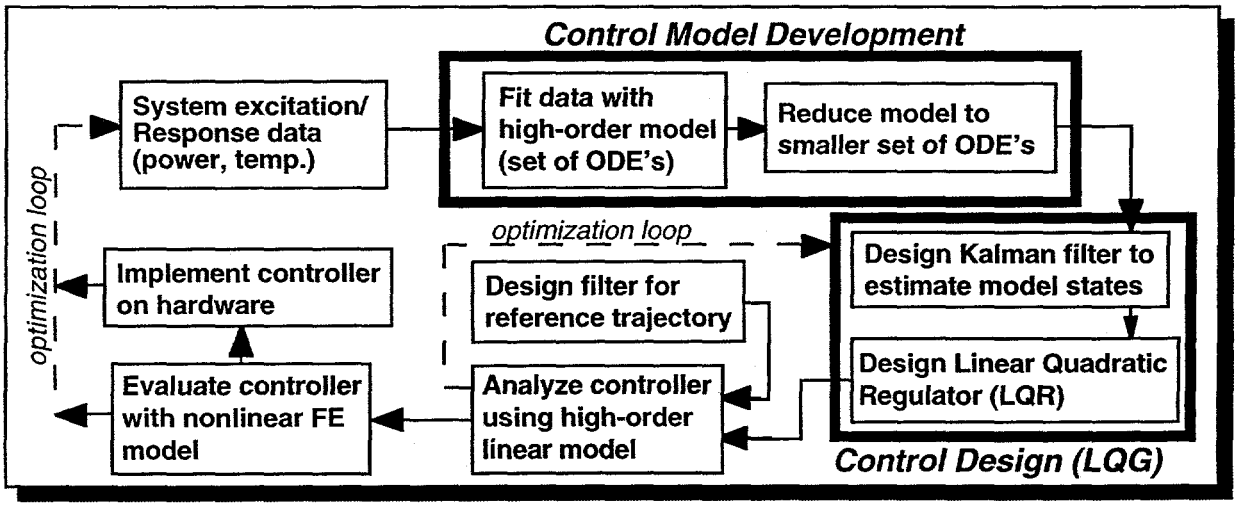

Figure 4. Schematic of the control design process utilizing a finite-element model for response data and closed-loop evaluation.

LINKING MODEL AND CONTROL

We have developed two methods to run large-scale simulations under closed-loop feedback control. The first method is to write the control algorithm as a subroutine, which is called from the physical simulation software. A convenient feature available within some control development software (e.g., MATRIXx, MATLAB) is the capability to automatically generate source code for the control design. The second communication method allows both the finite-element code and the

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control-development code to run as independent processes using UNIX system calls (sockets) to pass data between them. This approach requires communication I/O filters to be written for each code. The advantage of this approach is that the independent processes can run on different computing platforms (e.g., a CRAY and a SUN workstation) and the full power of the controller-development software is available for interactive modifications and evaluation.

Most real-time process-control algorithms run according to a clock that samples the sensors and updates actuator commands at a certain frequency. For an RTP system, a 5 to 20 Hz clock is typical. Linking the physical simulation to the controller thus requires that the simulation can be interrupted at this frequency, provide sensor information (e.g., wafer temperature), and accept new settings for the actuators (e.g., lamp powers). Accommodations for this procedure must be made to the numerical time-stepping and error-control algorithms of the finite-element software.

RESULTS

The LQG controller is linked with the finite-element model to evaluate the behavior of the closed-loop system. Running controlled simulations allows concurrent evaluation of both the controller design and the hardware design. We have used the closed-loop model to simulate a ramp from 800 °C to 1100 °C. Figure 5a shows the temperature history of the five "sensor" points on the wafer during a controlled simulation. The model does not include actual sensors; rather, specific points on the wafer that would be monitored by sensors in the actual hardware are designated as the sensor points for the simulations. The sensor points are located at the wafer center, the wafer edge, and three equally distributed intermediate wafer points (R=2.5 cm, R=5.0 cm, and R=7.5 cm). Note that the five temperatures track so closely that they cannot be distinguished from each other in Fig. 5a. The reference temperature trajectory specified for the simulation calls for a smooth curve at the start and finish of the ramp to minimize the temperature tracking errors and the power spikes that will occur for trajectories with a discontinuity in the slope. Figure 5b shows the power history for each of the five lamp zones corresponding to the ramp shown in Fig. 5a.

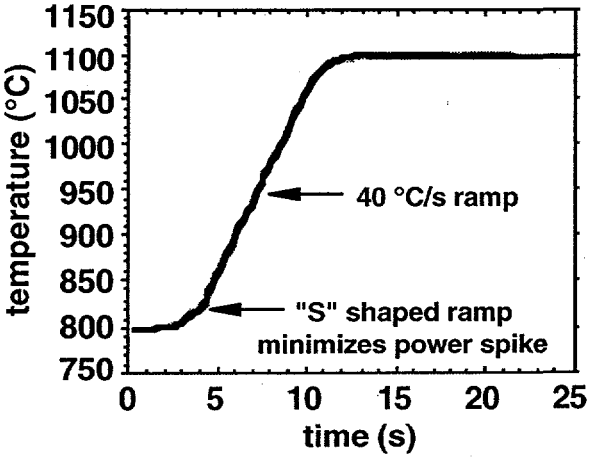

Figure 5a. Wafer temperature history during controlled simulation.

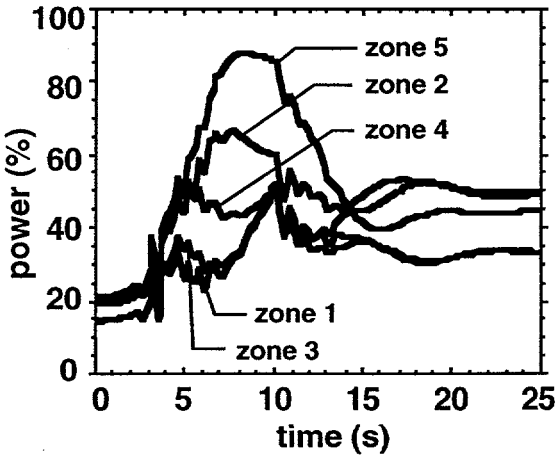

Figure 5b. Lamp zone powers during controlled simulation.

Wafer temperature uniformity is an important criterion for performance evaluation. Temperature gradients during high ramp rates can lead to stress fracture (slipping) of the wafer while temperature non-uniformity during steady conditions leads to non-uniformity of the process (e.g., chemical vapor deposition, oxide growth, or diffusion). Figure 5c shows the wafer temperature difference predicted for the trajectory shown in Fig. 5a. The dashed curve shows the maximum temperature difference as indicated by the five sensor points. A significant advantage of using a

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simulation for controller evaluation is that the model is not limited to information from the sensors. Temperature data is available over the entire wafer. The solid curve in Fig. 5c shows the maximum temperature difference across the entire wafer with a peak value of 6 °C which is almost twice that indicated by the sensors. The radial temperature profile corresponding to the time at which the maximum temperature difference occurs (time = 6 s) is shown in Fig. 5d. A slight overlap between the wafer and the support ring creates an annular region at the wafer edge with a slightly higher mass than the rest of the wafer. During high ramp rates, this high-mass region lags behind the rest of the wafer resulting in the temperature dip seen at the wafer edge in Fig. 5d.

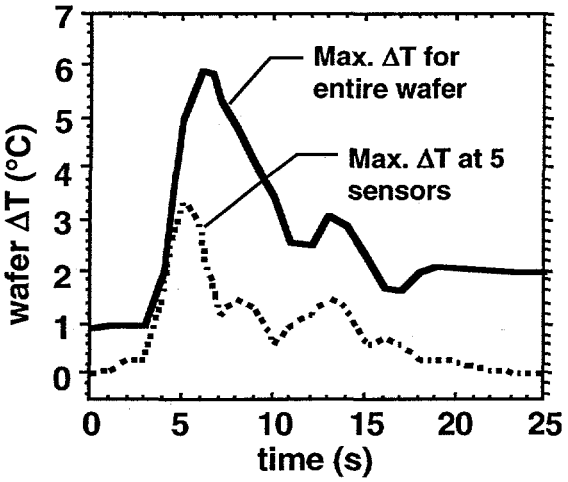

Figure 5c. Maximum temperature variation (ΔT) across the wafer during a controlled 40 °C/s ramp.

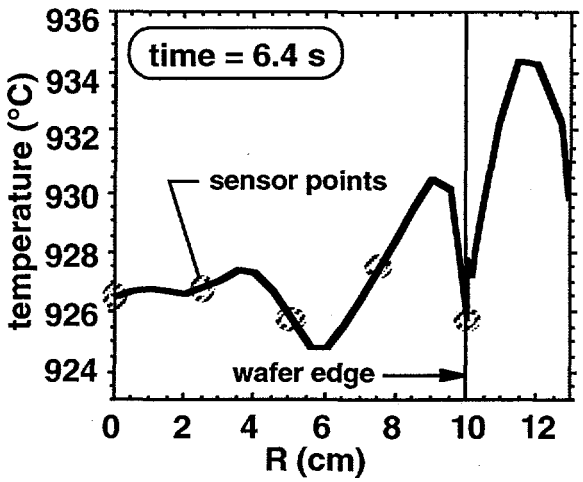

Figure 5d. Radial temperature profile on wafer at time of peak ΔT during controlled ramp.

Sensor Location

The optimal sensor locations depend on reactor design, control strategy, and process objectives. We investigate the effect of shifting the position of the outer sensor. Determining the best position requires consideration of the transient temperature uniformity requirements and the size of the exclusion region (i.e., annular area at the wafer edge containing no die) .

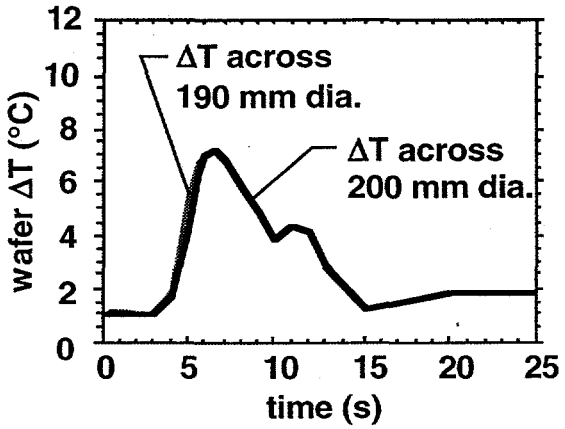

Figure 6a. Outer sensor at R=100 mm. Tight control on wafer edge increases variation at inner regions of the wafer.

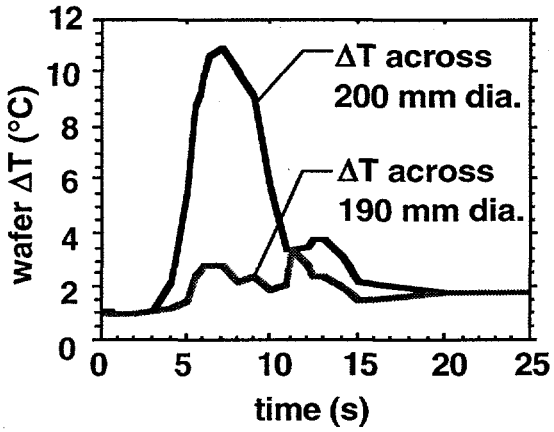

Figure 6b. Outer sensor at R=95 mm. Removing wafer edge from the active control zone significantly reduces ΔT across 190 mm of a 200 mm wafer.

The primary difficulty in maintaining wafer temperature uniformity during the high ramp rates is the wafer edge effect. If we design the controller to minimize temperature variation over a region that excludes the very edge of the wafer, then temperature uniformity over the inner portion of the wafer is significantly improved. Figure 6a shows the wafer-temperature variation for a simulation in which the temperature is controlled to the wafer edge (outer sensor at R = 100 mm). Figure 6b shows the wafer-temperature variation for a simulation in which the outer 5 mm of the wafer is excluded from the controlled zone (outer sensor at R = 95 mm). A comparison of Figs. 6a and 6b shows that by moving the outer sensor in from the wafer edge we degrade the overall uniformity, however, uniformity over the majority of the wafer (190 mm diameter) is improved. This effect is illustrated in Fig. 6c which shows the wafer temperature profiles during the time of worst case temperature non-uniformity during the ramp. From this analysis we can conclude two important points: (1) Design of the interface between the wafer and wafer-support ring should minimize variations in thermal mass, and (2) the position of the temperature sensors for optimal uniformity depend on the accepted exclusion region for the wafer edge.

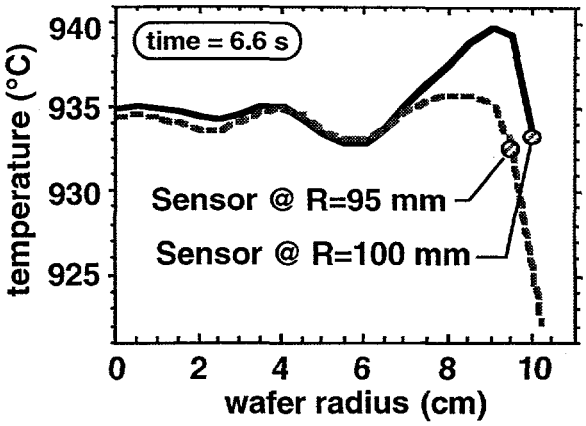

Figure 6c. Location of outer sensor has a large effect on radial temperature profile during high ramp rates (50 °C/s shown).

Ramp Rate Effects

The push for high ramp rates is generated by the need to reduce cycle time and thermal budget. We investigate the effect of increased ramp rates on temperature uniformity and cycle time. Increasing the ramp rate will reduce the transient time between setpoint temperatures, however, temperature variation on the wafer will increase resulting in longer stabilization times. The effect that ramp rate will have on the overall cycle time depends on reactor design and control strategy.

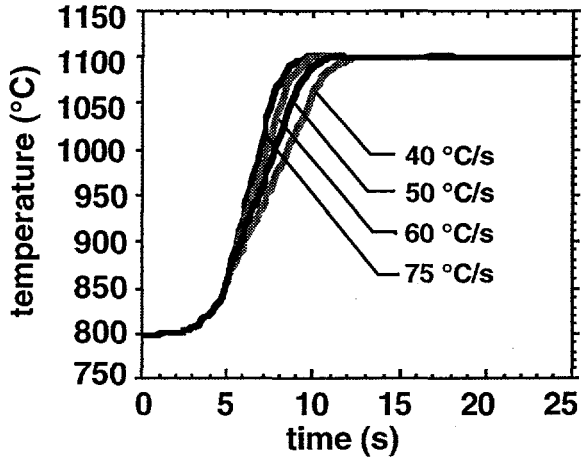

Figure 7a. Wafer temperature during controlled simulations with ramp rates of 40, 50, 60, and 75 °C/s.

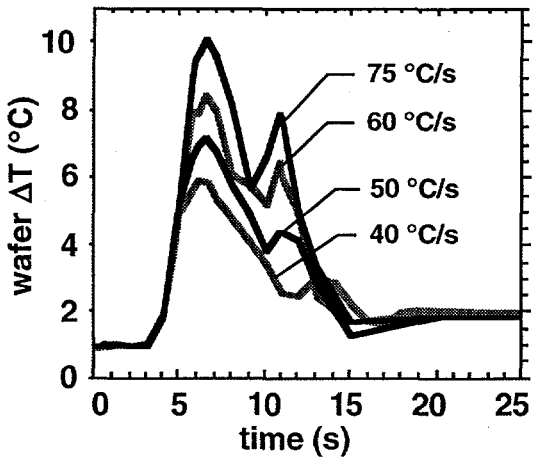

Figure 7b. Maximum temperature variation across the wafer during controlled simulations at ramp rates of 40, 50, 60, and 75 °C/s.

We have repeated the controlled ramp at a number of different rates. Figure 7a shows the wafer-temperature history of four ramps between 40 °C/s and 75 °C/s. The wafer-temperature variation

(over the entire 200 mm diameter) for each ramp is shown in Fig. 7b. The challenge of maintaining temperature uniformity on the wafer becomes greater as the ramp rate is increased. Both reactor design and controller design play a role in the realizable temperature uniformity. As the ramp rate increases, the power resources required to drive the states within the desired tolerance also must increase. Also, the higher ramp rates may require a longer stabilization time which will reduce the impact on cycle time reduction. If we impose the restriction that processing can begin only after the wafer temperature variation has decreased below 3 °C, Fig. 7b shows that the higher ramp rates provide little improvement in cycle time.

Feedback Gain

Weighting parameters in the controller define the balance between setpoint tracking and the range of power control. We have included a simple tuning parameter *(α)* in our controller to adjust the feedback controller gain. In this case, $Q = \alpha\overline{Q}$ where $\overline{Q}$ is a weighting matrix. (We note that a more appropriate procedure to improve performance involves tuning the entire Q and R matrices.) As the value of α is increased, the control action for a given tracking error $\left(\left|T_{reference} - T_{measured}\right|\right)$ is increased. Figure 8a shows the temperature variation on the wafer during a 50 °C/s ramp followed by a stabilization at 1100 °C. This simulation was run with tuning parameters of $\alpha=1$ and $\alpha=3$. Note that as we increase α from 1 to 3, the peak temperature variation on the wafer is reduced from 10 °C to 7 °C. The cost of the improvement in temperature uniformity is an increase in required power resources. Figure 8b, shows that we actually saturate power in lamp zone 5 (the outer zone) for the simulation with α equal to 3. With α equal to 1, we have no problem with power saturation, however, the controller now tolerates greater tracking errors resulting in a more sluggish response.

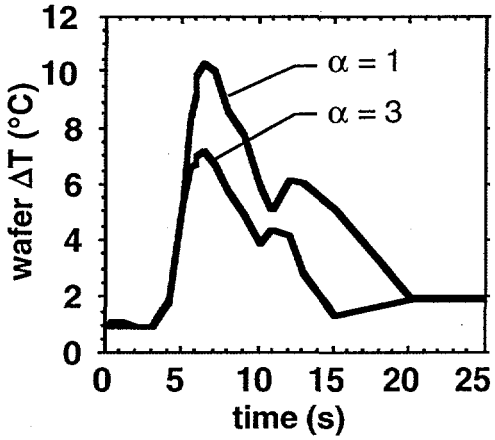

Figure 8a. Maximum temperature variation across wafer during a 50 °C/s ramp for two values of the control parameter α.

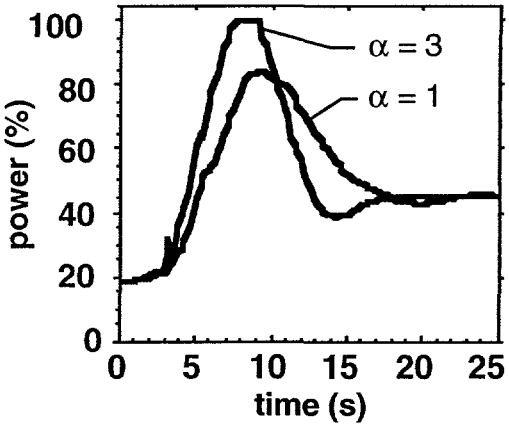

Figure 8b. Power history for the outer lamp zone during a 50 °C/s ramp for two values of the control parameter α.

Wafer Patterning Effects

It has been demonstrated that patterned layers can generate temperature variations on wafers in cold-wall RTP systems [13]. The magnitude of the pattern-induced temperature variations is a function of the length-scale of the pattern, the differences in optical properties (i.e., emissivity) within the patterned region, and the design of the reactor. The CVC reactor is designed to minimize the effect of wafer emissivity variations. Lamp heating is provided to the wafer back-side which is less susceptible to emissivity variations. In addition, the wafer front-side faces a

highly reflective chamber designed to approximate a blackbody cavity thus reducing sensitivity of wafer temperature to emissivity. In spite of these design precautions, large emissivity variations on the wafer can create significant temperature non-uniformity if the pattern size is sufficiently large (> 5 mm).

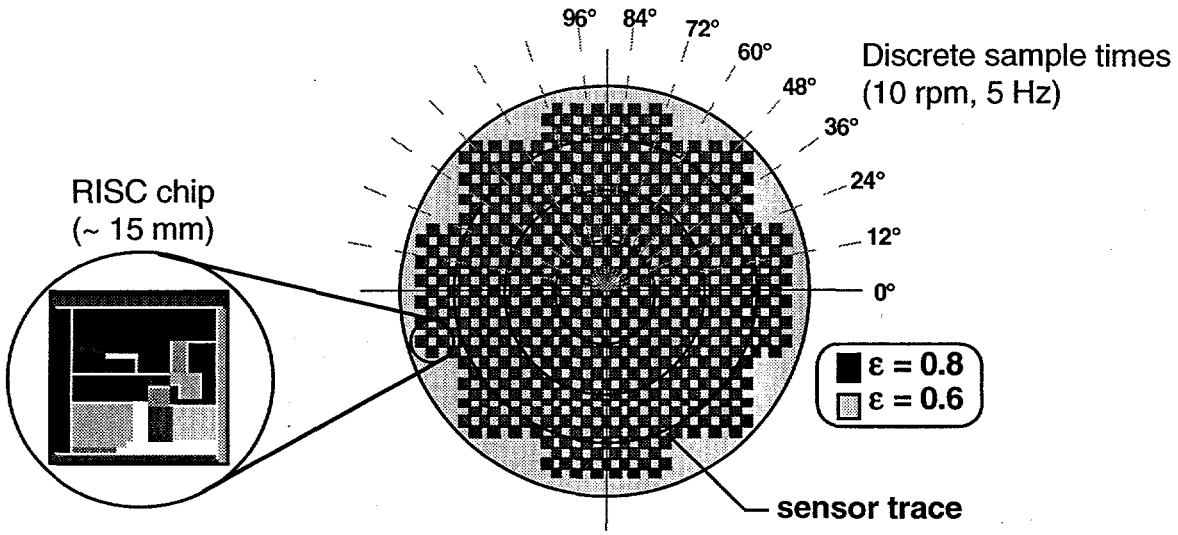

Figure 9. Complex emissivity variations on the wafer are approximated with a uniform checkerboard pattern in controlled simulations for evaluating temperature uniformity and control.

To evaluate the performance of our closed-loop system under less-than-ideal conditions, we repeated the ramp simulations using patterned wafers. Figure 9 shows a wafer with a checkerboard pattern used to approximate the complex emissivity patterns that may be encountered on a wafer with logic circuits. Both 5 mm and 10 mm patterns were simulated with emissivity varying between 0.6 and 0.8. Figure 10 shows wafer temperature profiles during the steady portion of a controlled simulation. The temperature profiles were predicted using a non-rotating wafer assuming three different emissivity patterns. We see that the temperature non-uniformity increases with the pattern length scale. The case with uniform emissivity (no pattern) shows the temperature uniformity limit that will be approached as the pattern length scale decreases.

Steady temperature waves are generated on the non-rotating wafer that are a function of patterning and reactor design. An additional complexity occurs in the case when the wafer is rotated. The pyrometers are located in fixed locations and temperatures are sampled at discrete times. As the wafer rotates with respect to the pyrometers, temperatures are measured at different points on the wafer. It is assumed in our simulations that the wafer rotates at a rate of 10 rpm and the controller samples temperature at a rate of 5 Hz. This results in a temperature measurement every 12 degrees of rotation. It is also assumed that the pyrometer spot size is small compared to the pattern size. Because the pattern-induced temperature changes with respect to azimuthal position, the temperature measured by each sensor varies in time as the wafer

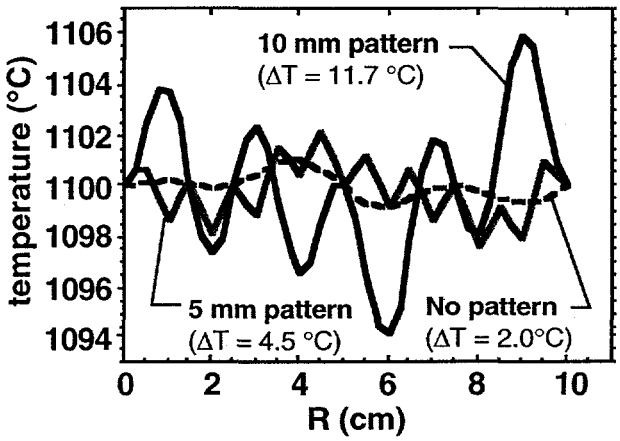

Figure 10. Controlled wafer temperature profiles for 3 emissivity patterns: uniform (ε=0.8), 5 mm pattern (ε_1=0.8, ε_2=0.6), and 10 mm pattern (ε_1=0.8, ε_2=0.6).

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rotates. Under closed-loop operation, the controller generates lamp power signals that attempt to compensate for the oscillating sensor measurements. The result is an oscillation in the lamp powers that in turn create an oscillation in temperature at each point on the wafer. Figure 11a shows the power history for one lamp zone during a controlled simulation of a rotating wafer. The oscillating signal is generated from temperature measurements on a wafer with a 10 mm checkerboard emissivity pattern. The resulting temperature oscillation at one point on the wafer during the simulation is shown in Fig. 11b.

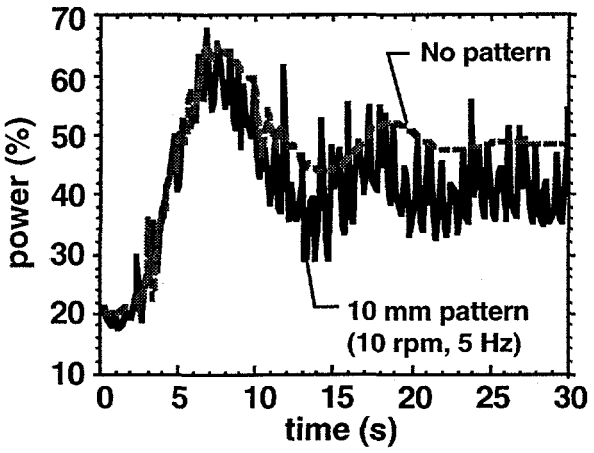

Figure 11a. Lamp power history (zone 2) during controlled simulations with a rotating wafer.

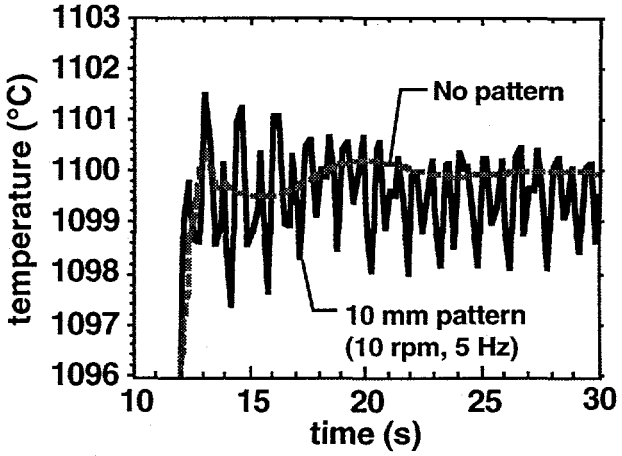

Figure 11b. Wafer temperature history during controlled simulations with a rotating wafer. (Temperature at R=2.5 cm).

The numerical simulations we have done are intended as a demonstration. A 10 mm pattern size is quite extreme and would probably not be seen in typical processes. The controller used for these simulations was designed using data obtained from simulations with non-patterned wafers, nonetheless it remained stable and performed as intended. If wafer patterning effects are anticipated, appropriate controller design steps (such as adding a notch filter) can be taken to minimize any undesirable response. The advantage of the closed-loop simulation is that it allows us to quantify the response of potential disturbances. The model results can then be used to guide design changes to improve the closed-loop system performance.

CONCLUSION

We have developed a thermal model to guide the design of the CVC RTP reactor. Using system response data obtained from the model, we have designed a MIMO controller for the five-zone reactor. Both the controller design and the reactor design were evaluated concurrently by linking the control algorithm with the finite-element thermal model. Closed-loop simulations of a thermal ramp from 800 °C to 1100 °C were performed with wafer temperature uniformity being used as a performance metric. System performance was evaluated under numerous conditions. Temperature uniformity was found to degrade with increasing ramp rate. Design of the interface between the wafer edge and the wafer-support ring was found to strongly influence temperature uniformity during high ramp rates.

The effect of control strategy decisions on system performance was demonstrated through adjustments to the feedback gain and sensor placement. Decreasing the feedback gain can lead towards sluggish response resulting in unacceptable temperature uniformity and tracking errors. Increasing the gain can create power demands that exceed the range of actuation resulting in power saturation and loss of control. The control requirements defined for the wafer edge greatly impact the control strategy and the resulting performance. If tight uniformity requirements are imposed over the entire wafer, then temperature must be monitored at the wafer edge. Controlling temperature at the wafer edge during high ramp rates requires large power reserves in the outer

lamp zone. By relaxing the tolerable error on the outer few millimeters of the wafer radius, we can shift the outside sensor in from the wafer edge and actively control a slightly smaller diameter region. This leads to a significant improvement in temperature uniformity across the reduced diameter during fast ramp transients in addition to reducing the power demand.

Power and temperature oscillations generated in a closed-loop simulation of a rotating wafer with patterned emissivity demonstrated the effect of a disturbance on our system. By anticipating potential disturbances, design modifications can be made to the reactor and/or controller to minimize undesirable system response. Using closed-loop simulations to thoroughly evaluate design concepts will lead to a robust system with superior process performance.

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