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Microfabrication of membrane-based devices by HARSE and combined HARSE/wet etching

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ABSTRACT

Deep-reactive ion etching (DRIE) of silicon, also known as high-aspect-ratio silicon etching (HARSE), is distinguished by fast etch rates ($\sim 3 \mu\text{m/min}$), crystal orientation independence, anisotropy, vertical sidewall profiles and CMOS compatibility. By using through-wafer HARSE and stopping on a dielectric film placed on the opposite side of the wafer, freestanding dielectric membranes were produced. Dielectric membrane-based sensors and actuators fabricated in this way include microhotplates, flow sensors, valves and magnetically-actuated flexural plate wave (FPW) devices. Unfortunately, low-stress silicon nitride, a common membrane material, has an appreciable DRI etch rate. To overcome this problem HARSE can be followed by a brief wet chemical etch. This approach has been demonstrated using KOH or HF/Nitric/Acetic etchants, both of which have significantly smaller etch rates on silicon nitride than does DRIE. Composite membranes consisting of silicon dioxide and silicon nitride layers are also under evaluation due to the higher DRIE selectivity to silicon dioxide.

Keywords: HARSE, DRIE, combined HARSE/wet etching, microhotplate, FPW, valve, flow sensor, composite membrane.

1. INTRODUCTION

Microfabricated membranes serve numerous applications in sensing and actuation. Resistive heaters fabricated on thin dielectric membranes, known as microhotplates, benefit from the low heat capacity and thermal conductivity of the membrane (1) and have been used for sub-atmosphere pressure sensing (2 - 4), flow sensing (5, 6), calorimetric (7) and conductometric (8) gas sensing and uncooled IR sensing (9, 10). Membranes are also remarkably robust and have been used in pressure sensing (11) and in micromachined valves and pumps (12).

Usually, membrane-based devices are fabricated by front or reverse side wet chemical etching, a process characterized by relatively slow etch rates, crystallographic dependence, consumption of precious wafer area and potential CMOS incompatibility. Membranes produced by surface micromachining do not suffer the limitations just mentioned, but have small underlying air gaps, usually no greater than $2 \mu\text{m}$, which can be restrictive for certain applications. For example, significant heat transfer by air conduction occurs between surface-micromachined membrane heaters and the underlying substrate, limiting their thermal efficiency (13).

We have used through-wafer HARSE to fabricate silicon nitride membrane-based devices such as microhotplates, flow and temperature sensors, valves and magnetically-actuated FPWs (14). This technique overcomes the aforementioned limitations associated with wet etching and surface-micromachining of membranes. Fabrication steps, as well as characteristics and limitations of this method are described. The performance characteristics of a HARSE microhotplate are given. Combined etching in which HARSE is followed by a brief wet-chemical etch is also described. This approach can be used to

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surmount difficulties arising from the relatively low etch selectivity of DRIE to silicon nitride over silicon. Finally, preliminary results of HARSE released, composite silicon dioxide/silicon nitride membranes are presented.

2. BASIC FABRICATION

The basic process flow for fabricating dielectric membrane devices by HARSE is illustrated in Figure 1. Processing begins with a silicon substrate coated with a suitable membrane material (Figure 1a). Low-stress, LPCVD silicon nitride was initially chosen for its good mechanical properties, chemical inertness and low thermal conductivity.

For FPWs and microhotplates, metals lines are next defined on top of the membrane material (Figure 1b). To relieve residual stress in the metal and stabilize its electrical characteristics, annealing should be performed at this point. For Ti/Pt heaters, for example, 500 °C in a N₂ ambient for 30 min is sufficient. After annealing, photoresist should be deposited over the metal to protect it during subsequent processing.

In step (c) the membrane etch mask is patterned in photoresist on the reverse side of the wafer. Aligning to front-side features such as metal heater lines is achieved with a back-side aligner such as the Karl Suss MA-6. Given that the DRIE etch rate on silicon is roughly 50 times that of photoresist, standard thick resists like AZ4903 easily provide adequate masking for etch depths up to 500 μm. After dry etching the silicon nitride to expose the underlying silicon, the silicon is etched via HARSE using the Bosch process (15). In this technique, alternating steps of aggressive etching and polymer deposition are used to maintain nearly vertical sidewall profiles during the etch. Etching is halted once the membrane material is reached. The photoresist mask is removed at this point with acetone.

Microhotplates produced in this way are shown in Figures 2 and 3. In Figure 3 a packaged die containing three DRI etched microhotplates is shown. At the left and right hand sides of the die are two small microhotplates 0.5 mm on a side; in the center is a large microhotplate, 2.75 mm on a side. These three microhotplates may be used in conjunction for three-wire, hot anemometry. If all three heaters/thermometers had been placed on only one membrane, thermal cross talk by conduction between the three devices would limit flow sensitivity. However, by placing the three devices on their own membranes, cross talk is reduced. It should be observed that HARSE has permitted the close spacing of the membranes. Such proximity is not possible via wet etching of {100} silicon with wet anisotropic etches like KOH due to the shallow angle (54.74°) formed between the exposed {111} planes and the wafer surface.

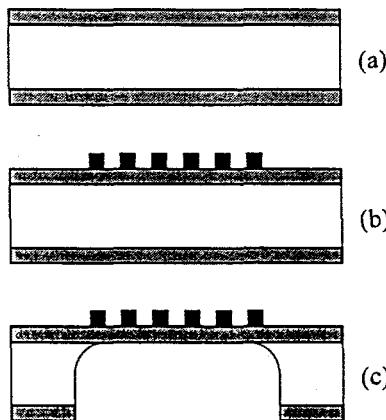


Figure 1: HARSE processing sequence for dielectric membrane devices. Starting substrates consist of a silicon wafer coated with a thin film that eventually becomes the membrane (a). For devices such as microhotplates, metal lines are deposited and annealed (b). The membrane etch mask is patterned on the reverse side of the wafer in thick photoresist. If the membrane material was deposited on both sides of the wafer, it is now etched using the photoresist mask. Finally, the silicon is etched by HARSE; again, the photoresist serves as the etch mask. HARSE is halted once membrane is reached.

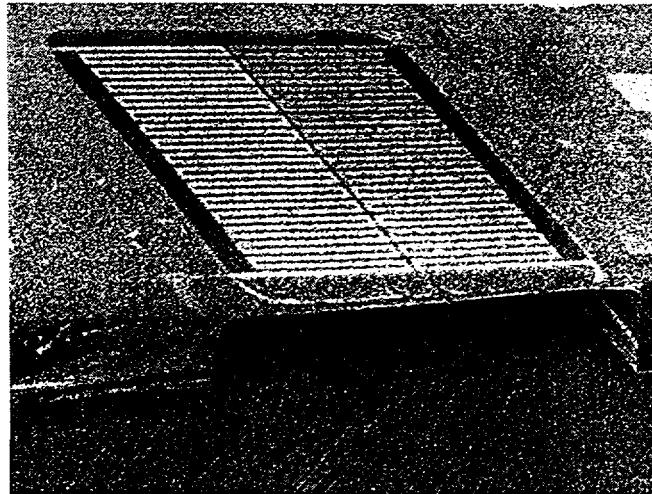


Figure 2: SEM cross section of a HARSE silicon-nitride-membrane microhotplate with a Pt heater. The wafer was diced about 25 μm away from the membrane, which is 2.75 mm on a side. Through-wafer etching is evident, as is the silicon "foot".

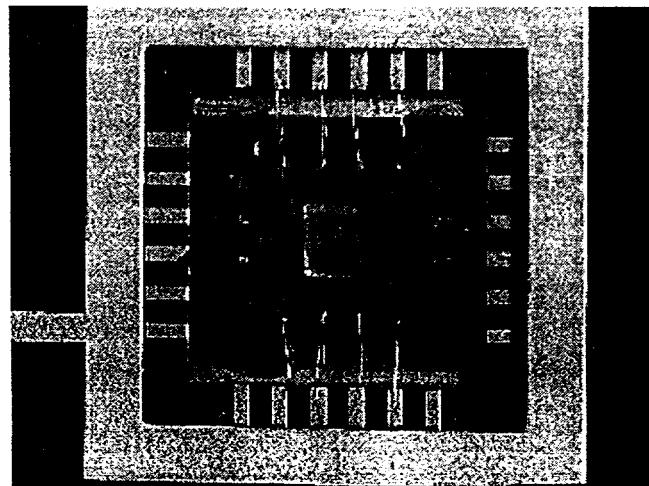


Figure 3: Photograph of a 24-PIN DIP packaged die with HARSE etched components. In the center, a Pt heater is placed on a dielectric membrane; the DIP well can be viewed through the transparent membrane. At left and right are temperature sensors placed on their own membranes for purposes of thermal isolation.

3. MICROHOTPLATE PERFORMANCE

Two essential characteristics of microhotplates are time response to a heating pulse, and steady-state power consumption. The time response of a HARSE etched, 1 mm^2 microhotplate to a square voltage pulse is shown in Figure 4. The device reaches $200\text{ }^\circ\text{C}$ in less than 8 ms and only 54 mW of applied power is required in the steady state. Larger membranes with an improved resistor design were also fabricated. For example, a 5.73 mm^2 HARSE-etched microhotplate reached $200\text{ }^\circ\text{C}$ in 11 ms and maintains that temperature with only 67 mW. Further enhancements in performance are expected as the heaters are inset further on the membrane and total heater resistance is reduced.

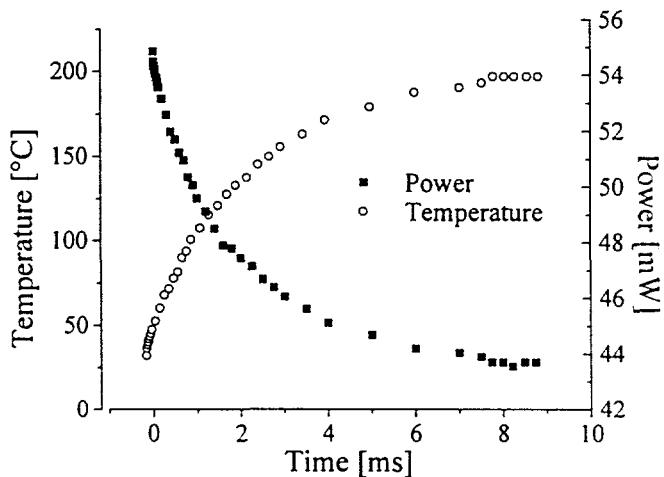


Figure 4: The time response of a 1-mm square hotplate to a square voltage pulse.

4. COMBINED DRI/WET ETCHING

A thin wedge of silicon often remains near the edges of a membrane after HARSE (Figure 5). This residual silicon, sometimes referred to as the silicon “foot”, is problematic for microhotplates and FPW devices. In the former case, the excellent heat conduction and large relative heat capacity of the silicon compromise the efficiency and speed of the hotplate. In the latter, the edge boundary condition of the membrane is poorly defined, and the acoustic modes are spoiled. Overetching to remove the foot is sometimes not a reasonable option due to the finite silicon nitride etch rate.

HARSE can be followed by a brief wet chemical etch to remove the residual silicon. After DRI etching to the membrane, the wafer is briefly inserted into a wet etch bath containing a common silicon etchant like aqueous KOH, TMAH or HF/Nitric/Acetic mixtures. Since these solutions have superior etch selectivity to silicon over silicon nitride, the foot can be removed without significantly etching the membrane.

The shape and orientation of the membrane is important during KOH etching when there is a significant amount of silicon remaining. One side of square membranes should be roughly aligned to the $\{100\}$ wafer flat to avoid unwanted widening of the etch pit as $\{111\}$ planes are exposed (Figures 6 and 7). Of course, circular membranes etched by HARSE will begin to take on a polygonal shape in KOH etching. If only a small foot remains, this shape modification may not be a problem depending on the intended application of the membrane device.

HF/Nitric/Acetic etches, sometimes called CP-4 or CP-8 depending on the relative concentration of the acids, can also be used to remove the silicon foot. Since they are isotropic silicon etchants, the

orientation problems noted above for KOH are not present with CP-x. However, CP-x also aggressively attacks many metals, especially the common Ti sticking layer. Thus, steps must be taken to protect metals from CP-x, and this can be a serious limitation of this approach.

Material	Etch Rate	Selectivity
Si {100}	2.5 - 3 $\mu\text{m}/\text{min}$	1
Thermal silicon dioxide	91 $\text{\AA}/\text{min}$	275
LPCVD silicon nitride	295 $\text{\AA}/\text{min}$	85
PECVD silicon carbide	180 $\text{\AA}/\text{min}$	139

Table 1: HARSE etch rates for various materials, and the ratios of the silicon etch rate to that of the listed material (selectivity).

5. COMPOSITE MEMBRANES

The DRI etch rate of SiO_2 is significantly less than that of silicon nitride (Table 1). Silicon dioxide would, therefore, appear to be a superior membrane material for DRI etched membranes since overetching could be used to remove the silicon foot without significant danger of etching through the membrane. Unfortunately, residual stress in oxide films is compressive, and silicon dioxide membranes tend to buckle.

A composite membrane material consisting of silicon nitride on top of silicon dioxide should be useful as a DRI etched membrane material. The tensile stress of the silicon nitride compensates the compressive stress in the silicon dioxide. Meanwhile, the oxide serves as an etch stop for the HARSE. Composite films of 1000 \AA of thermally grown silicon dioxide and 6400 \AA of PECVD silicon nitride are currently under investigation (Figure 8). Preliminary etch studies indicate that the HARSE selectivity to oxide is sufficient to permit overetching to remove the silicon foot. Also being studied are etch rates of oxynitride films.

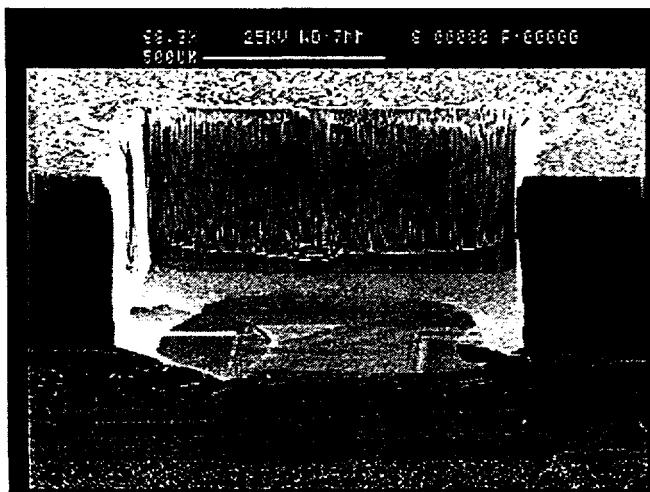


Figure 5: Cross section SEM of a DRI etched, magnetically-actuated FPW device. (During dicing the membrane cracked.) For illustration purposes the FPW is inverted such that the bottom of the wafer is at the top of the SEM. Metal lines can be seen through the thin membrane. Also noticeable is a thin layer of silicon remaining near the membrane edges (the silicon "foot").

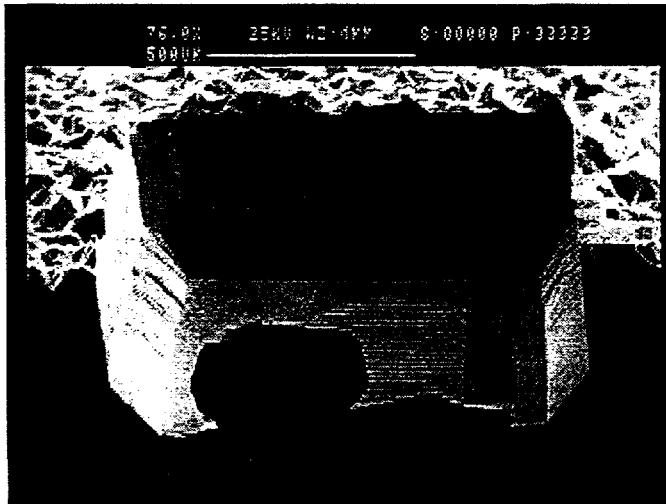


Figure 6: SEM view of a membrane produced by HARSE/KOH etching. The brief wet etch has revealed the {111} planes and reduced the size of the Si foot. With continued wet etching, the foot disappears. The roughness on the back side of the wafer is due to KOH etching of Si through pinholes in the nitride; the pinholes resulted from anomalous photoresist failure during HARSE. The membrane ruptured during dicing.

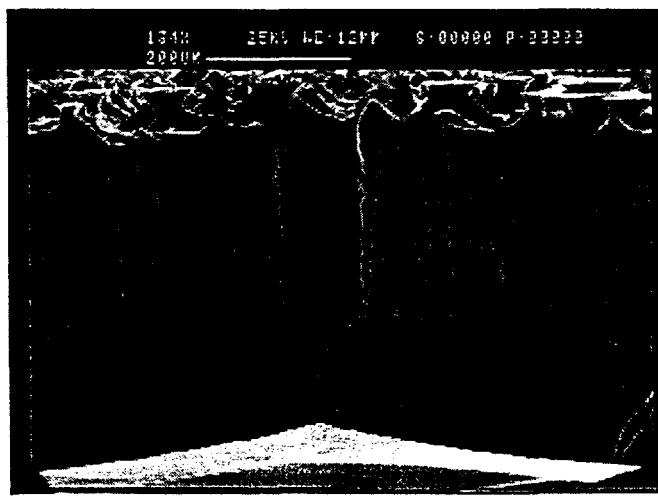


Figure 7: SEM close up of the etch pit corner of Figure 6. KOH is gradually revealing the {111} planes and reducing the size of the Si foot.



Figure 8: A composite membrane composed of 1000 Å of silicon dioxide and 6400 Å of silicon nitride. The oxide serves as an etch barrier so that the silicon foot can be etched without rupturing the membrane.

6. CONCLUSIONS

HARSE is a promising technique for the fabrication of membrane-based sensors and actuators. The rapid etch rate, crystal orientation independence, vertical side walls, high aspect ratios and CMOS compatibility of this technique lend it significant advantages over front or reverse side wet chemical etching. Vertical sidewalls and orientation independence, for example, allow for close placement of membranes and a significant reduction in consumed wafer area. The large, wafer-thick air gaps beneath HARSE etched membranes give them excellent thermal efficiency for microhotplate applications and increased deflection distance for pressure sensors and valves. Finally, although only dielectric membranes were shown here, silicon membranes can also be fabricated by this technique.

Poor etch selectivity of HARSE to silicon nitride, a popular membrane material, is an apparent disadvantage of this technique. Combined DRI/wet etching overcomes this limitation while preserving almost all of the advantages of HARSE. Composite oxide/nitride layers as well as oxynitride films show promise as membrane materials for use with HARSE.

7. ACKNOWLEDGMENTS

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