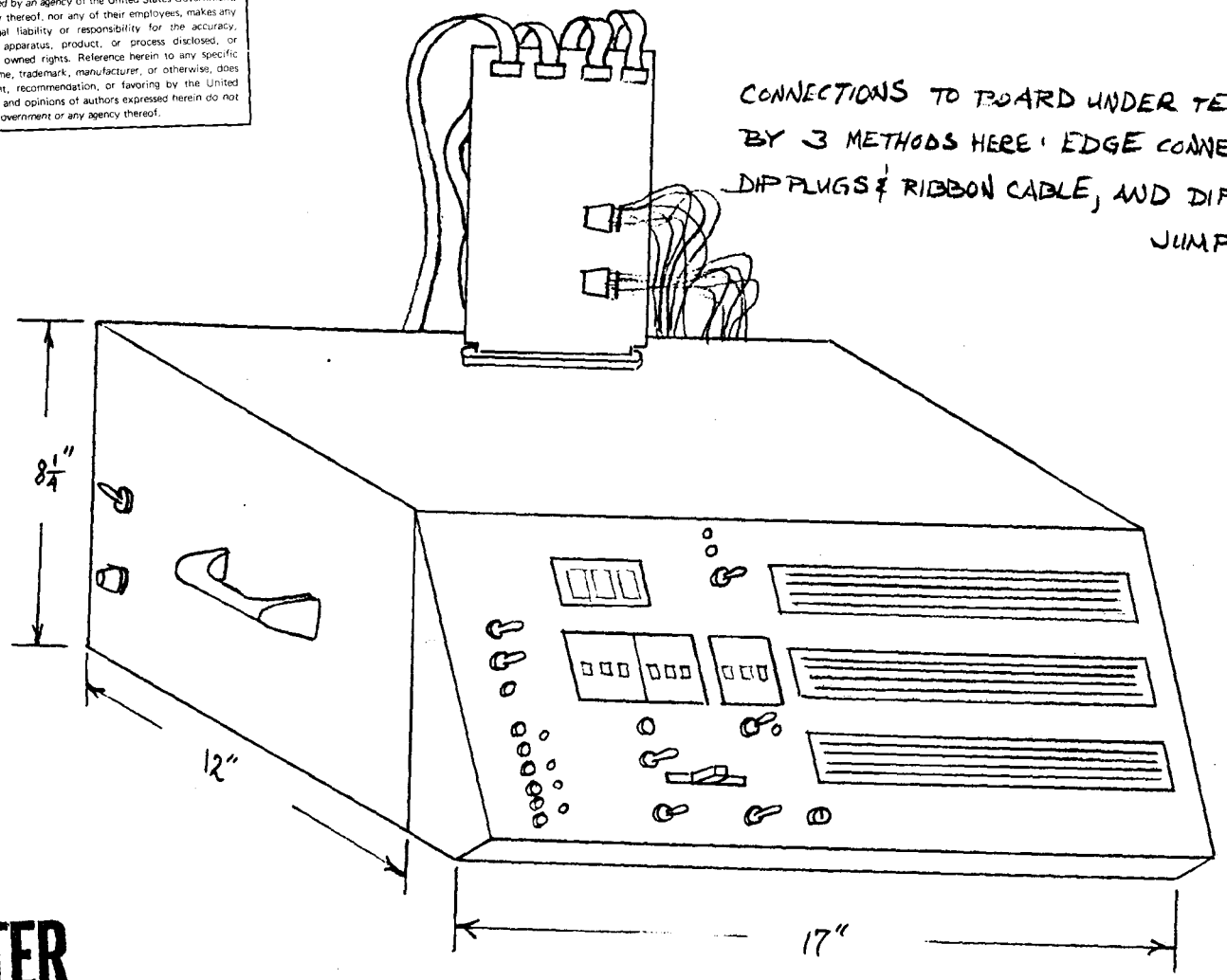
DOE/TIC--11398

CONNECTIONS TO BOARD UNDER TEST BY 3 METHODS HERE: EDGE CONNECTOR, DIP PLUGS & RIBBON CABLE, AND DIP CLIPS & WRAP-PIN JUMPER WIRES.



BONNEVILLE POWER ADMINISTRATION
H.Q. PORTLAND, ORE.
LOGIC BOARD TESTER,
GENERAL PURPOSE

Vilas Kaufmann

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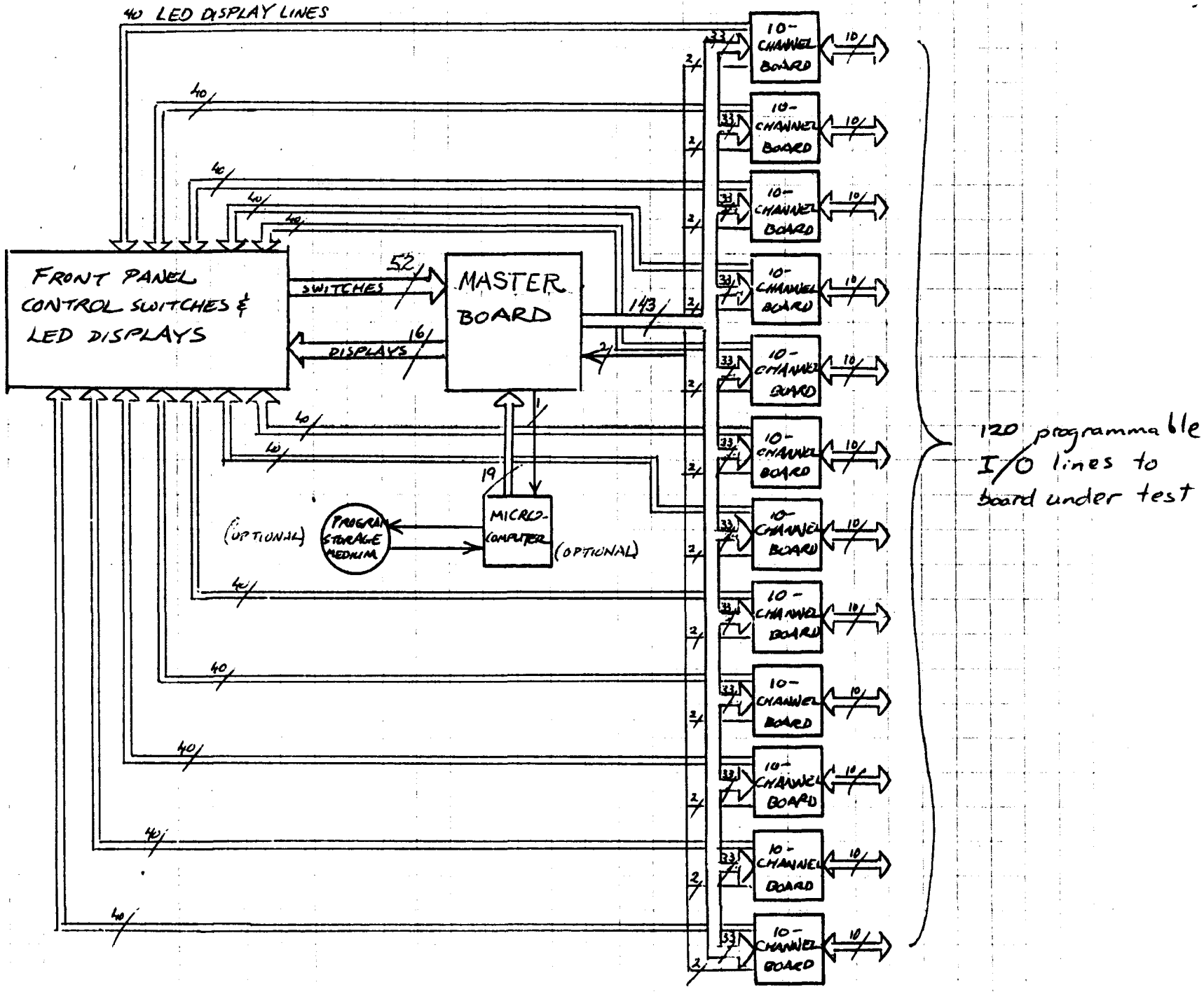
I. INTRODUCTION

As a logic board tester, this machine was designed to provide 120 independently programmable I/O channels, each having a 1024 bit data storage capacity. Its speed has been demonstrated at a solid 4.5 MHz (pin-change rate), and a glitch as narrow as 23 n-seconds on any channel should cause the machine to halt with an error indication in that channel. Narrower glitches will halt the machine without an error indication. As a secondary function, this tester should be able to operate as a basic data-domain logic analyzer, having the same performance features. Triggering on any combination of bits or channels is provided with up to 999 words of post-trigger recording within a memory frame of up to 1024 words, of up to 120 bits each. Another possible function of the tester would be programmable word generation. Programming is uncomplicated and programs may be modified "on the fly" during the board testing, a necessary feature in troubleshooting. Such modifications include addition or deletion of entire I/O channels and bit string generation of any predetermined length of 1's, 0's, or random patterns. This is in addition to single bit changes. It is possible to semiautomatically load square waves of varying periods, ranging from a change at every memory location, to a change after each 64 memory locations, each period being twice as long as the preceding one. Whole word transfers between any memory locations are very easy, enabling duplication or shifting of entire blocks of a program. A word search feature enables automatic location of any arrangement of bits of any length (up to 120). Various other convenience and fail-safe features are included.

See the introductory page of LOGIC BOARD TESTING-DETAILED VIEW

II. Block Diagram of Bonneville Power ADM Logic Board Tester



III. FAMILIARIZATION WITH TESTER

A. Power-On Initialization

1. All 120 channel registers are cleared. Each register holds 4 bits: a "BIT" gated to the data bus, and three channel function command bits, "TRIGGER", "INPUT and OUTPUT".
2. All the front panel thumbwheel switch settings are loaded into their respective registers on the Master Board.
3. The Hexadecimal Memory Address LED display shows that the channel memories are set at the "BEGIN" address of the PROGRAM BOUNDS thumbwheels.
4. The Master Board state LEDS show the machine to be in the "RECORD" (or "logic analyzer") mode, and the "DELAY" thumbwheel LED is lit showing that its value is set in the countdown register.

B. The PROGRAM BOUNDS Loop

1. The MEMORY SWEEP toggle is pressed to the right (count up), and, with the SWEEP RATE slide control set appropriately, the MEMORY ADDRESS display shows the channel memories to be looping between the BEGIN and END values set before power-on. Note the single step feature of this toggle.
2. Different values of BEGIN and END are entered by pressing the PROGRAM BOUNDS SET button. Note that this button does not work after the DELAY counter has caused a halt on completion of countdown (MEMORY SWEEP and CLOCK GENERATOR are both "dead" also). This condition is relieved by pressing the DELAY toggle up (SET), lighting the LED.
3. Pressing the MEMORY SWEEP toggle to the left causes the MEMORY ADDRESS to count down until the BEGIN value is reached whereupon countdown proceeds as the PROGRAM loop is exited.

C. The EDIT Functions

1. Unless stated otherwise, the two channel register ON-OFF switches, BIT and TRIGGER should always remain "OFF", to the left.
2. Press the CHANNEL SWEEP toggle to the right until the channel select cursor (top row of LED's) enters the field of active channels selected by a jumper wire on the Control Board. Continue to hold the toggle to the right and the cursor will loop through the active channels at the rate determined by the SWEEP RATE Control (slide pot). Pressing the toggle to the left causes the cursor to "home" on channels 0 and 120, dwelling alternately on these two.
3. The EDIT functions should not be clocked faster than about 1 MHz.

4. At power-on, any memory location will assume a somewhat random pattern of 1's and 0's for a given "word" comprising the active or implemented channels.
Clear such a word to all 0's by positioning the cursor over each MEMORY LED which is lit, making sure that the BIT switch is OFF, and pressing the WRITE button for each lit bit. Thus, each bit will go dark.
Write all 1's in any memory location by flipping the BIT switch to ON and pressing WRITE once as the cursor is positioned over each bit in a memory word.

5. Writing 1's and 0's "vertically" is even easier: first, dial in the length of the desired string of 1's or 0's in the DELAY thumbwheels, and press the DELAY toggle up, to SET. To clear a memory channel (writing all 0's), position the cursor over the desired bit position in memory, set BIT to OFF, hold WRITE pressed, and then either press MEMORY SWEEP to the right or turn CLOCK GENERATOR ON, momentarily. (Watch the PROGRAM BOUNDS) To write all 1's, first set BIT to ON and repeat.

6. To write a pseudorandom string of bits into a channel memory, first enable the random number generator by switching BIT to OFF and TRIGGER to ON. Now, the random string may be initialized by pressing the ENTER button for BIT and TRIGGER. The first 32 bits or so of the string are not truly random. They should be run out by advancing memory by 32 (HEX 20) counts. Reposition thememory to the starting location by pressing MEMORY BOUNDS SET. Dial in the length of the pseudorandom string in the DELAY thumbwheels, and press the DELAY toggle up to SET. If the DELAY LED was not lit, it must now be lit. Position the cursor over the selected channel. Press the WRITE (LOAD RANDOM PATTERN) button and hold it down. Press the MEMORY SWEEP toggle forward or momentarily run CLOCK GENERATOR and the random pattern is automatically loaded into the channel. For example, if the DELAY thumbwheel had a figure of 64 entered, and the MEMORY ADDRESS began at 0, at the completion of the random loading process, MEMORY ADDRESS would automatically stop at HEX 40 (Decimal 64). The latter applies to strings of 1's or 0's also.

7. Square waves having periods ranging from T_o to $64T_o$, where T_o is twice the length, in time, of one data frame from memory (or time between consecutive OUPUT pin changes) may be recorded in MEMORY. Connect square wave output from chip 17, pin 9 to EXTERNAL CLOCK input chip 16, pin 4, and then connect square wave chip 17, pin 8 to any channel I/O pin. Set CLOCK FREQUENCY selector to "1" for the basic square wave (or higher for longer periods). This square wave may be recorded by the TESTER in two modes: the Board Test Mode (INPUT/OUTPUT LED lit) and the RECORD mode (RECORD LED lit). In the Board Test mode any channel may assume one of three functions: INPUT, OUTPUT, or RECORDER (by default when neither INPUT nor OUTPUT, or when the CHANNEL REGISTER is cleared by pressing ENTER with BIT & TRIGGER OFF).

Every channel memory containing useful data must now be protected by accessing it with the CURSOR and pressing INPUT, if not done already. If done to OUPUT channels, their I/O lines must be disconnected (although OUTPUTS usually can be sacrificed). Now be sure that the channel for the square wave has its CHANNEL REGISTER cleared (making that channel a RECORDER), pressing ENTER, with BIT & TRIGGER OFF, to clear. Next, position the memory address to the beginning point for the desired string, by using MEMORY SWEEP, or by pressing PROGRAM BOUNDS SET, more typically. Now dial the decimal length of the desired square wave into the DELAY thumbwheels and press its toggle up (SET) to enter the value. Next, press the toggle down (COUNT), (noting that the LED goes out) to enable countdown. Then, momentarily switch on the CLOCK GENERATOR, and loading is complete.

The square wave always begins as a full half cycle high level. A convenient technique is to enter the full program loop length in the DELAY counter, or that plus 1, which brings the MEMORY ADDRESS back to the starting point (with the final square wave level in that location, however).

8. COPY

To "pick-up" a word in one memory location and automatically "deposit it" in another location, select the desired word by using MEMORY SWEEP. (To avoid possible problems, avoid doing this with the machine in the BOARD TEST mode: INPUT/OUTPUT LED lit.) When the desired word is displayed, press COPY and hold it pressed. Move the memory address (normally by using MEMORY SWEEP) to the deposit location. Release the COPY button. The word appearing at the selected location will disappear, and the selected word chosen by pressing COPY will now appear. This procedure does not destroy the copied word at the original location.

D. SEARCH MEMORY

This feature automatically locates those memory locations containing any given word or fragments of a word. First, clear all channel registers by pressing RECORD. Then, press SEARCH. Switch TRIGGER to ON. Position the cursor over each channel to be tested. Switch BIT on or off, as desired, and enter the value in the channel register by pressing ENTER. Reposition the cursor to program the next channel. Any number of combination of channels is thus programmed. Next, dial 000 into the DELAY thumbwheel switches, and press the DELAY toggle up to "SET". Then, press MEMORY SWEEP forward. The MEMORY ADDRESS will halt on the combination of digits entered in the channel registers. To start the next search after a halt, press the DELAY toggle up, to "SET".

E. SIMPLE BOARD TEST -- Simple Gates only; No Flip-Flops

The TESTER assumes the test mode after either INPUT CHAN or OUTPUT CHAN is pressed (so long as RECORD, which clears all the CHANNEL REGISTERS, is not pressed). Exit from this mode is accomplished by pressing RECORD. It is highly recommended that here the "CHANNEL BOARD" section of the TECHNICAL DESCRIPTION be read.

1. The program-building pass
   a. Clear the channel registers by pressing RECORD.
   b. Connect a known good board (or component) to the TESTER I/O ports by inserting it in a test socket or by attaching test leads. For practice, hook up a simple gate IC (7408, etc.).
   c. First, for the use of the microcomputer which may later record the finished program, a known "SCRATCHPAD" memory location must be selected and cleared for all output channels (meaning <u>from</u> the tester <u>out</u> to the board).
   At this point, the natural random pattern to exercise the inputs of the test board should be present in memory (since power-up). Position the cursor over each output channel and program its I/O port to be an output by pressing OUTPUT, MEMORY ADDRESS being at SCRATCHPAD for OUTPUT. Load in the PROGRAM BOUNDS, if needed. It is well to practice EDIT techniques 4, 5, 6, & 7 now that the TESTER is in the Board Test mode to experience building and modifying programs "on the fly".
   d. Press MEMORY SWEEP to the right or turn CLOCK GENERATOR on momentarily. After the memory has been swept through at least once, within the program bounds, the new test program is complete. The TESTER has recorded all signals appearing at any I/O port which has <u>not</u> been programmed as an INPUT or an OUTPUT. This is true at any time during the BOARD TEST mode.
2. The Program Verification Pass (or Test Pass)
   a. Now program the channels with the newly generated input data ("input" from the board under test to the TESTER) by positioning the cursor over each such channel and pressing INPUT.
   Another known scratchpad memory location needs to be selected and cleared for automatic entry of assigned input channels as the INPUT button is pressed.
   This is for later use by the microprocessor, as required.
   b. Press the PROGRAM BOUNDS SET button.
   c. Attach the bad board (or component) to be tested exactly as the good board was attached after program verification on good board
   d. Press MEMORY SWEEP to perform the test at low speed. For higher speeds, the CLOCK GENERATOR, residing on the Control Board (or external clock) should be used.
   e. As soon as the comparison circuitry detects an error, even if it is a very brief "glitch", the machine will halt instantly.* All I/O signals at the interface have been latched in the channels, and are displayed. By toggling the DISPLAY switch, MEMORY data is displayed alternately with GLITCH data in the same row of LED's. This causes any errors to blink the LED's, locating the exact point(s) of failure.

f. If constant false GLITCHES are experienced in d. & e. above, (TESTER shows error on an INPUT, whereas the actual circuit voltage matches the value in MEMORY), the test circuit is too slow for the TESTER[+] and the COMPARE DELAY segment of the delay line (SHEET 2 of 2) must be lengthened, either by advancing the delay tap feeding (47), pin 2 (@ 25ns/tap), or by inserting an additional delay line (e.g. Belfuse 0447-0750-05, 10 taps @ 75ns/tap) in the line to (47), pin 2. Currently, the Belfuse line is attached on the front edge of the MASTER BOARD and the taps are changed via wrap-pin jumpers, front panel control being a future refinement. Note that there is no lower response-time limit for recording; only for the actual board test (after the INPUT button is pressed for any channels).

g. Failures may be induced on inputs or outputs by momentarily shorting or pulling up. Note that even failures affecting only outputs are recorded, exactly as are the glitches in part (e), halting the TESTER. Toggling the DISPLAY likewise reveals these faults. In fact, this function is in effect while only output channels are assigned; a very useful feature during programming, revealing mistaken or faulty test connections. Use of a LOGIC PULSER is recommended.
A different type of failure may be induced by placing a small (100-600pF) capacitor to ground across a gate input or output. Note how the tester can be made insensitive (desensitized) to the error thus induced, by lengthening the COMPARE DELAY segment of the DELAY LINE.
In the "DETAILED VIEW" testing section ahead, it will be seen that for boards containing storage elements, such as flip-flops, it will be necessary to purge the board of bad logic states (initialize it) following each "glitch"-type failure to get it running again. Forcing one complete program cycle does this (press DELAY toggle up).

* Theoretically, glitches as narrow as 23 n-seconds may be recordable. Narrower glitches cause halts without recording the glitch. Instant halts for clock frequencies above about 2 - 3 MHz cease to be possible. At 4.5 MHz, the halt is one address location beyond the glitch. At 9 MHz the halt may be up to 2 address location beyond the glitch. Therefore, provision has been built into the MEMORY SWEEP toggle that sweeping in reverse does not execute program steps (inputs and outputs are frozen). Thus, one may step backwards through memory, toggling the display until the glitch appears.

+ This condition is highly beneficial, however, in revealing problematic slow circuits. In case where a given program will run on a known good board, and yet shows these symptoms on a problem board, this indicates the discovery of a slow I.C. Therefore, COMPARE DELAY should be minimized for each test program in order to sensitize the TESTER to slow circuits.

F. RECORD

This is the "logic analyzer" mode. Live data from operating equipment is recorded by connecting any of the 120 I/O lines to the points of interest, and simply clocking the TESTER via EXTERNAL CLOCK, internal signal generator, or even the CHANNEL SWEEP button. Only EXTERNAL CLOCK gives synchronous recording.

Pattern recognition triggering with post-trigger continuation of recording is set as follows:

1. Set TRIGGER ON
2. Enter the trigger pattern by positioning the CHANNEL CURSOR to each trigger location, switching DATA BIT ON or OFF, and pressing SET (under TRIGGER). Observe DATA BIT and TRIGGER LED's.
3. Dial in the number of clock cycles recording is to continue after trigger in the DELAY thumbwheels. Press SET (up).

This function should work, considering that its related functions SEARCH MEMORY & BOARD TEST do work. However, it has not yet been tested

J.F.

IV. USE OF TESTER PROGRAMMING SHEET

A. Spaces for two items are provided under each channel: the name of the point in the circuit being monitored or stimulated (typically, a circuit connector pin identification code) and, for OUTPUTS, an abbreviated program description for that channel.

B. OUTPUT channel numbers are underlined to distinguish them from INPUT channels.

C. Program Description Abbreviation Conventions:

1. Blank space: represents the "natural" random pattern occurring when power is turned on to the MEMORY. This is adequate for most OUTPUT needs.
2. Only a "1" or a "0": the entire program for this channel is all "1's" or "0's".
3. (A, B): C/D symbolizes that the contents of addresses A through B inclusive, are set at value C (1 or 0). D represents all the other addresses, which may be either $\bar{C}$ (0 or 1) or R, a random pattern.
4. T (A, B): $2^{X}T_{o}/D$ represents a square wave beginning with a high level at address A, and continuing to address B. $2^{X}T_{o}$ represents the period of the square wave where T_{o} is the fundamental test pin-change period (twice the time between address changes) and 2^{X} represents powers of 2, x being 0 through 6. D, as in part 3 is the remainder of the program being 1, 0, or R (random).
5. PR represents a pseudorandom data string. This may be used alone, filling the entire program memory, or it may be used in place of C or D in parts 3 or 4 above. The use of PR usually indicates that the random pattern is intended to be <u>varied</u> in the process of troubleshooting in order to more fully exercise the test circuit, activating unlikely responses from that circuit. This is easily done.
6. More complicated patterns will be indicated by reference to attached timing diagrams, etc.

D. Circuit modifications such as delay capacitors on flip-flops, interface IC's removed and replaced by sockets with component carriers wired to "jumper across" the interface, temporary rewiring of the circuit to provide clearing signals to flip-flops, memories, etc., should be listed at the top of the form.

MASTER COPY -- TESTER PROGRAMMING BOARD ID. _____ PROGRAM BEG ADDR ___ END ADDR ___

DELAY LINE SET: RAM SETTLING DELAY (ALWAYS MINIMIZE ~ 40ns) = ____. COMPARE DELAY (MINIMINZED) = ____.

Board modification for test -- for each cut land list: output node/INPUT CHAN // input node/OUTPUT CHAN or signal name

CH	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31	32	33	34	35	36	37	38	39	40
NAME																																									
PROGRAM																																								
CH	41	42	43	44	45	46	47	48	49	50	51	52	53	54	55	56	57	58	59	60	61	62	63	64	65	66	67	68	69	70	71	72	73	74	75	76	77	78	79	80
NAME																																								
PROGRAM																																								
CH	81	82	83	84	85	86	87	88	89	90	91	92	93	94	95	96	97	98	99	100	101	02	03	04	05	06	07	08	09	10	11	12	13	14	15	16	17	18	19	20
NAME																																								
PROGRAM																																								

MASTER COPY -- TESTER PROGRAMMING BOARD ID. #182-12104-1 (RODS) PROGRAM BEG ADDR 0 END ADDR 3E6

DELAY LINE SET: RAM SETTLING DELAY (ALWAYS MINIMIZE ~40ns) = 50ns. COMPARE DELAY (MINIMIZED) = ____.

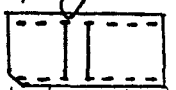
Board modification for test -- for each cut land list: output node/INPUT CHAN // input node/OUTPUT CHAN or signal name

Supply -12V to pin 73.
Add capacitors to ground:
150pF to U5-3
500pF to U22-4

U43-6 / CH79 // U34-2 / CH80

VH / NONE // U21-9 / SCRST (CH22)

Jumper plugs (in sockets) to replace I.C.'s:

U48: 

U42 & U46: 

CH	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31	32	33	34	35	36	37	38	39	40
NAME	P2-6	U21-8	DC4-5	DC5-13	DC4-6	DC4-7	DC4-14	DC4-8	DC4-15	DC4-9	DC4-16	DC5-1	DC3-10	DC2-1	DC2-2	DC2-3	DC2-4	DC2-5	DC2-6	DC2-7	DC2-8	DC4-3	DC2-15	DC2-9	DC2-10	DC2-11	DC2-12	DC2-13	DC2-14	DC5-10	DC3-4	DC3-8	DC3-9	DC3-7	DC5-3	DC5-2	DC3-11	DC3-12	DC3-13	DC3-14
PROGRAM	(4-11)=0/1	I(0,3E6)=I0												PR	"	"	"	"	"	"	"	(15,15)=0/1																			

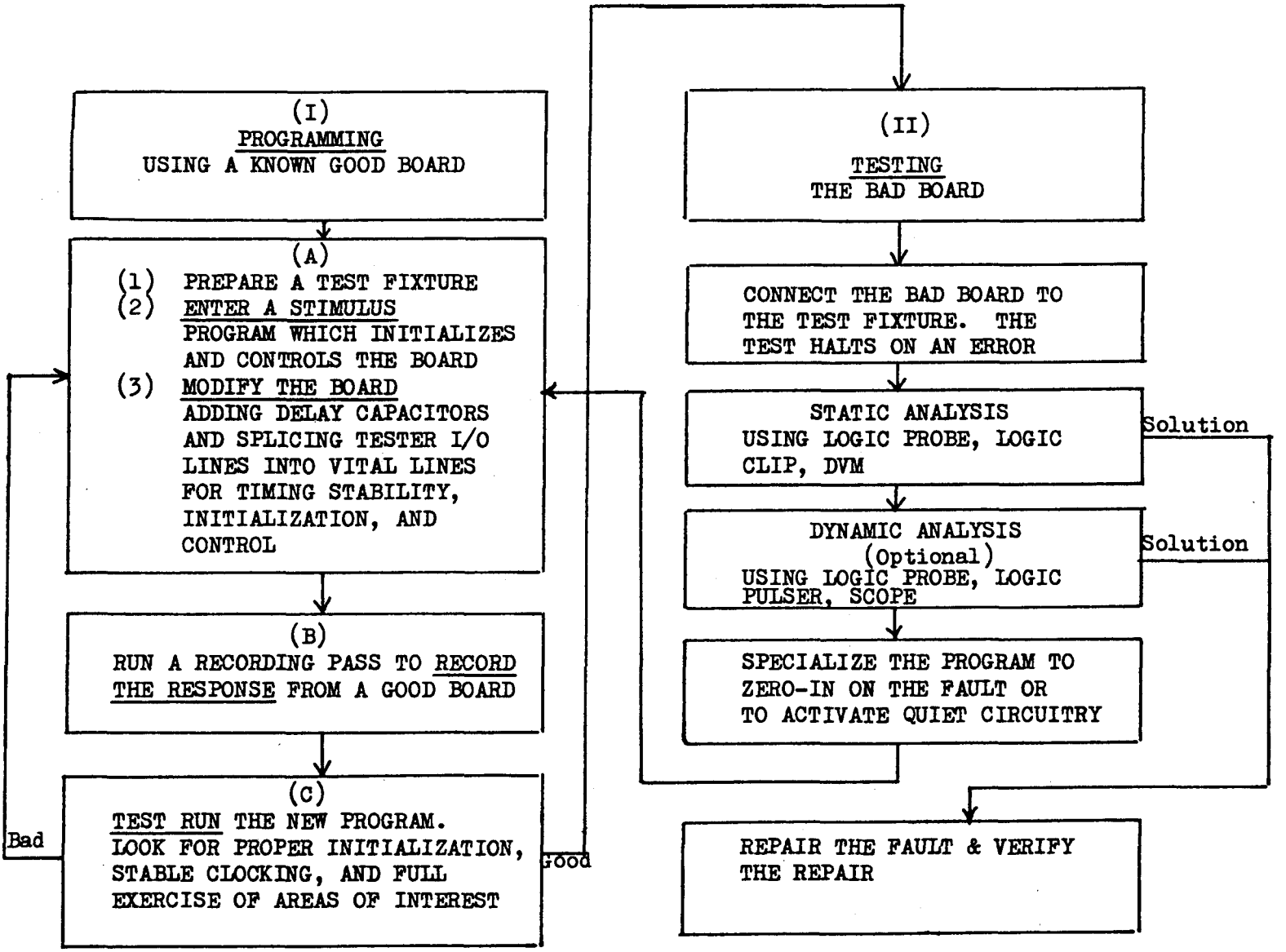
CH	41	42	43	44	45	46	47	48	49	50	51	52	53	54	55	56	57	58	59	60	61	62	63	64	65	66	67	68	69	70	71	72	73	74	75	76	77	78	79	80
NAME	DC3-2	DC3-5	P1-49	DC3-3	DC2-16	DC3-6	DC5-14	DC4-11	DC5-9	DC5-16	DC4-12	DC4-4	DC4-13	DC5-8	DC5-7	DC5-6	DC5-5	DC5-4	P1-75	DC5-11	DC5-12	DC3-15	DC1-4	DC1-10, 11	DC1-2	DC1-13	DC1-6	DC1-12	DC4-2	DC4-10	DC4-1	DC3-16	DC1-3	DC1-14					U43-6	U34-2
PROGRAM																																							PR	

CH	81	82	83	84	85	86	87	88	89	90	91	92	93	94	95	96	97	98	99	100	101	02	03	04	05	06	07	08	09	10	11	12	13	14	15	16	17	18	19	20
NAME	U40-12	U40-13	U40-14	U40-15	U41-12	U41-13	U41-14	U41-15																																		
PROGRAM																																								

V. LOGIC BOARD TESTING - DETAILED VIEW

This machine accomplishes testing by comparing a "signature" produced using a known good logic board with that of a faulty board. The good signature resides in the 1024-bit memories of any of the 120 independently programmable I/O channels. Errors in the board under test are revealed by alternately flashing the good signature and the test signature on the same set of display lights. Any discrepancy, or error, shows up as a flashing light, the other lights appearing to be steady on or off.

The testing process consists of two major phases: the program, building, or programming phase, and the testing phase.



A. PROGRAMMING

1. Documentation
   a. Mark the board logic diagram, writing TESTER I/O channel numbers next to the I/O pin numbers on the print.
   b. Fill out the TESTER programming sheet in pencil, marking the board I/O pin numbers next to each channel number

2. INTERFACING - using the TESTER programming sheet, connect wrap-pin jumper wires between the TESTER I/O pins and the test socket (usually an edge connector with wrap-pin tails) or fixture(s).
   a. Connections to IC's themselves should be via DIP clips having .030" diameter pins.
   b. Special interface chips can be handled by unsoldering them, inserting sockets, and plugging in component carriers wired to "dummy out" the chip.
   c. Other chips can be dummied out by replacing the chip with a socket and connecting TESTER I/O lines via DIP clips to the I/O signal lines of the extracted chip. The TESTER now "simulates" the chip.

3. LOAD THE BOARD STIMULUS (OUTPUT) PATTERN
   a. Decide how each input is to be stimulated. Random is good for most, but certain enables and many clocks will have to be specially dealt with.
   b. Choice of "canned" patterns
      1. The natural "random" pattern appearing in each memory at power-on. This may suffice for 90% of typical OUTPUT needs. No programming needed.
      2. Load string of 1's or 0's in each channel whose length is set by the number loaded into the DELAY counter. Complex combinations are possible.
      3. Load strings of pseudorandom patterns generated by the TESTER, likewise metered out in precise lengths.
      4. Square waves of periods ranging from the basic pin change rate, Fo to a minimum of 1/64 Fo (using IC 17 pin 8 as the signal source).
   c. Bit-by-bit writing of any pattern in any channel.

4. RECORD THE GOOD BOARD "SIGNATURE"
   Typically, this should be done first at a speed the eye can follow, using MEMORY SWEEP. This immediately discloses how the board is responding to your test program. Then, the board may be programmed beginning with the lowest CLOCK GENERATOR speeds. Note that even at this stage, the TESTER compares the data on the OUTPUT lines to the board under test with the data which is <u>supposed</u> to be on those OUTPUT lines. If, for some reason, such a line is being pulled high or low (most commonly due to interface

cabling mistakes joining a gate output on the test board with an I/O channel in the OUTPUT mode), the TESTER will halt and toggling the DISPLAY will reveal the discrepancy as a flashing light.

5. TEST THE NEW SIGNATURE ON THE GOOD BOARD
Command the OUTPUT channels to compare data. Using either MEMORY SWEEP or CLOCK GENERATOR, purge the board to be tested of any wrong logic states by forcing the TESTER to stimulate the board for at least one full program cycle, during which the board becomes initialized. The "halt override" is accomplished by pressing the DELAY toggle up to the SET position while clocking memory. Typically, on complex boards, especially those incorporating ROMS and many flip-flops, the program will not run the first time, halting on bad comparisons.
   a. Flip-flop timing problems are perhaps most common because random pattern testing is inherently prone to cause data change edges to coincide with clock edges at clocked flip-flops.
      1. Capacitors ranging from a few PF to about 700 PF (400 PF typical) are applied to either the clock or the data inputs and often the circuit is not indifferent as to which one.
      2. The points at which the capacitors are to be applied are discovered by toggling the DISPLAY. The blinking LED's, when correlated to the circuit diagram, will lead to certain flip-flops, and it takes but a few trials to discover where to apply the capacitor. These are best applied using round pin (.030 dia.) DIP clips and short wrap-pin jumpers. Tape the capacitor to the clip.
      3. Re-record the signature after each capacitor is applied and retest.
   b. Program, or signature, out-of-phase problems are perhaps the next most common and can be somewhat more challenging. A simple illustration of this problem is the flip-flop which changes state once (or any odd multiple of times) during a program cycle. So each succeeding pass, its output changes, and thus the TESTER detects an error on every other pass. Therefore, initialization of the board logic must occur sometime during every program cycle. Consequently, all crystal oscillators must be disabled, and free running counters must have their "CLEAR" inputs controlled by the TESTER. A somewhat more complex situation arises when the logic state of a board is independently controlled by a PROM program residing on the board. In one such case, the author found that the tri-state control input of the PROM could be used to create a floating (all 1's) logic level

from all the PROM outputs, and that this condition could be used to initialize the PROM iteself. It was found that one additional control over the PROM was quite helpful: a certain logic line controlled the stepping of the PROM from one state to the next, and originally this line was controlled by the PROM program itself. This line was cut and TESTER I/O lines were inserted to control and monitor the two cut ends. Thus, the PROM became the slave of the TESTER and the board was fully under control.

B. TESTING THE BAD BOARD

1. Two basic techniques are static analysis and dynamic analysis.
   a. In static analysis, the TESTER halts on an error and the error condition is thoroughly analyzed, using the board logic diagram to find out where a logic violation has occurred. This is quite effective for all types of short or open circuits or component failures. Logic probes, logic clips, and DVM's are usually needed. Slow logic is also detected.
   b. In dynamic analysis, the TESTER is forced to ignore error (DELAY toggle to SET) and continues to run. Sometimes, in this case, the speed of the test is made even greater than the speed at which the board runs in service. This is useful for revealing timing problems, "noisy" circuits producing gating or switching spikes (usually 50 n-sec. or less, requiring clocking at several MHz to be seen on a scope), or bad chips generating intermediate logic levels at certain times.

2. The program is specialized and expanded to "home in" on the error.
   Additional channels are programmed by attaching DIP clips to certain chips in the circuit where the error is suspected to originate. This takes us back to part I, Programming, but note that the program constructed thus far is not harmed or erased in the least by this process. It is merely added on to.

3. Sometimes "nuisance halting" on minor errors is encountered and it is not desired to take time to add a delay capacitor, etc. The offending channels can quickly be eliminated from the test by locating them with the CURSOR, setting the BIT and TRIGGER switches OFF, and pressing ENTER.

4. Full use should be made of DVM's oscilloscopes, logic probes, logic pulsers, logic clips, and any other diagnostic equipment commonly used in board troubleshooting to aid in tracking down the fault.

5. Minor modifications to the basic test program are sometimes helpful, such as changing clocking or timing, enabling or disabling certain gates to get a better view of gate activity, or

shooting new random patterns into certain OUTPUT channels to bring certain PROM outputs to life at certain times, for example. The latter technique is also sometimes useful to cure "two cycling" (flip-flop problems) where the program runs successfully only on every other pass.

It is possible to edit a test program "on the fly" in the middle of testing a bad board. Normally, to use the TESTER's EDIT features, one clears the machine first by pressing RECORD. This however, is not absolutely necessary, since the basic EDIT features (writing individual 1's or 0's, strings of 1's or 0's, or strings of random patterns) are functional during the board test mode (the INPUT/OUTPUT TESTER state LED is lit). OUTPUT channels are unaffected by such editing. INPUT channels get all 1's written into the current memory address location. This might appear to be a nuisance, but actually is not since the editing of an OUTPUT channel necessarily requires a re-recording of responses on the INPUT channels from a good board. It's no problem that an obsolete part of the program gets messed up. Even this problem can be avoided by "neutralizing" the INPUT channels prior to editing (see C, above).

VI. TECHNICAL DESCRIPTION

A. CHANNEL BOARD

General:

Each channel board consists of 10 independently programmable I/O channels. Basically, each channel may be independently or jointly edited, and during logic board testing it may independently assume any one of its three primary functions: transmitter (OUTPUT), receiver (INPUT), or recorder (by default, when neither OUTPUT nor INPUT). As a transmitter, it sends a stimulus program from the RAM to the board being exercised. It also checks the I/O line to the board to make sure that there is no fault (high or low) on that line by comparing (ME) and (EX) at the COMPARATOR, and simultaneously halts the TESTER and records the fault in the GLITCH CAPTURE LATCH in case of a fault. As a Receiver, it compares an expected good response previously recorded in RAM with the actual response again at COMPARATOR inputs (ME) and (EX), and in case of a noncomparison, the COMPARATOR halts the TESTER and clocks the GLITCH CAPTURE LATCH in time to record any glitch longer than 23 n-seconds, theoretically. Incidently, every output from every COMPARATOR is wired to every GLITCH LATCH, thus causing a snapshot of all events going on at the time of the GLITCH to be taken. As a recorder, the channel I/O line is gated to the D in (Data Input) of the RAM, which is enabled to write. The remaining basic function, the secondary function, is editing, and this is mainly accomplished via the buffer gated by (F). The operator or the microcomputer controller has access to the RAM input, via buffer (F). Another edit feature exploits the MEMORY LATCH which holds memory output while the memory address is changing. Thus, memory data for all channels may be transferred and written into any memory location. A secondary function for buffer (F) is to provide a steady level initiated by the operator or microcomputer, to the input of the COMPARATOR. This allows one to search memory or check the data stream arriving via the I/O lines.

1. THE DATA BUS

The DATA BUS is the heart of the TESTER, consisting of a signal loop beginning and ending at each channel RAM; at D out and D in, respectively. The RAM output, D out, is fed directly to the DISPLAY MULTIPLEXER for display on an LED. It also goes to the MEMORY LATCH, whose primary purpose is to block address-change transients from the rest of the circuitry. It is also used for latching D out data for writing back into RAM at a different address. Next along the loop we see a group of tri-state buffers, and a COMPARATOR gating network consisting of one complete 74LS08 and a complete 74LS51. This gating network feeds the 20 input COMPARATOR and its associated GLITCH CAPTURE LATCH, comprising two LS04's and two LS174's for all 10 channels. Buffer (C) blocks RAM data, permitting comparison of RAM data with either "BIT" data from buffer (F) or I/O data from the board being tested or recorded. Buffer (D) permits recording of I/O data.

Buffer (H) permits output of I/O data. Buffer (E) blocks I/O data being input to RAM from conflicting with "BIT" data which is being used to screen or search I/O data for a specific event.

2. CHANNEL COMMAND AND DISPLAY

a. Channel command is handled by the CHANNEL REGISTER and the CHANNEL FUNCTION ROM. The CHANNEL FUNCTION ROM (CFR) contains all of the command signals to the channel with the exception of TRIGGER which is used in conjunction with other commands. TRIGGER in effect, enables the COMPARATOR. The CFR receives two categories of inputs: master commands applying to all channels, which may be constant, from the MASTER REGISTER, or momentary, occurring in conjunction with the COPY button, and mixed commands from the CHANNEL REGISTER and from the MASTER BOARD, which may also include momentary signals from the MASTER BOARD.

b. The actual display for each channel consists of four dedicated LED's in a column arrangement. They are labelled from the top, as "CUR" for cursor, and "1", "2", and "3". The CHANNEL SELECT CURSOR consists of one signal line to each channel coming from the 1 of 120 decoder on the MASTER BOARD. This signal directly lights the "CUR" LED. LED's 1, 2, and 3 display two sets of three quantities, being driven directly by the DISPLAY MULTIPLEXER. LED 1, thus, shows "BIT" and "INPUT". LED 2 shows "TRIGGER" and "OUTPUT". LED 3 shows "MEMORY" and "GLITCH".

This arrangement was carefully chosen so that "BIT" and "TRIGGER", which are associated channel commands, can be seen together. Likewise, the associated commands INPUT and OUTPUT are viewed together. The multiplexing of "MEMORY" and "GLITCH" on the same LED is crucial to the use of the TESTER, because this permits the blinking of discrepancies arising in the data comparisons which the TESTER continually performs. Valid comparisons do not blink; mismatches blink. Switching from one set of 3 data quantities to the other is accomplished by a panel mounted switch.

The CHANNEL SELECT CURSOR does two other things: it gates the CHANNEL REGISTER load clock originating from front panel button hits or from the microcomputer; it also enables a tri-state buffer from the channel data bus to gate data to the microcomputer.

B. MASTER BOARD

GENERAL:

The MASTER BOARD functions can be grouped into two categories: addressing and clocking of the channel RAM's (Sheet 2 of 2), and channel function command and control (Sheet 1 of 2).

1. ADDRESSING AND CLOCKING OF MEMORY

The heart of these functions is the MEMORY COUNTER: three 74LS169's providing the 10-bit HEX address to the RAM. This counter is parallel loaded with a starting address from the LOWER MEMORY BOUND LATCHED MULTIPLEXERS (MBLM), (14), (15), and (18). An upper bound address is contained latched in multiplexers (33), (32), and (31), the outputs of which are fed to the UPPER BOUND COMPARATOR (21). When the MEMORY COUNTER output matches the upper bound address, (21) produces a level which causes the lower bound address to be loaded on the next positive clock transition. Thus, the count loops within the established bounds. The MBLM's are loaded from two sources: the microcomputer or the HEX-coded BEGIN and END PROGRAM loop BOUNDS thumbwheel switches, and their associated "SET" button which provides the clocking edge to load both the multiplexer latches and the MEMORY COUNTER.

The DELAY COUNTER stops the MEMORY COUNTER after a predetermined number of counts have elapsed. This feature is used for a variety of purposes, especially during editing, for writing predetermined lengths of data strings into memory, and during the RECORD mode, when recording can be allowed to go on for up to 999 clock cycles after the trigger event has been recognized by the channel COMPARATORS. Loading of the DELAY COUNTER is by means of the BCD thumbwheel switches, whose values are manually entered by pressing the DELAY toggle up to SET, or by pressing the PROGRAM BOUNDS SET button. Countdown is enabled in the DELAY COUNTER by the D type flip-flop (43) pin 8 going low. This flip-flop drives the DELAY LED, and has a variety of control inputs. The flip-flop PRESET (count) input is controlled by two front panel buttons: the DELAY toggle can be pressed down (COUNT) or the WRITE button may be pressed. Both initiate DELAY counting, indicated by the DELAY LED going out. The CLEAR input is enabled by pressing the DELAY toggle up (SET), or by the POWER-UP PULSE GENERATOR. Both load the count-down value into the DELAY COUNTER and remove the counter enable signal. The clocked input, D, of the same flip-flop is used as a missing pulse detector in the cases where the tester is looking for a particular data combination or "word" to come up in an "unknown" data stream; in other words, it seeks a data comparison in a long stream of non-comparisons. A series of non-comparisons produces a square wave from the COMPARATOR to the D input. A comparison is detected as a missing low level in the wave, a high being the COMPARATOR output for a match.

A minimum of 200 n-seconds is required from the time the MEMORY COUNTER is clocked to the time that a result returns to the MASTER BOARD from the COMPARATOR, explaining the reson for the delay line. Gate (410) pins 1, 2, and 3 insures that counting stops immediately as zero is attained. This is important when the machine is to be halted instantly on detection of the sought data combination (DELAY thumbwheels set to 000).

A similar flip-flop, (43) pin 5 is Q, controls MEMORY COUNTER. This one has three controls. The final CARRY output of the DELAY COUNTER goes low when a count of zero is reached. This output is wired to the CLEAR input of the flip-flop, causing Q to go low at zero. This shuts off the clock to the MEMORY COUNTER at (51) pin 3. The PRESET input of this flip-flop is driven by two sources. First, the POWER ON PULSE GENERATOR provides the PRESET in order to insure that the flip-flop is set to permit clocking of the memory counter. This same initialization pulse is used to clock the LOWER BOUND ADDRESS into the MEMORY COUNTER. Second, the vitally important ability to force the MEMORY COUNTER to keep going while the COMPARATOR circuitry is trying to shut it down, is provided by means of the DELAY toggle being pressed up (SET). This manual halt override allows viewing of failure events on an oscilloscope. The third control is the CLOCK input used to clock the low level tied to the D input to shut down the clock to the MEMORY COUNTER at (51), pin 3. Chip (41) pin 13 gates the output of the COMPARATOR circuitry to turn off the MEMORY COUNTER whenever a <u>non-comparison</u> of data is detected, as during BOARD TEST, when the expected circuit signature is continually matched with the actual circuit response to detect any deviation. Note that this same CLOCK signal is also fed down to the ENABLE inputs of the MEMORY COUNTER (11) pins 7 and 10. This provides a few nanoseconds of advance reaction time to halt the COUNTER before a possible clock comes along, which becomes significant at high frequencies. The Q output of this flip-flop also feeds pin 10 of (51) which is designed to stop any pulses which may be travelling in the delay line at the time that a halt is required. The $\overline{Q}$ output performs this same function at pin 10 of (45) which strobes the COMPARATOR circuitry.

The final major circuit on SHEET 2 of 2 is the frequency selectable SIGNAL GENERATOR. The 9 MHz crystal oscillator feeds the 8-output frequency divider (17), which, in turn, feeds most of its outputs into the 1 of 8 selector (16). One of the selector inputs (position 1 on the rotary switch) is for an EXTERNAL CLOCK for all purposes. The two unused divider outputs may be jumpered to this input. The output of the frequency selector feeds a positive edge detection circuit, the two flip-flops (44), and (410), and (52). (44) at the switch prevents switching transients. The effect of this circuit is to insure that an integral number of full square wave cycles is always presented to the TESTER.

2. CHANNEL FUNCTION COMMAND AND CONTROL

This discussion focuses on sheet 1 of 2, where we find the manual MEMORY and CHANNEL CURSOR sweep circuit, the CHANNEL CURSOR counter and decoder/driver circuit, the PSEUDORANDOM SEQUENCE GENERATOR, the POWER-UP PULSE GENERATOR, and the main feature, the CHANNEL FUNCTION COMMAND AND CONTROL circuitry associated with the 9 pushbuttons and switches on the left.

a. COMMANDS: BIT, TRIGGER & ENTER; INPUT & OUTPUT; RECORD; SEARCH; COPY & WRITE

1. The two double pole switches and their associated momentary pushbutton, at the top, BIT, TRIGGER, and ENTER, are for conditioning one channel at a time. By pressing ENTER, the settings of BIT and TRIGGER are both clocked into the CHANNEL REGISTER selected by the CURSOR. The effect on the channel of these two signals has been discussed in part A. You will note that the ENTER level is differentiated between (42) pin 6 and (510) pin 4 to produce a leading edge clocking spike. The need for this was due to the necessity of using an LS32 as the clock gate for the CHANNEL REGISTER. The ENTER button serves a secondary function of initializing the PSEUDORANDOM SEQUENCE GENERATOR. This GENERATOR is enabled by setting BIT to OFF and TRIGGER to ON. This secondary function of these switches does not conflict with their primary function, as described. TRIGGER, enabling (45) pin 1, gates the GENERATOR output to OR gate (48), requiring BIT to be OFF.
2. The INPUT and OUTPUT buttons are related and cause similar events. At this point, it will be helpful to refer to the PROM PROGRAM sheet. Three basic things are accomplished by pressing either of these buttons: the CURSOR selected channel is commanded to be either an INPUT or an OUTPUT I/O channel; the entire TESTER is caused to go into the BOARD TEST mode (INPUT/OUTPUT LED is lit) meaning that (41) pin 12 permits COMPARATOR outputs to halt the TESTER on a data mismatch, and the PROM program causes all designated INPUT (or OUTPUT) channels to cause a 1 to be written in the current memory location which must be a scratchpad location. Pressing the other button would pick out just the OUTPUT (or INPUT) channels. These two scratchpad locations in memory are accessible by the microcomputer so that it will know how to automatically redesignate the INPUT and OUTPUT channels from a tape recording made of the MEMORY contents after a particular test has been perfected. A fourth thing, which happens as a secondary functio, is that the MASTER REGISTER cell which stores the OR'ed combination of INPUT and OUTPUT (lighting the INPUT/OUTPUT LED, and enabling the COMPARATOR output to the MEMORY COUNTER) also inhibits the entry of any other button hit into the MASTER REGISTER via

gate (52). The only way to change the BOARD TEST state is by master clearing the TESTER by pressing RECORD, which clears all the CHANNEL REGISTERS but preserves MEMORY. The WRITE button and all of the EDIT features of the BIT, TRIGGER, and ENTER controls are still in effect during the BOARD TEST mode, a highly useful feature for editing programs during testing. Note that pressing either INPUT or OUTPUT sends a level via OR gate (59) to a differentiator, producing a clocking spike at [F] for the purpose of clocking channel assignments into scratchpad memory via (WE) on the CHANNEL BOARD.

3. The RECORD button is next on the panel. Pressing it sends a CLEAR level to all 120 CHANNEL REGISTERS, and then clocks a low level into the MASTER REGISTER which lights the RECORD LED. This low level also enables gate (49) which permits an inhibit level from the MEMORY SWEEP toggle to prevent writing into RAM and clocking of the MEMORY LATCH. The purpose of this is to permit the operator to examine the TESTER's MEMORY contents in the channel LED's without changing the contents of MEMORY. Once the RECORD button has been pushed, pushing anyone of thelower four command buttons both enters that button's flag in the MASTER REGISTER, lighting the associated LED, and clears out the previous flag in the MASTER REGISTER. The top two buttons INPUT and OUTPUT work a bit differently, as discussed above.

4. The next button in line is SEARCH, which enables the TESTER to have its memory contents automatically searched for any data pattern. Pressing this button merely enters the flag in the MASTER REGISTER which addresses all the CHANNEL FUNCTION ROMS to look for BIT and TRIGGER flags being set in any CHANNEL REGISTERS. Thus, when the TRIGGER flag is set in any channel, the associated BIT, high or low, becomes part of the data combination which will set off the COMPARATORS when that combination comes up in MEMORY, halting the TESTER immediately if 000 is entered in the DELAY COUNTER.

5. The next button is COPY. Pressing this button inhibits clocking of the MEMORY LATCH, allowing the 120-bit MEMORY word residing there when the button was pressed to be automatically written into any other memory location or its own location, when the button is released. First, the COPY/WRITE flag of the MASTER REGISTER is SET, and along with it the "COPY" bit of the REGISTER, at pin 2. This sets address 2 at the CHANNEL FUNCTION ROM which by itself, disables any writing to MEMORY. While the COPY button is held pressed, input [C] to the clock gate ((53) pin 8) for RAM Write Enable and MEMORY LATCH clocking is held low, preventing clocking.

MEMORY LATCH clock input [G] receives one positive transition, loading this latch with MEMORY contents at the current address as COPY is pressed. After a tiny delay, the portion of the CHANNEL FUNCTION ROM address, which is in effect only during the cutton pressing phase of the COPY operation, arrives at the ROM, adding address 1 to address 2 already there for a complete address of 3, which enables (G), allowing a write clock to reach the RAM, and also enables (E), which gates the output of the MEMORY LATCH to the D in (data input) of the RAM. Now, all that is needed to write the LATCH into the RAM is a clock. At this point the RAM address may freely be changed so long as COPY is held pressed. Releasing the COPY button generates this clock at [F]. Since releasing this button also changes the CFR address back to 2 from 3, a small delay network at (69) pin 13 stretches the addressing level until the clock from [F] has done its work. After this point, it is necessary that the MEMORY SWEEP may be used to change the MEMORY address for viewing of MEMORY contents without spoiling them. Therefore, address 2 remains at the CFR to insure this protection.

6. The WRITE button is used primarily to write a 1 or a 0 into any address location of any channel memory (RAM). By holding it pressed, strings of 1's or 0's may be written in a RAM. Also, if the PSEUDORANSOM SEQUENCE GENERATOR is enabled, as discussed above, random bit strings may likewise be written into RAM while holding both WRITE and MEMORY SWEEP pressed. The source of the data written in RAM is the CHANNEL REGISTER BIT latch, via buffers (F) and (E), activated during CFR address 16 (HEX). When WRITE is pressed, the MASTER REGISTER WRITE flag is set, producing address 6 at the CFR, which, by itself, inhibits writing to MEMORY. Another path from the WRITE button goes to (59) pin 9, which applies an input at (J) of the CHANNEL REGISTER and produces address 6 at the CFR also. This same path (to (59) pin 9) also branches to produce a clocking spike for the CHANNEL REGISTER which results in address 16 now being presented to the CFR. This same clocking spike has also clocked BIT into the CHANNEL REGISTER so that the data to be clocked into RAM becomes present at D in (RAM) and all that is needed is a clock. This clock is produced at F by differentiating the voltage transition produced by pressing WRITE. When WRITE is released, a spike generated at (67) pin 13 clears the CFR. The WRITE flag remains present in the MASTER REGISTER which permits one to use MEMORY SWEEP to view MEMORY contents without damage to the data.

b. The POWER-UP PULSE GENERATOR is based on the high input impedence characteristic of 74C14 Schmitt trigger hex inverters, causing the R-C networks at (611) to have long time constants. The principle

of operation is that initially, as power is applied, pins 4 & 5 of (45) must have opposite values, causing pin 6 to be high. After a long time has elapsed and both capacitors have changed fully, pins 4 & 5 again have opposite values, but these are now swapped with respect to their initial state. The POWER-UP PULSE is produced during the time that the voltages on pins 4 & 5 are trading places, one changing faster than the other. If the voltage that was high changes first, both 4 & 5 will be low simultaneously for an instant, producing a low-going pulse at pin 6.

c. The PSEUDORANDOM SEQUENCE GENERATOR was borrowed from the Ideas for Design Section of Electronic Design, July 19, 1979.

d. The CHANNEL CURSOR counter and decoder/driver is a stright-forward 128-count HEX counter driving a 1 of 120 decoder. The highest count pin (usually 120) signals a load input of the counter to parallel load what is usually all zeroes (a grounding plug to all inputs when a microcomputer is not in use). This produces a repetetive cycling of the CURSOR to all CHANNEL positions. Note that any one of the 120 decoder outputs may be last, so fewer than 120 channels may be implemented. The microcomputer has full control over the CURSOR.

e. The last major component is the MEMORY and CHANNEL CURSOR SWEEP circuit, based on a 555 timer (56). This circuit allows virtually identical control of both MEMORY and CHANNEL addresses. One may sweep both up and down, vary the sweep rate, and single-step up or down by momentarily pressing the sweep controls. A single step delay is incorporated such that, when pressing the toggle, a clock (single-step) pulse is sent out, followed by a reasonable delay before the 555 pulse generator cuts in to generate the sweep pulse train. Note that the MEMORY SWEEP OUTPUT unconditionally reaches the MEMORY COUNTER via K. However, clocking to the WRITE ENABLE of RAM and to the MEMORY LATCH is controlled by an elaborate gating scheme. For example, the latter clocking is inhibited during the RECORD mode at (49) pin 1, and also during MEMORY SWEEP in reverse, at (410) pin 13. This is to prevent the contents of memory from being damaged, or to inhibit program execution during BOARD TEST.

VII MAINTENANCE AND TROUBLESHOOTING

Most troubleshooting of the TESTER should be no more than moderately challenging at the worst, and practically all debugging experienced to date indicates that a competent technician, having the circuit drawings, the annotated "X-ray" view print of the CHANNEL BOARD, the MASTER BOARD layout print, and the TECHNICAL DESCRIPTION, should find most possible problems relatively easy to fix. The key to the special ease of troubleshooting the tester, besides simplicity of design and physical layout, is the LED display panel. Virtually all functions or malfunctions in the CHANNEL BOARD are reflected in the LED's. So, a fairly thorough checkout of the TESTER is possible by manually exercising each one of the LED's. This consists of addressing each channel and "ENTER"ing the various combinations of BIT and TRIGGER, "WRITE"ing ones and zeros in channel MEMORY, and then pressing INPUT and OUTPUT, noting the lighting of the corresponding LED's, and the writing in MEMORY of a "1" for each command. A further checkout would be the writing of various length strings of square waves in MEMORY as outlined in the FAMILIARIZATION section, part C.7. A more primitive exercise would be simple grounding of each channel I/O line while running in RECORD, watching each LED blink off as it is grounded. The remaining functions might be similarly exercised, as desired.

The static checkout procedures, detailed above, are especially useful in troubleshooting a CHANNEL BOARD on an extender card. The board layout facilites troubleshooting because the board consists mostly of 10 identical CHANNEL circuits in virtually identical parallel, consecutively numbered layout. Therefore, testing by comparing a suspected bad CHANNEL against a good one speeds fault location greatly. Probably the best place to begin comparing signals is the CHANNEL FUNCTION ROM, the obvious "nerve center".

PROGRAMMING FOR TBP18S030N CHANNEL FUNCTION PROM

Address	Function	PROM Output: 8 7 6 5 4 3 2 1 / Output Name: H G F E D C B A — Code	HEX
0	③	1 0 0 1 0 1 1 0	96
1	—	0 0 0 0 0 0 0 0	00
2	⑧ (≠①-IDLE)	1 1 0 0 1 1 0 1	CD
3	① (ACTIVE)	1 0 1 0 1 0 0 0	A8
4 & 5	—	0 0 0 0 0 0 0 0	00
6	⑦ (≠②-IDLE)	1 1 1 0 1 0 0 0	E8
7	—	0 0 0 0 0 0 0 0	00
8	⑤	0 1 1 1 1 0 1 0	7A
9	—	0 0 0 0 0 0 0 0	00
A	WRITE O.C. ONLY	1 0 0 0 1 1 0 0	8C
B ÷ D	—	0 0 0 0 0 0 0 0	00
E	INHIBIT WRITE	0 1 0 1 0 0 0 0	50
F	—	0 0 0 0 0 0 0 0	00
10	⑥	1 1 1 1 1 0 1 0	FA
11	—	0 0 0 0 0 0 0 0	00
12	INHIBIT WRITE	0 1 0 1 0 0 0 0	50
13-15	—	0 0 0 0 0 0 0 0	00
16	WRITE I.C. ONLY & ② (ACTIVE)	1 0 0 0 1 1 0 0	8C
17-1F	—	0 0 0 0 0 0 0 0	00

O.C. = ALL OUTPUT CHANNELS RESIDENT IN CHAN. REGISTER

I.C. = ALL INPUT CHANNELS RESIDENT IN CHAN. REGISTER

① = COPY WORD
② = WRITE BIT or PAPER TAPE TO MEMORY (μC)
③ = RECORD
④ = SEARCH MEMORY
⑤ = OUTPUT CHANNEL
⑥ = INPUT CHANNEL
⑦ = MEMORY TO PAPER TAPE (μC)

$(A = 2+8)_{16}$

$(E = 6+8)_{16}$

$(12 = 2+10)_{16}$

$(16 = 6+10)_{16}$

OUTPUT see note (A)

INPUT see note (B)

(A) Pressing OUTPUT writes channel assignments in scratchpad. Function ⑤ (OUTPUT) remains in channel reg. after OUTPUT button is released. This activates address 8

(B) Pressing INPUT writes channel assignments in scratchpad. Function ⑥ (INPUT) remains in channel reg. after INPUT button is released. This activates address 10_{16}.

MOTOROLA M6800 MICROCOMPUTER INTERFACE (USING MC6820 PIA) PROGRAMMIN

CA1	Word recognition strobe to μC (SEARCH MEMORY & RECORD) Input to μC only				
$\overline{CA2}$	RAM address advance, clock & instrument function command clock excluding individual channel functio				
$\overline{PA7}$	Enable for individual channel function load clock ($\overline{CB2}$)				
$\overline{PA6}$	" " instrument function load clock ($\overline{CA2}$)				
"	" " channel address load clock ($\overline{CB2}$)				
$\overline{PA5}$	" " RAM High Address load clock ($\overline{CB2}$)				
$\overline{PA4}$	" " " Low " " " ($\overline{CB2}$)				
$\overline{PA3}$	" " channel address clock (advance or load) (CB2)				
PA2	DATA — Memory out to μC. Programmed as an input line				
PA1	RAM address line 10				
PA0	" " " 9				
PB7	" " " 8				Address lines for individual channe
PB6	" " " 7	Channel address line 7		Address lines for instrument	functions (used w/ $\overline{PA7}$ & $\overline{CB2}$ pulse
PB5	" " " 6	" " " 6		functions (used w/ $\overline{PA6}$ & $\overline{CA2}$* pulse)	BIT ⊛
PB4	" " " 5	" " " 5		MEMORY TO TAPE	TAPE TO MEMORY
PB3	" " " 4	" " " 4		SEARCH MEMORY*	OUTPUT
PB2	" " " 3	" " " 3		SIGNAL GENERATOR ENABLE	INPUT
PB1	" " " 2	" " " 2		CLOCK MEMORY*	TRIGGER (enables COMPARATOR)
PB0	" " " 1	" " " 1		MASTER CLEAR	
CB1	Input to μC only (Not used)				
$\overline{CB2}$	Clock pulse - see above.				

⊛ used with trigger or as a data bit to memory comin from tape.

† This is an instrument funct

PARTS LIST

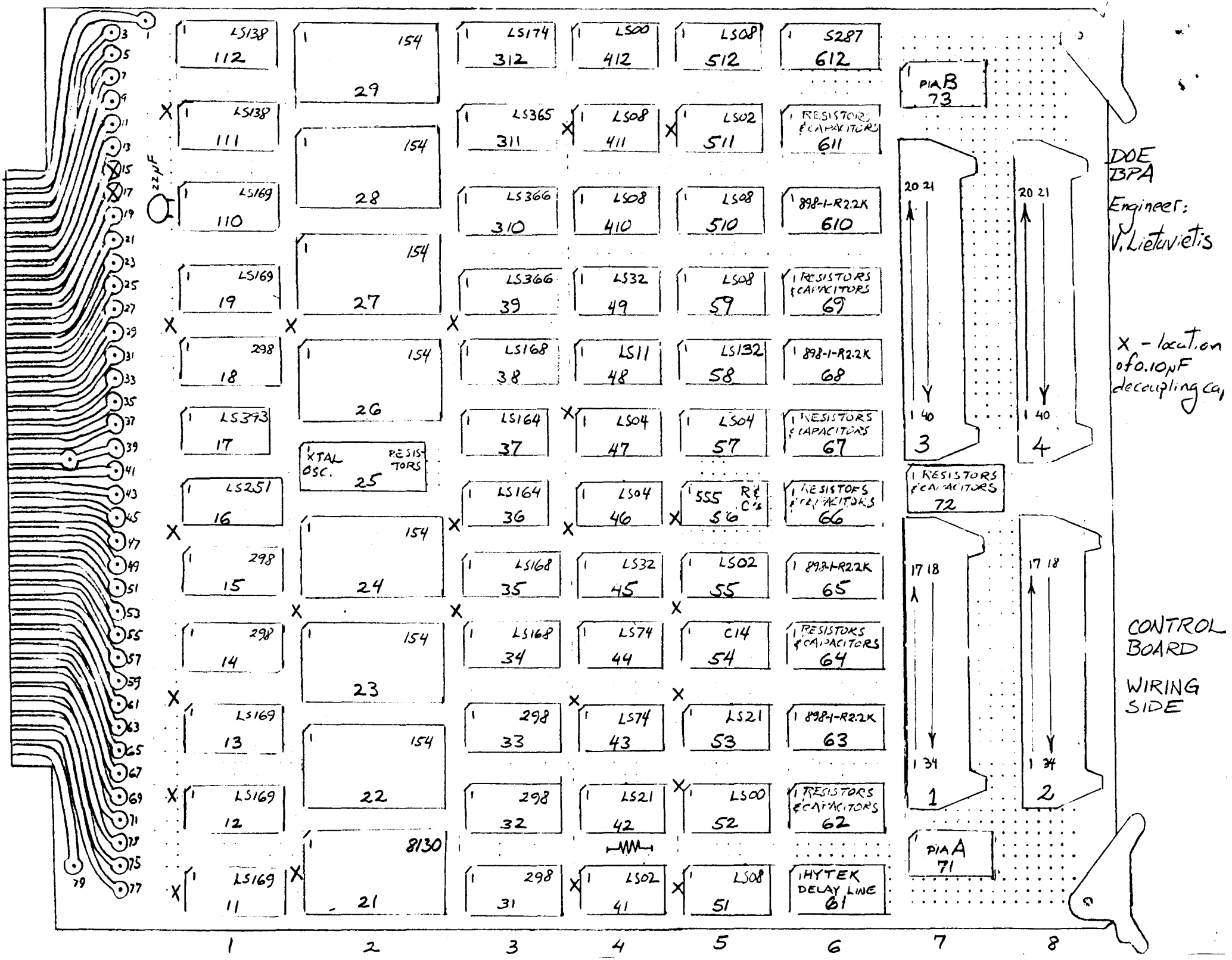
PART #	DESCRIPTION	AMOUNT	MANUFACTURER
CCK 17	Rack mountable card cage	1 ea	Vector
Custom	Front panel, 8 3/4 X 16 3/4 X 3/32, Aluminum	1 ea	In-House
	" " piano hinge, 1 1/2 X 16 3/4	1 ea	"
Custom	" " slope spacers, 25° wedge	2 ea	In-House
LYS-W-5	Power Supply, 5V, 30A	1 ea	Lambda Electronics
Custom	Channel Board, printed circuit	12 ea	Electronic Controls Design
3673	Plugboard (for Master Board)	1 ea	Vector
Custom	LED display board	4 ea	Electronic Controls Design
32F1462	LED, red	487 ea	Monsanto
T65-73MA6-SP	Thumbwheel switch, HEX. Custom, complement-only version of T65-13M6 with center blank spacer	1 ea	Cherry
T65-12M3	Thumbwheel switch, BCD complement only	1 ea	Cherry
SF21SCW191	Submin. toggle switch. ON-NONE-ON	4 ea	Cutler-Hammer
SF22FHW191-5	" " " MOMEN-OFF-MOMEN	3 ea	"
SA41SDW2	" pushbutton switch, momentary	8 ea	"
11700 Series	BCO-1, 14-pin BC DIP switch (8 position), octal output coded, 000,001,010,011,100,101,110,111	1 ea	Edison Electronics Div. McGraw-Edison
12200 Series	Front panel adapter	1 ea	
US155L	Slide potentiometer, 1.5 Meg, linear	1 ea	TRW
SW53AA147	Slip-on button, white	1 ea	Cutler-Hammer
SW53AA148	" " red	3 ea	"
SW53AA149	" " black	1 ea	"
SW53AA150	" " blue	2 ea	"
SW53AA152	" " green	2 ea	"
SW2AA10	Decorative bezel nut	15 ea	"
R680	Mating connector	15 ea	Vector
S-202	Circuit card ejector	26 ea	Scanbe
10200-800-10-.3C	Bus bar, dual voltage	108 ea	Bussco Engineering Inc.
ECI-6102-6-10.3	Bus bar, two bus voltage	7 ea	Eldre Components, Ir
923875-R	Double-row jumper header 40 post	12 ea	AP Products, Inc.
609-3442M	Wrap-post tail header, 34 pin	4 ea	T&B Ansley
609-4042M	" " " " 40 pin	4 ea	"
609-3400M	" " socket transition conn. 34c	4 ea	"
609-4000M	" " " " " 40c	16 ea	"
609-4003	Transition connector, PC board, 40c	12 ea	"
71-40	Flat cable "Blue Macs", 40 cond.	20' est	"
71-34	" " " " 34 cond.	5' est	"
71-14	" " " " 14 cond.	2' est	"
	Wire-wrap wire, No. 30	300' est	"
C-49	Pin, Klip-Wrap	82 ea	Vector
SC-1P4-CC	Lead socket, .030 - .040 lead	144 ea	Samtec
28524-01	IC socket, 24 pin, low prof., solder	12 ea	TI, etc.
28516-01	" " 16 pin " " "	504 ea	"
28514-01	" " 14 pin " " "	564 ea	"
CA-14S-103WW	" " 14 pin wire wrap	29 ea	Circuit Assemblies
CA-16S-103WW	" " 16 pin " "	34 ea	" "
CA-20S-103WW	" " 20 pin " "	1 ea	" "
CA-24S-103WW	" " 24 pin " "	20 ea	" "
D447-0750-05	Digital delay line, 75ns/tap	1 ea	Belfuse Inc

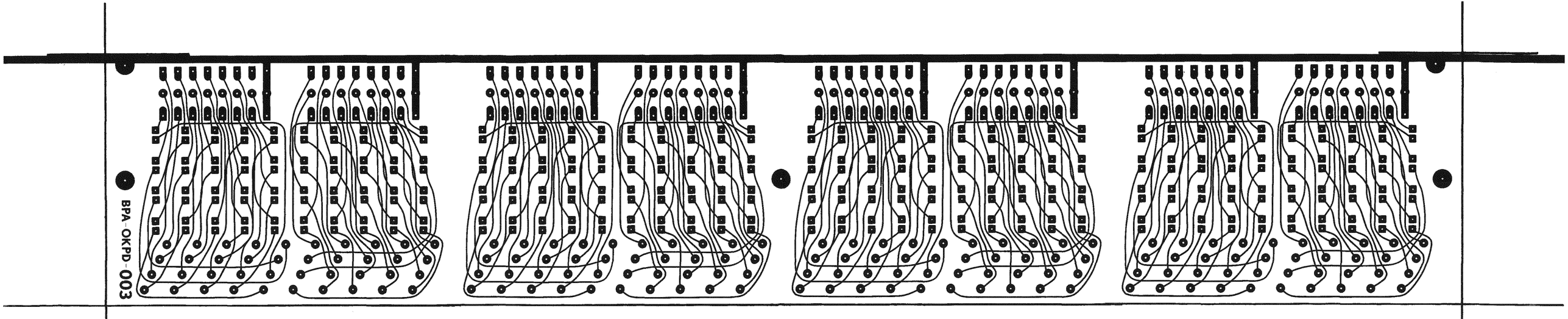
P A R T S L I S T

PART #	DESCRIPTION	AMOUNT	MANUFACTURER
HY-5010-250	Digital delay line, 25ns/tap	1 ea	Hytek Microsystems
S15R5-9	DIP crystal oscillator, 9 MHz	1 ea	Connor-Winfield Cor
74LS00	I.C.	2 ea	TI, etc.
74LS02	"	3 ea	"
74LS04	"	63 ea	"
74LS08	"	126 ea	"
74LS11	"	1 ea	"
74LS21	"	2 ea	"
74LS32	"	62 ea	"
74LS51	"	120 ea	"
74LS74	"	2 ea	"
74LS125	"	180 ea	"
74LS132	"	1 ea	"
74LS138	"	2 ea	"
74LS158	"	96 ea	"
74LS164	"	2 ea	"
74LS168	"	3 ea	"
74LS169	"	6 ea	"
74LS174	"	169 ea	"
74LS251	"	1 ea	"
74LS365	"	1 ea	"
74LS366	"	2 ea	"
74LS393	"	1 ea	"
74C14	"	1 ea	"
74154	"	7 ea	"
74298	"	6 ea	"
74S287	" (PROM)	1 ea	"
TBP18S030N	" (PROM)	120 ea	"
2125AL	" (RAM)	120 ea	Intel
3130	"	13 ea	National Semiconductor
555	"	1 ea	T.I.
764-1-R470	SIP resistor network, 470 ohm/pin	72 ea	Beckman Instruments
398-1-R22K	DIP " " 2.2K ohms/pin	4 ea	" "
	Resistor, 150 ohm, 1/4 W	1 ea	
	" 270 " "	1 ea	
	" 330 " "	1 ea	
	" 470 " "	6 ea	
	" 560 " "	5 ea	
	" 680 " "	6 ea	
	" 1K " "	7 ea	
	" 1.5K " "	3 ea	
	" 2.2K " "	3 ea	
	" 33K " "	1 ea	
	" 39K " "	1 ea	
	" 82K " "	1 ea	
	" 120K " "	1 ea	
	" 220K " "	1 ea	
	" 3.3M " "	1 ea	
	Capacitor, 500 pF	1 ea	
	" .001 mF	1 ea	
	" .01 mF	1 ea	
	" .10 mF, Tantalum	243 ea	
	" .15mF "	5 ea	
	" .33mF "	6 ea	
	" .47mF "	4 ea	
	" .68mF "	2 ea	

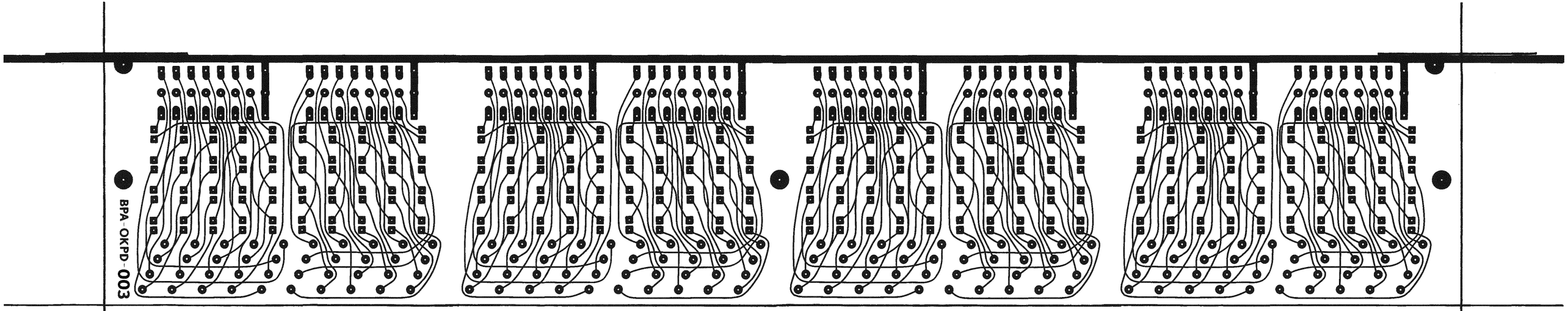
P A R T S L I S T

PART #	DESCRIPTION	AMOUNT	MANUFACTURER
	Capacitor, 1.0mF Tantalum	2 ea	
	" 1.5mF "	1 ea	
	" 6.8mF "	1 ea	
	" 22mF "	13 ea	
552-303Y-ICO/2	Shield beads, ferrite	36 ea	Krystinel Corp.
	I/O line jumper leads, wrap-pin sockets at ends, assorted lengths (& colors) from 9" to 18".	200 ea (Minimum)	
	Parts for <u>one</u> jumper:		
AP 923612	Contact Socket	2 ea	AP Products Inc.
	Stranded Wire, No. 28	9" - 18"	
	Heat-Shrink Tubing, 1/8" dia X 3/4"	2 ea	

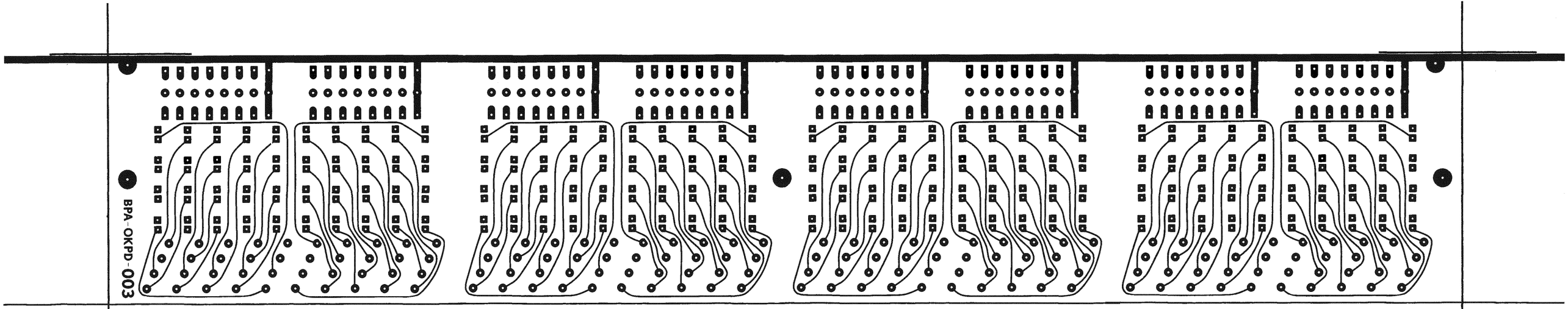

LS138 112
154 29
LS174 312
LS00 412
LS08 512
S287 612
PIA B 73
LS138 111
LS365 311
LS08 411
LS02 511
RESISTORS & CAPACITORS 611
22µF
LS169 110
154 28
LS366 310
LS08 410
LS08 510
898-1-R2.2K 610
20 21
1 40
3
20 21
1 40
4
DOE IBPA
Engineer:
V. Lietuvietis
LS169 19
154 27
LS366 39
LS32 49
LS08 59
RESISTORS & CAPACITORS 69
X - location of 0.10µF decoupling cap
298 18
154 26
LS168 38
LS11 48
LS132 58
898-1-R2.2K 68
LS393 17
XTAL OSC.
RESISTORS 25
LS164 37
LS04 47
LS04 57
RESISTORS & CAPACITORS 67
LS251 16
LS164 36
LS04 46
555 R & C's 56
RESISTORS & CAPACITORS 66
RESISTORS & CAPACITORS 72
298 15
154 24
LS168 35
LS32 45
LS02 55
898-1-R2.2K 65
17 18
1 34
1
17 18
1 34
2
298 14
154 23
LS168 34
LS74 44
C14 54
RESISTORS & CAPACITORS 64
CONTROL BOARD
WIRING SIDE
LS169 13
298 33
LS74 43
LS21 53
898-1-R2.2K 63
LS169 12
154 22
298 32
LS21 42
LS00 52
RESISTORS & CAPACITORS 62
8130
LS169 11
298 31
LS02 41
LS08 51
HYTEK DELAY LINE 61
PIA A 71
1 2 3 4 5 6 7 8



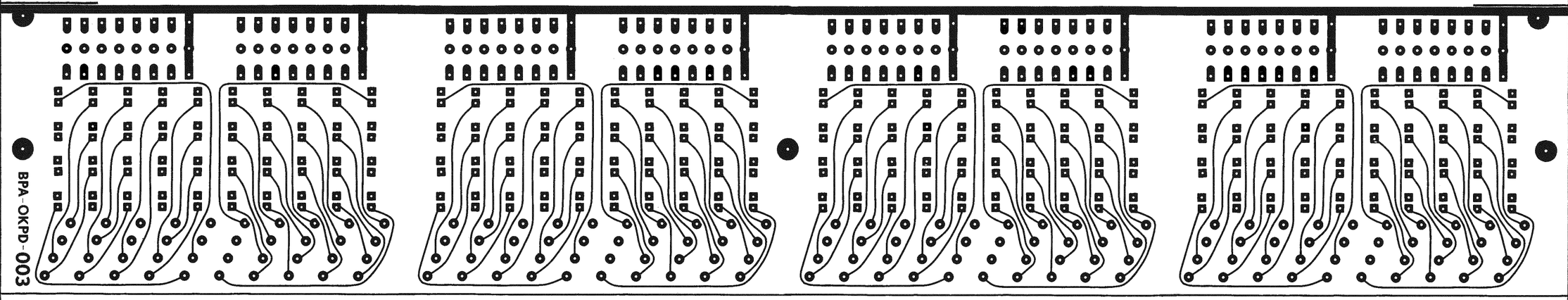
X-RAY VIEW
LED DISPLAY BOARD, 40 CHANNEL
DOE, BONNEVILLE POWER ADMINISTRATION
V. LIETUVIETIS



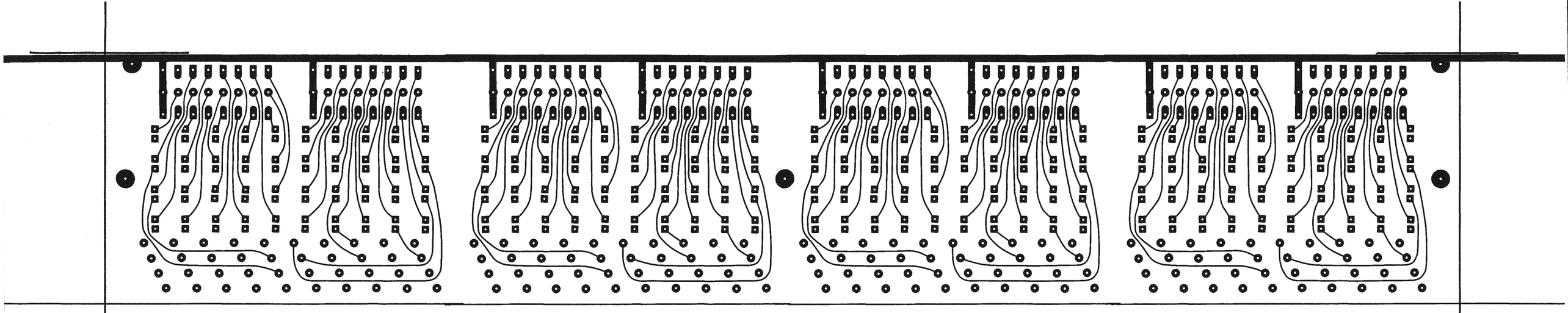
X-RAY VIEW
LED DISPLAY BOARD, 40 CHANNEL
DOE, BONNEVILLE POWER ADMINISTRATION
V. LIETUVIETIS



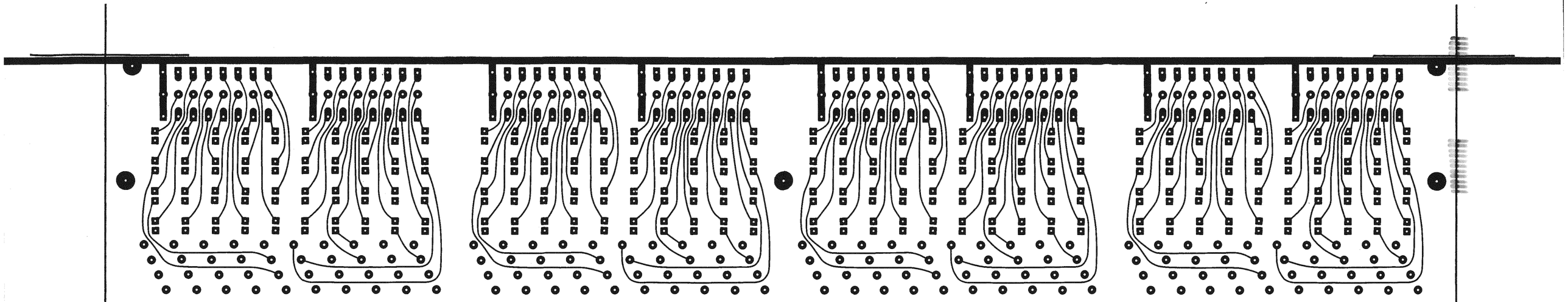
FRONT VIEW
LED DISPLAY BOARD, 40 CHANNEL
DOE, BONNEVILLE POWER ADMINISTRATION
V. LIETUVIETIS



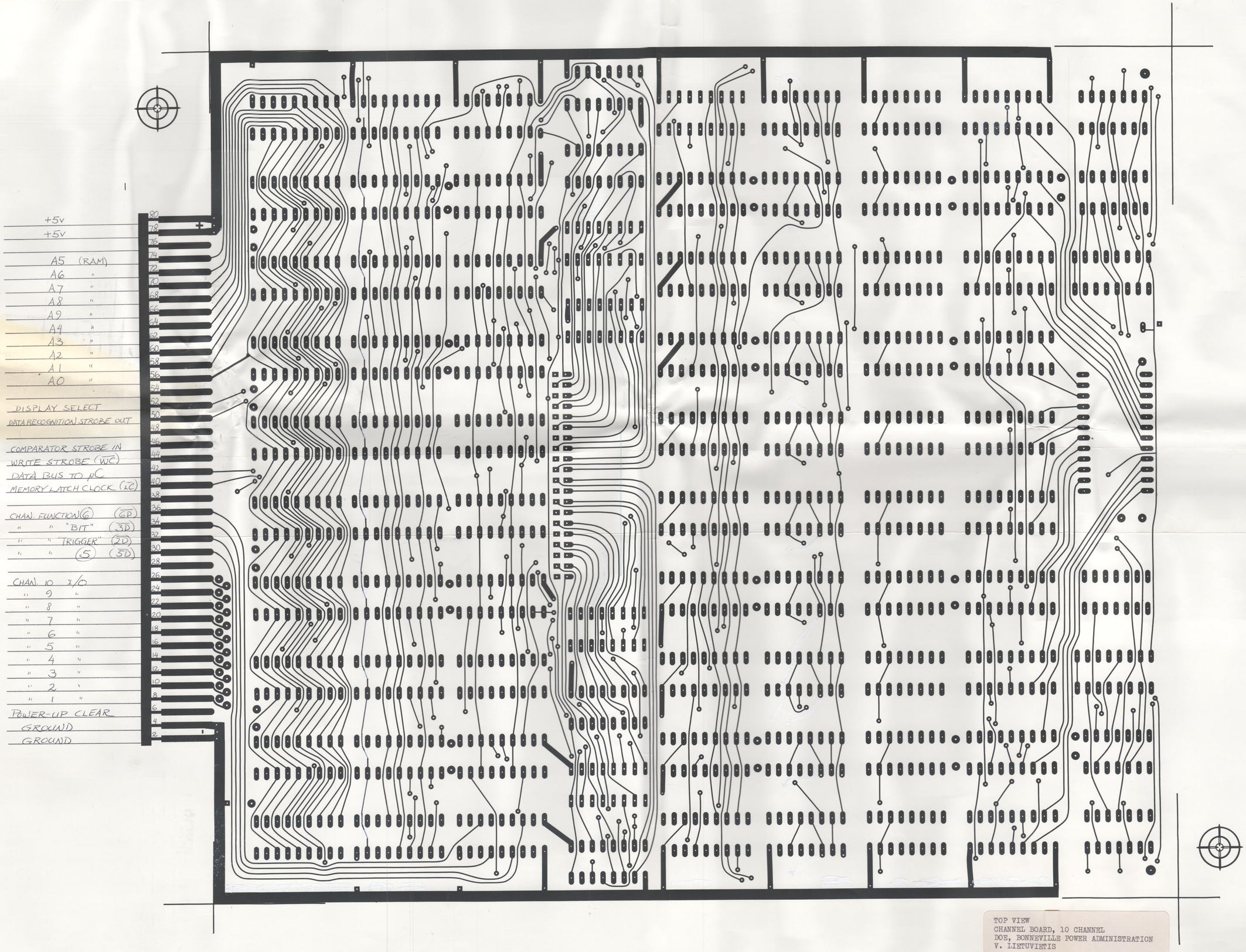
FRONT VIEW
LED DISPLAY BOARD, 40 CHANNEL
DOE, BONNEVILLE POWER ADMINISTRATION
V. LIETUVIETIS



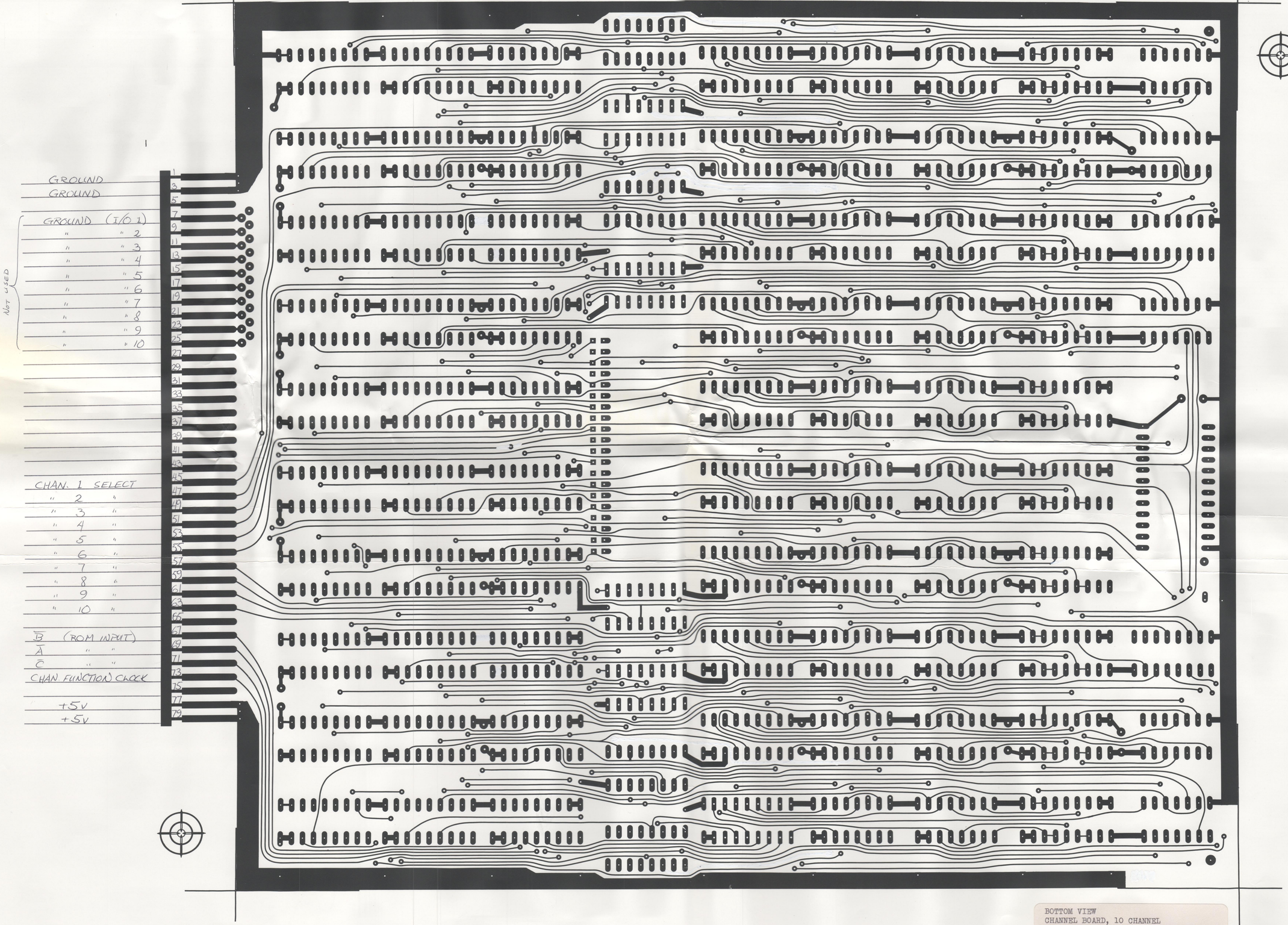
BACK VIEW
LED DISPLAY BOARD, 40 CHANNEL
DOE, BONNEVILLE POWER ADMINISTRATION
V. LIETUVIETIS



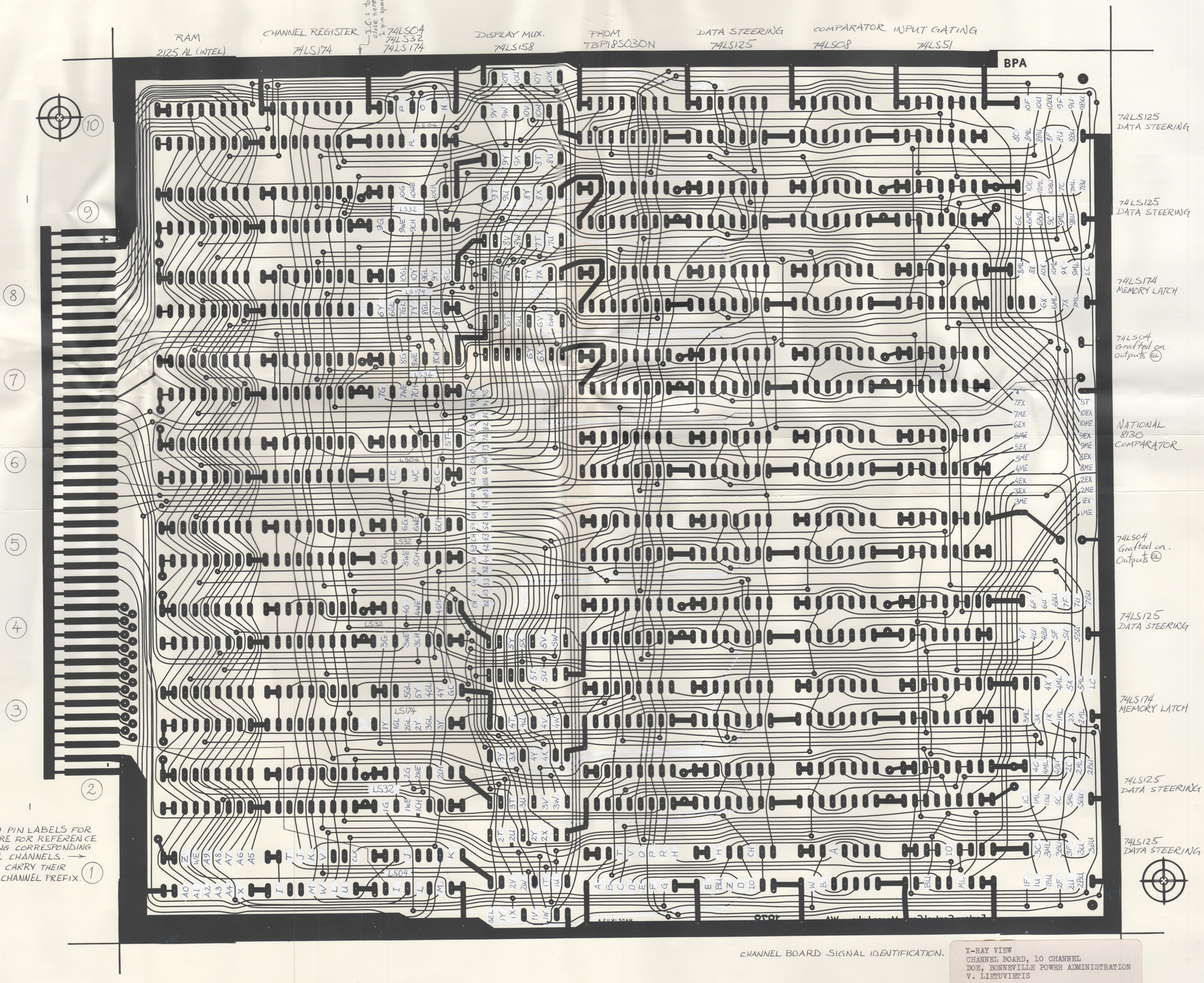
BACK VIEW
LED DISPLAY BOARD, 40 CHANNEL
DOE, BONNEVILLE POWER ADMINISTRATION
V. LIETUVIETIS



TOP VIEW
CHANNEL BOARD, 10 CHANNEL
DOE, BONNEVILLE POWER ADMINISTRATION
V. LIETUVIETIS



BOTTOM VIEW
CHANNEL BOARD, 10 CHANNEL
DOE, BONNEVILLE POWER ADMINISTRATION
V. LIETUVIETIS



UNPREFIXED PIN LABELS FOR CHANNEL 1 ARE FOR REFERENCE IN IDENTIFYING CORRESPONDING PINS FOR ALL CHANNELS. → UNIQUE PINS CARRY THEIR IDENTIFYING CHANNEL PREFIX. (1)

CHANNEL BOARD SIGNAL IDENTIFICATION.

X-RAY VIEW
CHANNEL BOARD, 10 CHANNEL
DOE, BONNEVILLE POWER ADMINISTRATION
V. LIETUVIETIS

— MASTER BOARD —

— CHANNEL BOARD —

10 IDENTICAL CIRCUITS IN PARALLEL (EXCEPT LINE (CH), AS NOTED) THIS SIDE OF - - - - -

MICROCOMPUTER INTERFACE

TRAILING EDGE

LEADING EDGE

POWER-UP PULSE GENERATOR FOR INITIALIZATION

BIT

TRIGGER

ENTER

INPUT

OUTPUT

SEARCH

RECORD

WRITE

COPY

MASTER REGISTER

LED's

PSEUDORANDOM SEQUENCE GENERATOR:

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CHANNEL REGISTER

INPUT

OUTPUT

CHANNEL FUNCTION ROM

BIT

TRIGGER

DISPLAY MULTIPLEXER

BIT/INPUT

TRIGGER/OUTPUT

MEMORY/GLITCH

LED 1

LED 2

LED 3

CHANNEL SELECT

CURSOR LED

MEMORY

GLITCH

MASTER BOARD

CHANNEL BOARD (UP TO 12, MAY BE RUN IN PARALLEL)

63 61 59 57 55 53 51 49 47 (45 42 / 52 45

CHANNEL SELECT CURSOR ← 1 OF 120 LINES

4 - 74154's NOT SHOWN

MEMORY SWEEP

CHANNEL SWEEP

SWEEP RATE CONTROL

NOTE: GROUNDING PLUG IS ATTATCHED TO THESE LINES WHEN MICRO-COMPUTER IS NOT USED

MICROCOMPUTER INTERFACE

CHANNEL ADDRESS (CURSOR CONTROL)

DATA OUTPUT TO MICROCOMPUTER

CHANNEL STATUS DISPLAY SELECT

NOTES:

1) MASTER BOARD: DISCRETE COMPONENT PIN LOCATIONS ARE KEYED TO THE MAST. BD. LAYOUT DRAWING. FRONT PANEL COMPONENTS ARE TERMINATED ON MAST. BD. CONNECTORS EG. 65.13 ⇒ LOC 65, PIN 13. OR ALSO (65) —|13|— ⇒ LOC 65, PIN 13

SHEET 1 OF 2

UNITED STATES DEPARTMENT OF ENERGY

BONNEVILLE POWER ADMINISTRATION

HEADQUARTERS: PORTLAND, OREGON

SCHEMATC DIAGRAM

LOGIC BOARD TESTER, GENERAL PURPOSE, TTL

VILIS I. LIETUVIETIS 9/30/80

MICROCOMPUTER INTERFACE

— MASTER BOARD —

— CHANNEL BOARD —

10 IDENTICAL CIRCUITS IN PARALLEL (EXCEPT LINE (CH), AS NOTED) THIS SIDE OF - - - - -

BIT
TRIGGER
ENTER
INPUT
OUTPUT
SEARCH
RECORD
WRITE
COPY

MASTER REGISTER

LED's

CHANNEL REGISTER
INPUT
OUTPUT

CHANNEL FUNCTION ROM
BIT
TRIGGER

DISPLAY MULTIPLEXER
BIT/INPUT — LED 1
TRIGGER/OUTPUT — LED 2
MEMORY/GLITCH — LED 3
CHANNEL SELECT — CURSOR LED
MEMORY
GLITCH

CHANNEL STATUS DISPLAY SELECT

PSEUDORANDOM SEQUENCE GENERATOR:
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MASTER BOARD
CHANNEL BOARD (UP TO 12, MAY BE RUN IN PARALLEL)
63 61 59 57 55 53 51 49 47 (45 42 / 52 45

TRAILING EDGE (611)
LEADING EDGE (611)
POWER-UP PULSE GENERATOR FOR INITIALIZATION

MEMORY SWEEP
CHANNEL SWEEP
SWEEP RATE CONTROL

CHANNEL SELECT CURSOR ← 1 OF 120 LINES
4 - 74154's NOT SHOWN

NOTE: GROUNDING PLUG IS ATTACHED TO THESE LINES WHEN MICRO-COMPUTER IS NOT USED

MICROCOMPUTER INTERFACE
(MSB) (73.7) PB6 (73.6) PB5 (73.5) PB4 — CHANNEL ADDRESS (CURSOR CONTROL) — (73.4) PB3 (73.3) PB2 (73.2) PB1 (73.1) PB0
(73.10) CB2 PULSE
(71.4) PA2 ENABLE
(71.7) PA6
(71.3) PA2
DATA OUTPUT TO MICROCOMPUTER

NOTES:
1) MASTER BOARD: DISCRETE COMPONENT PIN LOCATIONS ARE KEYED TO THE MAST. BD. LAYOUT DRAWING. FRONT PANEL COMPONENTS ARE TERMINATED ON MAST. BD. CONNECTOR EG. 65.13 ⇒ LOC 65, PIN 13. OR ALSO (65) —13— ⇒ LOC 65, PIN 13

SHEET 1 OF 2

UNITED STATES DEPARTMENT OF ENERGY
BONNEVILLE POWER ADMINISTRATION
HEADQUARTERS: PORTLAND, OREGON

SCHEMATC DIAGRAM
LOGIC BOARD TESTER, GENERAL PURPOSE, TTL

VILIS I. LIETUVIETIS 9/30/80

SIGNAL GENERATOR ON/OFF 1.27

FREQUENCY SELECTOR

EXTERNAL CLOCK SOURCE

DELAY SET/COUNT SWITCH

DELAY COUNTER

LOOK FOR COMPARISON OF DATA (SEARCH, RECORD)

LOOK FOR NON-COMPARISON OF DATA (BOARD TEST)

ONE PER CHANNEL BOARD

BACKPLANE FAREND

DELAY SET LED 1.25

MEMORY BOUND LATCHED MULTIPLEXERS

MEMORY COUNTER

LOWER BOUND ADDRESS

UPPER BOUND ADDRESS

MICRO-COMPUTER INTERFACE

PROGRAM BOUNDS SET 1.16

LOAD LOWER BOUND

DIALIGHT HEXADECIMAL LED DISPLAY

UPPER BOUND COMPARATOR

FERRITE BEAD, ONE LOOP OF WIRE. 3 PLACES. POSSIBLY UNNECESSARY.

RAM (1024 X 1)

MEMORY LATCH

74LS125

COMPARATOR

GLITCH CAPTURE LATCH

DATA BIT

MASTER BOARD (UP TO 12 IN PARALLEL)

UNITED STATES DEPARTMENT OF ENERGY

BONNEVILLE POWER ADMINISTRATION

HEADQUARTERS: PORTLAND, OREGON

SCHEMATIC DIAGRAM

LOGIC BOARD TESTER, GENERAL PURPOSE, TTL.

VILIS I. LIETUVIETIS Vilis Lietuvietis 9/30/80

SHEET 2 OF 2

SIGNAL GENERATOR ON/OFF 1.27 1.28

FREQUENCY SELECTOR OCTAL 2' ROTARY 2' SWITCH 2^3 1.32 1.33 1.34

EXTERNAL CLOCK SOURCE

DELAY SET/COUNT SWITCH 1.24 1.26

DELAY SET LED 1.25

LOOK FOR COMPARISON OF DATA (SEARCH, RECORD)

LOOK FOR NON-COMPARISON OF DATA (BOARD TEST)

(~LOC 9) 270

ONE PER CHANNEL BOARD

BACKPLANE FAREND 330

DELAY COUNTER

BCD THUMB WHEEL 10^0 10^1 10^2

RAM (1024 X 1)

MEMORY LATCH

FERRITE BEAD, ONE LOOP OF WIRE, 3 PLACES. POSSIBLY UNNECCESSARY.

~40ns RAM ADDRESS SETTLING DELAY

COMPARE DELAY ~80ns MINIMUM

COMPARE RETURN DELAY ~80ns

MEMORY BOUND LATCHED MULTIPLEXERS

MEMORY COUNTER

MASTER BOARD

CHANNEL BOARD (UP TO 12 IN PARALLEL)

74LS125

COMPARATOR

GLITCH CAPTURE LATCH

DATA BIT

I/O TO TEST BOARD

(MICRO) CB2 73.10

(MICRO) PA4 71.5

(MICRO) PA5 71.6

LOWER BOUND ADDRESS

UPPER BOUND ADDRESS

MICRO-COMPUTER INTERFACE

PROGRAM BOUNDS SET 1.16

LOAD LOWER BOUND

DIALIGHT HEXADECIMAL LED DISPLAY

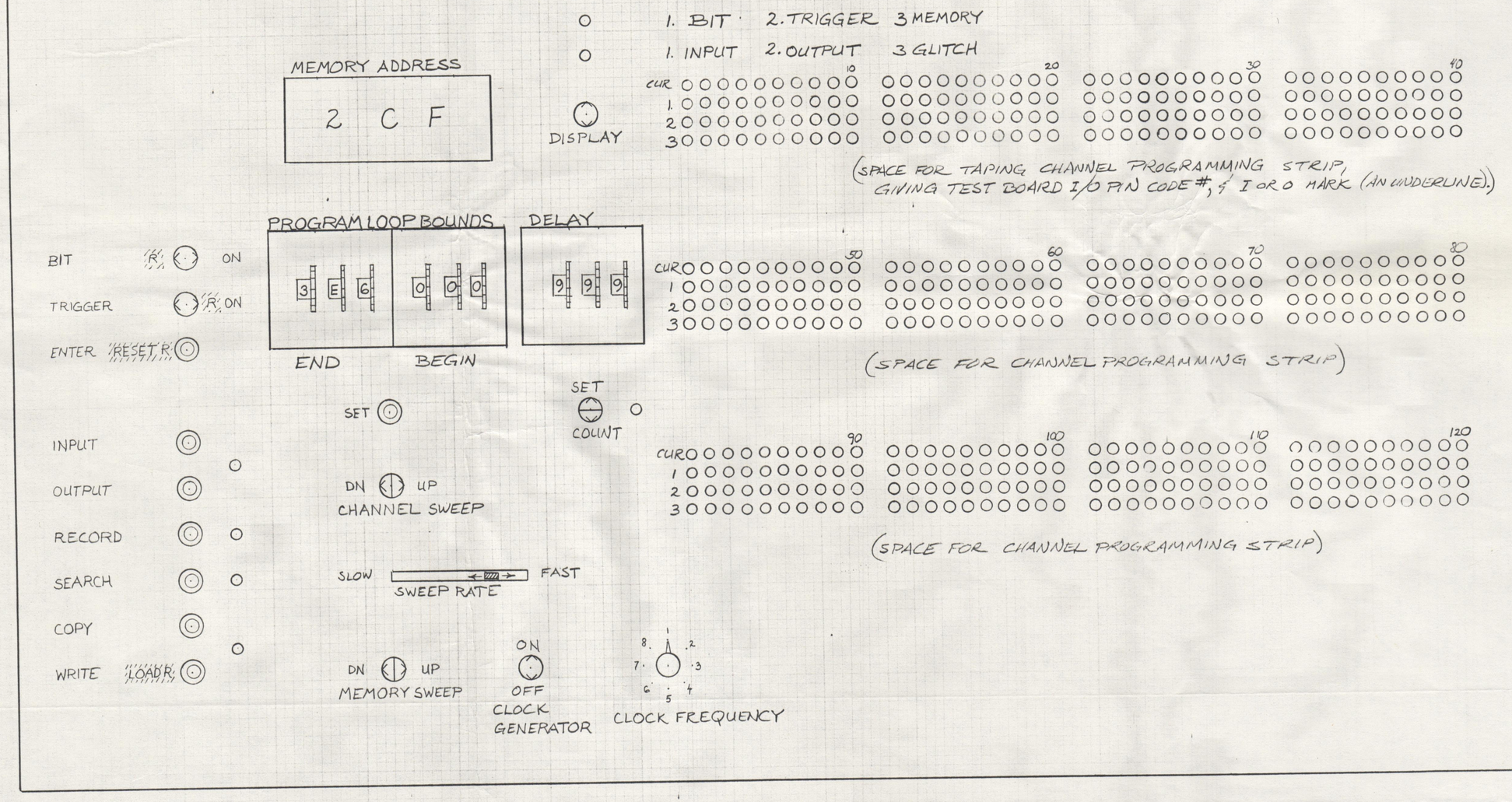
UPPER BOUND COMPARATOR

UNITED STATES DEPARTMENT OF ENERGY
BONNEVILLE POWER ADMINISTRATION
HEADQUARTERS: PORTLAND, OREGON

SCHEMATIC DIAGRAM
LOGIC BOARD TESTER, GENERAL PURPOSE, TTL.

VILIS I. LIETUVIETIS Vilis Lietuvietis 9/30/80

SHEET 2 OF 2



NOTES: 1) THE FOLLOWING SYMBOLS ARE USED ABOVE:

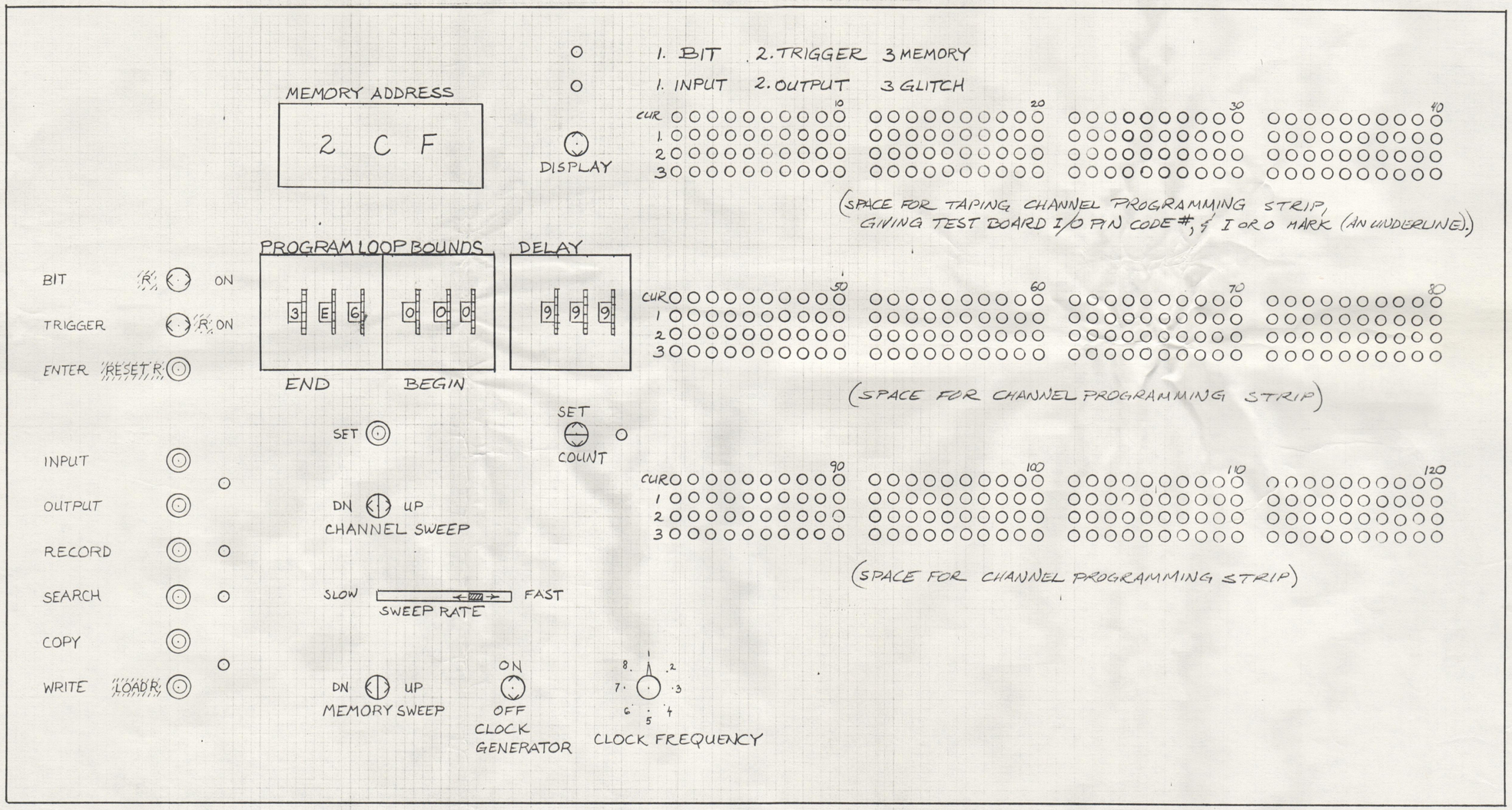
- ○ ↔ DEPICTS AN LED (ALL RED)
- ◎ ↔ DEPICTS A MOMENTARY CONTACT PUSHBUTTON SWITCH
- ⊖ ↔ DEPICTS A SINGLE POLE, DOUBLE THROW SWITCH, ON-ON
- ⊖ ↔ DEPICTS A DOUBLE POLE, DOUBLE THROW SWITCH, ON*-OFF-ON* (* MEANS MOMENTARY CONTACT - SPRING LOADED TO GO OFF)

2) BUTTON & TOGGLE COLORS: ENTER: RED; INPUT & OUTPUT: BLUE; RECORD: WHITE; SEARCH: BLACK; COPY & WRITE: GREEN
PROGRAM LOOP BOUNDS SET: RED; CHANNEL & MEMORY SWEEP: YELLOW.

UNITED STATES DEPARTMENT OF ENERGY
BONNEVILLE POWER ADMINISTRATION
HEADQUARTERS: PORTLAND, OR.

FUNCTIONAL DIAGRAM
CONTROL AND DISPLAY PANEL

10/1/80 Vilis Lietuvietis
V. LIETUVIETIS



NOTES: 1) THE FOLLOWING SYMBOLS ARE USED ABOVE:

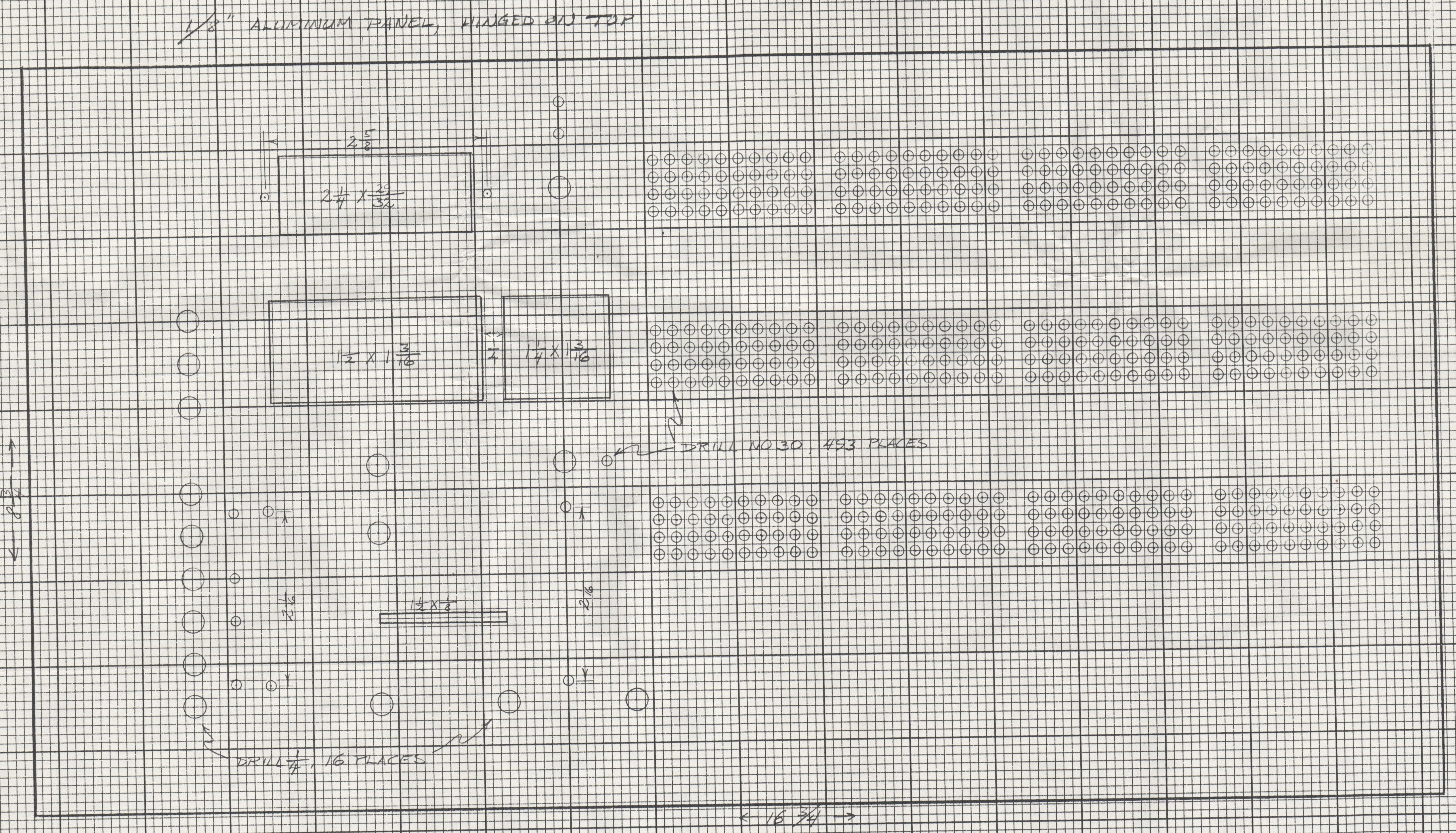
- O ↔ DEPICTS AN LED (ALL RED)
- ◎ ↔ DEPICTS A MOMENTARY CONTACT PUSHBUTTON SWITCH
- ◐ ↔ DEPICTS A SINGLE POLE, DOUBLE THROW SWITCH, ON-ON
- ◫ ↔ DEPICTS A DOUBLE POLE, DOUBLE THROW SWITCH, ON*-OFF-ON* (* MEANS MOMENTARY CONTACT - SPRING LOADED TO GO OFF)

2) BUTTON & TOGGLE COLORS: ENTER: RED; INPUT & OUTPUT: BLUE; RECORD: WHITE; SEARCH: BLACK; COPY & WRITE: GREEN
PROGRAM LOOP BOUNDS SET: RED; CHANNEL & MEMORY SWEEP: YELLOW.

UNITED STATES DEPARTMENT OF ENERGY
BONNEVILLE POWER ADMINISTRATION
HEADQUARTERS: PORTLAND, OR.

FUNCTIONAL DIAGRAM
CONTROL AND DISPLAY PANEL

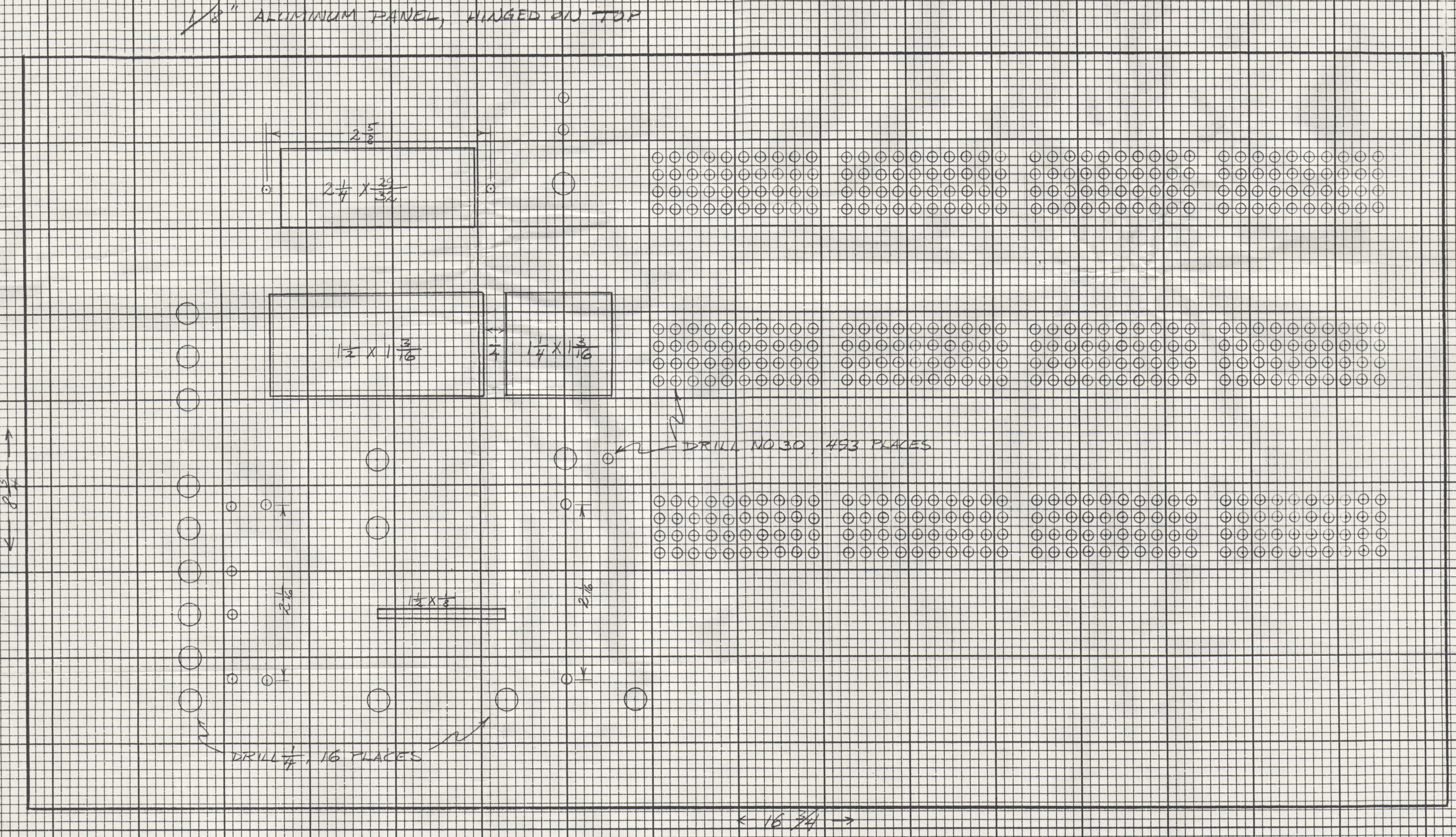
10/1/80 V. LIETOVIETIS



UNITED STATES DEPARTMENT OF ENERGY
BONNEVILLE POWER ADMINISTRATION
HEADQUARTERS : PORTLAND, OR.

DIMENSIONAL LAYOUT
CONTROL AND DISPLAY PANEL
9/15/80

V. LIETUVNIEKIS



UNITED STATES DEPARTMENT OF ENERGY
BONNEVILLE POWER ADMINISTRATION
HEADQUARTERS · PORTLAND, OR.

DIMENSIONAL LAYOUT
CONTROL AND DISPLAY PANEL
9/15/80

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