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BASIC MECHANISMS FOR THE NEW MILLENNIUM¹

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1.0 OVERVIEW

Underlying the response of semiconductor devices to radiation environments are the basic mechanisms for radiation damage in those devices. In order to fully interpret the radiation-induced response of devices, and thus be able to predict their responses in a variety of radiation environments, it is necessary to have a fundamental understanding of those mechanisms. In addition, as technology advances and device structures change, the interactions of the environment with device operation may be different and/or new effects may emerge. This trend has occurred in the past and will certainly continue as we enter into the new millennium.

There are three primary types of radiation effects of concern in the natural space environment.

(1) Total dose effects are those which result from the interaction of ionizing radiation with device materials, generating charge or charged centers which change device properties. These effects depend upon the total ionizing energy absorbed in the material (the total dose).

(2) Displacement damage effects are those which result from the displacement or dislodging of atoms from their normal sites in a crystal lattice or material structure by the interaction of energetic particles. These interactions create defect sites in the material. These effects depend upon the total fluence of particles incident on the material, the particle type, and the energy of the particle, and thus the radiation is described in those terms. (It should be noted that photons can cause displacement damage, but typically do so indirectly through the secondary electrons created by their interaction with materials.)

(3) Single event effects are those which result from the interaction of a single energetic particle passing through a device. Historically these effects have been associated with the high-density charge track created by the particle rather than the displacement damage created by the

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particle (although as will be shown later the displacement damage from a single particle can have measurable effects). The charge created by a particle depends upon the particle type and its energy.

Since the nature of damage created by these three radiation effects differs, the impact on devices varies depending on the device type. Devices that depend upon surface effects for their characteristics, such as MOSFETs (metal-oxide-semiconductor field-effect-transistors), are much more sensitive to total dose effects than displacement damage effects. Devices that depend upon bulk conduction or other material properties, such as BJTs (bipolar junction transistors), are much more sensitive to displacement damage than are MOSFETs. However, depending on the device structure, surface effects can also be an important effect in BJTs and lead to sensitivity to total dose irradiation. Single event effects can create current and voltage transients which markedly affect both surface and bulk devices.

This part of the Short Course will review the basic mechanisms for radiation effects in semiconductor devices. All three areas of radiation damage will be considered – total dose, displacement effects, and single event effects. Each of these areas will be discussed in turn. First an overview and background will be provided on the historical understanding of the damage mechanism. Then there will be a discussion of recent enhancements to the understanding of those mechanisms and an up-to-date picture provided of the current state of knowledge. Next the potential impact of each of these damage mechanisms on devices in emerging technologies and how the mechanisms may be used to understand device performance will be described, with an emphasis on those likely to be of importance in the new millennium. Finally some additional thoughts will be presented on how device scaling expected into the next century may impact radiation hardness.

Due to space limitations, not all mechanisms, devices and effects will be discussed, but rather representative examples of how the basic understanding can be used to elucidate device characteristics will be presented. This should provide some illustrative guidance on how to extend the understanding to devices or properties not covered here. Descriptions of circuit effects will also not be covered in any detail except in a few instances where to do so is useful to further comprehension of a mechanism and its consequences for devices.

Given the wealth of literature covering these topics, it would be unwieldy to try to make reference to it all within these course notes. A representative example of the source literature is cited which should allow the reader to delve into more depth in areas of interest, and to uncover other relevant references. Should any of the many workers in these areas feel that their work has been underrepresented, I apologize; any such oversights are unintentional.

2.0 TOTAL DOSE EFFECTS

In 1962 the Telstar 1 communications satellite failed as a result of the degrading effects of radiation in the Van Allen belts (pumped up as a result of US and Soviet high altitude nuclear tests of the period). Since that time, there has been intensive study into the effects of ionizing

radiation on semiconductor devices, and a wealth of literature now exists in this subject area. This section will only briefly provide an overview of the results described in that literature, and provide sufficient references for the reader interested in further information to access that literature.

2.1 BACKGROUND

Ionizing radiation is radiation that has enough energy to break atomic bonds and create electron-hole pairs (i.e., cause ionization) in the materials of interest. The amount of ionization is related to the total dose absorbed in the material, and is usually given in units of rads. One rad = 100 ergs/gm, and depends upon the material so that the material should be referenced (e.g., rads(Si), rads(GaAs), etc.). In the dose-rate regimes of usual interest in the space environments, the main concern from this energy deposition is the trapping of either or both the electrons and holes created in dielectric materials, and the subsequent alteration of properties of the devices. Since thermally grown silicon dioxide (SiO_2) is the dielectric material of most interest technologically, the discussions here will initially focus on its characteristics. The Metal-Oxide-Semiconductor (Silicon) (MOS) structure will be the subject of most of the discussion.

The fundamental processes occurring in SiO_2 when exposed to ionizing radiation are illustrated in Fig. 2.1. The incident radiation creates electron-hole pairs. The electrons are very mobile and are typically swept out of the oxide rapidly (in times the order of picoseconds [Hugh-73, Hugh-75a]). The holes are much less mobile, and undergo a stochastic trap-hopping process under the influence of the internal electric field. Before the electrons are swept out of the oxide, some of the electrons and holes will recombine. In addition, some small fraction of the electrons may be trapped. Typically a much larger fraction of the holes are trapped, many of them near the Si/ SiO_2 interface. In addition, interactions at the Si/ SiO_2 interface can give rise to interface trap sites, which can easily exchange charge with the silicon. The trapped carriers and interface traps are responsible for the primary changes in device properties caused by ionizing radiation (the total dose effects).

The trapped charges and interface traps are usually characterized by their impact on MOS device properties. In MOS capacitors, a convenient measure is the change in flatband voltage, ΔV_{fb} , caused by the irradiation. In MOS transistors, an important measure is the change in threshold voltage, ΔV_t . In both cases these changes can be separated by various techniques into the change due to charge trapped in the oxide, ΔV_{ot} , and that in interface traps, ΔV_{it} . A description of the various techniques for performing this separation is outside the scope of this work; a review can be found in ref. [Wino-89]. Representative examples of the changes observed in capacitor and transistor characteristics are illustrated in Fig. 2.2.

In dielectrics other than thermally grown SiO_2 , there can be significant hole and/or electron trapping in the bulk of the material (e.g. in SIMOX oxides [Boes-90] and in ZnS/CdS insulators on HgCdTe MIS devices [Mori-90, Mori-92]). Although not discussed in detail here, similar fundamental concepts apply and can be used to understand device response (as described in Section 2.3.5).

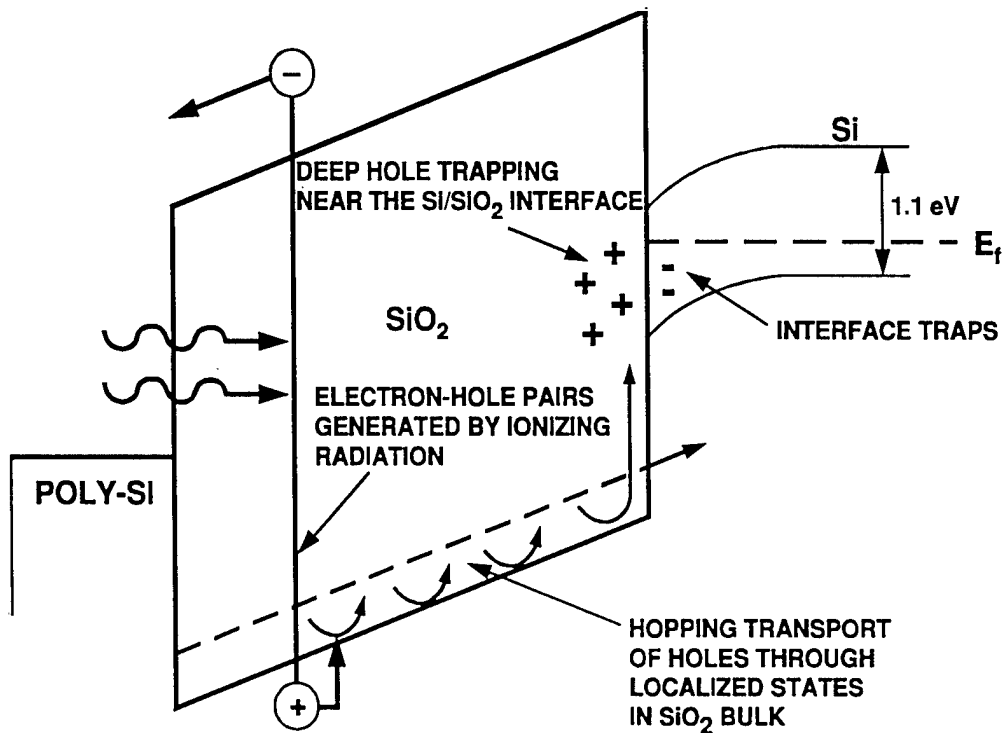


Figure 2.1. Band diagram of MOS structure schematically showing ionizing radiation effects (After [McLe-89]).

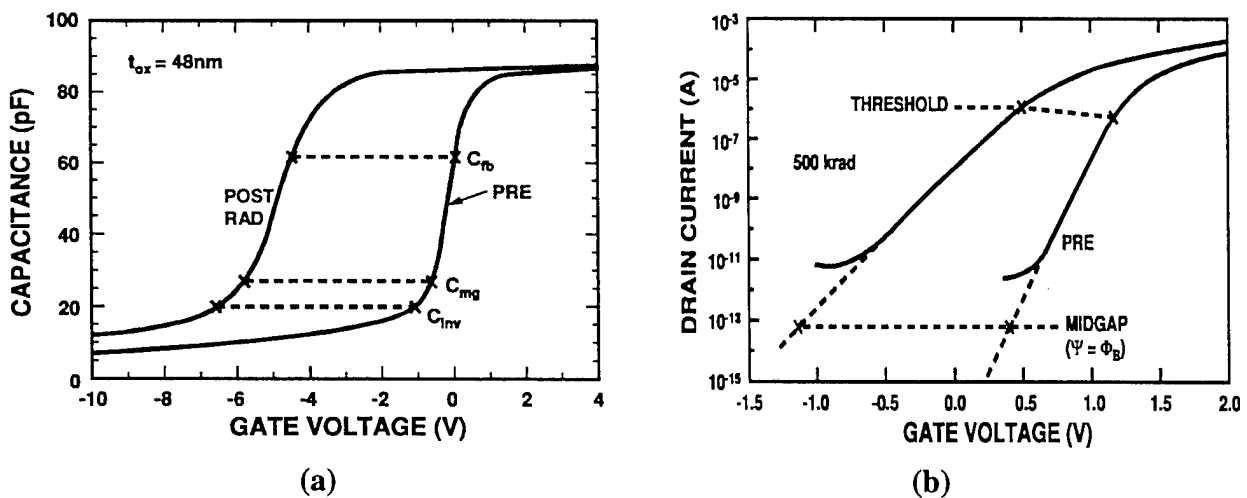


Figure 2.2. Effects of radiation on (a) capacitor C-V curves and (b) transistor I-V curves. Flatband, midgap, and inversion points are shown for the capacitance curve, and threshold and midgap points are shown on the transistor curve.

2.1.1 Charge Generation and Recombination

The total number of electron-hole pairs generated in a material can be determined by dividing the total ionizing energy absorbed in the material by the energy required to create the electron-hole pair. For silicon dioxide, various reports have found that the energy required to create an electron-hole pair is about 18 eV [Curt-74, Srou-74, Ausm-75, Sand-75]; more recent experiments have determined this energy to be 17 ± 1 eV [Bene-86]. Thus one finds that the number of electron-hole pairs generated per unit dose in silicon dioxide is $\sim 8.1 \times 10^{12} \text{ cm}^{-3} \text{ rad}^{-1}$ (SiO_2) [Bene-86].

Charge generation and recombination occur very rapidly, typically within the first picosecond of passage of the ionizing photon or particle. There has been a great deal of research on ionization and recombination in insulators, with two primary models of recombination having been developed. The columnar recombination model applies when the electron-hole pairs are close together, and thus a large number of the carriers may recombine [Lang-03, Brag-06, Jaff-29, Oldh-82]. The geminate recombination model applies when the electron-hole pairs are widely separated, so that a much smaller number of the carriers will recombine [Smol-15, Onsa-34, Onsa-38, Hong-78a, Hong-78b, Hong-78c, Nool-79, Sche-84]. As one might expect, there are a number of practical cases where the electron-hole pair density falls between the extremes treated by these models; several models for this transition region have also been developed [Mozu-66, Brow-81, Dozi-81].

The density of electron-hole pairs is determined by the stopping power or linear energy transfer (LET) of the ionizing radiation. For example, an α -particle with an energy of a few MeV has an LET of $\sim 1 \text{ MeVmg}^{-1} \text{ cm}^2$, and the columnar recombination model will apply. However, for a 1 MeV electron the LET is $\sim 1.6 \times 10^{-3} \text{ MeVmg}^{-1} \text{ cm}^2$, so the geminate recombination model would be expected to apply. The other important factor in determining the net recombination is the electric field in the oxide; the higher the electric field, the more carriers that will escape recombination.

The reason recombination is of interest in understanding device response is that it determines the number of carriers which can subsequently be trapped or interact to create interface traps at the Si/SiO₂ interface. The net fractional yield of carriers can vary widely depending upon the source of the ionizing radiation and the electric field in the oxide, as illustrated in Fig. 2.3. It should be noted that the Co⁶⁰ and x-ray data of Fig. 2.3 have been updated in [Shan-91].

For further information and descriptions of the charge generation process, the reader is directed to reference [McLe-89] and the references therein.

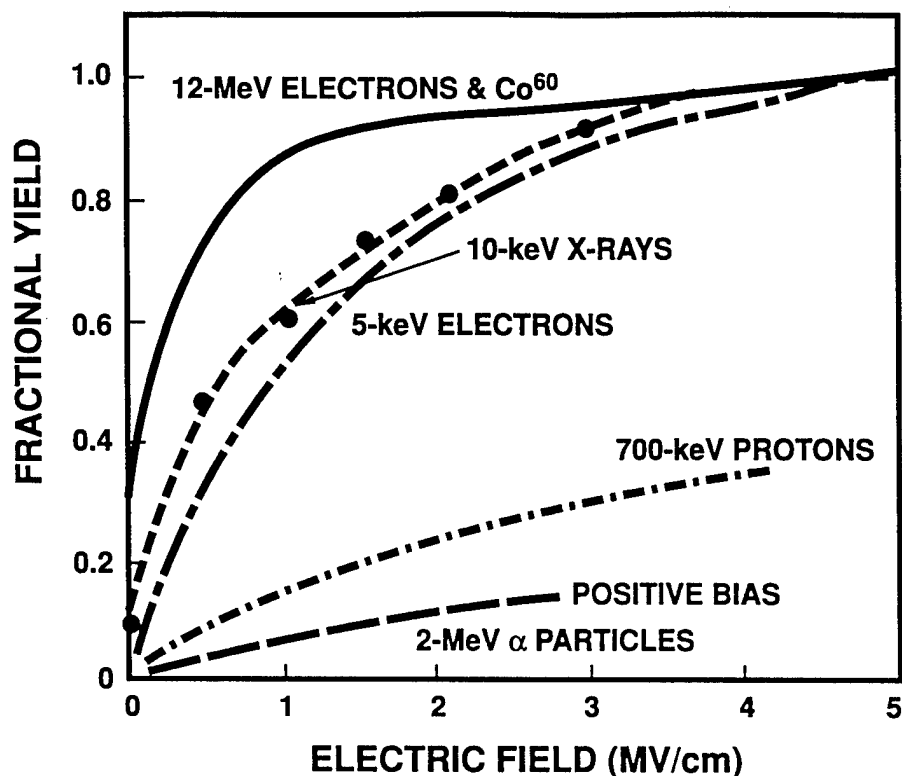


Figure 2.3. Fractional yield of carriers (those escaping recombination) in silicon dioxide as a function of applied field for several different kinds of radiation (After [McLe-89]).

2.1.2 Charge Transport

As mentioned earlier, the electrons in SiO_2 have a high mobility [Hugh-73, Hugh-75b, Hugh-78, Othm-80] and are swept out of the oxide within picoseconds at room temperature. In contrast, the hole transport cannot be described by a simple mobility. Holes show a slow dispersive transport which is temperature- and field-activated and can extend over many decades in time. This characteristic is illustrated in Figs. 2.4 & 2.5. At room temperature, for many oxide thicknesses and fields, the hole transport through the oxide may not be complete until times the order of seconds.

Two models have been proposed to account for this dispersive transport – (1) hopping transport, where the holes directly tunnel between localized trap sites within the SiO_2 bandgap [Boes-75, McLe-76a, McLe-76b, Hugh-75c, Hugh-77]; (2) multiple trapping, where the holes are trapped at localized traps but move via normal conduction in the valence band between trapping events [Srou-76, Curt-77, Silv-77, Scha-80]. Both of these models can be mathematically described by the Continuous-Time Random Walk (CTRW) model [Nool-77, Schm-77, Pfis-78]. This model can predict the universality observed in hole transport response with temperature and field which has been observed experimentally, as illustrated in Figs. 2.6 & 2.7. Certain details of the temperature dependence of the hole transport have been used to demonstrate that the microscopic

mechanism is trap hopping via small polarons, rather than the multiple trapping model [McLe-89].

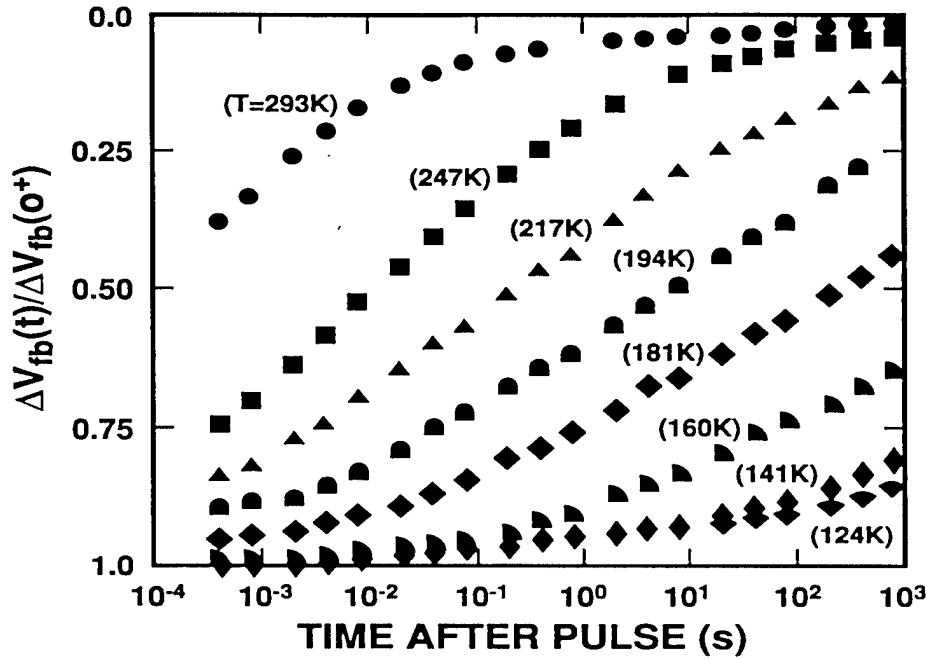


Figure 2.4. Recovery of flatband voltage (proportional to the fraction of holes transported through the oxide) after pulsed electron irradiation of an MOS capacitor under 1 MV/cm electric field for a series of temperatures (After [Boes-78]).

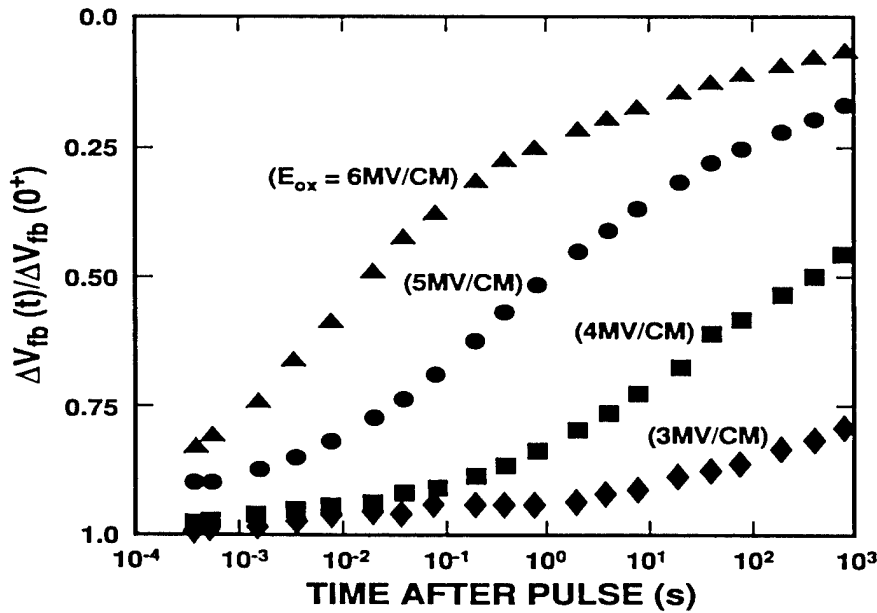


Figure 2.5. Recovery of normalized flatband voltage (proportional to the fraction of holes transported through the oxide) after pulsed electron irradiation of an MOS capacitor at 79 K for a series of oxide fields (After [McLe-78]).

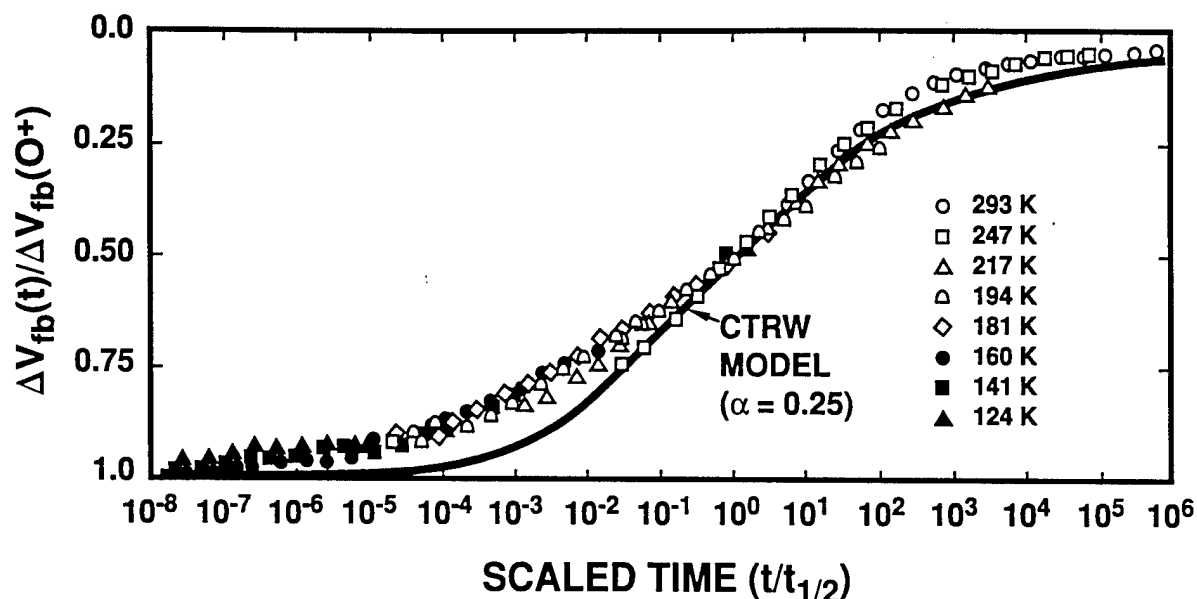


Figure 2.6. Recovery of normalized flatband voltage as a function of time (scaled to the time at which half of the initial shift is recovered) for a series of temperatures. The solid line depicts the calculated results from the Continuous-Time Random Walk model (After [McLe-89]).

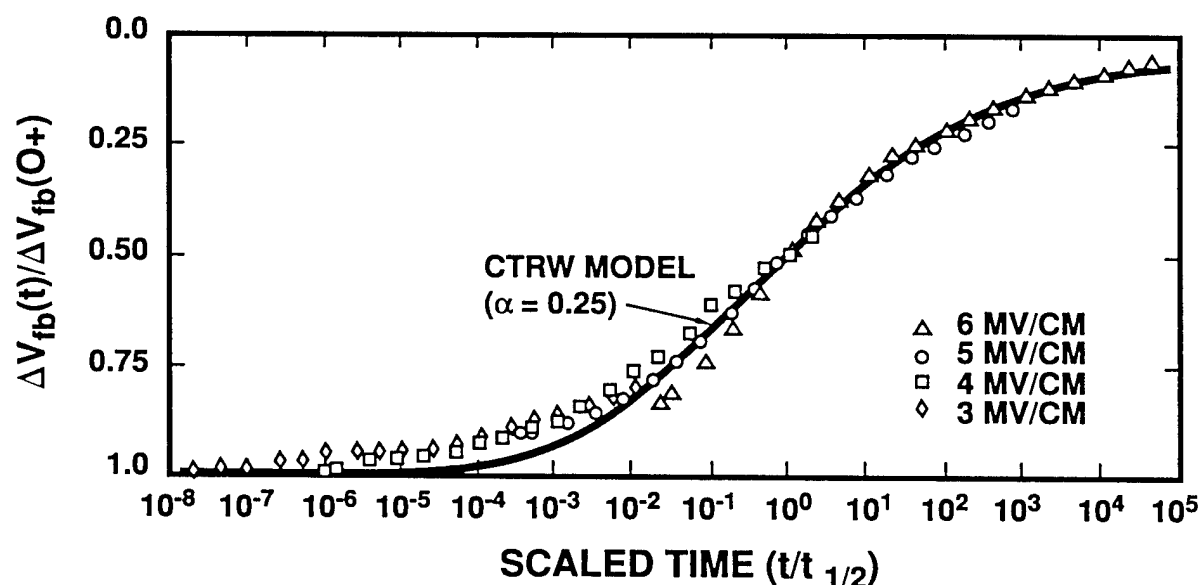


Fig 2.7. Recovery of normalized flatband voltage at 79 K as a function of time (scaled to the time at which half of the initial shift is recovered) for a series of oxide fields. The solid line depicts the calculated results from the Continuous-Time Random Walk model (After [McLe-89]).

It should be noted that there is evidence for a prompt hole transport occurring in short times ($<10^{-7}$ sec) before the slow, dispersive transport discussed above [Boes-76, Hugh-77, Srou-77]. This appears to be associated with an "intrinsic" polaron transport, rather than the above trap-associated polaron transport [Hugh-77]. This response could be of importance for

thin oxides ($d < \sim 15\text{nm}$, typical of commercial gate oxides), where most of the hole transport could be complete within this time. In addition, tunneling of holes out of the oxide could become important in this thickness regime (as discussed later in Section 2.1.3.1)

2.1.3 Positive Charge

2.1.3.1 Characteristics

The number of deep hole traps in the bulk of a thermally grown silicon dioxide layer is usually fairly small. Most of the hole traps reside near the Si/SiO₂ interface or near the gate electrode/SiO₂ interface [Gro-66, Zain-66, Mitc-67, Powe-71, Mitc-73, Derb-75, Aitk-76]. Thus the holes generated by ionizing radiation in the bulk of an oxide layer will be swept towards the Si/SiO₂ interface under a positive gate bias. There some fraction of the holes will be trapped, depending on the hole trap density and the capture cross-section for holes. These trapped holes give rise to a threshold voltage shift, ΔV_{ot} , given by

$$\Delta V_{ot} = -(q/\epsilon_{ox}) t_{ox} \Delta N_{ot} \quad (2.1)$$

where q = charge on the electron

ϵ_{ox} = dielectric constant of SiO₂

t_{ox} = thickness of the oxide

ΔN_{ot} = areal trapped charge density referred to the Si/SiO₂ interface

In this first order picture the primary concern from a device perspective is for the condition when positive bias is applied to the gate electrode. Under negative bias there can be appreciable hole trapping at the gate/SiO₂ interface, but the impact on device threshold voltage is very small (since the term t_{ox} in eqn. (2.1) becomes ~ 0).

The number of holes driven towards the Si/SiO₂ interface depends upon the direction and magnitude of the electric field in the oxide. The efficiency of hole trapping is also dependent on the field, and has been shown to have an approximate $E^{-1/2}$ dependence [Dozi-80, Tzou-83, Boes-85, Kran-87, Shan-90]. The phenomena for hole transport and trapping are illustrated schematically in Fig. 2.8. It should be noted that there can also be an appreciable trapping of electrons in some types of oxides.

Trapped holes can be removed (or neutralized by compensating electron trapping) either by thermal annealing or by tunneling of electrons from the silicon substrate. "Complete" thermal annealing often takes temperatures of up to 300°C or so [Zain-66, Danc-68, Danc-82, Shan-83, Shan-84, Shan-85, Shan-87, , McWh-90, Flee-91, Flee-92b, Shan-92a]. Thermally stimulated current² (TSC) measurements have shown a distribution of energies for the trapped holes [Shan-83, Shan-84, Shan-85, Shan-87, Flee-91, Shan-92a], as illustrated in Fig. 2.9. It should be noted that this distribution has been shown to be very similar for oxides fabricated by a wide variety of

² Thermally stimulated current measurements are made by applying a bias to the device and recording the current as the sample temperature is raised. The net current (after correcting for carrier injection and displacement current effects) is due to the thermal depopulation of charged traps.

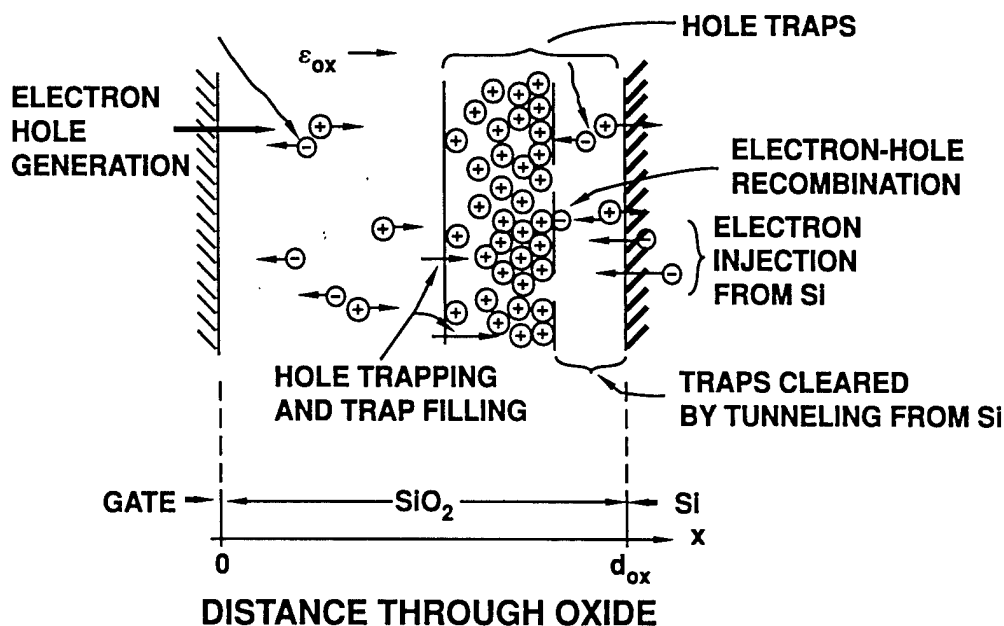


Figure 2.8. Oxide hole trapping and removal processes in an MOS structure under positive gate bias (After [Boes-86]).

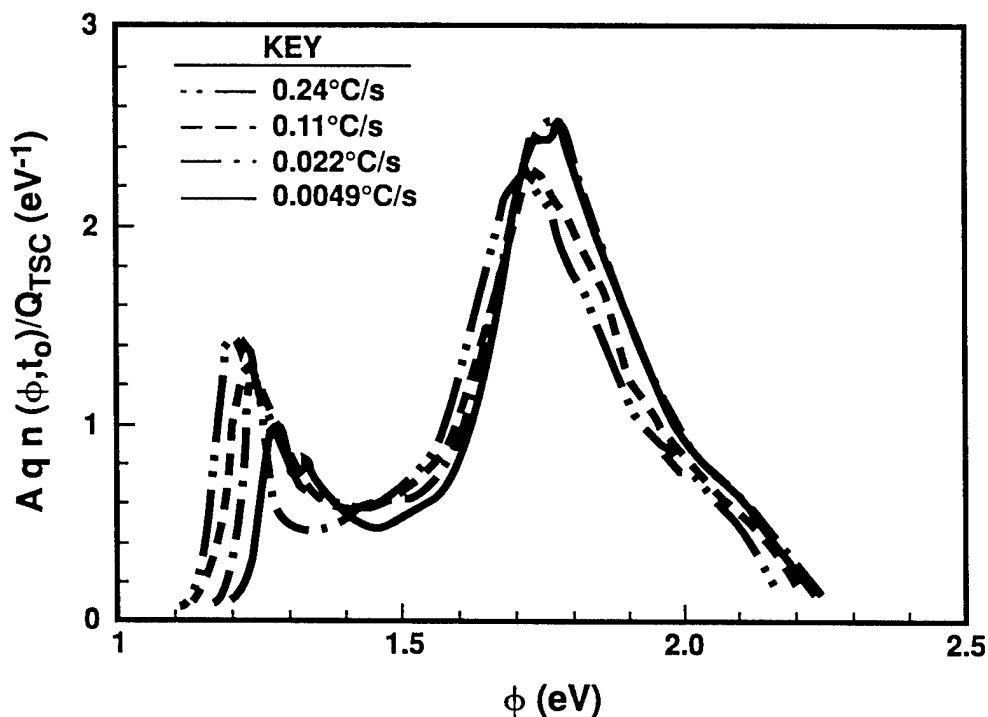


Figure 2.9. Energy distributions of trapped holes in an MOS capacitor inferred from TSC measurements at a series of heating rates (After [Flee-92b]).

processes, as illustrated in Fig. 2.10. Thus, these hole trap levels seem to be fairly universal in thermally grown SiO₂, and one would expect similar thermal annealing characteristics in many

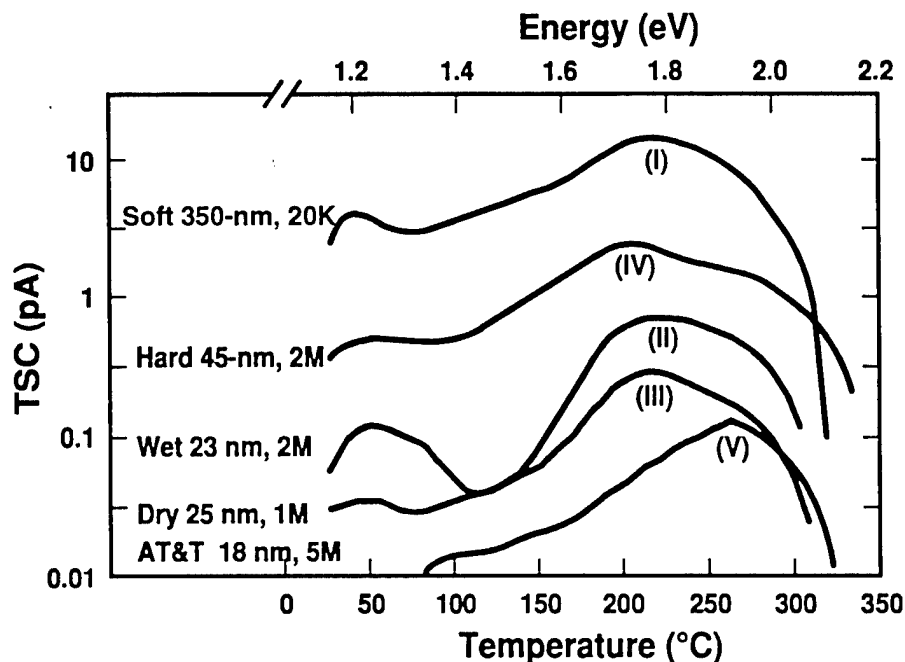


Figure 2.10. Energy distributions of trapped holes in an MOS capacitor inferred from TSC measurements for oxides fabricated by different processes and irradiated to different total dose levels (After [Flee-92b]).

devices. It is also of interest that the peak density of the trapped holes has been observed to move to lower energy as the radiation dose is increased. This suggests that the holes trapped at the higher irradiation doses occupy shallower trap levels on average than the holes initially trapped at the lower dose levels; this would then imply a faster initial thermal annealing rate for devices after high dose irradiation than lower dose irradiations [Flee-92b].

The so-called “tunnel anneal” process (whereby holes are neutralized or compensated by electrons tunneling from the silicon substrate or gate) can explain the roughly linear with $\log(t)$ dependence often observed for the removal of trapped holes at moderate temperatures [Derb-77, Wino-81, Manz-83, Wino-83, Schw-84, Oldh-86], as illustrated in Fig. 2.11. Because of the rapid decrease in tunneling probability with distance, this process can only affect those holes trapped within $\sim 4\text{-}5\text{ nm}$ of the substrate or gate electrode. However, this also means that for very thin oxides, ($< \sim 10\text{ nm}$), significant neutralization of the trapped holes could occur via tunneling in a relatively short time period [Saks-84, Bene-85]. Such a phenomenon has been observed in 5.3 nm oxides, where complete neutralization of the holes occurred about 1 second after generation and trapping of the holes, as illustrated in Fig. 2.12.

Given the above observations, trapped holes can be removed (or neutralized) by either of two processes – thermal annealing or tunneling of electrons. The rate of thermal annealing depends upon the energy distribution of the trapped holes. The rate of tunneling depends upon the spatial distribution of the trapped holes. These processes are illustrated in Fig. 2.13.

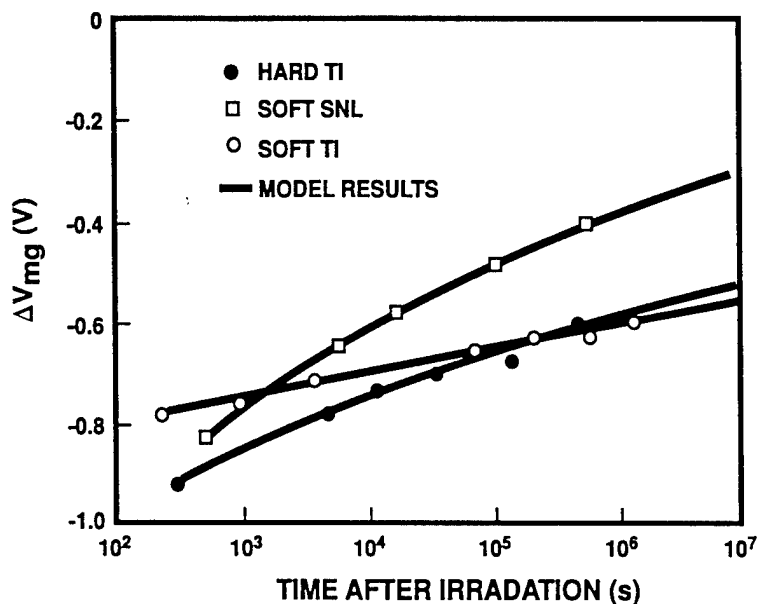


Fig. 2.11. Annealing of midgap voltage shift (approximately equal to net oxide-trapped charge) at room temperature for oxides fabricated by different processes. The solid curves are fits to the data using a model for electrons tunneling from the substrate to neutralize the trapped holes (After [Oldh-86]).

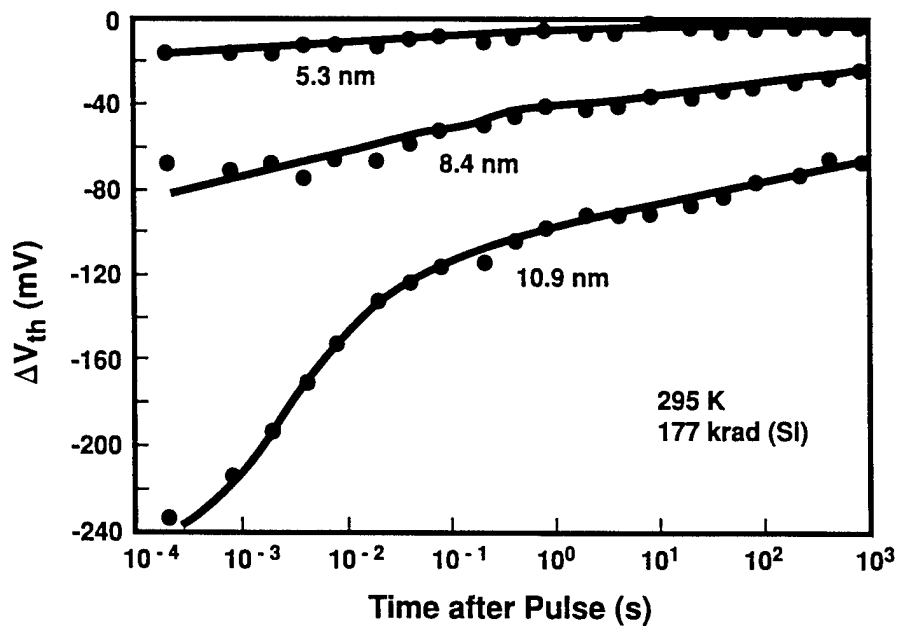


Figure 2.12. Recovery of threshold voltage shift at room temperature after a radiation pulse for thin oxide MOS transistors, showing rapid neutralization of holes by tunneling of electrons from the gate electrode and substrate (After [Bene-85]).

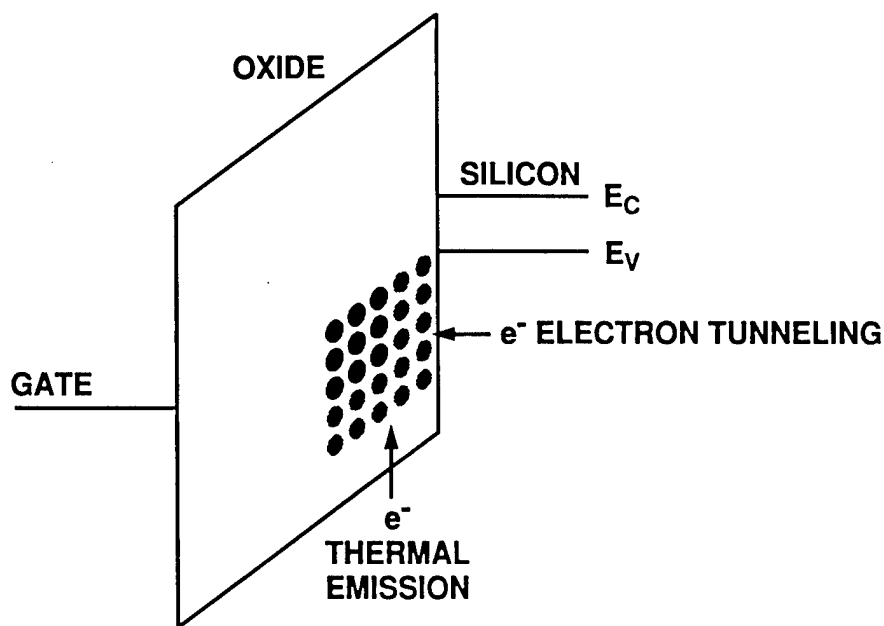


Figure 2.13. Schematic illustration of the thermal emission and electron tunneling processes by which trapped holes can be neutralized in SiO_2 (After [McWh-90]).

2.1.3.2 Microscopic Models

A great deal of work has been done investigating the nature of radiation-induced defects in SiO_2 (see the review in [Gris-82]). X-ray Photoelectron Spectroscopy (XPS) work has shown that the transition from silicon to stoichiometric SiO_2 is very abrupt (within one atomic layer), but that there is a region of 1-4 nm where the silicon-oxygen bonds are strained [Grun-78]. Further work showed that these strained regions were different between oxides which showed a large amount of hole trapping versus oxides with much lower hole trapping; this work also suggested that radiation cleaved a Si-O bond, generating a trivalent silicon defect [Grun-82].

Electron spin resonance (ESR) measurements have shown that ionizing radiation creates E' centers in silicon dioxide [Sige-74, Marq-75, Lena-83b]. The E'_γ center is a trivalent silicon defect associated with an oxygen vacancy [Feig-74], as illustrated in Fig. 2.14. Further work demonstrated a one-to-one correspondence between the radiation-induced buildup of E' centers and oxide-trapped charge, definitively establishing the link between this microscopic defect and trapped holes in typical thermal silicon dioxide [Lena-83b]. However, a lack of correlation between E' centers and oxide-trapped charge has been observed in some oxide structures, such as SIMOX and BESOI oxides [Conl-91, Herv-92, Warr-93]. Despite these studies, it appears that E' centers are primarily responsible for oxide hole trapping in most clean, thermally grown SiO_2 layers.

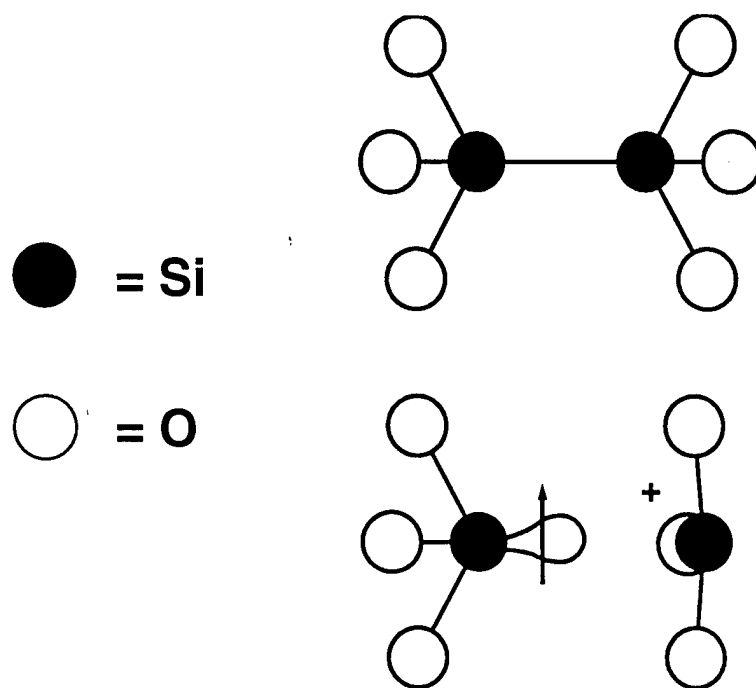


Figure 2.14. Illustration of the E'_γ center, an asymmetrically relaxed oxygen vacancy in SiO_2 (After [Warr-92]).

2.1.4 Interface Traps

2.1.4.1 Characteristics

Interface traps have energy levels within the forbidden band gap at the Si/SiO_2 interface, are located spatially at or very near that interface, and freely exchange charge with the silicon. Their net charge can be either positive, neutral, or negative. They can be further classified as donors (if they are positively charged when above the Fermi level, and neutral when below) or acceptors (if they are neutral when above the Fermi level, and negatively charged when below).

The majority of radiation-induced interface traps are not generated instantaneously directly by the radiation. However, there has been observed in some devices a portion of the total trap density created at the earliest measurement times after a radiation pulse [Boes-75, Boes-82, Boes-84]; this portion is thought to be produced by the direct interaction of the radiation at the interface. There has also been shown an "early" component, which builds up during the time period from milliseconds to seconds after a radiation pulse [Wino-81, Schw-86, Schw-87]. A third component builds up from seconds to very long times following irradiation [Wino-76, Wino-77, Wino-80, Nord-81, Wino-81, Sabn-83, John-86, Schw-86, Wino-86, Schw-87]. An example of the time dependence observed is shown in Fig. 2.15.

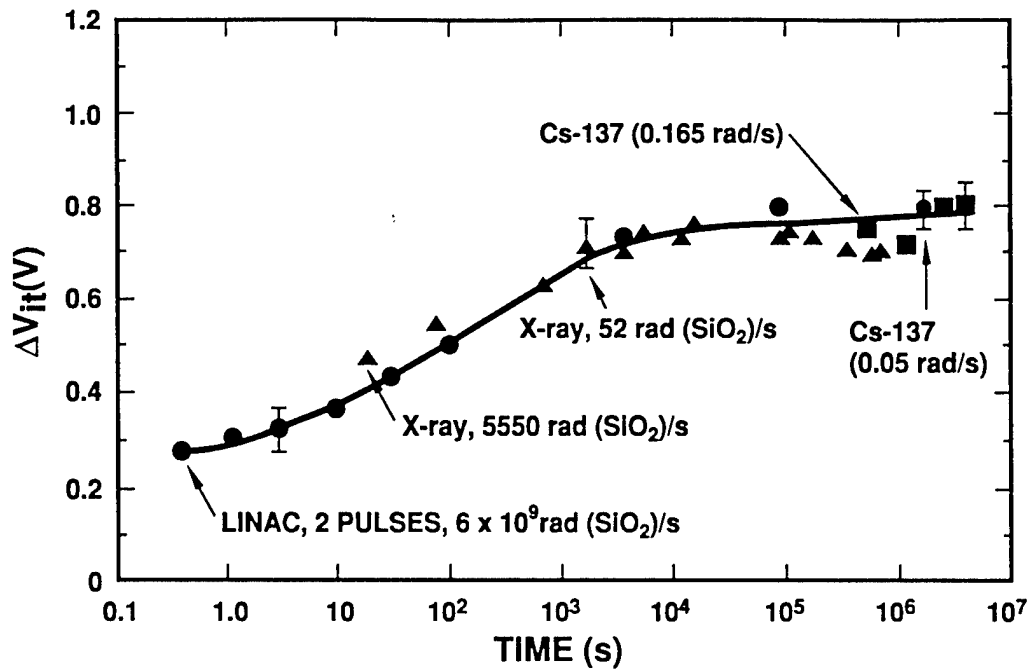


Figure 2.15. Threshold voltage shift due to interface traps as a function of time in NMOS transistors irradiated to 100 krad(SiO₂) at varying dose rates. Interface trap density is the same after a given irradiation or anneal time regardless of the dose rate (After [Flee-88b]).

The buildup of interface traps has often been shown to be sublinear with dose (e.g., depending on $D^{2/3}$) [Wino-77, Wino-80, Peck-82, Naru-83, Dozi-85], although stronger dependencies on up to linear have been observed [Kjar-75, Boes-84, John-84, Dozi-85, Buch-86, Flee-88b]. There has not been shown a true dependence of radiation-induced interface trap density on dose rate for MOS devices under typical operating biases; the apparent increase in interface traps observed at low dose rates is typically the result of the longer times during which the radiation is present and the accompanying long-time buildup of interface traps [Flee-88b]. This phenomenon is shown in Fig. 2.15 where for dose rates ranging from 6×10^9 rad(SiO₂)/sec to 0.05 rad(SiO₂)/sec (a range of over 11 orders of magnitude), the interface trap density at a given irradiation or anneal time is the same. However, in oxides in bipolar devices at low electric field, there has been observed an apparent dose-rate dependence for interface trap buildup. This appears to be caused by space charge effects [Flee-96], as described in Section 2.3.3.

There is also a strong dependence of interface trap buildup on electric field. The buildup is much greater at positive fields, and very small at negative fields [Aubu-71, Peel-72, Wino-76, Wino-77, Bako-78, Saks-80, McLe-80, Dres-81, Naru-83, Wino-85, Saks-86]. Under positive fields, the buildup tends to occur more rapidly at higher fields than at lower fields [Wino-77].

The rate of buildup of interface traps tends to be faster at higher temperatures [Wino-77, Wino-79, Sabn-83, Saks-87], although the final value does not appear to depend strongly on temperature as shown in Fig. 2.16. However, the generation of time-dependent interface traps

appears to be completely inhibited at temperatures below 100K [Hu-80, Wino-80, Saks-83, Saks-84]. Annealing has not generally been observed at typical operating temperatures [Wino-77, Wino-79, Hu-80, Sabn-83, Schw-84, Buch-86, Saks-87], but can occur for temperatures above 100°C [Wino-77, Wino-79, Sabn-83, Schw-84, Buch-86, Flee-87, Flee-88a]. An activation energy of 1.4 eV for annealing has been reported [Sabn-83, Flee-87, Flee-88a].

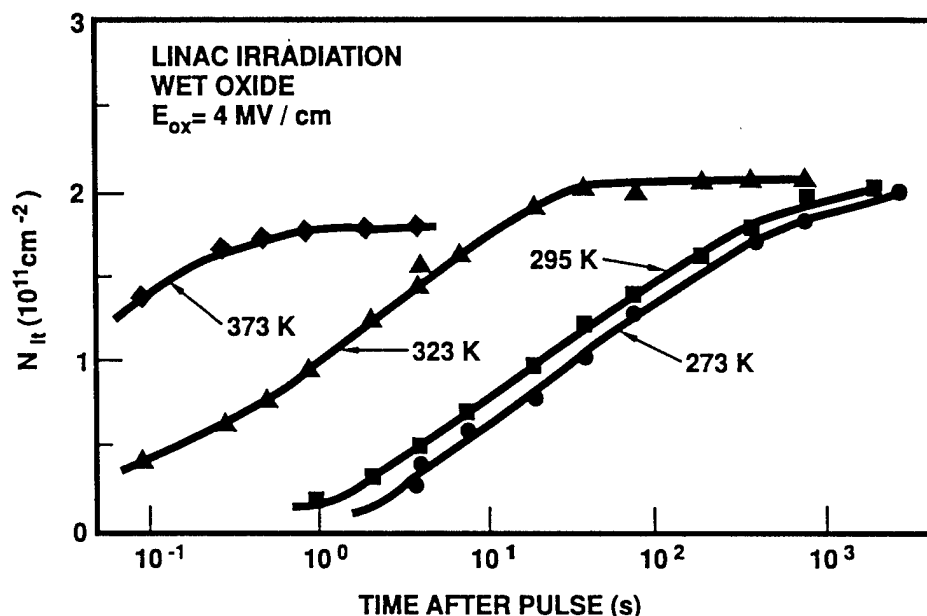


Figure 2.16. Interface trap density for MOS capacitors as a function of time after pulsed electron irradiation at a series of temperatures (After [Wino-77]).

As one might expect, the buildup of radiation-induced interface traps is strongly dependent upon the way in which the oxides were processed. These effects will not be discussed in detail here; only those of particular interest for future technologies will be described. A more complete description is available in references [Dres-89, Wino-89].

Generally the interface trap density generated by a given total dose depends upon the oxide thickness as t_{ox}^n , with values of the exponent varying from 0.5 to 2.0 [Derb-75, Ma-75, Visw-76, Naru-83, Schw-83, Shio-83, Saks-86]. However, for very thin oxides (~ 12 nm), a much more rapid fall-off in interface trap density has been observed [Ma-74; Shar-74, Ma-75, Visw-76, Naru-83, Bene-85, Saks-86] as shown in Fig. 2.17. In oxides of thickness 4-6 nm, no increase in interface trap density was observed for irradiations to 800 krad [Ma-74]. Thus in advanced technologies, radiation-induced interface traps may become less of a concern (for MOS gate oxides; field and screen oxides, which are thicker, are likely to still show such effects). It has also been observed that processes that cause compressive stress on the Si/SiO₂ interface (such as silicided gate electrodes) can reduce the generation of interface traps [Chin-83, Zeke-84a, Zeke-84b, Zeke-84c, Kasa-86].

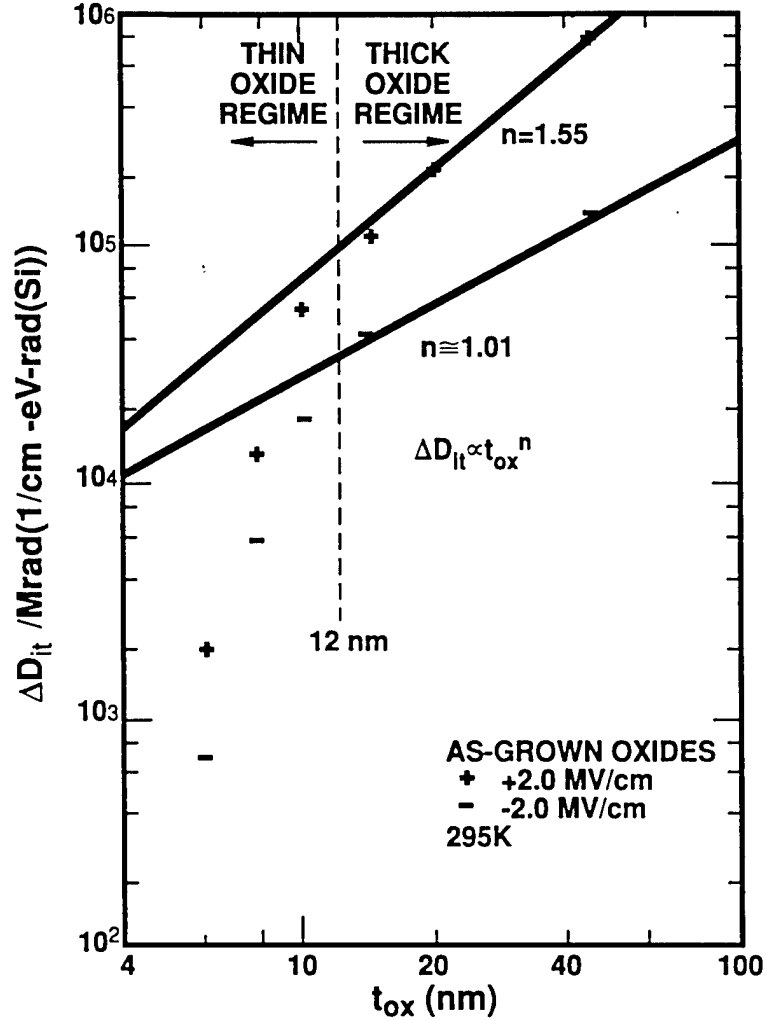


Figure 2.17. Dependence of the rate of interface trap creation by irradiation on oxide thickness in MOS capacitors. Solid lines are fits to this particular thick oxide data (other data in the literature can show a different power-law dependence), points show rapid fall-off for oxides <12 nm (After [Saks-86]).

2.1.4.2 Microscopic Nature

XPS results as described earlier have shown a significant amount of strain at the Si/SiO₂ interface, and in addition have identified intermediate oxidation states which could be converted into defects able to act as interface traps [Grun-77, Grun-79a, Grun-79b, Grun-80, Grun-82]. ESR experiments have shown that the P_b center is generated in MOS structures by ionizing radiation. This center is a trivalent silicon at the Si/SiO₂ interface bonded to three other silicon atoms with a dangling orbital perpendicular to the interface. Other work has shown a one-to-one correspondence between the number of P_b centers created and the number of interface traps created by radiation [Lena-81, Poin-81, Lena-82a, Lena-82b, Lena-83b, Lena-83a, Lena-84, Poin-84, Chan-86]. Illustrations of the P_b defects on (111), (110), and (100) silicon are shown in Fig. 2.18.

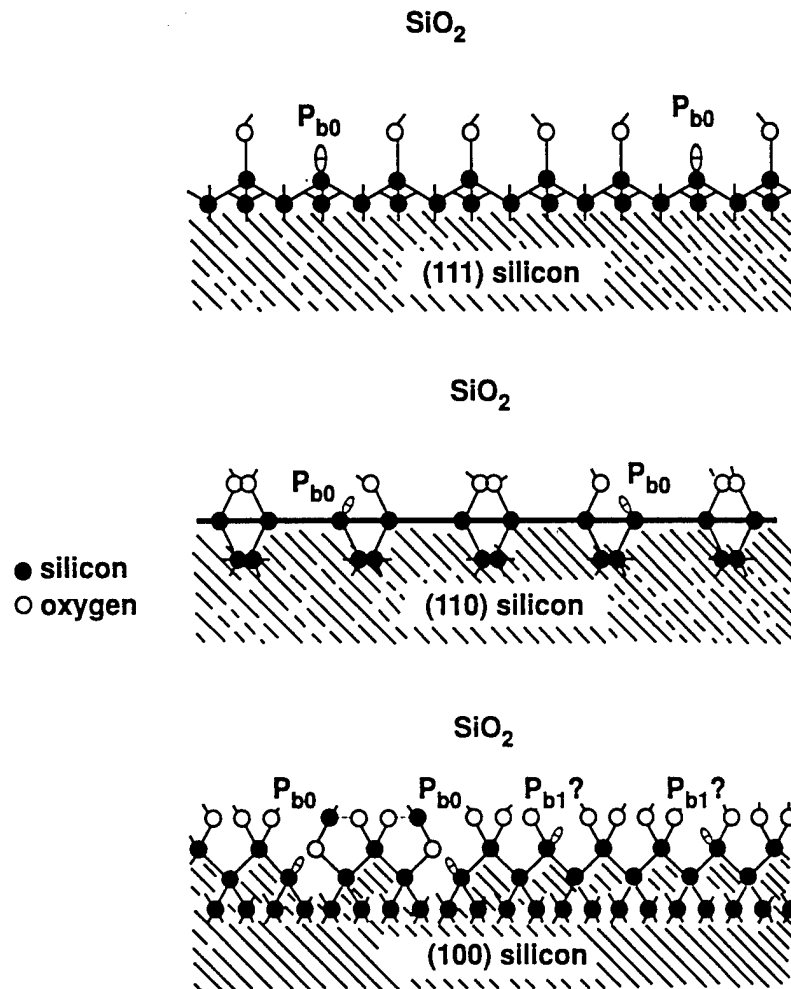


Figure 2.18. Schematic illustration of the Pb interface trap defect on (111), (110), and (100) silicon in MOS structures (After [Poin-81]).

ESR work has also shown that this primary interface trap is amphoteric, and the interface trap levels below midgap are donor-like, whereas those above midgap are acceptor-like [Lena-84, Gera-86]. This observation implies that the post-irradiation voltage shift in a device when the Fermi level is at midgap is primarily due to trapped holes (and/or electrons).

2.1.4.3. Models

There are a variety of models proposed for the creation of radiation-induced interface traps in the Si/SiO₂ system. They tend to fall into three general categories –

(1) hydrogen models, where a trivalent silicon atom at the Si/SiO₂ interface is bonded to a hydrogen atom; this bond is subsequently broken by a process associated with irradiation to leave a “dangling” bond which acts as the interface trap.

(2) injection models, where holes trapped at the interface are converted into interface traps by the injection of electrons.

(3) stress models, where the stress at the interface leads to broken bonds and thus interface traps under irradiation.

Each of these models will be discussed briefly in turn.

A large number of authors have proposed that hydrogen or a water-related species or defect is key to the creation of radiation-induced interface traps [Reve-71, Sah-76, Schl-76, Wino-76, Reve-77, Wino-77, McGa-78, Sven-78, Zieg-78, Wino-79, Peck-80, Wino-80, Brow-85, Gris-85, Schw-86, Schw-87, Shan-92b]. In some cases it was postulated that holes broke Si-H bonds at the interface, creating a dangling bond which was then the interface trap [Sah-83]. Others postulated that the radiation released H^0 in the bulk of the oxide, which dimerized to form H_2 that then diffused through the oxide to the interface where it reacted to form an interface trap [Gris-85]. Probably the most popular of these models is a two-stage mechanism, where radiation-generated holes transport through the oxide bulk where they release weakly bonded H atoms. These then transport to the interface as H^+ (protons), where they interact to create a dangling bond [Wino-76, Wino-77, McGa-78, Sven-78, Wino-79, Wino-80]. Yet another model (the hole-trapping/hydrogen transport (HT)² model) states that holes transport towards the interface where they are trapped, releasing near-interfacial hydrogen which then transports to the interface to create interface traps [Shan-90, Shan-92b]. The (HT)² model can also account for the observed $E^{-1/2}$ field dependence [Shan-92b].

The injection models also typically invoke a two-step process for interface trap formation. In this case the first stage is the trapping of holes at the Si/SiO₂ interface. Electrons (injected from the silicon or transported from the oxide bulk under appropriate bias) then recombine with the trapped holes in a way that causes a structural change at the interface, resulting in a dangling bond which then acts as the interface trap [Lai-81, Lai-83, Sabn-83, Sabn-85, Stan-85, Chan-86]. Other support for this type of model is provided by the observation by a number of workers that the dependence of interface trap build-up on electric field matches that for trapped holes (at least in polysilicon gate devices) [Hu-80, Brow-81, Flee-85, Wino-85, Schw-86, Shan-90].

Stress models are based on the assumption that the stress near the interface and its spatial extent can determine how defects can migrate to the interface. Experimental evidence has shown that stress apparently has a significant impact on the radiation-induced interface traps [Kasa-86, Chin-83, Zeke-84b, Zeke-84c]. XPS data has found strained Si-O bonds in the near interfacial region, and led to the so-called Bond-Strain Gradient (BSG) model [Grun-77, Grun-79a, Grun-79b, Grun-80, Grun-82]. In this model, radiation-generated holes break strained Si-O bonds near the interface. The resulting non-bridging oxygen defects migrate towards the interface under the influence of the strain gradient. Once these defects reach the interface, interface trap sites are created in the form of dangling Si bonds. It should be noted that there is electron spin resonance data which is inconsistent with this BSG model [With-87].

2.2 RECENT ENHANCEMENTS TO UNDERSTANDING

2.2.1. Hydrogen Effects/Model Updates

Work evaluating the time and electric field dependence of radiation-induced interface trap formation provides very strong support for the hydrogen transport model [Brow-91]. A strong dependence of the time for buildup of radiation-induced interface traps on oxide thickness was observed (Fig. 2.19). This would not be expected if a trapped-hole conversion process was predominant, since the rate-limiting step in this model should be independent of oxide thickness. In addition, the time dependence observed was as expected for a dispersive transport of H^+ ions. (However, as often seems to occur in the literature, there are examples counter to this data. For example, interface trap build-up did not show a t_{ox} dependence in [Shan-92b].)

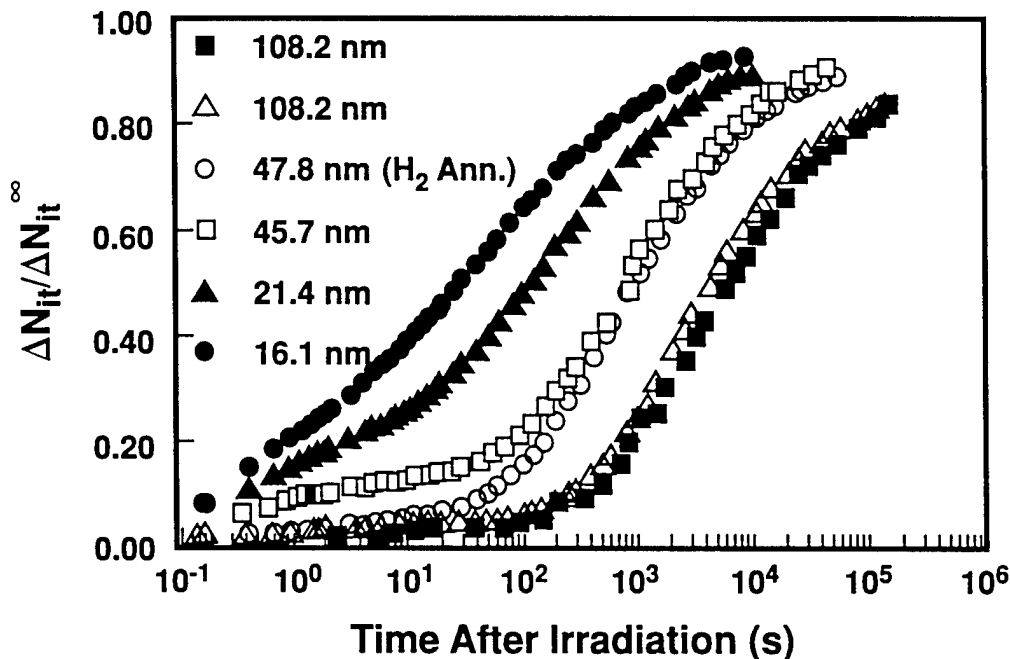


Figure 2.19. Increase in normalized interface trap density as a function of time after an electron irradiation pulse for MOS transistors of varying oxide thicknesses (After [Brow-91]).

That hydrogen plays a role in radiation-induced interface trap formation was unequivocally established by an isotope study in [Saks-92]. Figure 2.20 shows the difference in rates for interface trap buildup for devices annealed in deuterium versus those annealed in hydrogen. The time scale for buildup differs by 2.6 to 4.5 (depending upon gate bias during irradiation and other factors); although this is greater than what one would expect from the standard dispersive transport model for H^+ , a modified model achieved better agreement [Saks-92].

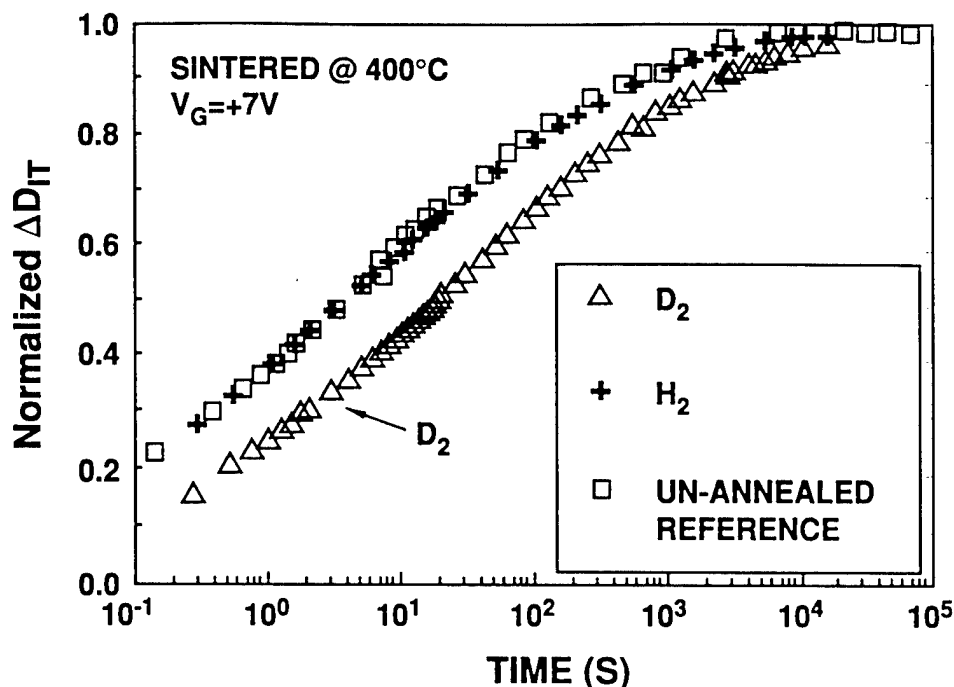


Figure 2.20. Comparison of buildup of normalized interface trap density after pulsed electron irradiation in MOS transistors annealed in deuterium, in hydrogen, or not annealed (After [Saks-92]).

There have been a number of additional experiments trying to more fully elucidate the role which hydrogen plays in the creation of interface traps. These have included studies of the redistribution of hydrogen after electron injection using Secondary Ion Mass Spectroscopy (SIMS) [Gale-83] and Nuclear Reaction Analysis (NRA) [Buch-93]; NRA has also been used to look at hydrogen motion from electron irradiation [Brie-90]. Oxide structures have been exposed to atomic hydrogen to evaluate the formation and passivation of interface defects [DoTh-88, Stah-93b, Stah-94]. Several studies have shown that upon exposing previously irradiated devices to anneals in molecular hydrogen, a simultaneous buildup of interface traps and decrease of trapped positive charge occurs [Kohl-88, Mrst-91a, Mrst-91b, Shan-90, Stah-90, Stah-93a, Stah-93b]. Much of this work [Stah-90, Mrst-91a, Mrst-91b, Stah-93a, Stah-93b] has been interpreted in terms of a model [Gris-83, Gris-84, Gris-85] in which the molecular hydrogen is cracked at a positively charged defect, producing a mobile H^+ and a hydrogen bound in the SiO_2 network. The mobile H^+ then moves toward the Si/SiO₂ interface, where it captures an electron from the silicon, reacts with an interfacial Si—H bond, and forms H₂ and a dangling Si bond (which is the interface trap defect). Molecular orbital calculations have been made to compare potential cracking sites (E' centers versus broken Si—O bonds with a trapped hole), with the calculations suggesting the broken Si—O as the more likely candidate based on the result that interactions between H₂ and E' centers were “unlikely at room temperature” [Stah-93a, Stah-93b]. However, ESR evidence shows clearly that H₂ and E' centers can interact at room temperature [Taka-87, Trip-87, Conl-92, Conl-93b, Conl-95a], casting doubt on these theoretical calculations. Nevertheless, the results of these studies do lend some insight into the process for interface trap

formation under irradiation, and strengthens the support of the hydrogen model (at least in some form).

It should be pointed out that recently evidence has been presented for a latent interface trap buildup in some devices [Schw-92a, Schw-92b, Flee-95c, Flee-97, Jakš-98]. In these instances, after the apparent saturation of buildup of interface traps, there is an additional increase occurring at later times as shown in Figure 2.21. This latent buildup can occur in both high- and low-dose-rate irradiation [Flee-95c]. It appears that this phenomenon is perhaps caused by hydrogen transport which has been retarded by the high density of oxygen vacancies in these devices, but otherwise reacts in the same way as in the "normal" interface trap buildup [Flee-95c, Flee-97, Jakš-98].

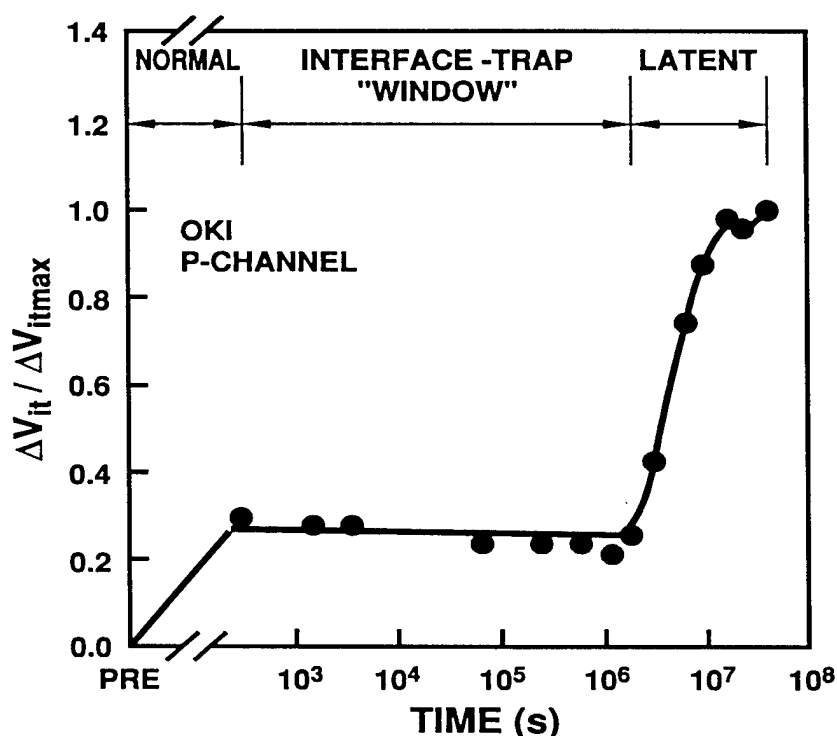
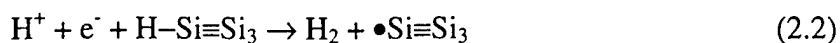


Figure 2.21: Normalized interface trap buildup as a function of time after irradiation in MOS transistors illustrating latent interface trap buildup and an interface trap "window" (where little buildup occurs) (After [Schw-92b]).

Based upon the results to date, it thus appears that the predominant mechanism for radiation-induced interface trap formation in gate oxides depends upon hydrogen. Much of the data supports the two-stage model [McLe-80] of hydrogen transport. (There are a number of experiments on various oxides that have shown dependencies not consistent with this particular mechanism, e.g., those showing a $E^{-1/2}$ field dependence for the buildup, but a large number of experiments tend to support it.) In the first stage, holes transporting through the oxide interact with the oxide structure to release H^+ ions. These then in the second stage undergo field-assisted ionic transport to the Si/SiO₂ interface where they react with Si—H bonds to form H₂ and a dangling bond interface trap. The reaction at the interface is presumed to be



However, it should be noted that there is strong evidence that this is not the only mechanism for interface trap formation. Several studies [Boes-88, Saks-88a] indicate that approximately 10% of the radiation-induced interface traps (primarily the very early time component) could be associated with the hole transport to the interface and subsequent creation of interface traps. In some experiments [Boes-88, Saks-88b], there also appears to be a component of the interface traps which is independent of field polarity, and thus attributed to diffusion of molecular hydrogen [Gris-85, Gris-88]. This component is not always seen, and is smaller than the other two components above.

2.2.2 Border Traps

Unfortunately, the complete picture is even more complicated than implied by the above discussions. In many cases a significant portion of the radiation-induced midgap voltage shift attributed to positive oxide-trapped charge has been shown to not truly “anneal” with time, but rather to be “compensated” in that the net charge can be switched from positive to neutral by changing the applied bias [Schw-84, Dozi-85, Leli-88, Leli-89, McLe-89, Stah-90, Flee-93a, Frei-93]. This phenomenon has been called by a number of different names, including slow states [Sah-66, Nico-82, Uren-89, Buch-90a], anomalous positive charge [Buch-90a, Frei-93], near interfacial oxide traps, switching oxide traps, and border traps [Flee-92a]. An example of the phenomenon observed is shown in Figure 2.22. Here one can see that by changing the applied bias between negative and positive values, the midgap voltage shift (typically assumed to be caused by trapped positive charge), can be made to decrease or increase at will.

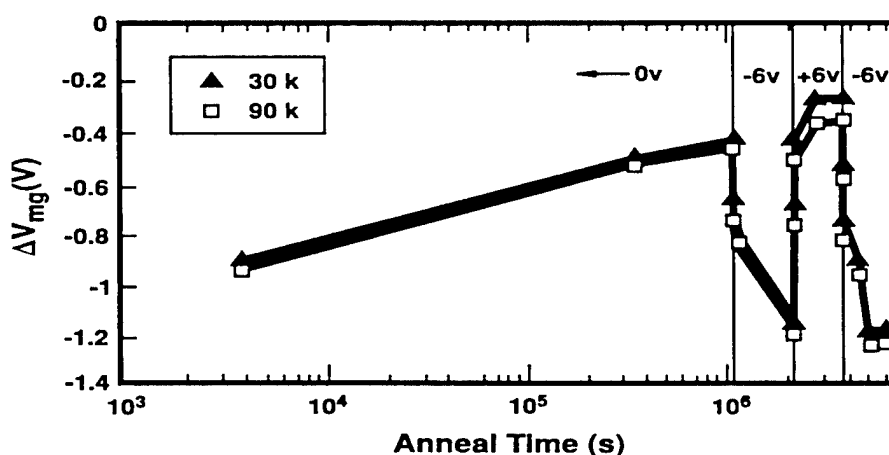


Figure 2.22. Midgap voltage shift in MOS transistors as a function of time after irradiation (to 30 krad(Si) and 90 krad(Si)) showing the reversibility of trapped charge as a function of bias voltage (After [Flee-93]).

The reversibility of charge state has clear implications for device stability and on characteristics such as rebound (where under positive bias after irradiation n-channel threshold

voltages can increase above their preirradiation values). Thus this effect is important to our understanding of devices. The term “switching oxide traps” focuses on the switching properties of the defect. “Border traps” highlights the physical location of the defect (being in the near interfacial region defined as within ~ 3 nm of the interface). “Anomalous positive charge” emphasizes a different structural nature for the trap. One could be tempted to argue that the discussion over the name for the phenomenon is primarily a semantic one. However, the issue really is more fundamental. It concerns whether the nature of the defect responsible for the effect is different from the defects associated with (nonswitching) oxide traps and with interface traps.

The HDL Hole Trap Model [Leli-94], illustrated in Fig. 2.23, is one attempt to explain both switching oxide traps and nonswitching oxide traps with a single defect center. It assumes that holes are trapped at an oxygen deficient site near the interface to form an E' center. Then the positively charged Si atom moves away from the uncharged Si atom and relaxes into a more planar configuration. The final separation distance between the two silicon atoms will depend upon the local bond strains. Then an electron tunneling from the silicon can be trapped on the neutral Si atom, eliminating the unpaired spin (and thus the E' signal). If the Si-Si bond is reformed, then the defect is truly “annealed”, and the charge state will not change with changes in bias. If the bond is not reformed, then the positive charge is merely compensated and a dipole is formed. If the bias is reversed, an electron could tunnel back into the silicon, returning the defect to its positively charged configuration. Thus the defect site is the same for both the switching and nonswitching oxide traps. This model has been used to explain a number of effects, including permanent annealing of trapped holes, switching behavior of trapped holes, compensation effects in thermally stimulated current measurements, trapping and annealing of neutral electron traps, and “apparent” conversion of trapped holes to interface traps [Leli-94].

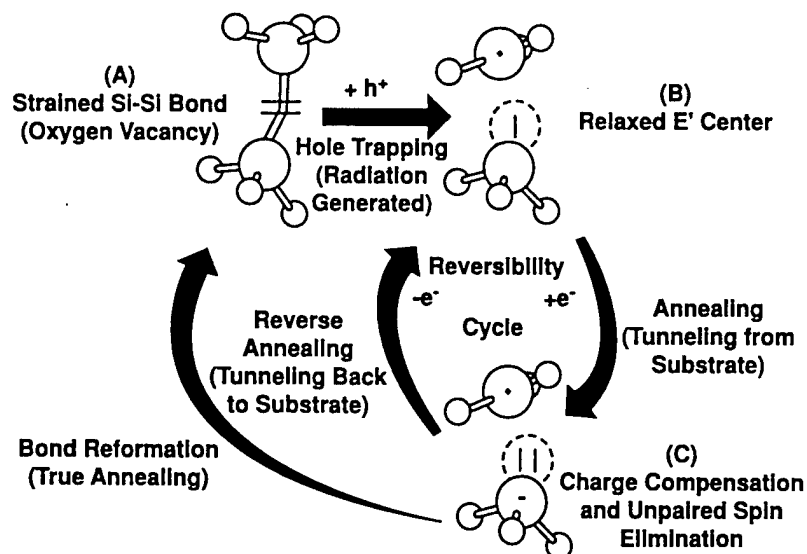


Figure 2.23. Illustration of the HDL hole trap model showing reversible charge compensation and true annealing of a trapped hole (After [Leli-94]).

The border trap nomenclature, focusing more on physical location, explicitly allows for different defects to be responsible for the reversible behavior observed. There have been reports of both "fast" border traps, which switch charge like interface traps but on a slower time scale [Flee-93a, Flee-95b, Flee-95c], and of "slow" border traps, which switch charge state even more slowly and are presumed responsible for the reversible changes observed in ΔV_{ot} . [Youn-79, Schw-84, Leli-88, Trom-88, Leli-89, Trom-91, Flee-93b, Frei-93, Frei-94, Leli-94, Flee-95c]. Direct evidence for the microscopic nature of slow border traps is given in [Warr-94, Conl-95b], where it was shown that the E'_γ center ($O_3=Si: +Si=O_3$, Fig. 2.14) can act not only as a deep hole trap, but also can switch charge states, consistent with the HDL model given above. The "fast" border traps were observed to have a different annealing response from that of the "slow" border traps, suggesting that they may have a different microstructure [Flee-95c]. It was postulated that these "fast" border traps might be in the oxygen-deficient ($O_{3-x}Si_xSi\bullet$) family of defects, some of which are very similar to the P_b centers which have been identified as responsible for the majority of interface traps [Flee-95c]. To date, there have not yet been unambiguous ESR data showing that these defects could in fact be responsible for the "fast" border traps.

Another model postulates two different defects as being responsible for the positively charged defects that can switch charge states and those which can be permanently annealed [Frei-93, Frei-94]. The defect was called "anomalous positive charge" (APC) after earlier work on electron injection [Lai-81, Trom-91, Roh-93]. One concern that has been raised with this nomenclature is that its origin was in avalanche electron injection experiments where extremely large electron fluences (compared to those generated by any practical radiation dose level) were used [Youn-79, Trom-88, Trom-91]. The conditions, samples, and characteristics of those experiments were very different from those used in typical irradiation experiments. However, the real question is whether a single defect, two defects, or (perhaps) multiple defects are involved. In [Frei-93] data was presented to show that the generation of trapped holes was linear with dose, whereas the generation of "APC" was strongly nonlinear (see Fig. 2.24). Data in [Stah-93b] showed that the number of defects which could reversibly exchange charge with the silicon depended upon the amount of hydrogen in the oxide. [Frei-93] argued that since hydrogen is not involved in the E' center complex, a different defect is involved in the charge exchange. However, more recent work has in fact shown interactions which can create E'/H complexes [Conl-93a, Conl-93b, Conl-95a], weakening this argument. Additional experiments in [Frei-94] showed that one type of trapped positive charge could be removed by injection of electrons from the substrate at room temperature, whereas the other ("APC") could not, and in fact was stable up to 160°C. These data, along with the different annealing behaviors observed in [Flee-95c] may in fact indicate rather strongly that more than one type of defect is involved in the oxide trapped charge, switching and non-switching. Overall, it appears that "border traps" may provide the best description for the phenomena observed.

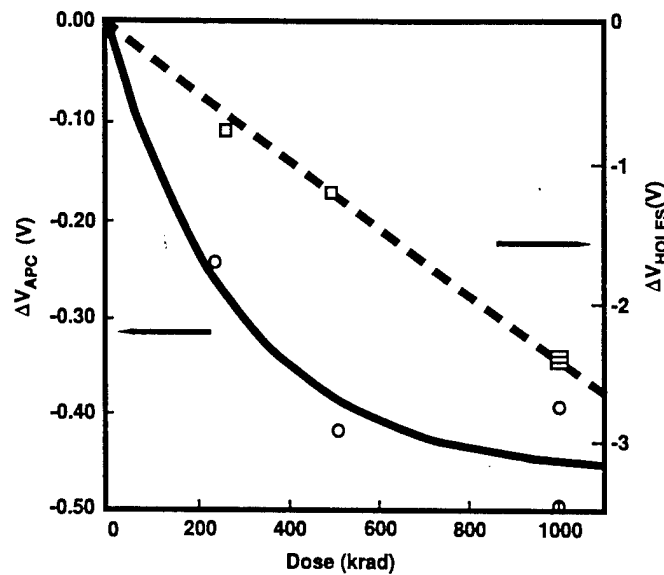


Figure 2.24. Radiation-induced generation of trapped holes and of “APC” (anomalous positive charge) as a function of radiation dose showing different dependencies on dose (After [Frei-93]).

2.3 DEVICE IMPLICATIONS

2.3.1 Microdosimetry Effects

As device feature sizes decrease, the total dose deposited by single energetic ions incident on transistor structures might be expected to cause device failures. This possibility was first raised in 1983 [Oldh-81], and apparently was observed in heavy ion tests conducted in 1991 [Koga-91] and 1992 [Dufo-92]. An example of what might be expected for holes trapped in the gate oxide region of a transistor from the passage of a single high-energy ion (Xe^{129} at 11.3 MeV per nucleon) is shown in Fig. 2.25. This plot is for an ion incident at 45° on a device with 20nm oxide thickness. For a device width or length of $0.5 \mu\text{m}$, the trapped charge region almost covers the entire width or length. If one assumes a device width and length of $0.5 \mu\text{m}$, and that the trapped charge was uniformly distributed over the device area, then the resulting threshold voltage shift would be 90 mV. This is almost equal to the margin available in some high density SRAMs before transistor leakage currents can cause stuck bits [Oldh-93]. Numerical simulations [Gail-94] have also reinforced this view that given the statistical variations in charge deposition and device parameters, total dose from single ions can cause stuck bits in advanced 4T SRAM devices and DRAMs [Duze-94].

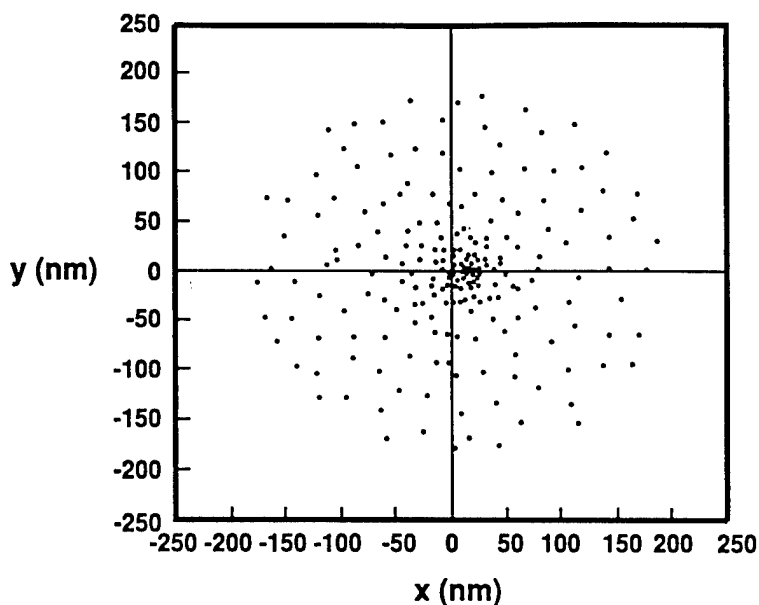


Figure 2.25. Calculated areal distribution of charge trapping at the Si/SiO₂ interface after passage of a single high energy ion at an angle of 45° to an oxide of 20 nm thickness. Each point represents a single trapped hole (After [Oldh-93]).

2.3.2 Thin oxide structures

Although microdosimetry failures have been observed on advanced, small geometry devices, there may be some trends with further scaling that will alleviate some of these problems. As gate oxide thicknesses are reduced below 10 nm, the hole trapping drops rapidly [Ma-74, Shar-74, Naru-83, Saks-84, Bene-85, Saks-86] (Fig. 2.26). Part of this effect is due to the fact that one expects the majority of the hole traps to be able to be neutralized by tunneling from the gate or substrate at thicknesses $< \sim 10$ nm. Another trend which may help radiation hardness of advanced devices is that the buildup of radiation-induced interface traps is also reduced for oxide thicknesses $< \sim 12$ nm [Ma-75, Visw-76, Naru-83, Bene-85, Saks-86], as shown earlier in Fig. 2.17. However, one must be aware of the fact that in many advanced devices dielectric isolation (in the form of field oxides or in trenches) may still be used. These oxide layers will remain relatively thick and thus be susceptible to effects from radiation-induced hole trapping and interface traps. Such effects can lead to device leakage as illustrated in Fig. 2.27.

There is a new radiation phenomenon that has been observed in very thin gate oxides – radiation-induced leakage current (RILC) [Scar-97]. As shown in Fig. 2.28, the background leakage through the gate oxide can increase markedly after irradiation in these thin oxides. This excess current is believed to be caused by trap-assisted tunneling, where the traps are created by the radiation [Saka-97]. This phenomenon may cause functional or parametric problems for circuits sensitive to such leakage currents.

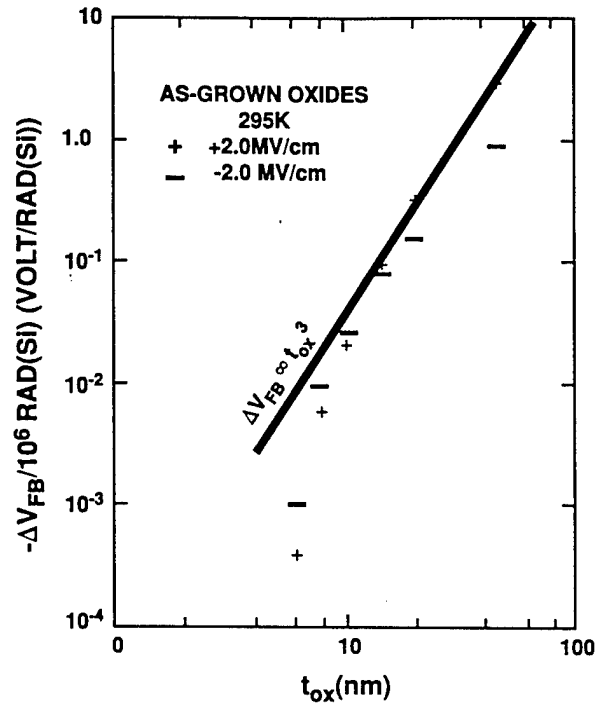


Figure 2.26. Dependence of the rate of flatband voltage shift caused by irradiation on oxide thickness in MOS capacitors. Solid line is a fit to this particular set of thick oxide data (other data in the literature can show different power law dependencies), points show rapid fall-off for oxides <10nm (After [Saks-86]).

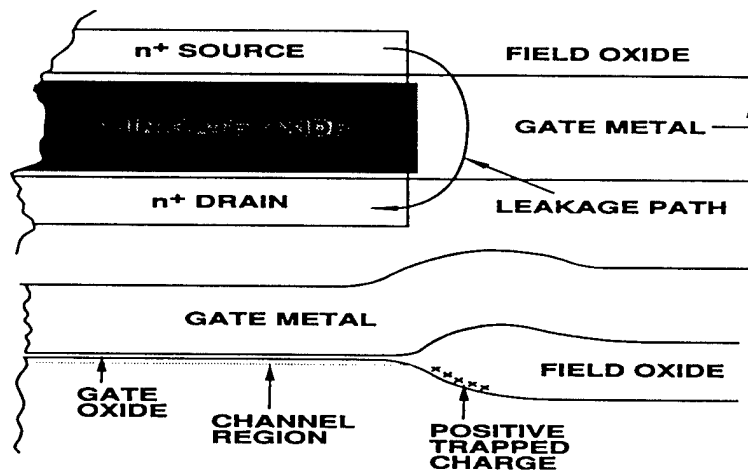


Figure 2.27. Illustration of the possible current leakage path caused by charge buildup in oxide isolation structures in MOS devices (After [Oldh-87]).

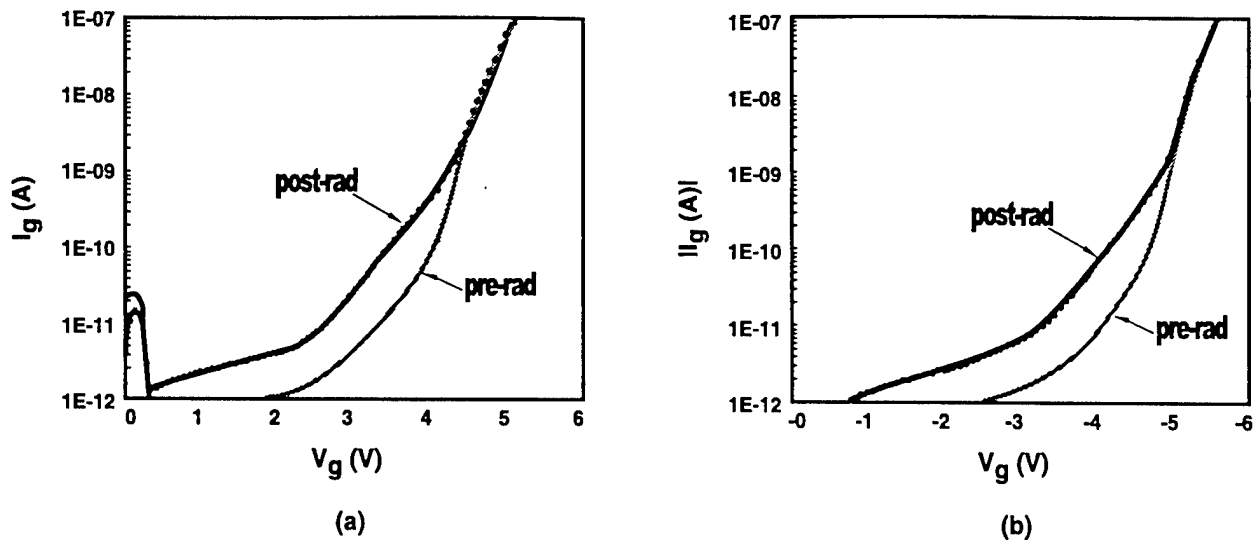


Figure 2.28. Gate leakage current as a function of voltage in MOS capacitors with 4.4 nm oxides before and after irradiation to a dose of 5.3 Mrad(Si). (a) Positive voltage sweep (b) negative voltage sweep. The low voltage peak in (a) is associated with electron tunneling and trapping (After [Scar-97]).

2.3.3 Low-Dose-Rate Bipolar Effects

Although they are not directly involved in the active operation of bipolar devices, oxide layers can play an important role in the performance of bipolar devices in radiation environments. In 1991, and confirmed in later work, it was reported that some types of bipolar devices showed greater gain degradation when irradiated at low dose rates than at higher dose rates [Enlo-91, Nowl-92, Nowl-93, Wei-94]. This effect is illustrated in Fig. 2.29, and is often called ELDRS (Enhanced Low Dose Rate Sensitivity).

The enhanced gain degradation did not appear to be caused by an enhanced interface-trap buildup, but rather by an increase in net positive charge in the oxide covering the emitter/base junction. (The cross-section of a typical bipolar device structure illustrating this oxide region is shown in Fig. 2.30.) It was not merely an effect of the increased time for the irradiation at the lower dose rates. This runs counter to the general experience in MOS devices, where, as discussed above in Section 2.1.3.1, the net positive charge has almost always been observed to decrease with decreasing dose rate due either to trapped-hole compensation or annealing and/or enhanced interface-trap buildup.

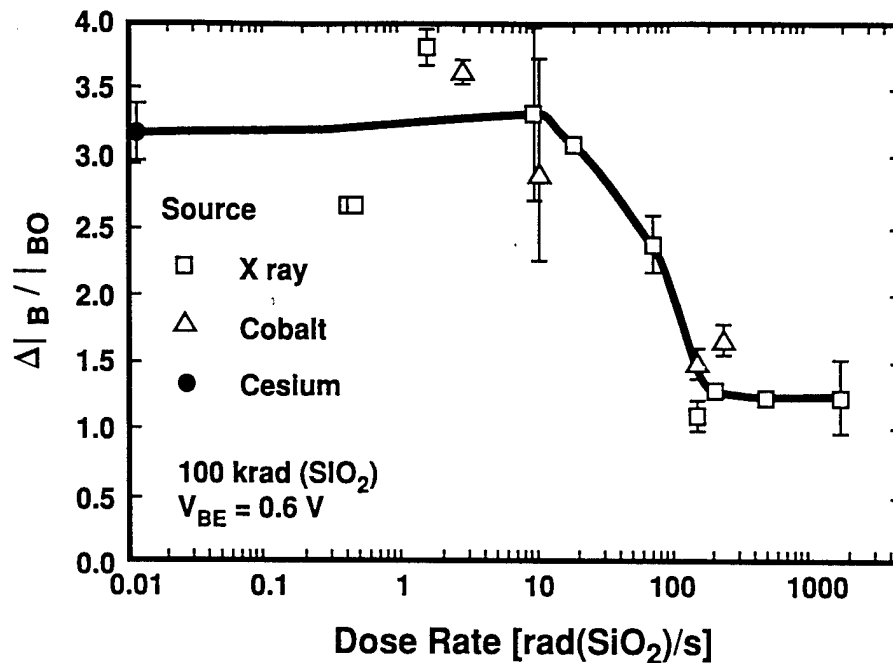


Figure 2.29. Dependence of the excess base current in bipolar transistors (irradiated to 100 krad (SiO₂)) on the irradiation dose rate. Increases in base current cause degradation in the transistor gain (After [Nowl-94]).

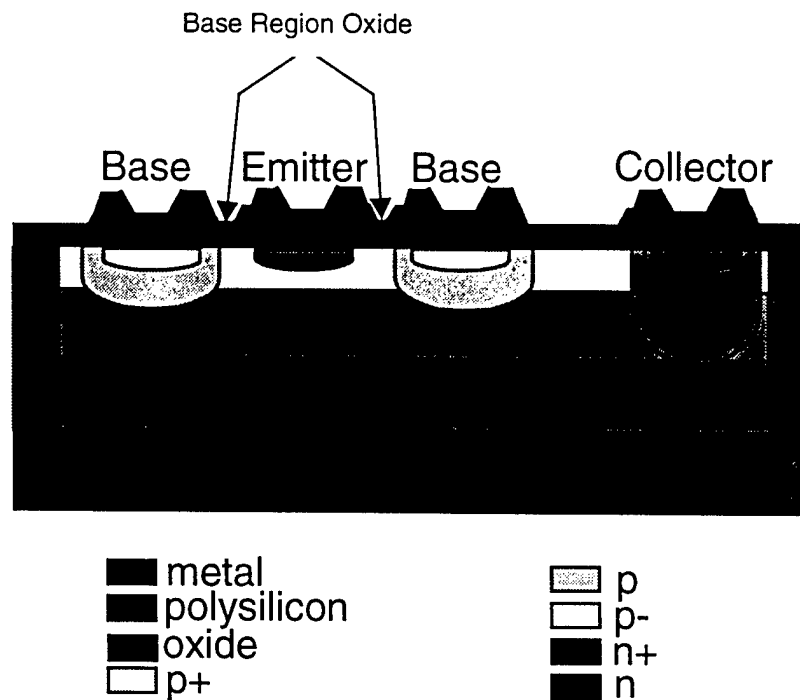


Figure 2.30. Cross-section of a bipolar device structure showing oxide regions where charge buildup can affect device performance. Particularly important is the oxide over the base region.

Several models have been proposed to explain this phenomenon – (1) Delayed buildup of interface traps at the surface of the base [McCl-94, Schm-95]; (2) Enhanced electron-hole recombination caused by electrons in shallow traps in the base oxide [Bely-95]; (3) Retarded hole transport and enhanced charge trapping in thick oxides because of the low electric field [Boes-85, John-95]; (4) Space charge effects in the base oxide associated with metastably trapped or slowly transporting holes [Flee-94a].

Simulations have shown how the increased trapped-hole density can lead to greater recombination in the base region of bipolar devices, leading to the observed gain degradation [Kosi-95].

Experiments looking at capacitors with oxides processed to simulate the oxide over the base/emitter junction (“screen oxide”) in a typical bipolar process have shed some light on the mechanisms for this phenomenon [Flee-94a]. It was found that oxides processed in this way had hole trapping efficiencies approaching 1, and apparently also had a large number of defects in the bulk of the oxide. The model developed indicated that at higher dose rates in these oxides, the hole transport process at low electric fields was slowed by several orders of magnitude by the large number of defects in the oxide. This slow transport coupled with the large amount of trapping at the Si/SiO₂ interface created a space charge that reduced the field in the bulk of the oxide, thereby increasing the recombination rate and thus decreasing the charge yield for holes. The slowly transporting holes also tend to drive the holes trapped near the interface closer to the interface, where they can be more easily compensated by electrons tunneling from the silicon. Both these effects combine to reduce the net positive charge at the interface. At the lower dose rates, the space charge effects are not observed (since the hole generation rate is much less), the charge yield is higher, the trapped holes are somewhat farther from the interface and thus less likely to be compensated. Overall the net positive charge is greater than in the high-dose-rate case.

Later work [Flee-96] expanded this model. It was found here that indeed in some devices enhanced interface trap buildup at low dose rates and low electric fields could play a role. In addition, for these oxides enhanced hole trapping was not observed, but rather the primary effect was a reduction in the number of compensating electrons, either in the bulk of the oxide or at the interface. The primary mechanism was still that of space charge effects in the oxide caused by delayed hole transport. The essence of the model is illustrated in Fig. 2.31.

This model was tested by performing irradiations at slightly elevated temperature (60°C). Since hole transport is thermally activated (see Section 2.1.2 above), by increasing the temperature one might expect the hole transport rate to be enhanced and the dose rate at which space charge effects become important to be increased. This was indeed found to be the case, as shown in Fig. 2.32. Additional experiments have also shown that an enhanced degradation similar to that observed at low dose rates can be obtained by irradiating at elevated temperatures from ~90°C to ~125°C [John-95, Schr-95, John-96c, Peas-96, Witc-96, Peas-97].

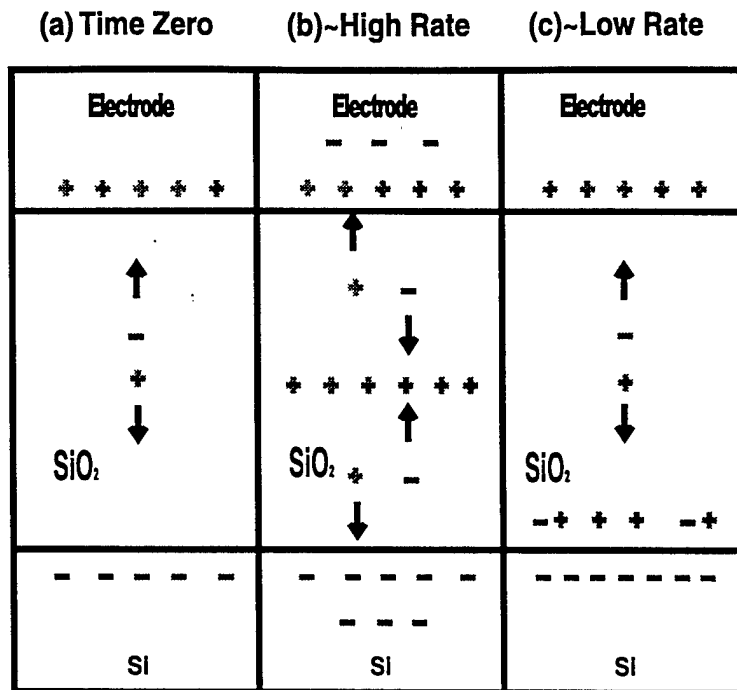


Figure 2.31. Illustration of the model for electron and hole transport responsible for the low-dose-rate effect in bipolar transistors. (a) at the start of irradiation, before significant trapped charge buildup, (b) during high-dose-rate exposure, when holes trapped in metastable traps in the bulk of the oxide cause space charge effects, (c) during low-dose-rate exposure, when some holes in metastable traps are emitted, space charge effects are minimized, and some holes transport to the Si/SiO₂ interface (After [Flee-96]).

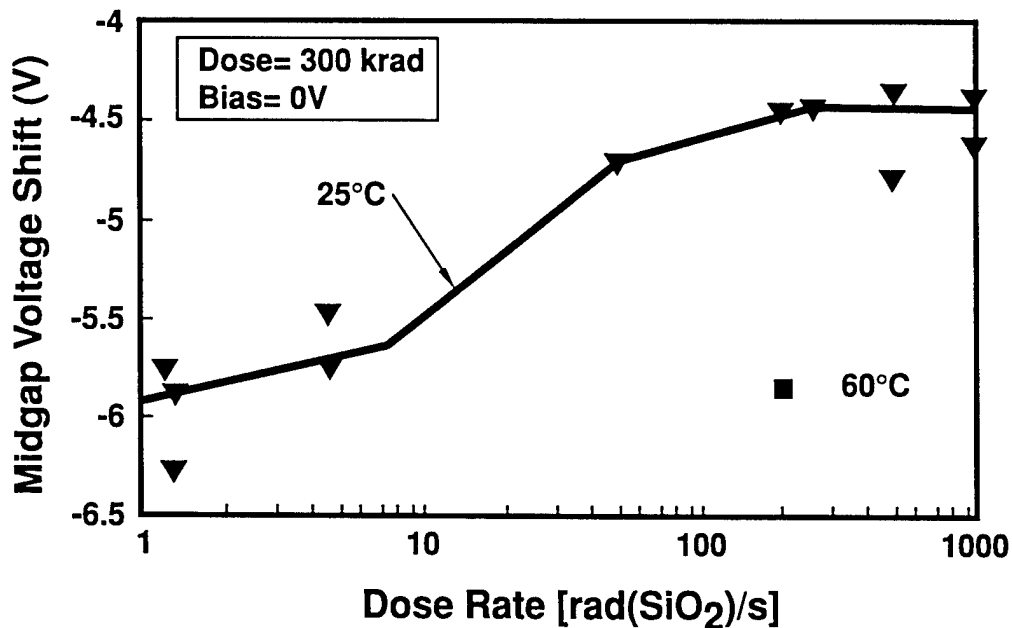


Figure 2.32. Comparison of midgap voltage shifts for irradiation at 25°C (triangles) and 60°C (square) of capacitors with a bipolar base oxide. Irradiation at 60°C shows the same midgap shift as the low-dose-rate irradiation (After [Flee-94a]).

It should be noted that since low electric fields play a role in this low dose rate effect, fringing fields from the emitter-base bias can also impact the magnitude of the effect [Nowl-93, John-94, Pers-97], as can differences in internal fields between npn and pnp devices [Schm-95, Schr-95, Schm-96, Pers-97].

An additional phenomenon associated with these space charge effects should be mentioned. As described in Sections 2.1.4.3 and 2.2.1, positively charged hydrogen atoms (protons) are often responsible for many of the radiation-induced interface traps. These are subject to the same space charge effects that affect the hole transport in bipolar oxides at low electric fields. Thus one might also expect that the radiation-induced interface trap buildup would show a similar dependence on dose rate as the net oxide-trapped charge density, increasing at low dose rates. This effect has been observed in some bipolar base oxides and radiation-soft thermal oxides [Flee-96].

2.3.3 MEMS Devices

Microelectromechanical systems (MEMS) are miniaturized mechanical devices fabricated with integrated circuit processing techniques (an example is shown in Fig. 2.33). They often contain both electronic and mechanical structures on the same device. Thus one must be concerned about the radiation response of the electronics as in any other IC, and also any potential interactions between the electronics and the mechanical structure [Knud-96, Lee-96]. One might expect that the mechanical structures would be relatively immune to changes from radiation at normal dose levels. However, these structures are often coupled electrically to the material around them (in some cases forming part of the sensing circuitry), and thus their properties can be altered by irradiation. Such changes have in fact been observed in MEMS accelerometers [Knud-96, Lee-96].

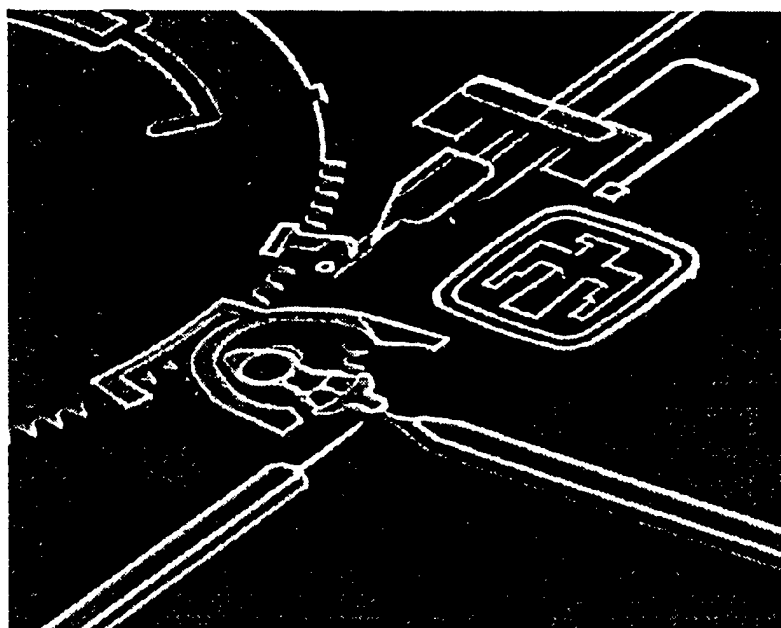


Figure 2.33. Example of a MEMS device structure.

In Fig. 2.34 is shown the output of a MEMS accelerometer when protons irradiate only the mechanical sensor. The structure of the accelerometer is shown in Fig. 2.35.

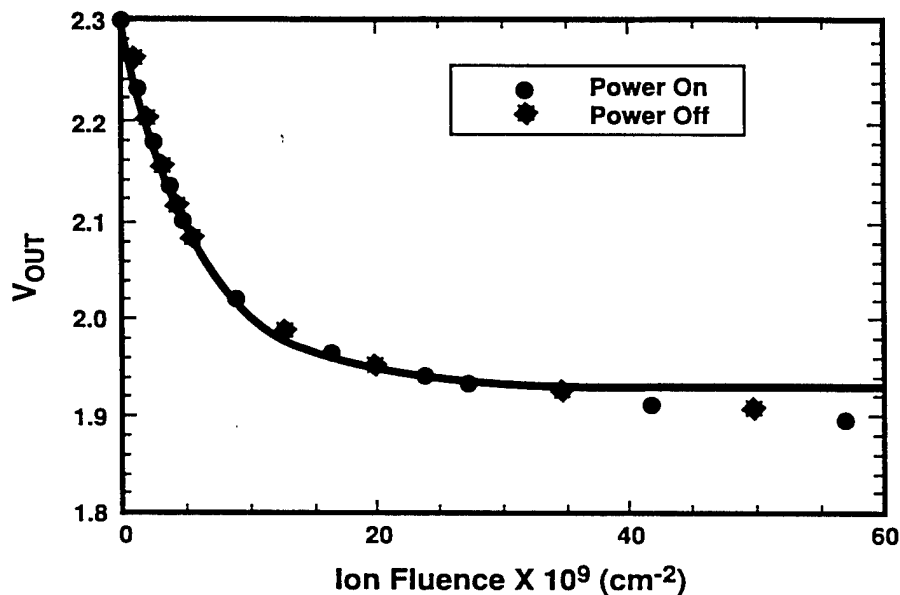


Figure 2.34. Output voltage in a MEMS accelerometer (ADXL50) as a function of proton fluence for the device both powered and unpowered (After [Knud-96]).

Analysis showed that the changes observed were caused by charge buildup in the dielectric layer underneath the moving beam. This charging changed the electric field distributions around the beam (which forms a variable capacitor in the sensing circuitry), which are the source of the output voltage shifts with irradiation. A different sensor design where the dielectric underneath the beam was covered by conductive polysilicon did not show this effect, since the trapped charge was screened by the conductive layer [Knud-96].

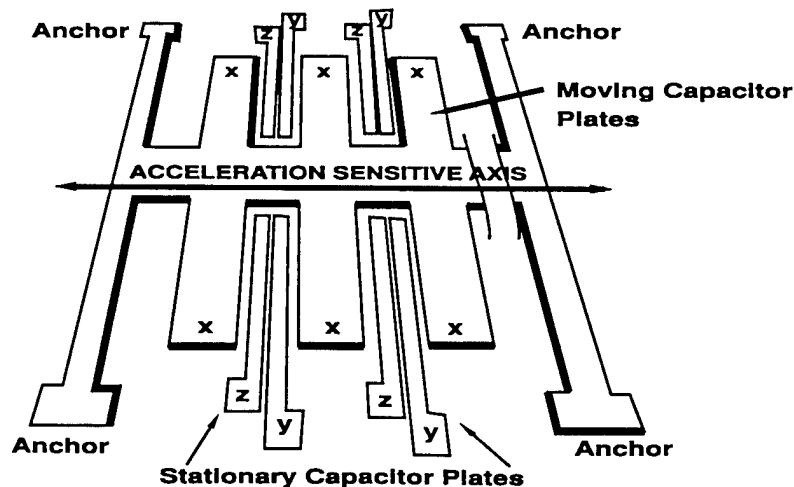


Figure 2.35. Structure of MEMS accelerometer showing the moving (X) and the stationary (Y & Z) beams (After [Knud-96]).

2.3.4 Other Devices

Mercury cadmium telluride (HgCdTe) infrared detectors use either passivated photodiodes or metal-insulator-semiconductor (MIS) structures as the basic detection element. They are usually also operated at cryogenic temperatures ($\sim 80\text{K}$). Work on the response of MIS HgCdTe devices to ionizing radiation has shown that many of the radiation-induced phenomena present in the Si/SiO₂ system are similarly present in this system. An example of the flatband voltage shifts for MIS capacitors (with a ZnS/CdS dual dielectric insulator layer) irradiated at 80K is shown in Fig. 2.36. With positive irradiation bias, the negative flatband voltage shift indicates positive charge trapping (as observed in the Si/SiO₂ system). Under negative irradiation bias, a positive shift occurs, indicating significant negative charge trapping in the insulator (not normally observed in thermally grown SiO₂). The buildup of radiation induced interface traps as a function of irradiation bias is shown in Fig. 2.37; in contrast to the Si/SiO₂ system, significant interface traps are created under negative bias in addition to under positive bias.

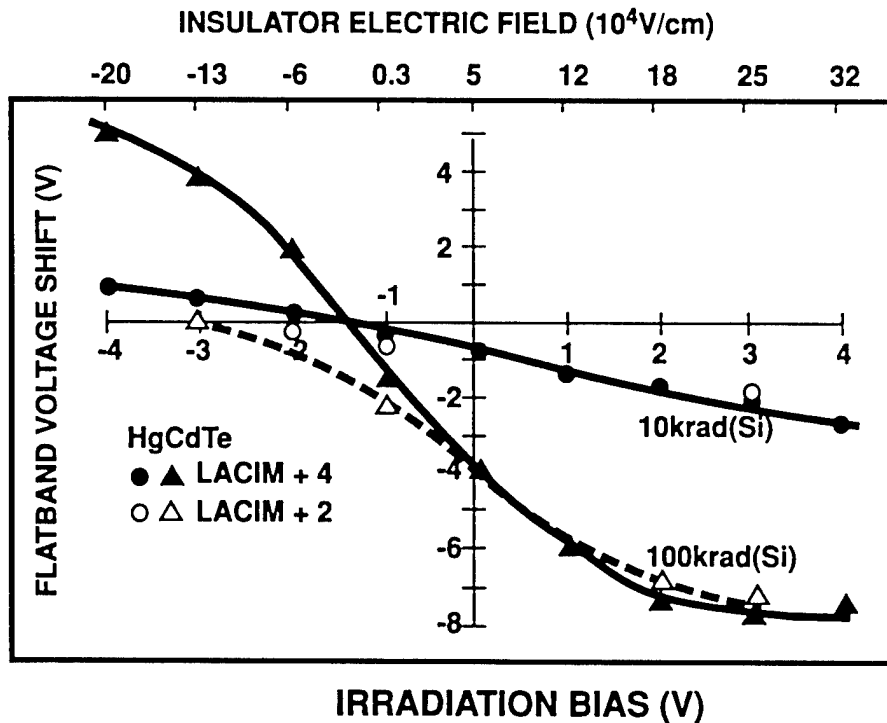


Figure 2.36. Flatband voltage shifts in different HgCdTe capacitors as a function of irradiation bias for two different dose levels (After [Mori-90]).

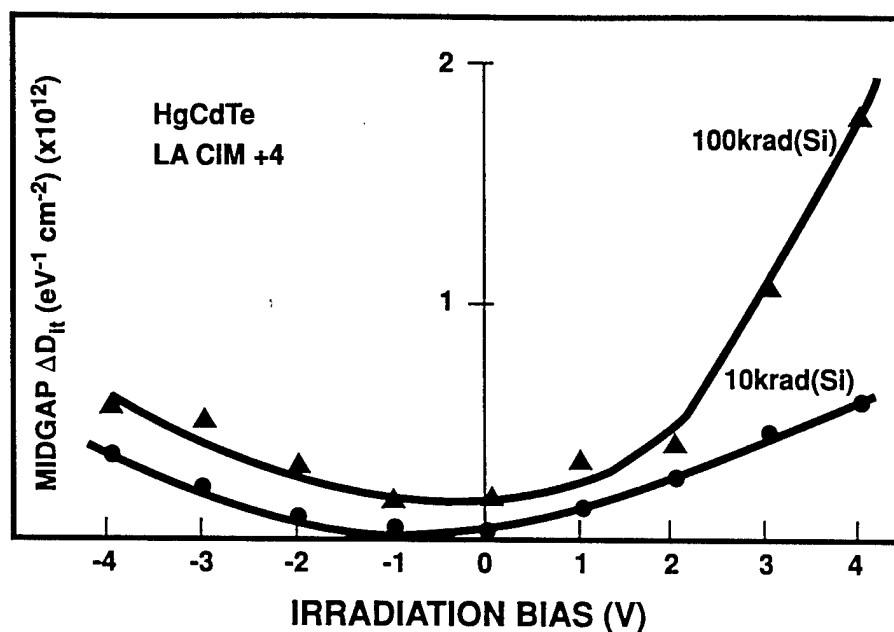


Fig. 2.37. Midgap interface trap density in an HgCdTe capacitor as a function of irradiation bias for two different dose levels (After [Mori-90]).

To provide the signal processing required, there may need to be silicon-based MOS circuits operating in conjunction with IR detectors (such as HgCdTe) at cryogenic temperatures. Also there are silicon IR imaging devices (such as CCDs) that are operated at low temperature. Interface traps typically do not play a significant role in device response in these circumstances, since as discussed in Section 2.1.4.1, the generation of interface traps is completely inhibited at temperatures below 100K. However, as discussed in Section 2.1.2, hole transport in SiO₂ can be effectively halted (the holes are trapped in place) at cryogenic temperatures at moderate electric fields. This can lead to large shifts in device characteristics compared to those observed at room temperature, as illustrated in Fig. 2.38. The double-humped structure of the 77 K data in this figure can be explained by the mechanisms described earlier. At low electric fields, a large number of the electron-hole pairs generated by the radiation recombine (see Section 2.1.1 and Fig. 2.3), leading to less trapped charge. At high electric fields, the holes become more mobile again leading to less charge trapping (see Section 2.1.2 and Fig. 2.5). To mitigate these large shifts at low temperature, approaches which create dielectrics with a substantial amount of electron trapping to compensate the charge from trapped holes [Saks-78, Saks-83] or which reduce the oxide thickness [Srou-77, Boes-78b] have been proposed.

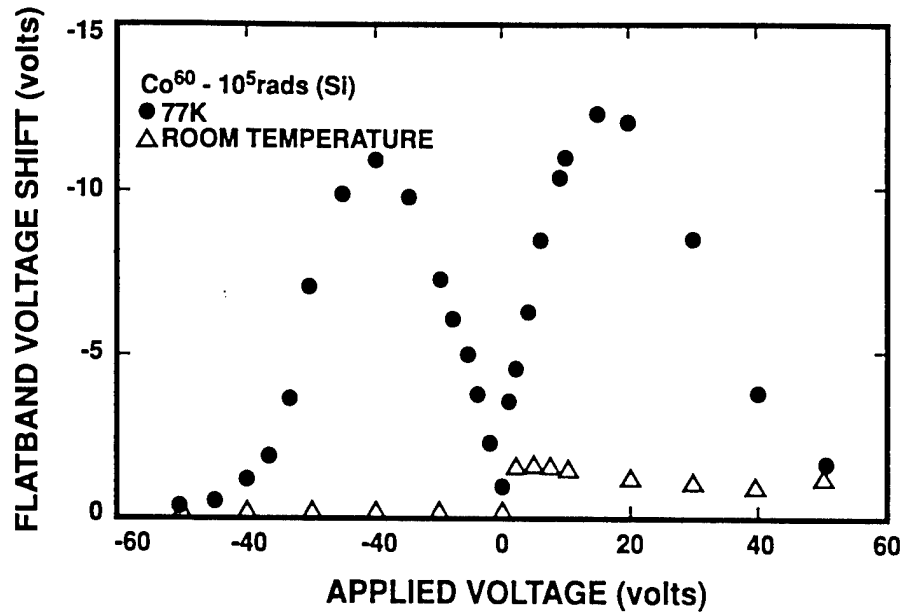


Figure 2.38. Flatband voltage shift in MOS capacitors as a function of applied voltage for irradiation at 77K and at room temperature (After [Srou-77]).

Since silicon carbide is a wide bandgap material, devices made from this material can operate at very high temperatures and thus hold promise for use in space nuclear power applications (and also commercial nuclear reactor applications). As might be expected (since their characteristics depend primarily on bulk material properties), JFET devices in silicon carbide have been shown to undergo little degradation in a total dose environment up to 100 Mrad(Si) (Fig. 2.39).

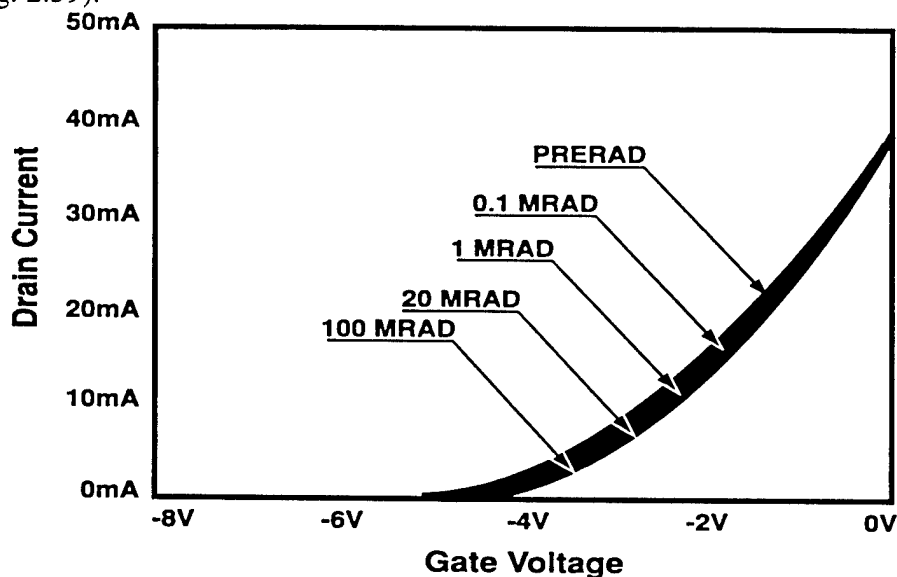


Figure 2.39. Current-voltage characteristics of a silicon carbide JFET for different total dose levels showing little effect from the irradiation (After [McGa-92]).

SiGe heterojunction bipolar transistors (HBTs) show promise for many high frequency applications, and can be relatively easily incorporated into a conventional silicon bipolar or BiCMOS manufacturing line. Thus SiGe technology may challenge GaAs for some high speed applications. Again as might be expected since they depend primarily on bulk material properties, these devices are relatively immune to ionizing radiation damage [Babc-95]. Devices grown by UHV/CVD also seem to have enhanced tolerance compared to modern silicon bipolar transistors since they have a thin dielectric emitter/base spacer, avoid implanting through the screen oxide, have a high doping at the surface of the base region, and have a lower thermal budget during processing [Babc-95]. Also in general, III-V heterojunction devices also tend to show little degradation with ionizing radiation [Subr-97].

3.0 DISPLACEMENT DAMAGE EFFECTS

3.1 BACKGROUND

3.1.1 Phenomenology

Energetic particles such as neutrons, protons, electrons, alpha particles, and heavy ions can create damage in semiconductor materials by displacing atoms as the particle transverses the material. (It should be noted that the secondary electrons produced by high energy photons can also cause this type of damage). This displacement damage can reduce minority carrier lifetime, change majority carrier charge density, and reduce carrier mobility, all of which lead to changes in device properties.

Much of the research in this area has focused on neutron irradiations of silicon, so this will be used to explain the general processes involved. The high-energy incident particle creates Frenkel defects (interstitial silicon and vacancy pairs) by collisions with silicon nuclei and by collisions of the primary recoil atom with other atoms in the silicon lattice. The interstitial silicon atoms, although very mobile even at 77K, do not form electrically active defect sites. On the other hand, the vacancies (also mobile at 77K) are effective by themselves as recombination and trapping centers, and also form electrically active defect complexes. These include the A center (a vacancy/oxygen complex), the E-center (a vacancy/n-type dopant complex, also called the P-V center for phosphorus/vacancy), and divacancies [Vook-68]. Since the interstitial silicon and vacancies are very mobile, many of them recombine shortly after creation so that only 5-10% remain to form stable defects [Mars-90, Mess-92].

Because the displacement cross-section for neutrons impacting silicon atoms is $\sim 3 \times 10^{-24} \text{ cm}^2$, an incident neutron will probably undergo only one interaction before exiting the active region of a device [Mess-92]. Thus most of the damage is actually done by the primary recoil (knock-on) atom (PKA). Simulations and experiments have provided insights into the damage track structure [Wood-81, Muel-82]. A representation of the defect and subcluster formation as a function of PKA energy is shown in Fig. 3.1.

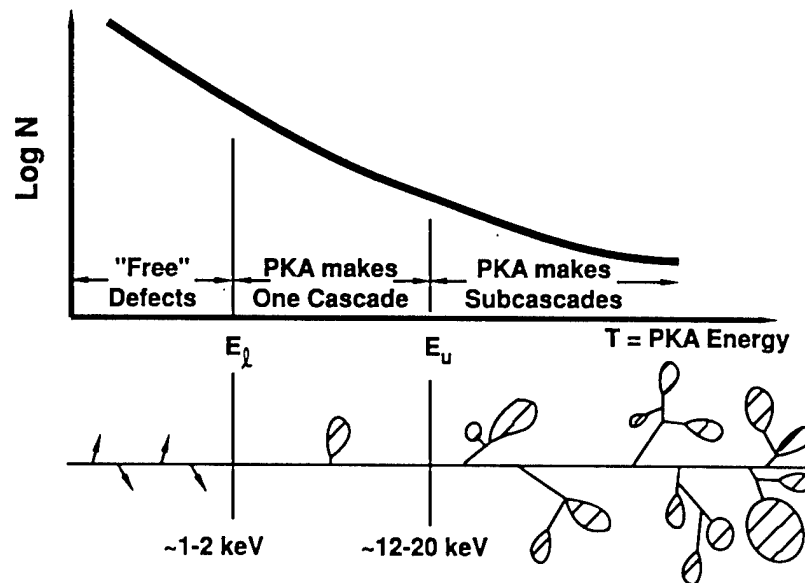


Figure 3.1. Schematic illustration of the defects and subcascades formed for primary knock-on (recoil) atom of different energies (After [Wood-81]).

The defects and subclusters created act as trapping, generation, recombination, compensation, and tunneling centers (illustrated in Fig. 3.2). These in turn can reduce minority carrier lifetime according to [Mess-92]

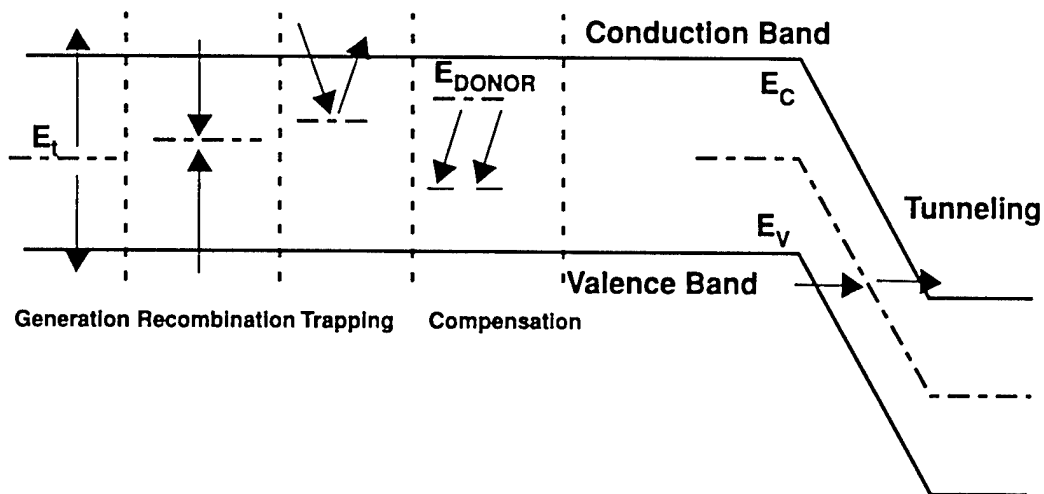


Figure 3.2. Illustration of the five primary effects that a defect level in the semiconductor band gap can have on device electrical performance (After [Hopk-96]).

$$1/t = 1/t_i + \phi/K(\delta n, p_0) \quad (3.1)$$

where t is the minority carrier lifetime, t_i is the initial minority carrier lifetime, ϕ is the neutron fluence, K is a universal silicon damage constant, δn is the injected carrier density, and p_0 is the majority carrier density. The effects on K of resistivity and injection level are shown in Fig. 3.3. Note that eqn. (3.1) leads to the Messenger-Spratt equation for gain degradation in bipolar transistors,

$$\Delta(1/\beta) = 1/\beta - 1/\beta_i = \phi/\omega_t K \quad (3.2)$$

where β is the common emitter current gain, β_i is the initial gain, and ω_t is the unity gain corner frequency [Mess-58].

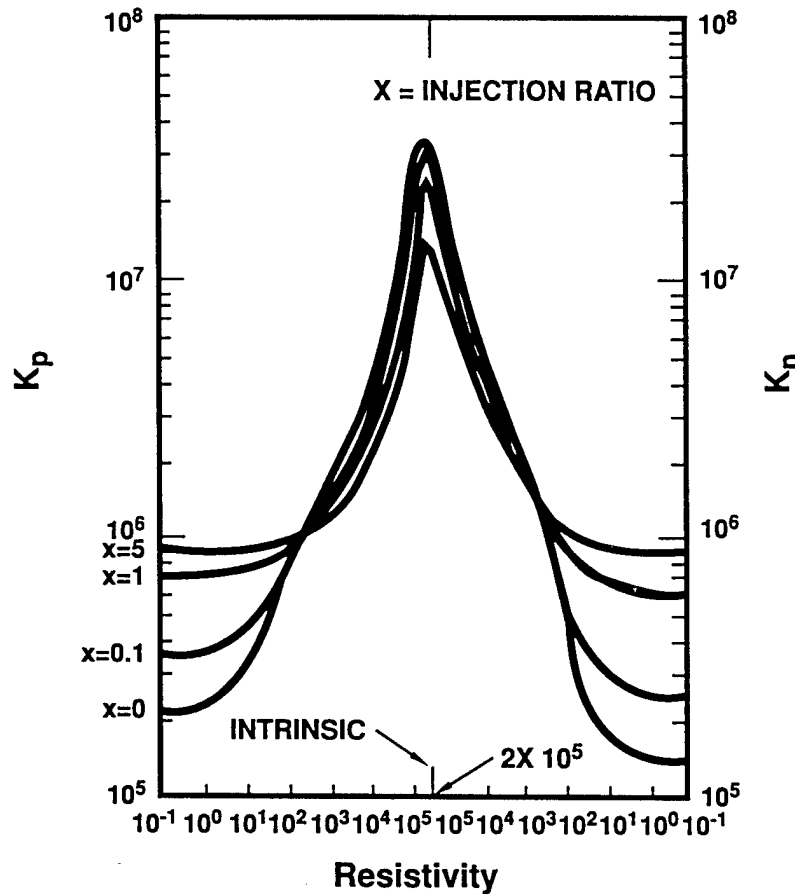


Figure 3.3. Damage constant in p- and n-type silicon as a function of resistivity and carrier injection ratio (After [Mess-92]).

The trapping levels associated with the defects can also reduce the majority carrier density in devices. An example of the carrier removal rates observed is shown in Fig. 3.4. These sites, when charged, can also increase the Coulomb scattering of charge carriers and thus their

mobility. For n-type silicon, analysis has shown the reduction in conductivity from these two effects has the form [Mess-86]

$$\partial\sigma/\partial\phi = -\sigma_i (K_i + 2K_{dv}) \quad (3.3)$$

where σ is the conductivity, σ_i is the initial conductivity, K_i is the introduction rate of the divacancy trapping center, and K_{dv} is the introduction rate of the donor vacancy trapping center.

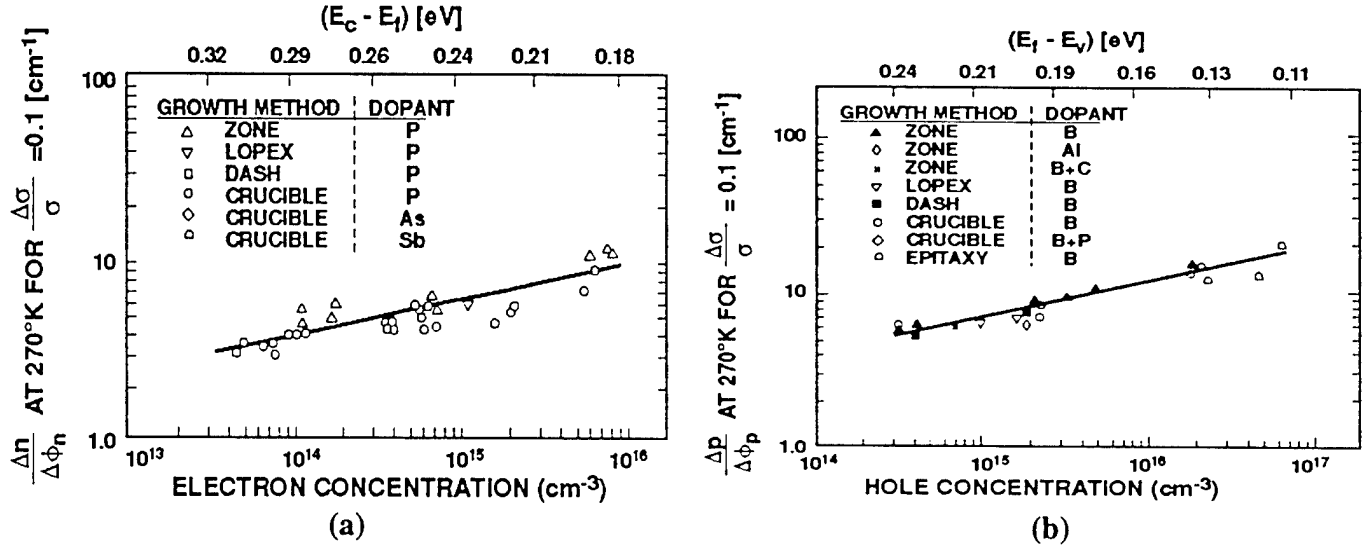


Figure 3.4. Carrier removal rates for (a) electrons and (b) holes in silicon grown by different methods and with different dopants and irradiated with 1 MeV neutrons. Removal rate is determined for a change in conductivity of 10% (After [Stein-68]).

In discussing the radiation damage caused by different particles and with different energy spectra, a common approach is to describe the damage produced in terms of an equivalent "standard" fluence. For example, reactors are routinely calibrated in terms of 1 MeV equivalent neutrons; in the solar photovoltaics community, different technologies are often compared by their response to 1 MeV electrons. In these approaches, the effect of a given environment is reduced to a fluence of, e.g., 1 MeV electrons, which produces equivalent damage.

3.1.2 NIEL

It has been demonstrated in several papers [Summ-87, Burk-88, Mars-89b, Summ-89a, Walt-91, Summ-93] that the displacement damage effects from a variety of different particles on several different technologies can be correlated on the basis of the nonionizing energy loss (NIEL). NIEL is a calculated energy loss per unit mass due to atomic displacements as a particle passes through a material; it thus does not include any energy loss to ionizing effects (i.e., creation of electron-hole pairs). NIEL has the same units as ionizing stopping power (eVcm²/g). The product of the NIEL and the particle fluence gives the total energy deposited as displacement damage along the track (similar to total ionizing dose).

The calculation of NIEL, S_{di} , for a monoatomic material consists of evaluating the expression [Walt-91]

$$S_{di} = (N/A_i) \sum_j \sigma_j(E) T_j(E) \quad (3.4)$$

where N is Avogadro's number, A_i is the atomic mass of the target atom, E is the energy of the incident particle, $\sigma_j(E)$ is the cross-section, $T_j(E)$ is the average energy of the recoil atom for the j^{th} type of interaction. Since not all of the recoil energy goes into displacements, $T_j(E)$ must be corrected for the energy lost in ionization processes. This partitioning has been discussed by Lindhard et al [Lind-63]; typically as the energy of the recoil atom increases, the fraction of total energy going into ionization processes increases as illustrated in Fig. 3.5. For compound materials, the total NIEL can be found by summing the contributions of each atomic species weighted by its atomic fraction f_i as described in [Summ-89b]:

$$S_d = \sum_i f_i S_{di} \quad (3.5)$$

$$\text{where } f_i = x_i A_i / \sum_i x_i A_i$$

and x_i is the stoichiometric number for the i^{th} element.

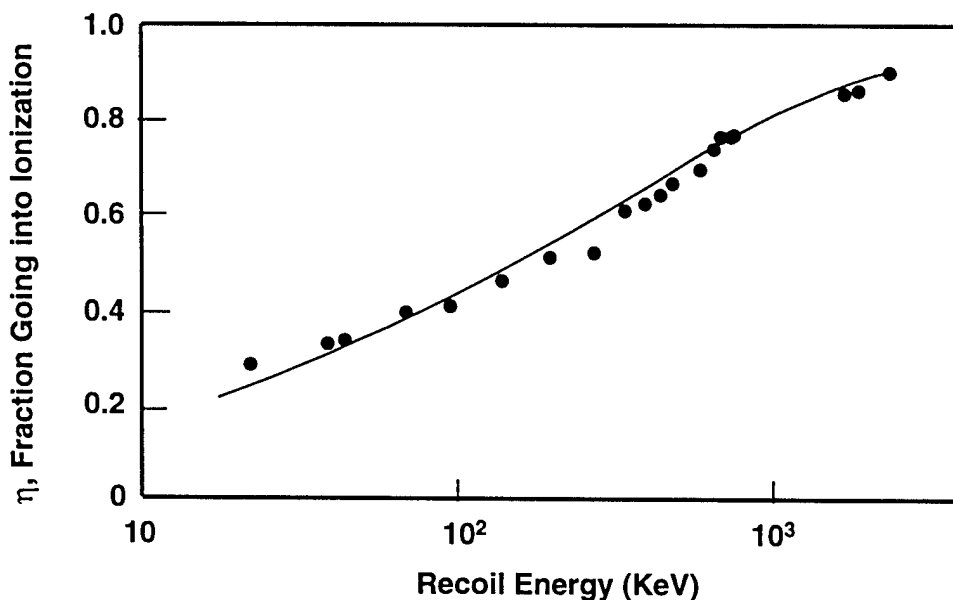


Figure 3.5. Fraction of total energy loss going into ionization processes as a function of the energy of the recoil atom (After [Satt-65]).

An example of the correlation observed between NIEL and short circuit current damage coefficients for proton and electron irradiation of GaAs solar cells is shown in Fig. 3.6. The advantage of having such a linear correlation between NIEL and experimental damage

coefficients is that one can calculate the expected degradation of device performance in a particular particle environment from knowledge of that environment, a measurement made at

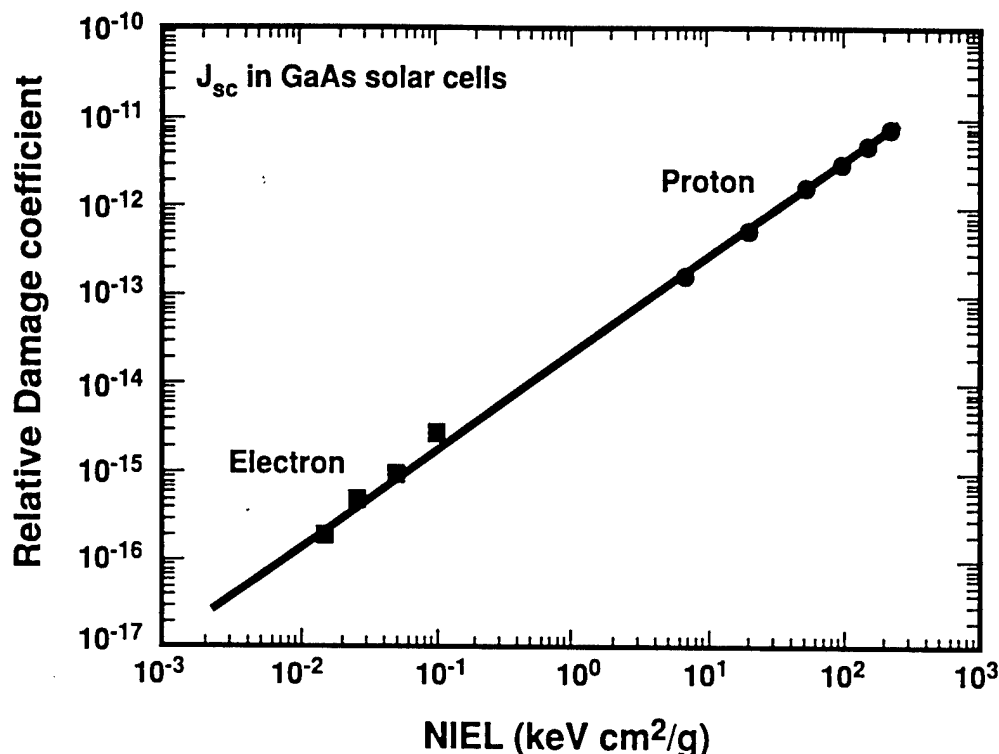


Figure 3.6. Relationship between short circuit current damage coefficient in GaAs solar cells and NIEL for proton and electron irradiation (After [Summ-93]).

one energy, and the calculated NIEL. The general result that NIEL is proportional to the number of stable defects created implies that the details of the interaction process itself are not usually important [Summ-87, Dale-91]. Thus the electrical properties of the stable defects are in general very similar, whether the displacements are in dense clusters or spread out as isolated centers (see Fig. 3.1, also [Alur-91, Mess-92, Hopk-96]). (However, it should be noted that there are some exceptions to this; for example, see the discussion of dark current in CCDs in Section 3.3 below). This linear dependence is found for relatively high NIEL values in most semiconductors, and for both low and high NIEL particles in n-type semiconductors [Summ-95].

It should be pointed out, however, that the linear correlation is not always observed. Figure 3.7 shows the damage coefficients for n- and p-type silicon exposed to electron and proton irradiation. Although the electron damage coefficient in n-type silicon shows a linear dependence on NIEL, that for p-type silicon shows an approximately quadratic dependence. The quadratic dependence at low NIEL has been observed for p-type Si, p-type GaAs, and p-type InP [Summ-95, Khan-96a]. The difference between the behavior observed for protons and electrons is likely a result of the much lower recoil energies typically produced by electrons. There appears to be a critical threshold NIEL value below which the damage coefficients for n- and p-type material diverge (as seen in Fig. 3.7). This value seems to be associated with the minimum

energy transfer needed for the formation of defect subcascades in the semiconductor [Summ-95]. The detailed mechanisms are not yet understood enough to completely explain this quadratic behavior.

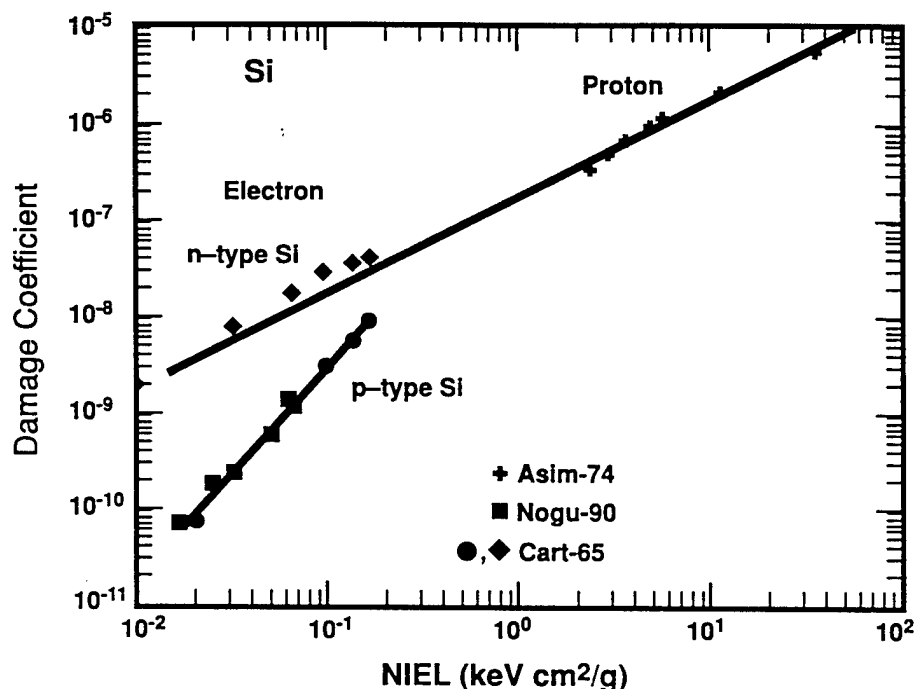


Figure 3.7. Relationship between diffusion length damage coefficients (crosses, circles, and diamonds), solar cell damage coefficients (squares) in silicon and NIEL for electron and proton irradiation (After [Summ-93]).

In GaAs, correlation between NIEL and photoluminescence damage constants for gamma and electron irradiation has been found to not be very good, whereas for heavier particles such as neutrons, protons, and heavy ions it is much better [Khan-96a]. Similar discrepancies have been observed between NIEL and lifetime degradation in GaAs for gamma and electron irradiation, but again is better for proton irradiations for energies below 200 MeV [Pare-97]. There are indications that these discrepancies arising at high energies may imply that the NIEL inelastic scattering parameter for proton irradiated GaAs needs revision [Carl-97]. Thus although there are many instances where damage constants correlate well with NIEL, there are cases where this correlation does not hold.

3.1.3 Defect Annealing

In general, annealing of displacement damage has not been described by a comprehensive theory. The situation is complicated by the fact that annealing depends strongly upon the carrier density level within the device. Fig. 3.8 shows the annealing factor (the amount of damage above its long-term value) of a bipolar transistor as a function of base-emitter voltage (and thus carrier injection level); the slowest annealing occurs when the transistor is off and has the lowest

carrier density. Temperature can also play a strong role in the anneal process, as shown in Fig. 3.9.

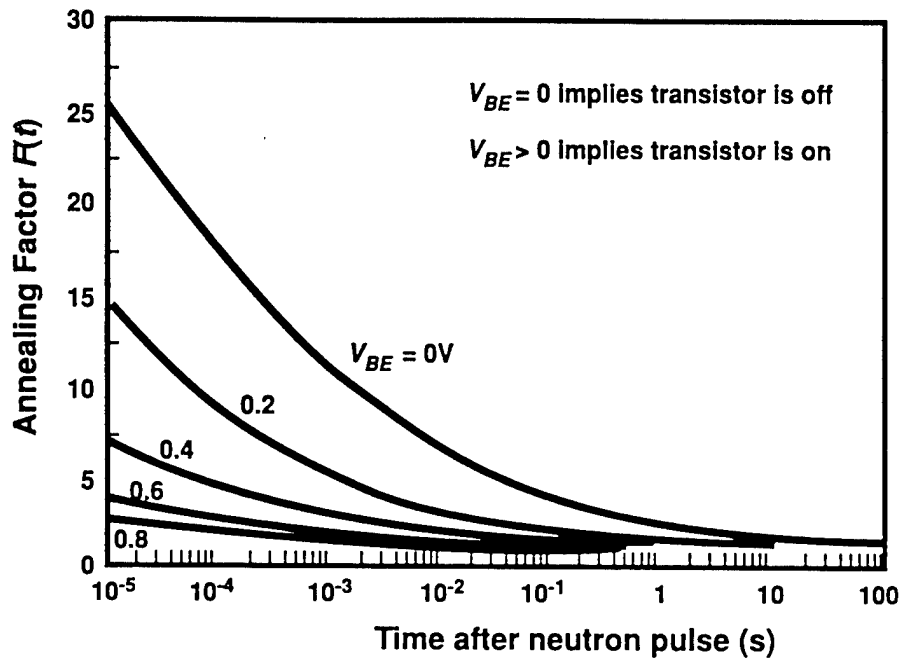


Figure 3.8. Annealing factor (amount of damage above the value at long times) at room temperature versus time after a pulse of neutron irradiation for bipolar transistors for a series of base-emitter voltages (After [Mess-86]).

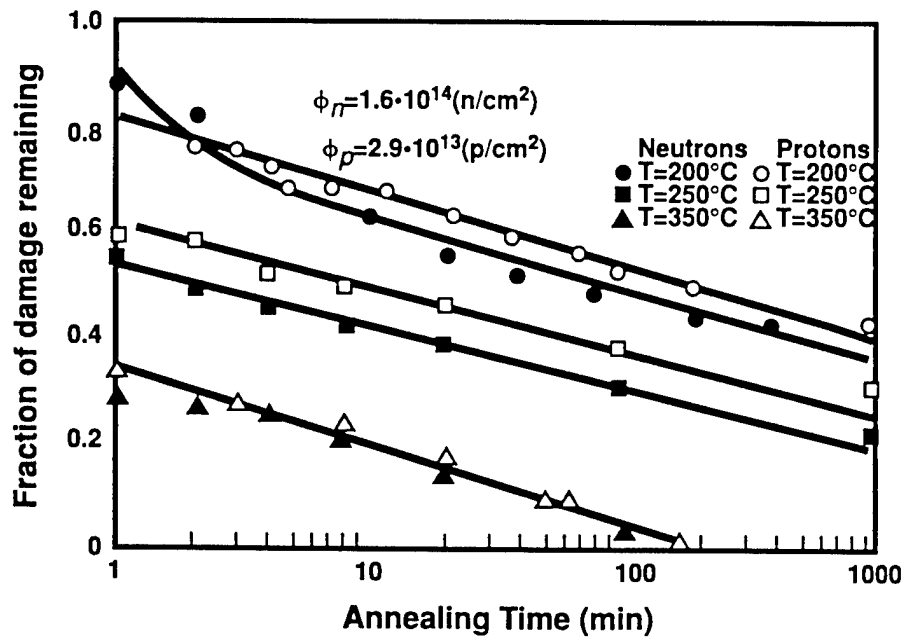


Figure 3.9. Damage annealing characteristics at different temperatures for a bipolar transistor after fast neutron and 16 MeV proton irradiations (After [Greg-70]).

3.2 COMPLICATING FACTORS

3.2.1 Defect Introduction

As seems to always be the case, the “true” picture is somewhat more complicated than described above. Although Eqn. (3.1) above does include some dependence of damage introduction on carrier concentrations (through the background majority carrier concentration and injected carrier density), defect introduction rates can further depend upon electron-hole recombination or carrier concentration both during and after the irradiation, upon the location within a device (e.g., a depletion region), and on the bias applied to the device [Drev-94]. For example, Fig. 3.10 shows the number of defects created by electron irradiation as a function of distance from the n^+ -p junction in a silicon solar cell [Drev-94]. There is a steep gradient in the concentration of traps as measured by two different techniques. It is thought that this gradient could be associated with the recombination of electron/hole pairs at defect sites (the energy released in this process could help effectively “anneal” the defect sites). Electron/hole pairs generated within the depletion region are rapidly separated by the internal electric field, and thus are much less likely to recombine at a defect within that region [Drev-94].

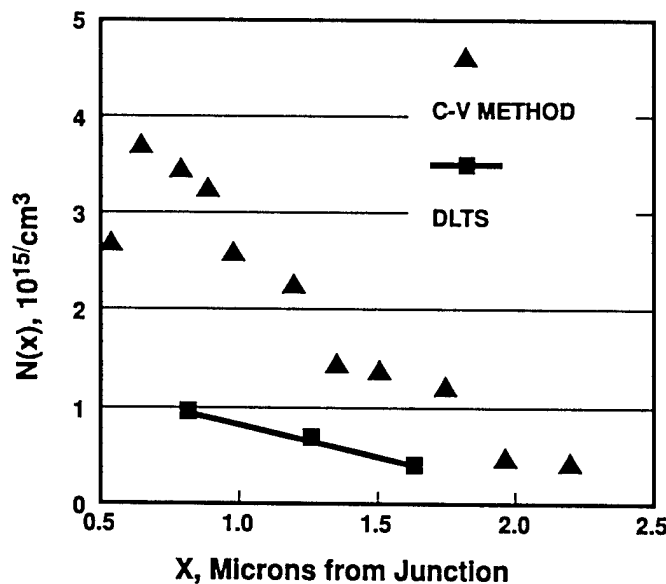


Figure 3.10. Defect concentration created by electron irradiation as a function of distance from the junction in a silicon solar cell as measured by DLTS and C-V techniques (After [Drev-94]).

3.2.2 Enhanced Carrier Generation

It has also been observed that in some cases the apparent “effectiveness” of displacement damage in generating carriers (e.g., dark current in CCD devices) is much greater than would be expected [Srou-85, Srou-86, Srou-89]. This has been associated with a spread in activation energies for thermal emission from traps, as shown in Fig. 3.11. Although most events can be described by the conventional thermal generation model of Sah-Noyce-Shockley [Sah-57], the events associated with small activation energies appear to be more consistent with phonon-assisted tunneling (with some contribution from the Poole-Frenkel effect) [Srou-89]. These results imply that defects generated in high-field regions of a device are likely to be more effective in generating carriers (and thus background currents) than those in low-field regions.

Another enhanced leakage current effect has been observed in high resistivity silicon diodes after neutron irradiation [Watt-96]. In this case the leakage current was found to be 50-600 times greater than that expected from standard Shockley-Read-Hall carrier generation. In effect the damage constant for these devices irradiated by Co^{60} gamma rays and 1 MeV neutrons did not scale with the NIEL. It appears that in the case of the neutron irradiation, defects were created which led to an intercenter charge transfer mechanism. This mechanism, illustrated in Fig. 3.12, has been observed in other work and can account for the enhanced carrier generation rates observed [Watt-96].

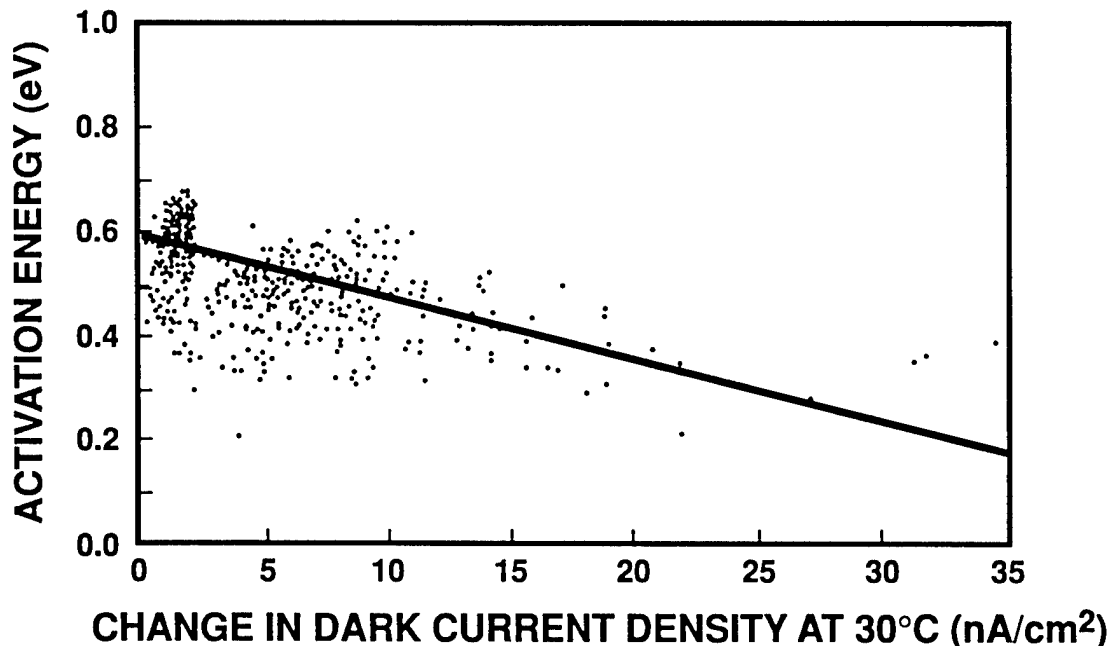


Figure 3.11. Activation energies versus neutron-radiation-induced dark current density in a CCD (After [Srou-89]).

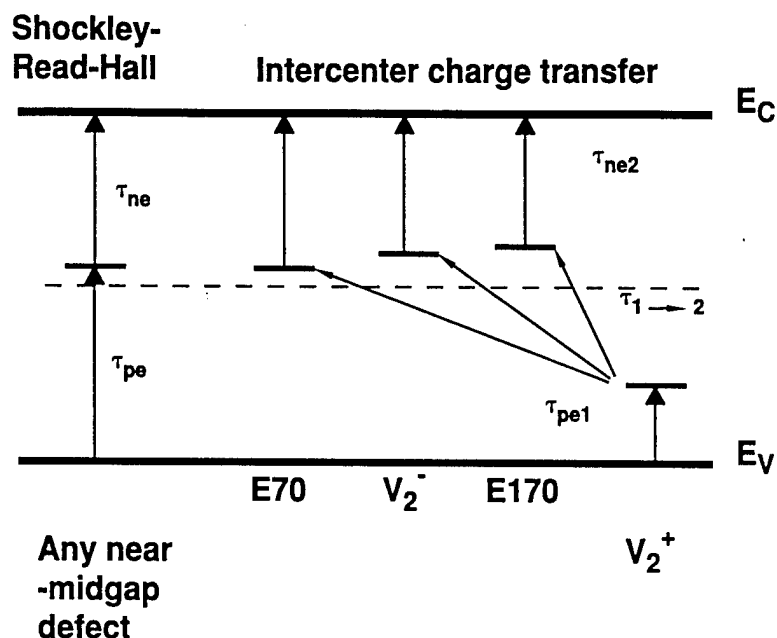


Figure 3.12. Schematic diagram of Shockley-Read-Hall and intercenter charge transfer charge generation processes (after [Watt-96]).

3.3 DEVICE IMPLICATIONS

The basic characteristics of displacement damage in devices – the creation of defects which can act as trapping sites causing minority carrier lifetime degradation, carrier removal, and mobility reduction—prove to be fairly universal across devices and radiation types. Thus this framework can be used to understand the response of many current and anticipated devices.

3.3.1 Solar Cells

The response of silicon solar cells in space radiation environments has been extensively investigated for over thirty years [Nash-71, Hove-75, Tada-82]. Much of this work examined environments in the low to medium fluence regime (up to 10^{13} p/cm² for protons and 10^{16} e/cm² for electrons), and found that the electrical performance decreased logarithmically with fluence. This dependence was well-explained by the reduction in minority carrier lifetime caused by the displacement damage from the irradiating particles. However, experiments at higher fluence levels showed an “anomalous” degradation which did not follow this trend – a rapid fall-off in electrical performance with fluence (along with an initial slight recovery of short circuit current) [Bebe-95, Mori-95, Yama-95, Oshi-96], as shown in Fig. 3.13. This “anomalous” degradation was explained and simulated by including the additional effects of majority carrier removal and minority carrier mobility reduction caused by the displacement damage (and which was not significant at lower fluence levels) [Oshi-96]. The good agreement between this theory and the experimental results is shown in Fig. 3.14.

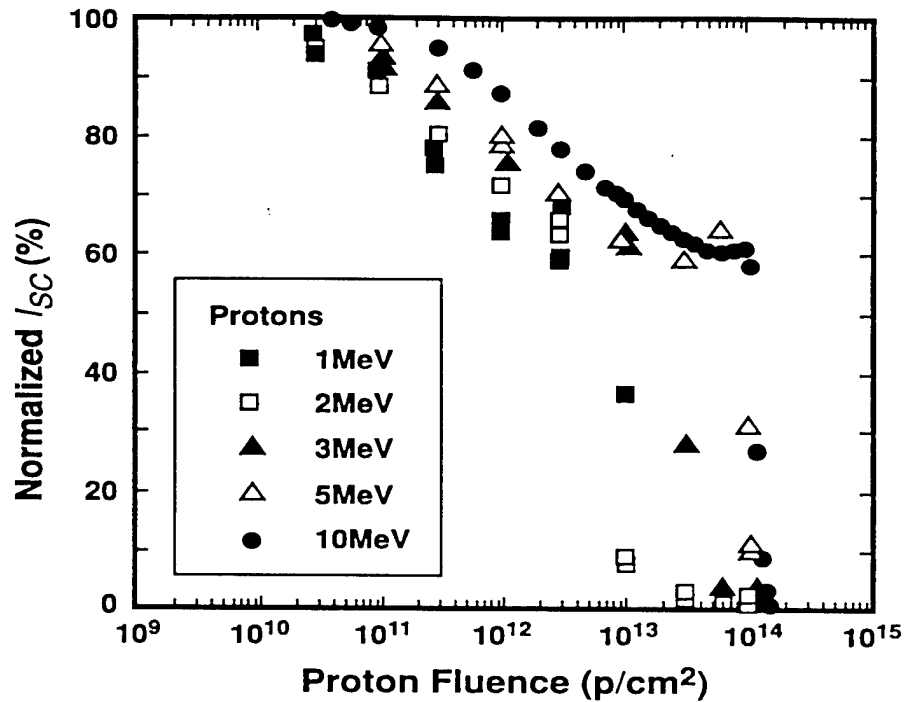


Figure 3.13. Normalized short circuit current in a silicon solar cell as a function of proton irradiation for different proton energies (After [Oshi-96]).

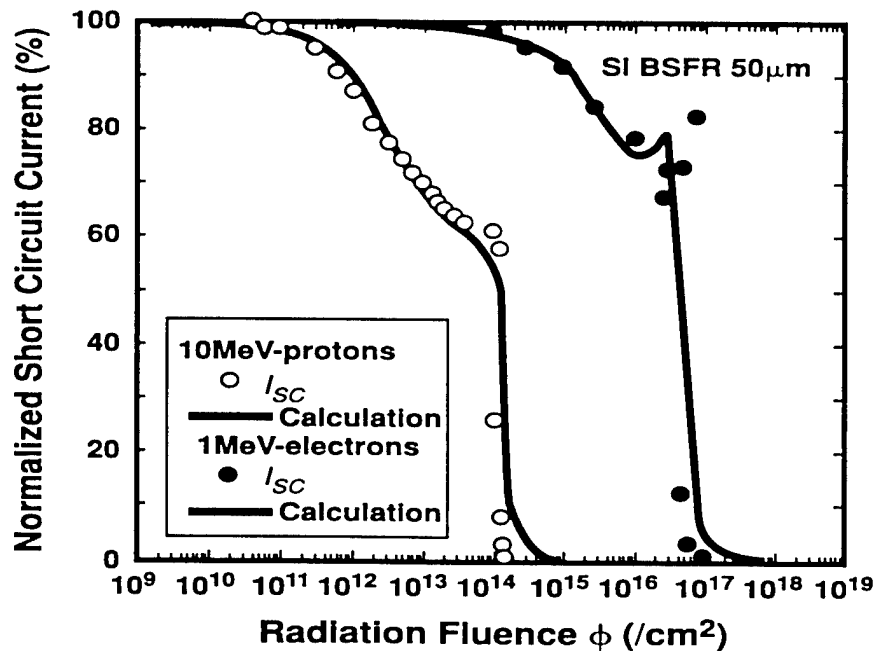


Figure 3.14. Simulation results (solid lines) of normalized short circuit current in a silicon solar cell compared to experimental data for irradiation by electrons and protons. Simulation includes minority carrier lifetime reduction, majority carrier removal, and minority carrier mobility reduction caused by the radiation damage (After [Oshi-96]).

Studies on more advanced solar cells made from InP [Walt-91] and $\text{Ga}_{0.47}\text{In}_{0.53}\text{As}$ [Walt-92] have shown that even though the defect centers created are very different from those in silicon and from each other, the damage response can be understood in terms of the NIEL for the given particle, energy, and material. This approach provides a basis for understanding why the InP solar cells are much more resistant to displacement damage than those made from Si or GaAs/Ge. For example, NIEL estimates show that protons are 12 times more damaging to Si than InP solar cells, and about 3 times more damaging to GaAs than InP cells [Walt-91]. The impact of this on efficiencies for solar cells from InP versus Si in various orbits is shown in Fig. 3.15.

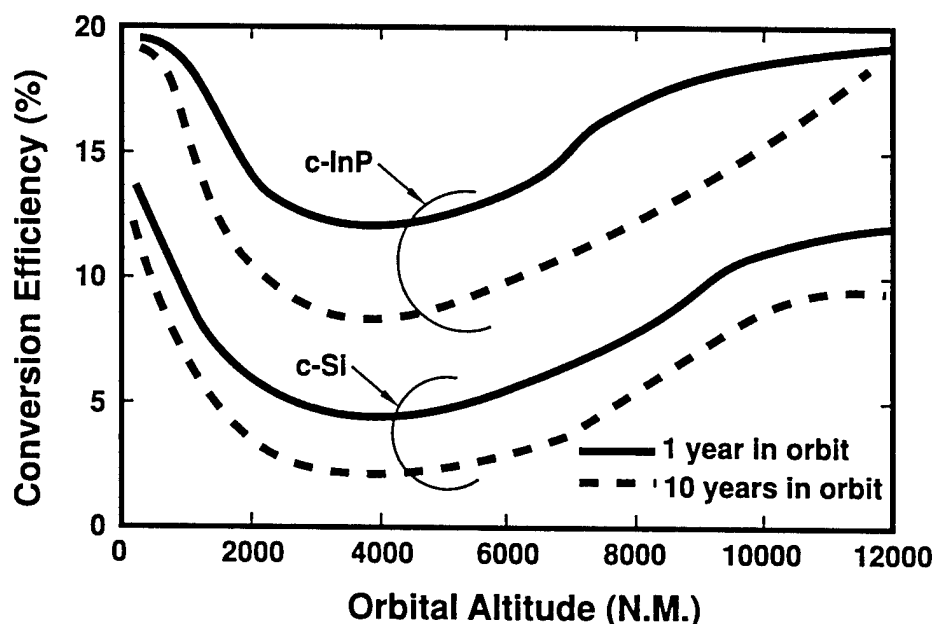


Figure 3.15. Calculated conversion efficiencies of InP and Si solar cells as a function of orbital altitude for 1 and 10 year missions (After [Walt-91]).

3.3.2 Advanced "Si-Based" Devices

For high frequency silicon bipolar devices, bulk displacement damage is typically not a significant problem. These devices have very narrow base widths, so that the increase in minority carrier recombination from displacement damage is small compared to other components of the base current. The decrease in gain degradation from the displacement damage as the cutoff frequency increases (i.e., the base width gets narrower) is illustrated in Fig. 3.16.

$\text{Si}_{1-x}\text{Ge}_x$ HBT devices show a degradation in performance with increasing proton fluence; this degradation is reduced by increasing the germanium content or increasing the proton energy as shown in Fig. 3.17. This trend agrees with that expected from the NIEL, which also decreases as the germanium content of the material or the proton energy increases [Ohya-96].

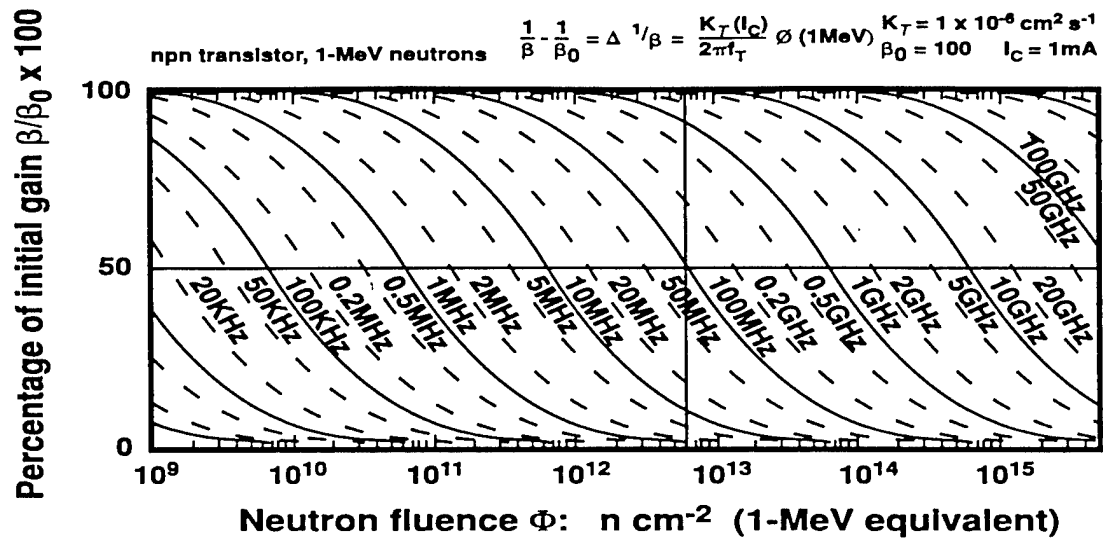


Figure 3.16. Bipolar gain as a function of neutron fluence for transistors with different cutoff frequencies (After [Holm-93]).

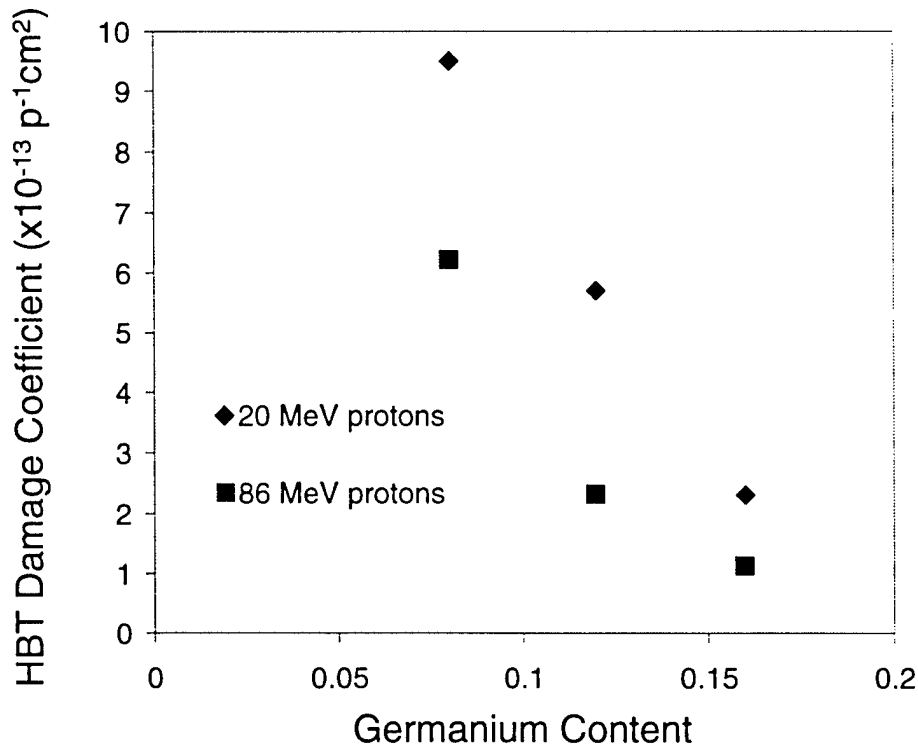


Figure 3.17 Degradation in $\text{Si}_{1-x}\text{Ge}_x$ transistors from proton irradiation for different germanium concentrations and different proton energies (After [Ohya-96]).

SiC devices may have application in space nuclear power systems. In a neutron radiation environment, they exhibit the common response of introduction of defects which cause carrier removal and mobility degradation [McLe-94]. These characteristics determine the response of the JFET devices commonly employed in this material system. Such devices have been shown to

be quite tolerant of very high neutron irradiation levels with a carrier removal rate of $\sim 4.5 \text{ cm}^{-1}$, corresponding to $\sim 5.5\%$ of the carriers being removed and a mobility reduction of 3.5% at a fluence of 10^{15} cm^{-2} [McLe-94].

3.3.3 Optoelectronic Devices

In advanced space systems, devices such as LEDs and semiconductor lasers may be used for optical interconnects or in optocouplers. Displacement damage in general can decrease the light output of radiation sources [Barn-86]. In horizontal cavity lasers the dominant degradation mechanism is non-radiative recombination in the active region of the device, whereas in vertical cavity surface emitting lasers (VCSELs) carrier removal is expected to be dominant [Paxt-97]. Again although the specific nature of the defects may vary, the primary effects can be understood in terms of the NIEL. For example, in Fig. 3.18 is shown the normalized lasing current threshold for an InGaAs/GaAs quantum well laser versus proton fluence. The carrier-removal-based damage factor from this data is within the experimental uncertainty of that which would be predicted from NIEL relationship. Results of irradiation by 200 MeV protons on multiple quantum well GaAs/GaAlAs laser diodes have also shown correlation with the NIEL [Zhao-97].

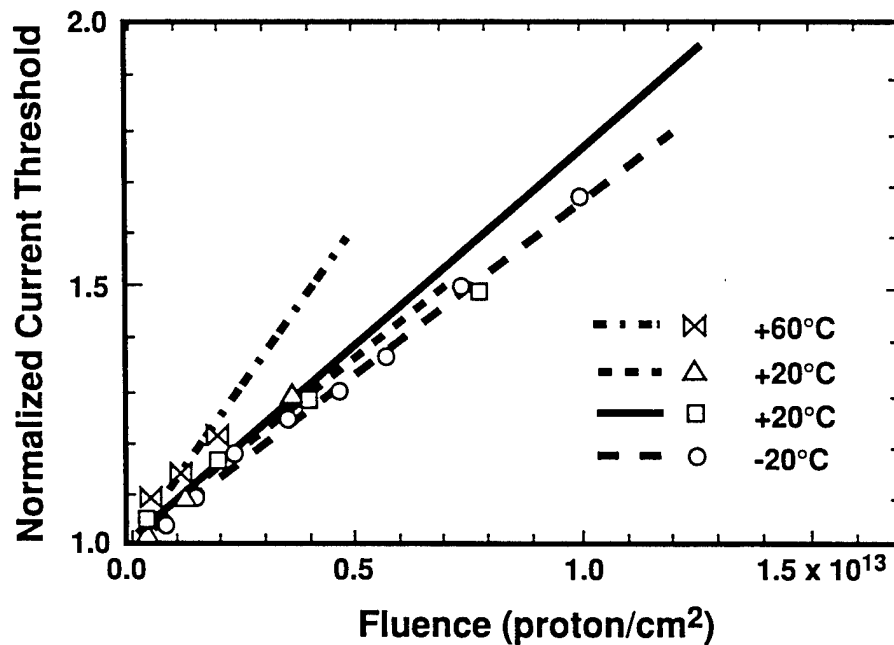


Figure 3.18. Normalized lasing current threshold at different temperatures for an InGaAs/GaAs quantum well laser versus proton fluence (After [Evan-93]).

By their nature photodetectors are in fact radiation detectors, and so produce a signal in response to ionizing radiation. Displacement damage can cause permanent effects such as increased dark currents and reduced responsivity [Wicz-86].

Quantum well infrared photodetectors (QWIPs) may provide some advantages for IR imagery. These are based on GaAs/GaAlAs quantum well structures, and their response to

displacement damage can be understood in terms of the effects on GaAs. In particular the primary concerns are carrier removal and degradation of carrier mobility and lifetime. The effect of displacement damage in QWIPs is mainly the removal of electrons from the quantum wells [Khan-96b]. Since the dark current has an exponential dependence on electron density and the IR absorption is directly proportional to the electron density [Liu-95], it is expected that the dark current would be the more sensitive parameter to radiation. However, since electron removal is the primary effect, the dark current actually decreases with irradiation as shown in Fig. 3.19; at a 0.8 MeV proton fluence of $2.5 \times 10^{13} \text{ cm}^{-2}$ the dark current has decreased by over four orders of magnitude. Concomitantly, the responsivity has degraded by a factor of 700 at this fluence level (Fig. 3.20).

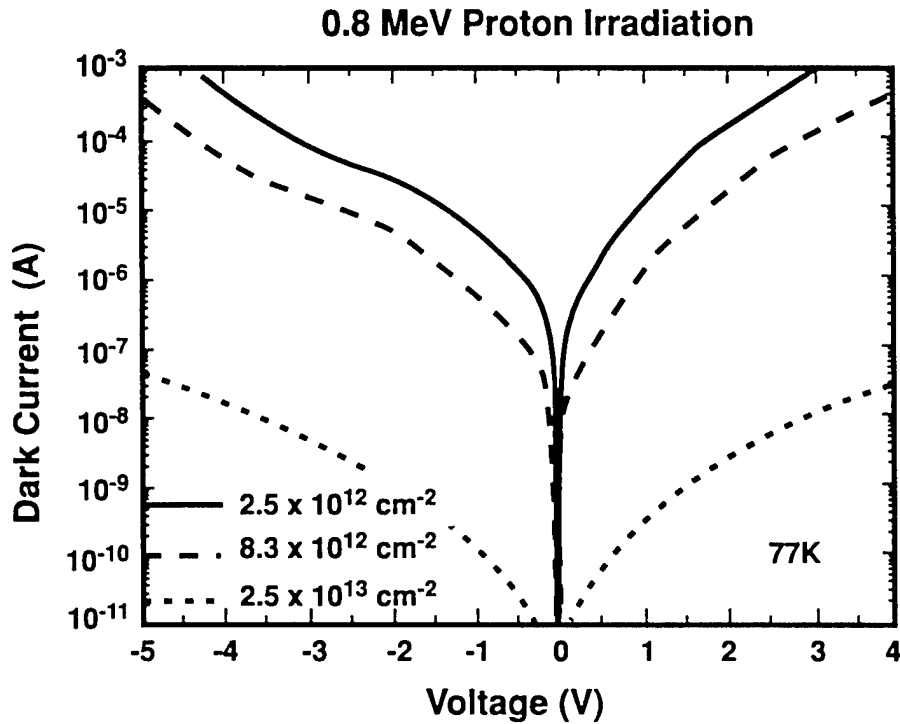


Figure 3.19. Dark current at 77 K versus voltage in a QWIP after irradiation at several proton fluences (After [Khan-96b]).

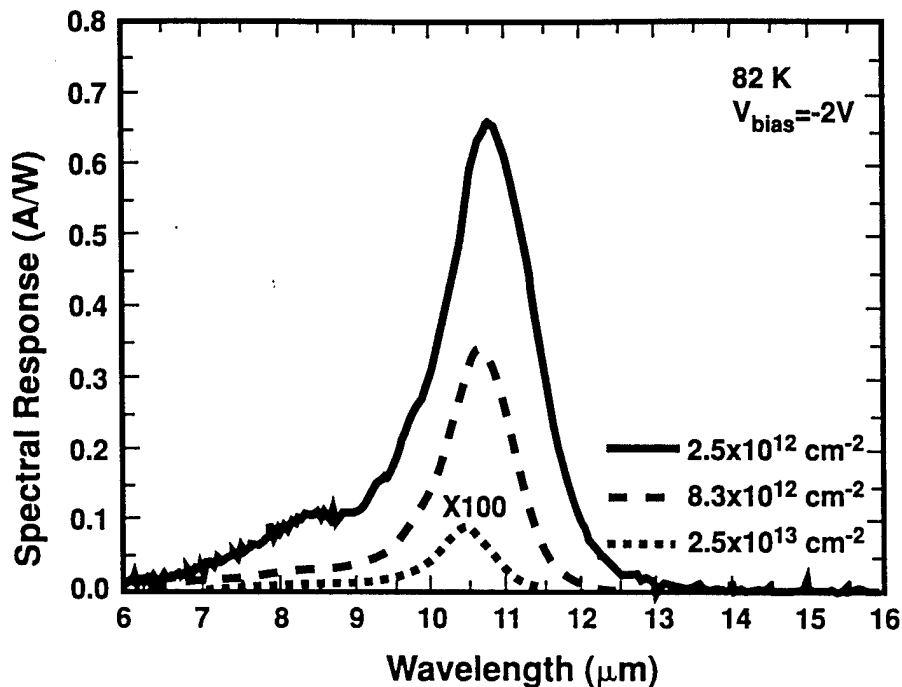


Figure 3.20. Spectral responsivity at 82 K versus wavelength in a QWIP after irradiation at several proton fluences (After [Khan-96b]).

3.3.4 High Temperature Superconductors

Another set of devices which may be used in advanced space systems are those based upon high temperature superconductors. A reduction in the superconducting critical temperature has been observed for $\text{YBa}_2\text{Cu}_3\text{O}_{7-\delta}$ and $\text{Bi}_2\text{Sr}_2\text{CaCu}_2\text{O}_8$ materials [Summ-89b, Lomb-92]. The shift of the critical temperature T_c with fluence ϕ versus NIEL is shown in Fig. 3.21, again showing an excellent correlation between a radiation damage parameter and this measure of displacement effects. However, the critical current has a much more complicated dependence on radiation-induced defects, often first increasing and then decreasing with irradiation level [Civa-90, vanD-90, Mezz-96, Khan-97]. This initial increase can be explained by the introduction of defects which cause enhanced flux pinning, thus leading to a higher critical current.

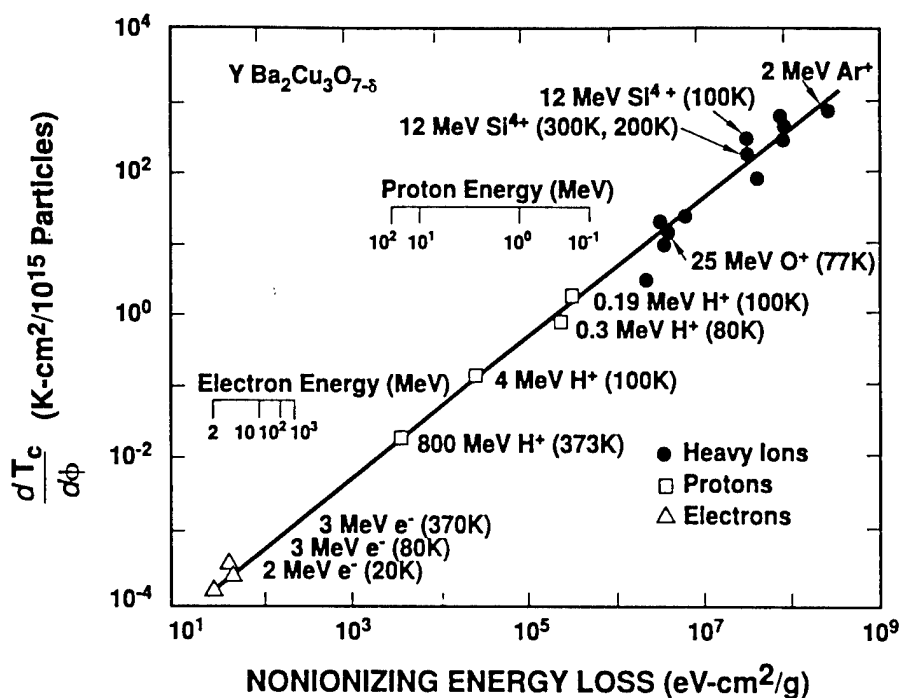


Figure 3.21. Rate of change in critical temperature with fluence for YBa₂Cu₃O_{7-x} versus NIEL for electrons, protons, and heavy ions at a wide variety of energies (After [Summ-89b]).

3.3.5 Silicon Detectors

Silicon detectors are widely used in high-energy physics experiments. With the increasing energy and luminosity of these experiments, these detectors are exposed to high particle fluences (up to several 10¹⁴ cm⁻²) and high ionizing radiation doses [Li-93, Wuns-97]. The detectors are often p⁺-n-n⁺ junction structures with high resistivity (~4kΩ-cm or greater) material. It has been observed that displacement damage can increase the leakage current of these detectors and also change the voltage required to fully deplete the device (which can affect the charge collection properties if the depletion voltage increases above the applied voltage) [Li-93, Wuns-97].

The increase in leakage current is easily explained by the creation of generation centers as illustrated in Fig. 3.2. The change in depletion voltage is caused by a change in the effective impurity concentration in these devices. The silicon can undergo type inversion (i.e., change from n- to p-type) as a result of displacement damage. This phenomenon is shown in Fig. 3.22. The n-type effective impurity concentration (N_{eff}) decreases with increasing neutron fluence, and approaches zero at ~2x10¹² cm⁻². Above this fluence level, the effective impurity concentration increases again, but is now acceptor-like (p-type material). This effect can again be explained by Fig. 3.2. Displacement defects form acceptor sites which compensate the donors, and then eventually dominate to change to material to p-type [Li-93, Li-96].

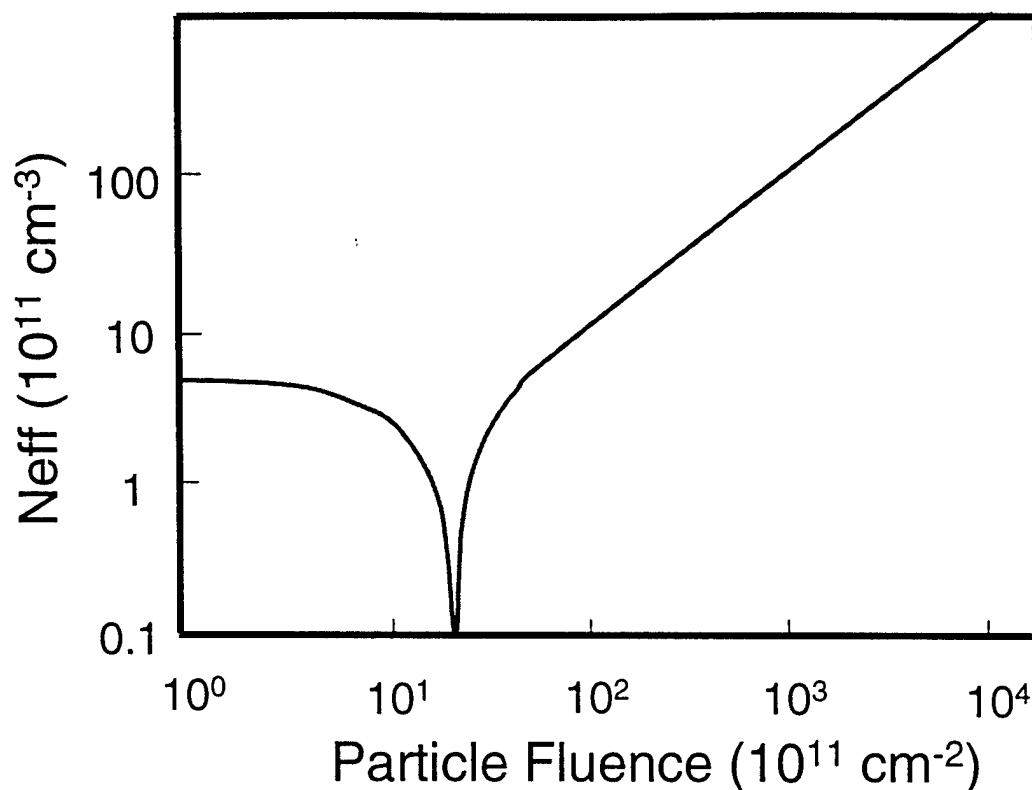


Figure 3.22. Effective impurity concentration in silicon as a function of neutron fluence determined from C-V measurement of silicon detectors. Note the inversion from n-type to p-type at $2 \times 10^{12} \text{ cm}^{-2}$ (After [Wuns-97]).

3.3.5 Single Particle Damage

The above discussion has focused on the average effects of displacement damage from a large number of particles. There is an issue, particularly for VLSI devices with very small geometries and active volumes, of whether a single particle (such as a neutron, proton, or heavy ion) can create enough displacement damage to cause device failure. This question was addressed in [Srou-81]. Some potential problem areas in MOS and bipolar devices are shown in Fig. 3.23. In the MOS device, one might expect lower punch-through voltages, channel mobility reduction, threshold voltage shifts, and enhanced gate leakage current. In the bipolar device, one might expect enhanced leakage current due to punch through and current gain degradation due to increased recombination. Experimental data in [Srou-81] showed measurable effects apparently from single neutrons on small bipolar devices. However, the interpretation of such single particle effects on bipolar gain changes or MOS threshold voltage shifts is difficult due to the dependence on the nature of the damage region. More clear-cut analysis is possible by evaluating changes in reverse-bias or dark currents.

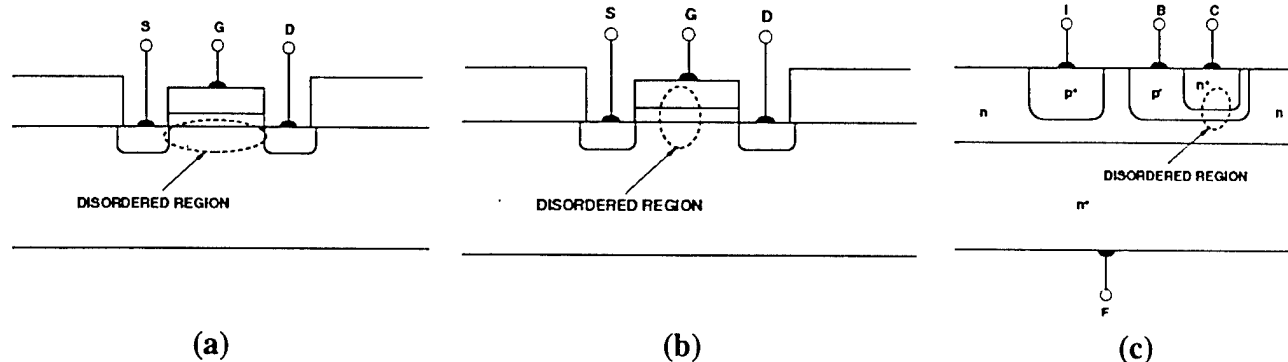


Figure 3.23. Schematic of possible displacement damage regions resulting from passage of a single particle in MOS (a & b) and bipolar (c) devices. In (a) the damage region might be expected to change channel properties such as punch-through voltage and channel mobility. In (b) the damage region might be expected to alter threshold voltage and gate leakage current. In (c) the damage region might be expected to change leakage current and bipolar gain (After [Srou-81]).

Such evidence for the importance of damage from a single particle is provided by data on proton effects on charge-coupled devices (CCDs). Although total ionizing dose effects can cause changes in CCD characteristics, device design, architecture, and operational parameters can minimize these effects. However, the displacement damage from a single proton can have a marked effect on parameters such as charge transfer efficiency (CTE) and dark current. For example, in a buried channel CCD the density of trapping states in the channel must be very low to maintain a high CTE (typically one would want a CTE >0.9999 , corresponding to $<10\%$ signal loss for 1000 transfers). This means that for a signal size of 1000 electrons, there must be less than one radiation-induced defect which traps an electron for every 10 pixels. With a typical packet volume of $50 \mu\text{m}^3$, this corresponds to a defect density of $\sim 2 \times 10^9/\text{cm}^3$ [Hopk-96]. It has been estimated that a 10 MeV proton fluence of $\sim 2.4 \times 10^8 \text{ cm}^{-2}$ can create 2×10^9 defect centers/ cm^3 [Holl-93]. This is well within the range of fluences expected in a typical space mission. Dark current can be similarly impacted by defects from a single proton. A single midgap state within a $20 \mu\text{m} \times 20 \mu\text{m}$ pixel can generate $\sim 3 \text{ pA/cm}^2$ at room temperature (assuming the state has a capture cross-section of 10^{-15} cm^2); this compares to the average dark current density in such devices of 10 pA/cm^2 [McGr-87].

Although this average increase in dark current density with displacement damage is important, a more significant effect is the increase in nonuniformity of dark current between pixels. An example of the dark current across a row of pixels in a CCD is shown in Fig. 3.24. Different portions of the row were masked during irradiation to achieve the different fluence levels shown. Different mean values of dark current can be seen for the different fluences, but also clearly evident are the large current spikes. These arise partly from inelastic nuclear reactions with a single proton; these deposit large amounts of nonionizing energy within a pixel

but are relatively rare [Srou-86, Hopk-96]. Another contributing factor to the high dark current spikes is the field-enhanced emission discussed above in Section 3.2.2. This effect has been

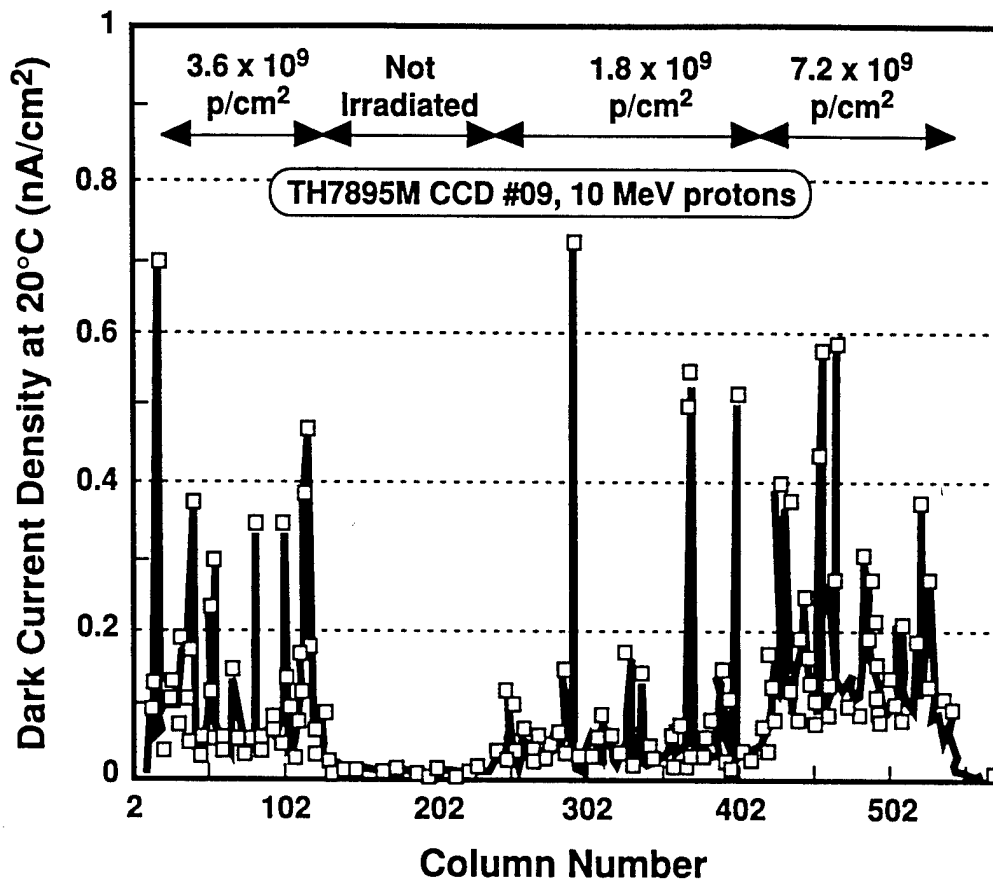


Figure 3.24. Dark current density in a pixel across a row in a CCD after proton irradiation to various fluence levels (obtained by masking different areas during irradiation) (After [Hopk-96]).

discussed in CCDs by a number of authors [Hopk-89, Mars-89a, Srou-89, Dale-90, Bang-91, Hopk-96]. It should be noted that these characteristics are representative of a circumstance where the NIEL approach no longer is adequate - namely when the affected volume is of same order as the damage region [Dale-94].

4.0 SINGLE EVENT EFFECTS

4.1 BACKGROUND

4.1.1 Description

A high-energy particle passing through a material can cause displacement damage as discussed earlier or electron-hole pairs by ionization of the atoms in the material. Charge collection as a result of the ionization interactions can cause changes in circuit operation or in the

information stored, leading to what are known as single event effects (SEE). An energetic ionizing particle going through a semiconductor material creates a track of ionization with a radius typically less than 1 μm and within which the carrier density decreases from the center with an r^{-2} dependence [Katz-68a, Katz-68b, Kobe-68a, Kobe-68b, Hamm-79]. A schematic depiction of a typical ionization track is shown in Fig. 4.1. The energy deposited by an incident particle is given by its stopping power or linear energy transfer (LET), usually given in units of $\text{MeVmg}^{-1}\text{cm}^2$. The stopping powers for ions at various energies can be calculated using the TRIM code [Zieg-85]. The LET describes the electron-hole density that will be generated along the track. In silicon, it takes 3.6 eV to produce an electron hole pair, so that an LET of 98 $\text{MeVmg}^{-1}\text{cm}^2$ will produce 1 $\text{pC}/\mu\text{m}$. In general, the deposited charge in a track Q_t (in $\text{pC}/\mu\text{m}$) can be determined from

$$Q_t = 1.6 \times 10^{-2} (\text{LET})(\rho)/E_p \quad (4.1)$$

where LET is in units of $\text{MeVmg}^{-1}\text{cm}^2$, ρ is the material density in g/cm^3 , and E_p is the minimum energy required to create an electron-hole pair in eV.

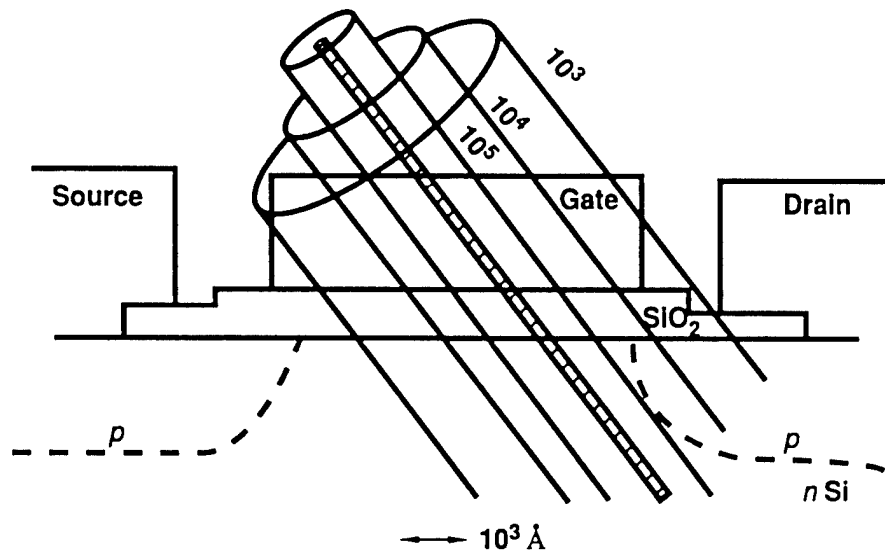


Figure 4.1. Schematic representation of the ionization track from a single energetic particle passing through a device structure showing the $1/r^2$ dependence of deposited dose (After [Brad-80]).

These electrons and holes can recombine via direct band-to-band transitions, Shockley-Read-Hall (SRH) recombination, or Auger recombination. Direct transitions have a low probability in indirect gap semiconductors such as silicon. SRH recombination depends upon the presence of localized traps in the forbidden gap of the material, and thus depends on the number of defects or impurities and the location in energy of their trap states. Auger recombination is a three-carrier interaction, and tends to dominate only at high carrier densities ($>10^{19} \text{ cm}^{-3}$ for silicon).

Those excess carriers that do not recombine can transport through the material by either drift or diffusion. Drift is motion which occurs in response to an electric field. Diffusion is motion which is driven by gradients in carrier concentration. In order for the excess carriers or charge generated by a particle to cause changes in device properties, the carriers must be transported by one of these mechanisms to active regions of a device where they can be collected and change the device or circuit characteristics or operation. For devices with several p-n junctions spaced within a few carrier transport lengths, interactions between those junction regions can act as parasitic devices. For example, a secondary photocurrent can be created when a two-junction device acts as a bipolar transistor [Cald-63].

Since particle tracks can create very high charge densities, they may create very high conductivity regions that can markedly alter the internal field structures in a device from their usual configurations. A depletion region can be effectively negated in the region of an ion track, and the fields associated with this region moved to the end of the track. This can cause the collection of an amount of charge much greater than that deposited in the equilibrium depletion region, leading to the "funneling" effect [Hsie-81]. This can lead to total charge collected at a circuit node much larger than would be expected from normal drift and diffusion, as illustrated in Fig. 4.2. It should be noted that drift and funneling typically cause collection of charge at a single circuit node, whereas diffusion can cause collection over several adjacent nodes.

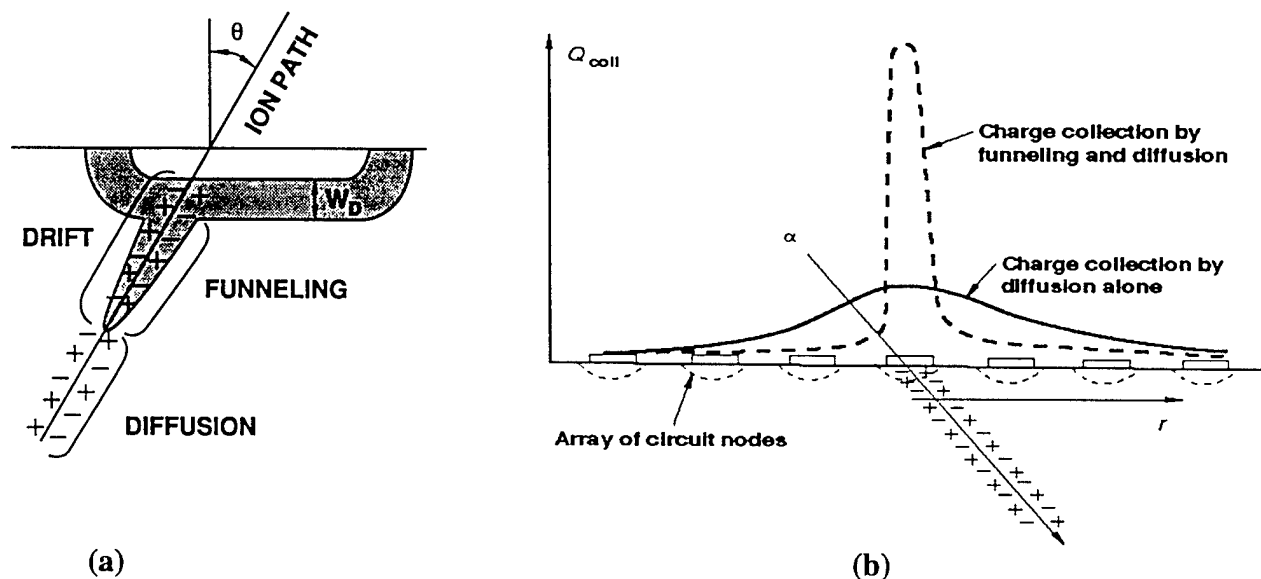


Figure 4.2. Charge collection from passage of a single ion (a) in a single junction and (b) in a circuit array showing collection due to drift, funneling, and diffusion. Note that the charge collected from diffusion can spread over several circuit nodes (After [McLe-82]).

When a high-charge-density track extends across several junctions, the regions on either side of the junctions are effectively coupled leading to the "ion shunt" effect [Knud-84, Haus-85, Knud-86]. In this situation charge can be transported along the track by drift, effectively "shorting out" what would otherwise be back-to-back p-n junctions, as shown in Fig. 4.3. As the

charge densities decrease from transport or recombination, the parasitic bipolar transistor may be turned on and contribute secondary photocurrent to continue the excess charge collection.

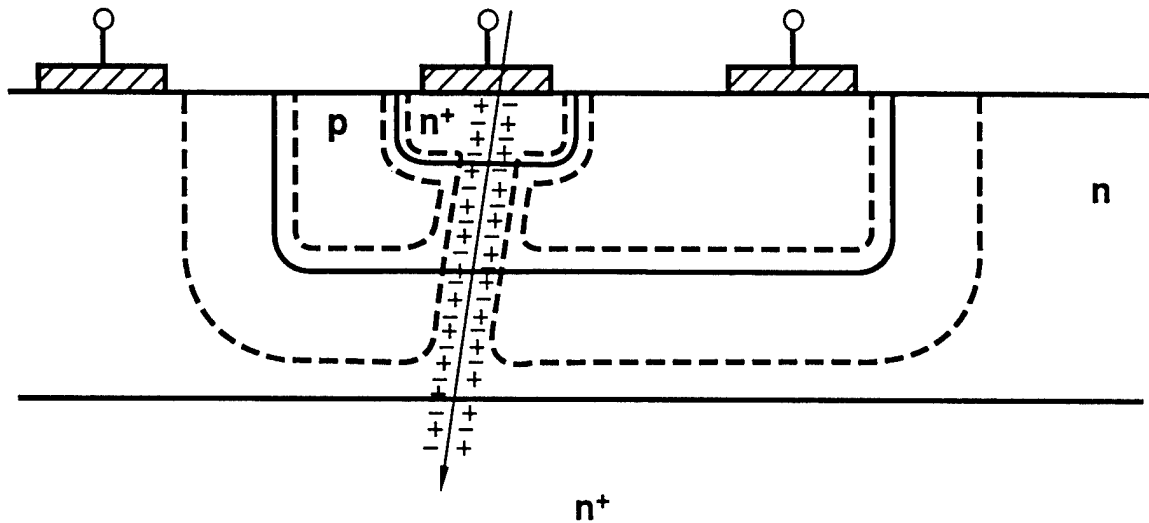


Figure 4.3. Illustration of the ion shunt effect where the high charge density along a track can connect device junctions (After [Kern-89]).

4.1.2 Mechanisms

There are a variety of single event effects which can be caused by single particles. These basic effects can be categorized as described below in Table 4.1.

Single particles can deposit enough charge on circuit nodes by the mechanisms described above to alter the logic state of the device, causing single event upset (SEU). In order to illustrate the SEU phenomenon, we will use a CMOS static random access memory (SRAM) as an example. An SRAM cell consists of cross-coupled inverters, as shown in Fig. 4.4. A particle striking a sensitive node of the device, e.g. the OFF n-channel transistor, can deposit enough charge to change the voltage on that node to what it would be in the opposite logic state. Whether a logic state upset occurs is then determined by whether the ON device (the p-channel transistor in this case) can restore the node to its "correct" voltage state before the feedback in the cell latches into the incorrect voltage state. The simulated evolution of voltage on the nodes for a strike which does not cause upset and one which does cause upset is shown in Fig. 4.5. In the case where the cell is not upset, there is a momentary disruption of the information in the cell (giving a SED - single event disturb).

Table 4.1. Types of Single Event Effects

Acronym	Definition	Description
SEU	Single Event Upset	Change of information stored
SED	Single Event Disturb	momentary disturb of information stored in memory bit
SET	Single Event Transient	current transient induced by passage of particle, can propagate to cause output error in combinational logic
SEGR	Single Event Gate Rupture	rupture of gate dielectric caused by high current flow
SEB	Single Event Burnout	destructive burnout caused by high current
SEL	Single Event Latchup	high current regenerative state induced in 4-layer device (latchup)
SES	Single Event Snapback	high current regenerative state induced in NMOS device (snapback)
MBU	Multiple Bit Upset	several memory bits upset by passage of same particle
SEFI	Single Event Functional Interrupt	corruption of control path by an upset

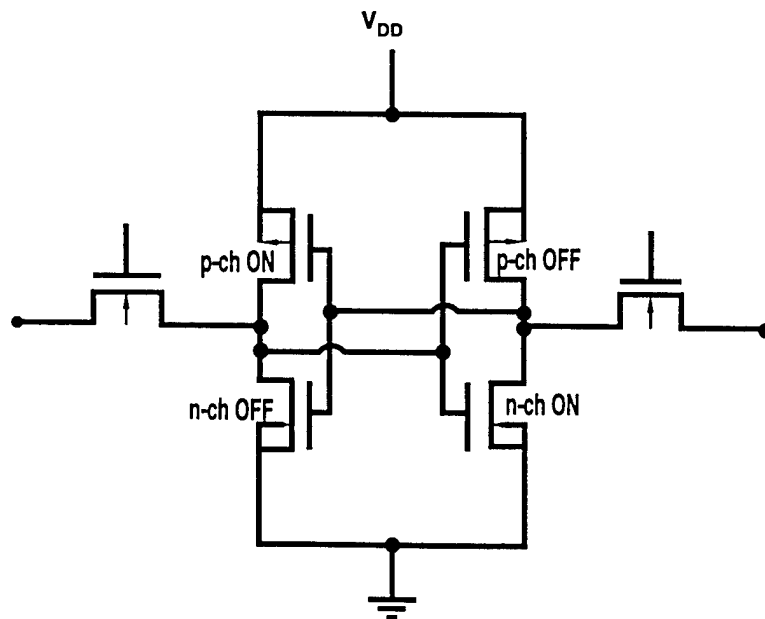


Figure 4.4. Schematic of a typical CMOS SRAM cell. The inverters on each half of the cell are biased in opposite directions, so that in each case one n-channel transistor and one p-channel transistor is ON and the other is OFF.

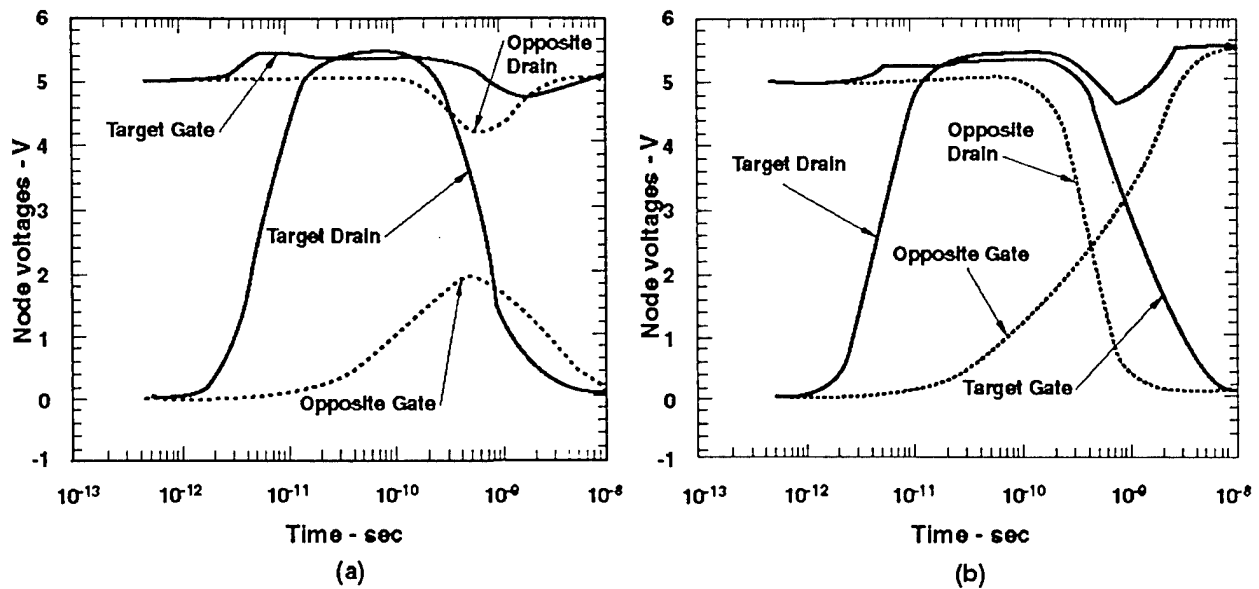


Figure 4.5. Simulated SRAM cell response for an ion strike (a) which does not cause upset and (b) for one which does cause upset. In (a) the ion hit changes the voltage on the struck node to the opposite state, but the node recovers to its original state (the disturbance does not fully propagate to the opposite side of the cell). In (b) the struck node does not recover and the memory cell voltages switch to the opposite state (After [Wood-93]).

It is also possible for single ions to cause “upset” or incorrect information in combinational or random logic. In this case the current or voltage spike (a SET - single event transient) can propagate through the circuitry to where it alters the stored state in a latch or causes an incorrect output state [Dieh-84, Li-84, May-84, Newb-90, Kaul-91, Leav-91, Baze-94, Buch-97]. This failure mode depends on the response time of the circuit being fast enough to respond to the “signal” generated by the ion’s passage, and thus may become more of a problem as circuit speeds increase in the future. It has also been observed in other high-speed circuitry, such as in analog devices [Koga-93, Nich-96, Turf-96] and in optical subsystems [LaBe-91, LaBe-93, Mars-96].

The typical way in which devices are characterized is to show the upset cross-section versus the LET of the incident ion. (The cross-section is determined by the number of errors generated by the particle beam divided by the fluence.) A representative example of this curve for a SRAM device is shown in Fig. 4.6. The critical LET is the minimum LET which will cause upset in the device, in this case $\sim 16 \text{ MeVmg}^{-1}\text{cm}^2$. The saturation cross-section is the maximum upset cross-section reached, and represents the total area of the device sensitive to upset (in this case $\sim 2 \times 10^{-3} \text{ cm}^2$).

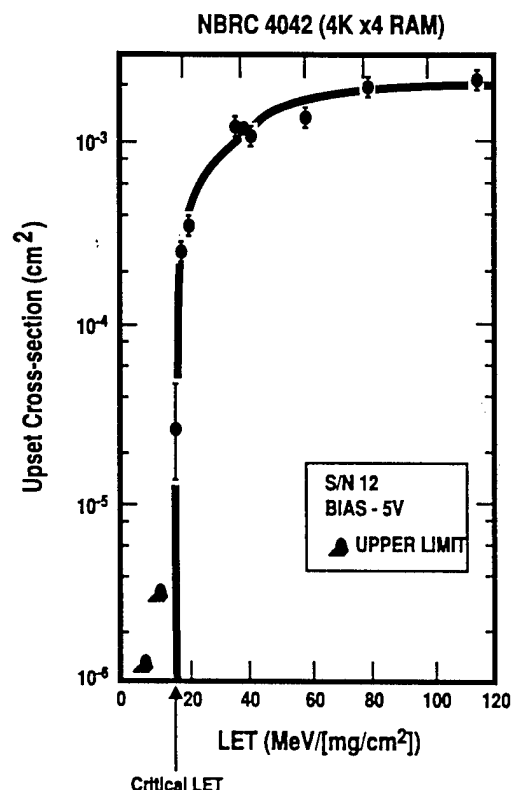


Figure 4.6. Single event upset curve for a static RAM showing upset cross-section versus ion LET (After [Koga-84]).

Whether a given circuit node will upset depends upon the total charge deposited and the time over which it is deposited. However, it has proved convenient to describe the sensitivity of a given circuit node by its critical charge (the minimum charge necessary to cause upset) as determined by computer simulations. Although this single number does not include any time information, it turns out to provide a fairly good measure of relative sensitivity (at least for the many circuits in which the circuit response time is longer than the primary charge pulse associated with the passage of the ion). The experimental measure of SEU sensitivity has typically been critical LET. Again this is not a strictly unique measure, since different ions with the same incident LET do not always produce the same charge distributions along the track, and thus may have different amounts of collected charge. The difference between charge track structures for Ag ions incident with 100 MeV and 1 GeV onto Si (both with an incident LET of $\sim 46 \text{ MeVcm}^2/\text{mg}$) is shown in Fig. 4.7. Given the large difference in carrier densities and extent, charge collection might be expected to be quite different for these two cases, particularly for small devices. In fact it has been shown that the LET concept breaks down for very small sensitive volumes and high-energy particles [Xaps-92]. However, critical LET has proved useful in general as a relative measure for characterizing circuit sensitivities. In this sense the concept of LET plays a similar role in describing ionizing energy deposition effects as does NIEL in displacement damage effects.

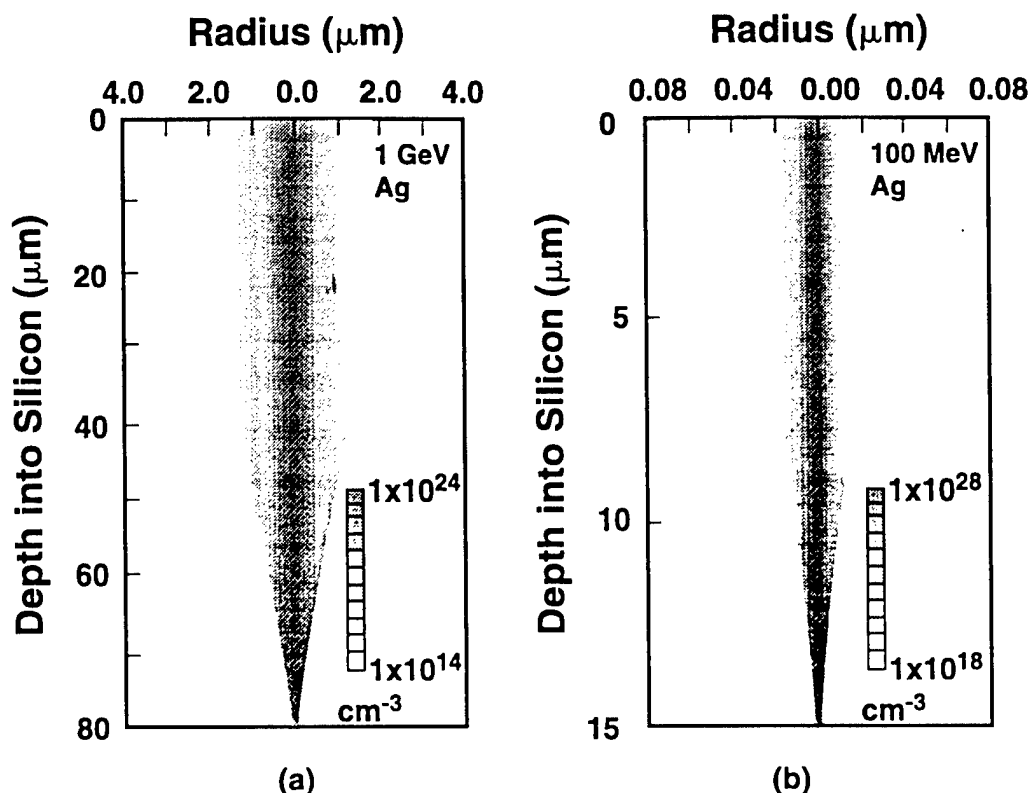


Figure 4.7. Ion track structure showing ion-induced carrier concentrations as a function of radius and depth for (a) 1 GeV and (b) 100 MeV Ag ions incident on silicon (Note the different scales in the two cases – the higher energy particle has much greater radius and depth, but a lower peak induced carrier concentration) (After [Dodd-96a]).

4.2 ENHANCEMENTS TO UNDERSTANDING

4.2.1 Dielectric Rupture - Single Event Gate Rupture (SEGR)

When a high electric field is imposed across a dielectric layer, and a high energy particle traverses that layer, the dielectric can undergo breakdown resulting in a permanent short-circuit through the dielectric [Wrob-87, Milg-90a, Milg-90b, Busc-92, Alle-96, Sext-97]. The field at which this breakdown occurs depends upon the LET of the incident ion, as shown in Fig. 4.8. The mechanism appears to be that the carriers generated by the particle in the dielectric create a conduction path, which at high electric fields can allow enough current to flow to create thermal runaway and damage to the dielectric.

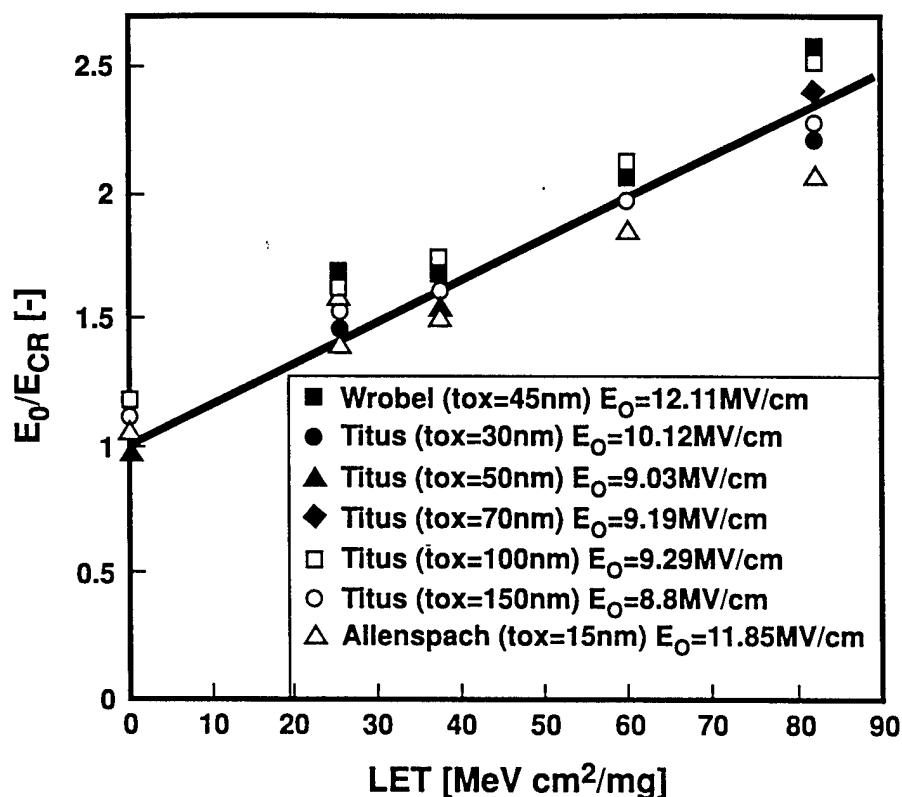
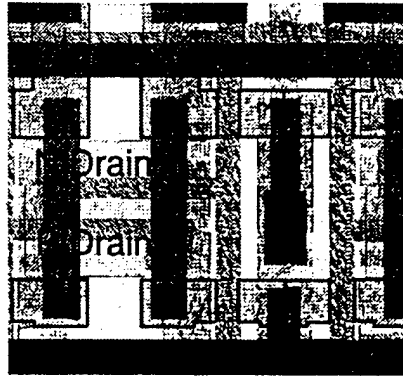


Figure 4.8. Critical oxide field for single event gate rupture in SiO₂ (normalized to the LET=0 value) as a function of LET. Data from different experiments from several workers using different oxides with different critical breakdown fields at an LET=0 are shown (After [Alle-96]).

4.2.2 Focused Beam Experiments

Additional insights and confirmation of models of SEU response in devices have been gained by focused beam experiments. These have been both heavy-ion microbeams formed by apertures or magnetically focused [Sext-96 and ref. therein], and by pulsed focused laser irradiation [Buch-88, Buch-90b, Goss-92, McMo-92, John-93, McMo-93, Buch-94, Meli-94]. In standard SEE testing, devices are flooded with a broad beam of accelerated particles, so that all devices and circuits on the integrated circuit are struck by ions. This configuration makes it difficult to conclusively identify the sensitive regions of the device and the mechanism(s) causing upset, particularly if several different mechanisms are possible. By using a focused beam, the area of a circuit or device struck by ions can be localized to submicron-sized regions. Such precision allows separation and identification of sensitive areas of the device and information on the upset mechanisms. Initial microbeam studies confirmed the field-funneling effect [Knud-82, Camp-83] and bipolar amplification or ion shunt mechanisms [Knud-84, Haus-85, Knud-86, Knud-87]. The effects on sensitive area for SEU from changes in V_{DD} , the incident ion, and site on the chip of the ion strike have also been observed in microbeam experiments [Bara-98]. An example of the identification of the regions of a 16-k SRAM cell sensitive to SEU is shown in Fig. 4.9.

Mask
Layout



Upset
Image

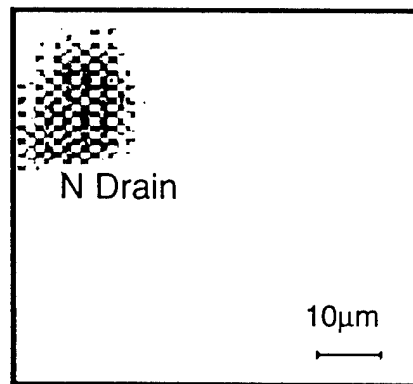


Figure 4.9. Microbeam image showing the regions of a 16-kbit CMOS SRAM cell sensitive to single event upset. The mask layout of the memory cell is shown for comparison (After [Horn-92]).

4.2.3 Simulation Results

A great deal of insight into the detailed mechanisms of SEE has been gained by device and circuit simulation. Much of this work had been based upon 1-D, 2-D, or quasi-3-D simulations [Hsie-83, Dodd-96a and references therein]. Although a number of useful results were obtained, with the advent of commercially available 3-D simulators which can run on high-end workstations, further progress and better accuracy is expected [Dodd-96a]. An example of the differences found in something as basic as depletion-region widths for simulators of different dimensionality is shown in Fig. 4.10; a difference of 1 μm in width between the one- and three-dimensional simulations is shown. A comparison of 2- and 3-D simulations of charge collection from an ion strike showed significant quantitative differences in both magnitude and time of the current response [Kres-86]. Such differences are certain to be accentuated as devices move to smaller geometries.

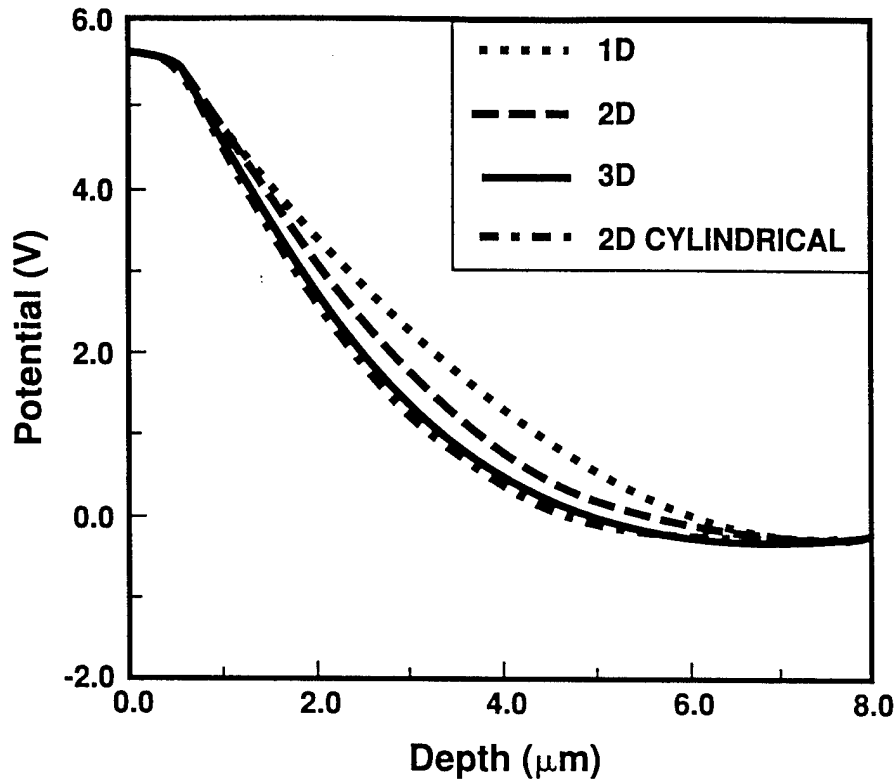


Figure 4.10. Electrostatic potential as a function of distance from the junction in a silicon diode as simulated using one-, two-, and three-dimensional codes (After [Dodd-96a]).

Simulations have been used to elucidate some expected trends in SEU phenomena [Dodd-96b]. For example, historically the most sensitive node in CMOS SRAM cells has been the OFF-drain of transistors outside the well. This may change in the submicron regime for some new technologies to inside-the-well OFF strikes. This switch could occur because the bipolar enhancement to charge collection increases at the smaller-feature-size technologies [Wood-93, Vela-94].

In general the advanced three-dimensional simulations show the increased complexity of modeling SEE in advanced device structures, so that intuitive analytical approaches may no longer be viable [Take-86, Duss-93, Oshi-93, Wood-93, Dodd-94, Vela-94, Dodd-95, More-95, Dodd-96a]. In fact, 3-D simulations of MOSFETs with 0.3 μm gate lengths have shown a new charge collection mechanism [Vela-94]. Immediately after an ion strike the field lines in the channel region were significantly perturbed so that the potential barrier between source and drain no longer existed and in fact a potential gradient was established between source and drain. This situation allowed a significant current flow, similar to that when the transistor was turned ON, as shown in Fig. 4.11. This elimination of the potential barrier by the ion strike does not occur in the longer 1.2 μm device.

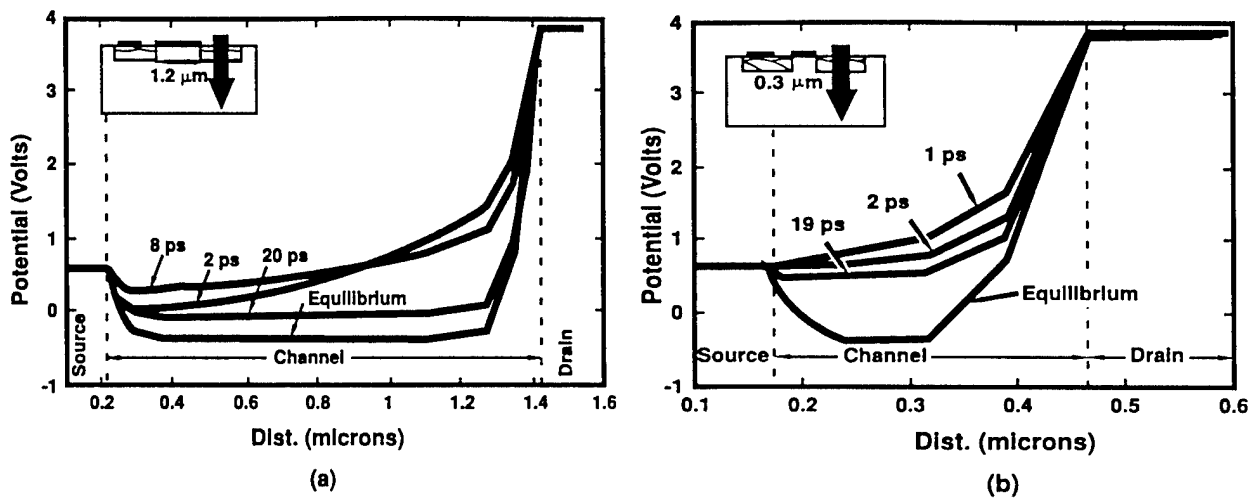


Figure 4.11. Potential distribution along the channel of a MOSFET for various times after an ion hit in the drain region. (a) 1.2 μm channel device (b) 0.3 μm channel device. Note that for the 0.3 μm device the potential barrier between source and drain does not exist for short times after the ion strike (After [Vela-94]).

Another area where simulations have proved useful is in analyses of the effects of angle of incidence on device upset sensitivities. For example, three-dimensional simulations have shown that in CMOS SRAM cells, ion paths directed towards the source of the n-channel pull-down transistor will cause upset at a lower value of LET than for paths directed away from the source [Wood-93]. Monte Carlo simulations have provided insight into the conditions under which the angle of incidence of proton strikes can play a role in device sensitivity [Akke-98].

A detailed discussion of SEE simulation is outside the scope of this work. For further information, the reader is directed to [Dodd-96a, Detc-97, Dodd-97] and references therein.

4.3 DEVICE IMPLICATIONS

4.3.1 Power MOSFETs

Two kinds of SEE damage have been observed in vertical power MOSFETs. These are single event burnout (SEB) and single event gate rupture (SEGR). They can result in degraded performance or catastrophic failure in these devices.

A diagram of a typical double diffused MOS (DMOS) vertical n-channel transistor as used in a power MOSFET is shown in Fig. 4.12. A heavy ion passing through the device can generate transient currents sufficient to turn on the parasitic bipolar transistor consisting of the n^+ source as the emitter, the p-body as the base, and the n-epi as the collector. The high fields present in the p-base/n-epi region allow a regenerative feedback mechanism via impact ionization to increase collector currents to the point where the device burns out. More detailed descriptions of the mechanisms are available in [Titu-96 and references therein]. Supporting

these models of SEB are data as follows: (1) the SEB sensitivity decreases with increasing temperature [Wask-90, John-92, Nich-93, Tast-93] since the impact ionization coefficient decreases with increasing temperature; (2) applied gate voltage has little effect on SEB sensitivity (Wask-90, Nich-93), as expected for a bipolar effect; (3) SEB of p-channel power MOSFETs is less likely since the impact ionization coefficient for holes is much less than that for electrons, and has not been reported in the literature [Fisc-87, John-96b].

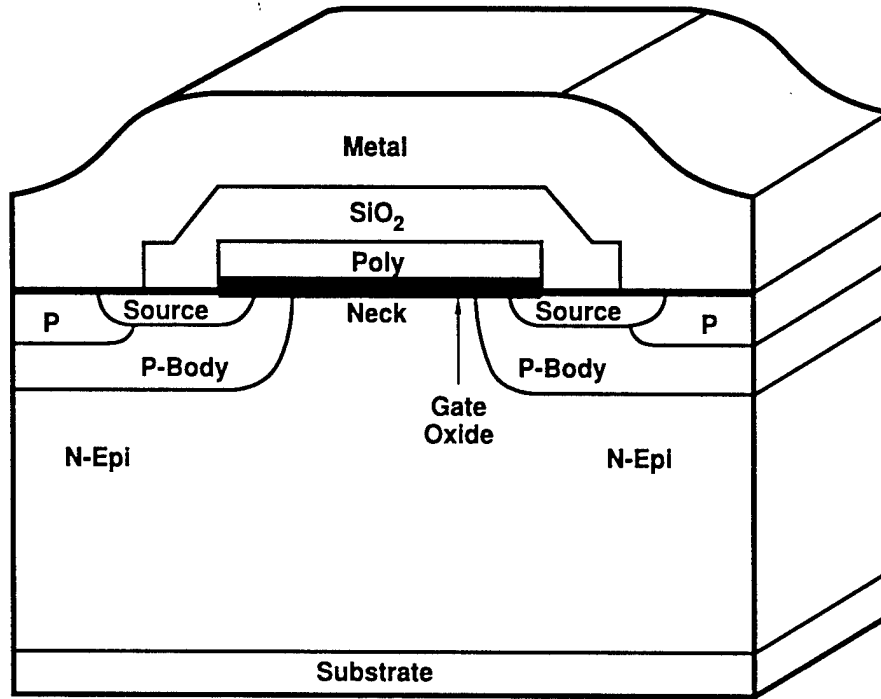


Figure 4.12. Schematic diagram of a vertical n-channel DMOS transistor showing the various regions of the device structure (After [Titu-96]).

The mechanism for single event gate rupture is illustrated in Fig. 4.13. After an ion strike, electrons are drawn towards the positively biased drain and holes are drawn towards the negatively biased (or grounded) gate. The holes at the interface increase the electric field in the oxide in a local region (effectively "transferring" a fraction of the drain voltage to the interface) for a brief period of time (as shown in Fig. 4.14). When added to the DC field already existing in the oxide, this field can be sufficient to exceed the breakdown field in the oxide, causing SEGR. The dependencies of SEGR on gate-source voltage V_{GS} , drain-source voltage V_{DS} , ion LET, and oxide thickness t_{ox} are intertwined; in one study the following relation was found [Titu-96],

$$V_{GS} = (0.87)(1 - \exp[-LET/18])(V_{DS}) - \frac{(1 \times 10^7)(t_{ox})}{1 + LET/53} \quad (4.2)$$

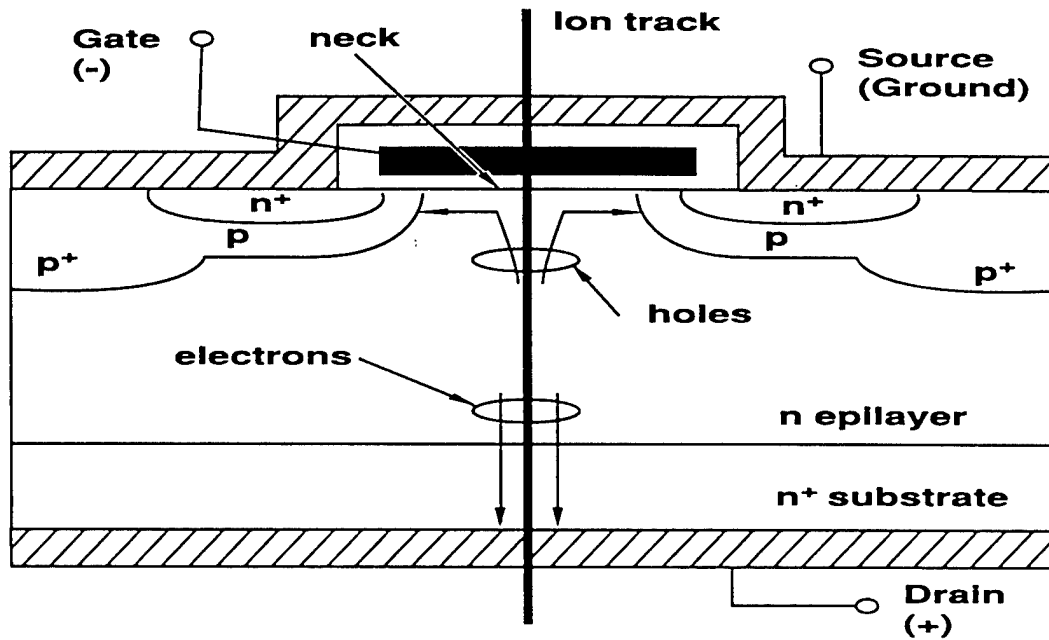


Figure 4.13. Illustration of the mechanism for SEGR in a power MOSFET. Charge builds up in the neck region after a heavy ion strike (holes piling up at the oxide interface and electrons transporting down to the positively biased drain). This increases the electric field in the gate oxide region (After [John-96b]).

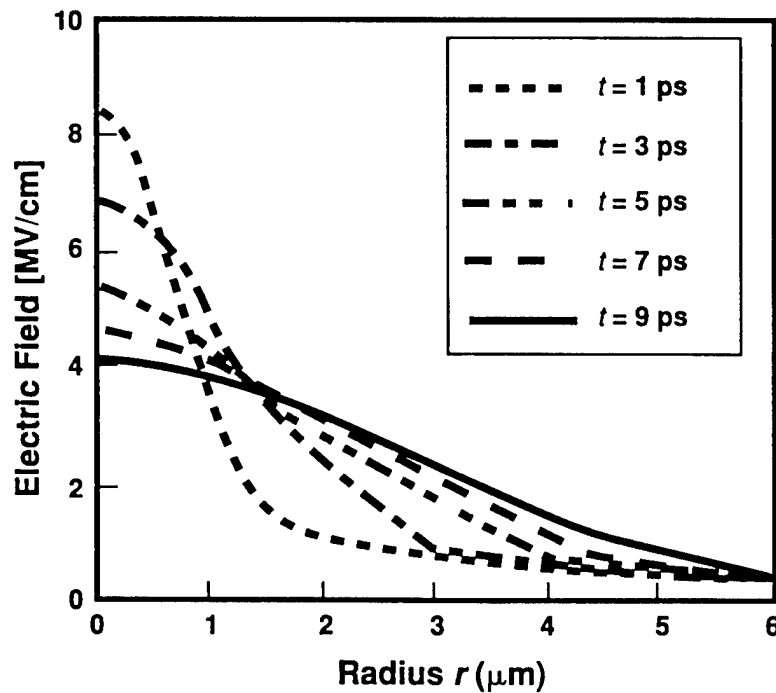


Figure 4.14. Electric field across the gate oxide in a power MOSFET versus radial distance from the ion track for varying times after the strike (values obtained from a charge-sheet model) (After [John-96b]).

(LET in this equation is in units of $\text{MeVmg}^{-1}\text{cm}^2$ and t_{ox} is in centimeters.) The coefficient of V_{DS} on the right-hand side shows the substrate's response to the ion and gives the fraction of the drain-source bias which appears across the gate oxide. The second term on the right-hand side gives the oxide's response to the ion and describes the bias needed to cause breakdown in the absence of a drain-source bias. Fig. 4.15 illustrates the applicability of this equation to a set of vertical power MOSFETs of identical process and design parameters but with varying oxide thickness.

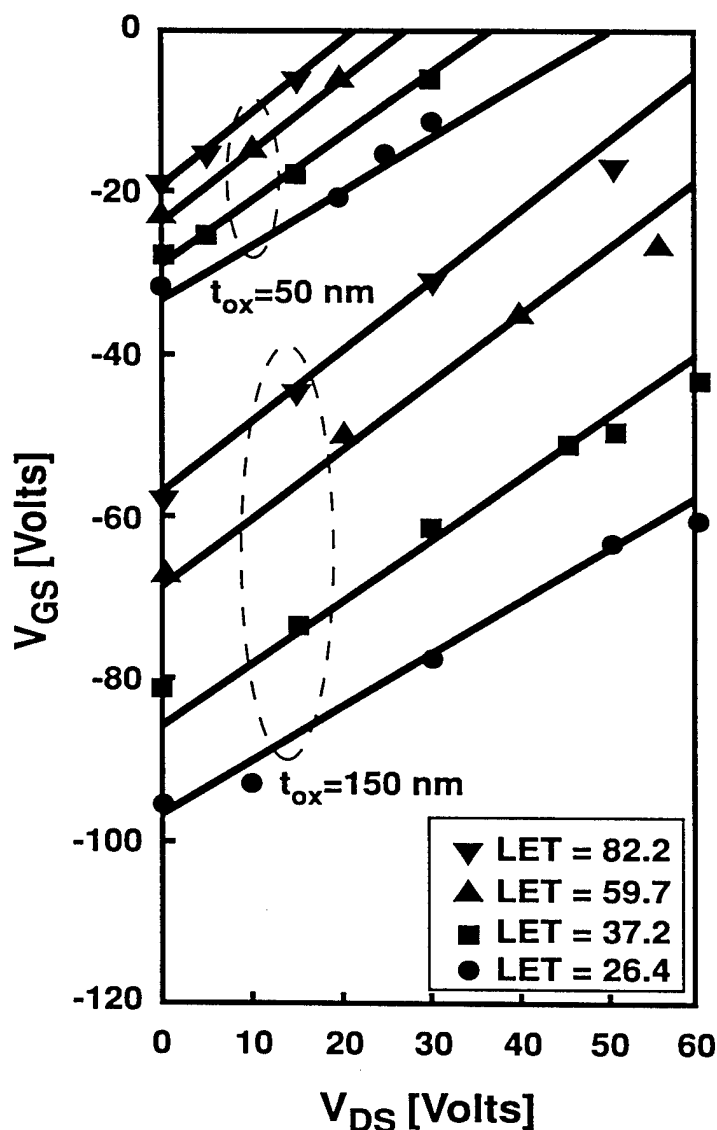


Figure 4.15. Measured SEGR response of vertical power MOSFETs with different gate oxide thicknesses at different LET conditions. Lines represented calculated results based on Eqn. (4.2) (After [Titu-96]).

It should again be noted that although most reports of gate rupture from single ions have been associated with power MOSFETs, the phenomenon has been observed in other devices

where high electric fields can be applied, such as nonvolatile memories [Pick-85], MOS capacitors [Wrob-87, Milg-90a, Milg-90b, Busc-92, Sext-97], SRAMs [Sext-97], field programmable gate arrays [Swif-95, Katz-97], and perhaps DRAMS [Swif-94]. A similar type of failure has been observed in amorphous silicon antifuses [Katz-97].

4.3.2 High Current States

Latchup is the activation of a parasitic four-layer SCR (semiconductor controlled rectifier) structure in devices which leads to a low-resistance, high-current state. It can be initiated by single ionizing particles impinging on a device structure. The classic model for latch-up is illustrated in Fig. 4.16. A heavy ion impinging on the structure creates a transient current that flows from the well contact to the substrate contact. This current causes a voltage drop within the well (and within the substrate) which can forward bias the parasitic vertical pnp transistor (or lateral npn transistor). This in turn will cause a larger current to flow from the p^+ source to the substrate (or from the n^+ source to the well), which can then cause a larger voltage drop within the substrate (or within the well). This voltage drop may forward bias the lateral npn transistor (or vertical pnp transistor). If the gains of the transistors and parasitic resistances are sufficiently high, the structure can enter into the regenerative feedback condition representative of the low-resistance latchup state.

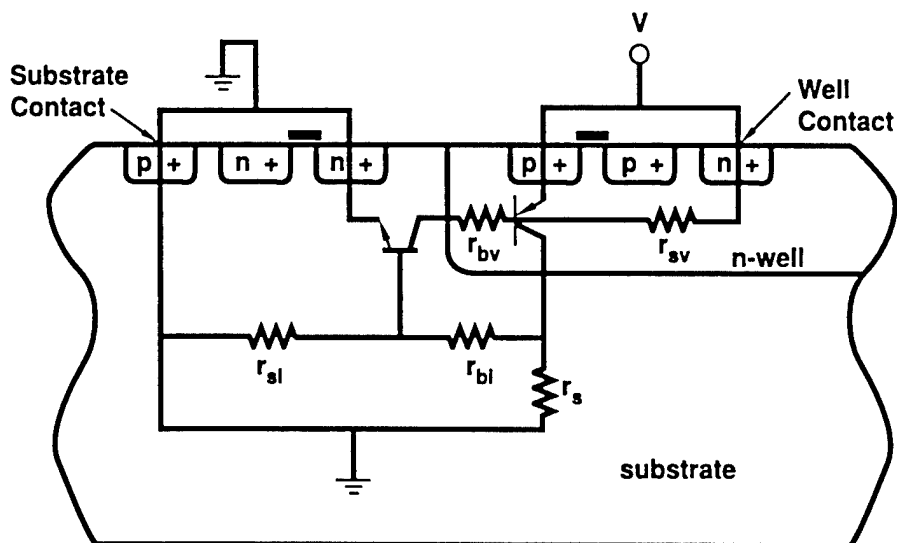


Figure 4.16. The two transistor model for latchup in an n-well CMOS device showing the parasitic elements of importance (After [John-96a]).

It should be noted that the time scale for latchup is significantly different from that of single event upset. In the former, the time scale is determined by the base transit times of the bipolar transistors, and is typically of the order of tens of nanoseconds. Thus diffusion currents (which occur over much longer times than drift currents) can be very important in initiating latch-up. In the latter, times over which charge collection is important are much shorter, so that diffusion currents are usually not a significant component [John-96a].

There are two other related high-current phenomena which can be initiated by single particles. Snapback [Sun-78, Hsu-82, Ocho-83, Beit-88] occurs in n-channel transistors when minority-carrier injection from the source junction reduces the avalanche breakdown voltage at the drain junction. The parasitic bipolar transistor formed by the source, substrate, and drain amplifies this injected current. It leads to a negative resistance region in the drain current-voltage characteristics. This effect has been observed in heavy ion experiments [Koga-89].

Second breakdown is a phenomenon which can occur in bipolar structures from localized heating in the reverse-biased base-collector junction [Sze-69]. A mesoplasma forms which allows a high current to flow in the small region of the mesoplasma, leading to a large drop in the breakdown voltage of the device. This also produces a negative resistance effect in the current-voltage characteristics. An effect apparently of this origin triggered by ions in a bipolar analog circuit has been observed [Koga-94].

4.3.3 Other Trends

Silicon-on-insulator (SOI) technology has advantages for radiation-hardened electronics and also for small-feature-size devices. The buried insulator limits the region from which charge can be collected for a given ion strike compared to bulk devices. Thus one might expect the sensitivity to SEU to be less for devices on SOI substrates. However, the charge deposited in the silicon region may be enough to cause minority carrier injection across the source-body junction, which can then activate a parasitic bipolar action between the source and drain [Alle-90, Kern-90, Mass-90]. This parasitic bipolar current can enhance the effect of the ion hit, leading to an increased sensitivity over what it would otherwise be. This current enhancement is illustrated in Fig. 4.17. (There are techniques for suppressing this bipolar current, such as by shorting the island body to the transistor source.)

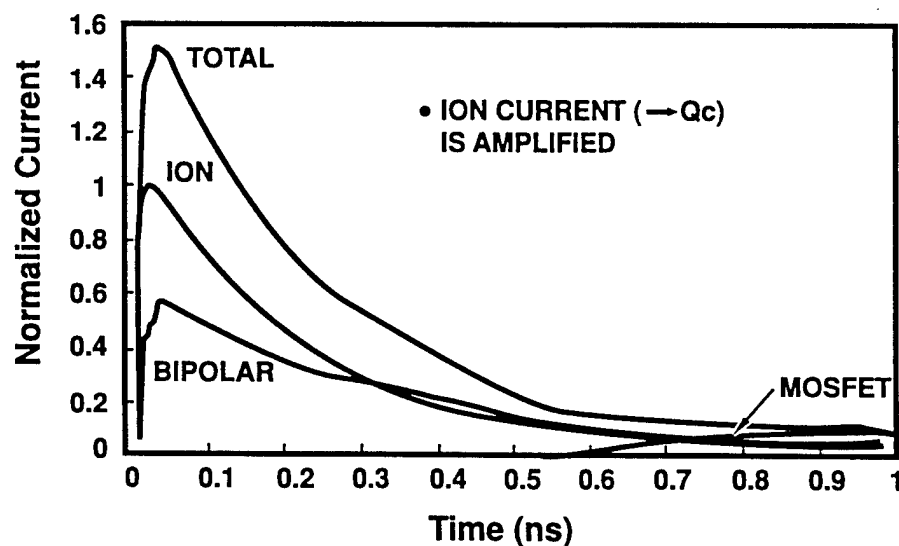


Figure 4.17 Currents which discharge the node during an ion hit on an SOI transistor. The current from charge collection from the ion track itself, and the current from parasitic bipolar action are shown (After [Kern-90])

5.0 ADDITIONAL IMPLICATIONS FOR THE NEXT MILLENNIUM

5.1 Scaling Background

The continuing increase in performance and capabilities of microelectronics has been made possible by the scaling of devices, where the dimensions of the transistors and the various elements of the device structure are reduced in such a way as to try to preserve the electric field patterns in the device [Denn-74]. Although initially such scaling was based upon maintaining either constant voltage or constant electric field [Denn-74, Bach-84], as feature sizes have continued to shrink the "rules" for scaling have become more flexible and varied [Dava-92, Hu-93, Fieg-94, Dava-95, Taur-95, Dava-96, Hu-96, Asai-97, Taur-97]. An example of the progression of feature sizes and performance expected for two scaling scenarios (high performance and low power) is given in Table 5.1 [Dava-96]. For this discussion we will not go into the many details of scaling, but rather focus on those areas which are likely to impact radiation response based upon our earlier discussions of basic mechanisms.

Table 5.1: CMOS Scaling Guidelines

Parameter	Late 80's	1992	1995	1998	2001	2004
Supply Voltage (V)						
High Performance	5	5/3.3	3.3/2.5	2.5/1.8	1.5	1.2
Low Power	--	3.3/2.5	2.5/1.5	1.5/1.2	1.0	0.8
Lithography Resolution (μm)						
General	1.25	0.8	0.5	0.35	0.25	0.18
Gate Level for Short L	--	0.6	0.35	0.25	0.18	0.13
Channel Length (μm)	0.9	0.6/0.45	0.35/0.25	0.2/0.15	0.1	0.07
Gate Insulator Thickness (nm)	23	15/12	9/7	6/5	3.5	2.5
Relative Density	1.0	2.5	6.3	12.8	25	48
Relative Speed						
High Performance	1.0	1.4/2.0	2.7/3.4	4.2/5.1	7.2	9.6
Low Power	--	1.0/1.6	2.0/2.4	3.2/3.5	4.5	5.8
Relative Power/Function						
High Performance	1.0	0.9/0.55	0.47/0.34	0.29/0.18	0.12	0.077
Low Power	--	0.27/0.25	0.20/0.09	0.08/0.056	0.036	0.027
Relative Power-Density						
High Performance	1.0	2.25/1.38	3.0/2.1	3.7/2.34	3.12	3.70
Low Power	--	0.7/0.63	1.25/0.6	1.02/0.72	0.90	1.00

Fig. 5.1 shows the trends of power supply voltage, threshold voltage, and gate oxide thickness versus channel length for CMOS logic technologies as collected from published data over recent years. The leveling off of nominal threshold voltage at $\sim 0.3\text{V}$ at operating temperature of 100°C occurs to minimize subthreshold leakage and maintain circuit noise

immunity [Dava-95, Dava-96, Taur-97]. Since minimization of CMOS circuit delays requires that V_t/V_{dd} be less than $1/4$ [Fieg-94, Taur-95], this in turn limits the minimum V_{dd} to $\sim 1.2V$. However, the gate oxide thickness continues to decrease in order to minimize short channel effects, so as can be seen the average electric field in the gate oxide will tend to increase approaching 5 MV/cm for the 0.1 μm channel length devices. It should be noted here that, in contrast to Fig. 5.1, the National Technology Roadmap for Semiconductors projects a continually decreasing power supply voltage, going below 1.2V around 2006 and reaching $\sim 0.5V$ in 2012 [NTRS-97]. However, the roadmap also states that there is no currently known solution to make technologies with these desired characteristics. The data of Fig. 5.1 represents what is possible (and some of the limitations) with current approaches.

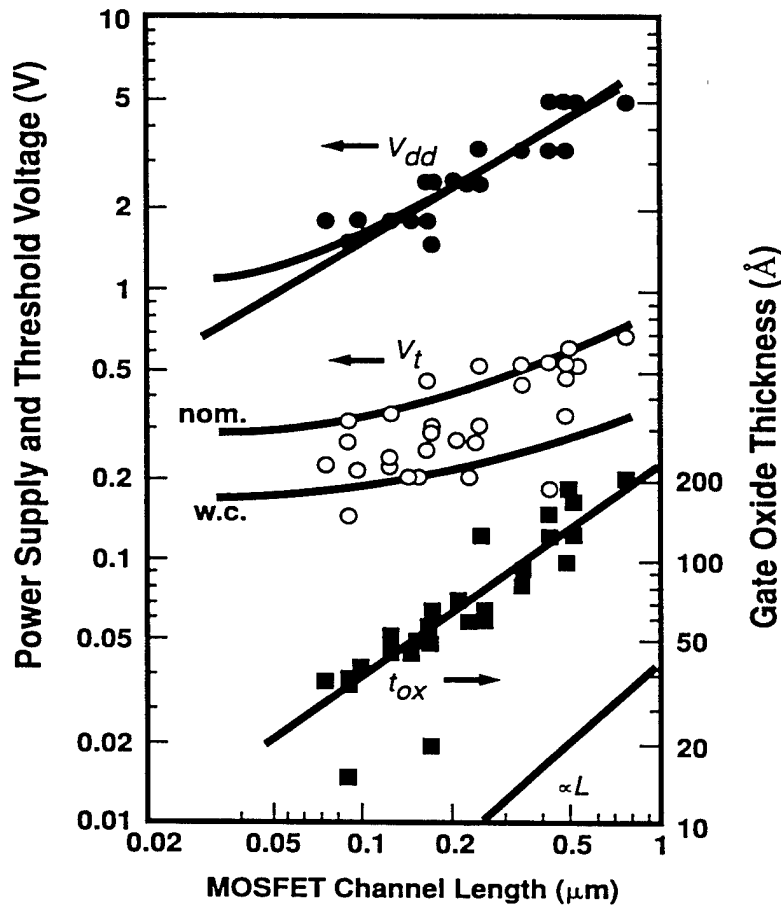


Figure 5.1. Trends in power supply voltage (V_{dd}), threshold voltage (V_t) for both nominal and worst-case (w.c.) values, and gate oxide thickness (t_{ox}) as a function of channel length in CMOS technologies as published in recent years. The leveling off of nominal threshold voltage at $\sim 0.3V$ at operating temperature of $100^\circ C$ occurs to minimize subthreshold leakage and maintain circuit noise immunity. A line showing a trend which would scale directly with channel length (L) is also shown (After [Taur-97]).

There have been a number of items identified as potential issues as feature sizes continue to decrease. One of these is that as gate oxide thickness decreases, quantum-mechanical

tunneling of electrons through the oxide can give rise to gate leakage currents. However, it has been shown that this is likely not a major concern for high performance devices until the oxide thickness reaches the range of 1.5-1.8 nm [Taur-97]. For devices such as DRAMs which are more sensitive to leakage currents, the minimum oxide thickness limit from tunneling currents may be somewhat higher, approximately 3 nm [Hu-96]. In many cases the lower limit of oxide thickness may be set by long-term reliability considerations. These dictate that the maximum oxide electric field be 7-8 MV/cm [Hu-97]; however, defect density considerations reduce this to a practical limit of ~5MV/cm [Dava-95, Dava-96, Hu-97].

There are other concerns associated with very thin silicon dioxide layers as the gate dielectric. These include boron diffusion from p^+ -polysilicon gate electrodes leading to poor threshold voltage control, increased subthreshold voltage swing, and degraded oxide reliability, and degradation of oxide reliability from implantation-induced substrate damage [Lin-96]. Nitrided oxides, reoxidized nitrided oxides, and oxynitrides have improved properties in these areas [Manc-93, Lin-96], making them potentially attractive for deep submicron devices. Other alternative dielectrics are also being considered.

In order to avoid the performance penalties associated with the nonscaling of threshold voltage, alternative circuit configurations and device structures have been proposed [Dava-95, Taur-95, Asai-97]. These include the use of multiple threshold voltages on a single chip [Dava-95, Asai-97, Taur-97] and devices which actively change threshold voltage by altering the back-gate bias [Dava-95, Asai-97].

Additional improvements in power and/or performance can be achieved by using SOI substrates. This reduces parasitic capacitances and the body effect, and can lead to factors of 1.3-2 improvement in circuit speed [Dava-95, Taur-95, Dava-96, Asai-97, Taur-97].

As device features approach the sub-0.1 μm regime, the number of dopant atoms in the depletion layer under the gate can be of the order of hundreds. At this level the discrete nature of the charge on the dopant atoms can become significant, leading to fluctuations in the threshold voltage and subthreshold slope for devices [Wong-93, Taur-95, Asai-97]. The variation depends upon gate length, as shown in Fig. 5.2. This potential problem can be avoided by changing the device structure (e.g., using a double-gated MOSFET [Taur-95]) or by using alternative doping profiles (such as an extreme retrograde profile [Taur-97] or undoped channel regions [Asai-97]).

5.2 Hardness Implications

With the above scaling background and the previous discussions of basic mechanisms, a number of observations about likely hardness trends/issues for the next millennium can be made.

One of the primary trends in scaling is the move towards shorter channel lengths. There have been a number of reports investigating whether there is any dependence of the radiation response of MOS devices on channel length. Several studies have shown little or no dependence [Yuan-77, Chen-81, Chen-82, Peck-82], whereas others have shown increased or decreased threshold voltage shifts as channel length decreases [Shar-75, Kim-82, Huan-85, Schr-85, Bhat-

90, Scar-92, Shan-93]. Transistors from different processes have shown different effects. An example of the dependence seen is illustrated in Fig. 5.3. In this case the n-channel threshold

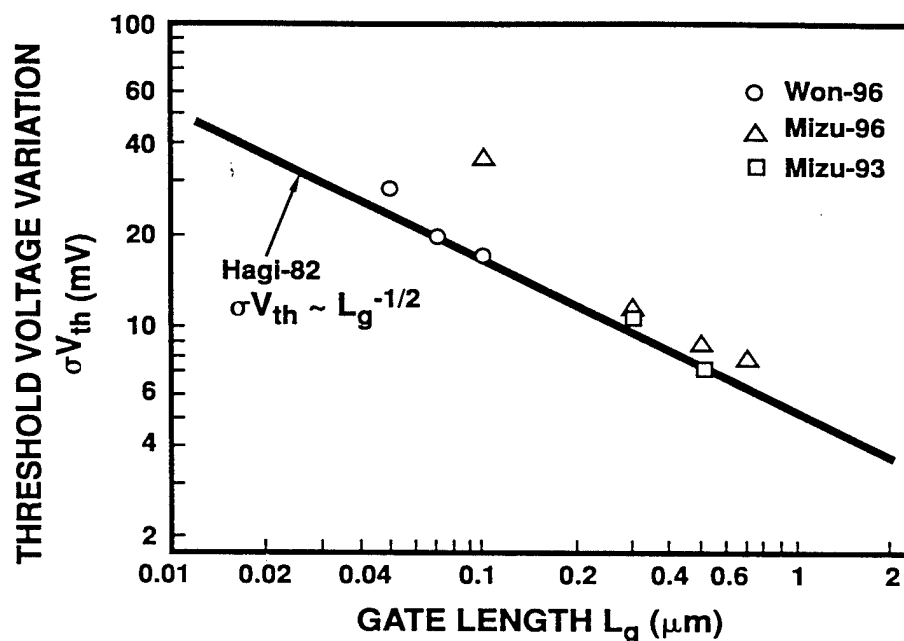


Figure 5.2. Standard deviation of threshold voltage variation caused by dopant fluctuations as a function of channel length. Points show data from several workers, solid line is a calculated value based on a model showing that this variation should depend upon the inverse square root of channel length (After [Asai-97]).

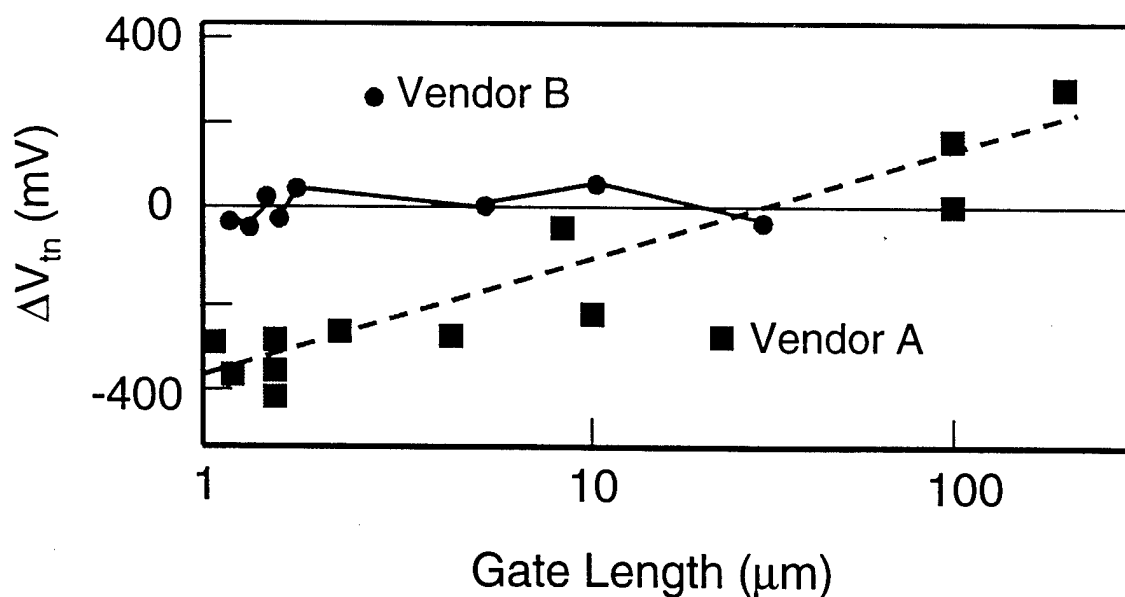


Figure 5.3. Radiation-induced threshold voltage shift of n-channel transistors as a function of channel length for devices fabricated by two different processes (After [Scar-92]).

voltage shift post-irradiation becomes more negative (for one process) as the channel length is reduced. This was due to reduced interface-trap charge in the shorter channel devices, as shown in Fig. 5.4. The geometric dependence of interface traps appeared to be related to stress in the oxides, the larger devices experiencing a greater tensile stress and thus more radiation-induced interface traps [Scar-92]. The interface-trap charge also led to smaller threshold voltage shifts in p-channel devices as the channel length decreased (Fig. 5.5). It should be noted that in other studies, the increased shift in n-channel devices was attributed to an increase in oxide-trapped charge as the channel length decreased [Shan-93]. For processes which show an increased shift as channel lengths decrease, scaling may not improve total dose hardness as much as expected. In addition, the fact that ICs also can contain transistors of different channel lengths also can impact both characterization and prediction of device response in different radiation environments.

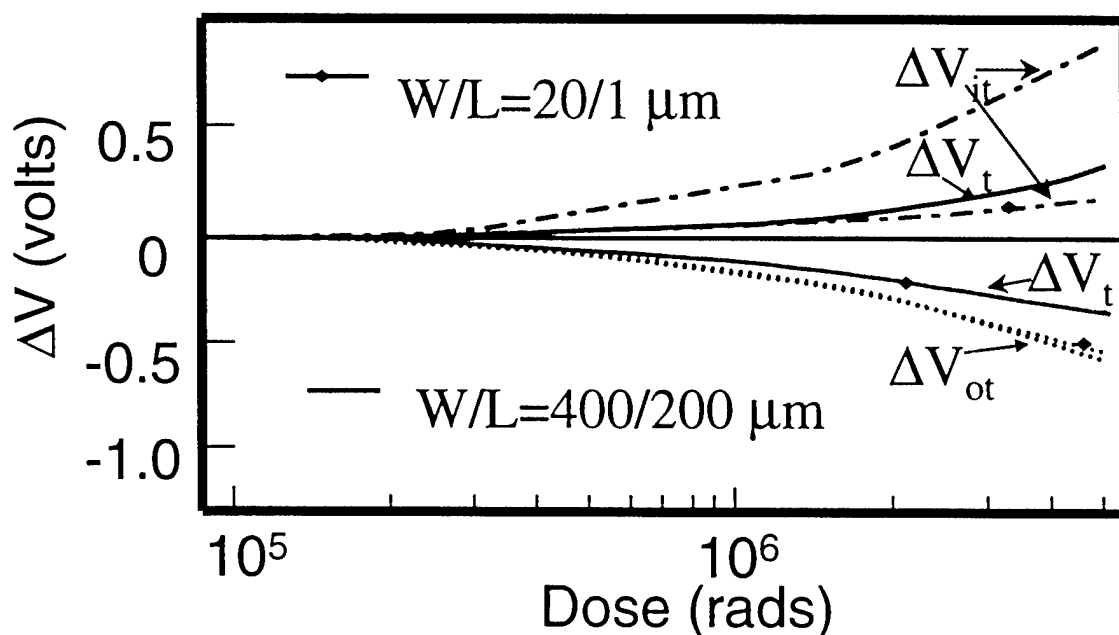


Figure 5.4. Components of radiation-induced charge in n-channel transistors of two different channel lengths showing greatly enhanced interface-trap buildup in the longer channel devices (After [Scar-92]).

As mentioned in section 2.3.2, for gate oxides thinner than 10 nm hole trapping and radiation-induced interface trap buildup decrease markedly. Thus for the highly scaled devices with gate oxides of 3-8 nm, hole trapping and interface traps are not likely to prove to be a major concern for the gate oxide in a radiation environment. The question of whether border traps may still cause device instability is not yet definitively answered. It should be noted, however, that even in highly scaled technologies there will be isolation dielectric layers which are still relatively thick. In a radiation environment these regions will continue to have appreciable hole trapping and interface trap buildup, which can lead to leakage and surface recombination currents. There may also be special circuits which control higher voltages (such as charge pumps

in flash memories) and thus have thicker gate oxides; these devices could still be affected by oxide-trapped charge and interface traps.

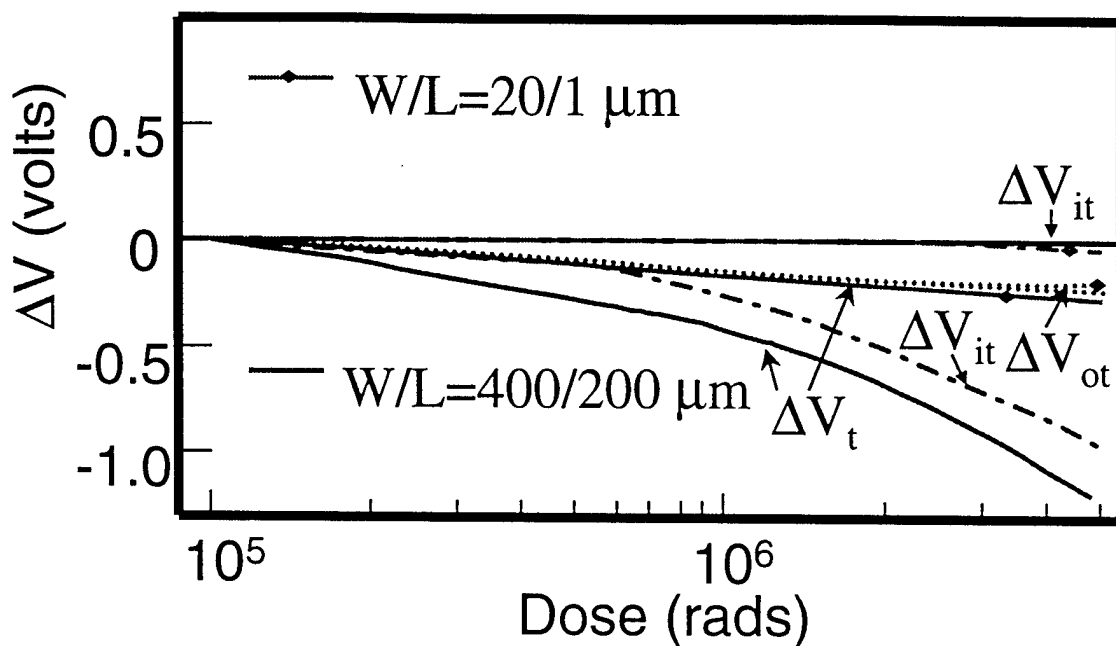


Figure 5.5. Components of radiation-induced charge in p-channel transistors of two different channel lengths showing greatly enhanced interface-trap buildup in the longer channel devices (After [Scar-92]).

Projections indicate that for highly scaled technologies the electric fields may be in the range of 5 MV/cm. From Eqn. (4.2) above and other similar data, this would imply that particles with an LET of $\sim 50 \text{ MeVmg}^{-1}\text{cm}^2$ could possibly cause gate rupture in such devices. However, there are data which show that the critical oxide field for breakdown increases as the oxide thickness decreases (Fig. 5.6). In contrast, there also exists data which show lower breakdown fields for thin oxides than those shown in Fig. 5.6 [John-98]. Thus if the scaling trends for oxide field and gate oxide thickness follow those predicted [Dava-92, Hu-93], the impact on ion-induced breakdown for advanced devices is not clear. It is possible that this failure mode could become a concern, in particular depending on device processing, but further work is necessary to definitively answer this question.

The possible use of SOI substrates for high performance or low power applications also raises additional possible leakage paths. These are illustrated in Figure 5.7, where the three oxides of interest are shown – the gate oxide, the sidewall oxide, and the buried (isolation) oxide. The sidewall oxide may be thicker than the gate oxide and thus show a larger response to radiation. The buried oxide can trap charge just as does the field oxide in a bulk technology, and can contribute a “back channel” leakage to the normal device current. (Trapped charge in the buried oxide can also cause changes in threshold voltage for fully depleted devices.) An example of parasitic currents in an SOI device are shown in Fig. 5.8.

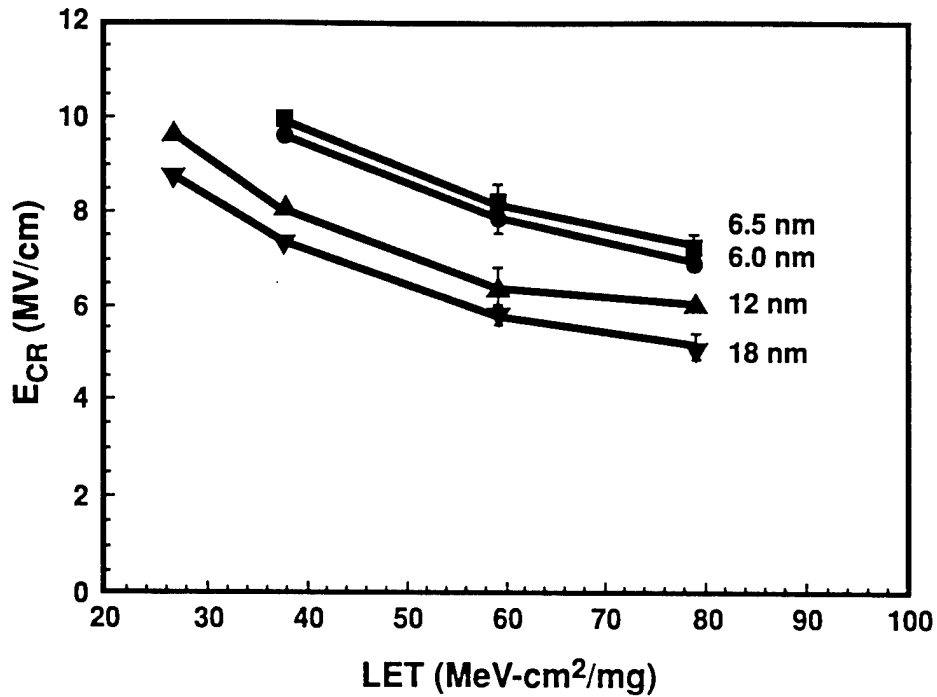


Figure 5.6. Critical oxide field for SEGR as a function of ion LET for various gate oxide thicknesses. In this data the breakdown field increases significantly for the thin oxides (After [Sext-97]).

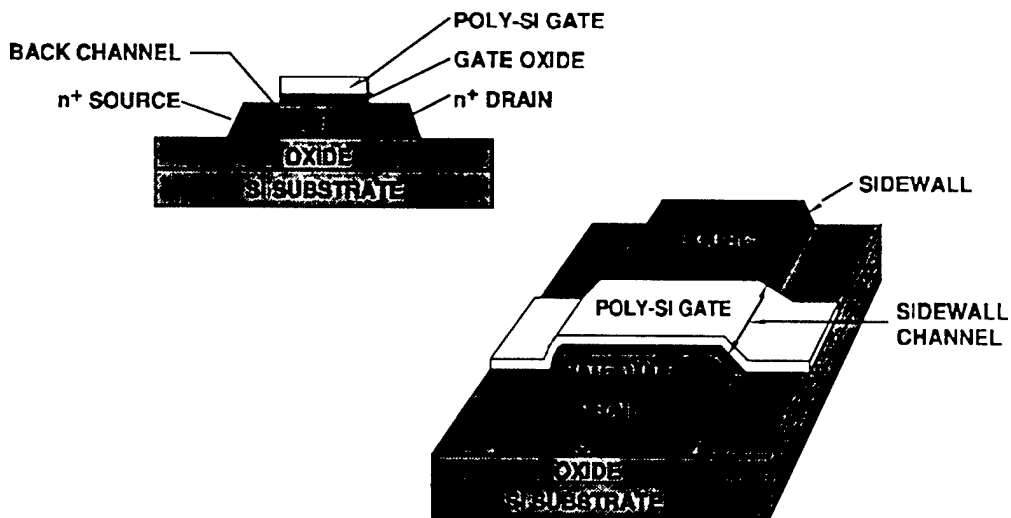


Figure 5.7. Schematic of an SOI transistor showing possible current leakage paths along the sidewall and along the back oxide interface (After [Dres-89]).

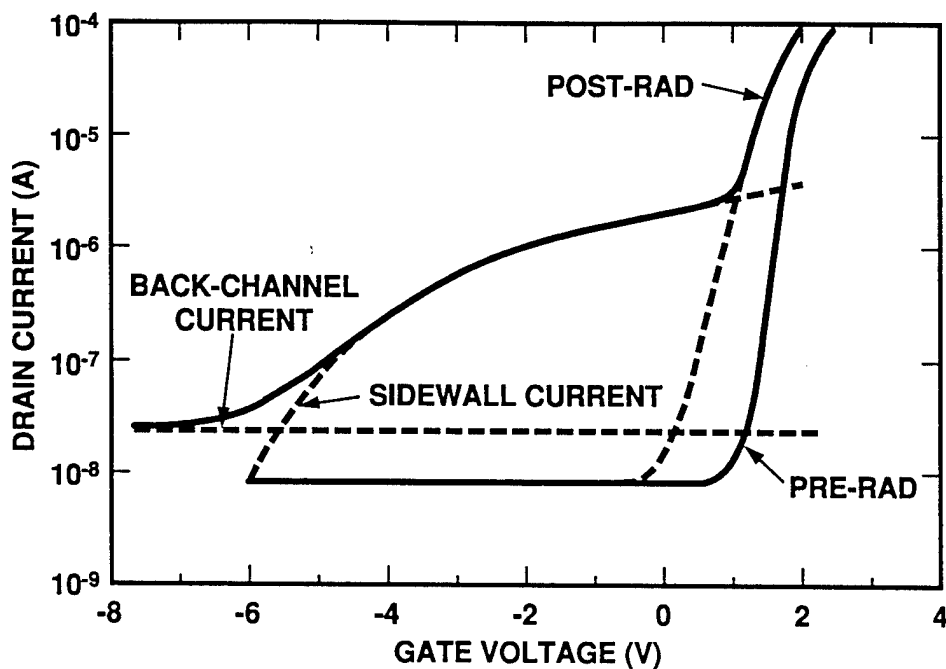


Figure 5.8. Sidewall and back-channel leakage currents from irradiation of an SOS (silicon on sapphire) n-channel transistor (After [Kjar-74]).

The use of reoxidized nitrided oxides for the gate dielectric may have hardness benefits even if the total thickness is not yet in the "ultrathin" (3-8nm) regime. The radiation-induced interface-trap buildup can be negligible in these dielectrics [Dunn-89], and the oxide-trapped charge can be lower or comparable to a thermal oxide [Dunn-89].

As described above, with the decrease in power supply voltages and device thresholds, subthreshold conduction can become even more important. Since microdose effects (Section 2.3.1) can adversely impact subthreshold conduction, one might then expect this to become more of a problem with future advanced technologies. However, the impact of this effect must be compared to other sources of variation. Fig. 5.9 compares the effect of microdose changes in threshold voltage versus that from doping fluctuations in scaled devices (using particular scaling rules [Dava-95]); for power supply voltages below 2 volts, the variations caused by doping fluctuations dominate. Thus if these scaling rules prove to be accurate, and advances in controlling effects from doping fluctuations are not made (by alternative device structures as mentioned above), subthreshold leakage from microdose effects is not likely to cause major problems in such highly scaled devices. Further mitigating any such microdose effects as devices scale is the general reduction in hole trapping and interface trap buildup in thin oxides.

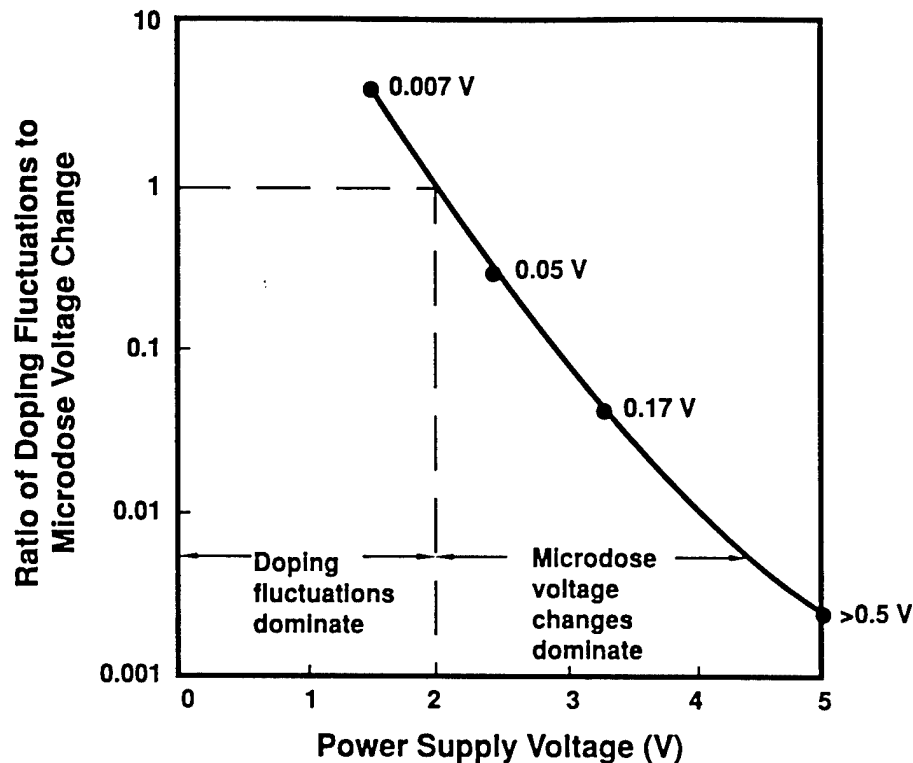


Figure 5.9. Comparison of the threshold voltage variations caused by doping fluctuations to those caused by microdose effects as devices are scaled to lower operating voltages (under a particular set of assumptions). Numbered points are the calculated value of threshold voltage variation at that power supply voltage (After [John-98]).

As devices continue to scale into the future, latchup might be expected to remain an important problem if not increase in importance since the gain of the parasitic bipolar transistors is likely to increase. However, there are two trends that may mitigate the problem [John-96a]. As devices scale to smaller geometries, power-supply voltages will decrease, and may drop below the voltage necessary to sustain latchup in internal circuit structures. Also for deep submicron devices, there may be a tendency to fabricate these in silicon-on-insulator (SOI) technologies, which are immune from latchup (since a contiguous four-layer structure does not exist). However, SOI devices can still be vulnerable to ion-induced snapback (Section 4.3.2).

As technologies move towards smaller feature sizes and thus less stored charge on circuit nodes, one might expect the critical charge for SEU to decrease. Indeed this trend was observed for many of the (currently) older technologies as shown in Fig. 5.10. However, results on more recent technologies with minimum feature sizes ranging from 0.4 to 1.5 μm do not follow this trend; in fact, the threshold LET has remained approximately constant in the range of 1.5 to 3 $\text{MeVmg}^{-1}\text{cm}^2$ (Fig. 5.11). This leveling off at a minimum LET has been postulated [John-98] to be the result of manufacturers taking into account the need to maintain a low upset rate from alpha particles or atmospheric neutrons during the design and manufacture of their parts [Lage-93, Lant-96]. If this is indeed the case and remains so, then advanced devices may not become significantly more sensitive than their present day (advanced technology) counterparts.

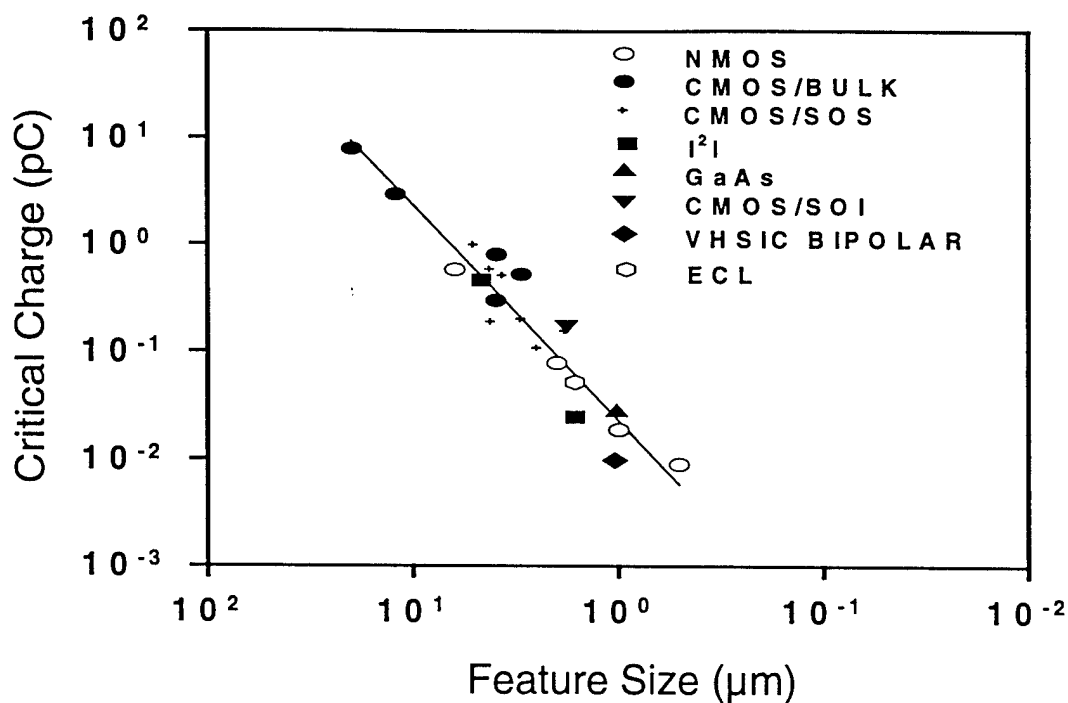


Figure 5.10. Relationship between feature size and critical charge for upset in various technologies. In this data all technologies show a similar trend to lower critical charge as the feature size decreases (After [Pete-88]).

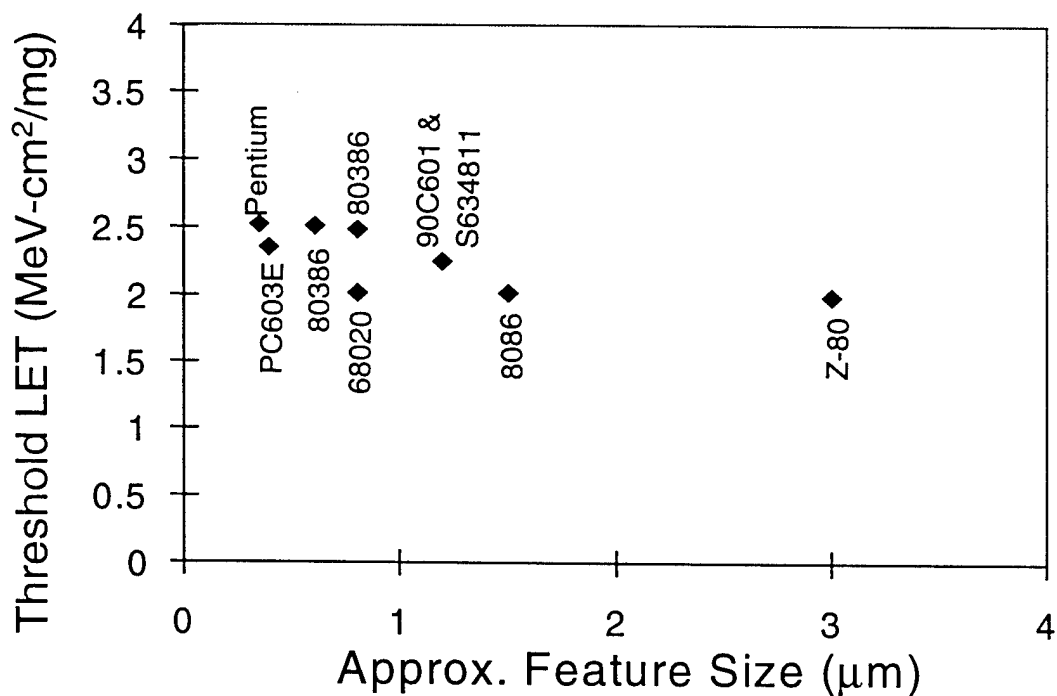


Figure 5.11. Threshold LET for single event upset for various generations of microprocessors over a ten year period as a function of approximate feature size. There does not appear to be a clear trend in this data, i.e., the threshold LET is relatively independent of feature size (After [John-98]).

However, the above comments on SEU trends primarily relate to latch or memory structures in devices. In general there are three factors which affect the upset rates caused by pulses from single event transients in logic in VLSI circuits. (1) The signal path of logic gates between the gate struck by the ion and either storage elements or output pins must be such that the pulse can propagate. For example, in an AND gate with the A input at "0" and the B input at "1", a pulse on the B input will not affect the output whereas a pulse on the A input can propagate through the output and continue down the logic chain. (2) The pulse must also be of sufficient amplitude and width to propagate down the logic chain. (3) The pulse as it propagates must also maintain sufficient amplitude and width to be stored in a register or transmit through the output.

As scaling continues, the charge required to switch logic gates decreases, as illustrated in Fig. 5.12 for a CMOS inverter. This falls in category (2) above and indicates that unless design or fabrication alterations from projected scaling occur, SEE in combinational logic may become more prevalent (as alluded to in Section 4.1.2 above). In addition, the error rate can be a function of frequency. The error rate is expected to increase with frequency for combinational logic (since the time during which such logic is susceptible is linearly dependent on frequency), but remain relatively constant for sequential logic (since the sensitive time depends primarily on the clock duty cycle rather than frequency) [Buch-97], as illustrated in Fig. 5.13.

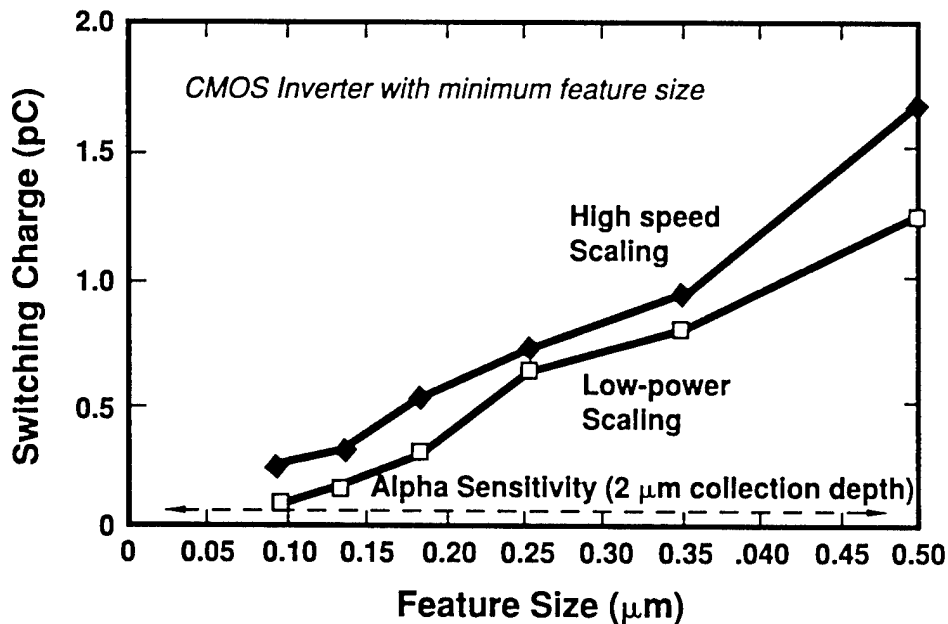


Figure 5.12. Effect of scaling on the switching charge of a CMOS inverter with minimum feature size. Calculations are shown for devices scaled under either high-speed scaling rules or low-power scaling rules (After [John-98]).

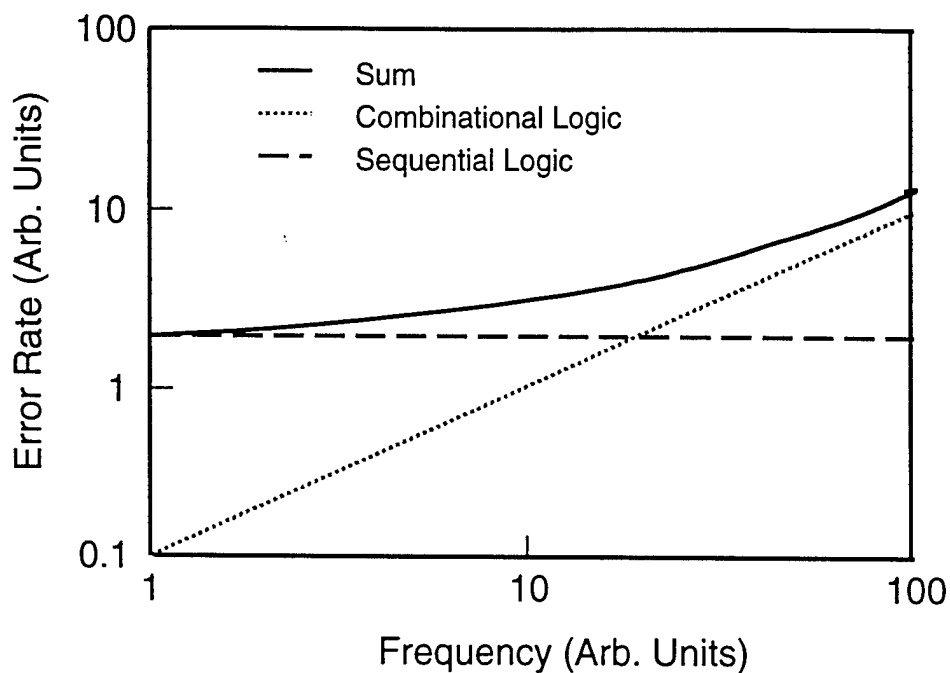


Figure 5.13. Schematic of error rate in logic ICs as a function of clock frequency for combinational and sequential logic (After [Buch-97]).

6.0 SUMMARY

Total dose effects involve the creation and trapping of charge in dielectrics and the creation of interface traps. The line between oxide-trapped charge and interface traps has been blurred somewhat by the fact that some of the positive charge states can exchange charge with the silicon (border traps), so that there really appear to be three kinds (as defined by their electrical characteristics) of traps of interest in the Si/SiO₂ system. Models for these traps continue to be refined, but certain features seem to be relatively well established. The oxide trap is primarily associated with the E' center. Many radiation-induced interface traps are formed by a two-stage process whereby holes transporting through the oxide release a hydrogen species which transports to the interface where they interact to form silicon dangling bond P_b centers (the primary interface trap). These charge centers can cause significant shifts in device properties and lead to device failure.

For devices in the new millennium, as gate oxide thicknesses decrease to ~10 nm and below, positive oxide trapping and interface trap buildup are likely to become only minor issues in gate oxide devices. In these structures however, new concerns may arise such as radiation-induced leakage current and perhaps gate oxide rupture from single ions. It should be emphasized that field oxides will still likely be much thicker than this, and also devices which require higher voltages (such as nonvolatile memories, charge pump circuits, power MOSFETs, etc.) will have thicker oxides. These devices will still be subject to concerns from oxide trapping and interface traps.

New phenomena such as the damage enhancement observed at low dose rates in bipolar devices must be considered. New device structures, such as MEMS, may also raise new manifestations of failure from the "same old" sources (e.g., charge trapping). Fortunately it appears that much of the knowledge gained on mechanisms can be applied to newer devices (such as MEMS, HgCdTe, SiGe, etc.).

Particle irradiation can dislodge atoms in device structures to cause displacement damage. This leads to defect sites which can act as traps, recombination, and generation centers. These in turn lead to minority carrier lifetime degradation, carrier removal, and mobility reduction. Again changes may be substantial enough to cause failure of devices. A convenient general technique (although there are exceptions) for quantifying and characterizing this damage between particle types and across energy regimes is the use of Non-Ionizing Energy Loss (NIEL). For small geometry devices in which the volume of interest is of the order of the damage region from a particle, NIEL will be less useful.

The basic concepts for displacement damage and NIEL have enabled understanding of effects across a wide range of devices, including silicon solar cells, InP and GaAs devices, SiGe, SiC, VCSELs, superconductors, and QWIPs. However, for particular cases (as in CCDs) the details of the damage interaction and location of the damage site can be important; for defects created by inelastic nuclear reactions or for defects in high field regions, the generation currents can be significantly higher than would otherwise be expected.

Single event effects are associated with the charge generated by the passage of a single high energy particle through a device structure, and its subsequent collection by active regions of the device. Charge collection can be augmented by effects such as funneling or bipolar action. The resulting current or voltage transients can be sufficient to change information stored in memory cells or to propagate through a logic path and cause incorrect outputs or wrong information to be stored. Linear Energy Transfer (LET) is a convenient general measure to indicate the amount of charge generated by a particle in a device. However, as device dimensions continue to decrease, LET as a general descriptor for upset sensitivity will become less valid.

Devices in which high voltages/fields may be present can experience catastrophic failure from single ions. Power MOSFETs are subject to single event burnout and single event gate rupture. Single-event-caused gate rupture has also been observed in devices such as nonvolatile memories, capacitors, FPGAs, and SRAMs, and may be an issue for future scaled devices as the typical field across the gate dielectric increases.

Latch-up can also be induced by single ions, as can the related phenomena of snapback and second breakdown. For future devices, this may remain a concern but may be mitigated by the move to lower supply voltages and possibly to SOI technologies.

As devices continue to scale, the LET thresholds for upset may not change markedly from those in advanced devices today. However, there may be an increased susceptibility in

combinational logic circuits to SEE. New phenomena may also be expected to arise as technologies progress.

Overall, the current knowledge of basic mechanisms for radiation damage in devices is expected to provide a sound foundation for future understanding as we progress into the next millennium. Areas where the "standard" understanding may prove inadequate often arise when it is based on average effects. As device feature sizes become smaller there are circumstances when average damage effects are no longer appropriate and the statistics of single photon or particle interactions are important. Beyond this, however, one might also expect that a few surprises will likely also be uncovered (as they have been in the past).

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