HIGH-EFFICIENCY SILICON SOLAR CELLS FOR USE WITH A PRISMATIC COVER AT 160 SUNS

SAND--90-7030

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ABSTRACT

For this program, Solarex developed a process sequence that could be used in a manufacturing environment to produce high-efficiency silicon concentrator cells. The cells had large gridlines to minimize series resistance losses and a prismatic cover to minimize shadowing. The front surface of the cell was textured to improve absorption of light and passivated to reduce front-surface recombination. Two separate diffusions steps were used: a deep emitter with a light surface concentration and a heavy diffusion to reduce recombination under the front contacts. Cell efficiencies as high as 22.25% were demonstrated at 75 suns and over 21.5% at 150 suns air mass 1.5 illumination.

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TABLE OF CONTENTS

LIST OF FIGURES

LIST OF TABLES

1 INTRODUCTION

1.1 Program Objectives

The purpose of this program was to develop a process capable of producing high-efficiency silicon solar cells for use at 100 to 200 suns concentration. This process was intended to include techniques expected to improve cell efficiency and result in a consistent and reliable module-ready end product.

No specific efficiency target was established. However, the achievement of low bulk resistivity silicon concentrator cells by researchers at the University of New South Wales with efficiencies that exceeded 25% established a state-of-the-art level we attempted to approach on Solarex's cell production line.

1.2 Summary of Accomplishment

Solarex developed a process sequence which resulted in 1.61 cm^2 low bulk resistivity concentrator cells with efficiencies after attachment of prismatic covers typically in the 20-21% range at 150 suns air mass 1.5.

The highest efficiency achieved during this program was 22.25% at 75 suns.

At the conclusion of this program, Solarex had developed a cell structure that had six photolithography steps and two diffusion steps. Techniques including surface passivation, patterned surface texturing, and deep emitter diffusions with low surface dopant concentrations were introduced into a commercial solar cell manufacturing environment.

Several problems associated with the measurement of the covered cells were also addressed during this program. Active-area efficiencies based on measurements of gridline coverage were found to be an unreliable indication of cell efficiency after attachment of a prismatic cover. Active-area efficiencies above 25% were measured on Solarex's cells from this program at Sandia National Laboratories. However, because uncovered cell short-circuit-current densities included reflection from gridlines into the cell active-area, the performance at concentration with a cover was overestimated. For this program, Solarex analyzed losses resulting from the cell covering operation and evaluated apparent discrepancies in covered cell performance based on uncovered active area measurements.

1.3 Approach

We selected a cell design that had a large area gridline coverage fraction to minimize series resistance losses and a prismatic cover to divert light that otherwise would have been reflected from the gridlines, into the active area of the cell. This approach was a continuation of previous work performed at Solarex in which heavily metallized concentrator cells with prismatic covers achieved 18-19% conversion efficiencies at air mass 1.5. The function of a prismatic cover is illustrated in Figure 1-1 below.

Our efforts focussed on optimizing our process steps to incorporate, as much as possible, the successful high-efficiency cell fabrication techniques emerging from university laboratories such as: front surface passivation, deep diffused layers with low surface dopant concentration, and techniques to preserve and perhaps even enhance minority carrier lifetimes.

We initially intended that the entire program be model-driven to as great an extent as possible. As work on the program progressed, however, and as results from a parallel program to develop a similar device at the University of New South Wales became available, our emphasis shifted to taking advantage of previously proven techniques as much as possible.

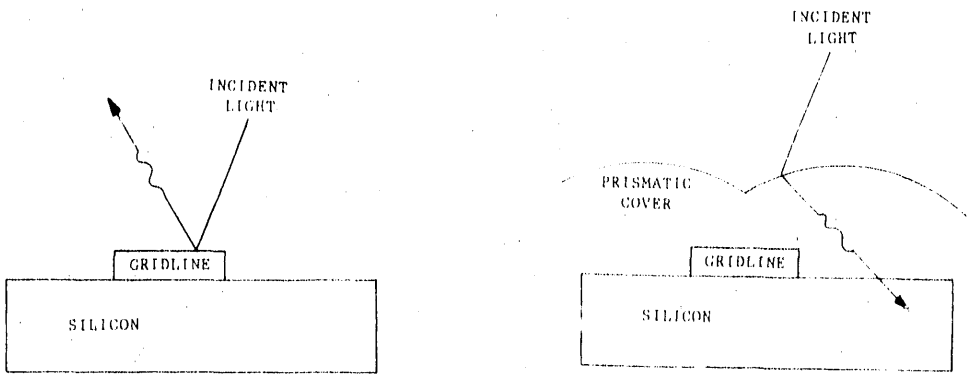


Figure 1-1
Solar Cell with Prismatic Cover Attached

Work on this program was organized into the following tasks:

Task 1: Device Characterization. Basic device and material parameters for concentrator cells fabricated for previous programs were measured. Special test samples were also prepared for this purpose. Electrical measurements at various light levels, quantum efficiency vs. wavelength curves, reflectance measurements, and spreading resistance profiles for both front and back junctions were made.

Task 2: Performance Improvement Modelling. We used the computer program, PC-1D, to evaluate the effect of critical design parameters such as bulk resistivity, cell thickness, minority carrier lifetime, dopant profile, and surface recombination velocities on cell performance at concentration. The results of the device characterization work were used as inputs to the model as they became available.

Task 3: Cell Improvement. Our development effort addressed problems specific to a cell design having large metal area coverage. Cell structures were fabricated with modifications that included: elimination of the diffused region under gridlines, limiting contact area between metal and diffused area, and placement of a separate heavily diffused layer under the gridlines to reduce recombination. Top surface texturing, passivation, and deep emitter diffusions with low surface dopant concentrations were included in the cell designs.

Task 4: Covering and Testing. Solarex subcontracted with Entech, Inc. to design and attach prismatic covers to the cell to enable evaluation of a complete device. Predictions of covered cell performance based on one-sun measurements was not a straightforward process because of reflections of incident light from the gridlines into the cell active area. This often resulted in overestimation of one-sun short-circuit-current densities. Measurements of cells at concentration was performed at Sandia National Laboratories.

2 PROCESS IMPROVEMENTS

2.1 Modelling

The effects of critical surface and bulk parameters on the performance of the baseline solar cells at concentration were studied using the computer model, PC-1D [1]. Since PC-1D is a one-dimensional model, it is not designed to directly handle effects that may result from the large metallized area interacting with the cell emitter. However, by assuming that the open-circuit-voltage is dominated by processes under the metal contacts and that the short-circuit-current density is dominated by the solar cell active area, the effects of cell design parameters on overall performance can be estimated.

Figure 2-1, shows the PC-1D simulation of the expected relationship between open-circuit-voltage and surface recombination velocity. Reducing front surface recombination velocity by two orders of magnitude--from 10^6 to 10^4 cm/sec--will provide an increase of approximately 25 to 30 millivolts in the solar cell open-circuit-voltage. An additional improvement of front

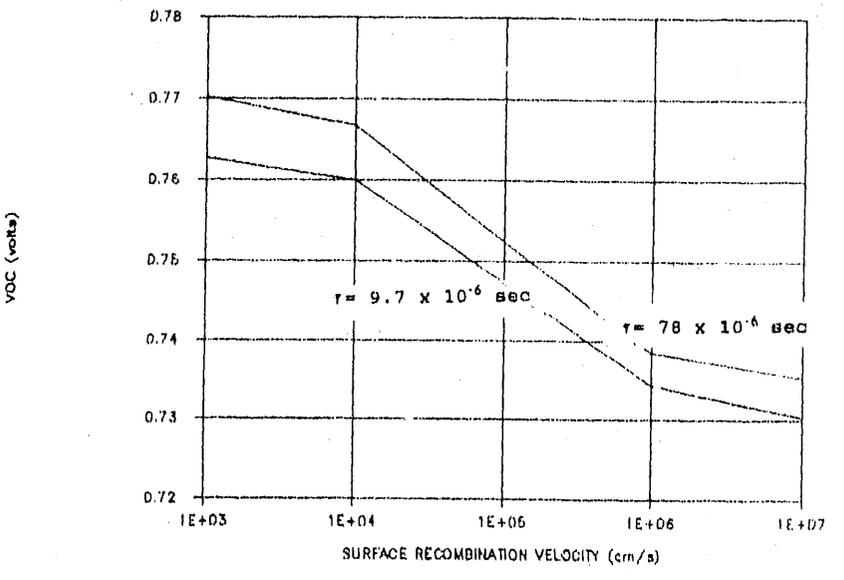


FIGURE 2-1
PC-1D Simulation of Open-Circuit-Voltage vs Front SRV

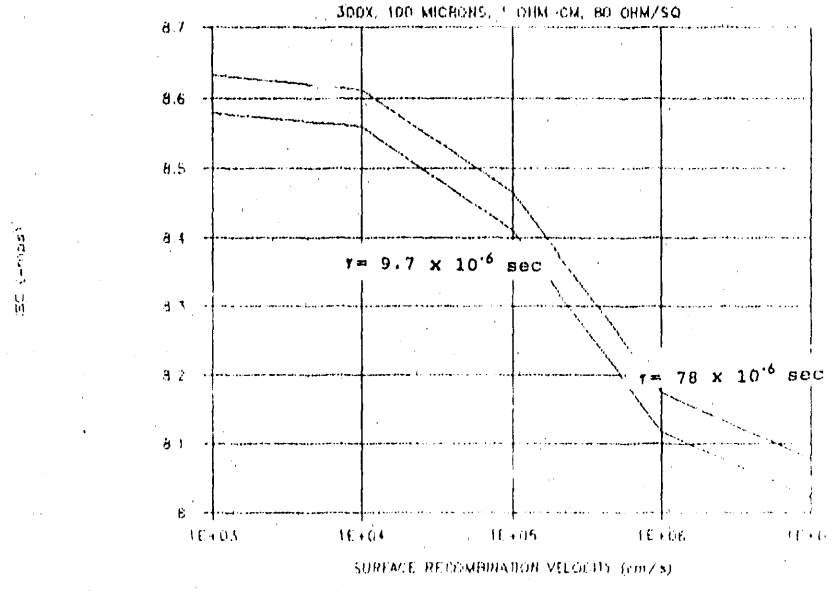


FIGURE 2-2
PC-1D Simulation of Short-Circuit-Current Density vs Front SRV

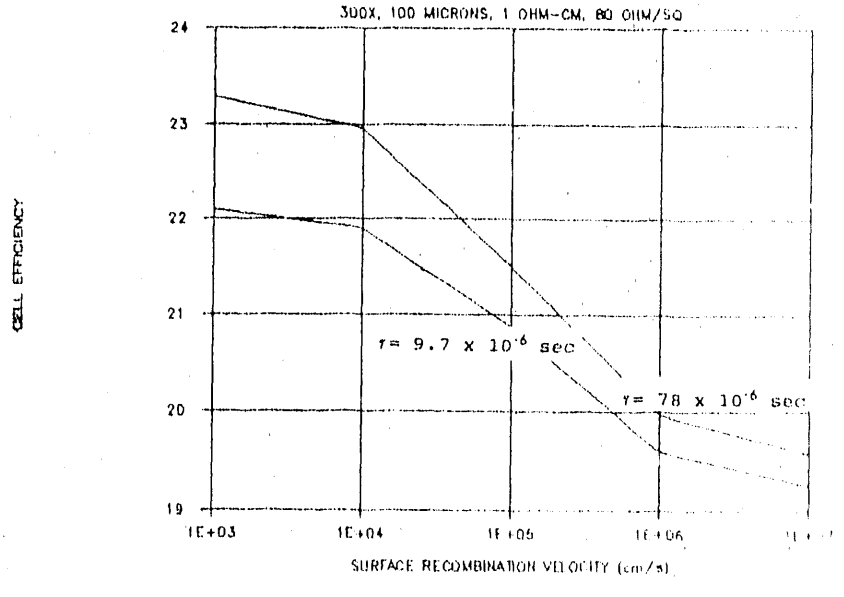


FIGURE 2-3
PC-1D Simulation of Cell Efficiency vs Front SRV

SRV to 10^3 cm/sec would contribute only an additional 3 to 4 millivolts. As a result, we targeted 10^4 cm/sec as an initial manufacturing goal which we believed would provide the most significant improvements in cell performance. Results are presented for two values of minority carrier lifetime in the substrate which we believed bracketed the range of post-processing conditions likely to be encountered in production. Similar results are shown for short-circuit current in Figure 2-2, and active-area-efficiency in Figure 2-3.

The role of minority carrier lifetime was studied with results shown in Figures 2-4 and 2-5. In silicon with 1 ohm-cm bulk resistivity, below a range of roughly 20 to 40 microsecond lifetimes degradation in all parameters is very rapid. Above that range, incremental improvements are relatively less insignificant.

Recombination at the back surface can play an important role, particularly for thin cells such as the 100 micrometer baseline cells. Even with a back-surface-field included in the cell model, short-circuit-current density is strongly effected by recombination for bulk resistivities less than about 1 ohm-cm. Figure 2-6 shows that for .2 ohm-cm silicon an increase in current of 2% can occur as back surface passivation improves the recombination velocity from $1x10^7$cm/sec to $1x10^4$cm/sec. The fill factor at concentration decreases as bulk-resistivity increases as shown in Figure 2-7, until a bulk-resistivity of near 10 ohm-cm is reached at which point conductivity modulation begins to offset the lower bulk dopant density.

As has been confirmed by results from university laboratories, [2,3] a wide range of bulk resistivities can be used to make high-efficiency concentrator cells. This is consistent with the modelled results shown in Figure 2-8. The best results are forecast for the lowest bulk-resistivity provided that required surface properties can be achieved, that bulk minority-carrier lifetimes can be maintained, and that the relationship between lifetime and bulk-resistivity follows the default relationship built into PC-1D.

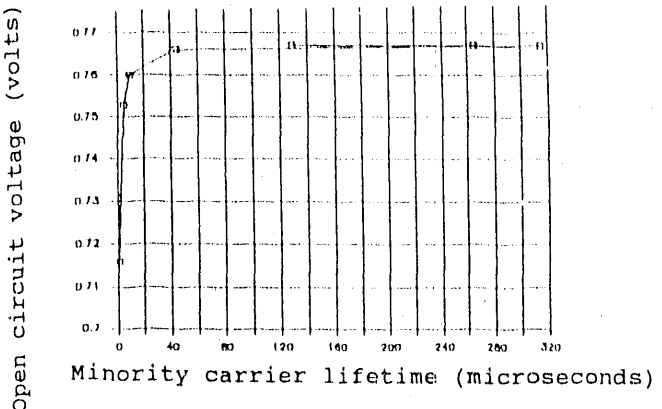


FIGURE 2-4
PC-1D Simulation of Open-Circuit-Voltage vs Minority-Carrier Lifetime

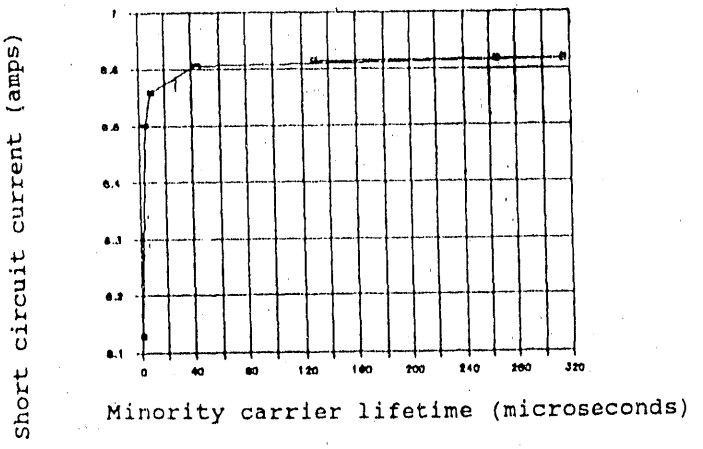
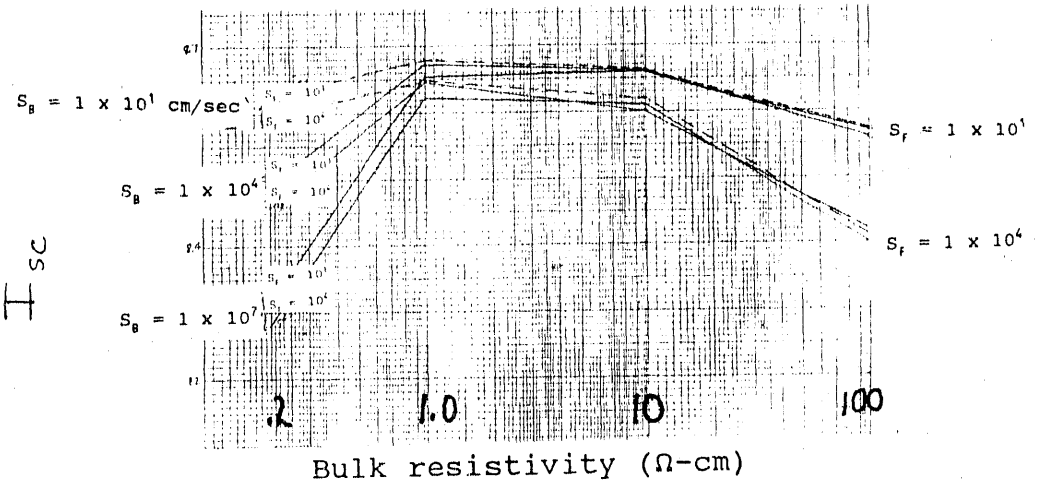


FIGURE 2-5
PC-1D Simulation of Short-Circuit-Current Density vs
Minority-Carrier Lifetime

According to our modelling studies, active area efficiencies at 150 suns (simulated by a solar cell with 50% shadowing at 300 suns) above 23% could be achieved by passivating the front and back surfaces of our baseline cells without reducing the minority-carrier lifetimes. Using a technique developed by Paul Basore [4] to include the effects of light trapping, an optimal thickness can be determined for various degrees of surface passivation. This result is shown in Figure 2-8 which predicts that active area efficiencies above 25% are possible.



S_f = Front surface recombination velocity
S_B = Back surface recombination velocity

FIGURE 2-6
PC-1D Simulation of Short Circuit Current vs
Bulk Resistivity

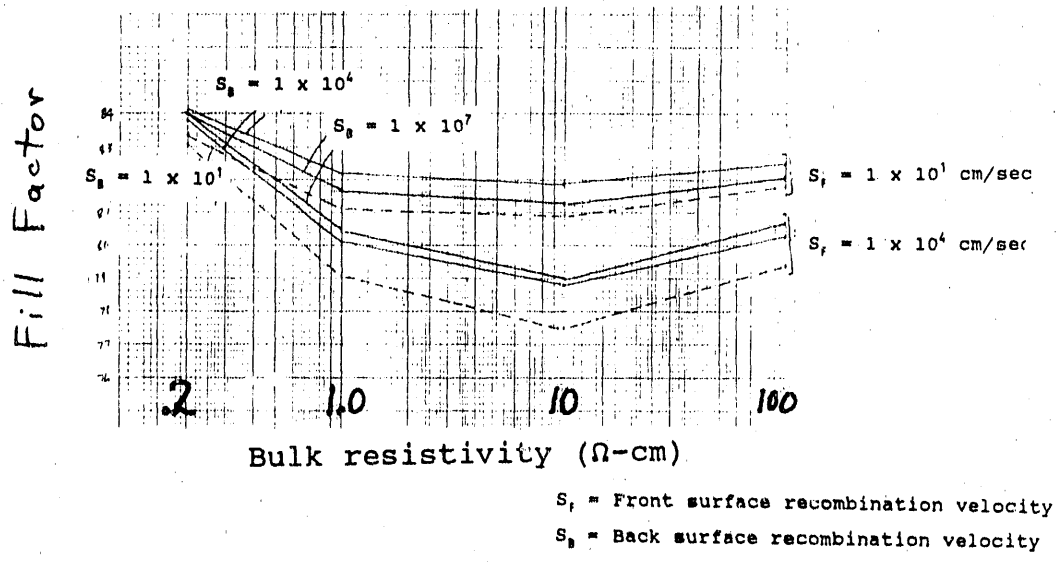


FIGURE 2-7
PC-1D Simulation of Fill Factor vs. Bulk Resistivity

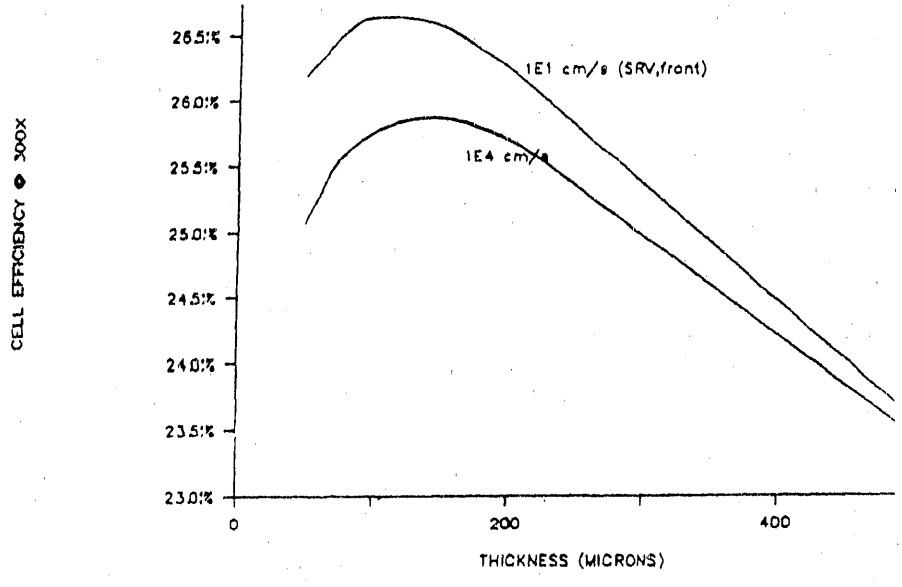


FIGURE 2-8
PC-1D Simulation of Efficiency vs Substrate Thickness

2.2 Device Characterization

A study was performed to identify the fundamental surface and material properties of our baseline cells to enable us to relate the actual measurements to the parametric curves obtained from modelling. In particular, we focussed on specific effects related to large metal contact areas. We developed a method [5] which used a metallization pattern that formed nine 1 cm^2 cells on a single substrate with metal coverage ranging from a few percent to nearly full coverage.

Reflectance measurements for a set of cells is shown in Figure 2-9. Quantum efficiency was obtained for each cell, using an automated rotating filter-wheel apparatus. Figure 2-10 shows the external quantum efficiencies for a set of metallized cells. Using a linear fit to the reflectance data for the set of cells, an internal quantum efficiency curve such as shown in Figure 2-11 was derived.

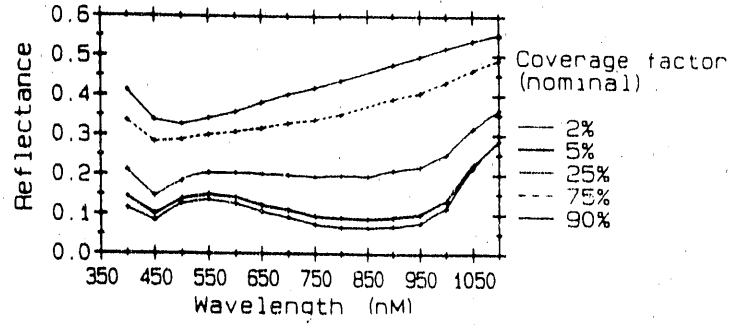


Figure 2-9
Reflectance vs Wavelength for a Set of Cells with Various Percent Metal Coverage

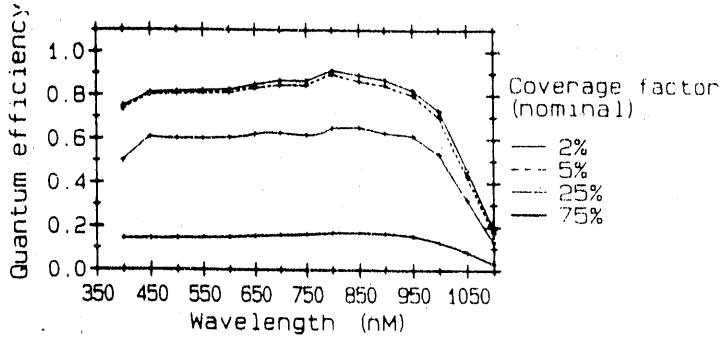


Figure 2-10
External Quantum Efficiency vs Wavelength for a Set of Cells with Various Percent Metal Coverage

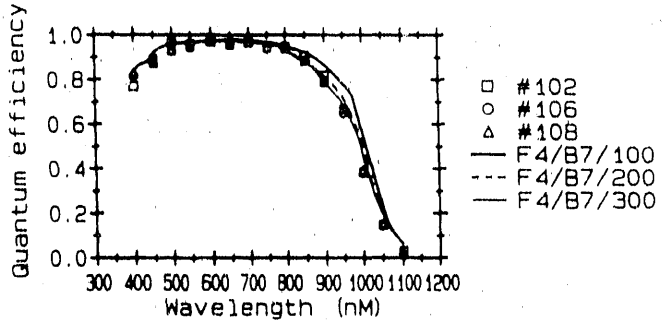


Figure 4: Fit to internal quantum efficiency. Key shows: front recomb. velocity/ back recomb. velocity/ base diffusion length (e.g. $1x10^{4}$ cm sec^{-1} / $1x10^{7}$cm sec^{-1}/100 microns).

Figure 2-11
Quantum Efficiency vs Wavelength
with Curve Fits Using Various Device Parameters

An in-house model using various values for front-surface recombination velocity, back-surface recombination velocity, and base diffusion length was fit to the quantum efficiency data. Parameters derived from this technique and the results from dark current-voltage curve analysis (generated from multi-light level measurements) is shown in Tables 2-1, 2-2, 2-3.

TABLE 2-1
Surface Recombination Velocity
at Various Solar Cell Interfaces

n+/titanium (gridline)	10^{6}-10^{7} cm/second
n+/air	5 x 10^{4} cm/second
n+/TiO_x (antireflective coating)	5 x 10^{3} cm/second

TABLE 2-2
Diffusion Length

Bulk Resistivity	Pre-processing	Completed Cell
.18 ohm-cm	193 micrometers (SPV)	108 micrometers
.35 ohm-cm	-------	143 micrometers
10 ohm-cm	-------	>482 micrometers

TABLE 2-3
CURRENT DENSITIES

$J_{oe'f}$ (Unpassivated emitter with AR coating)	5×10^{-13} A/cm^2
$J_{om'f}$ (Metallized emitter)	$2\text{-}3 \times 10^{-12}$ A/cm^2
J_{ob} (Metallized back)	$6\text{-}8 \times 10^{-13}$ A/cm^2

2.3 Optical Properties

Table 2-4 shows results from spectrometer measurements from samples placed in an integrating sphere. Each of these samples had a dual-layer, TiO_x/Al_2O_3 antireflective coating on the top surface. Random pyramidal etching reduces the reflectance integrated over the air mass 1.5 spectrum by 5.5% for the uncovered samples. The cover, with an index of refraction of 1.4, reduces the overall reflection from the untextured sample but contributes an additional 2% to the reflectance of the textured sample since it is not covered with an antireflection coating. As a result, the reflectance of the textured sample covered with an Entech prismatic cover is only 1.4% less than a comparable untextured sample with a cover. Reflectance versus wavelength curves for uncovered and covered wafers are shown in Figures 2-12 and 2-13 respectively.

TABLE 2-4

Reflectance of Silicon Wafers with Dual Layer AR Coating		
Silicon Surface	Uncovered	Covered
Smooth	.071	.050
Textured	.016	.036

The effect of the back surface topography on the cell's reflectance is illustrated in Table 2-5 which shows the results of measurements on silicon wafer samples with dual antireflective coating layers on the front and evaporated aluminum on the back. Texturing the front reduces reflection across the visible spectrum while texturing the back reduces reflection in the longer wavelengths.

Texturing both sides results in less long wavelength light being coupled out through the front of the cell than texturing the front side only.

TABLE 2-5

Reflectance of Silicon Wafers with Dual Antireflective Coating and Evaporated Aluminum on the Back

Front Silicon Surface	Back Silicon Surface	Estimated Loss in AM1.5 Current from Reflection	Reflectance at 1000 nanometers
Smooth	Smooth	.073	.64
Textured	Smooth	.037	.21
Smooth	Textured	.065	.15
Textured	Textured	.050	.15

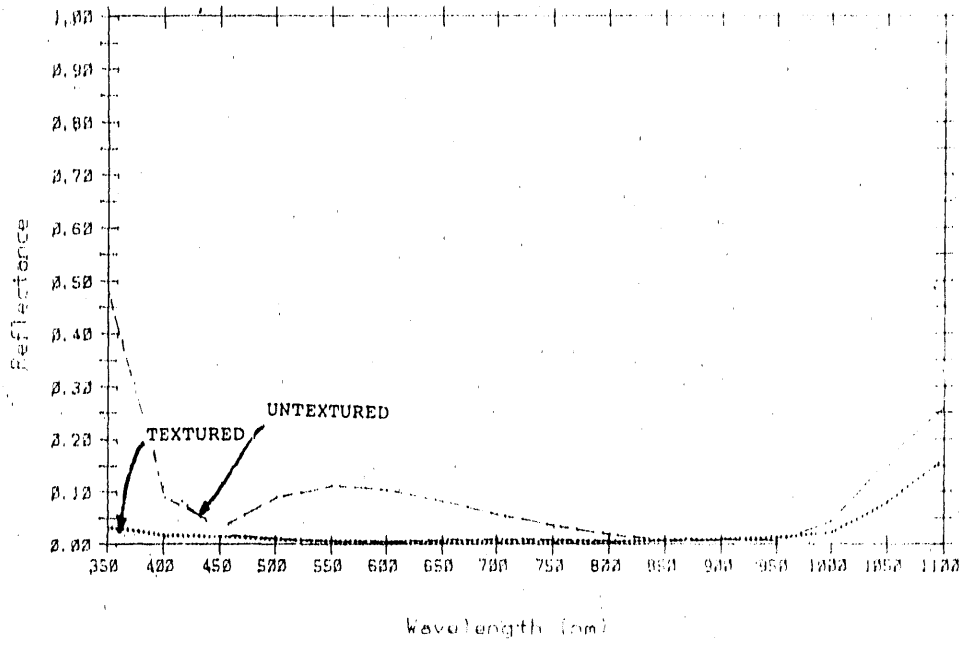


FIGURE 2-12
Reflectance vs Wavelength for
Textured and Untextured Silicon Wafers
without Prismatic Cover

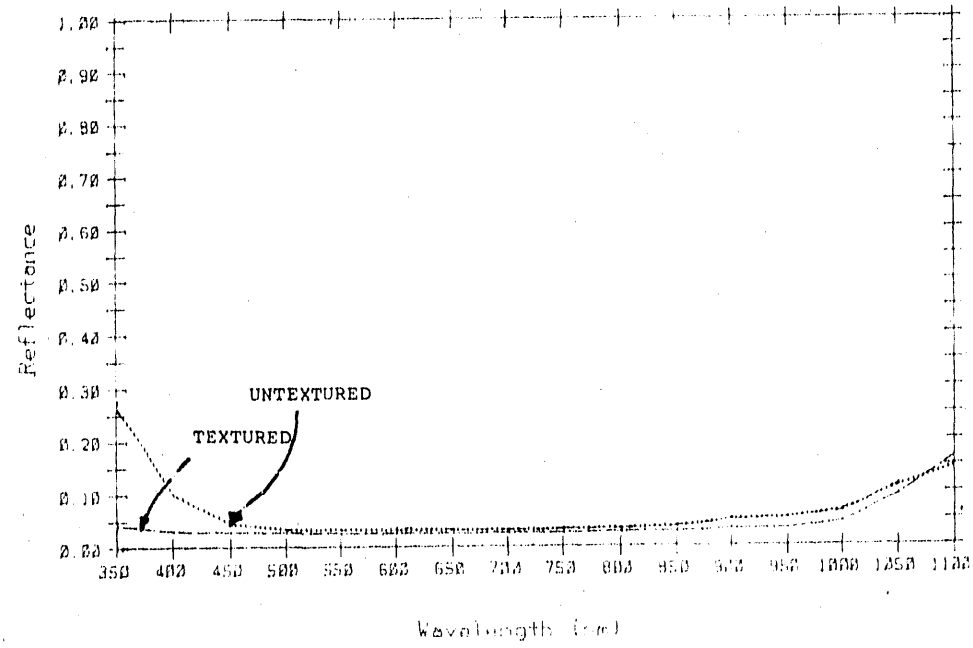


FIGURE 2-13
Reflectance vs Wavelength for
Textured and Untextured Silicon Wafers
With Prismatic Covers Attached

2.4 Surface Passivation

An experiment was performed to evaluate a procedure for growing an effective passivating oxide. Three different substrates were used: .18 ohm-cm float zone, .35 ohm-cm float zone, and 10 ohm-cm Czochralski silicon. An oxide was grown on wafers from each of these resistivity groups in dry oxygen at 875 degrees Centigrade for 10 minutes. Each group had a 75 ohm/square phosphorus diffused layer, an aluminum-paste alloyed back, and was covered with a dual antireflective coating whose performance was to some extent compromised by the presence of the thermal oxide. A typical space cell pattern with 32 micrometer wide gridlines on 1 millimeter centers was used.

Experimental groups with the following contacting methods were used:

A) A dot contact which reduced the grid-to- diffused layer contact area from .8% to .006%.

B) A control without a passivating oxide in which the entire gridline was in contact with the diffused layer.

C) Full contact between the gridline and diffused layer but with a passivating oxide covering the remaining cell active area.

D) The thin oxide grown during a pre-photolithography cleaning step which was present in Groups A) and B), was not present.

The results are shown in Table 2-6 and 2-7. Open-circuit-voltages were normalized to account for reduction in short-circuit-current caused by loss of antireflection coating optimization. The highest open-circuit-voltage, 637 millivolts, was obtained using the dot contact pattern and .18 ohm-cm silicon. This is very close to the value of 638 millivolts predicted by Paul Basore [6], for 200 micrometer, .2 ohm-cm silicon with minority-carrier lifetime of 10 microseconds. The lifetime of the .18 ohm-cm float zone silicon we used was 10.7 microseconds as determined by surface-photovoltage measurements at Wacker.

PASSIVATION MATRIX

CELLS SINTERED AT 500° C

AM1.5 MEASUREMENTS

		.18 OHM-CM FZ				.35 OHM-CM FZ				10 OHM-CM CZ			
		VOC	VOC,eq	ISC	FF	VOC	VOC,eq	ISC	FF	VOC	VOC,eq	ISC	FF
A) DOT CONTACT	mean:	0.624	0.626	0.118	0.774	0.622	0.625	0.122	0.783	0.570	0.573	0.128	0.780
	max:	0.630	0.632	0.121	0.804	0.626	0.627	0.124	0.801	0.580	0.583	0.132	0.808
B) CONTROL	mean:	0.605	0.605	0.130	0.706	0.614	0.614	0.133	0.774	0.606	0.606	0.144	0.783
	max:	0.612	0.612	0.131	0.744	0.620	0.620	0.134	0.796	0.613	0.612	0.147	0.807
C) OXIDE UNDER AR (REMOVED FROM PATTERN)	mean:	0.615	0.618	0.116	0.796	0.605	0.608	0.121	0.734	0.574	0.577	0.129	0.812
	max:	0.626	0.629	0.118	0.826	0.609	0.611	0.122	0.756	0.585	0.587	0.132	0.836
D) NO CHEM. OXIDE UNDER GRIDLINES	mean:	0.617	0.617	0.131	0.743	0.612	0.612	0.133	0.757	0.605	0.606	0.138	0.769
	max:	0.627	0.627	0.132	0.815	0.615	0.614	0.135	0.792	0.616	0.616	0.144	0.815

VOC,eq = Equivalent VOC at Isc of control group = VOC(Control)+.026xln (Isc, contr./Isc)

TABLE 2-6

PASSIVATION MATRIX

UNSINTERED CELLS

AM1.5 MEASUREMENTS

		.18 OHM-CM FZ				.35 OHM-CM FZ				10 OHM-CM CZ			
		VOC	VOC,eq	ISC	FF	VOC	VOC,eq	ISC	FF	VOC	VOC,eq	ISC	FF
A) DOT CONTACT	mean:	0.627	0.629	0.121	0.741	0.621	0.623	0.123	0.735	0.564	0.567	0.129	0.773
	max:	0.635	0.637	0.123	0.774	0.623	0.625	0.124	0.747	0.569	0.572	0.131	0.785
B) CONTROL	mean:	0.590	0.590	0.129	0.720	0.597	0.597	0.134	0.738	0.594	0.594	0.143	0.770
	max:	0.598	0.598	0.130	0.778	0.599	0.599	0.135	0.766	0.598	0.598	0.147	0.786
C) OXIDE UNDER AR (REMOVED FROM PATTERN)	mean:	0.571	0.573	0.119	0.728	0.599	0.602	0.118	0.751	---	---	---	---
	max:	0.604	0.606	0.123	0.752	0.608	0.610	0.123	0.782	---	---	---	---
D) NO CHEM. OXIDE UNDER GRIDLINES	mean:	0.593	0.593	0.128	0.722	0.590	0.591	0.129	0.715	0.599	0.599	0.144	0.778
	max:	0.605	0.605	0.129	0.785	0.605	0.606	0.129	0.755	0.601	0.601	0.145	0.795

VOC,eq = Equivalent VOC at Isc of control group = VOC(Control)+.026xln (Isc, contr./Isc)

TABLE 2-7

Based on a comparison of Groups B) and C), we concluded that passivation contributed to improving open-circuit voltages by reducing recombination at the contact between the gridline and diffused layer. The presence of the native oxide grown during our wafer cleaning procedure does not appear to have a statistically significant effect on cell performance.

It is interesting to note that the presence of a passivating oxide (or the process used to form it) decreased rather than increased the open-circuit-voltages of cells fabricated from 10 ohm-cm Czochralski silicon substrates. In addition, comparison of Tables 2-6 and Table 2-7 indicates that open-circuit-voltages of cells at the high side of the resistivity range studied improved with sintering while the low-bulk-resistivity cells degraded with sintering.

Although higher open-circuit-voltages are achievable using .18 ohm-cm float-zone silicon, we believed that the results of this matrix indicated that our passivating oxide growth technique was effective. Additional fine-tuning of the oxide growth procedure was performed throughout the program.

2.5 Diffused Layer Optimization

In an attempt to approach the open-circuit-voltages achieved at the University of New South Wales [7] we began to apply the procedure used there of a high-temperature, 3-hour, alloy step, to our solar cells. Instead of the shallow (.3 micrometer) junction depth used in our previous cell structures, this step resulted in emitters over a micron deep. Deep emitters covered with a good passivating oxide in low bulk resistivity silicon can be expected to reduce surface recombination.[8] There is also the possibility that gettering occurs resulting in improved post-processing minority-carrier lifetimes [9].

The first attempts to incorporate this procedure in our cell fabrication sequence resulted in severely reduced short-wavelength response. It was necessary to increase the pre-oxidation sheet resistivity in order to achieve the desired 75 ohm/square diffused layer after oxidation. Solarex's diffused layer produced by phosphine diffusion fell to a far lower sheet resistivity than diffused layers with comparable sheet resistivity produced by a solid source dopant at the University of New South Wales. We believe the difference to be attributable to a higher surface concentration of phosphorous resulting from phosphine diffusions with a larger amount of electrically inactive phosphorous that does not contribute to conductivity after the pre-deposition, but which diffuses into the silicon during the relatively long drive-in.

Using a modified mixture of gases as suggested by A. Cuevas [10] we were able to produce a diffused layer with the intended 75 ohms/square sheet resistivity after the long oxidation/gettering step which did not suffer from the loss of short-wavelength response found in our earlier attempts. The sheet resistivity following the pre-deposition was 180 ohms/square.

An empirical approach to forming ohmic contacts described in section 2.6 resulted in several problems. In order to establish an ohmic contact that would not adversely effect fill factor at concentration, it was necessary to use a larger gridline/diffused layer contact area on the order of at least several percent of the diffused area. This still allowed a significant contribution to recombination at the gridline/diffused layer; and efforts to reduce the surface concentration of the emitter made it more difficult to form an ohmic contact.

This lead to the use of two separate diffusion steps that would permit optimization of the emitter and contact areas independently. Since recombination at passivated current-collecting areas decreases as sheet resistivity increases and recombination at metallized area decreases as sheet resistivity decreases [11], this would allow a decoupling of two parts of the solar cell structure with diametrically opposed requirements. This structure which uses a deep heavily diffused region under metallized areas has been proposed [12] and developed [13] in previous work.

Spreading resistance measurements of the dopant profiles before and after oxidation are shown for the emitter region in Figure 2-14 and the metallized region in Figure 2-15.

2.6 Elimination of Shunting Paths

As the process sequence became more complex and as the number of photolithography steps increased, the opportunities for processing errors also increased. Despite the great care exercised in maintaining wafer cleanliness and use of proper handling techniques, a disturbingly large number of cells in the experimental groups were shorted out.

Observation of shorted cells under reverse bias using infrared imaging equipment supplied by Innovative Inspections, Inc. of Beverly, Massachusetts, identified three distinct shunting paths:

- a) Pinhole in the insulating layer between the busbar and the substrate. This is illustrated in Figure 2-16 and was corrected by protecting the oxide during brief exposures to hydrofluoric acid during post-diffusion deglazing steps and later by redepositing the oxide layer.

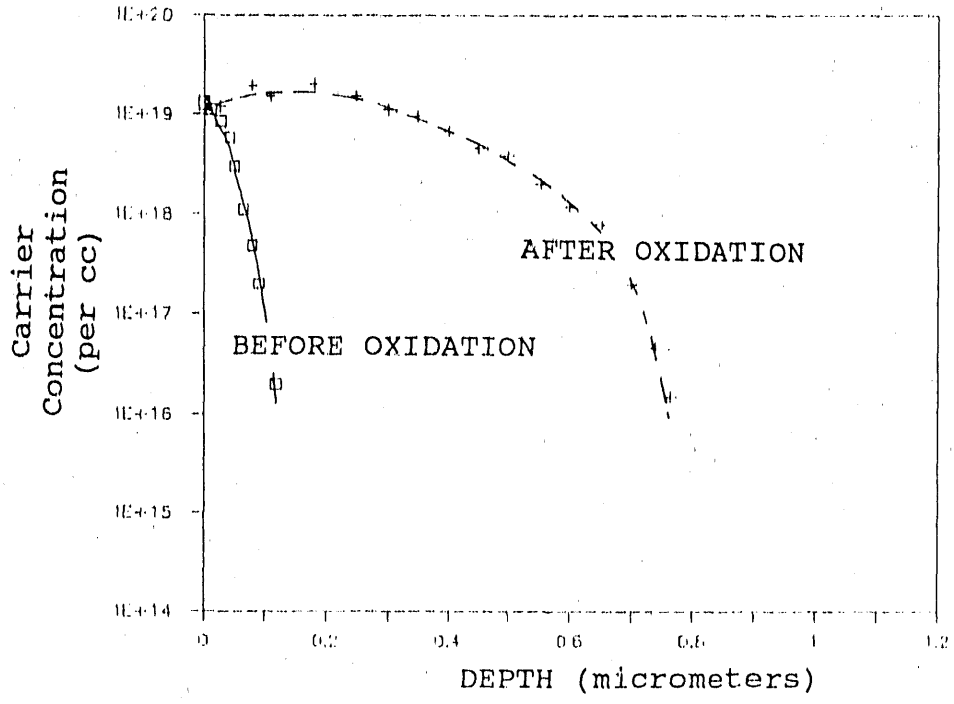


FIGURE 2-14
Emitter Dopant Concentration
Before and After Oxide Growth

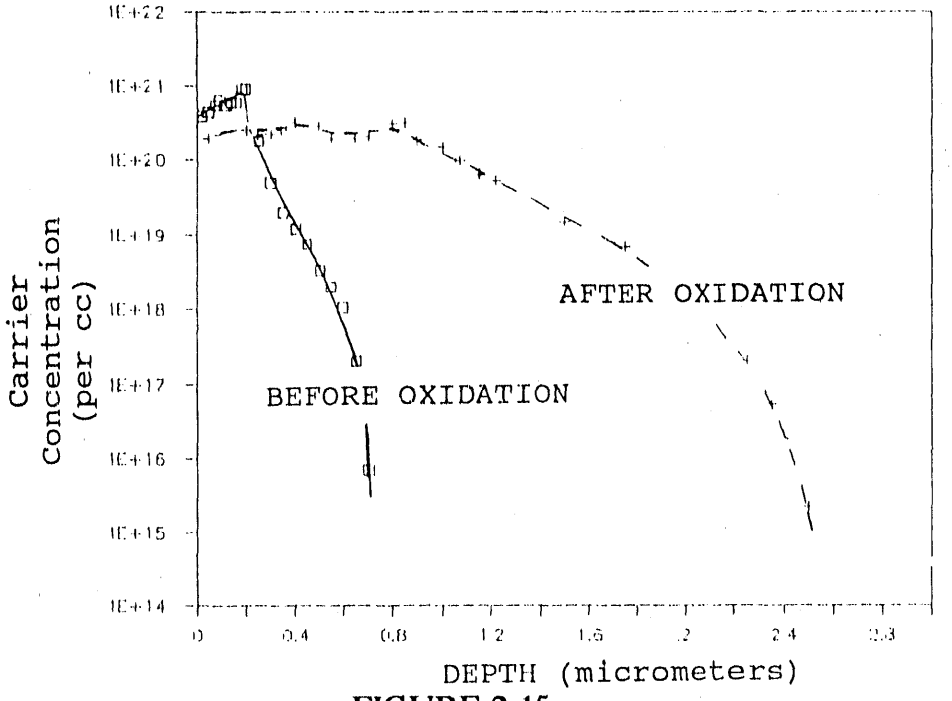


FIGURE 2-15
Emitter Dopant Concentration
Before and After Oxide Growth

- b) Etching of insulating layer at image of alignment pattern at the corner of the cell.

This is shown in Figure 2-17 and was eliminated by removing the alignment pattern from usable cell positions on the photolithography masks.

- c) Inadequate separation between busbar and undiffused p-region underneath. This mechanism is shown in Figure 2-18. Since the insulating oxide under the busbar had been used to also define the diffused region, a corner existed where because of the close proximity between the busbar and the substrate, the cell was vulnerable to shorts. This is illustrated in Figure 2-19. It is also possible that tunnelling occurred. This shunting mechanism was corrected by stripping the oxide used to define the diffused region and then redepositing an oxide over the area intended for the busbar that also covered approximately 10 microns of the diffused layer. The revised structure is shown in cross-section in Figure 2-20. Any penetration of the oxide layer at the oxide/silicon interface would then be to the diffused layer rather than to the substrate. This structure was used beginning with experiment 13 and resulted in a significant reduction in the number of shorted cells.

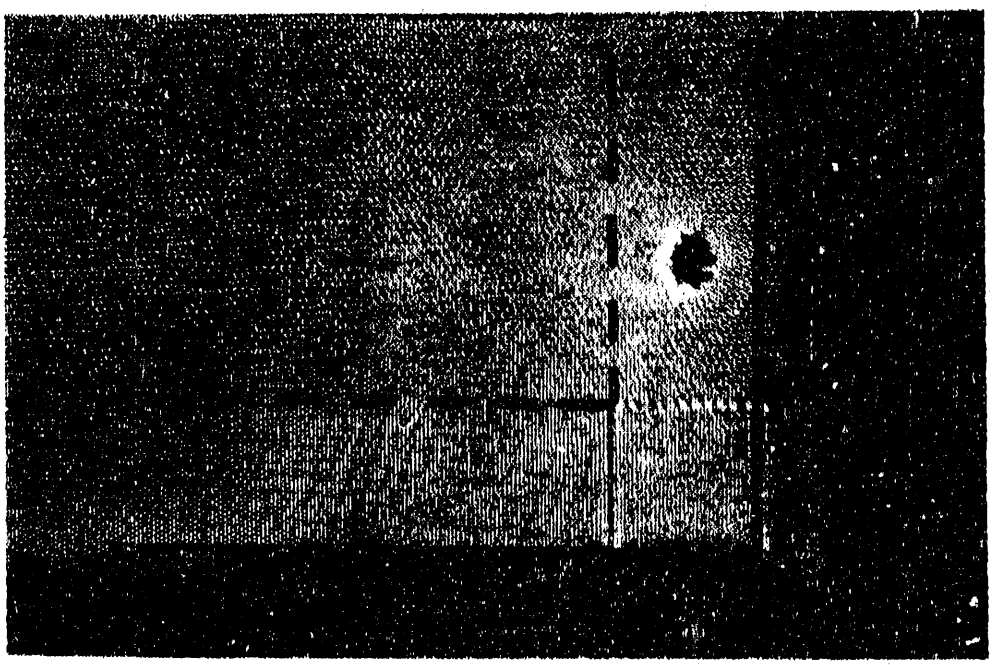


FIGURE 2-16
Infrared Thermogram Showing Pinhole Short

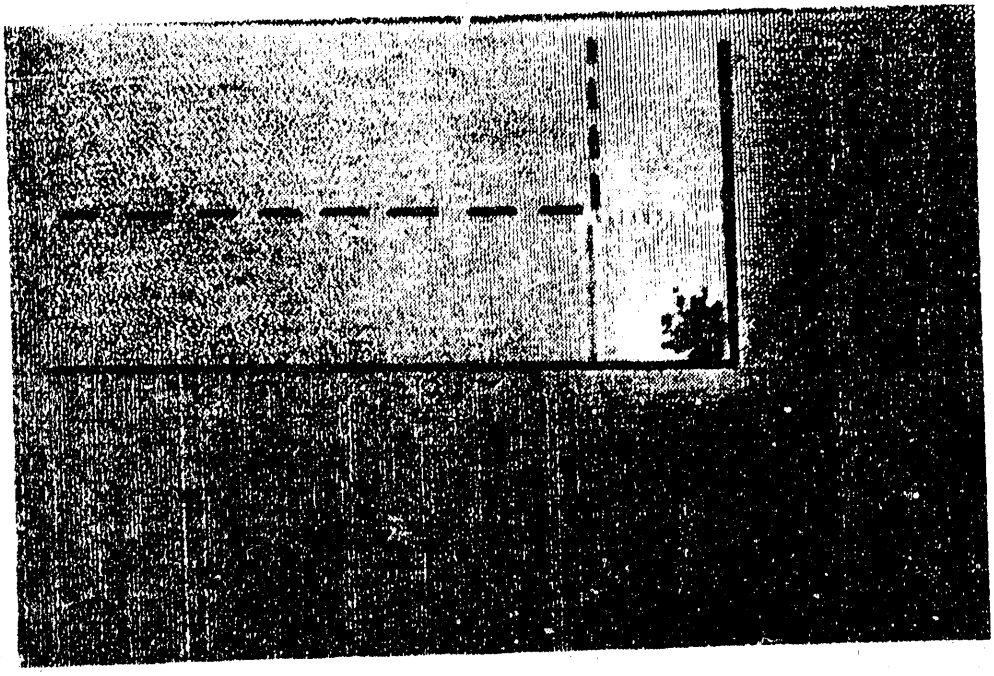


FIGURE 2-17
Infrared Thermogram Showing Short at Site of Alignment Target

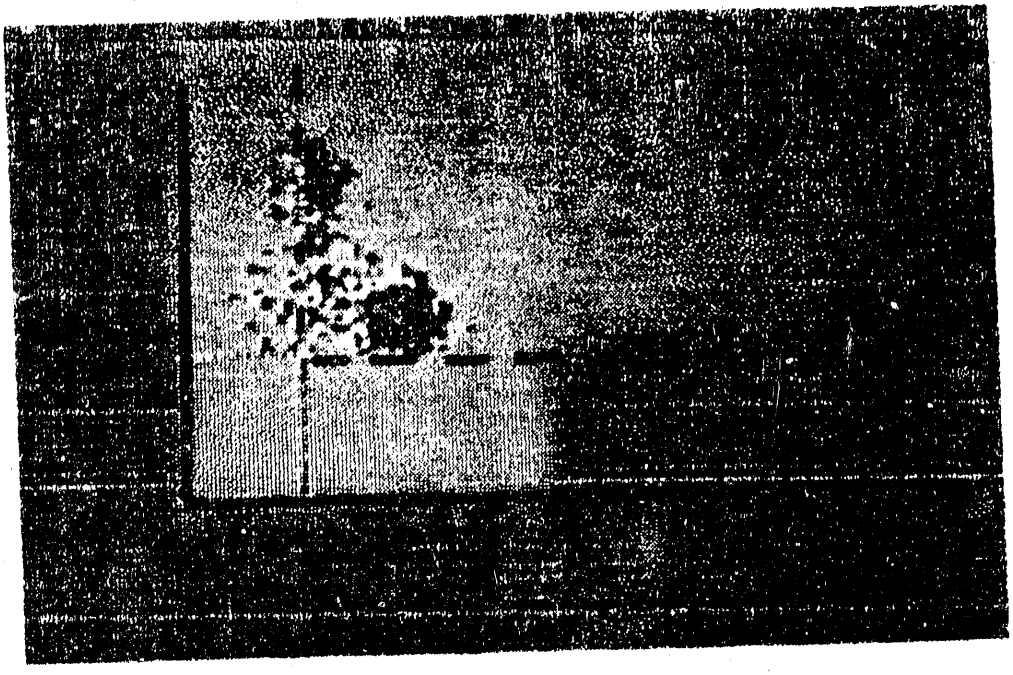


FIGURE 2-18
Infrared Thermogram Showing Short Between Busbar and Substrate

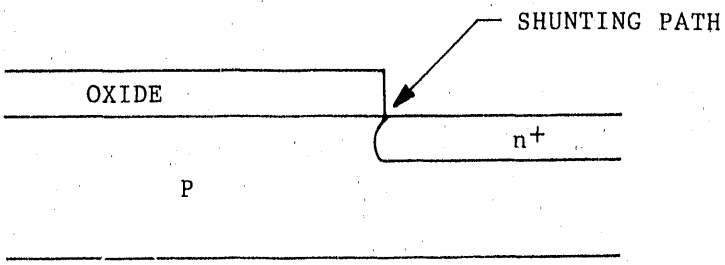


FIGURE 2-19
Solar Cell Cross-Section Showing Shunting Path

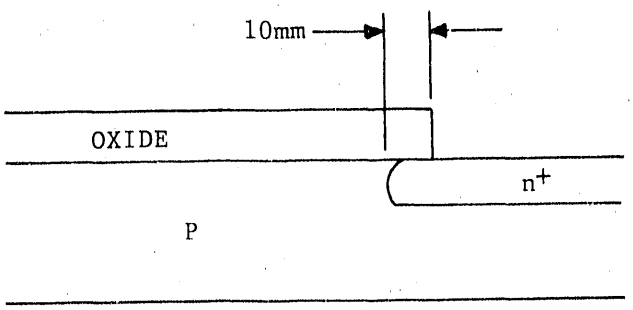


FIGURE 2-20
Solar Cell Cross-Section Showing Redeposited Insulating Layer

2.7 Summary of Experiments

Throughout this program, groups of silicon wafers were processed to characterize the fabrication techniques being considered and to optimize selected critical variables. A balance between avoiding excessive complexity and obtaining the maximum available information from each group processed was maintained. As the program progressed, a learning curve occurred resulting in progressively greater control over experimental procedures and processing steps. Experimental groups typically consisted of 25 to 75, 3-or 4-inch diameter wafers with a maximum potential of 21 cells per wafer processed.

Controls were run with each experiment. An attempt was made to limit the number of variables changed. Sometimes, however the variables were interactive -- such as n+ contact area and diffused layer sheet resistivity -- resulting in a combination of changes occurring at one time.

An overview of each experiment is given below. Key results are presented in greater detail in section 3.0.

Baseline cells. Solarex previously fabricated over 1000 1.58cm^2 silicon concentrator cells, as part of DOE contract No. DE-AC05-84ER80126, to be covered with an Entech prismatic cover and used in an Entech "crossed lens" point-focus module. These cells had close to 50% front grid metallization coverage to maximize cell fill factor at the 160 sun design concentration. A picture-frame type busbar surrounded the periphery of the cell with a deposited oxide underneath to prevent the diffused layer from forming under the bus. This oxide resulted in a planar diffused region which prevented contributions to reverse saturation current from large shadowed junction areas. The initial cells were processed using .35 ohm-cm float zone silicon approximately 225 microns thick. However, because of low fill factors (believed to be the result of large metal area in contact with the unpassivated silicon surface, thinner (100 micron) 1 ohm-cm float zone silicon was used. This enabled cells with good fill factors to be produced up to 160 suns but resulted in some loss of generated current because of the reduced silicon bulk without adequate provision for light-trapping. Cells with prismatic covers attached were typically in the 18-19% range.

Experiment 01. Samples were prepared for reflectance measurements during the device characterization phase of the program. These included samples with pyramidal texturing on front and/or back surfaces with and without evaporated aluminum. Optical properties of samples were also evaluated with prismatic covers attached to evaluate the performance of the entire optical package. Results from these measurements are reported in Section 2.3.

Experiment 02. Samples were prepared using a mask that generated several cells on each wafer with gridline widths that spanned a range from less than 1% coverage to over 90%. This was intended to evaluate the specific effects of the large metal area in contact with the diffused layer. A method was developed to separate the contributions to surface recombination velocity from the metallized and non-metallized regions. The results of this study in shown in Section 2.2.

Experiment 03. The first complete concentrator cells for this program were fabricated with the 75 ohm/square diffused layer not placed under either the busbars or gridlines. By doing this we attempted to extend the benefit of the planar junction to under the gridlines. These cells also had random pyramidal texturing of both front and back surfaces and were fabricated from 250 micron thick .18 ohm-cm float zone silicon. Active area efficiencies for these cells were around 20% showing no improvement over the baseline cells. Martin Green fabricated cells using a similar structure having no diffused layer under the gridlines and found no benefit [14] because the width of the gridline was less than a diffusion length.

Experiment 04. A layer of tin oxide was deposited on a diffused silicon wafer to evaluate the possibility of incorporating a transparent conductive oxide layer into the cell structure. The intent was to reduce diffused layer resistance and would have drawn upon the deposition capabilities of Solarex's Thin Film division in Newtown, Pennsylvania. However, titanium-palladium-silver front contacts evaporated through a shadow mask failed to make ohmic contact to the coating. As a result, no further work was pursued using transparent conductive oxides.

Experiment 05. Following an optimization matrix, cells with a thin thermally grown passivating oxide were fabricated. A pattern of small discontinuous dots comparable in density to the cells in the optimization trial, were placed under the gridline. Poor fill factors at 1 sun resulted from inadequate contact of the metal layer through the thin oxide to the diffused layer.

Experiment 06. Experiment 05 was repeated using larger contact areas optimized more for good ohmic contact than for optimal open-circuit-voltages. The result was reasonable fill factors at one sun (approaching .80). However, the fill factors dropped to unacceptably low levels as the concentration level reached as little as 50 suns.

Experiment 07. Even larger percent contact areas were evaluated. Although .80 fill factors at 300 suns (to simulate a cell with 50% metallization coverage at 150 suns) were achieved, the most consistently high fill factors were achieved on cells with 3% of the 75 ohm/square diffused layer in contact with the gridline metallization. The contact area, however was nearly two orders of magnitude greater than the "dot" contact used in the optimization study.

Experiment 08. As reports of success at the University of New South Wales with a 3-hour alloy/oxidation step became available, we decided to incorporate this step into our process to improve open-circuit-voltages and short-circuit currents. This step deepened the front and back junction and (presumably) improved the minority carrier lifetime of the bulk silicon by gettering. Our first attempt on (simpler one-sun) test cells resulted in severe loss of short wavelength response. This was due to excessive dopant concentration in our 75 ohm/square diffused layer which in addition had a larger component of inactive phosphorus than a comparable sheet resistivity produced at UNSW using a solid phosphorus dopant source.

Experiment 09. A new structure was fabricated using separate diffusion steps for the contact areas and the emitter. Dopant concentrations were adjusted to produce desired profiles after the high temperature thin oxide growth. Various contact patterns were evaluated with best results coming from cells with the entire width of the gridline in contact with a deep diffused region of the same width. Cells were fabricated using .18 ohm-cm float-zone silicon supplied by Wacker.

Experiment 10. In an attempt to improve the consistency of the ohmic contact, experiment 09 was repeated with cells in which only the current collecting areas were textured. The deep-diffused regions where the gridlines contacted the silicon were formed on polished silicon strips under the gridlines. This however, did not provide any noticeable improvement. In fact overall cell performance at one-sun was worse than the previous group because of inconsistent processing.

Experiment 11. A cell structure with a polished front and textured back was fabricated. Results from Section 2.3 suggested that with a prismatic cover the disadvantage of not having a textured front would be minor.

Experiment 12. Experiment 10 was repeated using a matrix of diffusion profiles and contacting patterns. Best results occurred for cells with the deep diffused region under the gridline occupying the entire width of the gridline.

Experiment 13. Experiment 12 was repeated using .35 ohm-cm float-zone silicon. Based on the results of infrared imaging of cells from previous groups,

the insulating layer under the busbars used as a diffusion mask was redeposited to eliminate shorting that occurred between the front metal and the base. The best covered cell from this program with an efficiency of 22.25% at 75 suns came from this group.

Experiment 14. Experiment 13 was repeated using .18 ohm-cm float-zone silicon and a heavier dopant concentration under the metallized regions. Improvements in fill factor and open-circuit-voltage were achieved which were offset by reductions in short-circuit-current density.

2.8 Cell Structures

Figures 2-21 through 2-23 show cross-sections of the cell structures used in experiments 03 through 07 and in experiment 10.

Four variations of the metal/diffused layer contact structure, shown in Figure 2-24, were evaluated in experiments 09, 10, 11, and 12. The best and most consistent results came from the structure shown in Figure 2-24.

A top view showing the cell gridline pattern used throughout the program is shown in Figure 2-25.

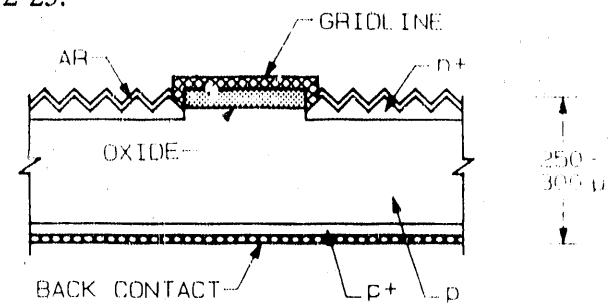


FIGURE 2-21
Solar Cell Cross Section: Reduced Emitter Area

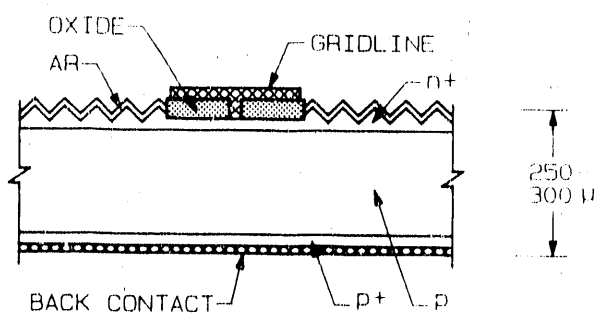


FIGURE 2-22
Solar Cell Cross Section: Point Contact

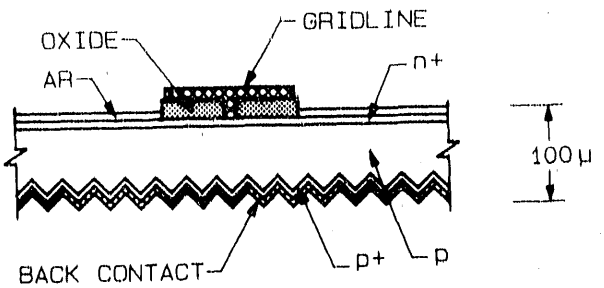


FIGURE 2-23
Solar Cell Cross Section:
Reflective Pyramids on Back

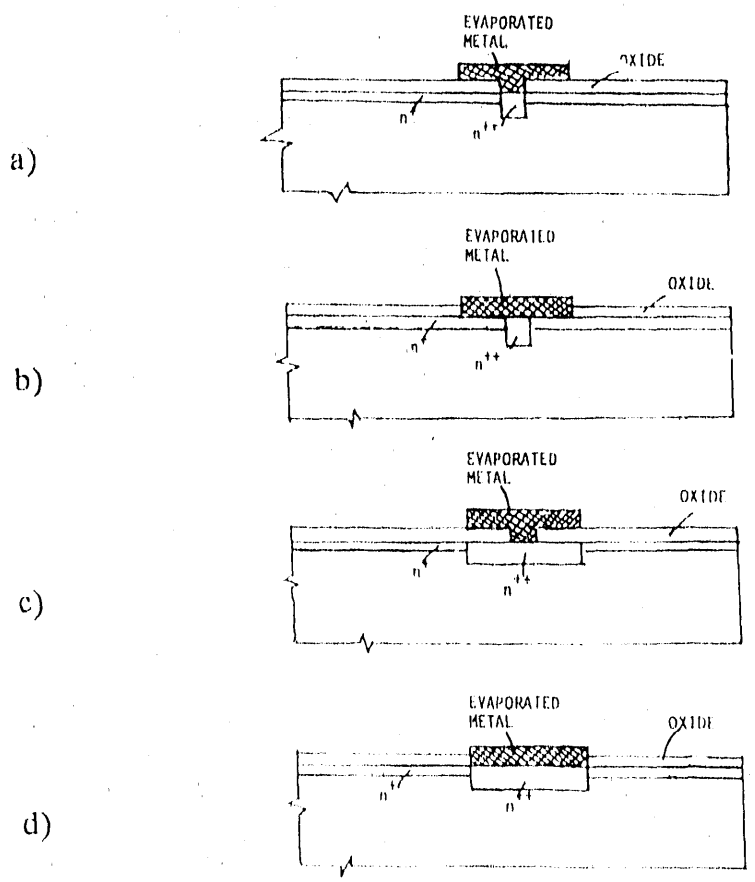


FIGURE 2-24
Solar Cell Cross Section: Various
Double Diffusion Contacting Methods

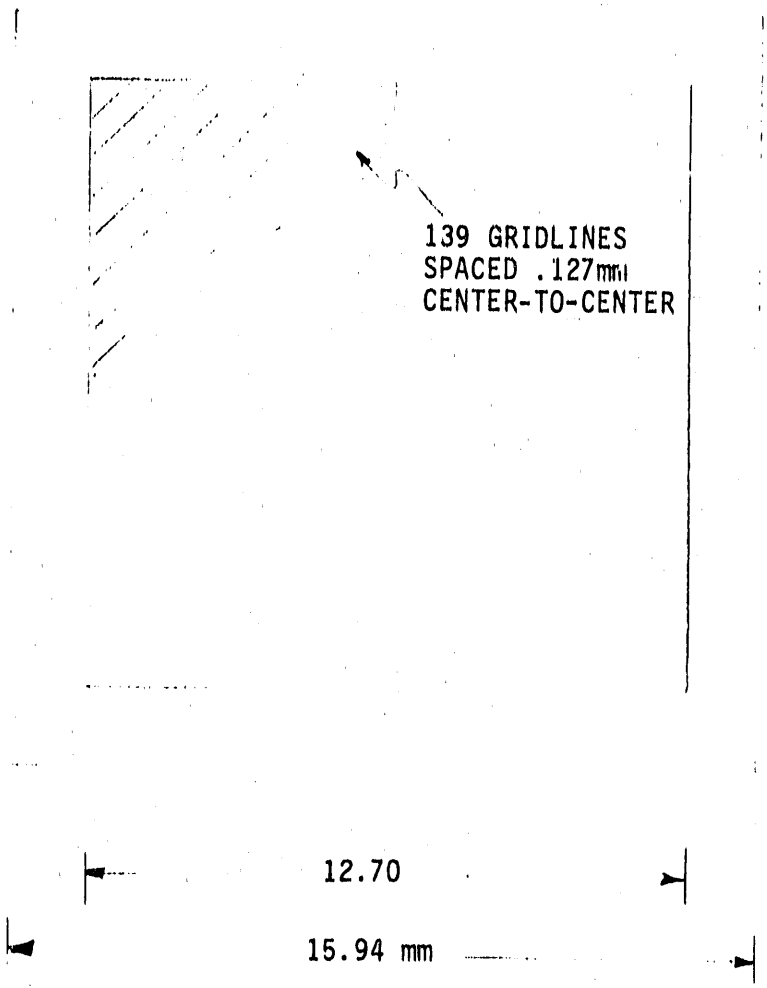


FIGURE 2-25
Solar Cell Metallization Pattern

3 RESULTS

3.1 Electrical Measurements

Table 3-1 summarizes the electrical characteristics of cells selected from the various experimental groups. Efficiencies at concentration measured after attachment of prismatic covers by Entech, Inc. are compared with expectations based on active-area efficiency calculations.

The cell active area efficiency is given by,

$$\eta_{act} = \frac{(P_{max})}{C \times (.1 W/cm^2) \times (1.62 cm^2) \times (1 - PercentCoverage)}$$

where,

P_{max} is the maximum power in Watts,

C is the concentration ratio, and

Percent Coverage represents the area of the solar cell inside the busbars that is shadowed by gridlines.

For cells with 50% gridline coverage, uncovered cells were measured at twice the concentration level of the covered cell efficiency to be simulated. The actual concentration level simulated is,

$$C_{simulated} = \frac{I_{sc}(C_{meas})}{I_{sc}(1 sun)} \times (1 - PercentCoverage)$$

Efficiencies after attachment of prismatic covers were generally 8.5-13.5% lower than we expected from the above active area efficiency calculation. Cells with active area efficiencies of over 25% dropped to 21-22.25% after attachment of prismatic covers. Linewidths were measured optically both at Solarex and at Sandia with reasonable consistency between the two measurements; data for both 1-sun and concentration were obtained at Sandia. The relationship between efficiency measurements on covered cells and expectations based on active area efficiencies is shown in Figure 3-1.

TABLE 3-1

COMPARISON OF COVERED AND UNCOVERED CONCENTRATOR CELLS AT 150 SUNS

	UNCOVERED					COVERED				RATIO			
										Covered/Uncovered Results			
CELL #	% Shad.	Active Area 1xJsc	Voc	FF	Active Area Eff.	1xJsc	Voc	FF	Eff.	Jsc	Voc	FF	Eff.
12-5-1	44.3%	0.0401	0.749	0.779	23.4%	0.0344	0.747	0.798	21.2%	0.886	0.997	1.024	0.904
12-4-4	36.4%	0.0382	0.761	0.757	22.0%	0.0350	0.751	0.786	20.7%	0.917	0.987	1.038	0.939
12-5-2	44.3%	0.0395	0.754	0.774	23.1%	0.0360	0.748	0.79	21.3%	0.911	0.992	1.021	0.920
12-13-3	36.4%	0.0359	0.76	0.795	21.7%	0.0346	0.756	0.819	21.4%	0.964	0.995	1.030	0.988
12-13-4	36.4%	0.0355	0.757	0.816	22.0%	0.0344	0.754	0.8	20.7%	0.968	0.996	0.980	0.942
12-13-5	36.4%	0.0362	0.759	0.779	21.4%	0.0347	0.755	0.816	21.4%	0.959	0.995	1.047	0.998
12-13-11	36.4%	0.0358	0.759	0.817	22.2%	0.0344	0.756	0.794	20.6%	0.959	0.996	0.972	0.929
13-a3-2	49.2%	0.0421	0.755	0.775	24.6%	0.0356	0.757	0.779	21.1%*	0.846	1.003	1.005	0.859
13-a3-5	44.3%	0.0385	0.756	0.782	22.8%	0.0362	0.767	0.801	22.0%*	0.939	1.015	1.024	0.967
13-a3-8	44.7%	0.0420	0.757	0.795	25.2%	0.0356	0.757	0.773	20.9%*	0.846	1.000	0.972	0.830
13-a3-7	45.3%	0.0393	0.753	0.786	23.3%	0.0356	0.752	0.795	21.4%	0.906	0.999	1.011	0.918
13-a3-9	48.2%	0.0416	0.755	0.800	25.1%	0.0356	0.754	0.801	21.6%	0.856	0.999	1.001	0.862
13-a4-3	46.3%	0.0397	0.756	0.791	23.7%	0.0351	0.754	0.796	21.2%	0.884	0.997	1.006	0.862
14-r-3	38.4%	0.0338	0.762	0.811	21.1%	0.0322	0.757	0.809	19.8%	0.951	0.993	0.998	0.939
14-u-11	41.3%	0.0355	0.755	0.778	22.2%	0.0353	0.749	0.781	20.8%	0.996	0.992	1.004	0.936
7C1-15	42.0%	0.0354	0.732	0.808	20.9%	0.03371	0.729	0.81	19.9%	0.952	0.996	1.002	0.954
7C1-17	44.3%	0.0364	0.732	0.821	21.7%	0.03365	0.728	0.818	20.0%	0.924	0.995	0.996	0.922
7C1-21	44.3%	0.0364	0.731	0.808	21.7%	0.0337	0.728	0.81	19.9%	0.926	0.996	1.002	0.915
7C2-34	49.2%	0.0363	0.729	0.812	21.5%	0.03365	0.729	0.809	19.8%	0.927	1.000	0.996	0.922
13-a3-2	49.2%	0.0421	0.742	0.811	25.8%	0.0356	0.739	0.815	21.6%	0.846	0.996	1.005	0.836
13-a3-5	44.3%	0.0385	0.743	0.813	23.3%	0.0362	0.739	0.827	22.25%	0.939	0.995	1.017	0.955
13-a3-8	44.7%	0.0420	0.743	0.823	25.7%	0.0356	0.739	0.815	21.6%	0.846	0.995	0.990	0.839
14-r-3	38.4%	0.0337	0.747	0.832	21.1%	0.0322	0.742	0.824	19.8%	0.955	0.993	0.990	0.937
14-u-11	41.3%	0.0355	0.737	0.809	22.4%	0.0353	0.732	0.813	21.1%	0.996	0.993	1.005	0.944

*Actual concentration for these cells was 175 suns.

FIGURE 3-2
Covered Cell Efficiencies at Concentration vs Expectations

	UNCOVERED					COVERED				RATIO			
										Covered/Uncovered Results			
CELL #	% Shad.	Active Area 1xJsc	Voc	FF	Active Area Eff.	1xJsc	Voc	FF	Eff.	Jsc	Voc	FF	Eff.
7C1-15	42.0%	0.0354	0.732	0.808	20.9%	0.03371	0.729	0.81	19.9%	0.952	0.996	1.002	0.954
7C1-17	44.3%	0.0364	0.732	0.821	21.7%	0.03365	0.728	0.818	20.0%	0.924	0.995	0.996	0.922
7C1-21	44.3%	0.0364	0.731	0.808	21.7%	0.0337	0.728	0.81	19.9%	0.926	0.996	1.002	0.915
7C2-34	49.2%	0.0363	0.729	0.812	21.5%	0.03365	0.729	0.809	19.8%	0.927	1.000	0.996	0.922
13-a3-2	49.2%	0.0421	0.742	0.811	25.8%	0.0356	0.739	0.815	21.6%	0.846	0.996	1.005	0.836
13-a3-5	44.3%	0.0385	0.743	0.813	23.3%	0.0362	0.739	0.827	22.25%	0.939	0.995	1.017	0.955
13-a3-8	44.7%	0.0420	0.743	0.823	25.7%	0.0356	0.739	0.815	21.6%	0.846	0.995	0.990	0.839
14-r-3	38.4%	0.0337	0.747	0.832	21.1%	0.0322	0.742	0.824	19.8%	0.955	0.993	0.990	0.937
14-u-11	41.3%	0.0355	0.737	0.809	22.4%	0.0353	0.732	0.813	21.1%	0.996	0.993	1.005	0.944

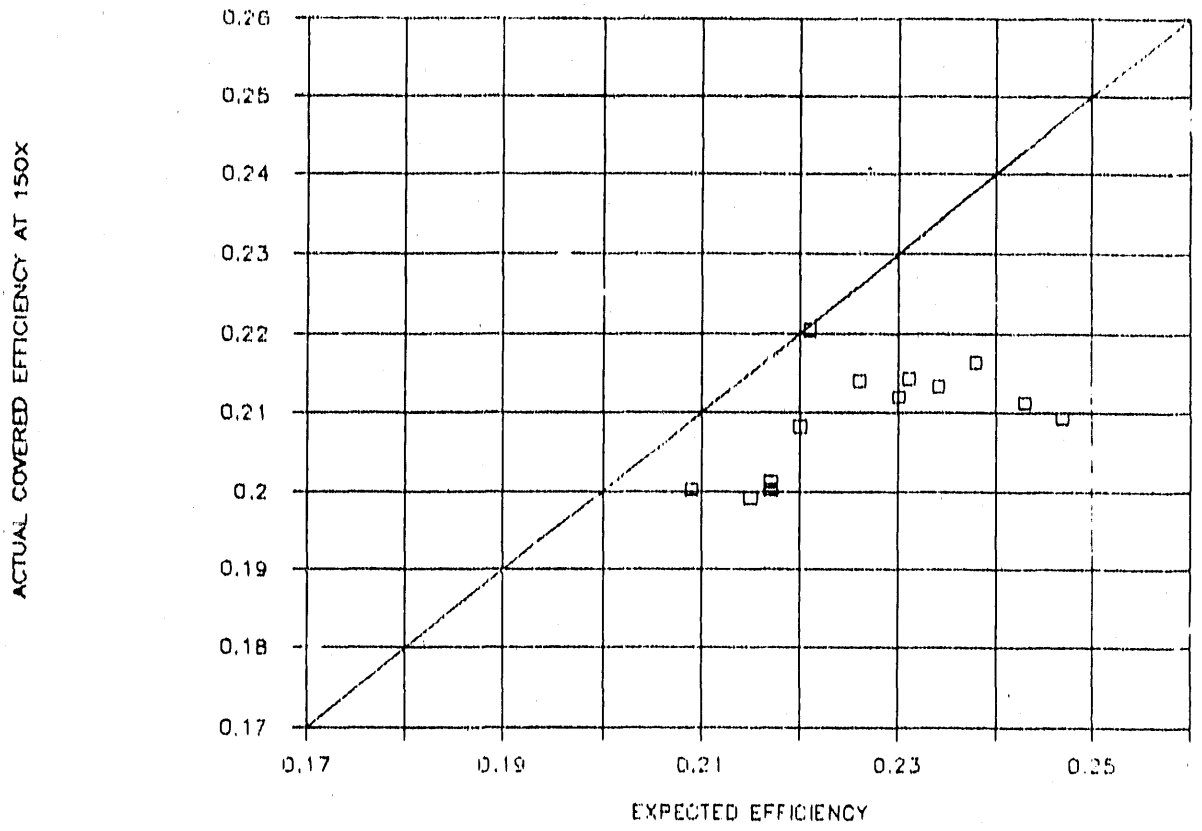


FIGURE 3-1
Covered Cell Efficiencies at Concentration vs. Expectation

3.2 Analysis of Covered Cell Losses

To understand the apparent discrepancy between the efficiencies of covered cells shown in Figure 3-1 and expectations based on active area efficiencies of uncovered cells, a series of LBIC (Laser Beam Induced Current) scans were performed by Sandia. Figure 3-2 shows a LBIC scan which traversed the diagonal of a covered cell (12-5-1) perpendicular to the gridlines. Some relative loss in generated current occurs as the busbar is approached at either end resulting in a loss of approximately 5% in potentially available short-circuit-current. There are also a few downward "spikes" which correlate with visual defects in the covered cell such as minor cover delaminations and local misalignments. Patches of reflective areas that form Moire patterns [15] between the gridlines and coverslide "prisms" were noticeable in varying degrees on many of the covered cells. The reflectivity appeared to be a strong function of the angle of incidence and was frequently noticeable near the periphery of the cell illuminated area.

Figure 3-3 shows LBIC results from a scan across the diagonal of a cell (13-A3-10-3). A prismatic cover was applied and then removed from the portion of the cell shown on the right-hand side of Figure 3-3. The maximum current generated from the covered section of the cell is approximately 2-3% less than the normalized current generated in the uncovered section. This is the result of reflection losses from the top surface of the prismatic cover and is consistent with the conclusions of section 2.3.

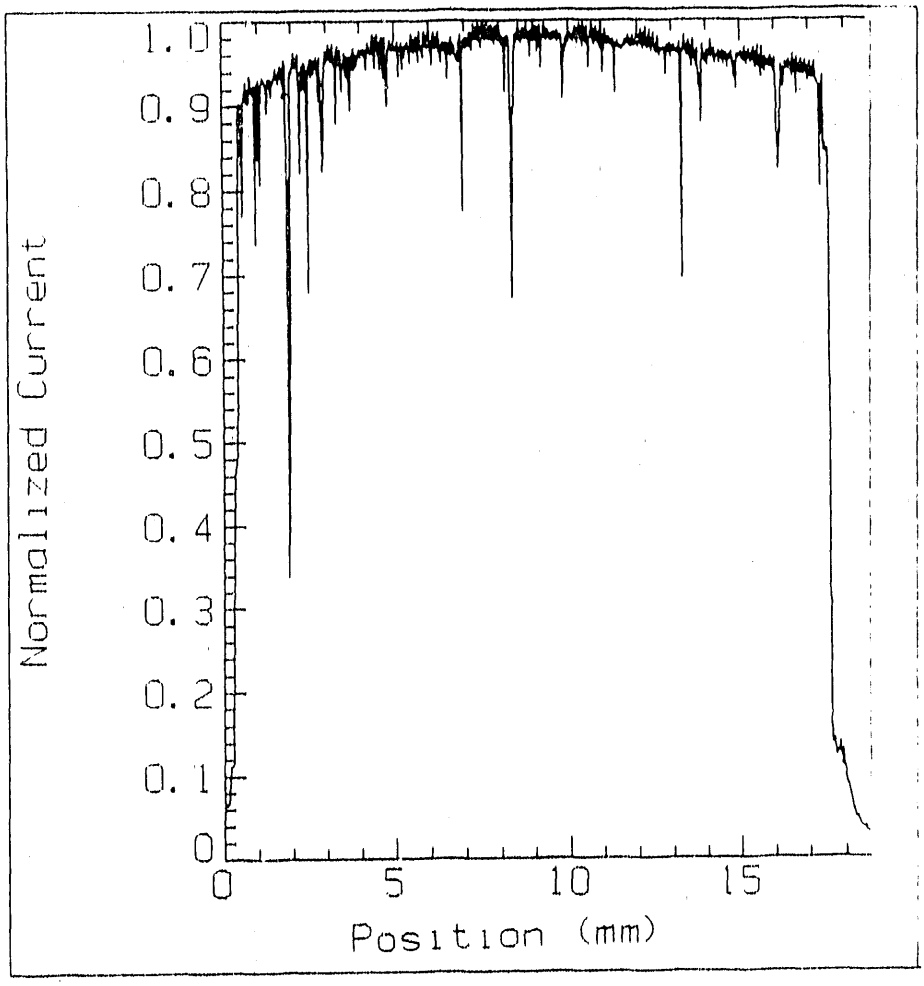


FIGURE 3-2
LBIC Scan of Covered Cell

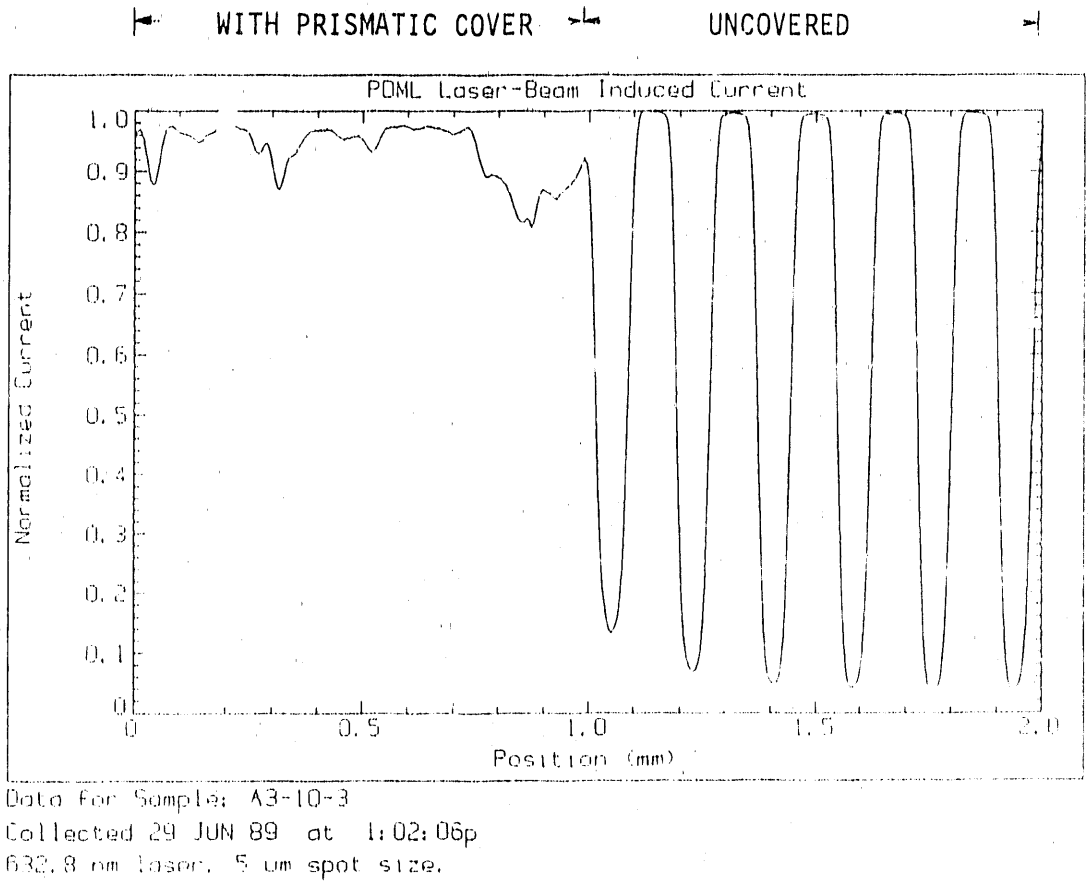


FIGURE 3-3
LBIC Scan of Cell with Cover Partially Removed

The combined losses from cover defects and reflection from the top surface of the prismatic cover, however, do not account for the entire discrepancy between actual covered-cell results and expectations. The LBIC scan of Figures 3-4 and 3-5 show how uncovered cell short-circuit-current densities were overestimated because of reflection of incident light into the cell active area.

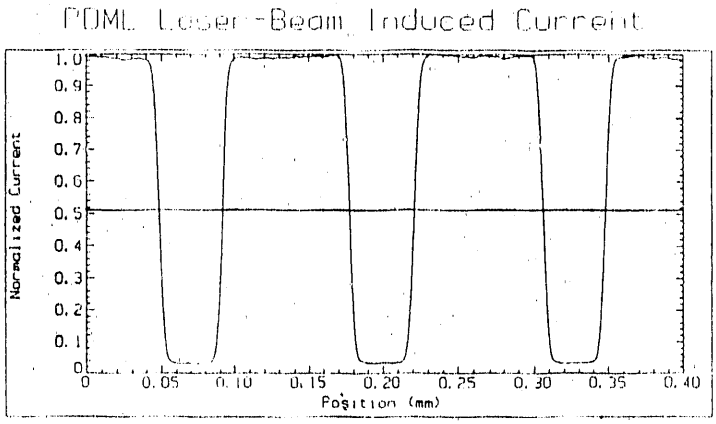


FIGURE 3-4
LBIC Scan of Uncovered Cell

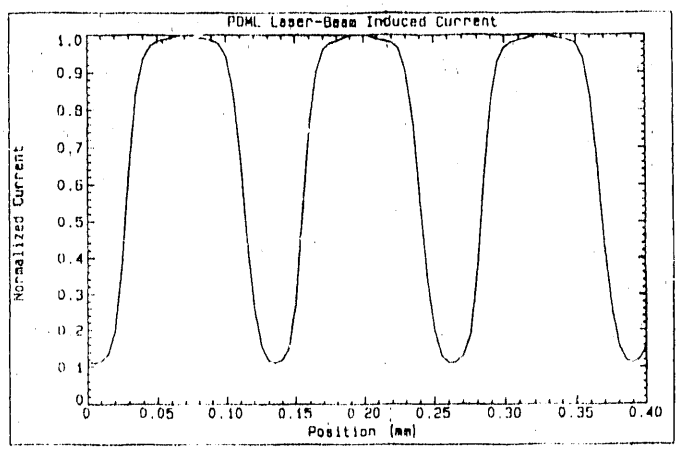


FIGURE 3-5
LBIC Scan of uncovered cell

Figure 3-4 shows a LBIC scan across an uncovered cell (7-D2-7). When the laser beam traverses the gridline there is (almost) no current generated. The transition to the active region is fairly sharp and occurs over a distance approximately on the order of the beam width. For this cell, the gridline width calculated using the distance between points at which 50% of the normalized light is generated is fairly close to the optically determined linewidth. However, the opposite is the case in Figure 3-5 in which the scan across the uncovered cell (B2-5) shows varying amounts of current generation as the laser beam moves across the gridline. The curve never approaches zero current generation, apparently the result of light being reflected from the gridline into the cell active area. As a result, the short circuit current measured on uncovered cells is deceptively high and leads to an over-estimation of the active area efficiency.

4 MANUFACTURING TECHNIQUES

Table 4-1 provides a detailed list of steps used for the final cell fabrication groups.

4.1 Comparison with Conventional Cell Fabrication Techniques

The cell fabrication sequence described in the previous section, requires approximately two weeks for a trained technician to complete. This is roughly twice the time required to process a standard space qualified silicon solar cell at Solarex. The only non-standard equipment used is a mask aligner.

Several critical requirements, not significant in conventional cell processing, are important:

- Maintaining accurate alignment of sequential photomasking steps
- Controlling diffusion conditions with lower dopant concentration to be compatible with subsequent oxide growth steps
- Keeping passivating oxide sufficiently thin so as to not reduce effectiveness of the antireflective coating
- Obtaining heavily doped silicon with relatively long minority carrier lifetimes
- Maintaining a higher degree of cleanliness for wafers and process equipment than is typically required for space cell fabrication

4.2 Prismatic Cover Attachment

Although excellent results have been achieved by Entech, Inc. by attaching prismatic covers to very similar devices fabricated at the University of New South Wales [16], some additional optimization may be appropriate before the technique is used in a large-scale production environment.

As stated in section 3.1, we believe that covered cell performance falling short of expectations to be largely the result of over-optimistic active area efficiency measurements. In addition, however, some covering losses--such as local misalignments, delaminations, and lens shape modifications caused by adhesive in the grooves -- may be avoidable in the future. The process, as applied to these experimental cells requires a fairly high degree of personal skill and experience and might be difficult to control in production. An experimental technique being studied at Sandia to directly mold covers onto cells covered with silicone rubber may be a step in the direction of solving that problem.

TABLE 4-1
CELL FABRICATION SEQUENCE (EXPT 14)

STEP	COMMENT
ETCH	
ETCH	325 MICRONS, 25% NaOH
CLEAN	
TEXTURE MASK	
GROW OXIDE	WET O_2, 950 DEG C FOR 3 HRS
PHOTOLITH 1	
HF/RESIST REMOVAL	OPEN ACTIVE AREA TO BE TEXTURED
KOH ETCH TEXTURING	
KOH	4% SOLUTION WITH IPA, 100°C, 12 MIN.
CLEANING	RANDOM PYRAMIDS 10 MICROMETERS HIGH
DEEP DIFFUSION MASK	950 DEG C IN PHOSPHINE FOR 15 MIN
LIGHT DIFFUSION PATTERNING	
PHOTOLITH 3	
HF/RESIST REMOVAL	OPEN EMITTER REGION
RCA CLEAN	
LIGHT DIFF.	832 DEG C, REDUCED PH3
THIN OXIDE GROWTH	
RCA CLEAN	
THIN OXIDE	980 DEG C FOR 3 HRS
ALUMINUM ALLOY/HCL	ALUMINUM PASTE
OXIDE PATTERNING	
PHOTOLITH 4	
HF/RESIST REMOVAL	OPEN AREA FOR OPPOSITION OF BUSBAR INSULATION
CLEAN	
SiO2 EVAPORATION	
PHOTOLITH 5	
SiO2 EVAP.	1200 ANGSTROMS
RESIST REMOVAL	
METAL MASK	
PHOTOLITH 6	DEFINE GRIDLINE & BUSBAR PATTERN

TABLE 4-1 (continued)
CELL FABRICATION SEQUENCE (EXPT 14)

STEP	COMMENT
FRONT EVAP	2500 ANGSTROMS Ti, 1600 ANGSTROMS Pd
LIFTOFF	
BACK EVAP	2500 ANGSTROMS Ti, 1600 ANGSTROMS Pd
AG	50% COVERAGE, 8-10 MICRONS THICK
AR	¼ WAVELENGTH TiOx, Al_2O_3
SAW/SINTER	
TEST	AM1.5 DIRECT

5 CONCLUSIONS

5.1 Potential for Manufacturing High Efficiency Concentrator Cells

Throughout this program, our capability of producing high-efficiency solar cells progressed as we incorporated high-efficiency fabrication techniques into the manufacturing environment at Solarex.

Use of concentrator solar cells designed for use with a prismatic cover clearly have the advantage eliminating the compromise between shadowing and grid conductance losses.

We did not come as close as we would have liked (or expected prior to the results of section 3.2) in closing the gap between the state-of-the-art established at the University of New South Wales or Stanford and commercial solar cell production. However we did develop a technique that we believe has the potential--with some additional optimization -- for producing large numbers of high-efficiency concentrator cells.

5.2 Future Directions

Several areas stand out as possibilities for further work:

- Steps could be taken to further improve wafer cleanliness during high temperature oxidation and diffusion steps. Because equipment was not available at Solarex to safely introduce 1, 1, 1 Trichloroethane (TCA) into our quartz tubes, we relied on modified cleaning techniques which perhaps resulted in less than optimal bulk and surface properties.

- It is possible that the process sequence could be simplified to eliminate one or more of the photolithography steps.

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