LBL--32246

DE93 010446

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October 1992

This work was supported by the Director, Office of Energy Research, Office of High Energy and Nuclear Physics, of the U.S. Department of Energy under Contract No. DE-AC03-76SF00098.

A HIGH RESOLUTION 14-BIT ADC FOR GAMMASPHERE PROJECT

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ABSTRACT

A system of 110 high performance A/D converters, required for the Gammasphere Project at the Lawrence Berkeley Laboratory, is described. The ADCs are compact, linear (±0.006% integral, ±0.5% differential), with a conversion deadtime of 5.3 μs and channel profile flatness of 50% over a 13-bit range. The converter is based on a new low power (0.25 W), low cost, monolithic high speed sampling ADC, exibiting a very high stability and no missing codes over the entire 16-bit range. Differential linearity was achieved by applying the "Gatti method", covering a 8-bit range. Measured data and methods of testing the ADC are also presented.

I. INTRODUCTION

A high performance analog-to-digital converter was designed for supporting a large Gammasphere Detector System under development at the Lawrence Berkeley Laboratory [1]. The system consists of 110 large Compton-suppressed Ge detectors (Fig.1) that will greatly surpass detection efficiencies reached in the past. The steps in analog processing of detector signals include a fast, economical ADC, having a differential nonlinearity of 1% or better over the 13-bit range.

A number of commercially available ADCs meet some of the requirements (such as range, integral linearity, conversion rates, power consumption, size and cost). All of them exibit poor differential nonlinearity of 100% at best, far from the 1% goal. However, the nonlinearity can be reduced to the desired level by implementing the "Gatti method" [2], also known as the sliding scale method, or "dithering".

The basic idea of the method is to add a voltage pedestal to the analog input signal before each A/D conversion. A digital equivalent of the pedestal is later subtracted from the data before the readout. The pedestal magnitude is different for each conversion. Such an averaging, if performed over a sufficient portion of the ADC range, will reduce the differential nonlinearity to a desired level.

A new monolythic, low power 16-bit track/hold ADC (Analog Devices' AD7884) has become recently available [3], having most of the characteristics close to (or surpassing) the required ones. Some of the most important are:

Conversion time:	5.3 μs
Resolution:	16 bit
Integral linearity:	±0.006%
Gain/offset TC	±2 ppm/°C
Noise	120 μV rms
Power	250 mW

A differential nonlinearity of ±0.5 LSB and no missing codes over the entire signal range covering 16 bits are guaranteed. However, over the 14-bit range (by eliminating the last 2 bits), the resulting differential nonlinearity of 0.25 LSB is still too large. Linearity was reduced to the desired level by implementing the Gatti method mentioned above. However, the circuit complexity and power dissipation have increased accordingly.

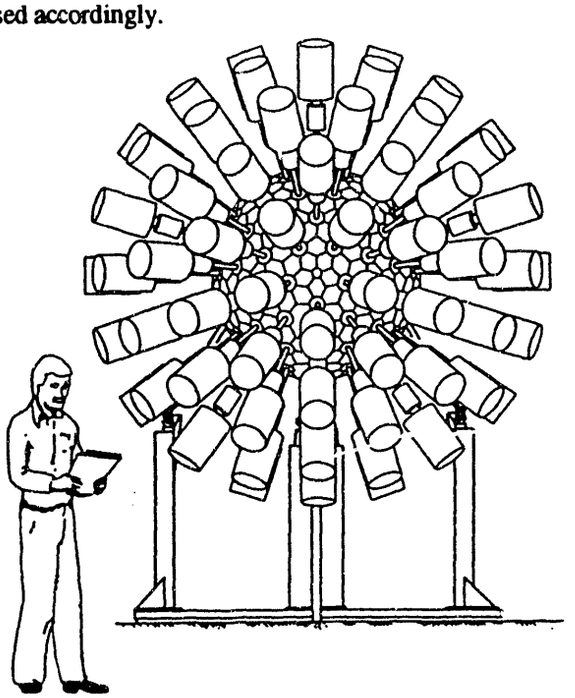

Fig.1. A sketch of the GAMMASPHERE detector system.

II. DESCRIPTION OF THE ADC

The ADC was conceived as a complete, self-contained unit. All components are SMT, placed on one side of a small (2"x3") P.C. board. The other side has connecting pin strips for an easy detachment from the supporting mother-board. The advantage of this approach is that all ADCs in the system are identical and thus interchangeable. Also, mass production is simple and therefore less expensive in spite of the larger number of components per ADC. Isolation from sources of noise is improved and crosstalk between ADCs is reduced by keeping them separated. It is also believed that such a device can be used in many other applications where high performance and inexpensive ADCs are required.

A block diagram of the ADC is shown in Fig.2. The ADC input, in a range from 0 V to +10 V, brought from analog processing circuits, must be offset by an inverting amplifier in order to accomodate the AD7884 operating range of ±5 V. A precision +5 V reference provides the voltage for adjustable offset and serves as an external reference supporting both AD7884 and a 12-bit DAC. Additional amplifiers (A1 through A4) serve as secondary reference source followers in order to keep the required voltage levels as rigid as possible.

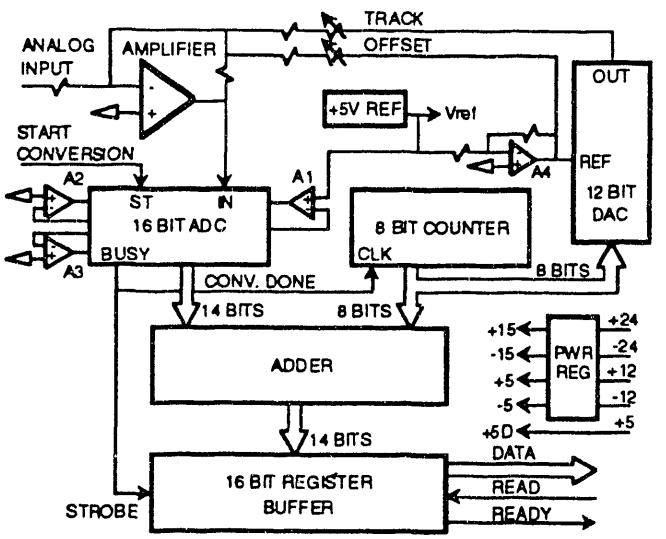

Fig.2. Block diagram of the 14-bit high performance ADC.

The ADC, when not busy, tracks the input signal all the time. A conversion starts upon the receipt of an external command, made to coincide with the peak of the ADC input signal. At the end of conversion, a 14-bit adder is used to sum the ADC data and the contents of the 8-bit counter, in order to compensate for the analog offset provided by the DAC.

The adder output is next stored in a buffer register by a properly delayed strobe pulse. A read ready signal is then sent into the dataway. Out of the register's 16 bits, 14 bits are used for data and the remainder for externally provided tagging. At this time the counter is advanced by one count, changing the input amplifier offset in anticipation of the next conversion. The tri-state register data can be read out at any time by an external read command. The data is updated by each strobe pulse regardless of the read command timing.

Most of the circuits run on ±5V power supply, exept for the DAC, requiring ±15V. The Gammasphere system uses standard NIM voltages. In order to reduce these voltages to the proper level, each ADC board comprises also four subregulators. They provide additional immunity to noise and interference, which is in turn paid for by a slight increase in cost and power dissipation, from 1.5W to 2.5W.

III. EVALUATION OF THE ADC

A thorough evaluation of the 16-bit AD7884 ADC preceded its selection as a key component. A CAMAC-based test system was set-up (Fig.3), that is made compatible with IBM AT processors via a Crate Controller and an Interface Card, respectively. A program called VDIG, written specifically

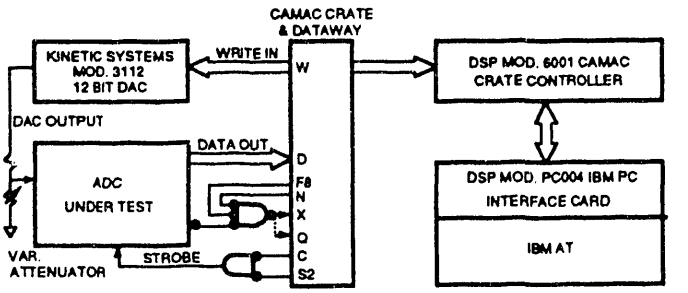

Fig.3. CAMAC-based test station for A/D converters.

for such evaluations, was used. The ADC under test presents the data to the CAMAC dataway through a simple interface card. A CAMAC compatible 12-bit DAC is also used for controlling the ADC input over entire range in programmable steps of a desired magnitude. The ADC can be also tested with externally provided calibrating signal sources, supplying shaped pulses at selected rates.

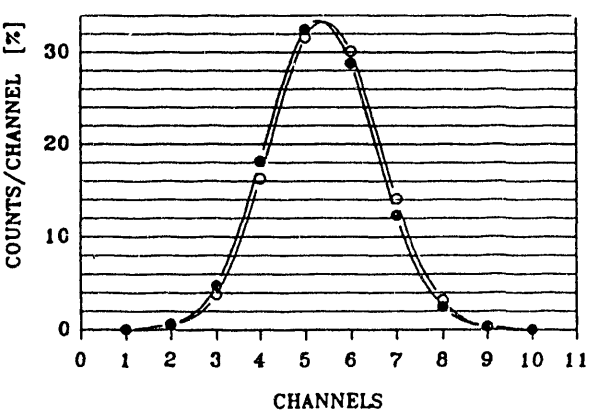

Fig.4. Distributions of 22,500 conversions of a constant D.C. input (ADC resolution: 16 bits; LSB calibration: 152 µV/channel). Hollow circles: dithering disconnected.

LSB calibration of the ADC set for a 16 bit resolution and 10V input signal range is 152 μV. Due to internal noise generated by the sample/hold and the ADC sections, conversion of a D.C. signal is distributed over several channels (1 channel = LSB). Two distributions, each containing 22,500 samples, are shown in Fig.4. One distribution was taken with the dithering connected and the other one without it. Except for a small shift, the two distributions are identical, proving that the linearization circuits do not contribute to the noise.

A good channel profile is required in ADCs intended for gamma ray spectroscopy. By reducing the ADC resolution to 14 bits, LSB gets wider four times, compressing the distribution of Fig.4 into a single channel. Channel profiles were then measured (Fig.3) by scanning the ADC input in small increments with the D.C. DAC output. The results (Fig.5) show that the dithering reduced slightly the flatness of channel profile. If the ADC resolution were further reduced to 13 bits (by eliminating the lowest bit), the two adjacent channels would merge, resulting in a channel profile almost 50% flat.

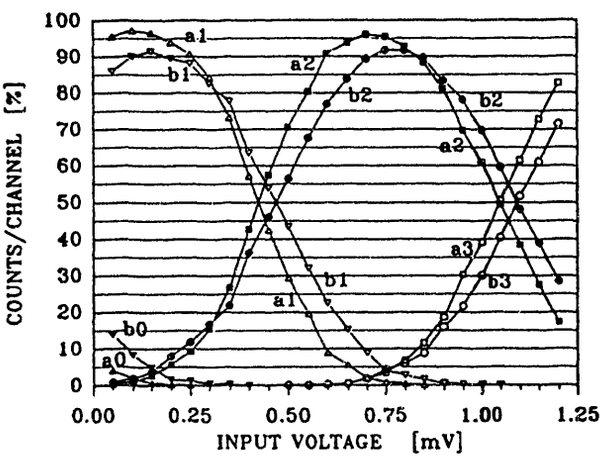

Fig.5. Profiles of arbitrary channels 1, 2 and 3 obtained by scanning the ADC (resolution: 14 bits) with a DAC (Fig.3). Curves a, obtained without dithering, exibit somewhat flatter tops.

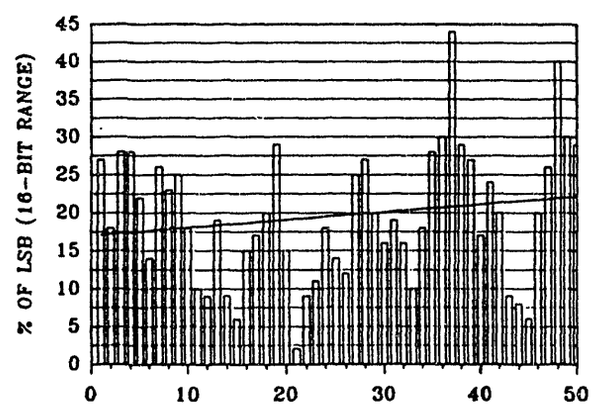

Fig.6. Hystogram of centroids (16-bit resolution) of 50 samples (22,500 conversions per sample) over a period of one hour shows a statistical variation of 68 μV and average drift of 15 μV. (Calibration: 152 μV/LSB).

In order to test thermal stability of the AD7884 ADC, 50 groups of 22,500 samples each were taken over a period of one hour. The ADC input was disconnected. The hystogram of centroids (Fig.6) shows a statistical fluctuation of 45% of the LSB (i.e. 48 μV). The average drift over that period amounted to 15 μV (solid line).

Integral nonlinearity of AD7884 alone was measured by scanning a selected portion of the range in fine voltage steps, generated by the DAC. A preset number of conversions per step was performed and the centroid calculated. Such a plot over five channels (16-bit resolution) is shown in Fig.7 (curve a). The increment per step at the ADC input was 3 μV, and 22,500 samples per step were taken. Curve b is a linear interpolation.

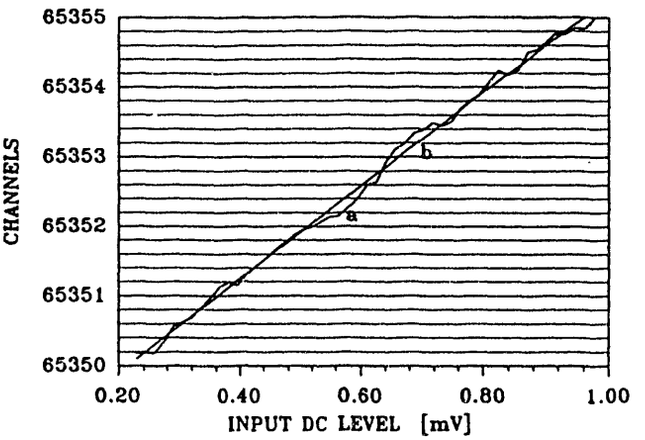

Fig.7. Integral nonlinearity test by scanning the ADC input in 3 μV steps (22,500 conversions/step averaged, curve a). Curve b is a linear interpolation of the data.

IV. REDUCTION OF DIFFERENTIAL NONLINEARITY

Ramping pulse generators are usually used for testing a differential nonlinearity of ADCs. In this case, BNC Inc. Mod. PB-4 and LG-1 (Pulse and Ramp Generators, respectively) were used (Fig.8). Also, a modified IBM PC-based Pulse Height Analyzer (Nucleus, Inc. PCA) stored and sorted the ADC data, covering a range of 13 bits. The Analyzer's internal ADC was disconnected for this test.

The AD7884 ADC alone exibits unusual differential nonlinearity patterns, as seen in a plot of first 2000 channels (the range was 13 bits, Fig.9). Depending on the unit under test, the spikes may point in either direction.

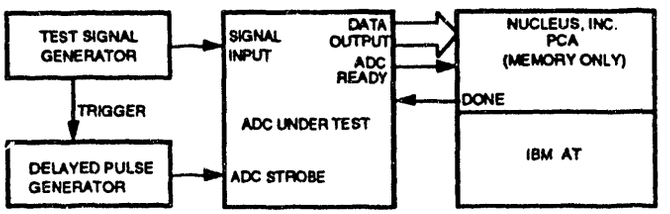

Fig.8. Test station for the measurement of differential nonlinearity.

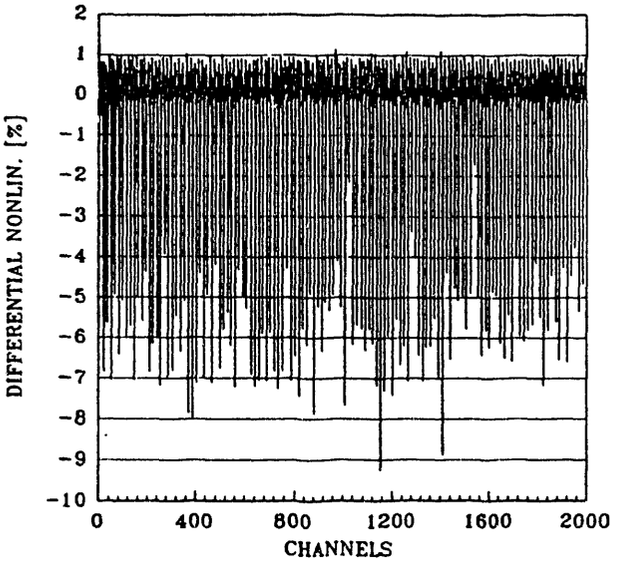

Fig.9. Differential nonlinearity plot of AD7884 (first 2000 channels of the range reduced from 16 bits to 13 bits).

This kind of differential nonlinearity pattern is desirable, because much narrower dithering range is required to smooth down the spikes to a desired percentage. Many earlier ADCs exibit strong binary patterns in differential nonlinearity over the whole ADC range. Dithering in such cases must cover a large portion of the signal range, making the linearization process more difficult.

A section of 250 channels (Fig.10a) is taken as an example for demonstrating the reduction in nonlinearity as a function of dithering range. The process is simulated in several steps. In Fig.10b dithering was simulated over a 1-bit range, in Fig.10c over a 2-bit range and so on up to Fig.10f (5-bit range). The scale of Fig.10f is expanded in Fig.10g.

V. ADC PERFORMANCE AND CONCLUSIONS

Several ADCs were built and tested so far. Only a limited number of AD7884 samples are available at this time. The SMT version of the ADC is to be releasd soon. All the tested units performed uniformly and very well.

In addition to the tests described above, designed for evaluating ADC's characteristics, a number of real spectra was measured with an ORTEC/EGG, Inc. germanium detector (diameter: 70 mm, lenght: 80 mm) [4]. A Co^{60} spectrum (Fig.11) had been collected for a period of three days. The spectrum in Fig.12, also collected over a three-day period, shows a background radiation including traces of contaminating radioisotopes in the test area.

Differential nonlinearity of ±0.4% (Fig.13) was tested with a ramp generator. Taking into account that the average number of counts per channel, 680,000, was relatively low, the nonlinearity is actually even better.

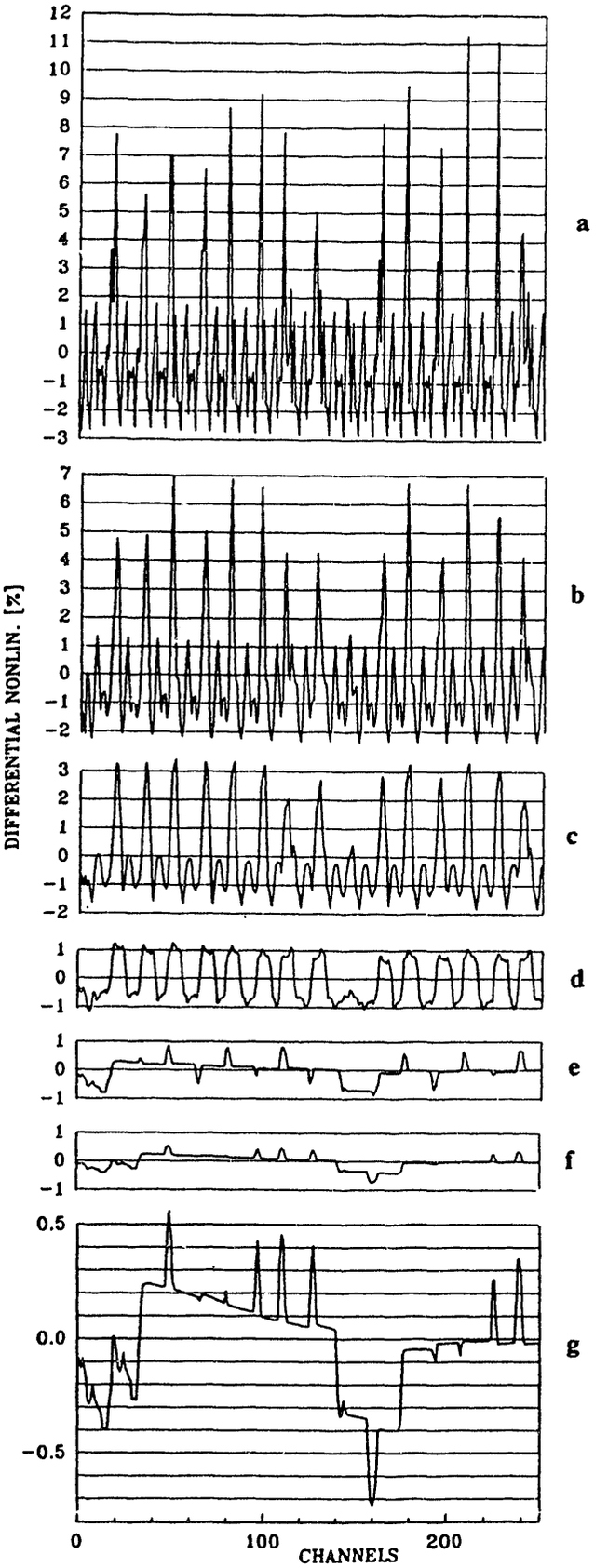

Fig.10. Simulation of the effect of dithering range on the reduction of differential nonlinearity; a: A section of 250 undithered channels; b through f: Simulated dithering over a range of 1, 2, 3, 4 and 5 bits, respectively.

The high-performance ADC, described here, met all (or surpassed some) design goals except for conversion deadtime. Original requirement was 5 μs or less. This parameter, 5.3 μs, was given as a preliminary value by the manufacturer of AD7884. All tested units met the above specification and it is believed that the final specification will be the same. However, even somewhat longer deadtime is acceptable for the Gammsphere System and is not considered critical.

Fig. 14 is a photograph of the complete ADC. A simple, 2"x3", 3-layer P.C. board is easy to test and maintain. For high-density packaging, the ADCs can be stacked back-to-back in pairs or lined up in a row. Low dissipation per unit eliminates many problems associated with the cooling of densely packaged systems.

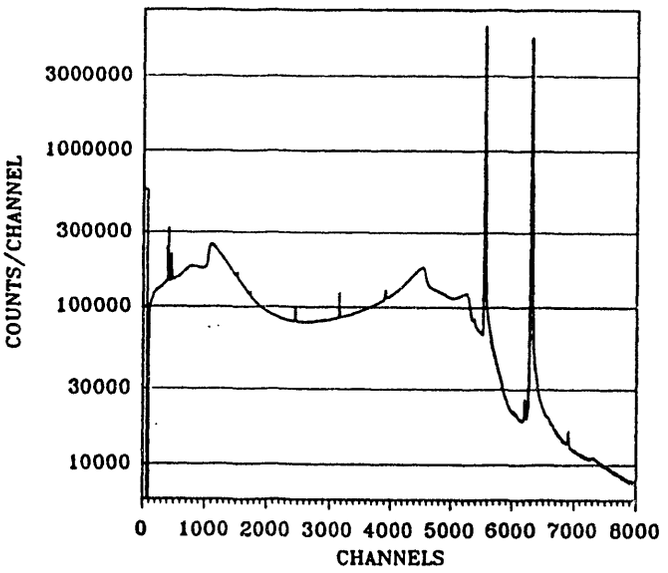

Fig.11. A Co^{60} spectrum, collected over a period of three days with a Germanium Detector.

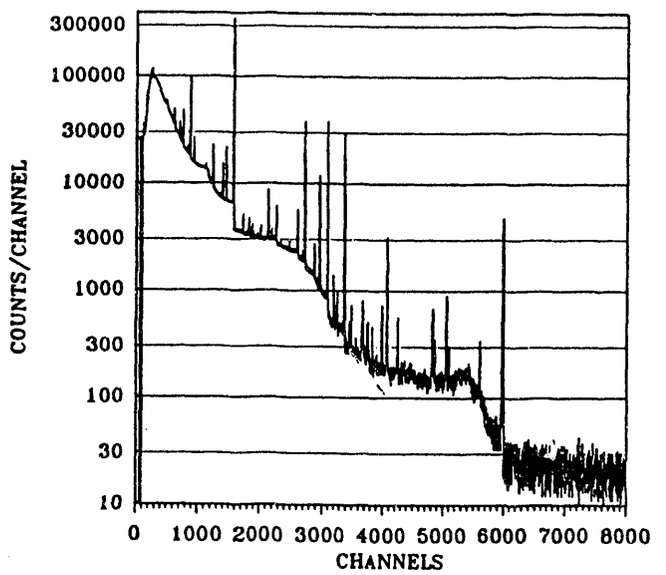

Fig.12. Background radiation in the experimental area collected over a period of three days.

VI. ACKNOWLEDGEMENTS

This work was supported by the U.S. Department of Energy under Contract Number DE-AC03-76SF00098. Reference to a company or a product name does not imply approval or recommendation of the product by the University of California or the U.S. Department of Energy to the exclusion of others that may be suitable.

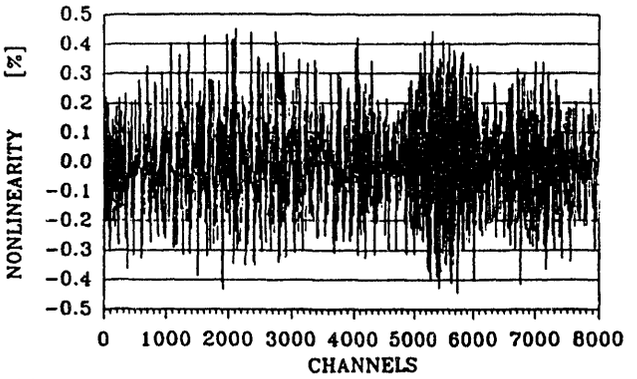

Fig.13. Differential nonlinearity measured with a ramp generator (mean: 680,000 counts/channel).

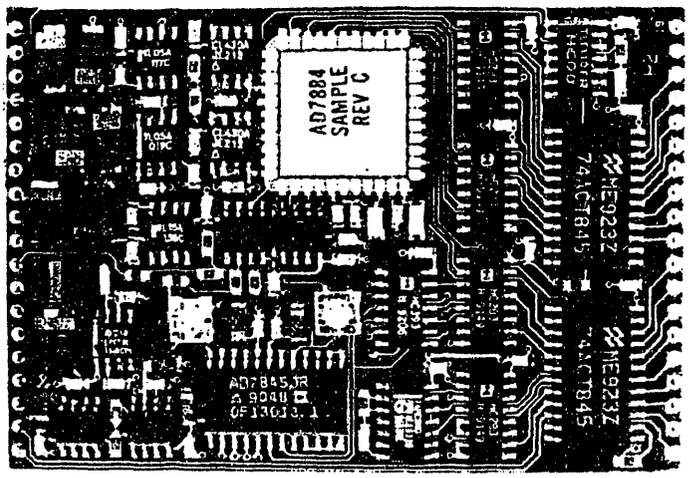

Fig.14. All-SMT, 2"x3", three-layer P.C. board has all ADC components on one side. The middle layer is a solid ground plane.

VII. REFERENCES

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