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The Use of Light Emission in Failure Analysis of CMOS ICs

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ABSTRACT

The use of photon emission for analyzing failure mechanisms and defects in CMOS ICs is presented. Techniques are given for accurate identification and spatial localization of failure mechanisms and physical defects, including defects such as short and open circuits which do not themselves emit photons.

I. INTRODUCTION

The accurate diagnosis and precise location of failure mechanisms and defects in CMOS ICs are often difficult tasks. Many techniques are available, but successful failure analysis requires careful selection of these techniques and the sequencing of their use. Nondestructive techniques are usually preferred if they are easy to implement and have a high probability of success. One such technique is photoemission microscopy, which utilizes the photons emitted by the defects themselves or by transistors which are operating abnormally due to the presence of the defects. Its attributes include high spatial resolution, simple sample preparation and installation, and absence of special environmental requirements.

Photoemission microscopy has been used for many years for specific analytical purposes and is being increasingly used as a general purpose tool for IC failure analysis. The first report of light emission from reverse-biased Si junctions has been attributed to Newman's paper in 1955 [1,2]. The correlation of nonuniform photoemission with silicon dislocations was shown by Chynoweth and Pearson in 1958 [3], who observed that only a small fraction of the dislocation sites emitted light. Other early papers reported the observation of uniform light from defect-free junctions [4] and investigated light emission from microplasma sites [5]. More recently, photon emission has been used to investigate silicon integrated circuit defects such as gate oxide shorts [6-8] and electrostatic discharge damage [8,9]. In addition, photon emission has been used to analyze IC failure mechanisms including latch-up [10,11], snapback [12-14], hot-carrier degradation [15-17], and defect-free structures in "normal" operation, including dielectric films [18], MOS transistors [13,14,19], and ICs [15,17].

Photoemission microscopy for IC analysis has commonly been performed using conventional microscope optics in a low ambient light environment with relatively unsophisticated electrical stimulus. Some companies have developed custom photoemission systems with image intensifiers and specially-adapted optics and electronics. Fortunately, for those unable to develop this themselves, commercial photoemission microscopes have become available during the past several years which combine night vision technology with computer image processing to achieve submicrometer spatial resolution. As a result, photoemission microscopy is now a widely recognized tool for mainstream IC failure analysis.

Commercial manufacturers of photoemission microscopes are beginning to provide optional equipment, such as notch filters, which may be used to help identify physical mechanisms by their spectral characteristics [20,21]. The spectra published by Chynoweth and McKay for Si junctions are widely referenced [22]. Other papers provide recent spectral data for dielectric films [21], gate oxide shorts [21], p-n junctions [11,21], latch-up [11], ESD damage [21], and hot carriers in MOSFETs [16,21,23,24]. The motivation for these efforts centers on understanding the mechanism(s) for light emission generation. An additional incentive is the possible use of light emission spectra as a signature for distinguishing between different types of light emitting sources. The use of spectral signatures has increasing utility as multilevel, submicron structures make optical imaging of defects more difficult.

Proper use of photoemission microscopy as a failure analysis tool requires consideration of the IC design and how the transistors in the IC are electrically driven (stimulated). Both of these factors have a great influence on photon emission from defects and defect-free structures within the IC. For example, it has been shown that some types of gate oxide shorts emit light only under certain bias conditions [25,26]. And it has been observed

that certain defects, such as interconnection shorts which do not emit light themselves, may cause emission of transistors connected to the shorted node, leading to the possibility of misdiagnosing the failure as a transistor defect instead of a bridging short.

This paper reviews the use of photon emission for analyzing failure mechanisms and defects in CMOS ICs. Data are presented for pn junctions, test transistors, test circuits, and CMOS ICs. Techniques are given for accurate identification and spatial localization of failure mechanisms and physical defects, including defects such as short and open circuits which do not themselves emit photons.

II. METHODOLOGY

Several electronic structures were investigated for light emission properties and the relationship of these properties to their associated currents and bias conditions. These structures include: (1) diodes, (2) n- and p-channel test transistors, (3) a 49-stage ring oscillator, and (4) four ICs that had different types of defects which were localized using photoemission microscopy. The diodes and transistors provided base knowledge of device behavior and the circuits provided a verification of these properties at higher integration levels. All measurements were performed at room temperature.

The diodes were square n^+ regions with 1000 μm sides in p-wells. The diodes were evaluated to provide a reference for the analysis of the transistors. The characteristics of the individual n-channel and p-channel test transistors are shown in Table 1 below. All of these transistors had polysilicon gates with no metallization over the gate region. The 1.25 and 1.75 μm transistors were fabricated with a twin-tub process and all others were made with a p-well process. The 1.25 μm n-channel transistors had lightly doped drain (LDD) structures and the other transistors had conventional source/drain structures.

Two ring oscillators, each having 49 inverters, were evaluated. The n-channel and p-channel transistor width/length dimensions were 5/1.25 and 5/1.5 μm for the first oscillator and 20/1.5 and 28/1.75 μm for the second oscillator; the n-channel transistors had LDD and the p-channels were non-LDD structures. These oscillators were tested at V_{DD} = 5 V and at this voltage the self-oscillation frequencies ranged from about 25 to 35 MHz.

Photoemission microscopy has been routinely used at Sandia during the past 10 years for failure analysis of CMOS ICs made by Sandia and by commercial IC vendors. This work has resulted in numerous cases of successful usage of light emission to localize the root cause of failure. For this paper, four CMOS IC examples are given.

For all structures except the CMOS ICs, bias voltages were applied and I-V measurements were made using an Hewlett-Packard HP4145B Semiconductor Parameter Analyzer. Various conditions of drain and gate biasing were used, with drain voltages ranging from 0 to 10 V and gate voltages typically ranging from 0 to 1 V greater than the drain voltage. Stimuli were applied to the CMOS ICs with either the HP4145B interfaced through manual switches to the inputs or with production digital test equipment such as the Advantest T3342. Photoemission from the device under test (DUT) was simultaneously measured using an EMMI (Emission Microscope for Multilayer Inspection) model 1600W manufactured by KLA Instruments Corp. This system captures the image from an optical microscope and transforms it via the image intensifier and TV camera video into a digital format (Fig. 1a).

Table 1. Test Transistor Parameters

	channel length (drawn, μm)	channel width (drawn, μm)	drain structure	gate oxide thickness (Å)
n-channel	1.25	30	LDD	180
	2, 3, and 4	16	non-LDD	450
p-channel	1.75	30	non-LDD	180
	2, 3, and 4	16	non-LDD	450

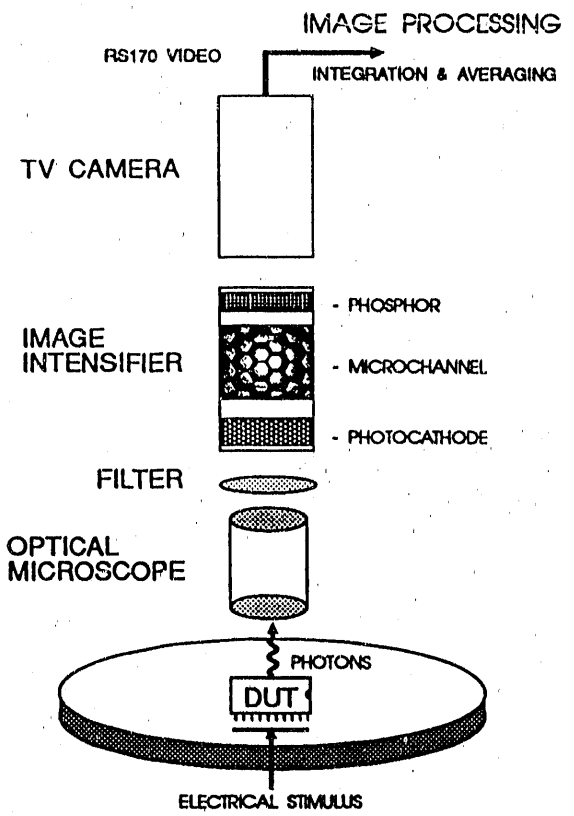

Fig. 1 (a) KLA EMMI photoemission system.

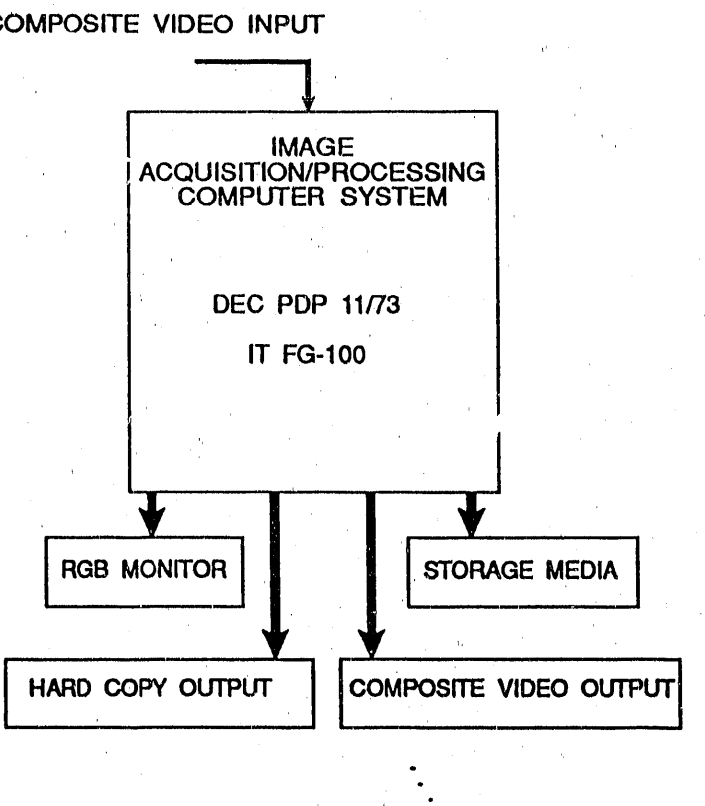

Fig. 1 (b) Sandia image processing system.

Software algorithms perform image processing on the digitized data to enhance the detection of the DUT photons. The detection sensitivity can be controlled by varying the analog integration (AI) time of the measurement and the number of signal averages (SA).

The relative photoemission intensity was measured using a custom image processing system (Fig. 1b). The custom image acquisition/processing system is based on a DEC PDP 11/73 minicomputer using an Imaging Technologies FG-100 frame grabber/image store. The composite video (RS170) output of the KLA EMMI system was digitized and stored to perform quantitative analysis, image comparison/enhancement, and hard copy production.

The modulation transfer function (MTF) for the whole photoemission system is a function of many factors, including the spectra emission from the IC, the material which the photons must pass through or be reflected around in the surface layers of the IC, the optical lens characteristics of the microscope, the notch filter bandwidth, the photocathode response, etc. The MTF for the system shown is largely determined by the S-25 photocathode response, which varied by a factor of 2 in the wavelength range from 400 to 800 nm and decreased by a factor of 50 at 1000 nm.

III. RESULTS

Diodes

The diodes were analyzed in the reverse bias condition. Light emission was observed in real time (without signal integration) as the magnitude of the reverse bias voltage was increased from 0 to 20 V. Avalanche breakdown of the diode occurred at about 19 V and light was not observed until the bias reached this magnitude. Initially, light spots formed at the corners of the diode structure; this location of emission is consistent with the higher electric fields that occur at the corners. Faint light emission with no signal integration was observed at one junction corner with diode current as low as 25 μA. As the reverse bias voltage was increased, a continuous ring of light formed at the edges around the structure. Although these diodes had no evidence of point defects,

it is common to observe light emission from random locations around the junction periphery which corresponds to the pre-avalanche leakage current characteristic of "soft", defective pn junctions.

Transistor pn Junctions

Light emission of the reverse biased drain to p-well junction of an n-channel test transistor (3 μm channel length) was also observed in real time as the reverse bias voltage was swept beyond the junction breakdown voltage. Initially light spots appeared at the outer corners of the drain junction boundary and then emission increased to a continuous line of light along the drain as the bias was increased.

n-Channel Transistors

The light emitting properties of the four different types of n-channel test transistors were measured. The light emission amplitude and associated drain and p-well currents were observed as a function of gate-source and drain-source bias voltages. Identical bias voltages, current measurements, and light emission amplitude measurement techniques were used for all four types of n-channel transistors. The differing transistor geometries were chosen to observe the light emission properties as the channel electric field strength was increased with decreasing channel length and constant V_{DS}.

The magnitude of the light emission for a given transistor was measured and was found to correlate with the magnitude of its p-well current (I_{PW}), an observation attributed first to Childs et al. [27] and subsequently reported by others [14,16,23,28]. The drain current (I_D) and I_{PW} magnitudes are given in Fig. 2 for the 2 μm channel length transistor with V_{DS} = 5 V as V_{GS} was swept from 0-6 V. Fig. 2 shows that the peak of I_{PW} occurs at approximately $V_{DS}/2$ while I_D continues to increase as V_{GS} increases. Light emission was observed for I_D values as low as 500 nA.

Fig. 3 shows a 3-dimensional (3-D) plot of the EMMI light emission data observed from the drain/p-well region of the same 2 μm channel length n-channel transistor. This image was collected with V_{GS} = 2.5 V (V_{DS} = 5 V) using a 100 video frame integration (AI) time. Light emission intensity was measured by integrating this signal (pixel intensity) over the image.

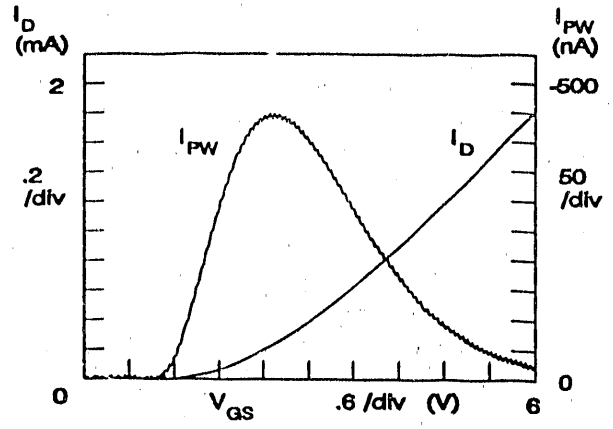

Fig. 2. I_D and I_{PW} as functions of V_{GS} (V_{DS} = 5 V) for an n-channel transistor with a channel length of 2 μm.

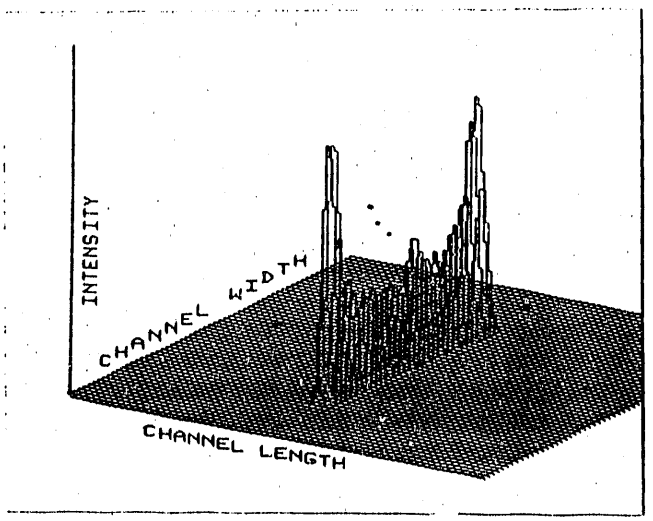

Fig. 3. 3-D plot of the EMMI light emission data observed from the drain/p-well region of the 2 μm n-channel transistor.

Fig. 4 shows a normalized plot of light emission intensity data (Fig. 3) as a function of V_{GS} (V_{DS} = 5 V). The shape of this curve is similar to that seen in Fig. 2 for I_{PW}, which is normalized and replotted in Fig. 4. The approximate correlation between light emission amplitude and I_{PW} can be seen in the two curves. An important observation is that significant light emission is found only in a restricted region of the saturated state of the transistor. Normal logic states (and some logic voltages produced by defects) cause transistors to be in a non-saturated bias condition and therefore to emit relatively low intensity light.

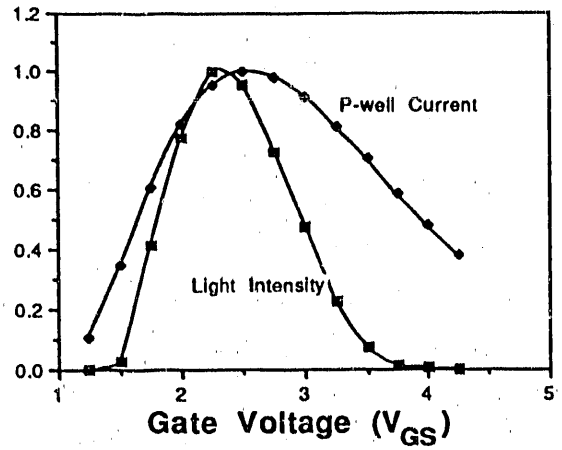

Fig. 4. Normalized plots of I_{PW} and the emission intensity for an n-channel transistor of 2 µm channel length as a function of V_{GS} (V_{DS} = 5 V).

In Fig. 5, the light emission amplitude for three different channel length transistors is plotted as a function of V_{GS} (V_{DS} = 5 V) and transistor channel length with the light emission normalized to that of the 2 µm transistor. The large increase in light emission observed for decreasing channel length (and hence increasing channel electric field strength) is apparent.

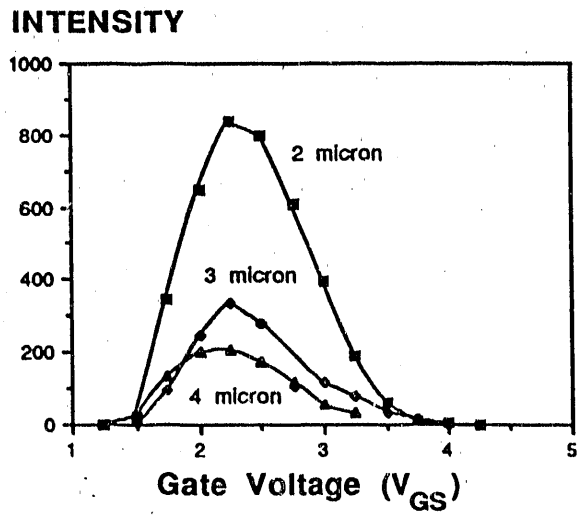

Fig. 5. Light emission amplitude as a function of V_{GS} (V_{DS} = 5 V) and transistor channel length for n-channel test transistors of 2, 3, and 4 µm channel length.

p-Channel Transistors

Currents and voltages (I_D, I_{SUB}, V_{GS}, V_{DS}) of the 2, 3, and 4 µm channel length p-channel test transistors were measured in a manner similar to that of the n-channel transistors. Light emission was not observable in any of the p-channel transistors at V_{DS} = - 5 V with V_{GS} = - 2.5 V using the EMMI maximum integration time of 2000 frames. V_{DS} was then increased to a maximum of - 10 V for the substrate current and light emission measurements of the 2, 3, and 4 µm channel length transistors. The substrate current was measured at V_{DS} = - 5 V for the 1.75 µm transistor. The much lower light emission associated with p-channel devices made higher drain voltage biasing necessary. Fig. 6 shows I_{SUB} and I_D as functions of V_{GS} for a 2 µm transistor with V_{DS} = - 10 V.

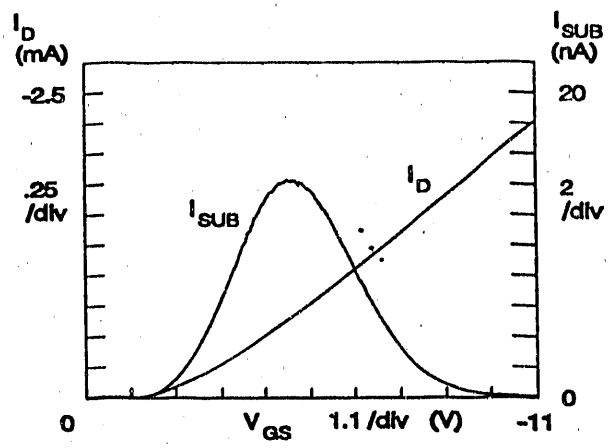

Fig. 6. I_{SUB} and I_D as functions of V_{GS} (V_{DS} = - 10 V) for a p-channel transistor with a 2 µm channel length.

For comparison Fig. 7 shows I_{PW} and I_D for a 2 µm n-channel transistor as a function of V_{GS} at V_{DS} = 10 V. Figs. 6 and 7 show approximately similar p- and n-channel transistors characteristics for their respective substrate and p-well photon-induced currents. The n-channel peak current was I_{PW} = 246 µA and the p-channel peak current was I_{SUB} = 14.3 nA. The ratio is about 17,000 and is an approximation of their respective light emission intensities under the same biasing conditions. Direct comparison of the photoemission amplitude over a 17,000X range is beyond the dynamic range capability (2000X) of the EMMI, so only a comparison of I_{SUB} and I_{PW} is possible.

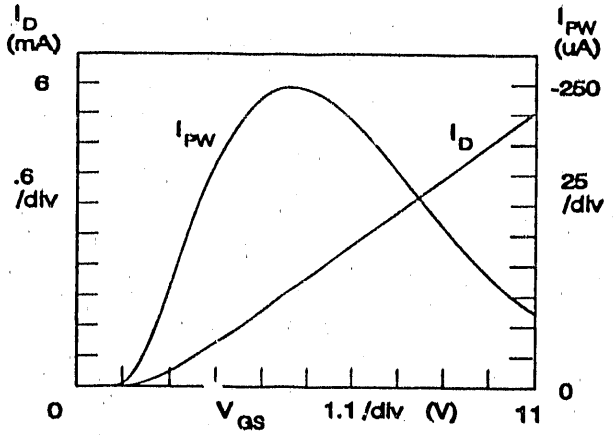

Fig. 7. I_D and I_{PW} as functions of V_{GS} (V_{DS} = 10 V) for an n-channel transistor with a channel length of 2 μm.

The magnitude of the light emission for the 2 μm channel length p-channel transistor again approximately correlated with the magnitude of the substrate current. Fig. 6 shows that the peak of I_{SUB} occurs at approximately $V_{DS}/2$ while I_D continued to increase as V_{GS} increases. Fig. 8 shows the normalized comparison of the integrated light emission signal and the normalized substrate current. As with the n-channel comparison, an approximate correlation is observed.

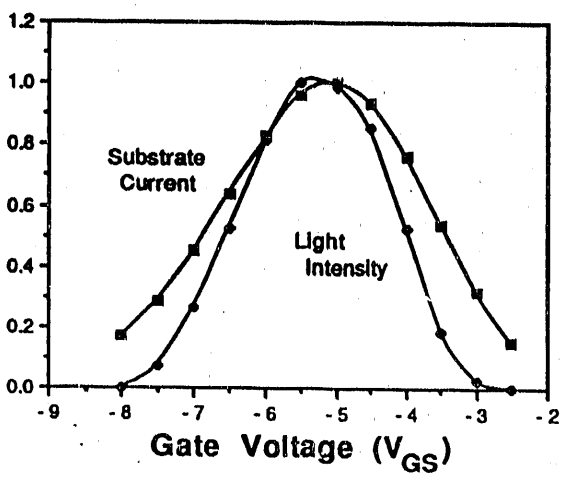

Fig. 8. Normalized plot of I_{SUB} and the emission intensity for the 2 μm channel length p-channel transistor as a function of V_{GS}.

Gate Oxide Rupture of an n-Channel Transistor

Several nondefective n-channel transistors were biased with a ramp voltage on the gate to p-well regions. At approximately 55 V, the transistor gate oxide ruptured. This formation of a gate oxide short was observed as a bright flash of light. The flash event was captured by videotaping the output of the EMMI during gate oxide rupture and then digitizing the video frame-by-frame (Fig. 9). This flash was interpreted as possible photoemission by energetic surface carriers due to current crowding (skin effect) on the surface of the conductor [29]. This current crowding may be due to high instantaneous current of capacitive discharge during the rupture event [30]. The duration of the light flash was probably much less than the video frame time (33 ms), but the saturation and slow response time of the photoemission system facilitated its observation. Note that the light flash bends towards the inner corner of the metallization where the electric field is concentrated and ends at a point on the transistor gate. This "end" point is the physical location of the gate oxide short. This phenomena was observed on several other gate oxide rupture experiments, including p-channel transistors.

Fig. 9. Transistor gate oxide rupture flash.

Ring Oscillators

Ring oscillators were used to demonstrate that light emission could be observed for transient switching situations. Each transistor in the ring emits light when it is saturated during the logic transition. The ring oscillator was allowed to operate while the EMMI performed a 300 frame integration of the light emission from the surface of the circuit. The oscillator frequency was about 30 MHz for V_{DD} = 5 V.

Fig. 10 shows the light emission from n-channel transistors of the ring oscillator. The light emission that occurs during the transition is individually too weak to detect for a single cycle, but over the course of many millions of cycles, light is detected in the 1.25 μm n-channel transistors of this circuit. It was not possible to observe emission from the 1.5 μm p-channel transistors of this circuit, which is consistent with the individual transistor emission characteristics described previously. This capability of photoemission microscopy to detect transient light events that would not yield sufficient emission in the static bias condition is useful for many CMOS circuits and for dynamic MOS circuits.

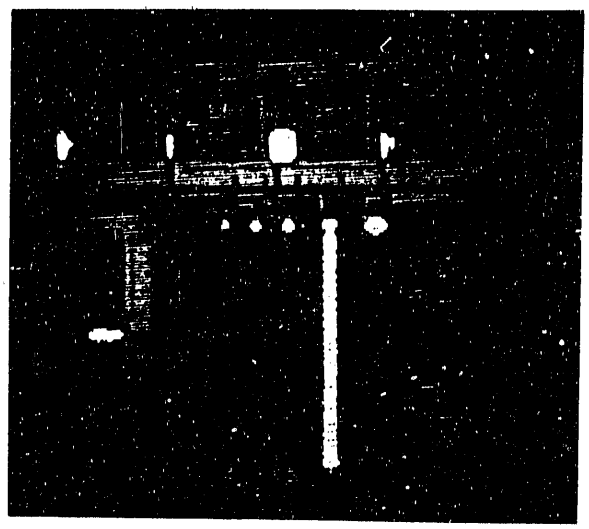

Fig. 10. Emission of light by the n-channel transistors in an operating ring oscillator.

Fig. 11 shows a transistor schematic for a conventional, static CMOS inverter. Fig. 12 shows the logic transfer and measured I_{DD} characteristics for this type of inverter. This inverter was made from one of each of the 2 μm channel length (16 μm channel width) n and p-channel transistors. For these measurements inverter input V_G varied from 0 to 5 V with V_{DD} = 5 V. The points where V_{GS} is approximately $V_{DS}/2$ for the n and p-channel transistors are shown on this figure as "N-CH" and "P-CH", respectively. These values are near V_{GS} = 1.9 V for the n-channel transistor and V_{GS} = - 2.4 V for the p-channel transistor (V_G = 1.9 and 2.6 volts respectively).

Fig. 13 shows the n-channel p-well (I_{PW}) and p-channel substrate (I_{SUB}) currents for the same inverter of Fig. 12. Note that the peaks of I_{PW} and I_{SUB} are within about 0.4 V of the $V_{GS} = V_{DS}/2$ points and that the peak of I_{SUB} occurs at nearly the same value of V_G as the peak of I_{DD}.

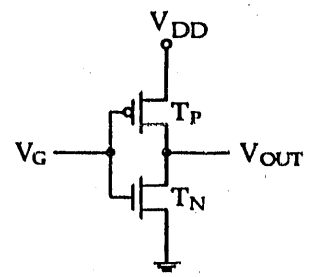

Fig. 11. Schematic for a CMOS inverter.

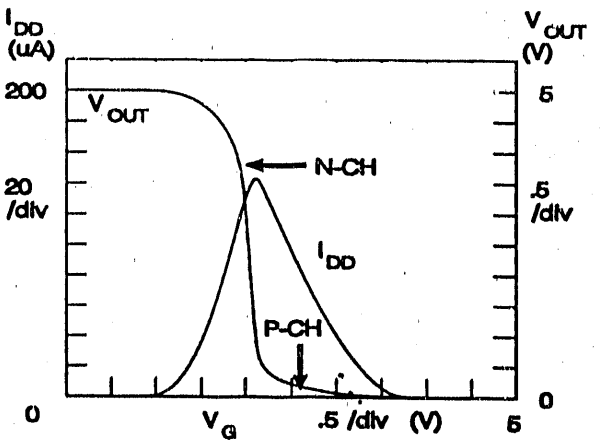

Fig. 12. I_{DD} and V_{OUT} as a function of V_G for an inverter showing the maximum emission regions for the n and p-channel transistors.

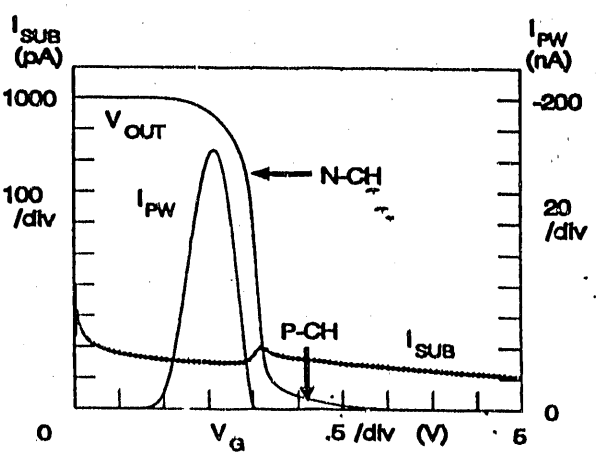

Fig. 13. I_{PW} and I_{SUB} as a function of V_G for the inverter of Fig. 11 (with V_{OUT} from Fig. 12).

The photon emission for the n-channel transistor T_N will follow the I_{PW} curve and will occur over an approximate range of $1.0\ V < V_G < 2.0\ V$, with peak intensity at about $V_G = 1.6$ V. It is significant for failure analysis to note that there is a region from $2.0 < V_G < 3.6$ V (Fig. 12, 13) in which elevated drain current exists, but I_{PW} and photon emission are absent. The p-channel does not emit significantly during the inverter transition as evidenced by the very small I_{SUB} peak of about 200 pA.

CMOS Integrated Circuits

Four cases are given from failure analysis performed at Sandia. These examples were chosen to illustrate the use of photoemission analysis to identify and localize physical defects in CMOS ICs.

Case 1: This IC was designed and manufactured by an ASIC vendor using a gate array technology with 1.5 μm transistor channel lengths (drawn). The IC performs a custom logic function with about 8100 logic gates. The photoemission analysis located multiple gate oxide shorts (Fig. 14).

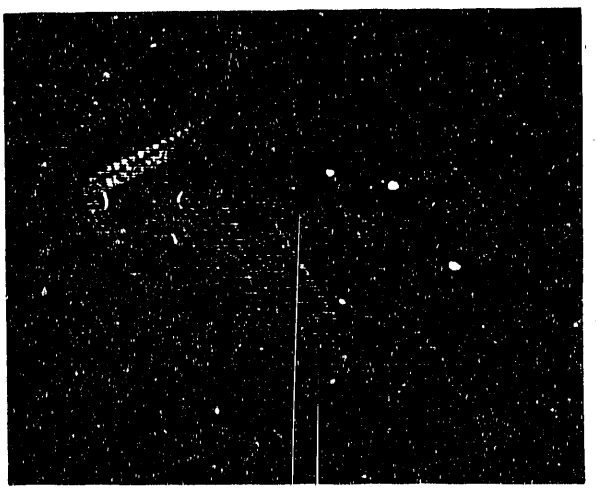

Fig. 14. Four light emitting gate shorts visible at IC power-up.

These light emitting gate shorts were observable simply by repeatedly applying power to the IC and observing the "random" power-up logic state (no input stimulus changes were applied after power-up). It was possible to change the power-up logic state (and therefore the gate oxide short bias/photoemission) by changing the microscope background illumination intensity during the power-up. The changes in the illumination produced variation in the power-up logic state due to the injected photocurrent effect on logic gate stabilization. For this case it was not necessary to utilize complex digital test equipment for the IC stimulus in order to successfully achieve photoemission for defect identification. This fortuitous occurrence of photoemission without the application of complex IC stimuli has often happened during failure analysis at Sandia, justifying the use of simple power-up and initialization/clocking techniques prior to the use of more complicated stimulus conditions. For these situations, it appears that defects can preferentially influence the power-up conditions so as to result in the most favorable logic (bias) condition for light emission. In some cases, however, it has been found to be necessary to utilize large digital test equipment to provide over 10,000 test vectors to the IC to produce the light emitting condition.

A different fabrication version of this IC had a parasitic n-channel transistor problem. Although these parasitic transistors were operating in a saturated bias condition ($V_G = V_D = V_{DD} = 10$ V), no light emission was observable with the KLA EMMI system. This occurred because the effective channel length for the parasitic transistors was very high (about 30 μm) producing a very low drain/p-well electric field. (I_D for each parasitic transistor was about 20 μA).

Case 2: A 16/32-bit microprocessor equivalent to the National 32C016 (about 65,000 transistors; 1.25 μm technology) had gate oxide shorts that could not be determined from random power-up logic conditions. A 15K test vector set was then cycled repeatedly through the IC while the EMMI was put in the integration mode. Four transistors having gate oxide shorts were detected (Fig. 15). This case illustrates that the integration mode of the EMMI can be used to find defects, again without identification of the specific test vectors responsible for producing light emission.

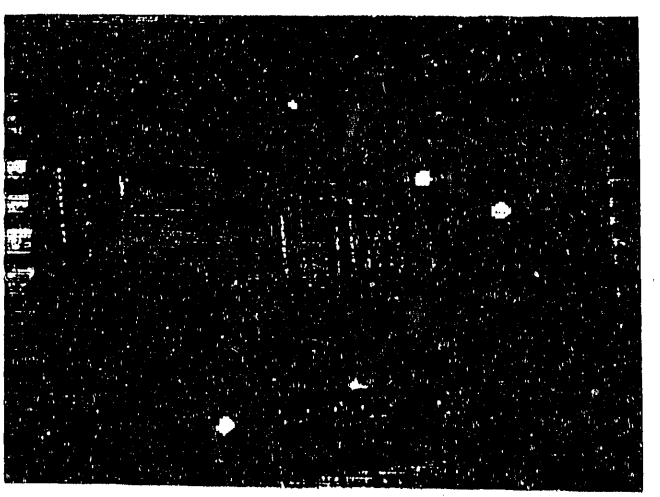

Fig. 15. Light emission visible from four gate shorts during repeated cycling of a 15K vector set.

Case 3: A functionally-failing 2-channel scaler IC of about 2000 transistors did not produce light emission for a normal application of vectors. However, it was noticed that the quiescent power supply current (I_{DDQ}) spiked for about 0.25 seconds during power-up. The EMMI was put in the integration mode and the IC was repeatedly powered up. Several n-channel transistors showed light emission in a row of flip-flops (Fig. 16). Upon further inspection, these transistors were found to not be defective, but were being driven by a clock line that had a metallization open circuit. The clock line provided the clock signal input to the flip-flops. The light emitting n-channel transistors were in the inverters which were the first gates connected to the clock input inside the flip-flops. This case illustrates another type of failure analysis situation in which the light emitting devices may not be defective, but their emission is a result of a defect or failure mechanism in the electrical (nodal) vicinity.

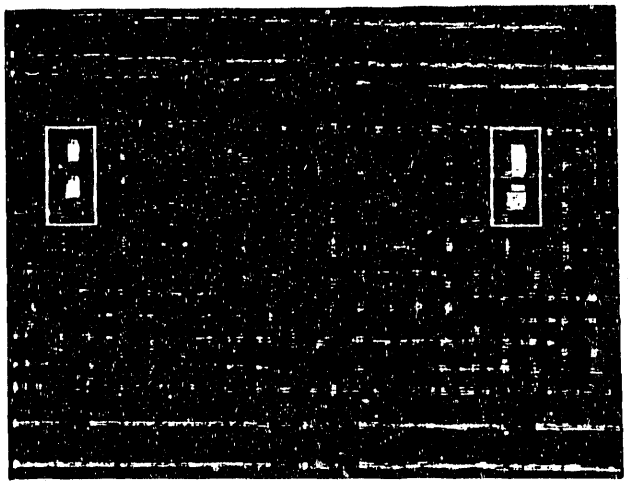

Fig. 16. Transient n-channel emission resulting from an open clock line.

Case 4: This IC is a custom interface controller with about 8000 transistors (2000 logic gates) and was manufactured using the same technology as the IC of Case 3 (Sandia's 4/3 technology: 4 μm minimum width metal and 3 μm minimum width polysilicon [6]). This IC failed due to a photoresist defect which produced a metallization patterning error that shorted the output of a 2-NAND to V_{DD}. Photoemission was observed in one of the n-channel transistors of this logic gate (I_{DS} for both 2-NAND n-channel transistors in series was about 4 mA at V_{DD} =5 V). The reason for light emission from only one of the two n-channel transistors will be discussed in the next section.

Spectral Analysis

Spectral measurements were made for a gate short, a reverse-biased diode, and an n-channel transistor in saturation. Notch filters were used on the EMMI system by placing them over the DUT. The results of this technique on three samples are seen in Fig. 17. The light intensity has been normalized and corrected for the detector's wavelength sensitivity and the signal integration time. The monotonically increasing intensity with wavelength has been observed previously [21,23,31]. The decrease in intensity at 800 nm for the gate short and diode is contrary to previous results. We currently are investigating other methods for spectral measurement to determine the source of discrepancy between our measurements and those of others.

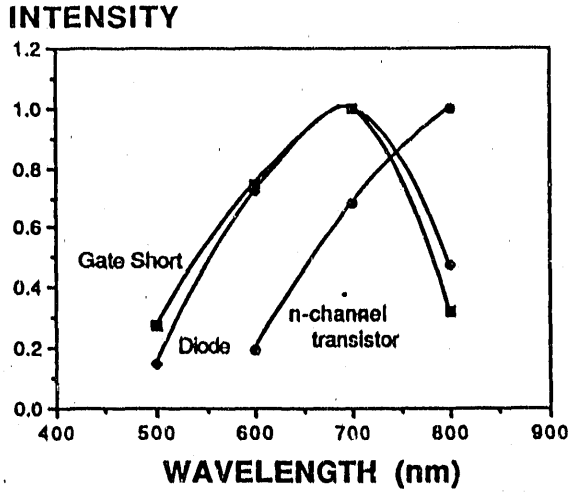

Fig. 17. Measured spectra for three different light emitting features.

Clearly more work is necessary to determine if spectral analysis of light emission is practical for source identification in integrated circuits.

IV. DISCUSSION

Photoemission microscopy is a powerful tool for CMOS failure analysis. In certain cases, small submicron defects or failure mechanisms can be identified within minutes of equipment setup with this nondestructive analysis technique. This technique is particularly useful in quickly locating certain defects, such as "soft" pn junctions and gate oxide shorts. The electrical stimuli (test vectors) required to expose these particular defects can often be the random states associated with power-up of the IC. For very low level defect light emission,

continuous cycling of the IC over many millions of test vectors can identify the defect using the photoemission microscope integration mode. The location of non-light-emitting defects by identification of hot electron photoemission in transistors driving the defect is less straightforward but can also be very effective. T data presented here and by others show that light emission will not occur unless the drive transistor has terminal voltages that place it into a saturated bias state. The saturated bias state is defined as the region where $V_{DS} > V_{GS} - V_T$ and $V_{GS} > V_T$ (V_T = threshold voltage). A high electric field in the channel is a necessary requirement for transistor photoemission. The magnitude of the drain current is not directly correlated with this photoemission.

Several factors may increase the hot carrier light emission for a particular transistor: (1) enhanced AC biasing effects, (2) circuit design, and (3) statistical variation due to fabrication. It has been observed that, under certain conditions, hot carrier degradation during AC operation may be increased over DC biasing degradation [32-34]. Such AC degradation increases with increasing clock frequency and can occur in transfer gates in static RAM cells [34]. Although some of the enhancement may be due to experimental setup [35], the possibility of enhanced degradation was not conclusively eliminated. In fact, in a CMOS static RAM, the access transistor degradation was found to be the limiting hot carrier concern for the IC [17]. These access transistors were found to emit more light than surrounding transistors.

Certain areas of a circuit may be more susceptible to hot carrier stress than others. The transfer gate mentioned above is one example. It is also possible that certain transistors may be weaker due to statistical fabrication variations within the transistors [36]. These transistors may see the same bias stress as other transistors but degrade more (and emit more photons) due to normal processing variations in such physical parameters as gate oxide thickness and effective channel length.

Two photoemission situations are shown in Fig. 18 (a,b), illustrating how high channel current can exist but light emission may or may not be observable. The "worst case" defect (but "best case" for light emission) in Fig. 18 (a,b) is a zero ohm bridge (R_{DEF} = 0 ohms) between the gate output and V_{DD}. In Fig. 18 (a) the terminal bias voltages for T_N are $V_{GS} = V_{DS} = 5$ V, therefore T_N is in weak saturation. Light will be observed in the drain/channel region of T_N although it is not the optimal emission condition. Light would probably not be observed in T_P if the defect was a zero ohm connection to the ground bus. T_P would be in weak saturation, but

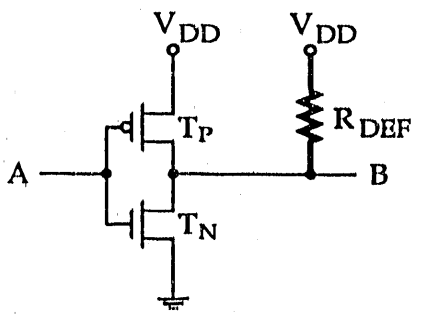

Fig. 18 (a). Bridge defect on an inverter output.

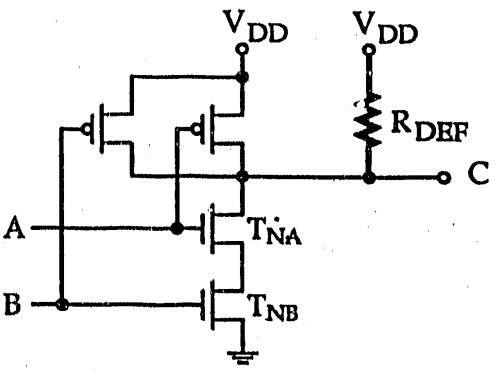

Fig. 18 (b). Bridge defect on a 2-NAND output.

its greatly reduced light emission would probably not produce observable photons.

Fig. 18 (b) shows a V_{DD}-bridged defect on the output of a 2-NAND gate. When $V_A = V_B = 5$ V, a relatively large drain current exists in T_{NA} and T_{NB}. In IC Case 4, this current was about 4 mA for a metallization short to V_{DD} (R_{DEF} = 0 ohms). For this case, $V_C = 5$ V, $V_{DS} = 4$ V for T_{NA} and $V_{DS} = 1$ V for T_{NB}, which resulted in light emission for T_{NA} (saturation bias) and no light emission for T_{NB} (nonsaturation bias).

When R_{DEF} is not 0 ohms, then the V_{DS} values across the affected transistors will depend upon the value of R_{DEF}. In Fig. 18 (a), V_{DS} on T_N will drop as R_{DEF} increases. When $V_{GS} > V_{DS} + V_T$ occurs, T_N goes into the nonsaturated state and channel light emission ceases.

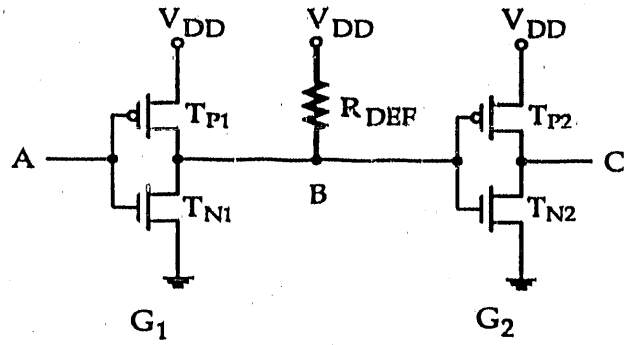

Fig. 19. Bridge defect in an inverter pair.

Therefore, the existence of light emission in a transistor driving a resistive defect load (RDEF > 0) is determined by individual defect resistance values.

Defects that are bridged to power supply voltages can also affect downstream (or driven) logic gates. Fig. 19 shows an inverter pair in which a resistive defect is connected between node B and the V_{DD} supply. If $V_A = 5$ V, then V_B may not be pulled down all the way to ground voltage. If V_B is pulled down to $1\text{ V} < V_B < 4\text{V}$ (for $V_T = 1$ V), then both transistors of G_2 are on and elevated drain current exists in T_{N2} and T_{P2}. The best case for G_2 light emission occurs near $V_B = 0.5\ V_C$, which depends upon the value of R_{DEF}. If R_{DEF} is large (>10 Kohms for typical technologies), then T_{N1} will pull down into non-saturation producing a weak logic zero on node B. This would decrease the likelihood of photodetection. This illustrates that photodetection in G_2 may or may not occur depending upon the value of R_{DEF}.

The conclusion for photodetection in driving load transistors is that the bias state and terminal voltage magnitudes are clearly the dominant factors that determine photon emission and not the magnitude of the drain current (or I_{DD} for the IC).

Another powerful detection capability of photoemission microscopy was illustrated in two of the IC failure analysis cases presented here. A defect may cause weak intensity photon emission that is undetectable in a single short cycle of a test vector set. However, continuous cycling of the IC through its complete (or appropriate subset) vector pattern can often expose the defect or failure mechanism if the photoemission microscope is used in an integration mode. This was illustrated in Case 2. Failure analysis in Case 3 uses the same principle, but used repeated power-up cycles. In both of these cases, the defects were detected without knowledge of the relationship between defect characteristics and the specific logic states required for photoemission detection. The success of the photoemission integration technique depends on the rate (duty factor) with which the photoemitting site is biased into its emitting state by the test vector pattern.

It has also been found at Sandia that photoemission microscopy, combined with I_{DDQ} testing [37,38], is a very useful technique for IC design characterization and validation. For example, photoemission from n-channel transistors in an internal memory array of a custom IC was used to determine that high I_{DDQ} after power-up was due to bit lines not initialized or latched properly. Photoemission has also been used in dynamic CMOS circuitry to determine which precharged bit lines in memory arrays discharge first.

V. CONCLUSIONS

This paper has presented data showing the strengths and weaknesses in using the photoemission microscopy technique for CMOS ICs. Photoemission microscopy is a powerful failure analysis tool often leading to rapid non-destructive identification of defects, particularly for gate oxide shorts, soft pn junctions, and certain situations in which non-light emitting defects can cause adjoining driver or load transistors to conduct and emit photons. In particular, the use of the integration mode of the instrument was shown to provide simple failure analysis of ICs that would have otherwise been difficult. Light emission from conducting transistors has been shown to be highly dependent upon the bias state of the driving and load transistors. In addition, light observation is highly dependent upon the opacity of overlying layers in an IC.

Future developments, such as quick spectral analysis of light emitting sources and application of gated photocathodes for stroboscopic acquisition, will enhance this already powerful technique.

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