(2)

SERI/PR-9080-1-T3

MIS SOLAR CELLS ON THIN POLYCRYSTALLINE SILICON

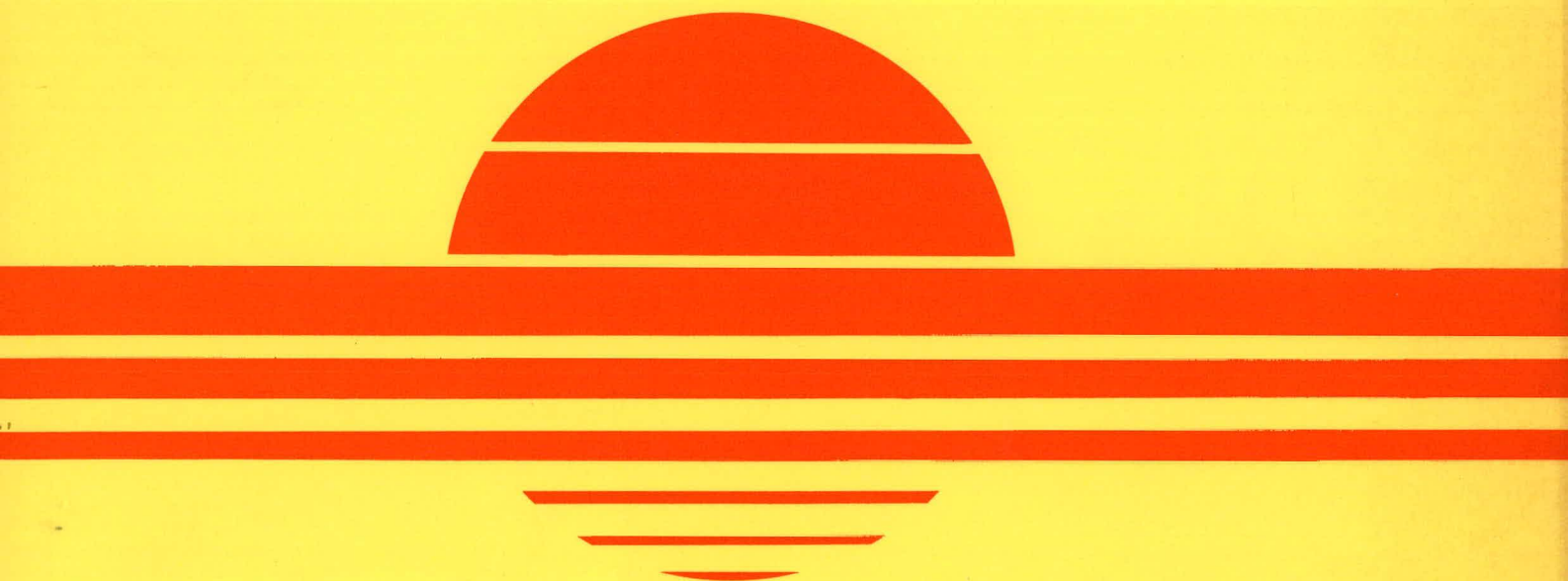
Progress Report No. 3 for Period September 1—November 30, 1980

By
Wayne A. Anderson

December 1980

Work Performed Under Contract No. AC02-77CH00178

State University of New York at Buffalo
Electrical Engineering Department
Amherst, New York



U.S. Department of Energy

Solar Energy

DISCLAIMER

DISCLAIMER

SERI/PR-9080-1-T3
Distribution Category UC-63

MIS SOLAR CELLS ON THIN POLYCRYSTALLINE SILICON

Progress Report No. 3
September 1, 1980-November 30, 1980

Wayne A. Anderson

December 1980

The State University of New York at Buffalo
Electrical Engineering Department
4232 Ridge Lea Road
Amherst, New York 14226

Prepared for the

Solar Energy Research Institute
Photovoltaic Programs Office
1617 Cole Boulevard
Golden, Colorado 80401
Solar Energy
Under Sub-Contract XM-0-9080-1

OBJECTIVES

Task 1 of this project involves electron-beam deposition of thin silicon films on low cost substrates. The goal is to obtain 20 μm thick films having 20 μm diameter crystallites which may be recrystallized to > 40 μm. Material characterization and device studies are to be included in efforts to reach a 6% conversion efficiency by March 1981.

The second task deals with MIS solar cell fabrication on various types of silicon including poly-Si, ribbon-Si, silicon on ceramic, and thin film silicon. Conduction mechanism studies, optimum engineering design, and modification of the fabrication process are to be used to achieve 13% efficiency on Xtal-Si and 11% efficiency on poly-Si.

Task 3 involves more detailed test procedures and includes spectral response, interface and grain boundary effects, computer analysis, materials studies, and grain boundary passivation. Stability and degradation studies will be performed as part of Task 4.

TABLE OF CONTENTS

LIST OF FIGURES

LIST OF TABLES

1. SUMMARY

Thin (10-30 μm) Si films are deposited on Si substrates by electron beam deposition. The substrates are held at 500-600° C during deposition in a vacuum of about 5×10^{-5} Torr and a rate of about 1 μm/min. Depositions on (100), (111) and Wacker poly-Si show the film to replicate the substrate when it comes to surface features and X-ray diffraction data. The new Ti pump chamber gives a factor of 10 improvement in vacuum. A new crucible design was introduced to eliminate certain impurities from the Si film. The results of this step are yet to be seen.

Electrical characterization of the e-beam Si films is being done by spreading resistance measurement and evaluation of MIS diodes. Ln (I)-V data give a linear plot but a high n-factor. $\frac{1}{C^2}$-V data give two straight line sections which must be evaluated. Photovoltaic response shows J_{scmax} = 1.5 $\frac{mA}{cm^2}$ and V_{ocmax} = 125 mV. This low photovoltaic response may be caused by 1) impurities, 2) a dead layer between substrate and film, or 3) high defect density in the film. These possibilities are being investigated. We are also evaluating all previous work on grain boundary models to aid in deriving a model which fits our experimental data.

MIS cell fabrication has involved the use of a new mask which gives 4 cm^2 cells with 7% grid shading. Cells have been made on Wacker poly-Si and Monsanto Xtal-Si, both of which were polished in our laboratory. An effort is being made to improve etching and polishing techniques.

MIS analysis centers on I-V-T, G-V-f and C-V-f studies of grain boundaries. G-V-T data do not give consistant trends for evaluating grain boundaries. C-V-f and G-V-f show some significant grain boundary effects in a frequency range from 5 Hz - 50 Hz. This indicates that grain boundary interface states predominate from d.c. to about 100 Hz. A quantitative evaluation will be given in the next report.

Reliability studies continue on Cr-MIS cells under shelf-life, light bias and out-of-doors conditions. Good stability is shown for the first two situations. A rapid degradation in the grid contact is shown in the out-of-doors study. A new grid design is being evaluated to remedy the situation. An evaluation of the quality of the D.I. H_2O used in wafer cleaning is being conducted to 1) improve on V_{oc} and 2) to eliminate the trend towards reduced V_{oc} with time.

2. INTRODUCTION

This project is undertaken to develop a low-cost, thin-film, MIS solar cell which will eventually sell for < 50¢/watt. This MIS process is being optimized for single crystal silicon and poly-Si prior to application to thin-film Si. This involves fabrication, grain boundary effects, and reliability studies. Thin Si films are e-beam deposited on Si, stainless steel, Ti, and glass substrates to evaluate the potential for future use as a low-cost semiconductor. It is our intent to combine the optimized MIS process with the thin e-beam Si film to produce a low-cost vacuum process to fabricate solar cells.

Our studies during this reporting period involve most of these areas of interest. The e-beam Si deposition work has concentrated on the use of different Si substrates, SEM analysis, X-ray diffraction, and some electrical characterization. Some samples have been sent out for SIMS analysis and an evaluation of defect density as well as crystallinity. An evaluation of all previous studies on grain boundary mechanisms is being made to aid in comparing theoretical and experimental data concerning conduction mechanisms. A new grid design is now in use which gives about 7% shading. We now can make cells with several areas including 2 cm^2 and 4 cm^2 on a single wafer. I-V-T analysis have been conducted to evaluate grain boundary conduction mechanisms. C-V-f and G-V-f data are also used to evaluate grain boundary effects. Reliability studies continue with the main emphasis on preparing new cells for study.

3. THIN FILM SILICON DEPOSITION AND ANALYSIS

3-1. Thin Film Silicon Deposition and Surface Analysis (M. Jackson)

Electron beam deposition of silicon onto a variety of substrates continued this quarter. The work on stainless steel substrates, reported in the last quarter, has been suspended in favor of using low resistivity, crystalline silicon substrates. The strategy is to optimize the deposition parameters so that a crystalline silicon film is obtained on these substrates. Once this goal is achieved, less expensive substrates such as metallurgical grade silicon or metals may be utilized. Ultimately, a highly crystalline silicon film or an inexpensive substrate is desired for use in low cost solar cells.

A SIMS analysis was performed on a silicon film on silicon substrate sample. The results are listed in Table 1. Carbon and copper were the major impurities with concentrations in excess of one part per hundred. These results led to the following changes in the e-beam deposition unit.

Table 1
SIMS ANALYSIS OF E-BEAM
SILICON PRIOR TO RE-DESIGN OF THE SYSTEM

Element	SIMS Data	Impurity (ppm)
B	$1.1 \times 10^{17}/cm^3$	2.2
C	5.3×10^{20}	10,600
Fl	<	-
Na	5.2×10^{17}	10.4
Mg	2.2×10^{17}	4.4
Al	2.3×10^{17}	4.6
Cl	<	-
K	10^{16}	0.2
Ti	2.4×10^{15}	0.05
Cr	2.1×10^{17}	4.2
Fe	3.4×10^{17}	6.8
Ni	3.9×10^{17}	7.8
Y	2×10^{15}	0.04
Zr	1.9×10^{17}	3.8
Cu	5.1×10^{20}	10,200

A new copper crucible was designed with an inch and a quarter diameter. The old crucible had a diameter of seven-eights of an inch. It is felt that the e-beam had contacted the sides of the old crucible and this led to copper contamination of the silicon source. Backstreaming of oil vapor from the mechanical pump was considered to be the source of the carbon. A coaxial trap was placed in the foreline to eliminate any oil vapors. In an effort to remove the other impurities, the screws used to hold the substrates to the substrate heater where replaced with #304 stainless steel screws. Two quartz heater lamps, used for baking out the chamber, were removed. An exterior heating system is being considered.

A titanium sublimation pump was added to the system. A drop in the base pressure of the system from 5×10^{-6} Torr to 8×10^{-7} Torr was observed. Deposition now takes place at a pressure of 5×10^{-6} Torr as opposed to 1×10^{-5} Torr prior to adding the Ti-sublimation pump. Next quarters report should contain a SIMS analysis of a sample made after the above changes were implemented.

This quarter's runs are summarized in Table 2. The majority of the samples prepared were silicon films on (111) silicon substrates. The substrates were unpolished or polished. The surface features and crystallinity of these films were discussed in last quaters's report. Suffice it to say, that the films duplicated the surface structure of the substrate and oriented themselves in the (111) direction. Repeated success using the (111) substrates led to the use of polished (100) single crystal and Wacker polycrystalline silicon substrates. Figure 1 shows SEM micrographs of the films obtained on (100) silicon and the Wacker poly. Once again, the replication of the substrate surface is obvious. Figures 2 and 3 show X-ray analysis of the two films. Again the film structure contains crystals having the same preferred orientation as the substrate. No grain boundaries are evident under the SEM, but more work needs to be done to determine the actual size of the film's crystallites. One should be aware that the X-ray analysis for the Wacker poly silicon film is highly position dependent. The peaks on the X-ray analysis will change (grow or shrink) in response to position changes of the sample in the X-ray beam.

In conclusion, the e-beam deposited thin films take on the surface features of the underlying substrate. The crystal orientation of the film appears to be the same as that of the underlying substrate. The size of the crystallites in the film has yet to be determined, but the SEM micrographs do not show any

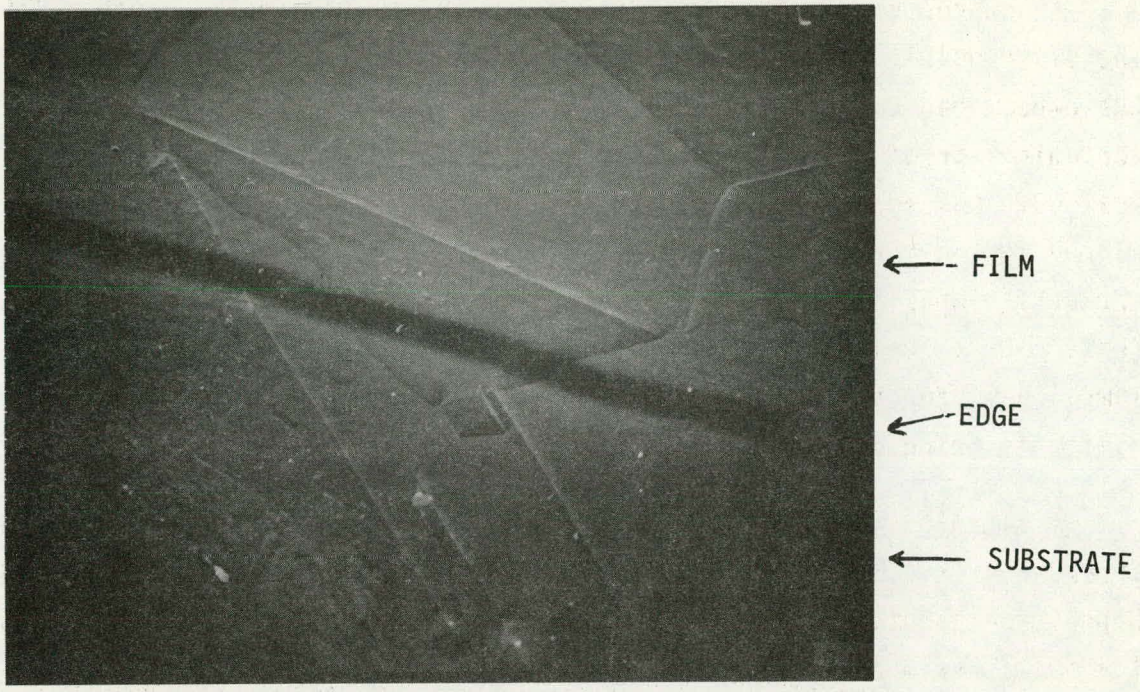


Figure 1A SEM micrograph (100X) showing an e-beam Si film on a Wacker Si substrate. Replication of the substrate is obvious

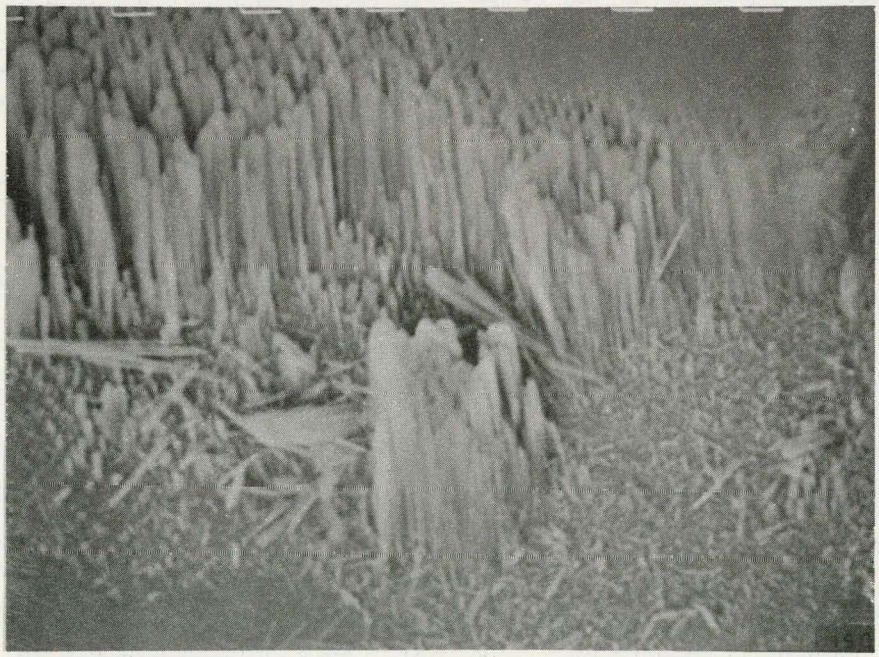


Figure 1B SEM micrograph (1500X) showing whisker-like columnar growth at the edge of a Si substrate

Figure 2 X-ray data for an e-beam Si film on a (100) Si substrate

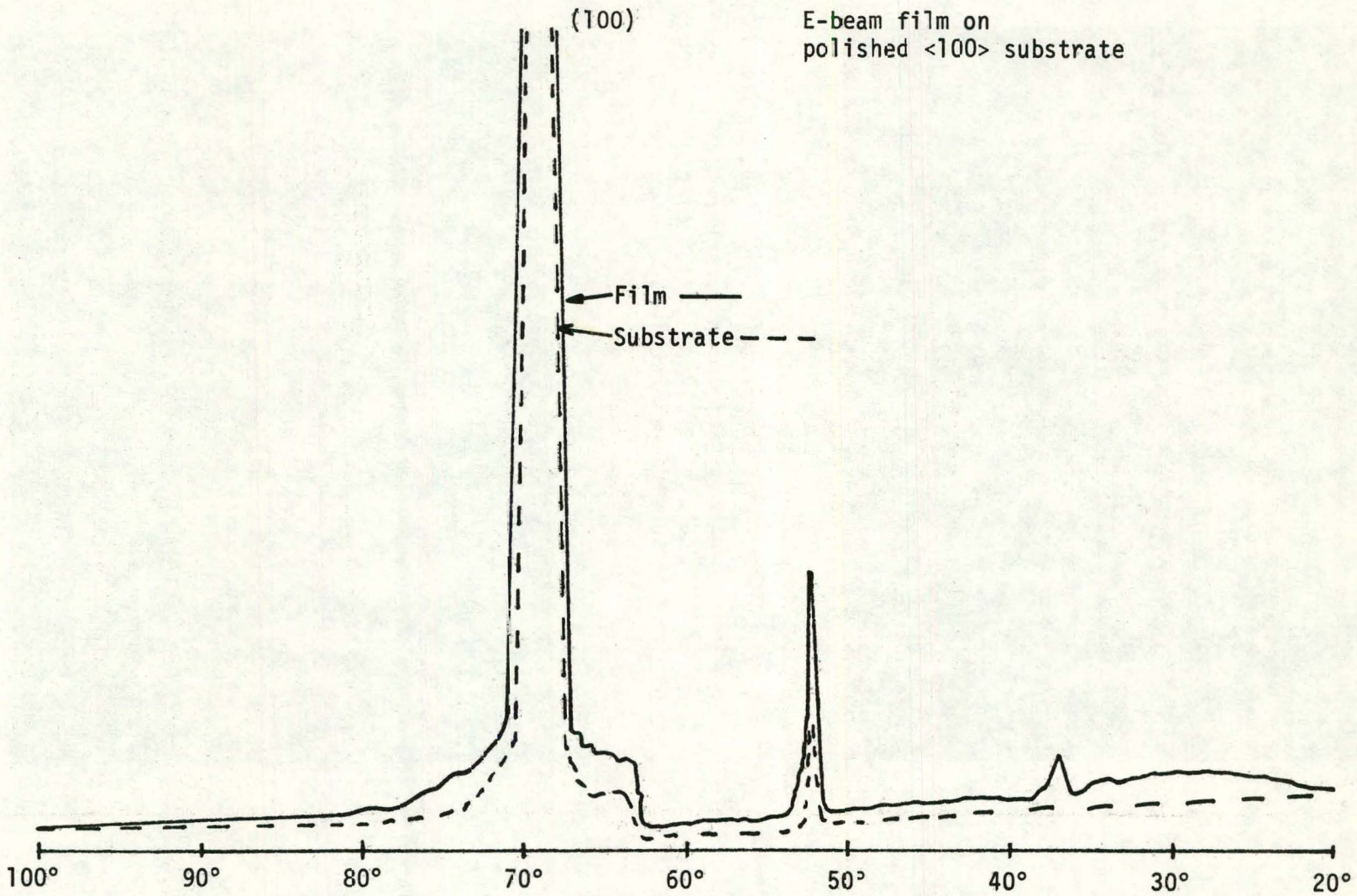
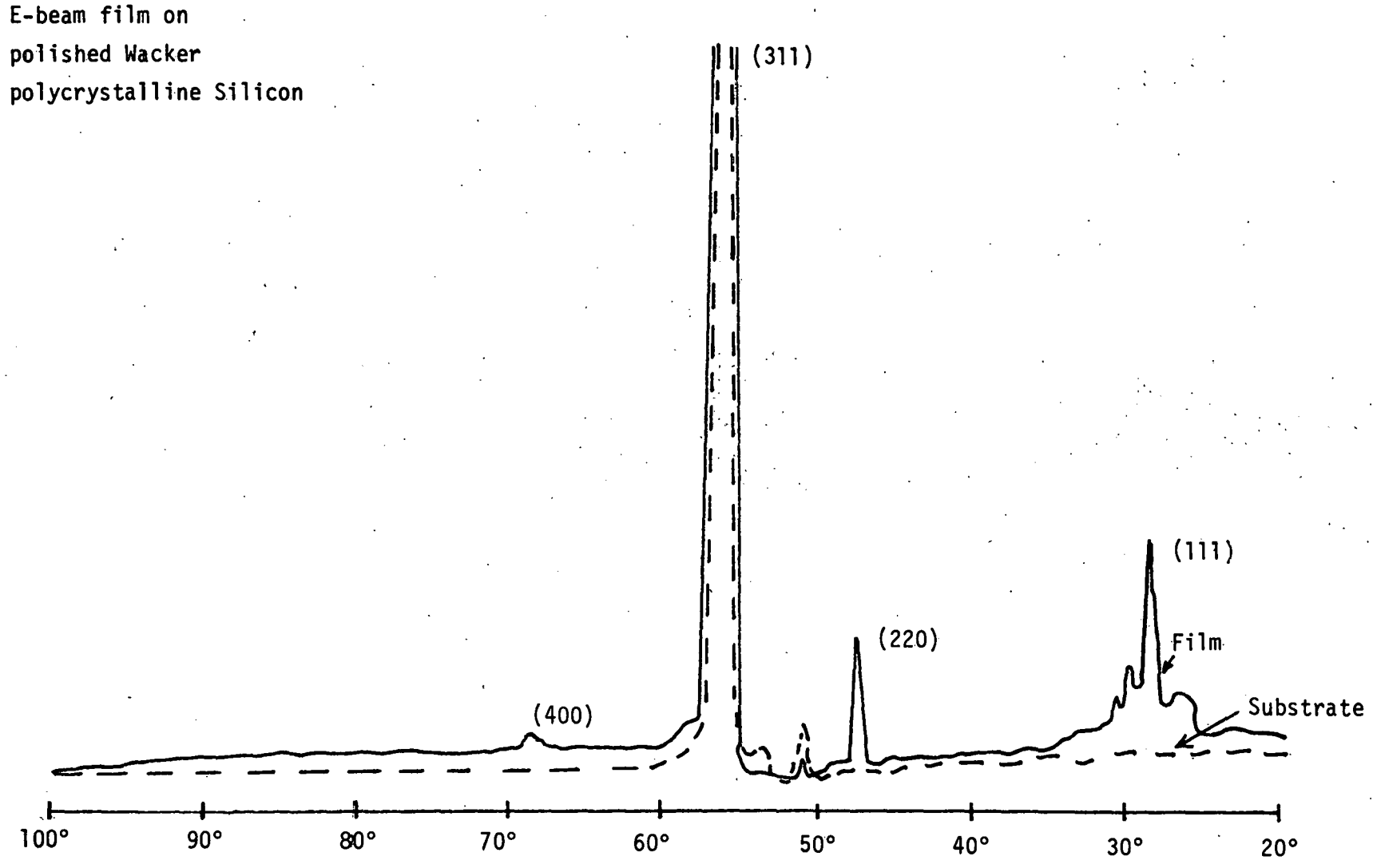


Figure 3 X-ray data for an e-beam Si film
on a Wacker Si substrate



cracks or grain boundaries. Next quarters work should shed some light on this question.

Table 2

SUMMARY OF E-BEAM DEPOSITIONS

Date	Vacuum (Torr)	Substrate Temperature (° C)	Film Thickness (μm)	Average* Deposition Rate (μm/min)
9/30/80	$8x10^{-6}$	545	7	0.25
10/10/80	$8x10^{-6}$	550	12	0.55
11/6/80	$7x10^{-6}$	550	17	0.85
11/13/80	$5x10^{-6}$	525	7	0.47
11/25/80	$5x10^{-6}$	500	25	1.25

* Average Rate is film thickness divided by total deposition time. Initial deposition rates are usually very low, hence rates above 1 μm/min have been regularly observed.

3-2 Thin Film Silicon Electrical Studies (F. Kai)

Electron-beam deposited polycrystalline silicon MIS diodes have been tested by "Current-Voltage" (I-V) and "Capacitance-Voltage" (C-V) measurements. The I-V measurements are studied to determine the "barrier height" ϕ_B, and the ideality factor, "n" value. From an I-V test we can also study the "series resistance" and "shunt resistance" effects. In this study three classes of I-V curves have been plotted: (1) under dark forward bias, (2) under light forward bias, (3) under dark reverse bias. For the single crystal-silicon Schottky-barrier or thin-oxide MIS diodes, a plot of C^{-2} versus V can determine the doping, N_A, of the device. If N_A is constant throughout the depletion region, the curve should be a straight line. A study of the doping profile in thin film silicon and substrate is made possible by the "C^{-2} versus V" plot.

The I-V characteristic of the electron-beam deposited thin-film silicon on p-type silicon is plotted in Figure 4. The ideality factor is 4.24. The barrier height is calculated from the plot to be 0.683 eV. The dark log J-V characteristics do not show serious series resistance effects. The light J-V characteristics also do not show series resistance effects. The dark current at zero-bias is extrapolated to be 10^{-2} mA/cm^2 which is a very high value. The dark reverse-biased plot shows a large reverse current. This may be due to a high trap density distribution.

The C-V plot for this sample is shown in Figure 5. There are three regions shown in the curve:

(i) small forward-biased region
(ii) small reverse-biased region
(iii) large reverse-biased region.

The results indicate that there are different doping (impurity and trap) concentrations throughout the sample. It has previously been pointed out herein from X-ray analysis, that the thin film silicon deposited by e-beam grows in the same orientation as the silicon substrate. The doping concentrations in the film and the substrate are different. The substrate-film interface may result in a layer of deep traps.

The curve shape for the forward bias applied in (i) is close to the approximation of a Schottky barrier with uniform negative charge density equal to the acceptor density N_A. The small reverse bias applied in (ii)

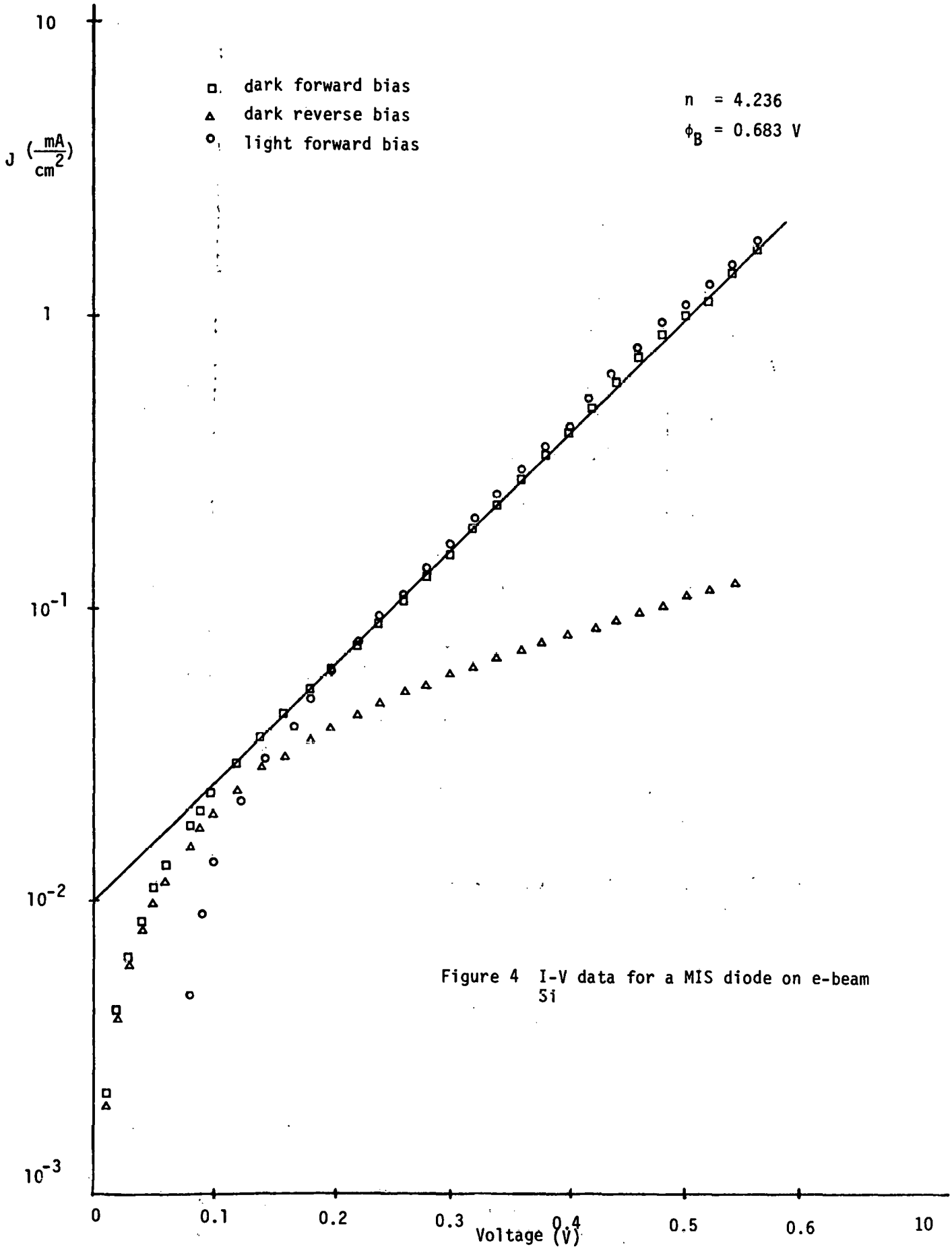


Figure 4 I-V data for a MIS diode on e-beam Si

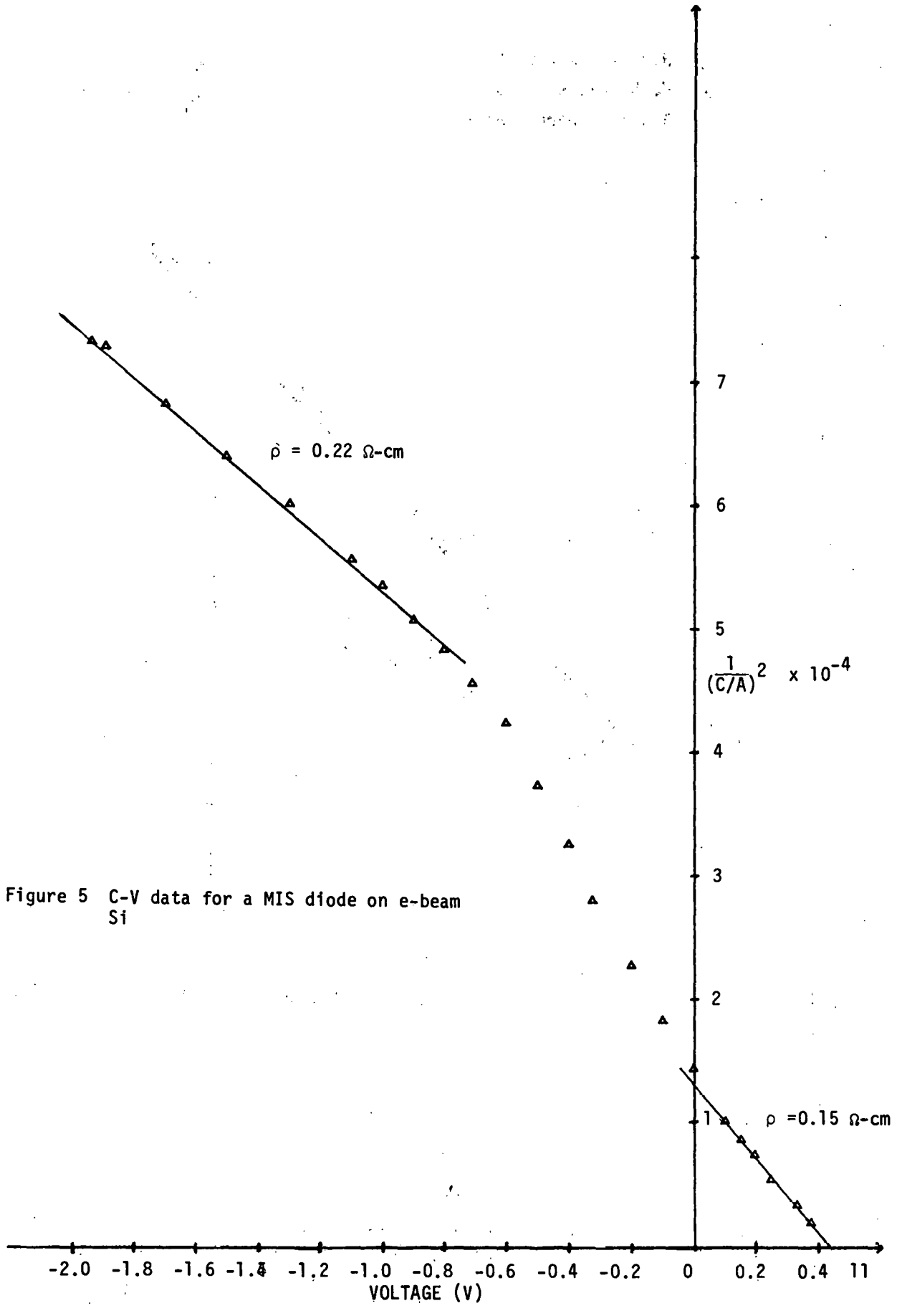


Figure 5 C-V data for a MIS diode on e-beam Si

shows a steeper slope. The actual mechanism of this region is not clear now. It may represent a "transition region."

The large negative bias is applied in (iii) with a smaller slope in the absolute value sense. The space-charge region contains both the acceptors and the empty hole traps which are enhanced by the large reverse bias. The film-substrate interface forms a p-p^+ junction. The total capacitance C measured is composed by three capacitance:

$$\frac{1}{C} = \frac{1}{C_i} + \frac{1}{C_{sc_1}} + \frac{1}{C_{sc_2}}$$

where

C_i = insulator layer capacitance

C_{sc_1} = space-charge capacitance due to oxide-film interface

C_{sc_2} = space-charge capacitance due to film-substrate interface.

The energy band diagram is shown below in Figure 6.

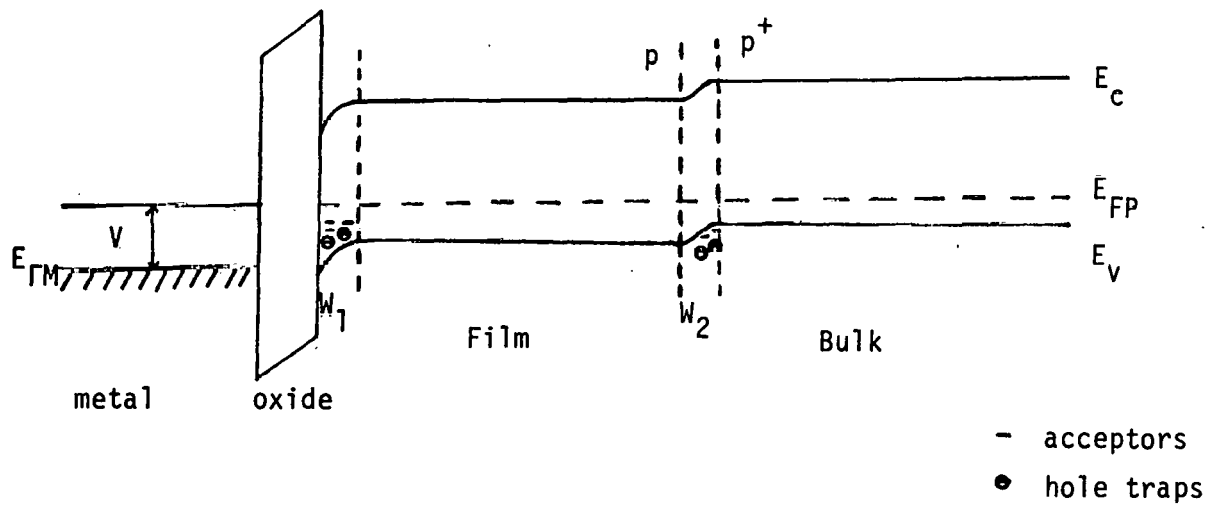


Figure 6 Band diagram which may explain C-V data for a MIS device using an e-beam Si on Si substrate

The I-V and C-V measurements of the e-beam deposited polycrystalline thin-film diode can be used as a tool to analyze the doping and trap density distributions throughout the sample and the current-conduction mechanisms as well. The I-V plot obeys an exponential law. This can be studied further to understand the "space-charge limited current" contribution to the device. From C-V measurement, the effect of "deep traps" and the film-substrate interface trap densities can be analysed. In the next report, more experimental work and theory will be developed. Appendix A contains a condensed analysis of some previous work on grain boundary effects in poly-silicon. The next report will finish this survey and outline new directions for a model which fits our experimental data on small grain poly-silicon.

4. Cr-MIS SOLAR CELL FABRICATION

4-1 Device Processing Techniques (G. Rajeswaran)

The Cr-MIS solar cell is considered to be a structural design that would ultimately produce a > 10% efficient device on thin film polycrystalline silicon. We have previously reported[1] a revised processing scheme to increase efficiency and reproducibility in Cr-MIS cells. Such a processing technique was shown to be applicable to various types of potentially low cost silicon substrates.[2] In this report, we discuss these device processing techniques and the modifications that were introduced to make reproducible cells.

The Cr-MIS cell is normally fabricated using the structure 710 Å SiO A/R coating/Al grid/60 Å Cu conductive layer/30 Å Cr/20 Å SiO_x/p-type silicon/Al ohmic contact. The top metallic layers and the A/R coating are deposited in a one pump-down process after the silicon surface is cleaned and oxidized. It is imperative that the silicon surface be extremely clean before oxidation. All our processing variations were introduced at this stage of fabrication.

a) Planar Etch (P.E.)

MIS devices are surface oriented devices. The nature and quality of these surfaces play an important role in shaping the characteristics of these devices. The rougher the surface, the higher is the density of surface states and poorer the quality of the device. A planar etch that would react with all crystal orientations at the same rate is necessary to conform with a single processing technique that deals with all types of silicon substrates. A mixture of 75% HNO_3, 17% CH_3COOH and 8% HF serves this prupose.[3] A treatment of this planar etch on any type of silicon substrate for approximately one hour produces an uniform, polished surface.[2] The volume ratio of the constituents acutely governs the accuracy of the planar etch. A very small variation from a 75:17:8 ratio results in a preferential rate of etch on different crystal orientations, causing etch pits. As an initial step in the fabrication sequence, all unpolished silicon substrates were treated with the planar etch solution for an hour. This step was omitted on mechanically polished silicon wafers obtained from the manufacturer. Agitation of the planar etch solution produced uneven

surfaces, whereas, a free standing planar etch solution resulted in a high degree of polish on one side of the wafer and striations on the other.

The metal-insulator-semiconductor (MIS) junctions were formed on the smooth, glossy side of the silicon wafers and the aluminum (Al) back contacts made on the striated, coarser side.

b) One Cleaning, One Oxide Process (OO)

In the OO process, the silicon wafers are degreased and treated with deionized (DI) water. The thin native oxide is stripped by immersion in hydrofluoric acid (HF), washed in DI water, blown dry in a stream of dry Nitrogen (N_2) and immediately placed in a vacuum system and pumped down. The back aluminum contact is then evaporated on the coarser side of the wafers. A near-perfect ohmic contact is made by sintering the samples in a muffle furnace at 600° C in air. This produces a thin oxide ($\sim$ 20-25 Å) on the front surface at the same time. On cooling, the samples are remounted in the vacuum system and the top metallic layers and the anti-reflection coating are evaporated consecutively in a one pump-down process at a pressure of 1×10^{-5} Torr.

This process was frequently used in our earlier investigations. The results were never consistent and the photovoltaic data scattered. The contamination of the front surface, when removed from high vacuum, for the purpose of back contact sintering, was a prime suspect for this random device behaviour. The one cleaning, one oxide process was abandoned and a double cleaning, double oxide process was introduced.

c) Double Cleaning, Double Oxide Process (DD)

The back contact is sintered at 600° C and a thin oxide grown on the front surface simultaneously using the one cleaning, one oxide process. To counter the contention that the front surface is contaminated prior to ohmic contact formation, this surface has to be cleaned again in HF without destroying the aluminum on the back. By spreading a layer of photoresist on the Al and by curing it, the back contact can be protected from further cleaning steps. The front surface is then cleaned in a DI, HF, DI cycle without exposure to air. Next, the photoresist is removed with acetone, and the wafer washed thoroughly in a DI water stream, blown dry

in dry nitrogen and the thin oxide regrown in the muffle furnace at 580° C. In cooling, the wafer is remounted in a vacuum system, pumped down and the top layers evaporated.

The DD process of fabrication resulted in consistent photovoltaic data on similar substrates and even an increased efficiency.[1]

d) Double Cleaning, One Oxide Process (DO)

The back aluminum contact is sintered twice in the DD process. The double cleaning, one oxide process eliminates the first sintering while otherwise maintaining the same fabrication sequence as the DD process.

The advantage of the DO process over the other two is that the elegance of the DD process is preserved while eliminating a fabrication step at the same time.

4-2 Summary of Photovoltaic Data (G. Rajeswaran)

A summary of solar cell photovoltaic data from a study conducted on substrates of varying resistivites is given in Table 3. For comparison, the data from a Wacker-Chemitronic polycrystalline silicon solar cell is also shown.

The lower the resistivity of the substrate, the lower the lifetime of the minority carriers and hence a smaller short circuit current (J_{sc}) results. The series resistance (R_s) is lower on the other hand and contributes to a higher fill factor. With increasing resistivity, J_{sc} increases and the fill factor drops. The anomalous case of smaller J_{sc} on the cell made on 8-15 Ω-cm substrate is due to a bad anti-reflection coating and a diffused grid pattern which reduces the active area of solar insolation. We have seen in our previous investigations that a resistivity of between 1 Ω-cm and 5 Ω-cm results in an optimum efficiency solar cell. The substrates of the class (1-4 Ω-cm) consistently exhibited higher efficiencies than the other resistivities. Nevertheless, it was observed that these so called higher efficiencies are always $\leq$ 10%, which led us to the conlusion that the quality of the silicon substrates was questionable.

Spectral response studies on the cells of Table 3 and on some other cells are shown in Table 4. At long wavelengths, the ratio of spectral responses approximately correspond to ratios of diffusion lengths.[2,4]

Table 3

SUMMARY OF SOLAR CELL PHOTOVOLTAIC DATA

SUBSTRATE	RESISTIVITY Ω-cm	V_{oc} V	J_{sc} ** mA/cm^2	FF	EFFICIENCY η% ACTIVE AREA	EFFICIENCY η% TOTAL AREA	PROCESSING
MONSANTO <100>	0.05-0.15	0.58	17.0	0.75	7.4	6.1	P.E., DD Process (600° C)*
MONSANTO <100>	1-4	0.57	23.0	0.71	9.2	7.7	P.E., DD Process (600° C)*
MONSANTO <100>	8-15	0.53	19.0	0.67	6.8	5.6	P.E., DD Process (600° C)*
WACKER POLY	1-10	0.53	21.0	0.72	8.0	6.6	P.E., DD Process (600° C)*
WACKER POLY	1-10	0.52	25.5	0.63	8.2	6.9	P.E., DD Process (590° C)*

* Temperature at which oxide is grown

** Based on NASA-Lewis calibration and using ELH lamp @ 100 mW/cm^2

Active area = 2.0 cm^2

Total area = 2.42 cm^2

Table 4

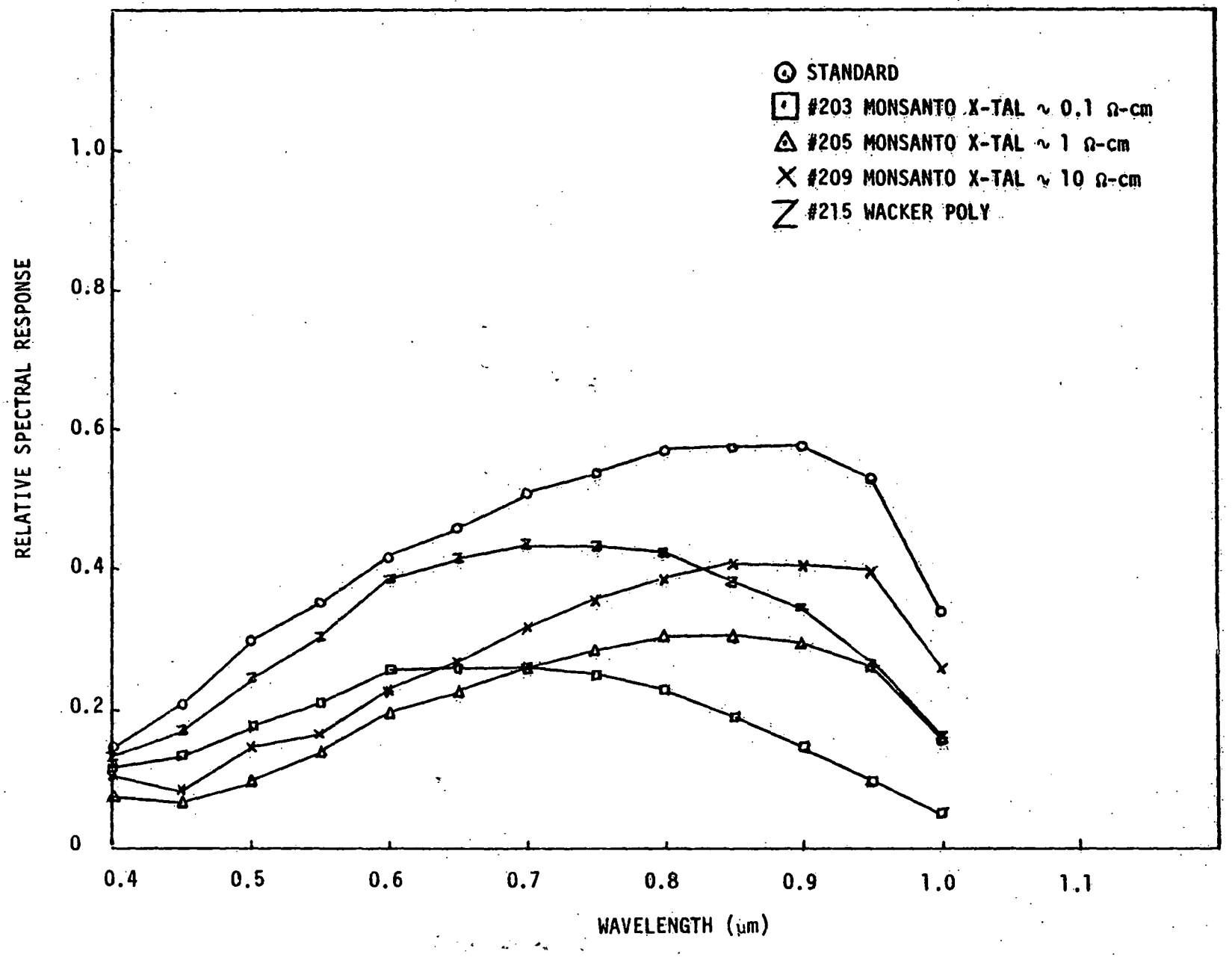
DIFFUSION LENGTH DATA

Substrate	Resistivity Ω-cm	Relative Response at 1.0 μm	Diffusion Length (μm)
STANDARD p-n	-	0.3382	184
MONSANTO <100>	0.05-0.15	0.0471	26
MONSANTO <100>	1-4	0.1568	85
MONSANTO <100>	8-15	0.2567	140
MONSANTO <100>	> 5	0.2164	118
WACKER POLY	1-10	0.1582	86

Using this fact, and a calibrated silicon solar cell, it is found that the diffusion length of single crystal silicon of optimum resistivities (1-4 Ω-cm) is 85 μm. This is of the same order as Wacker polycrystalline silicon. This is indicative of the bad quality of Xtal silicon used in our recent fabrication studies. Figure 7 shows the spectral response curves as a function of substrate resistivities. As anticipated, the diffusion length of minority carriers increases from low to high resisitivity substrates.

Series resistance is an important parameter in solar cell design and fabrication. It is a power dissipating factor[5] and the maximum achievable output power of a solar cell is decreased. This effect can be seen in the "softening" of its current-voltage characteristic in the fourth quadrant. The series resistance in a Cr-MIS solar cell arises from the contribution of the top metal layers and the grid (R_G) and also the semiconductor base resistance (R_B). R_G, the contribution of the metallic layers and the grid metal, can be minimized by an optimum grid design. Smaller finger widths and increasing distances of separation between them will reduce the grid shading loss but the minority carriers will have to flow a longer distance

Figure 7 Spectral response of Cr-MIS cells as a function of substrate resistivity



to the current collecting fingers. Evidently, there is an optimum spacing for a maximum short circuit current and minimum front layer resistance.

A vacuum deposited 3000 Å layer of aluminum has a sheet resistance of 1.56 Ω/[]. 30 Å Cr/60 Å Cu layers have an average sheet resistance of 50 Ω/[]. A new grid was designed[6] with a grid finger width of 0.1 mm and the spacing between the fingers being 1.67 mm. There were two large area cells, the largest being 4 cm^2, and many small test diodes and cells with different solar (active) and dark areas. Figure 8 shows the Cr/Cu metal mask (actual size) with different area openings, the grid-contact mask for different areas and the antireflection coating mask. Table 5 summarizes the data on the diodes and cells of various areas.

The grid mask was fabricated on a thin molybdenum sheet by a photolithographic process following by chemical etching. Care was taken in the design to account for undercut and side etching at grid fingers. The Cr/Cu mask and the A/R mask were made on thin brass (2 mils).

Table 6 summarizes the preliminary data on solar cells fabricated with the new mask. A higher J_{sc} on all devices comparable to those in Table 3 indicates a lower shadow loss. The fill factor is consistently smaller on 4 cm^2 cells than on 2 cm^2 cells. The equation governing the operation of a solar cell as given by ($R_{sh} \to \infty$)

$$J = J_L - J_o \left[\exp\left\{\frac{q\left(V+I\cdot\frac{A_T}{A_s}\cdot R_s\right)}{nkT}\right\} - 1\right] \qquad 4\text{-}1$$

where

$$R_s, \text{ the series resistance} = R_G + R_B \qquad 4\text{-}2$$

R_G = 0.212 Ω for a 24 line structure, as in 4 cm^2 cell

R_B = 0.497 Ω for a 12 line structure, as in 2 cm^2 cell

and

R_G = resistance due to the grid and Cr/Cu layers

$$R_B = \text{semiconductor resistance} = \frac{\rho_B H}{A} \qquad 4\text{-}3$$

and H = thickness of the wafer, A = the area of the cell and ρ_B = resistivity of silicon.

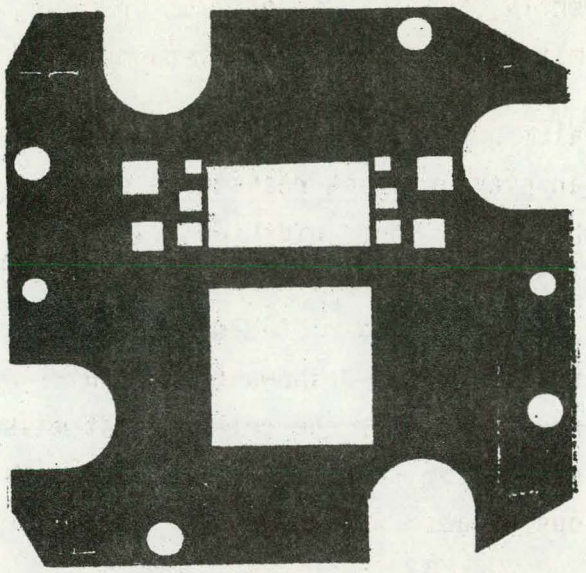


Figure 8a New Cu/Cr mask.

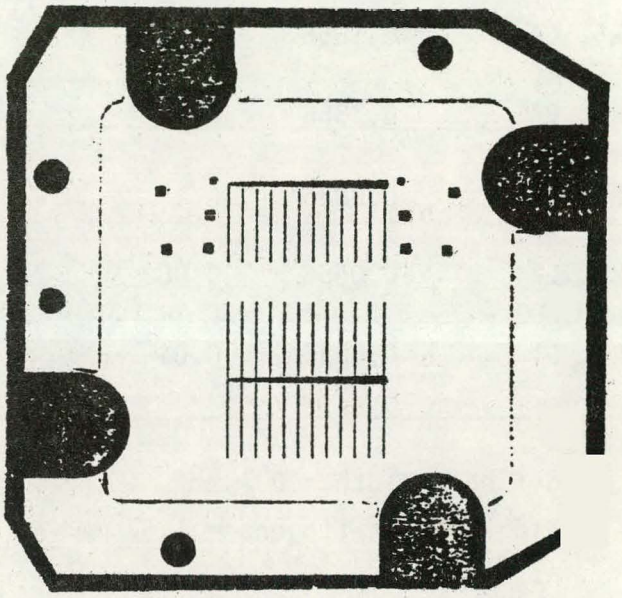


Figure 8b New grid mask.

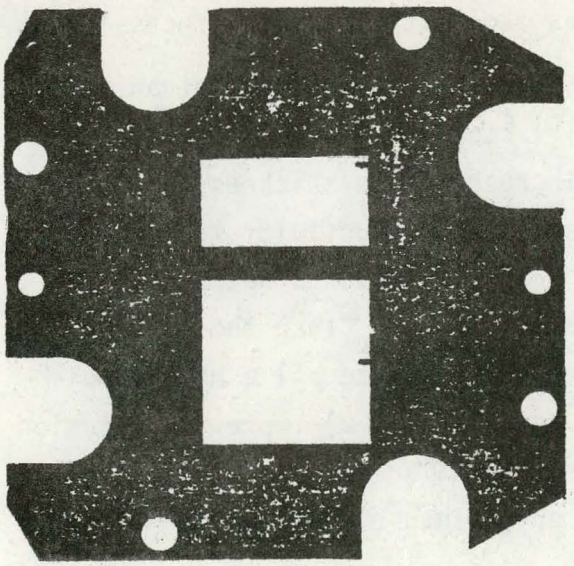


Figure 8c New A/R mask.

Table 5

NEW MASK DATA

CELL IDENTIFIER	AREA (cm^2) ACTIVE A_s	AREA (cm^2) TOTAL A_T	SHADING $\frac{A_T - A_s}{A_T} \times 100$ (%)	NO. OF FINGERS	GRID CONTRIBUTION TO SERIES RESISTANCE (Ω)
LARGEST	3.68	4.0	8.0	24	0.212
LARGE	2.0	2.12	5.65	12	0.49
R5, L5	0.1856	0.2	7.2	-	-
R4, L4	0.1356	0.15	9.6	-	-
R3, L3	0.0856	0.1	14.4	-	-
R2, L2	0.0656	0.08	18	-	-
R1, L1	0.0336	0.04	16	-	-

Grid finger width = 0.1 mm
Spacing between fingers = 1.67 mm

For solar cells of two different areas made with the same processing at the same time, the ($I \cdot \frac{A_T}{A_s} \cdot R_s$) drop is higher for larger cells than for smaller ones, resulting in a slightly smaller fill factor for large area cells. R_G of large area cells can be reduced by increasing the thickness of grid metal deposition or by replacing it with a higher conductivity metal grid. It is significant to comment on the (High Quality) Monsanto wafer shown in Table 6. This substrate gave a much better V_{oc} and J_{sc} than the others (V_{oc} = 0.59 V and J_{sc} = 26-27 mA/cm^2). These are due to 1) a highly polished surface which reduces surface state density and 2) improved diffusion length. Illuminated I-V data for cells on this wafer are shown in Figure 9. Thicker grid metal will increase fill factor in future samples.

Table 6

PHOTOVOLTAIC DATA ON LARGE-TO-SMALL AREA CELLS (NEW GRID)

SUBSTRATE	RESISTIVITY (Ω-cm)	AREA (cm^2) ACTIVE	AREA (cm^2) TOTAL	V_{oc} (V)	J_{sc} ** (mA/cm^2)	FF	EFFICIENCY η% ACTIVE	EFFICIENCY η% TOTAL	PROCESSING
MONSANTO <100>	0.05-0.15	3.68	4.0	0.51	21.7	0.68	7.5	6.8	P.E., DO Process (580° C)*
		2.0	2.12	0.50	20.5	0.70	7.2	6.8	
MONSANTO <100> (High Quality)	1.5-2	3.68	4.0	0.59	26.1	0.62	9.6	8.9	DO Process (600° C)*
		2.0	2.12	0.59	27.0	0.66	10.6	10.0	
		0.14	0.15	0.58	18.4	0.76	8.1***	7.3***	
MONSANTO <100>	> 5	3.68	4.0	0.54	24.5	0.60	7.9	7.2	DO Process (580° C)*
		2.0	2.12	0.54	26.0	0.61	8.5	8.1	
		0.14	0.15	0.53	19.2	0.51	5.2***	4.7***	

* Temperature at which oxide is grown

** Based on NASA-Lewis calibration and using ELH lamp @ 100 mW/cm^2

*** No anti-reflection coating

In future cells, a high efficiency will be achieved by

1) Better polishing techniques to give $V_{oc} \simeq 0.59$ V.

2) Better grid performance using a solder dip to give FF $\simeq$ 0.75.

3) Improved A/R coating to give $J_{sc} \simeq$ 30 mA/cm^2.

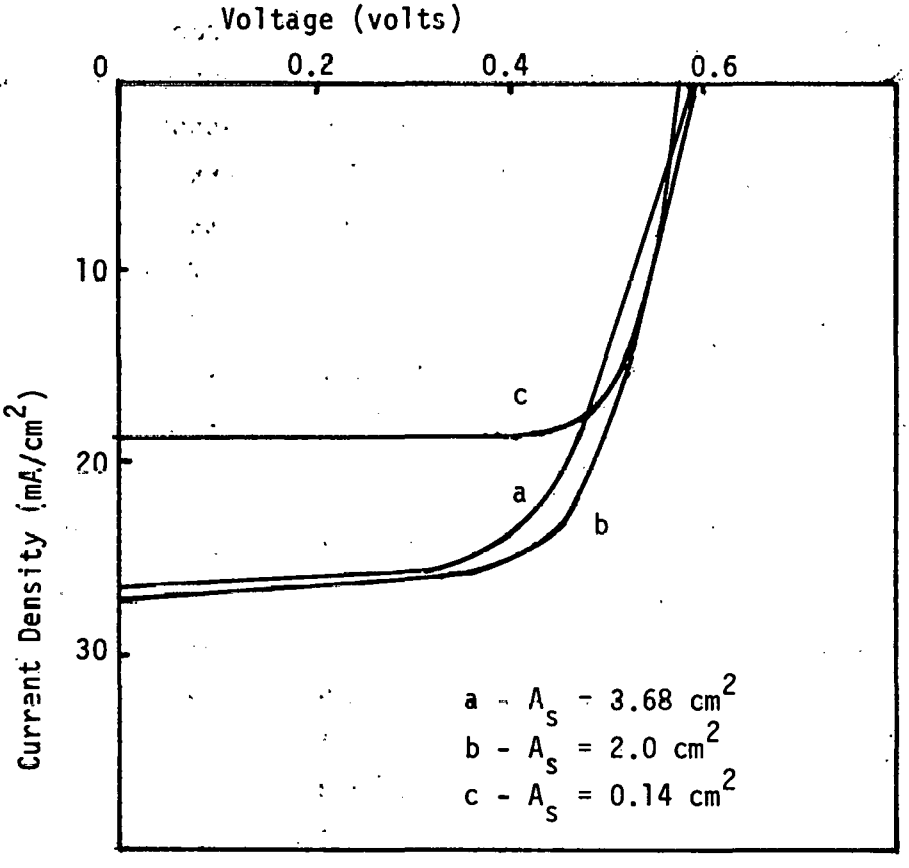


Figure 9 Photovoltaic I-V data comparing 4 cm^2, 2 cm^2 and small area cells

5. ANALYSIS OF MIS SOLAR CELLS

5-1 Grain Boundary Studies by C-V-F and G-V-f (V. J. Rao)

In the course of our investigations on polycrystalline Si MIS solar cells, we have undertaken the work on C-V, G-V, G/f - f measurements of polycrystalline MIS diodes in order to evaluate the grain boundary effects on interface states. To date, neither theoretical nor experimental data are available on C-V measurements of grain boundaries in polycrystalline silicon solar cells.

The determination of the density of states distribution in the grain boundaries of polycrystalline silicon is very useful in developing our understanding of the physical properties of the material and in particular of the role of grain boundaries. Capacitance-voltage and conductance-voltage measurements on Schottky diodes appear to be a promising technique for the determination of density of states. The purpose of this work is to explore the frequency dependence of both the conductance and capacitance of Schottky devices in order to deduce the depletion width and density of states in the region of the Fermi level and below. If the frequency dependence is measured and analysed with and without externally applied dc voltage, as is the case for most of the present work, very useful data could be obtained about the role of grain boundary effects.

The electrical properties of interface states are characterized by interface state density, the position in the energy gap of the silicon and the capture cross section. The most widely used tool for investigating these interface state properties is the MIS diode. Dispersion of the capacitance can be used to obtain information about the energy distribution and density of interface states.[8] The capacitance technique, however, has severe limiations. Essentially, the difficulty is that interface state capacitance must be extracted from measured capacitance which consists of oxide capacitance, depletion layer capacitance and interface state capacitance. This difficulty does not apply to the equivalent parallel conductance because conductance arises solely from the steady state loss due to the capture and emission of carriers by interface states and is thus a more direct measure of these properties. Conductance measurements yield more accurate and reliable results particularly when the density of interface states is low as in the thermally oxidized system. Both the capacitance and

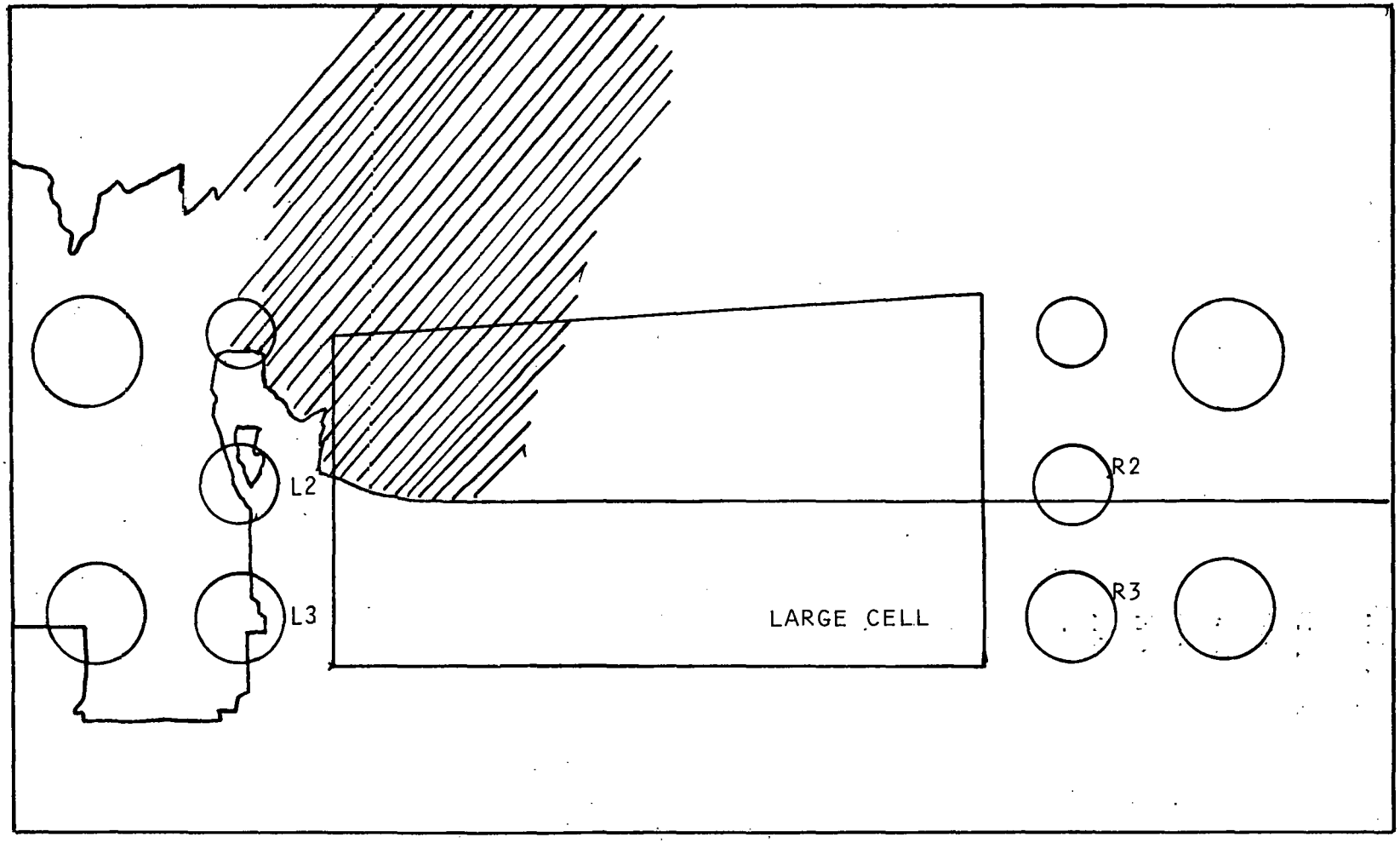
equivalent parallel conductance as functions of voltage and frequency contain identical information about interface states. Greater inaccuracies arise in extracting this information from the capacitance.

In order to evaluate MIS measurements with regard to interface states, it is desirable to have one dimensional current flow perpendicular to the interface. This condition may not apply when the silicon underneath the field plate and beyond is inverted. Then the capacitance and conductance are dominated by the lateral a.c. current-flow. Because of the positive polarity of surface charge, p-type silicon is normally inverted and is therefore most easily investigated in the inversion region.

A study of grain boundary effects is made using a wafer of Hamco polysilicon having very large grains. A comparison in data is made for a small diode having a single grain boundary and another small diode of the same area with no grain boundary. A sketch showing diodes and grain boundary location for this study is given in Figure 10. Measurements of capacitance C (f, V) and conductance G (f, V) as a function of frequency are made using the in phase and quadrature components from a PAR 5204 lock-in-amplifier. Modulation voltage remained at 25 mV peak to peak. An operational preamplifier to combine a.c. and d.c. components, facilitated measurements of C (f, V) and G (f, V) under bias. During the measurements, the sample remained at room temperature in air. The system set-up to measure capacitance and conductance was previously given[7] (Figure 11). Standard glass capacitors are used to calibrate the lock-in-amplifier.

Figures 12 and 13 show the C(f, V) curves for diodes on the grain (R_3) and grain boundary (L_3) at various frequencies (20 H_z <f< 5000 H_z). A description of the main features of the curves will be presented. Significant changes in C-V and G-V data are noted when comparing diodes with and without grain boundaries. One significant feature is the nature of the capacitance-voltage characteristics in the voltage range where the semiconductor surface is inverted. The specific features which deserve reference are 1) the 20 H_z and 50 H_z curves in case of a diode on the grain exhibit an increase in the capacitance when the top contact is reverse biased while the diode on the grain boundary shows a decrease in capacitance and becomes saturated. It appears in case of R_3 that the signal frequency is low enough so that the minority carriers within the inversion region become mobile and

Figure 10 GRAIN BOUNDARY LOCATION FOR I-V-T STUDY



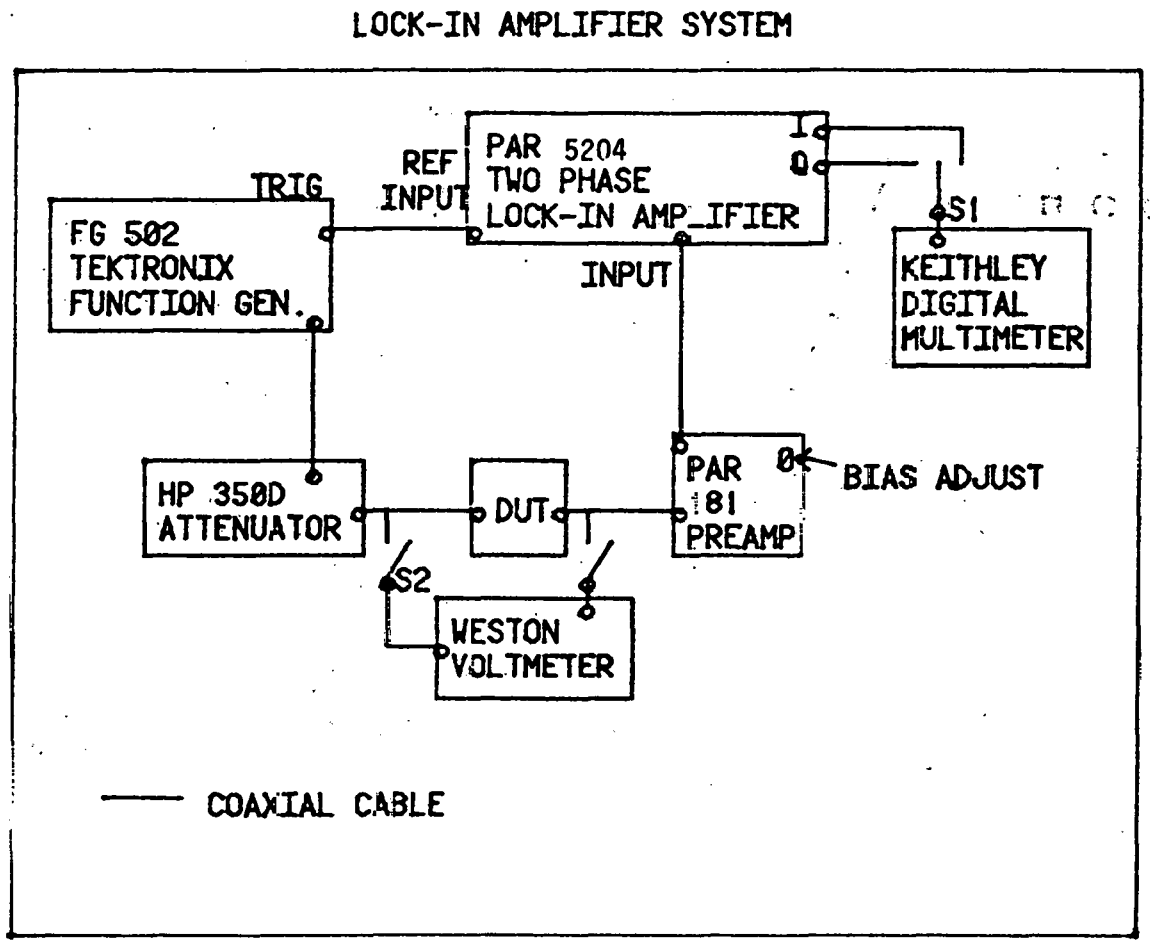


Figure 11 Lock-in-amplifier circuit for C-V-f and G-V-f studies

Figure 12 C-V-f data for a MIS diode on a single grain

#168 (R_3) on the grain

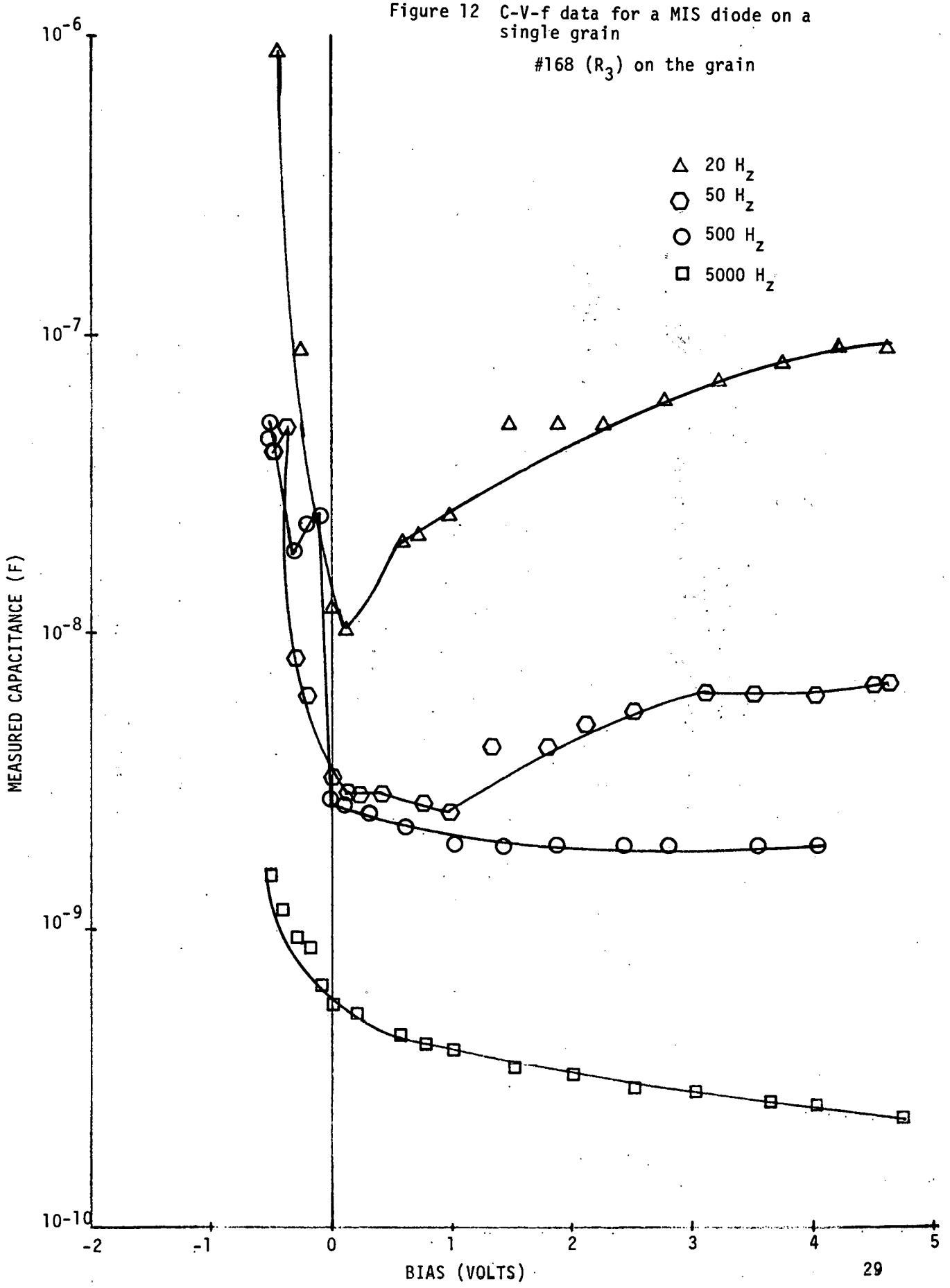
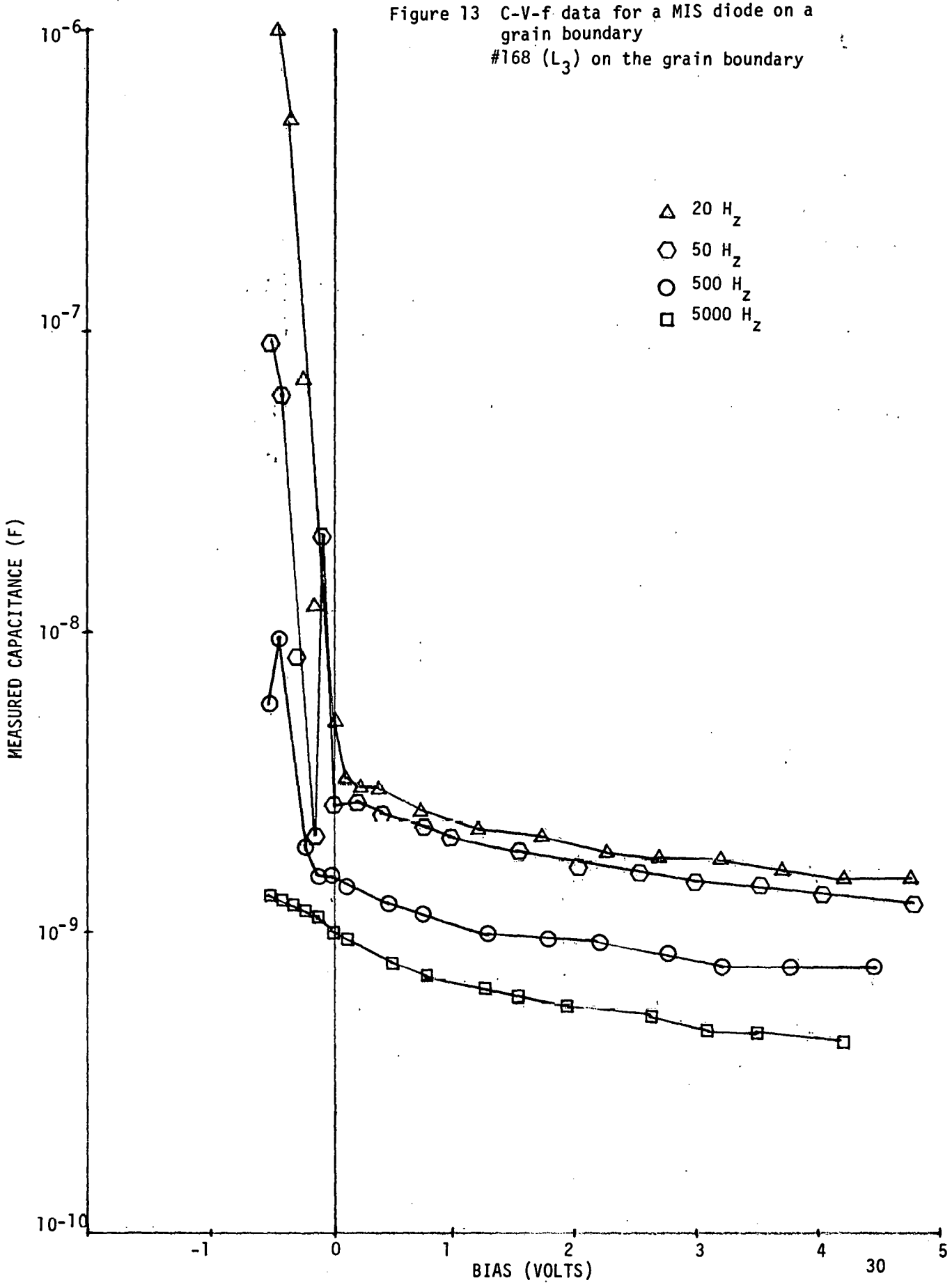


Figure 13 C-V-f data for a MIS diode on a grain boundary
#168 (L_3) on the grain boundary



would follow the variations of the measurement signal and contribute to the capacitance in an additive manner to the space charge capacitance which therefore will be higher than in the high frequency case. Accordingly, with increased inversion the capacitance rises and becomes saturated with applied bias.

It can be seen that in the 500 H_z frequency range, the capacitance becomes practically constant in both the cases R_3 and L_3, when the semiconductor surface is inverted. This constant capacitance corresponds to the limit reached by the depletion region width. In this frequency range, the majority carriers would be able to follow the dc bias but not the ac signal.

At very high frequencies in both cases, the capacitance decreases as a function of bias, which may mean that the minority carriers cannot accumulate near the surface even in the bias range corresponding to inversion. The minority carriers cannot follow the a.c. bias and hence do not accumulate at the surface or d.c. bias changes rapidly to the inversion side and capacitance is measured before minority carriers can accumulate near the surface. This may correspond to the transient case.

The two curves of 20 H_z and 50 H_z for R_3 exhibit a minimum at about 0.1 and 1 volt respectively, which is followed by an increase in the capacitance. This may be due to the fact that all charge within the semiconductor consists of acceptor ions and therefore the depletion region is comparitively large and correspondingly the space charge capacitance is small.

Conductance for both R_3 and L_3 is plotted as a function of bias at various frequencies and they are shown in Figures 14 and 15, respectively. One significant feature is that conductance decreased in the bias range 0-0.5 mV followed by an increase in the conductance which becomes saturated when it is reverse biased in the case of R_3. In the case of L_3, conductance decreases and then becomes saturated. The conductance curves at high frequency have not changed appreciably in shape but have in magnitude. The magnitude of the conductance is higher at all frequencies for R_3 compared to L_3. Also, conductance data are much more frequency dependent for L_3.

5-2 Auger, ESCA, and Elliposmeter Studies

A paper written by Dr. B. W. Lee is given in Appendix B which describes these studies related to the stability of the Cr-MIS solar cell. This work was partially reported in one of our previous reports.[8]

Figure 14 G-V-f data for a MIS diode on a single grain

#168 (R_3) on the grain

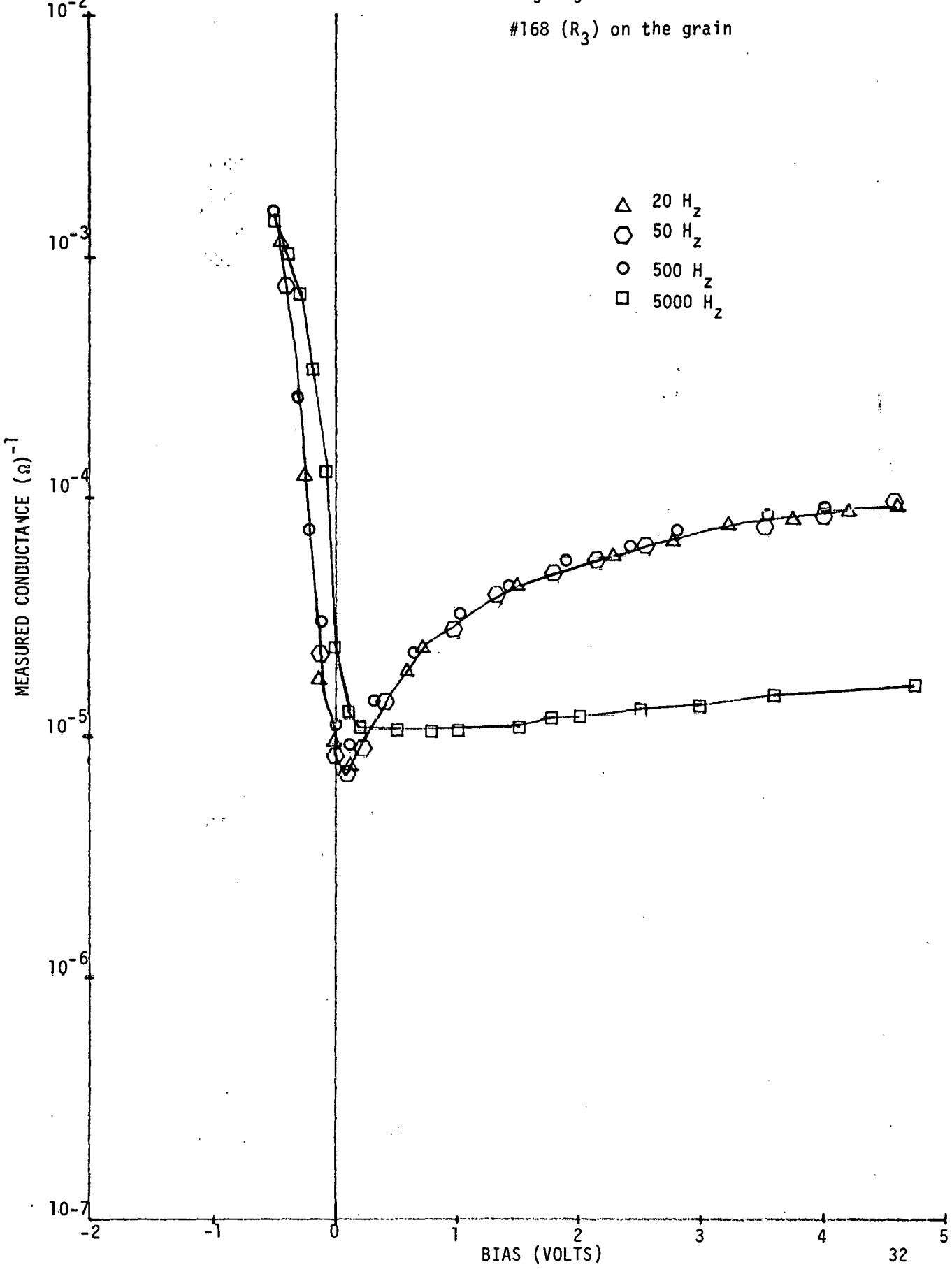
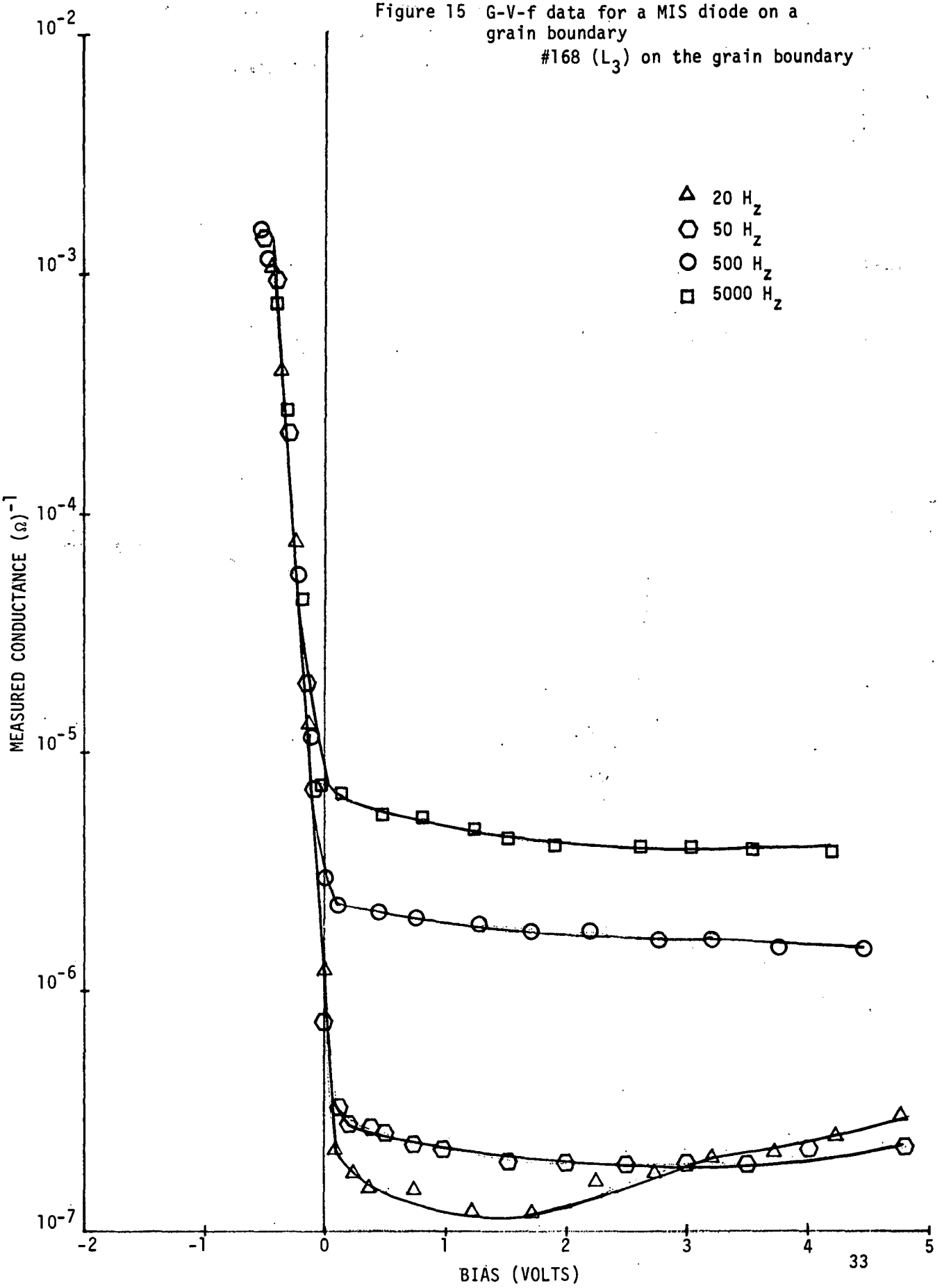


Figure 15 G-V-f data for a MIS diode on a grain boundary
#168 (L_3) on the grain boundary



6. RELIABILITY STUDIES (M. Thayer)

This reliability study explores the degradation of MIS cells exposed to light, dark, or environmental conditions. An ELH lamp calibrated at AM1 illumination was used to test each cell. Test results of the cells subject to light or dark conditions are summarized in Table 7. Cells used in the light bias study were continuously illuminated by a 300 W tungsten lamp. The open circuit voltage (V_{oc}) and efficiency (η) of these cells initially dropped 15% but are now at a relatively constant value. After a year of testing, the shelf-life study still indicates that little degradation of the MIS cells has occurred.

A solar panel consisting of nonencapsulated and encapsulated cells was placed on the roof. After a week of exposure, the fill factor of the non-encapsulated cell had dropped from .66 to .3. This indicates that the series resistance of the contact had increased. Visual inspection indicated that both the anti-reflective (AR) coating and the aluminum contact had degraded. The aluminum contact had degraded to such an extent, that in order to obtain a good contact, test probes were pierced through the anti-reflective (AR) coating further down the aluminum bus bar. Once this was done the fill factor was found to be 0.6. This is conclusive proof of degradation found in exposed contacts. Sylgard 184 was used as an encapsulant for the cells that were placed outdoors. After two months of operation the open circuit voltage had dropped 35%. Microscopic examination of an encapsulated cell indicates degradation of the aluminum grid.

Degradation of the encapsulated cells could be due to:

1) Chamical reaction.
2) Ionic transport of aluminum.
3) Impurity migration of Al into the surrounding layers.
4) Moisture.
5) Degradation of silicon, silicon ovide barrier.

Moisture tests can be performed by placing cells in 95% relative humidity. Encapsulated cells could be sprayed with saline solution. Methods of encapsulation could be improved by encapsulating cells in a vacuum or in a controlled atmosphere. Chromium could be deposited beneath the aluminum grid to prevent diffusion of aluminum into copper. Results from these tests will indicate whether to continue using Sylgard 184.

Table 7

SOLAR CELL RELIABILITY DATA

A. SHELF LIFE STUDY

Cell	Date	V_{oc}(V)	$J_{sc}(\frac{mA}{cm^2})$	FF	$P_o(\frac{mW}{cm^2})$	Comments
53	9/21/79	0.51	24.0	0.72	8.8	XTAL
	3/6/80	0.51	24.5	0.65	8.1	
	4/29/80	0.48	23.5	0.70	7.9	Now Illuminated
65	8/22/79	0.53	28.5	0.71	10.7	XTAL
	1/24/80	0.54	26.5	0.72	10.3	
	5/8/80	0.53	25.5	0.69	9.4	
	5/27/80	0.52	23.5	0.70	8.6	
	7/30/80	0.52	27.0	0.73	10.3	
	8/25/80	0.53	26.0	0.75	10.3	
	10/5/80	0.52	23.5	0.74	9.0	
	10/28/80	0.53	26.0	0.72	9.8	
206	10/12/79	0.53	28.6	0.63	9.6	XTAL
	4/8/80	0.51	30.0	0.68	10.4	
	4/29/80	0.51	30.5	0.61	9.4	
	5/27/80	0.50	28.0	0.68	9.5	
	6/27/80	0.50	29.0	0.66	9.6	
	7/30/80	0.50	31.5	0.69	10.7	
	8/25/80	0.51	30.0	0.72	10.9	
	10/5/80	0.49	30.0	0.66	9.7	
	11/28/80	0.50	28.5	0.68	9.7	

B. LIGHT BIAS STUDY

126	3/18/80	0.53	26.0	0.68	9.4	Hamco,
	5/8/80	0.51	25.5	0.67	8.7	Pressure
	5/27/80	0.51	22.5	0.70	8.0	Contract
	6/27/80	0.51	23.5	0.68	8.2	
	7/30/80	0.51	24.5	0.66	8.3	
	8/25/80	0.51	24.0	0.68	8.4	
	10/15/80	0.50	25.0	0.66	8.2	
	11/12/80	0.47	22.0	0.60	6.2	Placed outdoors (10/15/80)
162	4/1/80	0.50	23.5	0.63	7.4	Wacker,
	5/8/80	0.49	22.0	0.58	6.3	Silver
	5/27/80	0.48	19.5	0.54	5.0	Epoxy
	6/27/80	0.49	21.5	0.51	5.4	
	7/30/80	0.49	20.0	0.55	5.4	
	8/25/80	0.49	22.0	0.50	5.1	
	10/6/80	0.49	21.0	0.48	5.0	
	12/5/80	0.49	21.0	0.50	5.2	
53	5/27/80	0.48	21.5	0.72	7.4	XTAL
	6/27/80	0.48	23.5	0.72	8.2	
	7/30/80	0.48	24.0	0.72	8.3	
	8/25/80	0.48	23.5	0.72	8.1	
	10/6/80	0.47	22.5	0.71	7.5	
	12/5/80	0.47	23.0	0.70	7.7	

7. REFERENCES

1. W. A. Anderson, G. Rajeswaran, K. Rajkanan and G. Hoeft, "A Revised Process to Increase Efficiency and Reproducibility in Cr-MIS Solar Cells," IEEE Electron Device Letters, Vol. EDL-1, No. 7, pp. 128-130, July 1980.

2. W. A. Anderson and G. Rajeswaran, "An Evaluation of Potentially Low Cost Silicon Substrates for MIS Solar Cells," J. Appl. Physics, accepted for publication.

3. K. E. Bean, "Anisotropic Etching of Silicon," IEEE Trans. Elec. Dev., ED-25, 1185, 1978.

4. S. K. Dey, W. A. Anderson, A. E. Delahoy and C. Cartier, "Spectral Response and Diffusion-Length Studies of Amorphous, Polycrystalline, Ribbon, Epitaxial and Single Crystal Silicon MIS Solar Cells," J. Appl. Physics, 50 (6), June 1979, pp. 4425.

5. K. Rajkanan and J. Shewchun, "A Better Approach to the Evaluation of the Series Resistance of Solar Cells and Area Dependence of Performance Characteristics," Solid State Electronics, Vol. 22, pp. 193-197, 1979.

6. R. J. Handy, "Theoretical Analysis of the Series Resistance of a Solar Cell," S. S. Elec., 10, p. 765, 1967.

7. J. K. Kim, W. A. Anderson and S. L. Hyland, "Relating Computer Simulation Studies with Interface State Measurements of MIS Solar Cells," IEEE Trans. Elec. Dev., ED-26, p. 1777, 1979.

8. W. A. Anderson, "MIS Solar Cells on Thin Polycrystalline Silicon," SERI Report No. 2 on contract XM-0-9080-1, dated September 1980.

8. CONCLUSIONS

1. E-beam Si films on Si substrates replicate the substrate in surface features and crystallite orientation.

2. MIS cells scaled from 2 cm^2 to 4 cm^2 show about the same efficiency. Scale-up to large area is not a problem.

3. G-V-f and C-V-f data may eventually give quantitative data on defect density at the interface of grain boundaries.

9. PLANS FOR THE NEXT QUARTER

1. Continue e-beam Si deposition and further evaluate electrical properties.

2. Improve etching and D.I. H_2O procedures in preparing Si.

3. Improve MIS cell efficiency.

4. Continue evaluating grain boundaries by C-V-f and G-V-f.

5. Expand reliability studies.

10. RESEARCH PARTICIPANTS

B. W. Lee	-	Assistant Professor - Auger Study, Rutgers
V. J. Rao	-	Post Doctoral
G. Rajeswaran	-	Research Assistant
F. Kai	-	Research Assistant
M. Jackson	-	Research Assistant
M. Westcott	-	Undergraduate Assistant, Work Study
M. Thayer	-	Undergraduate Assistant
P. Talarico	-	Technician
J. Bennett	-	Secretary

11. REPORTS/PUBLICATIONS/PRESENTATIONS

1. W. A. Anderson, G. Rajeswaran, K. Rajkanan and G. Hoeft, "A Revised Process to Increase Efficiency and Reproducibility in Cr-MIS Solar Cells," IEEE Electron Devices Letters, Vol. EDL-1, pp. 128-130, July 1980.

2. W. A. Anderson, M. A. Jackson and F. Y. T. Kai, "E-Beam Deposited Thin Silicon Films for Solar Cells," IEEE Conference on Electron Devices Activities in Western New York, Rochester, New York, October 16, 1980.

3. W. A. Anderson, G. Rajeswaran, F. Kai and M. Jackson, "Studies Leading to a Thin Film MIS Solar Cell," 4th Annual Photovoltaic Advanced R & D Conference, Colorado Springs, Colorado, November 18-20, 1980.

APPENDIX A

SURVEY OF PREVIOUS WORK ON CONDUCTION MECHANISMS IN SMALL CRYSTAL POLY-SILICON

Introduction:

During the past ten years thin film polycrystalline silicon has been studied by many researchers because of the possible application to low cost, large area solar cells. Experiments as well as theories on the electrical properties of small grain size polycrystalline silicon films are studied. This section is a survey of some of the previous work done by these researchers in order to give a clear picture to study the current conduction mechanisms which will permit us to fabricate low cost, large area polycrystalline Si solar cells. Our next report will present a survey of other work and outline our approach to the problem.

(A) John Y. W. Seto[1]

(i) Sample Preparation:

Polycrystalline films ion implanted with boron to precisely control doping concentration.

(ii) Assumptions:

(1) Does not believe in "impurity segregation"[2] at the grain boundary.

(2) Electrical transport properties of polycrystalline films governed by "carrier trapping" at the grain boundary.[3,4]

(3) One type of impurity atom present. Impurity atoms are totally ionized, and uniformly distributed with a concentration of N/cm^3.

(4) Grain boundary thickness is negligible compared to grain size L. It contains Q_t/cm^2 of traps located at E_t with respect to the intrinsic Fermi level. The traps are assumed to be initially neutral and become charged by trapping a carrier.

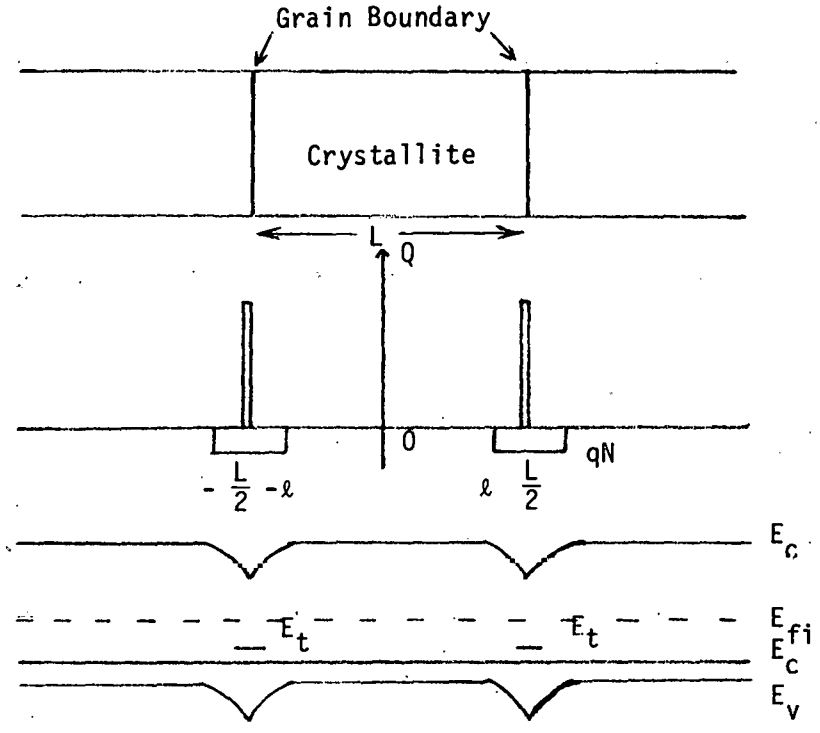


Figure A-1. Model Used by Seto[1]

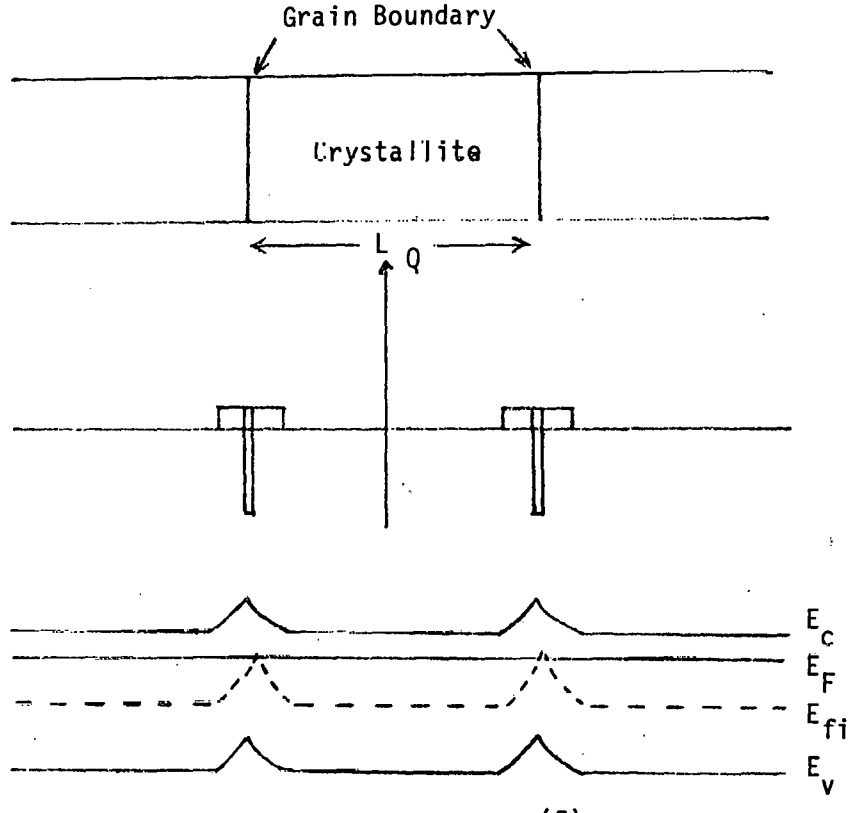


Figure A-2. Model Used by Baccarain et.al.[5]

(5) Neglect the contribution to the resistivity by the bulk of the crystallites and consider only the resistance of the grain-boundary region.

(iii) Basic Model:

The two important contributions to the current across the grain boundary are:

a) Thermionic emission

b) Tunneling (field emission)

In this paper tunneling is neglected and the dominant current is from thermionic emission. We will see below the different expressions for conductivity in the two cases and the existence of a mobility minimum.

Define:

$$p_a = \frac{n_i}{Lq}\left(\frac{2\pi\epsilon kT}{N}\right)^{\frac{1}{2}} \exp\left(\frac{E_B+E_f}{kT}\right) \exp\left[\frac{qL}{2}\left(\frac{N}{2\epsilon kT}\right)^{\frac{1}{2}}\right] \qquad \text{A-1}$$

$$J_{th} = qp_a \left(\frac{kT}{2\pi m^*}\right)^{\frac{1}{2}} \exp\left(-\frac{qV_R}{kT}\right)\left[\exp\left(\frac{qV_R}{kT}\right)-1\right] \qquad \text{A-2}$$

If $V_a \ll kT$

$$J_{th} = q^2 p_a \exp\left(\frac{1}{2\pi m^* kT}\right)^{\frac{1}{2}} \exp\left(-\frac{qV_R}{kT}\right) V_a \qquad \text{A-3}$$

$$\sigma = Lq^2 p_a \left(\frac{1}{2\pi m^* kT}\right)^{\frac{1}{2}} \exp\left(-\frac{qV_R}{kT}\right) \qquad \text{A-4}$$

Case (1): $LN < Q^*$

Under case (1) the crystallite is completely depleted of carriers and the traps are partially filled.

$$E_B \propto N \qquad \text{A-5}$$

$$LN = \frac{Q_t}{2\exp[(E_t-E_f)/kT]H} \qquad \text{A-6}$$

$$E_f = E_t - kT \ln[\tfrac{1}{2}Q_t/LN - 1] \qquad \text{A-7}$$

$$\sigma \propto \exp[-(\tfrac{1}{2} E_g - E_f)/kT] \qquad \text{A-8}$$

$$\mu_{eff} = Lq\left(\frac{1}{2\pi m^* kT}\right)^{\frac{1}{2}} \exp\left(-\frac{E_B}{kT}\right) \qquad \text{A-9}$$

Case (2): $LN > Q_t$

Under case (2), only part of the crystallite is depleted of carriers.

$$E_B \propto \frac{1}{N} \qquad \text{A-10}$$

$$\sigma \propto T^{\frac{1}{2}} \exp\left(-\frac{E_B}{kT}\right) \qquad \text{A-11}$$

(iv) Conclusions:

From eqs. (5) and (10), the energy barrier, E_B, exhibits a maximum as a function of doping. Eq. (9) shows that the mobility will have a minimum as a function of doping. The minimum occurs at

$$LN = Q_t$$

This behaviour is explained well by trapping state theory.

(B) Baccarani, Ricco and Spadini[5]

(i) Sample preparation:

Phosphorus-doped sputter deposited polycrystalline silicon films.

(ii) Assumption:

a) The existence of monovalent trapping centers.

b) Grain-boundary traps consist of states with a uniform density of acceptors in the upper half of the band-gap and donors in the lower half.

(iii) Basic Model:

(1) Monovalent trapping states at the grain boundary

Define: N_t = acceptor states of grain boundary traps

N_D = impurity concentration

N_D^* = impurity concentration such that when $N < N_D^*$, the crystallites are entirely depleted.

W = depletion width

L = grain size

E_B = barrier height

E_a = activation energy

For $N_D < N_D^*$, the crystallites are entirely depleted:

$$E_B = \frac{q^2 L^2 N_D}{2\varepsilon} \qquad \text{B-1}$$

$$\sigma \propto \exp(-\frac{E_a}{kT}) \qquad \text{B-2}$$

where

$$E_a = \tfrac{1}{2} E_G - E_t \qquad \text{B-3}$$

For $N_D > N_D^*$, the crystallite are partially depleted:

$$\text{(i)} \quad E_B = \frac{q^2 N_t^2}{8\varepsilon N_D} \qquad \text{for } E_F - E_t - E_B >> kT \qquad \text{B-4}$$

$$\text{(ii)} \quad E_B = \tfrac{1}{2} E_G - E_t + kT \ln\{qN_D^{\frac{1}{2}} N_t / [N_c (2\varepsilon N_B)^{\frac{1}{2}}]\} \text{ for } E_t + E_B - E_F >> kT \qquad \text{B-5}$$

$$\sigma \propto \frac{1}{T} \exp(-\frac{E_a}{kT}) \qquad E_a = E_B \qquad \text{B-6}$$

$$\text{(iii)} \quad \sigma \propto \frac{(E_B)^{\frac{1}{2}}}{(kTN_t)} \exp(-\frac{E_a}{kT}) \qquad \text{B-7}$$

(2) Continuous energy distribution of interface states

The limiting value of the impurity concentration N_D corresponding to complete depletion of the crystallite is N_D^*:

$$N_D^* = \left(\frac{N_{ss}}{L}\right)\left(1 + \frac{q^2 N_{ss} L}{8\varepsilon}\right)^{-1} kT \, \ell n\left(\frac{N_D^*}{n_i}\right) \qquad \text{B-8}$$

For $N_D < N_D^*$

$$\sigma \propto \frac{1}{T} \exp\left(-\frac{E_a}{kT}\right) \qquad \text{B-9}$$

when

$$E_a = \frac{1}{2} E_G - \frac{LN_D}{N_{sc}} \qquad \text{B-10}$$

For $N_D > N_D^*$

$$E_B = \frac{q^2 N_{ss}^2 E_F^2}{8\varepsilon N_D} \qquad \text{for } N_D >> \frac{q^2 N_{ss}^2 E_F}{2\varepsilon} \qquad \text{B-11}$$

$$E_B = E_F \qquad \text{for } N_D << \frac{q^2 N_{ss}^2 E_F}{2\varepsilon} \qquad \text{B-12}$$

(iv) Conclusion:

a) Impurity segregation and carrier trapping at the grain boundary both take place in polycrystalline silicon. Experimental data show evidence of some impurity segregation at the grain boundary, at least when it is phosphorus doped.

b) Trapping states are nearly monovalent, and peaked at midgap.

(C) H. C. Card and W. Hwang[6]

(i) Sample preparation: Not mentioned.

(ii) Assumption:

The dark-carrier transport in Schottky barriers on polycrystalline silicon is dominated by both majority carrier and minority carrier transport. For certain values of grain sizes, the minority carrier injection dominates so that the metal-polysilicon contact resembles a p-n junction rather than a Schottky barrier.

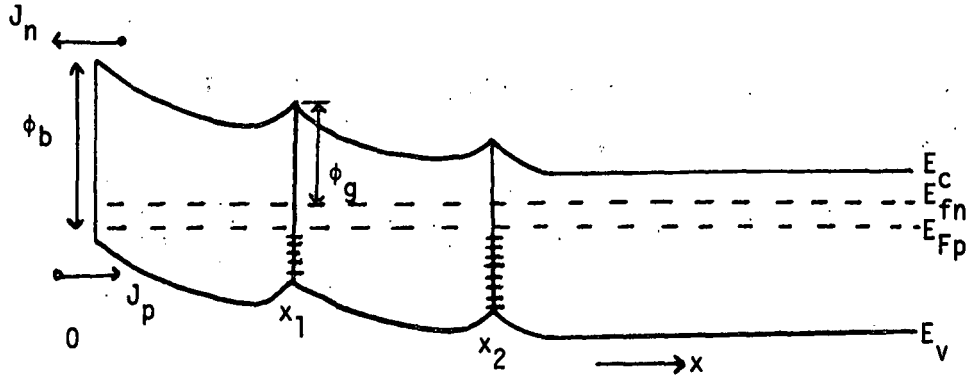
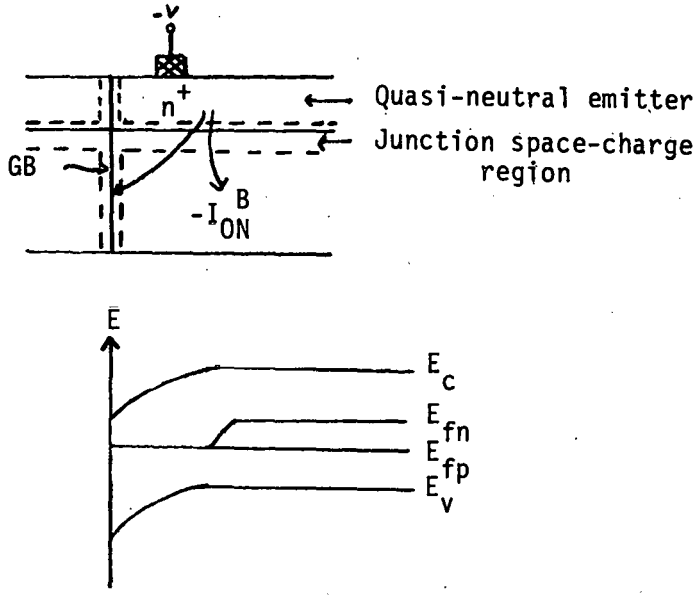
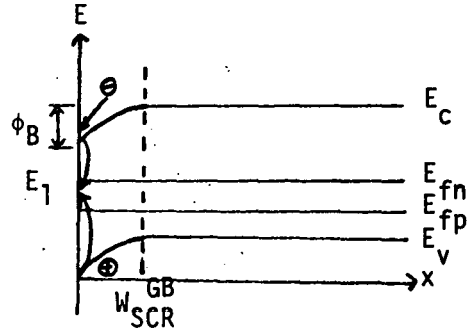


Figure A-3. Model Used by Card and Hwang[6]





Quasi-equilibrium and monoenergetic density of surface states.

Figure A-4. Model Used by Fossum and Lindholm[9]

(iii) Basic Model:

For n-type semiconductor, the majority carrier current is

$$J_n = A^* T^2 \exp(-\frac{q\phi_b}{kT})[\exp(\frac{qV}{kT}) - 1] \qquad C\text{-}1$$

The contribution to the dark current from the injection of minority carriers:

$$J_p = \frac{qD_p n_i^2}{L_p N_d} [\exp(\frac{qV}{kT}) - 1] \qquad C\text{-}2$$

For low doping concentations Jp/Jn is negligible for $\phi_b \leq 1.0$ eV

For polycrystalline silicon the effective value of L_p may be expected to be short. J_p/J_n may be expected to increase to exceed unity. Consider two different cases in majority (or minority) carrier transport in the polysilicon Schottky barrier.

(A) Majority-Carrier Transport:

1) Electrode-Limited Conduction:

Transport of electrons across the grain boundaries does not restrict the current.

2) Bulk-Limited Conduction:

The majority-carrier current is dominated by the transport across the grain boundaries; the contact potential ϕ_b does not restrict the current. (The case for the low ϕ_b)

Assuming there are N grain boundaries each of barrier height ϕ_g within the silicon film and these are parallel to the surface of the semiconductor:

$$J_n = 2A^* T^2 \exp(-\frac{q\phi_g}{kT}) \sinh(\frac{qV}{2NkT}) \qquad C\text{-}3$$

Define: V_1 = voltage drop across the Schottky barrier

V_2 = voltage drop across the total of the N grain boundaries

$$J_n = A^* T^2 \exp(-\frac{q\phi_b}{kT})[\exp(\frac{qV_1}{kT}) - 1]$$

$$= A^* T^2 \exp(-\frac{q\phi_g}{kT}) \sinh(\frac{qV_2}{2NkT}) \qquad \text{C-4}$$

The applied voltage $V = V_1 + V_2$

(B) Minority-Carrier Transport:

1) The presence of grain boundaries in polycrystalline silicon is expected to reduce the majority-carrier current for a given voltage.

2) The minority-carrier injection current is increased by the presence of the grain boundaries. The efficient recombination centers reduce L_p.

The recombination rate at the grain boundary:

$$J_{r1} = qN_{is}\, \sigma\, vn(x_1)V_1 \qquad \text{C-5}$$

N_{is} = interface state density at the grain boundary

σ = capture cross-section for electrons

v = thermal velocity

$n(x_1)$ = electron concentration of the first grain boundary at position $x = x_1$.

The recombination current (J_{r1}) of (5) assumes that all interface states between the quasi-Fermi levels E_{fn} and E_{fp} for electrons and holes contribute equally to the recombination. It assumes that the recombination traffic through these states is limited by the supply of electrons rather then of holes.

The effective diffusion length (L_p^*) for the injected minority carriers:

$$L_p^* = N_r d \qquad \text{C-6}$$

N_r = no. of grain boundaries near the silicon surface

d = grain size to allow all of the injected minority carriers to recombine.

$$J_r = qN_{is}\,\sigma\,v\,N_e \exp(-\frac{q\phi_q}{kT})\,V_1 \qquad \text{C-7}$$

$$J_p = \sum_r J_{ri} = N_r J_r = \frac{qD_p n_i^2}{L_p^* N_d}\left[\exp(\frac{qV_1}{kT}) - 1\right] \qquad \text{C-8}$$

After some manupulation, the minority-carrier injection current is obtained:

$$J_p = qn_i \left(\frac{D_p N_c N_{is}\sigma v V_1}{N_d d}\right)^{\frac{1}{2}} \exp(-\frac{q\phi_q}{2kT}) \exp(\frac{qV_1}{2kT}) \qquad \text{C-9}$$

The minority-carrier injection ratio is defined as:

$$\gamma = \frac{J_p}{J_n + J_p} \qquad \text{C-10}$$

It is very close to unity in the polycrystalline Schottky barrier; the minority-carrier injection often dominates the dark current.

(iv) Conclusion:

(1) Majority-carrier transport in metal-polysilicon Schottky barriers undergoes a transition with bias voltage from electrode-limited to bulk-limited.

(2) For a range of grain sizes, and of interface state densities at the grain boundary, the dark current may be dominated by the injection of minority carriers.

(3) The minority-carrier current obeys an $\exp(\frac{qV}{2kT})$ dependence reminiscent of the high-injection regime of single-crystalline Si.

(4) A transition from an $\exp(\frac{qV}{2kT})$ to $\exp(\frac{qV}{kT})$ dependence is observed with the low-voltage component due to minority carrier diffusion current.

(D) A. K. Ghosh and T. Fang[7,8]

(i) Sample Preparation:

3 μm grain size SnO_2/Si heterojunction cell. Poly-silicon was obtained from Wacker.

(ii) Assumptions:

(1) For columnar-growth polycrystalline solar cells, the open circuit photovoltages and fill factors were assumed to be the same as in single crystal.

(2) The dopant concentration at the mobility minimum follows:

$$N_d \sim \frac{10^{12}}{d} \text{ cm}^{-3} \qquad \text{D-1}$$

(3) No variation of mobility is assumed.

(4) The change in lifetime is the more dominant factor.

$$\tau_{eff} = \frac{1}{\sigma v N_{sr}} \qquad \text{D-2}$$

N_{sr} = effective density of recombination centers.

(iii) Basic Model:

(A) Dark I-V characteristics:

(i) Grain sizes $\leq$ 100 μm

$$J = J_{od}(e^{\lambda d V}-1) + J_{or}(e^{\lambda r V}-1) \qquad \text{D-3}$$

$$J = J_{or}(e^{\lambda r V}-1) \quad \text{for small grains} \qquad \text{D-4}$$

where $J_{or} = \frac{q n_i w}{10^{-5} d}$ = reverse saturation current due to recombination

(ii) Grain size > 100 μm, forward bias near V_{oc}

$$J = J_{ot}(e^{\lambda t V}-1) + J_{od}(e^{\lambda d V}-1) \qquad \text{D-5}$$

where $J_{ot} = AT^2 \exp(-\frac{\phi_B}{kT})$

$$J_{od} = \frac{q D_p P_{no}}{L_p} + \frac{q D_n n_{po}}{L_n}$$

(B) The Short-Circuit Photocurrent:

(i) From bulk contribution:

$$J_2 = q\left[\frac{\alpha_2 N^1 \exp(-\alpha_2 \ell_2)}{\alpha_2 + \frac{1}{L_p}} - \frac{2\alpha_2 N^1 \exp(-\alpha_2 \ell_2)\left[\exp(-\frac{d}{L_p}) - \exp(-\alpha_2 d)\right]}{L_p(\alpha_2^2 - \frac{1}{L_p^2})\left[\exp(\frac{d}{L_p}) - \exp(-\frac{d}{L_p})\right]}\right] \quad \text{D-6}$$

(ii) From barrier contribution

$$J_1 = GqN^1[1 - \exp(-\alpha_2 \ell_2)] \quad \text{D-7}$$

The total current for MIS, SnO_2/Si or ITO/Si is

$$J_{sc} = J_1 + J_2 \quad \text{D-8}$$

(C) The open-circuit photovoltage:

$$V_{oc} = \frac{nkT}{q} \ell n \left(\frac{J_{sc}}{J_o}\right) \quad \text{D-9}$$

(i) For grain size $\leq$ 100 μm

$$V_{oc} = \frac{2kT}{q} \ell n \left(\frac{J_{sc}}{J_{or}}\right) \quad \text{D-10}$$

(ii) For grain size $\geq$ 100 μm

$$V_{oc} = \frac{kT}{q} \ell n \left(\frac{J_{sc}}{J_{od}}\right) \quad \text{D-11}$$

(D) Fill factor

$$FF = \left(1 - \frac{1}{\lambda V_{oc}}\right)\left(1 - \frac{\ell n \lambda V_{oc}}{\lambda V_{oc}}\right) \quad \text{D-12}$$

(iv) Conclusion:

(1) Grain boundaries act as recombination centers (with capture cross-section of 2×10^{-16} cm^2)

(2) For small grain sizes, the surface recombination centers affect the lifetime more than any dopant concentration.

(3) For materials with a direct bandgap, smaller grain sizes and thicknesses are likely to result in efficiencies equivalent to thicker indirect bandgap material of larger grain size.

(4) Depending on the height of the intergrain boundary barriers, tunneling rather than thermionic emission may be the preferred mode of intergrain boundary crossing for carriers in the dark.

(E) J. G. Fossum and Fredrik A. Lindholm[9]

(i) Sample Preparation:

Thin film polysilicon devices from C. Feldman. No experimental data are shown.

(ii) Assumptions:

(1) Recombination occuring in the grain boundary charge region reduces the excess electron density to nearly zero at the edge of the space-charge region.

(2) Grain-boundary recombination rates are small enough so that both E_{fn} and E_{fp} are nearly flat and the separation is nearly constant across the space charge region.

(3) The grain-boundary width is much smaller than the space-charge region width, $W_{scr_o}^{GB}$.

(iii) Basic Model:

A. Thermal Equilibrium

Consider a distribution of donor ($N_{st}^{D}(E)$) and acceptor ($N_{st}^{A}(E)$) surface states within the bandgap.

A net charge density Q_{GB}:

$$Q_{GB} = q \int_{o}^{E_g} N_{st}^{D}(E)[1 - f(E,E_f)]\, dE - q \int_{o}^{E_g} N_{st}^{A}(E) f(E,E_f) dE \qquad E\text{-}1$$

where E_F = Fermi level, depends on the doping level N_{AA}

$$[E_F - E_v]_x > W_{scro}^{GB} \simeq kT\, \ell n\left(\frac{N_v}{N_{AA}}\right) \qquad E\text{-}2$$

N_V = effective density of states at the valence band.

In polycrystalline silicon, Q_{GB} is positive for p-type grains.

The grain-boundary potential barrier height ϕ_{Bo} is obtained by

$$\phi_{Bo} = \phi_{Bo}[N_{AA}, N_{st}^{D}(E), N_{st}^{A}(E)] \qquad \text{E-3}$$

(B) Nonequilibrium

For quasi-equilibrium assumption:

$$P(x)N(x) = N_i^2 \exp\left(\frac{E_{FN}-E_{FP}}{kT}\right) \simeq \text{constant} \qquad \text{E-4}$$

with excitation applied: $P(0), N(0) >> n_i$

In order to specify P(0), N(0)

a) The excitation provides substantial numbers of holes and electrons at the grain-boundary surface.

b) No physical constraints are imposed on ϕ_B.

For any nonequilibrium, steady state condition, with "sufficient excitation," P(0) and N(0) will have attained the values that maximize Us.

$$Us = \frac{1}{2} (S_p S_n)^{\frac{1}{2}} n_i \exp\left(\frac{E_{FN}-E_{FP}}{2kT}\right) \qquad \text{E-5}$$

The grain boundary-recombination current density J_{GB}^{B}:

$$J_{GB}^{B} = - J_p(0) = J_n(0) = \frac{9}{4} (S_p S_n)^{\frac{1}{2}} n_i \exp\left(\frac{E_{FN}-E_{FP}}{2kT}\right) \qquad \text{E-6}$$

$$S_{n(eff)}^{GB} = \frac{1}{4} (S_n S_p)^{\frac{1}{2}} N_{AA}^{\frac{1}{2}} [N(W_{scr}^{GB})]^{-\frac{1}{2}} \qquad \text{E-7}$$

This is a "nonlinear" boundary condition for minority carriers at the edge of the grain boundary space charge region.

For "high injection:"

$$S_{n(eff)}^{GB} = \frac{(S_p S_n)^{\frac{1}{2}}}{4} \qquad \text{E-8}$$

The boundary condition is "linear."

The recombination current density at the grain boundary:

$$J_{GB}^{SCR} = \frac{q}{2} (S_p S_n)^{\frac{1}{2}} n_i \exp(\frac{qV}{2kT}) \qquad \text{E-9}$$

(iv) Conclusion:

(1) This theory defines the effective minority-carrier lifetime in a grain in terms of the actual lifetime and the effective recombination velocity.

(2) The reciprocal slope factor of exactly two results from the quasi-equilibrium and steady state condition at the grain boundary.

(3) The fundamental physical mechanisms which influence the cell conversion efficiency is revealed from analysis of the dark current-voltage characteristics.

REFERENCES

1. John Y. W. Seto, J. Appl. Phys., 46, 12 (1975).
2. M. E. Cowher and T. O. Sedwick, J. Electrochem. Soc., 119, 1565 (1972).
3. P. Rai-Choudhury and P. L. Hower, J. Electrochem. Soc., 120, 1761 (1973).
4. T. I. Kamins, J. Appl. Phys., 42, 4357 (1971).
5. G. Baccarain, B. Ricco and G. Spadini, J. Appl. Phys., 49, 5565 (1978).
6. H. C. Card and W. Hwang, IEEE Trans. Electron Devices, Vol. ED-27, No. 4, 700 (1980).
7. A. K. Ghosh, Tom Feng, M. Maruska and C. Fishman, Thin Film Polycrystalline Silicon Solar Cells, Quarterly Report #1, January 1, 1979 - March 31, 1979.
8. A. K. Ghosh, Tom Feng, H. Maruska and C. Fishman, Quarterly Report #2, April 1, 1979 - June 30, 1979.
9. J. G. Fossum and F. A. Lindholm, IEEE Trans. Electron Devices, Vol. ED-27, 692 (1980).

APPENDIX B

STUDY OF STABILITY OF MIS POLYCRYSTALLINE SILICON SOLAR CELLS BY AUGER ELECTRON SPECTROSCOPY*

B. W. Lee, J. M. Kuo, and B. Lalevic
Department of Electrical Engineering
Rutgers University
Piscataway, New Jersey 08854

and

W. A. Anderson
Department of Electrical Engineering
SUNY at Buffalo
4232 Ridge Lea Road
Amherst, New York 14226

* Supported by Department of Energy (DE-AC 03-79ET23044), NSF (ENG 78-10445), Air Force Office for Scientific Research (AF-0136) and Research Corporation.

ABSTRACT

Auger electron spectroscopy and ion sputtering techniques were used to investigate the free surface composition and MIS solar cell fabricated on polycrystalline silicon. A layer of ~20Å of mixture of silicon oxide and chemisorpted oxygen atoms were found on the Si surface. For the Cr-Cu-Cr-SiO_2-Si solar cell, the copper layer is the key factor for reducing the series resistance of the metal layers. The pure oxide layer was found to be almost nonexistant and a mixture of silicon oxygen and chromium was detected between the silicon and metal interface. Compositions of the cell were investigated as a function of temperature. The results were used to estimate the life time of the cell. It was found that the cell should have a very long life time if operated under 200°C.

INTRODUCTION

The MIS (Metal-Insulator-Semiconductor)-Schottky barrier solar cell is currently receiving a great deal of attention in view of its simplicity and applicability to the large-area thin-film semiconductor solar cells that may prove suitable for terrestrial solar energy conversion. The MIS polycrystalline silicon solar cell is of particular interest because of its advanced processing technology and the possible low cost for mass production. The ultimate goal is to produce silicon cells at a cost of < \$0.50/W with an efficiency > 10%.

It has been reported [1-5] that the presence of a thin insulating layer ($\sim$20Å) at the metal-semiconductor interface of a Schottky-barrier solar cell would improve the open-circuit voltage of the cell. The insulating layer has an associated tunneling probability and thus reduces the dark (majority carrier) current of the MIS-Schottky barrier [6]. As a result of decreasing the dark current, the open-circuit voltage is increased, and the conversion efficiency of the solar cell is thus enhanced. However, the conversion efficiency is strongly dependent on the semiconductor surface condition and the method of preparing the metals [7].

Solar cells are normally operated under an evaluated temperature 50 ~ 100°C. Atomic interdiffusion between the metal, oxide and semiconductor layers of the cell at the evaluated temperature could possibly cause degradation of the cell and thus reduce its lifetime. It is important to investigate the compositons and the interdiffusion of the various films in a MIS solar cell in order to estimate its lifetime.

In this paper we report the results of the compositional studies on the metal semiconductor interface and on temperature influence on metallic interdiffusion.

EXPERIMENTAL

The dimensions of the various films in a Wacker polycrystalline Si MIS solar cell are indicated in Fig. 1. The fabrication process has been reported previously [8].

Figure 1 shows the structure of a Cr-Cu-Cr-SiO_2/Si MIS solar cell for Auger study. Chromium is chosen as the metal film for its low work function and the fact that it becomes continuous at ~ 30Å thichness. A thin copper film (~ 50Å) is introduced above the chromium film forming a Cr-Cu-Cr sandwich to reduce the series resistance of the metal layer. The top Cr layer is introduced to prevent oxidation of the thin Cu film. An efficiency of 8.8% was reported [8] on cells fabricated on Wacker polycrystalline Si using the MIS structure shown in Fig. 1. Actual solar cells use 30Å Cr adjacent to the SiO_2 and do not have the top Cr layer which increases optical transmission into the Si.

A series of studies on MIS solar cell compositons and interatomic diffusion between various films after different heat treatments were conducted using Auger electron spectroscopy (AES) and ion sputtering techniques. The compositions of a polycrystalline silicon with a thin oxide layer (~ 20Å) were also investigated for comparison with the results of the completely fabricated solar cells. The measurements of the film compositions were conducted in an ultra-high

vacuum (UHV) system equipped with low energy electron diffraction (LEED), Auger electron spectroscopy (AES) and an ion sputtering gun. A schematic diagram of the UHV system is shown in Figure 2. Samples were mounted in the main chamber and then the system was pumped to 10^{-9} torr. The surface compositions of both free polycrystalline silicon and MIS solar cell surfaces were studied by AES with a CMA (cylindrical mirror analyzer). Ion-sputtering AES profiles were taken for analyses of the compositions of the metal, oxide and silicon layers.

Six diodes cut from the same wafer were subjected to heat treatments at different temperatures and then analyzed by Auger profiling. The samples studied are listed in Table 1. Samples 1 and 2 were not heat-treated. In sputtering through the metal and oxide layers, complete Auger profiles were taken at metal-metal, metal-oxide and oxide-semiconductor interfaces to carefully examine the atomic interdiffusion between the various layers.

RESULTS AND DISCUSSION

Figure 3a shows the Auger profile of the polycrystalline silicon virgin surface. The surface was contaminated with carbon and oxygen, and a shift in the high energy Si Auger peaks was not observed. The intensity of the low energy Si peak was weak, as indicated in Fig. 3a, because the surface was covered by carbon and oxygen, and the low energy peak has a shallow ($< 10\text{Å}$) electron escape depth. A small shift in low energy Si peak was observed when the low energy part of the profile was amplified. This indicated that only a small portion of the Si atoms was oxidized at the surface. The oxygen peaks were greatly reduced

after a few seconds of ion sputtering as shown in Fig. 3b, thus confirming that most of the oxygen atoms were chemisorpted to the silicon surface.

Figure 4 shows the composition of the surface of sample 2. The chromium surface had a very large amount of oxygen. In Fig. 5, the ion-sputtering AES profile shows the compositions of the cell from the chromium surface to the polycrystalline silicon. It is clear that oxygen and chromium existed throughout and diffused into the silicon for a thickness of 35 to 40Å.

The fact that a large amount of oxygen was detected in both chromium layers indicated that a large portion of the chromium was oxidized. The oxygen was introduced into the chromium layers during the device fabrication purposely to reduce the work function of the chromium layer [7,9]. The resistivity of the chromium film would probably increase by the existance of oxygen atoms which are likely to oxidize part of the chromium atoms to form chromium oxide. On the other hand, the copper film over the Cr layer would reduce the series resistance of the whole metal film and thus of the completed solar cell. In general, the boundary between the copper and chromium layers is not well defined because of the interdiffusion between the copper and the chromium layers as shown in Fig. 5. It is significant that the Cu does not fully penetrate the Cr to disturb the Cr-SiO_2-Si region. It is clear that introducing the copper film into the cell is the key factor for a low internal resistance cell.

The SiO_2 layer between the chromium and silicon layers is rather difficult to define. As shown in Figure 5, the oxygen signal

at this region seemed to be associated with the chromium rather than the silicon. Figure 6 is the AES profile taken at this region. Elemental silicon atoms have an Auger peak at 92 eV. When the silicon atoms are oxidized, this peak shifts from 92 eV to 86 eV. A large silicon peak at 92 eV is observed in Fig. 6. This indicated that the silicon Auger signal intensity mostly came from elemental silicon atoms rather than from silicon atoms of SiO_2. In other words, only a small portion of oxygen atoms were oxidizing silicon atoms and the rest were either associated with chromium atoms or simply mixed with Cr and Si without oxidizing either of them. Further studies are required to clarify the role of the SiO_2 or interfacial layer in a MIS solar cell.

Figures 7 to 10 show the ion-sputtering AES results of samples 3 to 6, respectively. A careful study of these profiles shows that the cells are stable with respect to heat treatment under 200°C. No further interdiffusion between different films was observed after the devices were fabricated. It is clear from Fig. 9 that copper atoms do not diffuse through the chromium layer adjacent to silicon even after 70 hours of heat treatment at 203°C. This indicates that the cell is not likely to degrade if operated under 200°C. However, operating a MIS solar cell at a temperature higher than 200°C would result in a severe degradation. Figure 10 shows the AES ion-profile of sample 6 which was heated to 600°C in an UHV chamber for 10 minutes. It is clear that the cell is completely destroyed by diffusion of copper atoms throughout the whole cell.

CONCLUSION

In conclusion, AES studies of the MIS solar cells indicated that the cells have a temperature limit of 200°C for long lifetime operation. Diffusion of copper atoms in the cell becomes a fatal problem at temperatures above 200°C. The oxide layer in the MIS cell is a complex film with contents of chromium, silicon and oxygen and its important role in a MIS cell operation needs further study and clarification. Another interesting aspect is the trade-off between the reduction in a work function and increase in series resistance by introducing oxygen into chromium layer. A systematical study of the open-circuit voltage of these cells with different oxygen content should optimize the MIS cell operation.

ACKNOWLEDGMENT

We would like to thank R. K. Ni and M. Rowe for their assistance with the experiment.

REFERENCES

[1] R. J. Stirn and Y. C. M. Yeh, Appl. Phys. Lett. 27, 95 (1975).

[2] W. A. Anderson and R. A. Milano, Proc. IEEE 63, 206 (1975).

[3] D. R. Lillington and W. G. Townsend, Appl. Phys. Lett. 28, 97 (1976).

[4] H. C. Card and E. S. Yang, Appl. Phys. Lett 29, 51 (1976).

[5] H. J. Hovel, Solar Cells, Academic Press (1975).

[6] H. C. Card and E. H. Rhoderick, J. Phys. D: Appl. Phys. 4, 1589 (1971).

[7] Wayne A. Anderson, Jin K. Kim and Alan E. Delahoy, IEEE Trans. Electron Devices, Vol. Ed-24, No. 4, 483 (1977).

[8] W. A. Anderson, A. E. Delahoy, J. K. Kim, S. L. Hyland and S. K. Dey, Appl. Phys. Lett. 33(7), 588 (1978).

[9] J. C. Peruchetti, G. Gewinner and A. Jaegle, Surface Science 88, 479 (1979).

FIGURE CAPTIONS

Fig. 1: Structure of a MIS solar cell. The copper layer is introduced to reduce the series resistance of the metal film and the top chromium layer is for preventing the copper film from oxidation.

Fig. 2: Schematic diagram of the UHV system equipped with LEED, AES, mass spectrometer, and ion sputtering gun for surface analysis.

Fig. 3a: AES profile of Si virgin surface. Small SiO_2 signal was detected.

Fig. 3b: AES profile of Si surface after a few seconds of ion sputtering. The oxygen peak was greatly reduced by sputtering and thus confirmed that the oxygen atoms were chemisorpted to the silicon surface.

Fig. 4: AES profile of the surface of sample 2. Sample 2 was not heat treated. The chromium surface had a very large amount of oxygen.

Fig. 5: The ion-sputtering AES profile of sample 2. It showed the compositions of the cell from the chromium surface to the polycrystalline silicon.

Fig. 6: An AES profile taken at the SiO_2 region. It indicated that the silicon Auger signal was contributed for the most part from elemental silicon atoms rather than from SiO_2.

Fig. 7: The ion-sputtering AES profile of sample 3. Cu did not penetrate the Cr into the SiO_2 region.

Fig. 8: The ion-sputtering AES profile of sample 4. It also shows that Cu does not influence the electronic properties at the Cr-SiO_2 junction and the cell is stable even after 158°C, 168 hours heat treatment.

Fig. 9: The ion-sputtering AES profile of sample 6. It shows that the cell is not likely to degrade if operated under 200°C.

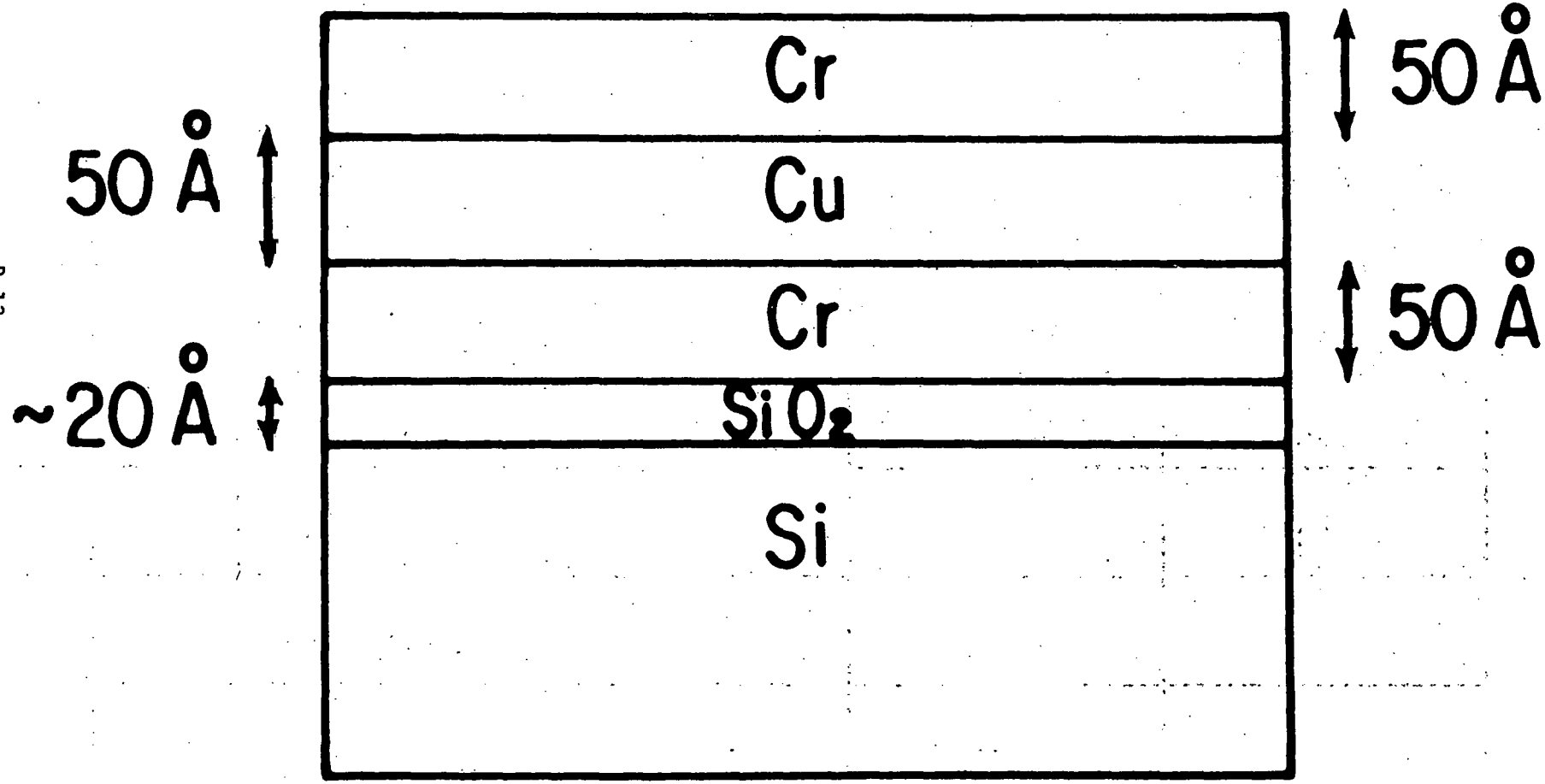
Fig. 10: The ion-sputtering AES profile of sample 6 which was heated to 600°C in an UHV chamber for 10 minutes. The cell is completely destroyed by diffusion of copper atoms throughout the whole cell.

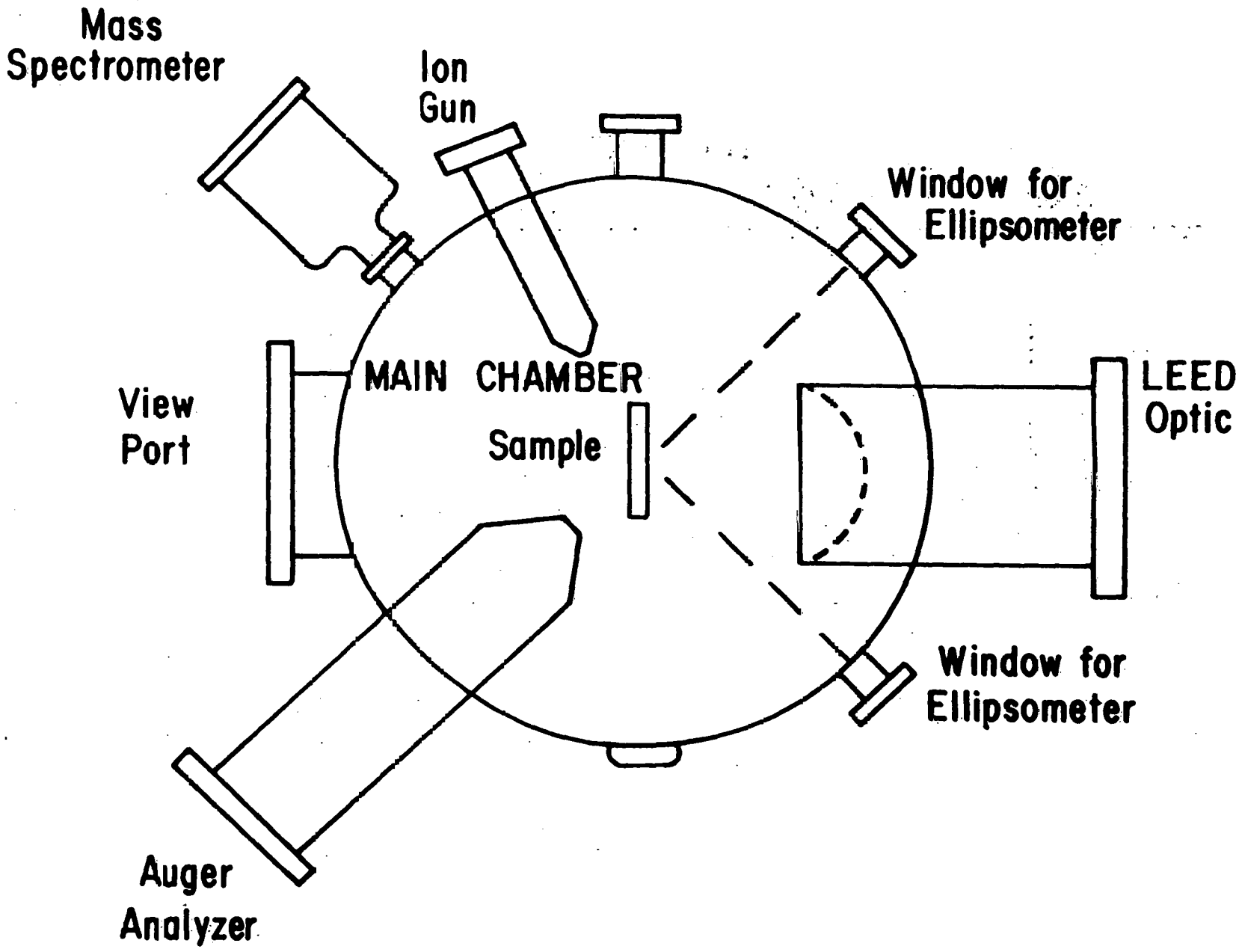
SAMPLE	STRUCTURE	HEATING TEMPERATURE (° C)	HEATING ENVIRONMENT	HEATING TIME (Hours)
1	SiO_2/Si^*	----	----	----
2	$Cr\text{-}Cu\text{-}Cr\text{-}SiO_2/Si^*$	---	----	----
3	$Cr\text{-}Cu\text{-}Cr\text{-}SiO_2/Si^*$	150	UHV	4.5
4	$Cr\text{-}Cu\text{-}Cr\text{-}SiO_2/Si^*$	158	atomosphere	168
5	$Cr\text{-}Cu\text{-}Cr\text{-}SiO_2/Si^*$	203	atomosphere	70
6	$Cr\text{-}Cu\text{-}Cr\text{-}SiO_2/Si^*$	600	UHV	10 (minutes)

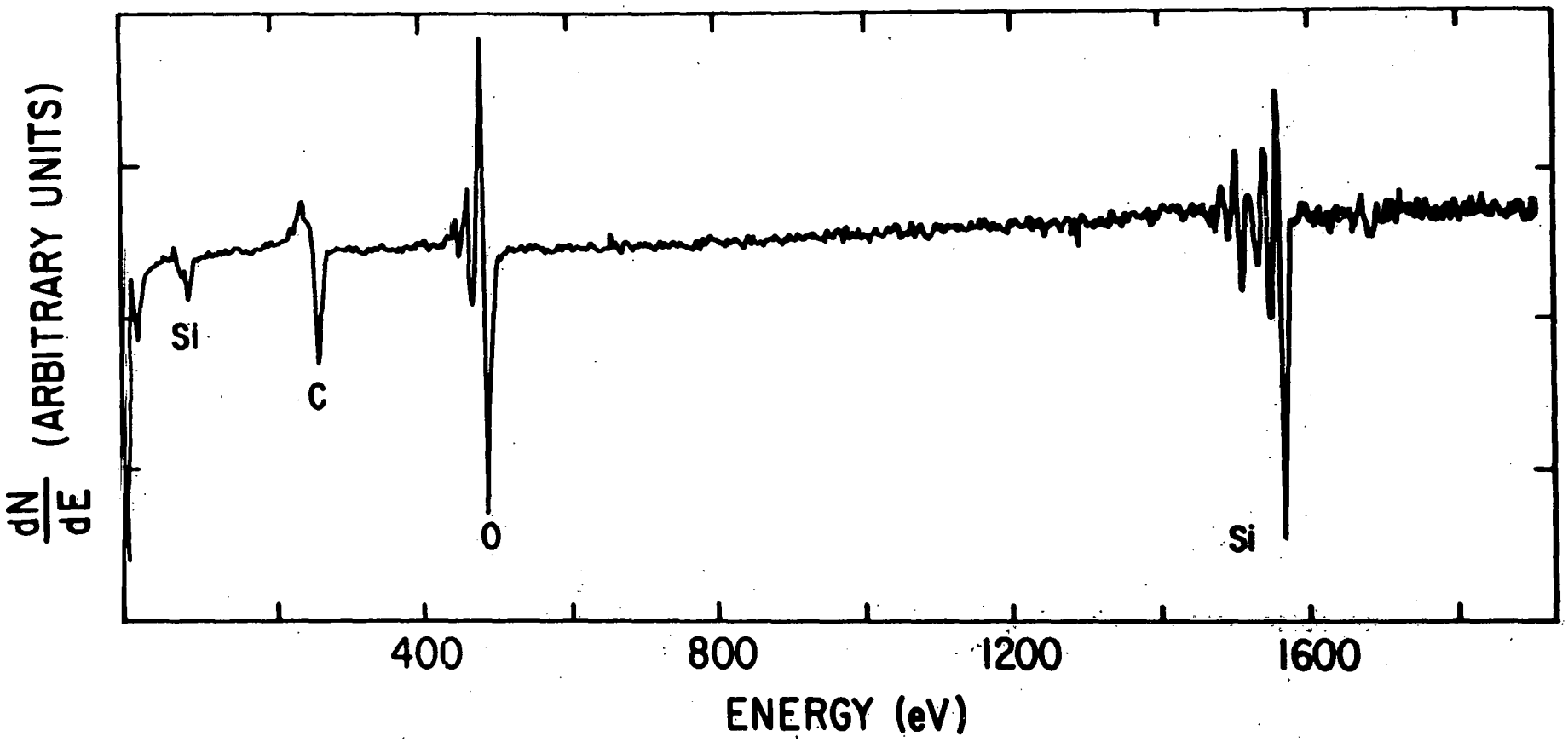
* Polycrystalline Silicon

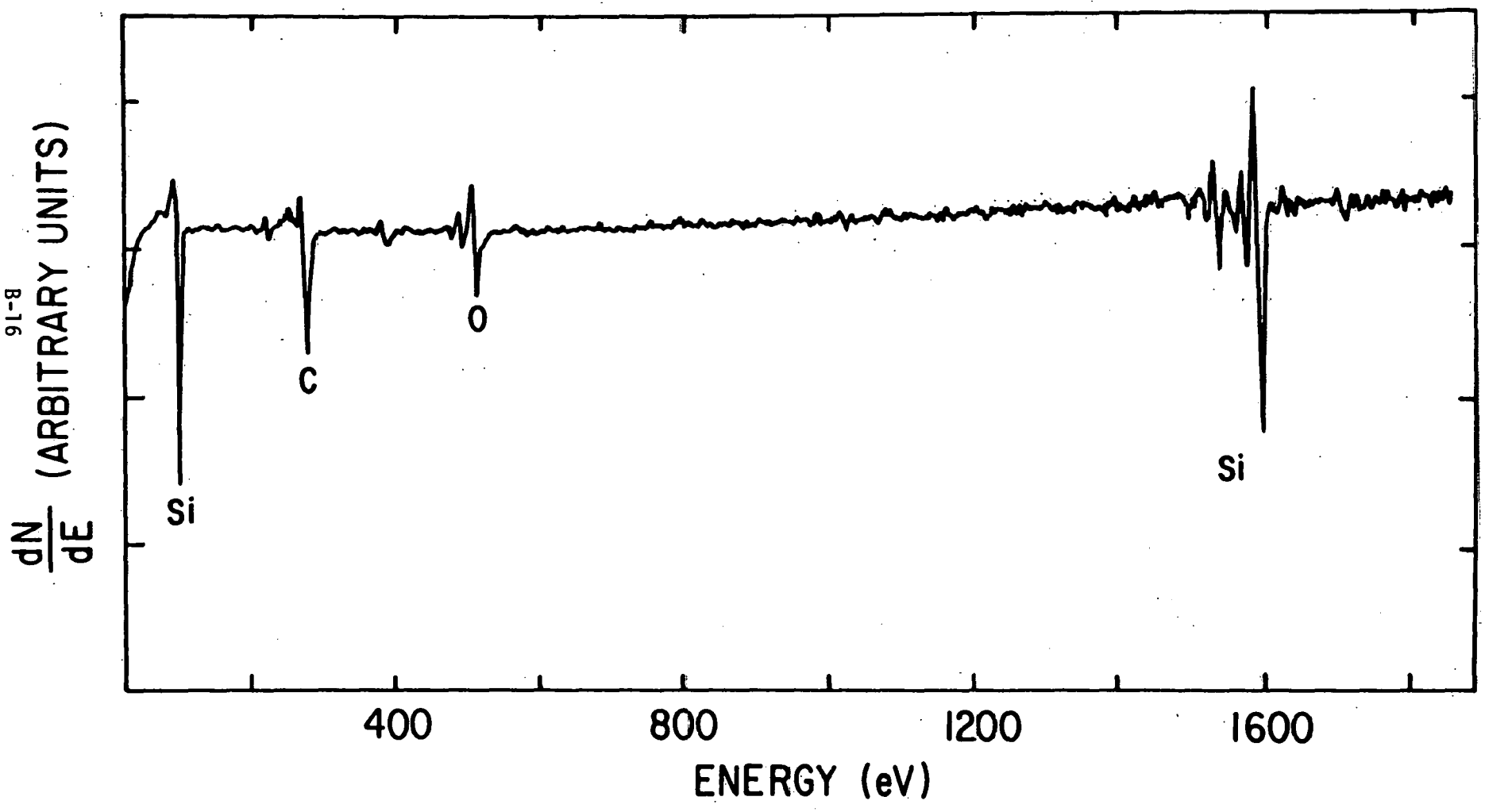
TABLE 1

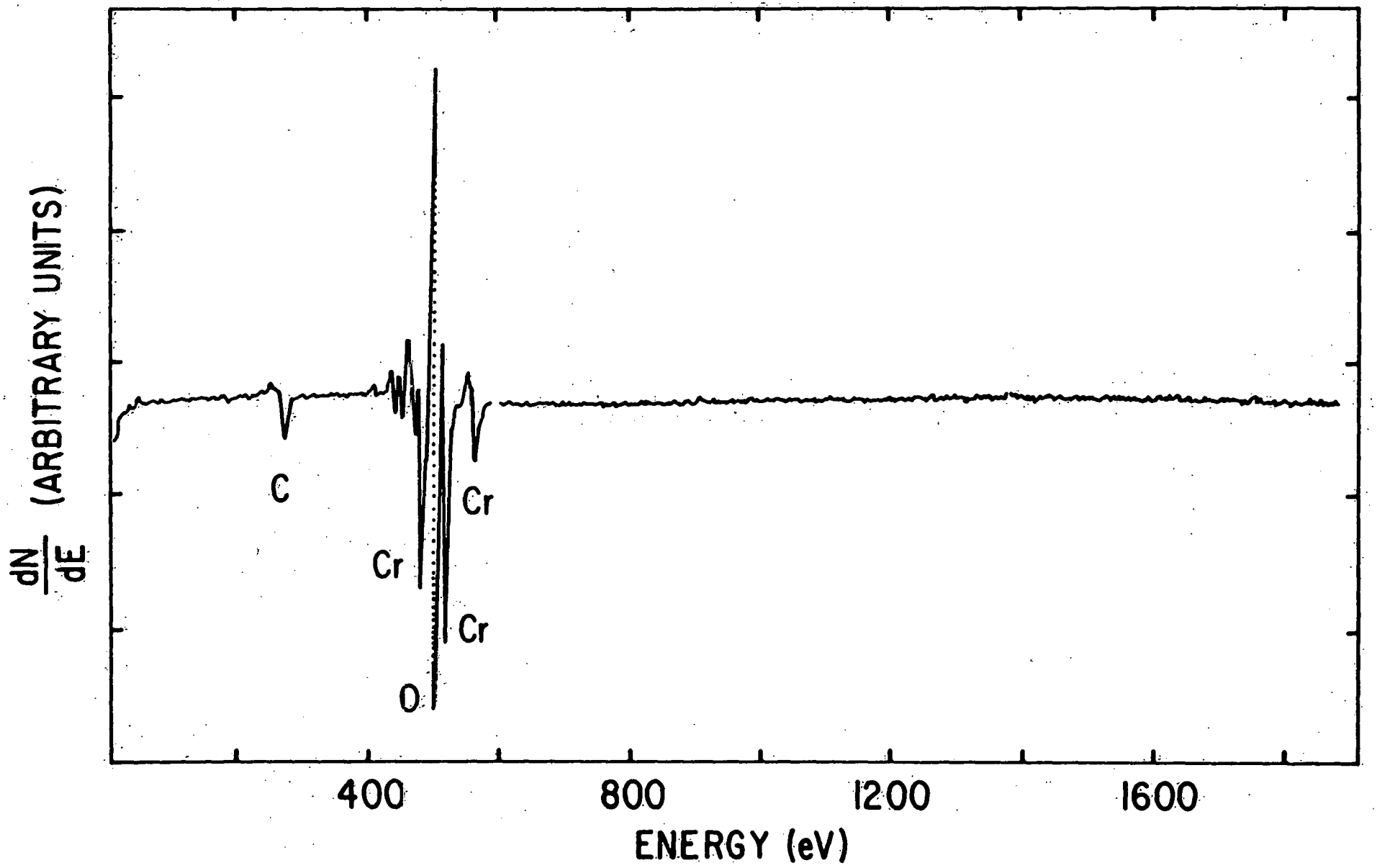
Six samples were analyzed. Four of them were heat-treated at different temperatures and environments as listed in the table.

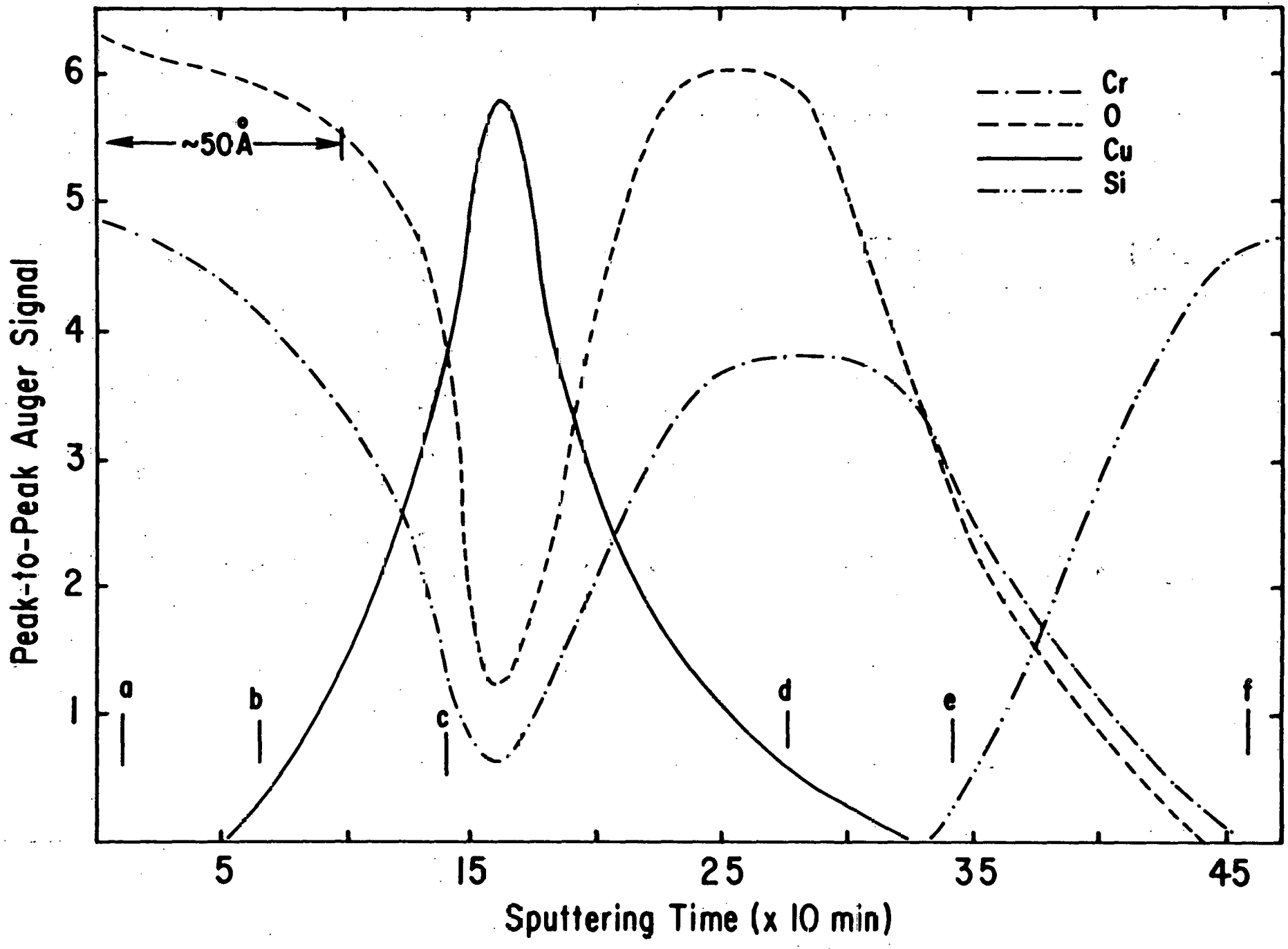

Cr
Cu
Cr
SiO2
Si
50 Å
50 Å
50 Å
~20 Å

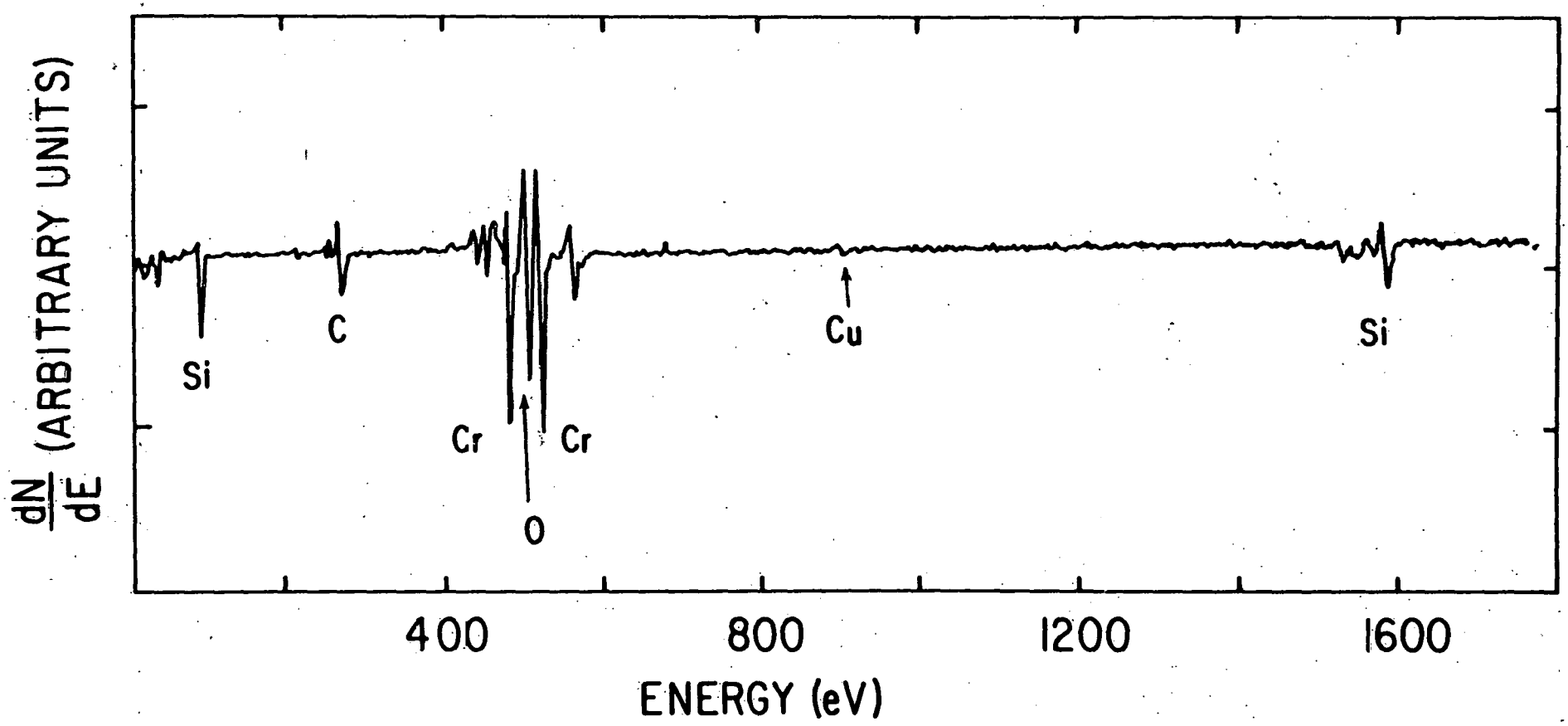

Mass
Spectrometer
Ion
Gun
Window for
Ellipsometer
MAIN CHAMBER
Sample
View
Port
LEED
Optic
Window for
Ellipsometer
Auger
Analyzer

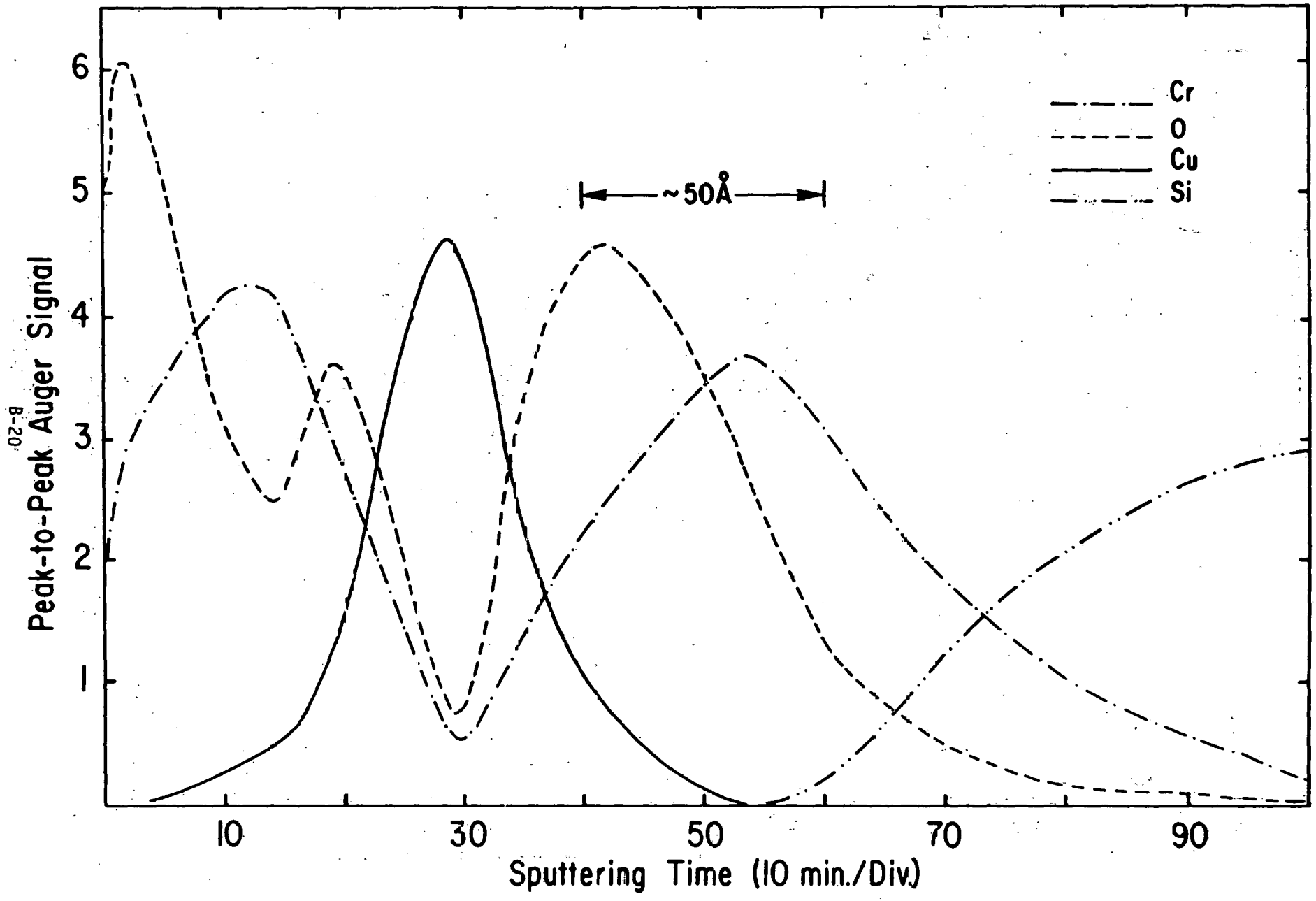

dN/dE (ARBITRARY UNITS)
Si
C
O
Si
400
800
1200
1600
ENERGY (eV)

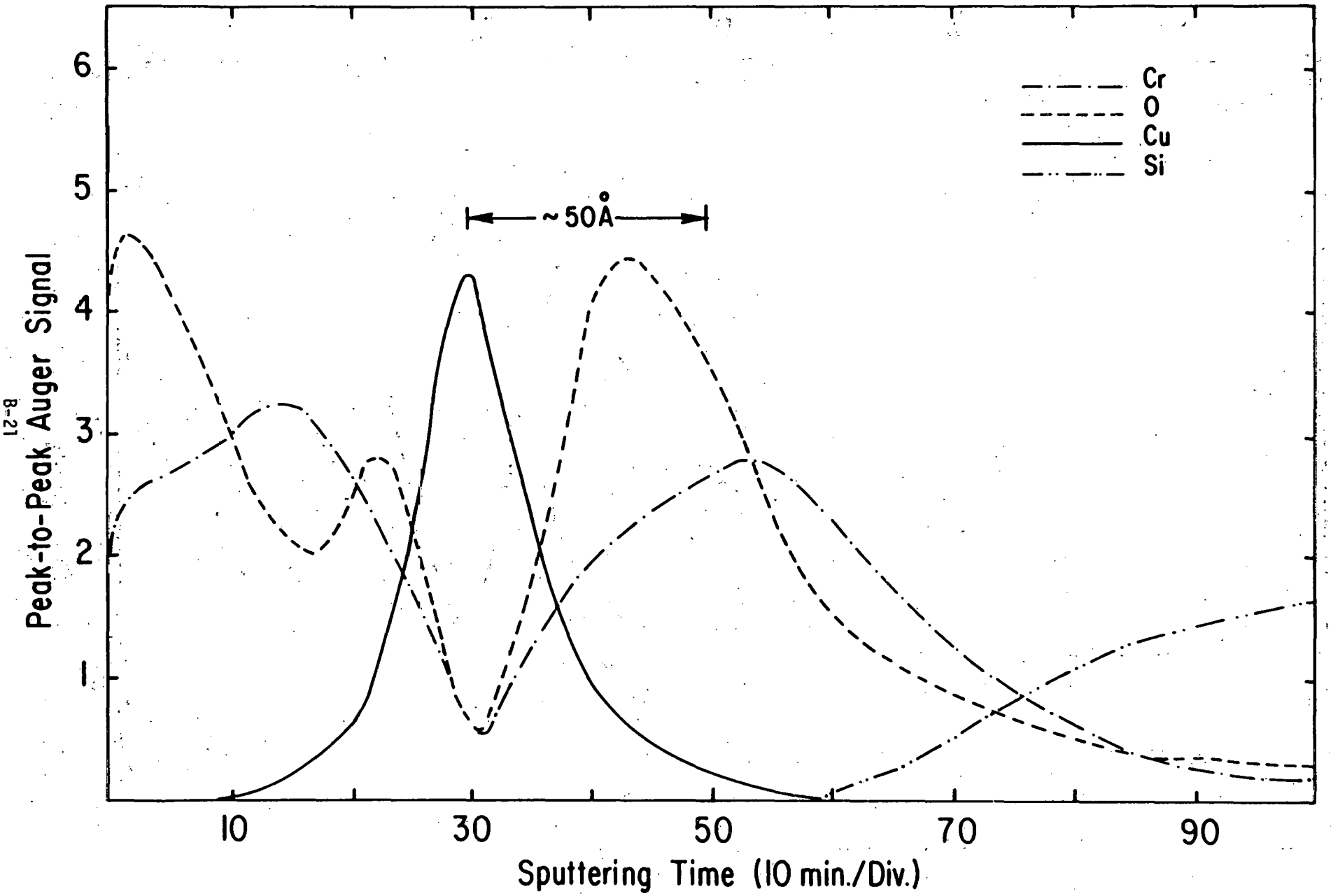

dN/dE (ARBITRARY UNITS)
Si
C
O
Si
400
800
1200
1600
ENERGY (eV)

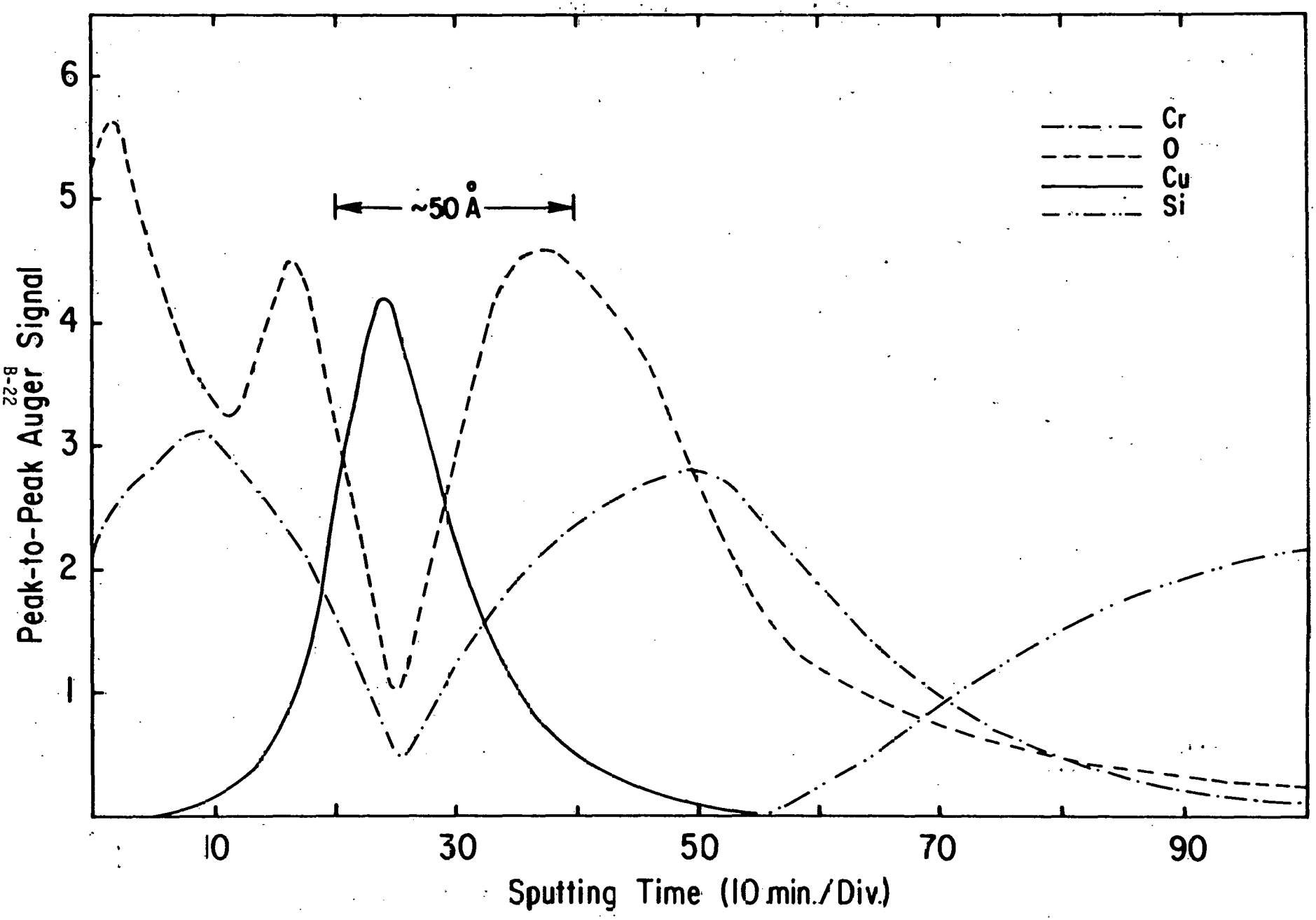

dN/dE (ARBITRARY UNITS)
C
Cr
Cr
Cr
O
400
800
1200
1600
ENERGY (eV)


Cr
O
Cu
Si
~50Å
a
b
c
d
e
f
Peak-to-Peak Auger Signal
Sputtering Time (x 10 min)
1
2
3
4
5
6
5
15
25
35
45


dN/dE (ARBITRARY UNITS)
Si
C
Cr
O
Cr
Cu
Si
400
800
1200
1600
ENERGY (eV)


Cr
O
Cu
Si
~50Å
Peak-to-Peak Auger Signal
1
2
3
4
5
6
10
30
50
70
90
Sputtering Time (10 min./Div.)


Cr
O
Cu
Si
~50Å
Peak-to-Peak Auger Signal
1
2
3
4
5
6
10
30
50
70
90
Sputtering Time (10 min./Div.)


Cr
O
Cu
Si
~50 Å
Peak-to-Peak Auger Signal
1
2
3
4
5
6
10
30
50
70
90
Sputting Time (10 min./Div.)