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CRYSTALLIZATION OF SILICON FILMS ON GLASS: A COMPARISON OF METHODS*

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ABSTRACT

The lure of flat panel displays has stimulated much research on the crystallization of silicon films deposited on large-area transparent substrates. In most respects, fused quartz is ideal. It has high purity, thermal shock resistance, and a softening point above the silicon melting temperature. Unfortunately, fused quartz has such a small thermal expansion that the silicon film cracks as it cools. This problem has been attacked by patterning with islands or moats before and after crystallization, by capping, and by using silicate glass substrates that match the thermal expansion of silicon. The relative merits of these methods are compared. Melting of the silicon film to achieve high mobility has been accomplished by a variety of methods including lasers, electron beams, and strip heaters. For low melting temperature glasses, surface heating with a laser or electron beam is essential. Larger grains are obtained with the high bias temperature, strip heater techniques. The low-angle grain boundaries characteristic of these films may be caused by constitutional undercooling. A model is developed to predict the boundary spacing as a function of scan rate and temperature gradient.

INTRODUCTION

Two primary applications for crystallized silicon on amorphous substrates are dielectrically isolated devices and matrix displays. For dielectric isolation, most of the work has been done on thermally oxidized silicon wafers. This substrate is fully compatible with integrated circuit processing and eliminates thermal expansion problems. However, for the display application, silicon wafers are too small, too opaque, and too expensive. For a display medium such as a liquid crystal twist cell, a large area, transparent, inexpensive substrate is needed. Transistors fabricated on this substrate could provide threshold switching for each display element and decoding, multiplexing, and line driver circuitry.

Thin film transistors have been studied for over 20 years. Various semiconductors, such as CdS,[1] CdSe,[2] amorphous hydrogenated silicon,[3-6] and polycrystalline silicon,[7-9] have been investigated. For display element switching, the mobility of these materials is adequate, but for peripheral circuitry, much higher mobility is needed. The necessary mobility can be obtained by melting a

*Research performed by the authors was done at Bell Laboratories, Holmdel, N.J.

deposited silicon film to produce large crystal grains. With this material, both switching and control circuitry potentially could be fabricated on a single substrate.

The work on this problem has concentrated on transparent fused quartz substrates. In most respects, fused quartz is ideal. It is available with high purity and in arbitrarily large areas. It can be heated to the silicon melting point without deformation, and it is resistant to thermal shock. Unfortunately, the thermal expansion coefficient of fused quartz ($\alpha \sim 0.5 \times 10^{-6}/^{o}C$) is small compared to that of silicon ($\alpha \sim 3.5 \times 10^{-6}/^{o}C$). As the silicon cools from the melt, its contraction relative to the fused quartz can produce severe crazing of the film. This problem is illustrated in Fig. 1. A 1.0-μm-thick silicon film was chemically vapor deposited on a 0.5-mm-thick fused quartz plate. A 2-W argon ion laser beam focused to a ~250-μm-diam spot was scanned across the film. This produced a pool of molten silicon (Fig. 1A) that solidified at the trailing edge with single crystals up to 200 μm x 20 μm in size. A network of cracks (Fig. 1B) typically appears a few seconds after the film solidifies.

Recently, various radiant energy sources have been substituted for the laser. Geis et al. demonstrated uniform melting with a resistively heated graphite strip in close proximity to the silicon film.[10] Similar results are obtained by focusing radiation from a tungsten filament[11,12] or an arc lamp[13] on the film. This increases the working distance and reduces potential contamination. To achieve a narrow melt zone across the full width of the substrate, the sample must be heated to 1000-1300°C. In the graphite strip heater case, this bias temperature is provided by placing the sample directly on a resistively heated graphite plate. Other systems use a bank of incandescent lamps.[12] The distinguishing features of the zone melting techniques are 1) high bias temperature, 2) slow scan speed (0.1-1.0 mm/s), and 3) much wider melt perpendicular to the scan than along it.

To prevent the molten silicon from agglomerating, the film is encapsulated with SiO_2 (Fig. 2A). By making the encapsulation 1-2 μm thick, the surface remains flat, and the resulting crystal texture is uniform.[10] Films crystallized by this method typically have very large grains (10 mm x 1 mm) with (100) crystal planes parallel to the substrate. As shown in Fig. 2B, a characteristic feature of silicon films that have been microzone melted at high bias temperature is a network of low-angle grain boundaries.[14] These

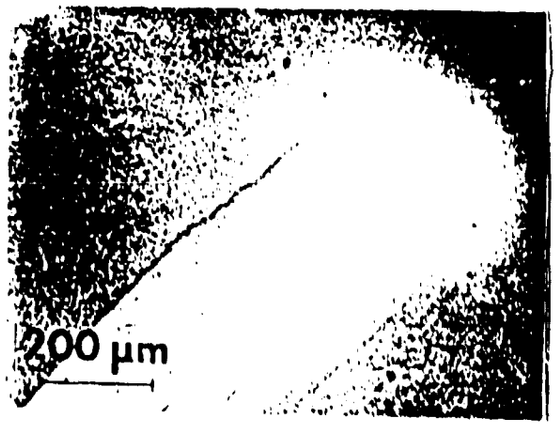

Fig. 1A. Reflection micrograph of a Si film on fused quartz during laser melting, showing large grains trailing the high reflectivity molten pool.

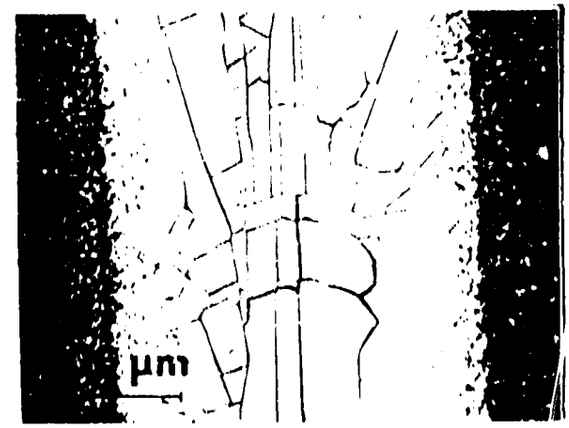

Fig. 1B. Reflection micrograph of the crack network that forms shortly after cooling.

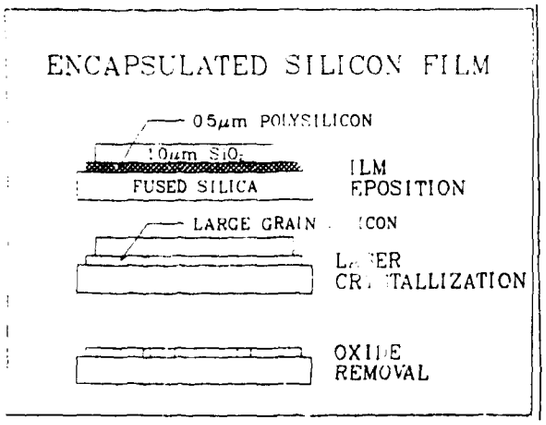

Fig. 2A. Schematic showing temporary crack suppression with an encapsulating film.

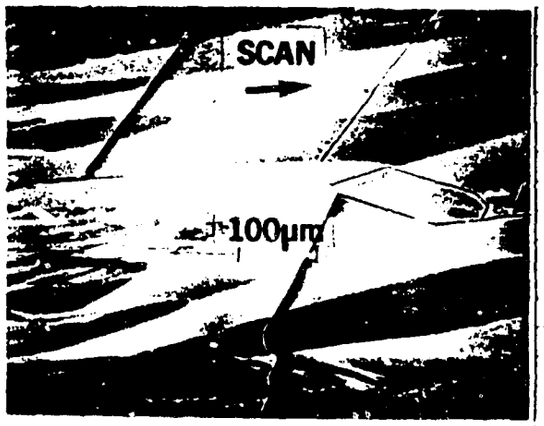

Fig. 2B. Electron channeling micrograph of a strip heater melted Si film on fused quartz. Cracks form when the encapsulation is removed.

boundaries separate crystallites with a 1-2° difference in the [100] direction out of the plane. A model to predict the spacing of these boundaries is developed in the last section.

The uniformity of crystal orientation in these films substantially improves electron mobility. Indeed, on fused quartz substrates where the film is under tensile stress, mobilities better than in bulk silicon have been measured.[15] Unfortunately, this tensile stress also produces cracks (Fig. 2B). These cracks are less dense than in laser melted films, but they still make circuit fabrication impractical.

CRACK SUPPRESSION TECHNIQUES

An encapsulating SiO_2 film >100 nm thick suppresses crack formation. However, when the SiO_2 is completely removed, a network of cracks inevitably forms during subsequent processing. Much better performance is obtained by only removing the SiO_2 cap from the small islands where devices are to be built. As shown in Fig. 3, this substantially reduces the number of cracks.

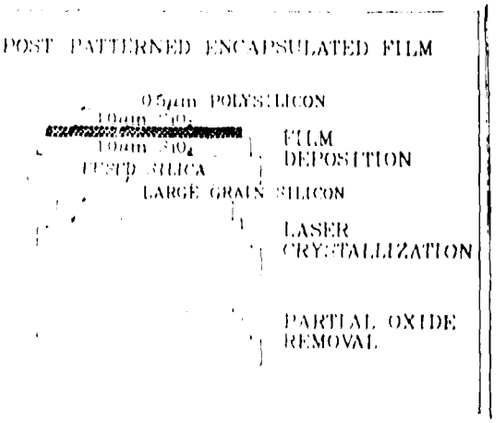

Fig. 3A. Schematic showing partial cap removal to suppress cracks.

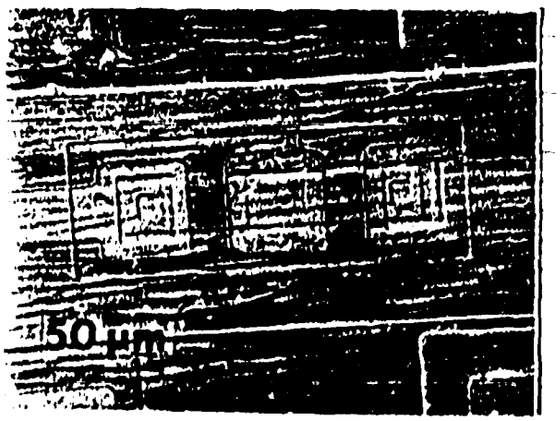

Fig. 3B. PMOS transistor fabricated in a crack-free region.

A large fraction of the devices are functional.[16] This film was melted with a ∿30 μm x ∿1 cm cylindrically focused argon ion laser beam in combination with an 1100°C bias temperature. This hybrid technique allows large-area zone melting with steeper temperature gradients than a strip heater provides, thus giving better melt stability and more closely spaced low-angle grain boundaries, as discussed in the last section.[17]

An alternative method is to define islands in the crystallized silicon before removing the SiO_2 cap. The idea is that sufficiently small islands can withstand the stress without cracking. There are two variations to this approach. In the first, a photoresist layer is patterned into islands and then baked to protect the underlying SiO_2. The exposed SiO_2 is removed with a HF solution. The underlying Si and the photoresist are then removed with a KOH solution. Finally, the SiO_2 over the islands is removed. Unfortunately cracks that form between the encapsulated islands often penetrate far enough under the cap to nucleate cracks within the islands when the overlying cap is removed.

In a variation of this technique, moats are patterned in the photoresist to define islands. Both the SiO_2 and the Si are sequentially removed from the moats before the SiO_2 over the rest of the area is removed. These steps are shown schematically in Fig. 4A. The idea is that cracks are suppressed by the SiO_2 while the moats are fabricated. The moats would then prevent cracks from propagating into the islands when the SiO_2 is removed. As shown in Fig. 4B, surface cracks in the fused quartz often allow cracks to cross the moats into the islands.

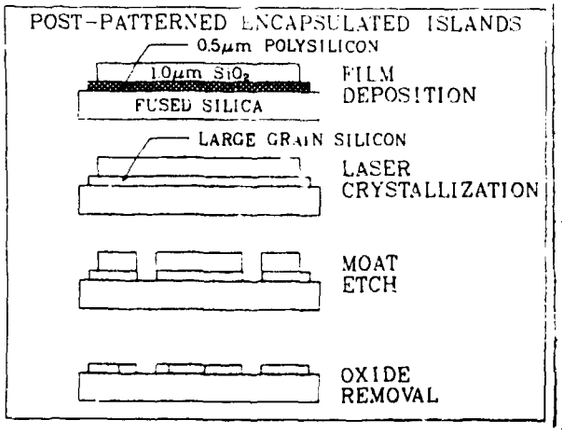

Fig. 4A. Schematic showing patterning with moated islands after crystallization.

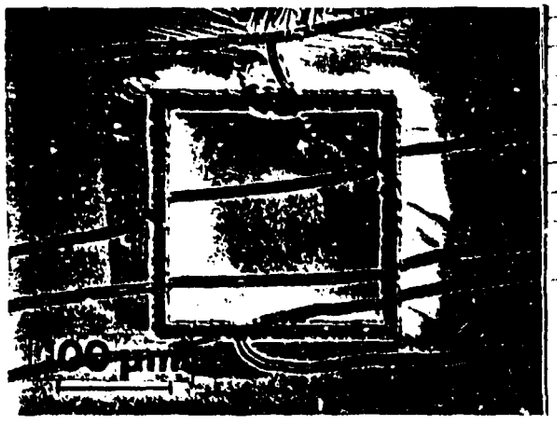

Fig. 4B. Unsuccessful island in which cracks propagate through the fused quartz.

A better solution is to pattern the silicon film prior to crystallization, as shown schematically in Fig. 5A. This technique was used by Kamins and Pianetta in their early work on silicon crystallization on fused quartz.[18] The idea is to define islands small enough to withstand the stress. Isolated islands, however, have two problems. The first is mass transport. When silicon melts, the volume is reduced ∿12%, which causes the silicon island to pull away from its original boundary, often leaving voids along the edge. Conversely, when the silicon solidifies, it expands ∿12% to form a sharp pinnacle with the last material to freeze. The remedy for this problem is to pattern the silicon into long, narrow strips, rather than islands. The molten zone is then passed along the length of the strip. In this way, the contraction and expansion problems are relegated to the ends, and the center is uniform and flat (Fig. 5B). The second problem is edge cooling. If the silicon is melted with radiation that is weakly absorbed in the surrounding fused quartz, the

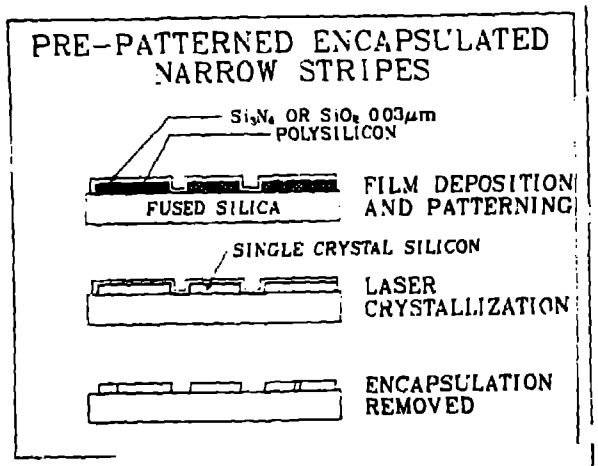

Fig. 5A. Schematic showing patterning into moated islands prior to crystallization.

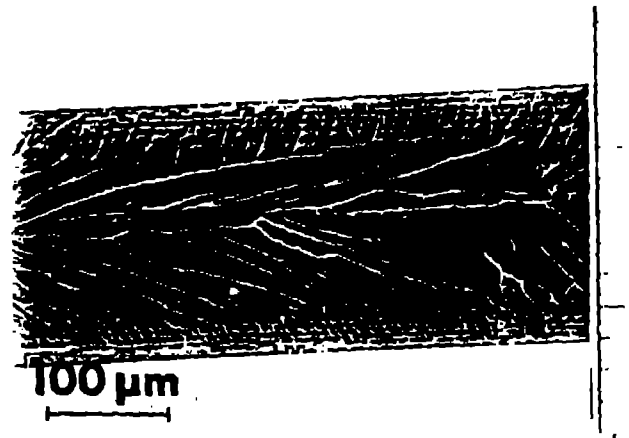

Fig. 5B. Micrograph of a crack-free, pre-patterned strip showing nucleation due to edge cooling.

edges of the strips remain cooler than the center. This causes crystals of random orientation to nucleate along the edge (Fig. 5B), resulting in reduced device performance.

The edge cooling can be remedied by depositing additional absorbing films, such as polysilicon, either above or below the isolated strips.[19] A simpler approach is to define the strips with a narrow moat.[18,19] In this way, radiation absorbed in the surrounding polysilicon suppresses edge cooling. One problem with the moat technique is that cracks can propagate through the surface of the fused quartz. The polysilicon surrounding the moats should also be patterned to reduce cracks.

Another solution to the edge cooling problem is to shape the laser beam to preferentially heat the edges.[19] Various masking and interference techniques have been used for this purpose. Another elegant approach is to melt the silicon with radiation that is absorbed more strongly in the fused quartz than in the silicon. This is easily done with the $\lambda = 10.6$ μm line of a CO_2 laser and naturally provides the desired temperature profile.[20] With a hotter edge, a crystal nucleus forming in the center can spread to make a single crystal-island.

Long, narrow strips with internal moats and CO_2 laser heating have been combined very successfully at the Xerox Research Center.[21] As shown schematically in Fig. 5A, the central moated region usually solidifies as a single crystal, typically 100 μm x 25 μm. When the encapsulation is removed, the outer silicon may crack but the inner islands are substantially free of cracks.

THERMAL EXPANSION MATCHED SUBSTRATES

To varying degrees the patterning techniques described above reduce the cracking problem but do not eliminate it. The obvious alternative is to select a substrate whose thermal expansion closely matches that of silicon. In itself, this is not difficult. A number of silicate glass compositions meet this criterion. They have good transparency and surface finish, and they are substantially cheaper than fused quartz. What they lack is the purity, thermal shock resistance, and high softening temperature of fused quartz.

We have tested three types of silicate glass: Corning 1723, an alumina-silicate glass; Corning 7059, a low soda barium-borosilicate glass; and Corning 7740, a borosilicate glass better known as Pyrex.[22] These three types were selected for high annealing point (710°C, 639°C, and 560°C, respectively), resistance to thermal shock, and low alkali metal content.

The annealing point is defined as the temperature at which the glass viscosity is 4×10^{13} poise. Above this temperature, nonuniform stress can easily distort the plate. Empirically, we found that if these glasses were supported on a flat substrate they could be heated to 620°C for up to 1 hour. This is the temperature used for silicon deposition by pyrolytic decomposition of SiH_4.

The low softening temperature of the silicate glasses requires the silicon to be melted by surface heating. This is easily done with a focused argon ion laser beam. As shown in Fig. 6, the resulting crystal structure is comparable to that obtained on fused quartz. The zone melting techniques can not be used with silicate substrates because the high bias temperature would melt the glass.

The thermal expansion of these glasses is plotted in Fig. 7 as a function of temperature for comparison with the expansion of silicon and fused quartz. These glasses follow the thermal expansion of silicon up to ~600°C, but they expand substantially more than silicon at higher temperatures. This applies a tensile stress to the silicon during heating that is relieved when the silicon melts. As the silicon cools from the melt, it is under a compression that effectively suppresses cracking.

The key problem with the silicate glass substrate is that impurities in the glass can diffuse into the silicon, ruining the electronic characteristics. As shown in Fig. 8, alkali metals are a particular problem. This sample of type 7740 glass was coated with 1.0 μm of SiO_2 before the 1.0-μm Si layer was deposited. The secondary ion mass spectroscopy depth profile shows that sodium from the glass diffused through the silicon before the deposition was complete. The boron in the glass was effectively blocked by the SiO_2 layer even after laser melting.

To isolate the glass impurities from the silicon, composite buffer layers are required. Our best results were obtained on type 7059 glass using a 1.0-μm layer of SiO_2 for adherence, a 200-nm layer of Si_3N_4 to block alkali metal diffusion, and a second 1.0-μm SiO_2 layer to provide a better electrical interface for the 1.0-μm Si layer.

As yet, devices have not been fabricated in these films. Novel processing techniques must replace the high-temperature steps in conventional integrated circuit processing. In particular, the gate oxide, which is usually grown at 1150°C, must now be grown at 650°C or below. Two possibilities are plasma oxidation and high-pressure oxidation. The risk of contaminating existing silicon processing facilities with impurities from the glass has also precluded device fabrication.

LOW-ANGLE GRAIN BOUNDARY FORMATION

As mentioned in the introduction, a prominent feature of silicon films that have been microzone melted at high bias temperature is a network of low-angle grain boundaries. These boundaries have a characteristic wishbone shape and separate crystallites with a 1-2° difference in orientation. The origin of these low-angle grain boundaries is an instability of the melt front, which leads to faceting. The low-angle boundaries form where adjacent facets meet at the trailing edge of the melt.

These facets have been studied both by rapid quenching of the melt[23] and by direct microscopic observation of the melt front[24] as shown in Fig. 9C. Both techniques show that the facets are most commonly bounded by (111) crystal planes, which are the usual limiting planes for silicon crystal growth.

Melt front instability and faceting are commonly produced in bulk crystal growth by constitutional undercooling.[25,26] In this section, we develop a constitutional undercooling model for the melt front instability in microzone crystallization of thin silicon films.

Fig. 6. Electron channeling micrograph of large grains produced by laser melting a Si film deposited on a silicate glass substrate with a SiO_2 buffer layer.

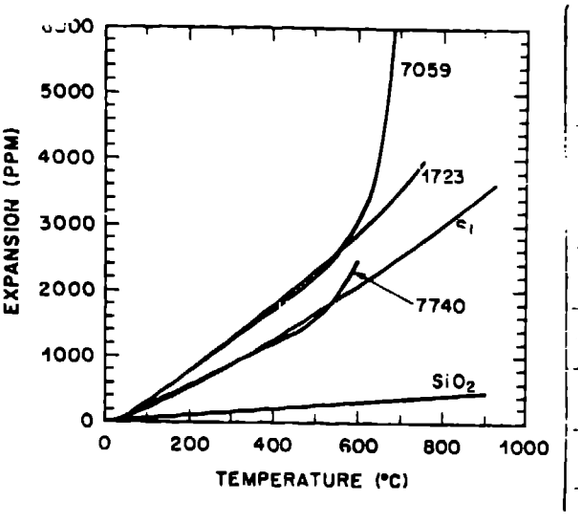

Fig. 7. Comparison of the thermal expansion of Si, fused quartz, and glass types 1723, 7059, and 7740 as a function of temperature.

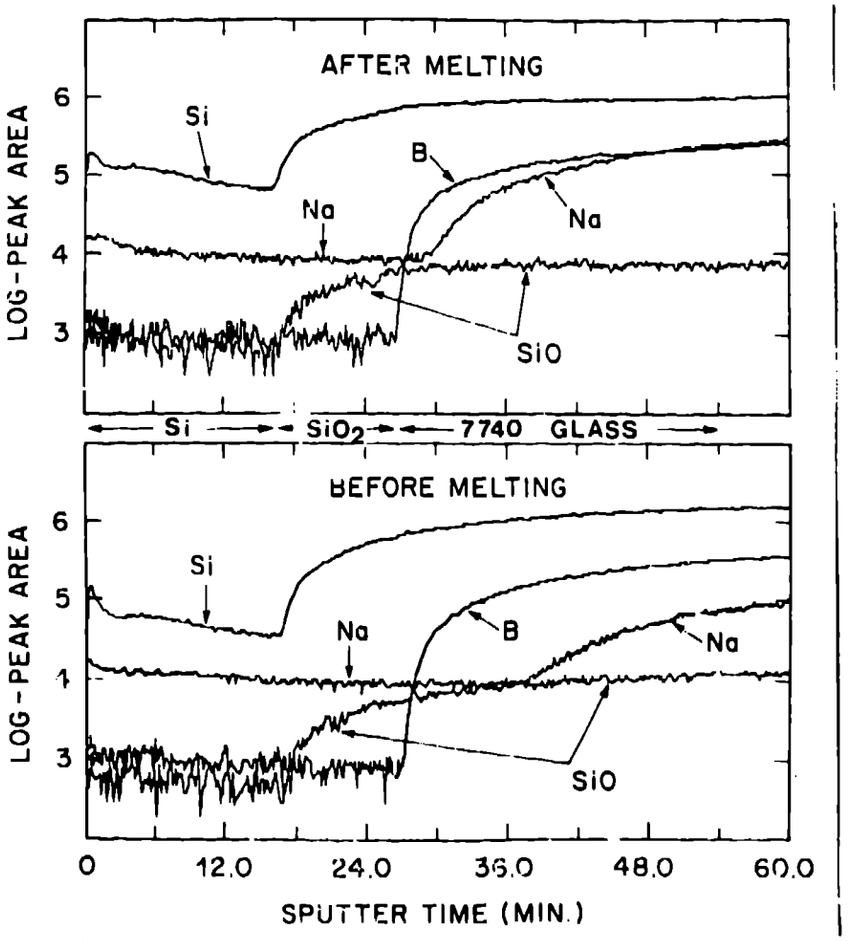

Fig. 8. Secondary ion mass spectroscopy analysis of the composition in depth of a 1.0-μm Si film deposited on a type 7740 glass substrate with a 1.0-μm SiO_2 buffer layer. The composition after melting (top) is compared with the same sample before melting (bottom).

To explore the effects of constitutional undercooling, consider the hypothetical phase diagram (Fig. 9A). This phase diagram has a character similar to the published silicon-oxygen binary system[27] but has been simplified for illustration. For very low impurity concentration, we assume that both the liquidus and solidus are straight lines and that the segregation coefficient is k = 0.1, as shown in Fig. 9B. Thus, if the impurity concentration in the solid is $C_o = 1 \times 10^{18}/cm^3$, the impurity concentration in the adjacent liquid is $C_o/k = 1 \times 10^{19}/cm^3$. As the melt zone is scanned, impurity atoms are rejected from the solid, building up a concentration gradient in the liquid ahead of the interface, as shown in Fig. 9D. In the simple diffusion model,[28] this concentration gradient is given by the expression:

$$C(x) = C_o \left[1 + \frac{(1 - k)}{k} \exp\left(-\frac{R}{D} x\right)\right] \quad (1)$$

where R is the scan rate and D is the diffusion coefficient of the impurity in the liquid. When the concentration gradient is referred to the phase diagram, it implies that the freezing temperature of the liquid (T_L) also has a spatial dependence given by

$$T_L(x) = T_o - mC_o \left[1 + \frac{(1 - k)}{k} \exp\left(-\frac{R}{D} x\right)\right] \quad (2)$$

where T_o is the freezing temperature of pure silicon and m is the slope of the liquidus. This curve is plotted in Fig. 9E using convenient parameters.

In the simple theory of constitutional undercooling, a linear temperature gradient of slope G imposed on the melt is assumed. If

$$G < \frac{mC_o R}{D} \quad \frac{(1 - k)}{k} \quad (3)$$

there is a region (Fig. 9E) where the actual temperature is below the equilibrium freezing temperature. This region is constitutionally undercooled. Therefore, a perturbation of the interface that enters this region will tend to grow.

Let us assume that the projection grows until it no longer has undercooled liquid ahead of it. The projection length would be the distance from the average interface to the intercept of the temperature curve and the equilibrium freezing temperature curve, as marked with the dashed line in Fig. 9E.

If the projection is constrained by (111) growth facets, it will have the characteristic triangular shape. Thus, the spacing of adjacent low-angle boundaries will be comparable to the length of the undercooled region (Fig. 9F). This allows us to calculate the dependence of grain boundary spacing on both temperature gradient and scan speed. These relations are most easily expressed as a function of the length of the undercooled region, x_o.

We obtain

$$G = \frac{mC_o}{x_o} \frac{(1 - k)}{k} \left[1 - \exp\left(-\frac{R}{D} x_o\right)\right] \quad (4)$$

which is plotted as $x_o(G)$ in Fig. 10, and

$$R = -D/x_o \cdot \ln\left[1 - \left[k/(1 - k) \cdot Gx_o/mC_o\right]\right] \quad (5)$$

which is plotted as $x_o(R)$ in Fig. 11. These curves indicate that the undercooled region and the boundary separation will go to zero for a sufficiently high temperature gradient or for a sufficiently slow scan speed.

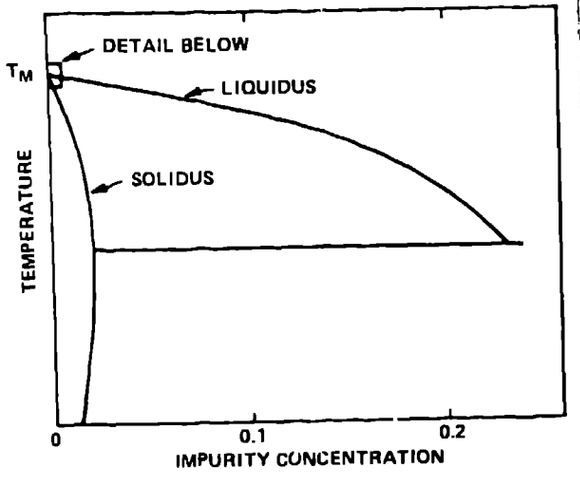

Fig. 9A. Hypothetical phase diagram for impure Si.

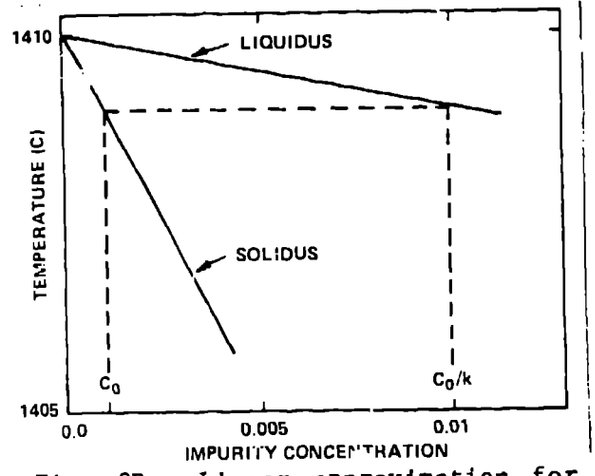

Fig. 9B. Linear approximation for the phase diagram at low-impurity concentrations.

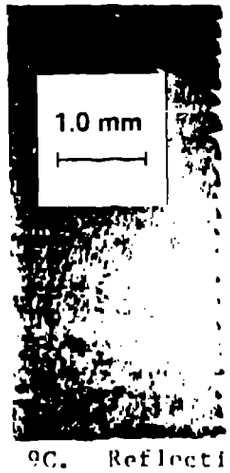

Fig. 9C. Reflection micrograph of melt front faceting during strip heater crystallization.

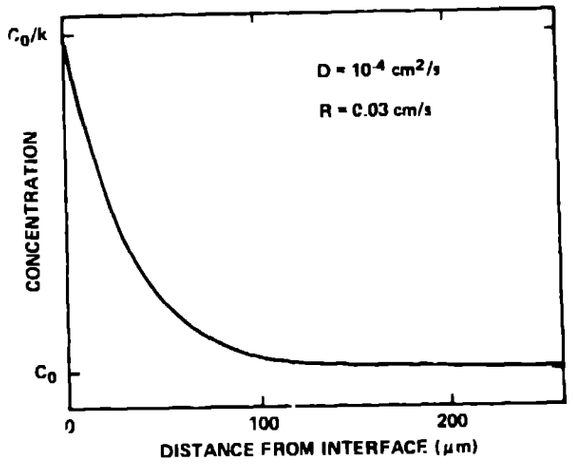

Fig. 9D. Impurity concentration profile in the liquid.

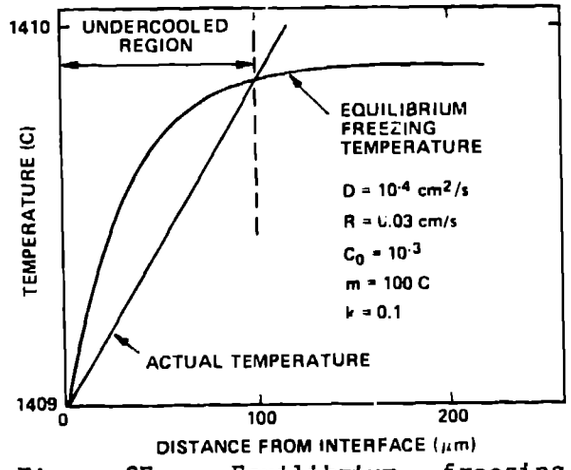

Fig. 9E. Equilibrium freezing temperature profile and the imposed temperature gradient produce a constitutionally undercooled region.

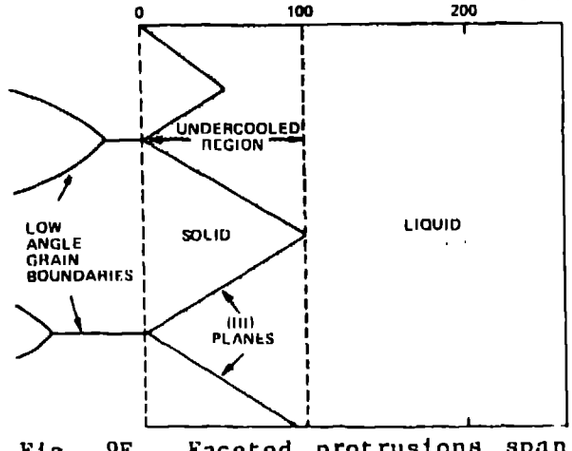

Fig. 9F. Faceted protrusions span the undercooled region and form low-angle grain boundaries where they meet.

The general character of these curves corresponds with observation. Increasing the temperature gradient reduces the boundary separation. For example, the boundaries in Fig. 2B that have a 50-100-μm spacing were produced with a 1-mm-wide graphite strip. Whereas the 5-10-μm spacing in Fig. 3B were produced with a ∿30-μm-wide laser beam that provides a much steeper temperature gradient. As yet, we have not been able to obtain a sufficiently steep gradient to eliminate the boundaries.

It has also been observed that the boundary spacing is reduced by lowering the scan speed. Geis has reported a $x_o \propto R^{1/2}$ dependence,[23] which does not show the sharp knee of Fig. 11. Our measurements show a small increase in spacing with scan speed, in keeping with the flat portion of Fig. 11, but we have not observed the abrupt decrease in spacing at slow speeds.

This simple model does not take into account lateral impurity segregation. In a metal that does not facet, lateral segregation causes an increase in boundary separation as the scan speed is reduced because there is more time for the impurity to diffuse.[28] However, in a material such as silicon where the facets are bounded by (111) planes, the separation of adjacent projections is constrained. This should reduce the effect of lateral segregation. Nevertheless, lateral segregation may make the change in boundary spacing with scan speed less abrupt.

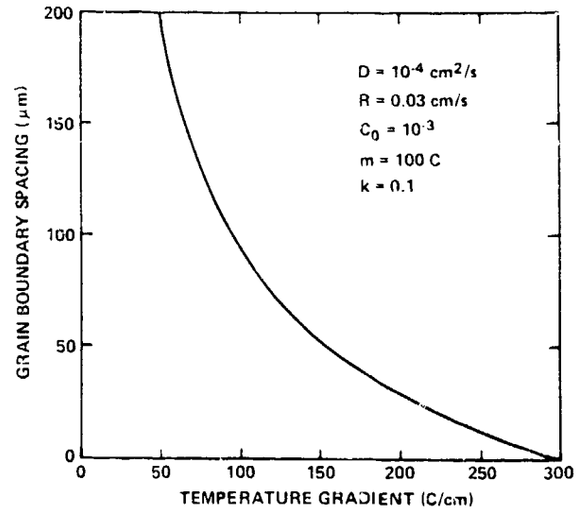

Fig. 10. Predicted grain boundary spacing as a function of the thermal gradient.

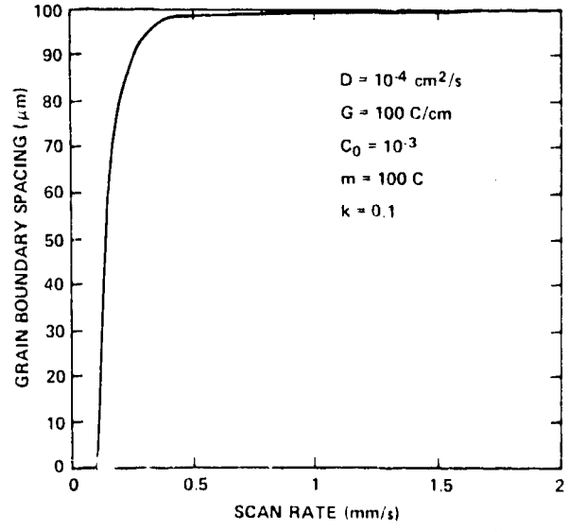

Fig. 11. Predicted grain boundary spacing as a function of scan rate.

In considering which impurities might cause constitutional undercooling, oxygen and nitrogen are potential candidates. These elements are commonly found in the substrate or capping layer or in the atmosphere in which the melting is performed. Distinguishing such impurities from the capping layer may be difficult because they may segregate to the surface. In addition, only small concentrations may be needed. The examples used a concentration of $C_o = 10^{-3}$. However, as seen in Eqs. (4) and (5), the key factor is k/mC_o. If k were smaller or m were larger, a much smaller concentration would produce the same result.

CONCLUSION

The crystallization of silicon films on fused quartz is an attractive technology for control circuitry on flat panel matrix displays. Thermal stress cracking, however, remains a problem. Although patterning techniques have substantially suppressed cracking, the device yields needed for displays require further improvement.

Silicate glass substrates exchange the thermal stress problem for contamination and processing problems. The development of an expansion matched, pure, high melting temperature substrate could make an important impact on this field.

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