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Ultra-Low Power Microwave CHFET Integrated Circuit Development

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ULTRA-LOW POWER MICROWAVE CHFET INTEGRATED CIRCUIT DEVELOPMENT

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Abstract

This report summarizes work on the development of ultra-low power microwave CHFET integrated circuit development. Power consumption of microwave circuits has been reduced by factors of 50-1000 over commercially available circuits. Positive threshold field effect transistors (nJFETs and PHEMTs) have been used to design and fabricate microwave circuits with power levels of 1 milliwatt or less. 0.7 μm gate nJFETs are suitable for both digital CHFET integrated circuits as well as low power microwave circuits. Both hybrid amplifiers and MMICs were demonstrated at the 1 mW level at 2.4 GHz. Advanced devices were also developed and characterized for even lower power levels. Amplifiers with 0.3 μm JFETs were simulated with 8-10 dB gain down to power levels of 250 microwatts (μW). However 0.25 μm PHEMTs proved superior to the JFETs with amplifier gain of 8 dB at 217 MHz and 50 μW power levels but they are not integrable with the digital CHFET technology.

Acknowledgment

The authors are indebted for the technical processing assistance of Geraldine Lopez, Melissa Cavaliere, and Andrea Ongstad as well as Charlie Sandoval and Florante Cajas for device characterization and circuit testing. Thanks also goes to Mike Lovejoy, Gary Patrizi, and Dennis Rieger who did much of the development of the thin film capacitors and airbridge inductors. The authors are also indebted to former Sandians Marc Sherwin and John Zolper, who played an important role in developing this technology.

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I. Introduction

Portable communications is the driver for many low power electronic applications. Impressive performance improvements in digital integrated circuits without increases in power consumption has been the norm. However, no good solutions have been available for reducing the level of power consumption for microwave circuits. The commercial world largely operates on the basis of frequently changed or recharged batteries. Many defense applications could benefit from eliminating the battery change or recharge requirement. Examples of these would include miniature tagging and monitoring devices. Furthermore, many defense applications do not operate on the same cost model as high volume commercial applications. Technologies that are cost prohibitive for commercial applications will not generally get developed for low volume, special needs defense applications. The goal of this work has been to develop new technology for drastically reducing power consumption of microwave circuits for portable communications up to 2.4 GHz. This can be done by optimizing high gain, high frequency devices for lower power, lower frequency operation.

GaAs and Silicon-based technology are currently the most popular choices for microwave applications requiring amplification devices. These devices are not optimized for ultra-low power applications. GaAs MESFETs (metal-semiconductor field effect transistors), which are the primary device for frequencies above 5 GHz, also require a negative gate bias. Typical power dissipation for a single GaAs MESFET biased for a small-signal, low noise microwave gain block are on the order of 50 mW which is prohibitive for many battery-powered applications. The GaAs MESFET and the Silicon bipolar junction transistor (BJT) are also poor choices for low power logic circuits.

The CHFET (complementary heterostructure field effect transistor) technology developed at Sandia [1] is another low-power digital technology using GaAs-based devices. The n-channel JFET was shown to be comparable to a MESFET in performance but with a higher gate turn-on voltage [2]. This suggests that the JFET may be an excellent microwave device and one that is easily integrable with low-power digital technology. It will then be possible to design mixed-mode (digital and microwave analog) systems and subsystems on a single chip.

A primary goal of this research was to develop a low power microwave monolithic integrated circuit (MMIC) capability that is compatible with the digital CHFET technology. This capability would enable miniaturized system on a chip concepts with size reduction and low power consumption as the primary goals. A secondary goal was to explore the limits of ultra-low power consumption of microwave circuits using other devices that do not offer on-chip digital capability.

This report summarizes the results of a Laboratory Directed Research and Development (LDRD) project performed at Sandia National Laboratories (case #3520.040). The project summarized in this report was made up of the

following efforts: development of low power CHFET devices for microwave applications and development of advanced CHFET devices (0.3 μm gates) for lower power microwave and higher performance digital applications, development of MMIC technology, and demonstration of ultra-low power microwave circuits using JFETs, PHEMTs, and JFET-based MMICs.

II. Background

The CHFET technology has been developed previously at Sandia as a low power digital technology [1]. An n-channel JFET is fabricated on the same substrate as a p-channel HFET as shown in Figure 1. The nJFET is doped only by ion implantation and is separately optimizable from the pHFET, which is doped by a combination of epitaxy and ion implantation. Self-aligned processing (source and drain implants self-aligned to the refractory gate) is utilized in order to improve the performance of the devices. JFETs are attractive compared to MESFETs because of their higher gate turn-on voltage. The self-aligned JFET eliminates excess gate capacitance present in the conventional JFET from metal overhang as well as junction broadening. This typically leads to a rf-performance penalty in the conventional JFET compared to MESFETs of the same gate length. It was shown that the self-aligned JFET has rf performance comparable to a MESFET of the same gate length [3]. Further details of the digital CHFET technology can be found in reference 1. The following discussion pertains to evaluating the CHFET devices for microwave operation.

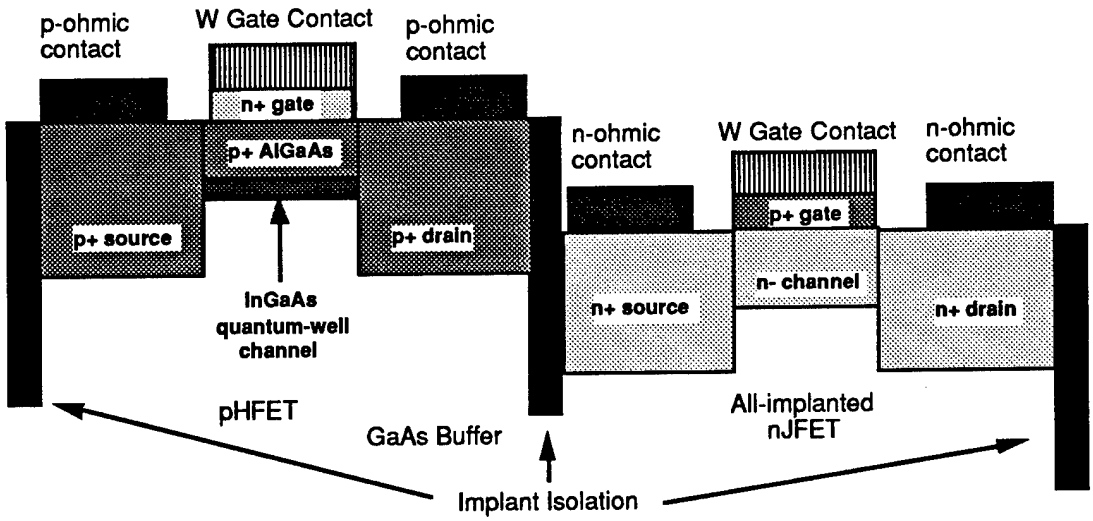


Fig. 1. Schematic device cross sections of the first generation complementary nJFET and pHFET devices. These devices are independently optimizable.

The CHFET devices are optimized for low voltage operation in order to minimize power consumption. The nJFET operates with an f_{max} of 35 GHz for a 0.8 μm gate length. Because of the high electron velocity in GaAs, the nJFETs can be biased at lower drain voltages and still maintain a relatively high f_{max}. This high f_{max} makes the self-aligned JFET an attractive device for microwave operation. The nJFET is a positive threshold device (requirement for complementary logic) which makes single supply operation an attractive feature of this technology, both for digital and microwave applications. Commercially

available MESFETs require both positive and negative power supplies. A MESFET with a positive threshold voltage is not useful for complementary logic due to the low gate turn-on voltage. Thus a unique opportunity exists to combine digital and microwave technology on the same chip by utilizing the nJFET as a microwave device.

In order to achieve low power microwave functions, the technology must be able to achieve microwave amplification at low current levels. However, at low current levels, the performance of the device (such as f_{max}) will degrade. Therefore, technologies with the highest intrinsic performance will be suitable candidates for low power microwave function. We have studied both PHEMTs (pseudomorphic high electron mobility transistors) and nJFETs as low power microwave devices. Not surprisingly, the PHEMT achieved the lowest power levels as it is an intrinsically higher gain device. However, the nJFET is the technology of choice for integrating with low power digital technology.

III. Technology Development

Hybrid 0.7 μm nJFET Narrow Band Amplifier

An nJFET fabricated in the digital CHFET process was evaluated as a microwave device. A narrow-band amplifier was selected as a test vehicle since its successful implementation demonstrates the feasibility of most MMIC functions. The approximate gate length used was 0.7 μm and the gate width was 100 μm. Though not explicitly designed for microwave operation, the device's microwave properties are impressive with $f_t > 13$ GHz, $f_{max} > 20$ GHz and a minimum noise figure of about 1.6 dB (with a 12 dB associated gain) all measured at a 1 mW DC bias level (1 V drain bias and 1 ma).

S-parameters were measured at wafer level and used to design a narrow-band 2.4 GHz microstrip based amplifier. The wafer was then thinned to 100 μm and amplifiers were fabricated from both standard 100 mil stripline packaged parts as well as a chip and wire assembly. The amplifier was fabricated on Rogers TMM-10 25 mil thick substrate, shown in Figure 2 for an amplifier with a packaged part.

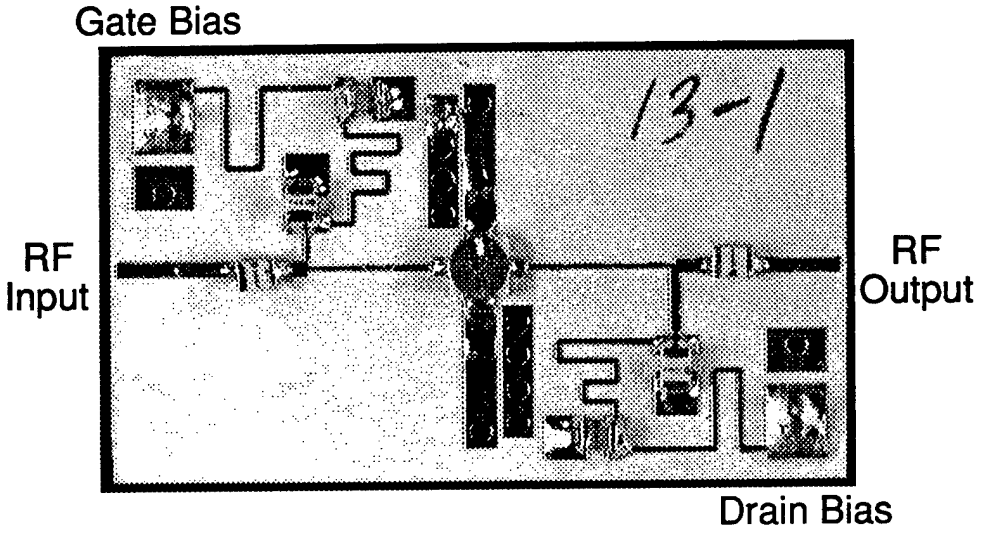


Fig. 2. Photograph of a narrow-band CHFET amplifier using a packaged nJFET.

Tests were performed using an HP 8510C network analyzer and, for selected parts, using an HP 8971 noise figure meter. The measured gain vs. frequency is plotted in Figure 3 for four amplifiers using packaged parts and three amplifiers with chip and wire assemblies. Peak gains between 8 and 10 dB were measured. The matching circuits accurately centered the frequency about 2.4 GHz for the chip and wire parts. Package parasitics were not adequately accounted for and are responsible for the shift in frequency for packaged parts. The minimum noise figure was about 2.5 dB and occurred at a frequency higher than the gain's peak. This is not surprising as the amplifier was designed for maximum gain and not minimum noise figure. A minimum

noise figure design should achieve a value more consistent with the on-wafer measured value of 1.6 dB, although some gain would be sacrificed. The amplifier gain and input and output return loss are plotted in Figure 4.

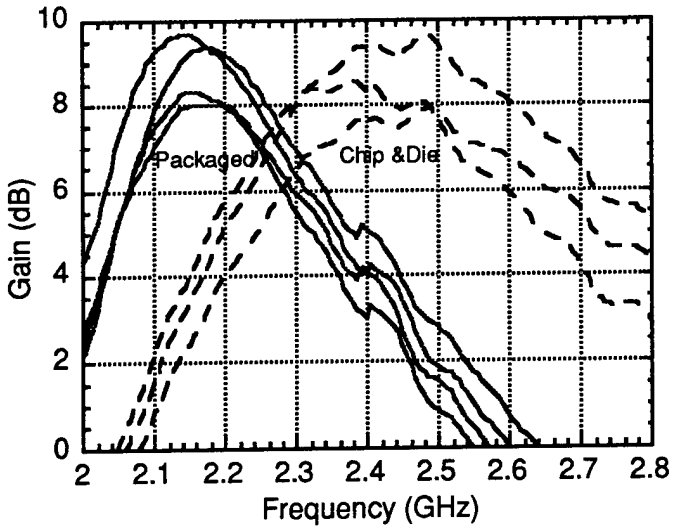


Fig. 3. Gain characteristics of four packaged and three chip and die narrow-band amplifiers operating at 1 mW.

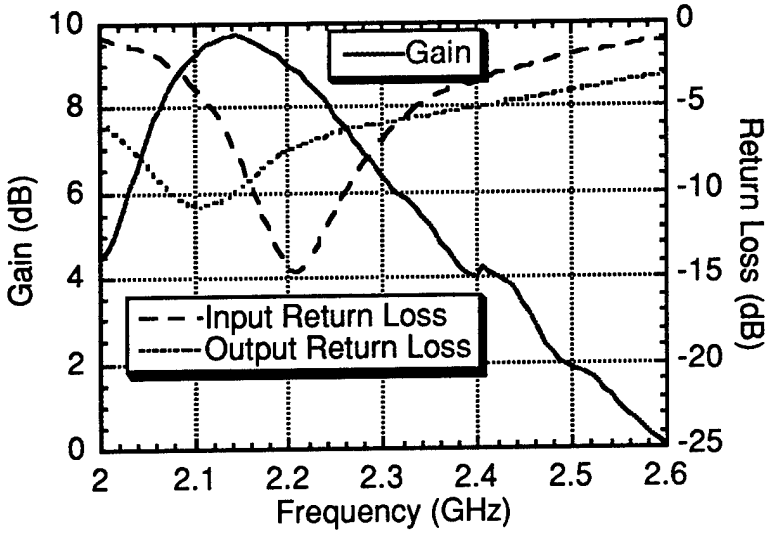


Fig. 4. Amplifier gain and input and output return loss for a narrowband amplifier operating at 1 mW.

MMIC Implementation of 0.7 μm nJFET Narrow Band Amplifier

The performance of the narrow band amplifier was very close to what was simulated using the JFET S-parameters. The good agreement between simulation and the fabricated circuit verified the promise of JFETs as low-power microwave devices. In order to further the goal of mixed-mode technology development, a MMIC design of the LNA was next implemented. Passive elements for MMICs included implanted GaAs thin film resistors (adapted from the CHFET process), airbridge inductors, and SiN thin film capacitors. The capacitors and inductors were developed for other Sandia programs and were implemented into a MMIC for the first time.

The narrowband amplifier was redesigned for on-chip matching. With low current operation the device presents a high impedance. On-chip matching to this high impedance presented a challenge, especially for ensuring stability. Never the less, an adequate design was achieved using conventional narrowband matching networks. A schematic of the completed design is shown in Figure 5.

In order to fabricate the JFET MMIC (JMMIC) the new process steps for thin film capacitors, airbridges, plated metal for transmission lines and inductors, wafer thinning, and backside plating for transmission line ground planes needed to be implemented in the proper sequence so as not to modify the JFET devices. Table 1 shows the standard CHFET process steps (minus p-FET fabrication at this time) in the left column and insertion of the new process steps in the right column. It is seen that some of the CHFET process steps double as MMIC steps as well.

Step	*CHFET Process Steps*	*MMIC Process Steps*
1	Alignment Mark	
2	JFET Channel Implants	
3	JFET Gate Formation	
4	JFET Source/Drain Implants	Resistor Implants
5	JFET Ohmic Contacts	Resistor Ohmic Contacts
6	JFET Via Contacts	
7	JFET Metal 1	Metal 1
8		Capacitor Dielectric (SiN)
9		Metal 2
10		Airbridge Post
11		Plated Metal
12		Wafer Thinning and Backside Plated Metal

Table. 1. Process steps needed for fabricating a JMMIC.

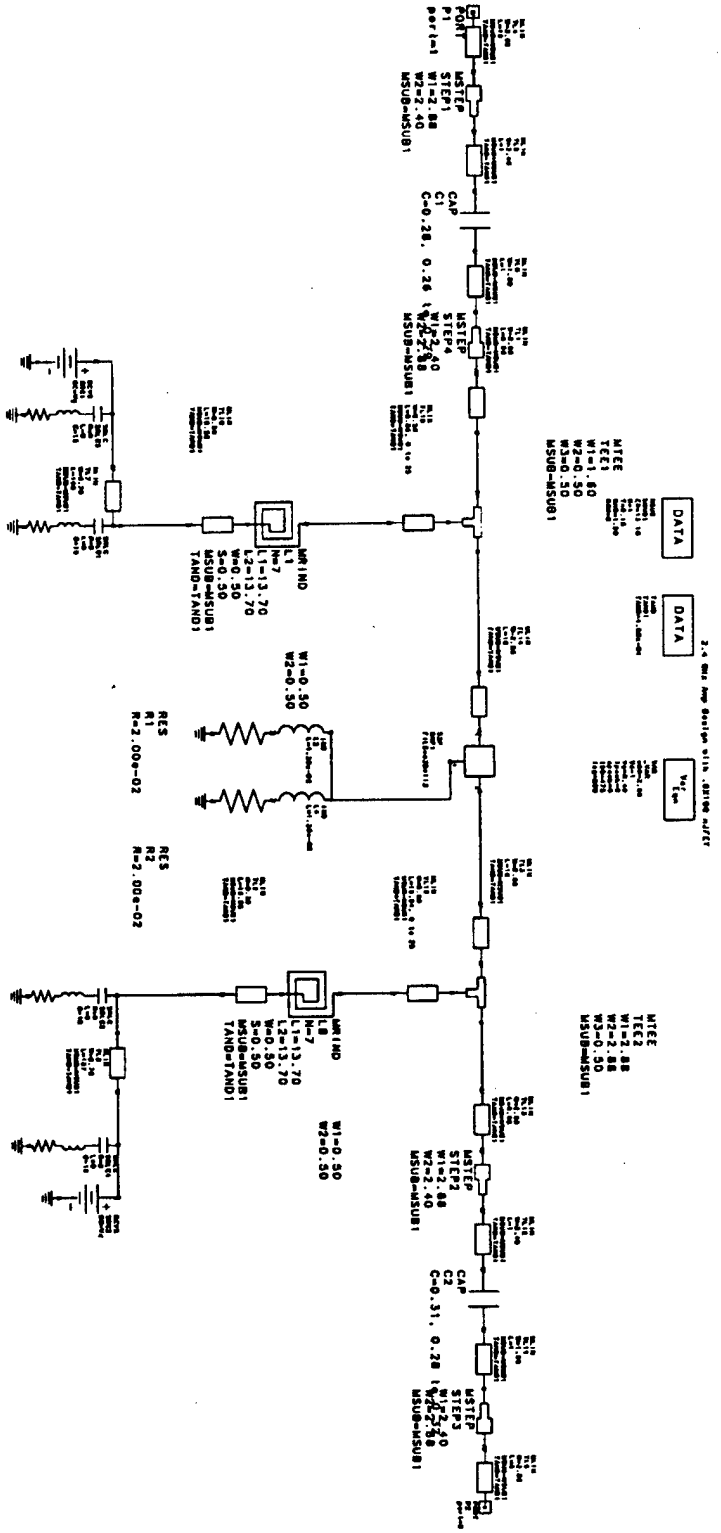


Figure. 5. JMMIC Schematic.

The JMMIC circuits were successfully fabricated. An image of a completed MMIC is shown in Figure 6. The chip size is 2.8 x 2.3 mm^2. The active device area is a small part of the chip size as the chip size is largely determined by the passive elements and the transmission lines. No special problems were noted as a result of combining JFET with MMIC process steps. Increased process complexity (and ultimately cost in a manufacturing sense) was the main effect of the added process steps.

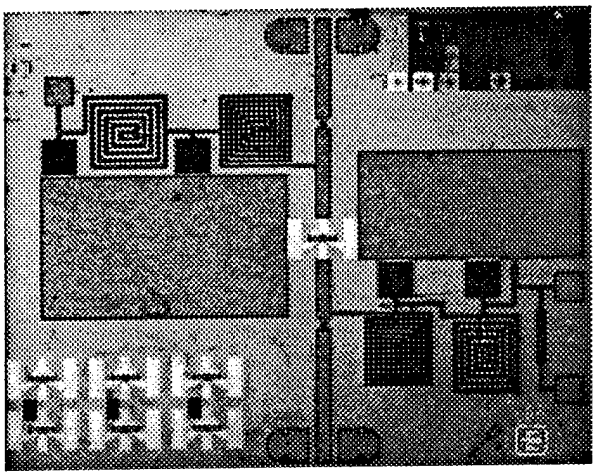


Fig. 6. Microphotograph of the fabricated 2.4 GHZ MMIC.

The JMMICs were silver epoxied to a metal package lid along with chip capacitors for bias stability and alumina microstrip circuit adapters (J Micro Technology) to facilitate microwave probing. The bypass capacitors were 330 pF on the drain supply and 270 pF on the gate supply. Microwave gain and return loss measurements were performed on an 8510C network analyzer using Cascade Microtech Microwave Probes calibrated using a TRL calibration. The amplifiers design goals were 2.4 GHz center frequency, 1-2 mW power consumption, 10 dB gain with 8 dB input/output return loss as in the amplifier based on the discrete JFET. Shown in Fig. 7 are plots of the gain (10.1 dB peak at 2.45 GHz), and input/output return loss (>15 dB at 2.45 GHz) all measured at a 2 mW DC bias condition (Vds=2V, Id=1 mA). The remarkable match to the design goals and good agreement with the hybrid amplifier of Figures 3 and 4 is an indication of excellent device modeling, circuit design, and process control. It is also a further indication of the promise of using CHFET devices as low power MMICs.

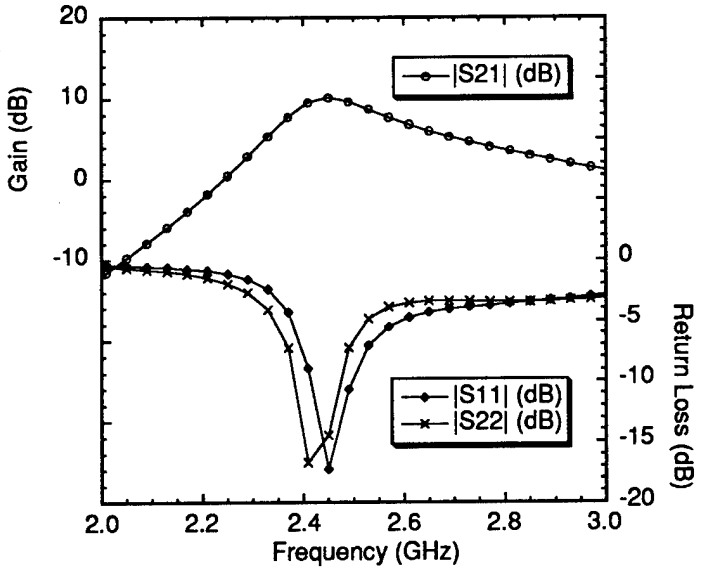


Fig. 7. Measured gain and return loss of the MMIC operated at a 2 mW power level.

Development of 0.3 μm Gate Length Technology

The performance of the CHFET technology can be further increased by shrinking the gate length of the devices. We have reduced the gates from optically patterned 0.7 μm lengths to the 0.3 - 0.4 μm range by the use of e-beam lithography. Both W and W/WSi_x bilayer gates have been patterned. While the W gates are preferable for the non-alloyed ohmic contacts to JFETs because of its greater conductivity, WSi_x gates make superior Schottky contacts for $0.4 \leq x \leq 0.5$ [17]. The Schottky contacts are better for conventional pHFET structures (i.e. non JFETs) and for these FETs the W/WSi_x bilayer gate provides both a good Schottky contact and low gate resistance. Good anisotropic profiles with low plasma damage and sub 0.5 μm W/WSi_x bilayer gates have been obtained with negative electron-beam resist and reactive ion etching in a SF_6/Ar chemistry [4]. A representative gate profile prior to resist removal is shown in Figure 8. A short gate W process works well with the same conditions as the W/WSi_x bilayer gates. The short gate processes have been used to fabricate self-aligned nJFETs and pHFETs. These devices show promise for even higher performance CHFET circuits.

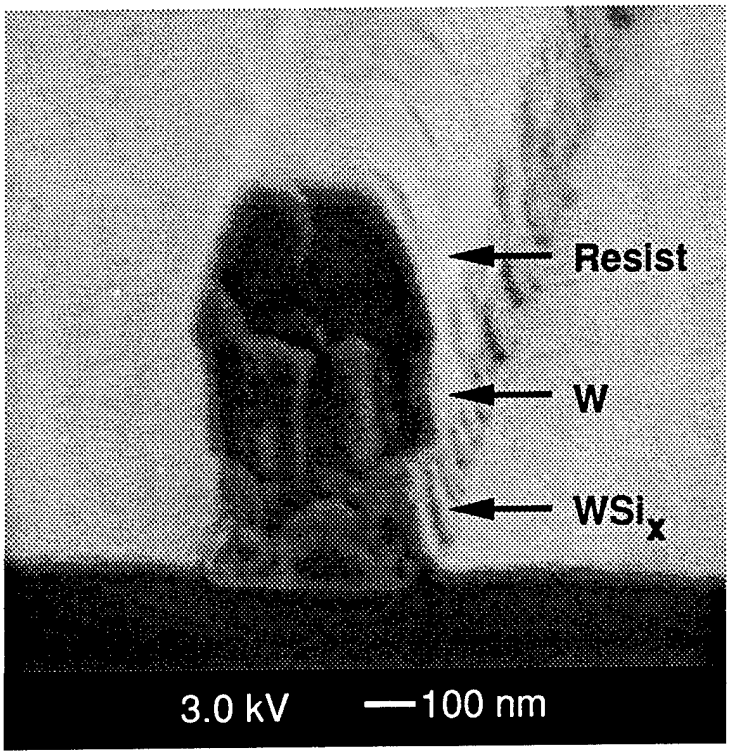


Fig. 8. SEM cross-sectional image of a 0.3 μm W/WSi$_x$ bilayer gate taken prior to resist removal.

Performance of 0.3 μm nJFETs

In addition to short gate definition, the process must be designed to address short channel effects. The channel's active region should be made more shallow and steps must be taken to prevent buffer conduction and associated threshold voltage shift from the source and drain implants. The nJFET p^+ gate implant was changed from Zn to Cd to maintain a high surface doping level greater than 10^{19} cm^{-2} while moving the pn junction closer to the surface [5]. The channel active region was kept the same with a Si implant energy of 70 KeV along with a C backside confinement implant [5]. The Si dose was adjusted to keep the threshold voltage the same. The lateral short channel effects were addressed by implementing a sidewall process with a shallow 40 KeV SiF implant under a 0.1 μm wide SiN sidewall [5] and a deeper 50 KeV Si implant spaced from the gate by the sidewall in the source and drain regions.

Using this process a high performance 0.3 x 40 μm JFET with W gates was fabricated. The drain I-V characteristics are shown in Figure 9. A maximum transconductance of 265 mS/mm was measured with an f_t of 49 GHz, f_{max} of 58 GHz, and a subthreshold slope of 110 mV/decade. The f_t increases proportionately with inverse gate length from 0.7 μm to 0.3 μm, indicating that short channel effects have been suppressed. The increase in f_{max} is not proportional to inverse gate length, indicating that high gate resistance is an important factor at these short gate lengths.

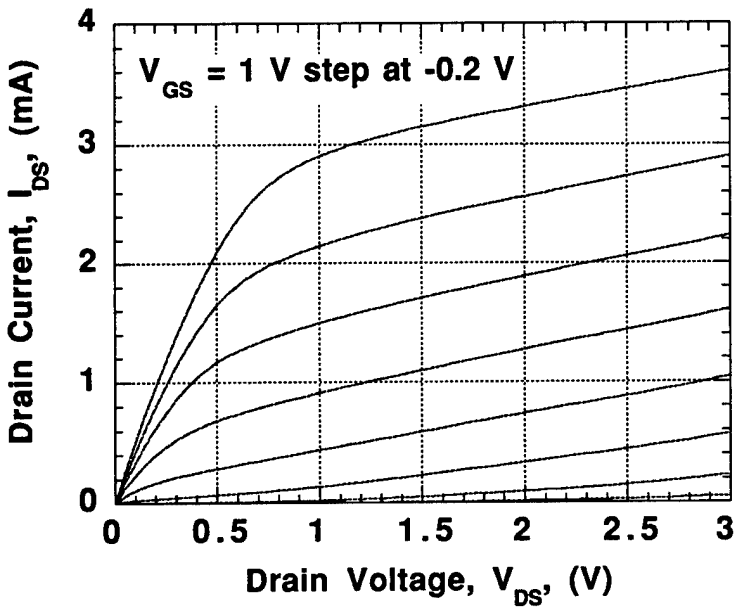


Fig. 9. I_{DS}-V_{DS} characteristics for a self-aligned 0.3x20 μm nJFET.

Simulation of 0.3 μm JFET Amplifiers

Performance enhancements of the nJFET devices has been improved by shrinking the gate length from 0.8 μm to 0.3 μm. Intrinsic f_t has been improved almost threefold over the 0.8 μm numbers to near 60 GHz (Figure 10). The maximum oscillation frequency (f_{max}) was seen to improve significantly (compare Figure 11 to 10), especially at lower power levels.

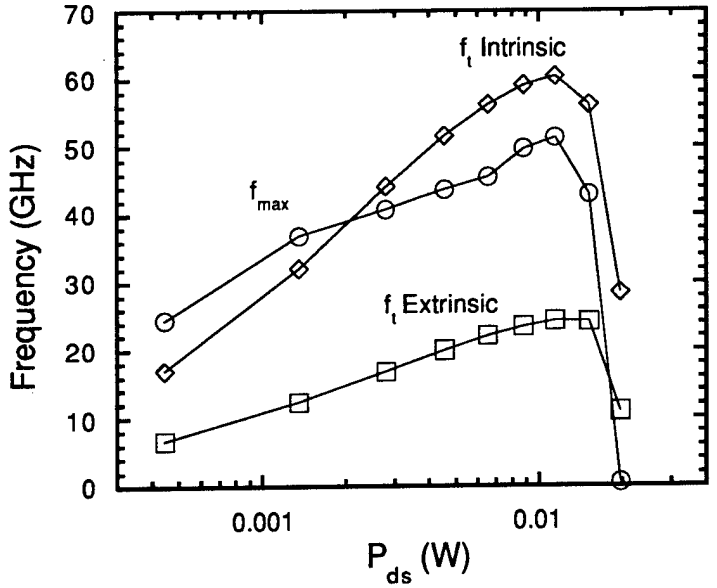


Fig. 10. Plot of the maximum oscillation frequency (f_{max}) and the intrinsic and extrinsic transit-time frequencies (f_t) as a function of DC drain power ($P_{ds}=V_{ds}I_{ds}$) for a 0.3x40 μm^2 JFET. (V_{ds} = 1.5V & V_{gs} = [-0.5,1.5]V).

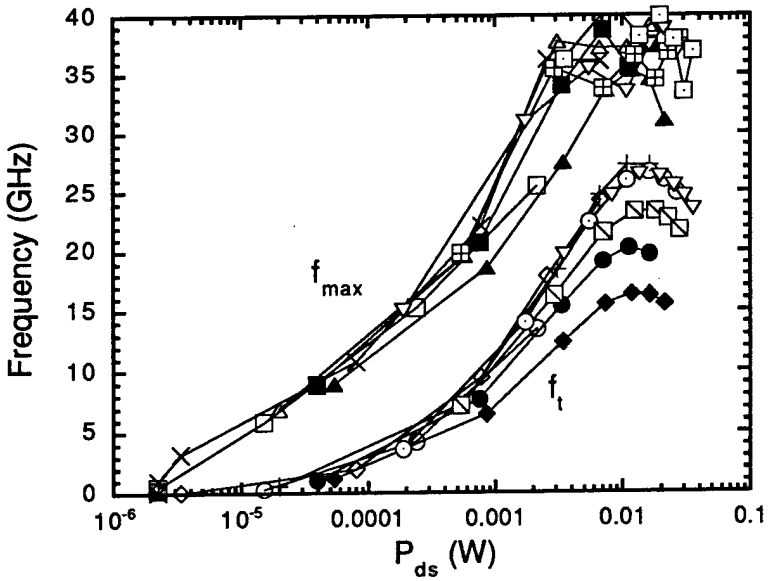


Fig. 11. Plot of the maximum oscillation frequency (f_{max}) and the intrinsic transit-time frequency (f_t) as a function of DC drain power ($P_{ds} = V_{ds} I_{ds}$). All were measured at V_{ds} = 1.5 V. Data is shown for for a 0.8x100 μm^2 JFET's with 7 different implant doses (1.3x10^{13} to 2.7x10^{13} cm^{-2}) which controls their thresholds from +0.9 to -0.7 V.

On-wafer S-parameters were used to simulate an amplifier and these gains in device performance resulted in a 4x reduction in circuit power (250mW for 10dB gain). Though this improvement is impressive, much larger reductions in power dissipation were projected and realized using pHEMTs as discussed below. Additionally, the cost of changing our baseline CHFET technology to this smaller dimension were determined as too high for success and further exploratory work with PHEMTs circuits was deemed more promising (see section IV).

0.4 μm pHFET Devices

The pHFET structure was completely redefined for the 0.4 μm design compared to the 0.7 μm design. A doped-channel GaAs/AlGaAs pHFET was chosen for the current design. A 100 Å Be-doped GaAs channel with a 50 Å GaAs spacer, a 150 Å $Al_{0.75}Ga_{0.25}As$ undoped barrier layer, and a 100 Å cap layer form the active layers of the pHFET. This pHFET is still process compatible with the GaAs self-aligned nJFET. The doped channel pHFETs can be adjusted for the desired threshold voltage independently of the nJFET, while maintaining high gate turn-on voltage demonstrated in HIGFETs with high Al mole fraction AlGaAs barriers. Lateral short channel effects are especially severe in compound semiconductor pFETs. They have been addressed in this work with a 0.1 μm wide SiN sidewall process using 50 KeV Zn implants under the sidewalls and 125 KeV implants in the source and drain regions.

pHFETs with gate lengths ranging from 1.0 to 0.3 μm was fabricated and characterized. The transistors scaled very well down to 0.5 μm gate length. The output conductance and subthreshold slope degraded noticeably at 0.4 μm gate length and severe short channel effects were observed at 0.3 μm. Nevertheless, good rf characteristics were observed down to 0.4 μm gate lengths. Drain I-V characteristics for a 0.4 x 20 μm pHFET are shown in Figure 12. A maximum transconductance of 62 mS/mm was with f_t of 11.5 GHz and f_{max} of 13 GHz. The subthreshold slope ranges from 130-170 mV/decade for gate lengths 0.5 μm and longer, as seen in Figure 13. At 0.4 μm gate length the subthreshold slope increases to 310 mV/decade. These subthreshold slopes are still not as good as nJFET values but are clear improvements even at long gate lengths from our previous pHFETs [1]. The transconductance decreases only slightly to 54 mS/mm when operating biases is reduced to 1.0 V on the gate.

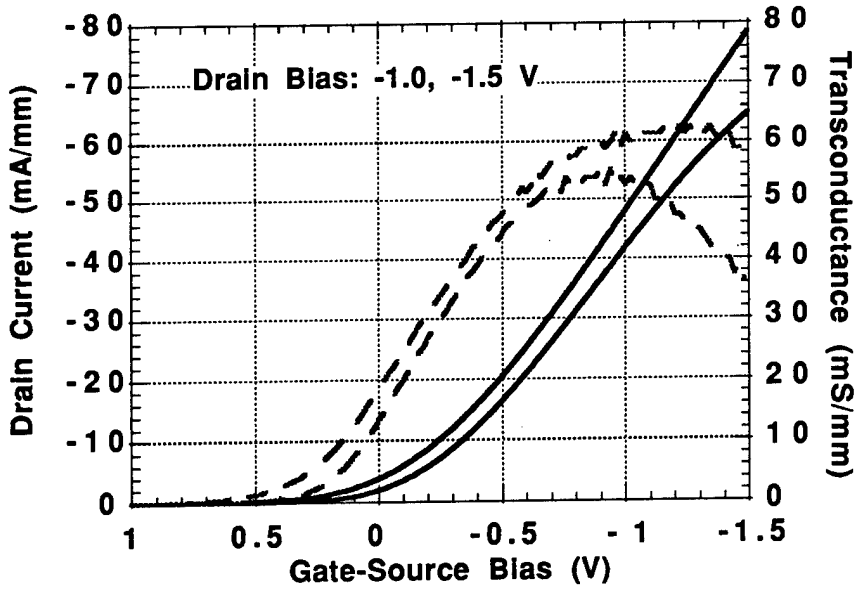


Fig. 12. I_{DS}-V_G and g_m-V_G characteristics at drain biases of -0.5, -1.0, and -1.5 V for a self-aligned 0.4x20 μm pHFET.

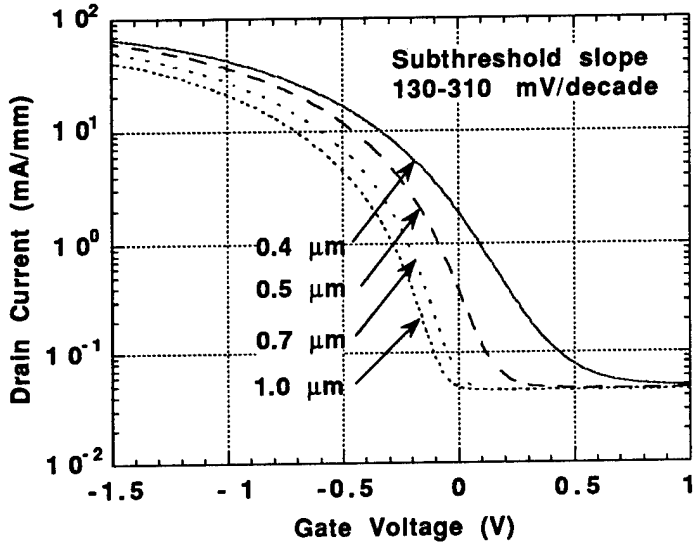
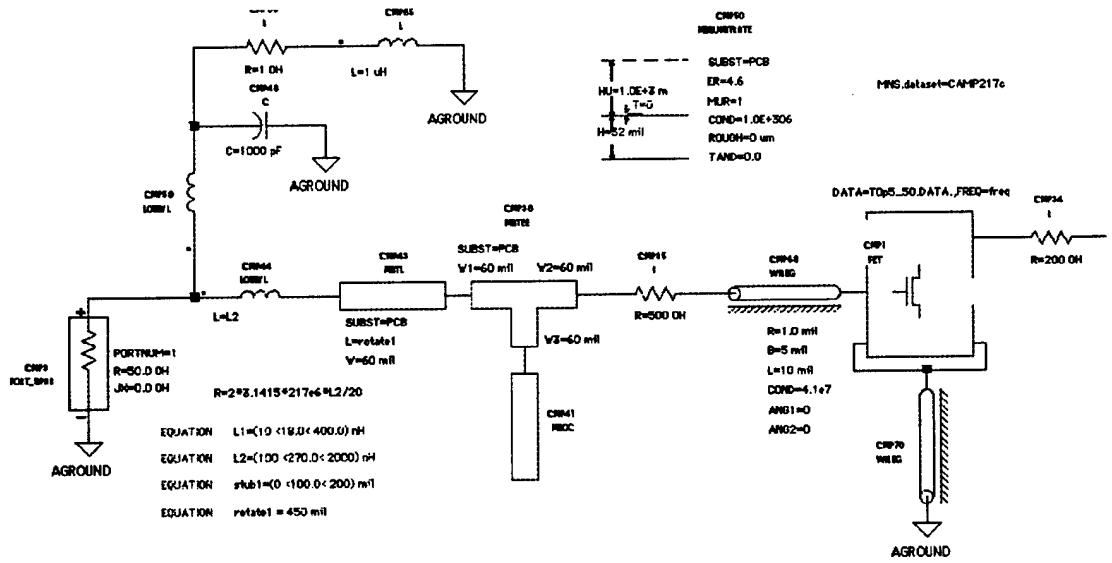


Fig. 13. I_{DS}-V_G characteristics at a drain bias of -1.0 V for a self-aligned 0.4x20 μm pHFET.

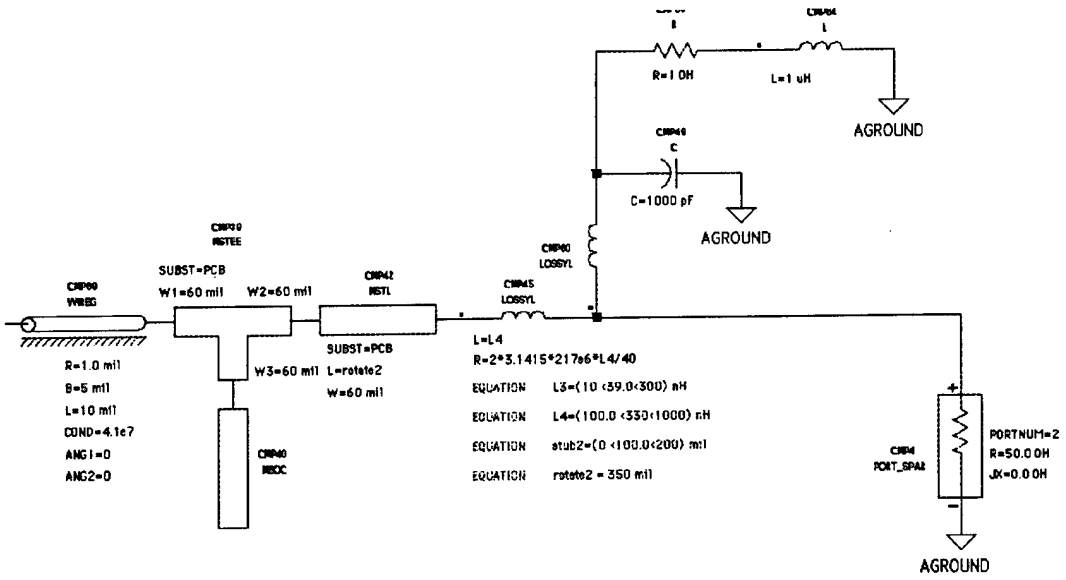
IV. PHEMT Circuits

A single-stage ultra-low-power amplifier was developed based on a CSRL fabricated, 0.2x10 μm^2 pHEMT device. A gain of 10dB at V_{ds} = 1.0 V with I_d < 150 μA at 215 MHz was realized.

Figure 14 shows the schematic of the amplifier circuit. A split inductor design was selected in order to avoid the extremely small capacitors necessary in more conventional LC matching networks. The stubs to either side of the transistor provide convenient adjustment (by cutting) of the resonant frequency of the matching networks. The resistors to either side of the transistor were required based on stability simulations. Both input and output matching networks are necessarily high-Q to achieve the required impedance transformation. Inductor Q limitations were found to be a severe design restriction.



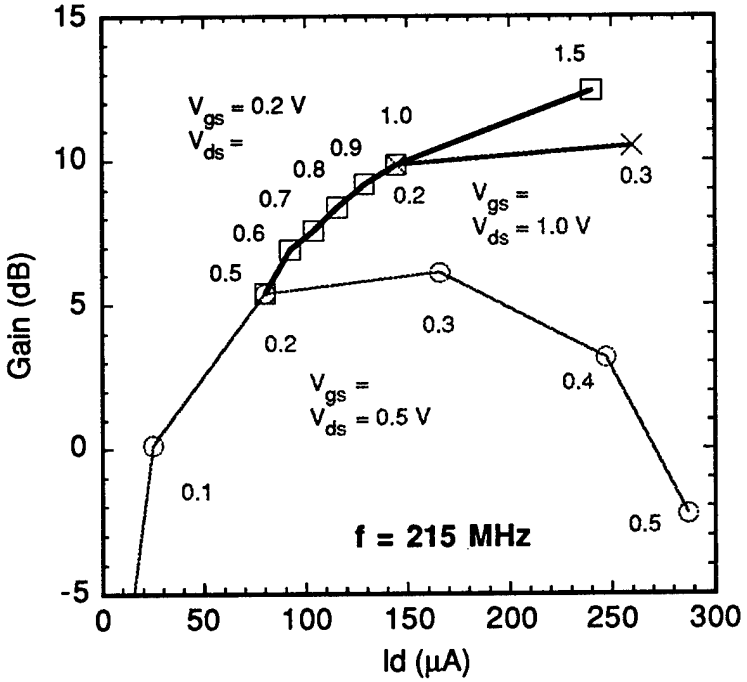
a)



b)

Figure 14. Schematic diagram of the 217 MHz pHEMT LNA. a) Input circuit. b) Output circuit.

Figure 15 shows the peak gain of the circuit at a variety of bias points. The design goal was 10 dB gain at 217 MHz with Vds=0.5V and Id=50 μA for a bias power level of 25 μW. Clearly, the measured gain falls short of this target. The first construction of the amplifier used chip inductors which resulted in only a few decibels of gain under the best of bias conditions. Substitution of hand-wound wire inductors resulted in an improvement of about 6 dB. The present low gain is believed to be still due to the low Q of the inductors.



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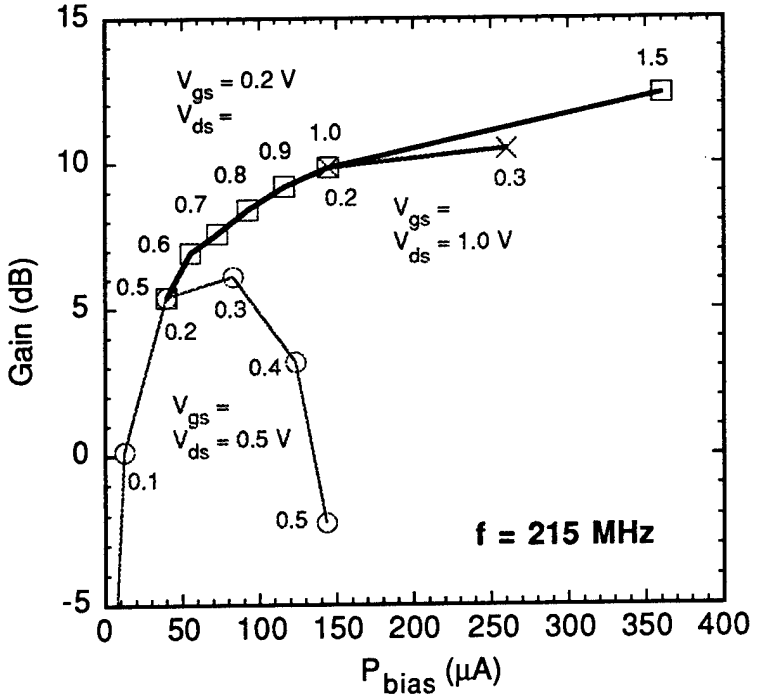

b)

Figure 15. Measured peak gain at various bias conditions . a) Current x-axis. b) Bias power x-axis.

Figures 16 and 17 show the measured noise figure performance. Figure 16 shows the gain and noise figure versus frequency with the device at V_{ds} = 1V and I_d = 100 μA in which the peak gain is about 9 dB with an 8 dB noise figure. Figure 17 shows the noise figure and gain at various bias points at 218 MHz. The noise figure is excessive for what would be expected from a pHEMT. This is believed due to excessive loss in the matching network. Note in Figure 17 that the noise figure is relatively constant with applied bias. This suggests that the noise figure is dominated by matching losses - not basic device limitations. Also, an excessive matching loss is consistent with the lower than expected circuit gain.

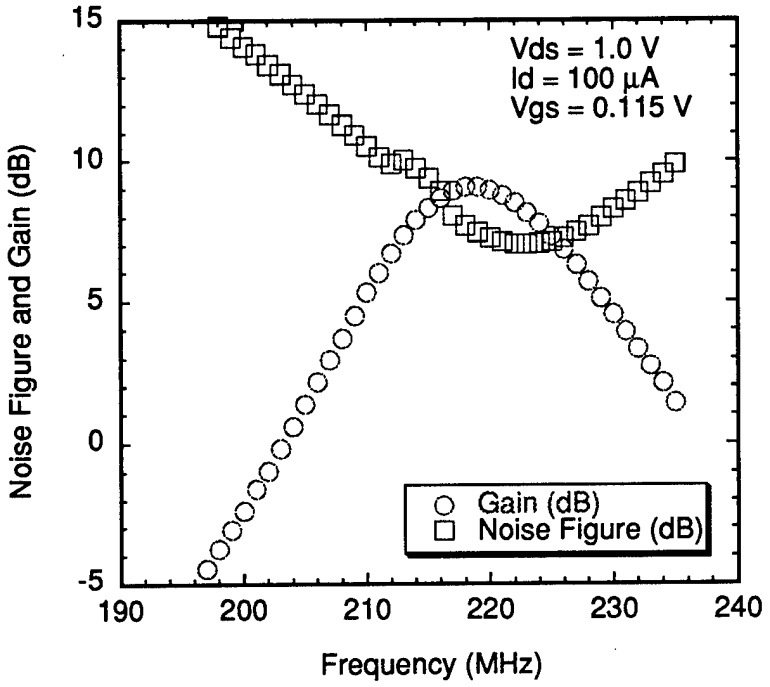

Figure 16. Measured noise figure and gain versus frequency.

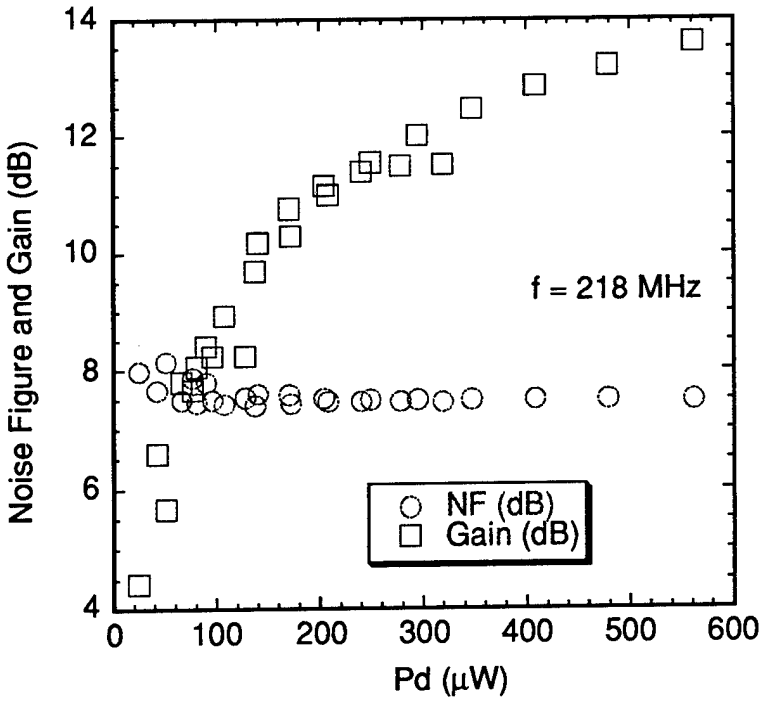

Figure 17. Measured noise figure and gain at 218 MHz for a variety of bias conditions.

To address this issue, we tried another inductor design with a heavier gauge wire which resulted in an increase in Q. Figures 18 and 19 summarize the improvements seen with the pHEMT amplifier constructured with these higher-Q inductors. This data can be compared to the previous results as shown in Figures 8. A few dB gain increase is observed. The NF has also been cooresponding reduced by a dB or so. Fig. 19 shows the improved amplifiers gain and noise figure vs. frequency at V_{ds}=0.5 and 1.0V with 100μA bias.

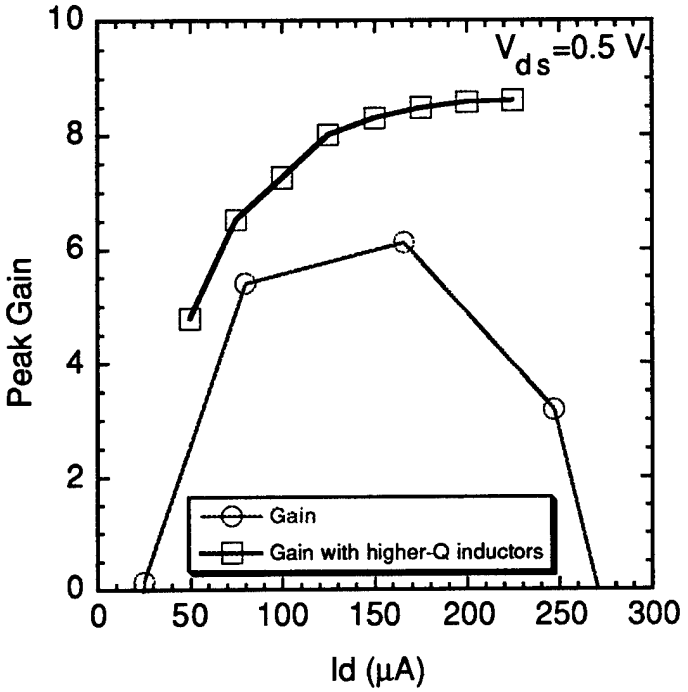

Figure 18. Measured peak gain at V_{ds}=0.5 V at various current bias levels for the old and new inductor configuration.

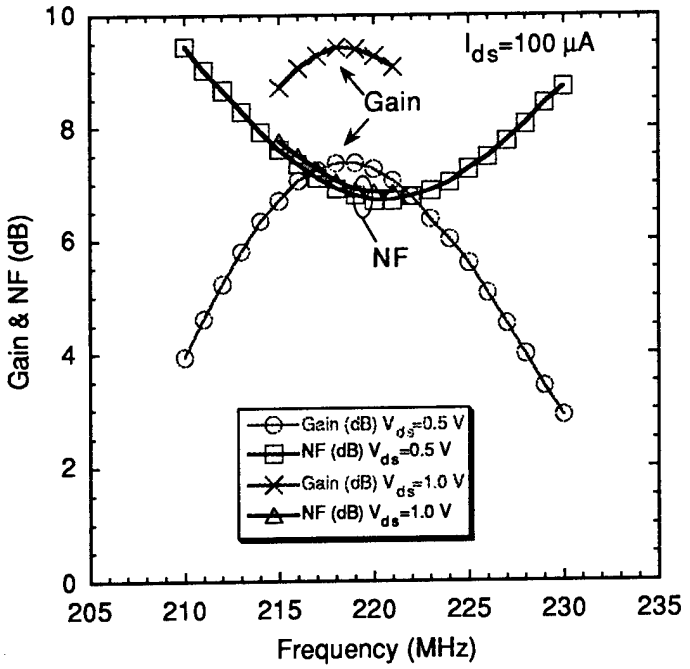

Figure 19. Measure gain and noise figure of the improved amplifier at V_{ds}=0.5 and 1.0 V .

In general, a gain higher than 10 dB is required for most system needs. If three stages of this current design are used, a bias of 75 µA would be required for 20dB gain. Other configurations are of course possible. For example, with V_{ds}=1.0V a 50µA bias can produce about 20dB gain. The bias for the three stages can be "stacked" from the 3V battery. The noise figure of the resulting amplifier would exceed 7 dB which may be excessive for system requirements.

V. Conclusions

This work has shown that power consumption of microwave circuits can be reduced by factors of 50-1000 over commercially available circuits. We have demonstrated microwave amplifiers with as little as 50 μW power consumption at 217 MHz for 0.25 μm gate length PHEMTs. This work also showed that MMICs compatible with digital CHFET technology can achieve power levels in the range of 1 (0.25) mW at frequencies of 2.4 GHz (217 MHz). These power levels go far beyond what has been reported in the literature and are promising for greatly extending battery life in portable electronics.

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Appendix A. LDRD Summary

Refereed publications resulting for the work: 2

A. G. Baca, J. C. Zolper, M. E. Sherwin, D. F. Dubbert, V. M. Hietala, R. J. Shul, L. R. Sloan, and M. J. Hafich, "Complementary HFET Technology for Low-Power Mixed-Mode Applications," *Mat. Res. Soc. Symp. Proc.*, vol. 421, p.227.(1996) p. 227.

R. J. Shul, M. E. Sherwin, A. G. Baca, J. C. Zolper, and D. J. Rieger, "Short Gate Etching of W/WSi Bilayer Gates," *Electronics Letters,* vol 32, p. 70 (1996).

All other reports and publications resulting from the work: 2

A. G. Baca, J. C. Zolper, D. D. F., V. M. Hietala, L. R. Sloan, R. J. Shul, M. E. Sherwin, and M. J. Hafich, "Complementary HFET Devices for Wireless Digital and Microwave Applications," *Electrochemical Society Meeting*, San Antonio, TX, USA, (1996), p. 73.

J. C. Zolper, A. G. Baca, M. E. Sherwin, V. M. Hietala, and R. J. Shul, "Ion Implanted GaAs JFETs with ft > 45 GHz for Low Power Electronics," *GaAs IC Symposium*, Orlando, FL, USA, (1996), p. 159.

Number of patent disclosures: 0

Number of patent applications: 0

Number of patents: 0

Number of Copyrights: None

Number of students: None

Number of post docs: None

Number of permanent technical or scientific staff: None

Number of awards (and their names): None

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