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A NEW REACTOR SAFETY CIRCUIT FOR LOW-POWER-LEVEL OPERATION*

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ABSTRACT

In the operation of nuclear reactors at low-power levels, one of the primary instrumentation problems is that the statistical fluctuations of reactor neutron population are accentuated by conventional log-count-rate and differentiating circuits and can cause frequent spurious scrams unless long time constants are incorporated in the circuit. Excessive time constants may introduce undesirable delay in the circuit response to legitimate scram signals. This paper develops the concept of a count doubling-time monitor which generates a scram signal if the number of counts from a pulse type neutron detector doubles in a given period of time. The paper demonstrates the theoretical relation between count doubling time and asymptomatic periods. A practical circuit to implement the function is described.

Introduction

The Zero Power Reactor No. 6 (ZPR-6) facility is operated by Argonne National Laboratory to provide reactor physics data in support of the United States Reactor Development program. Its instrumentation includes BF_3 proportional counters and the associated pulse counting electronics along with BF_3 DC ionization chamber circuitry to monitor reactor power levels. With the present reactor cores all the instrumentation is sensitive to source flux levels during reactor startup.

Future program needs, however, will require the study of fast neutron, epithermal and thermal neutron zones surrounded by blanket zones. Since the detectors will be located outside the blanket zones, the DC ionization channels may be prevented from monitoring the flux at source levels and this may require that rate of change power level monitoring capability be incorporated in the pulse type instrument channels. The counting rates from the pulse channels may be lower than 100 counts per second. The statistical fluctuations of reactor neutron population are large at the low counting rates and these fluctuations are accentuated by conventional log count rate and differentiating circuits. Either excessively long time constants must be incorporated in the log count rate and differentiating circuits or relatively frequent spurious scram signals must be accepted.

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An alternative to conventional period instrumentation utilizes circuitry which measures the time interval required to double the count over that in a previous interval. By ensuring that this doubling time does not become too short, the required safety function is assured.

It should be noted that a system using counts permits the uncertainty in the value of the number of counts to be balanced against an allowed increase in power level. Limitation on the size of the power level increase is determined primarily by the time interval selected. In conventional period measuring devices the uncertainty in the measured value of the period is balanced against circuit response speed.

At low and medium power levels, where counting channels are effective, it is acceptable to allow modest increases in power level before initiating protective action provided the protective action is very fast after the maximum acceptable power level increase has been reached.

Theory of Operation

Existing rate-of-change-of-power-level monitoring circuits measure the reactor period by using an appropriate circuit to obtain the logarithm of the counting rate and subsequently differentiating this signal with respect to time. If the reactor is on a period asymptotic to a constant value, the resulting signal is a measure of the reactor period. This is shown as follows:

1. $C(t)/C(o) = e^{\alpha t}$

Where: $C(t)$ is the counting rate at time t,
$C(o)$ is the counting rate at time zero,
α is the inverse of the reactor period T, and
t is elapsed time.

2. $\alpha = d/dt\,[\ln\{C(t)/C(o)\}] = T^{-1}$

Although the "count doubling time" measuring circuit is not a period measuring circuit, the doubling time and period are related for asymptotic periods. The relation is given by:

3. $T_{j-(j+1)} = \alpha^{-1}_{j-(j+1)} = \dfrac{\Delta t_{j-(j+1)}}{\ln[N_{(j+1)}/N_j]}$, where

$T_{j-(j+1)}$ is an asymptotic period measured between t_j and $t_{(j+1)}$,

$N_{(j+1)}$ is the number of counts occurring between t_j and $t_{(j+1)}$,

N_j is the number of counts occurring between $t_{(j-1)}$ and t_j, and

$t_{j-(j+1)}$ is the time duration between time t_j and time $t_{(j+1)}$.

The circuit* measures the time necessary for the number of counts in the interval from t_j to $t_{(j+1)}$ to equal twice the number of counts in the interval from $t_{(j-1)}$ to t_j. If this time is less than a preselected value, a scram is initiated as soon as $N_{(j+1)}/N_j$ is equal to 2. The scram will occur on the basis of the time required for $N_{(j+1)}/N_j$ to equal 2 regardless of whether the reactor is on an asymptotic or transient period. In practice, if the times required for $N_{(j+1)}$ to be twice N_j are greater than the preselected value, the circuits are reset at definite Δt intervals, $N_{(j+1)}$ replaces N_j as the reference count, no scram is initiated and the count sampling continues.

The ratio $N_{(j+1)}/N_j$ may, of course, be any appropriate constant. However, the factor 2 is certainly acceptable from safety considerations for low and medium power level reactor operation and is convenient from circuit considerations. The statistical fluctuations in the count associated with $N_{(j+1)}/N_j = 2$ are also acceptable. If, for example, a scram is desired when $N_{(j+1)}/N_j = 2$ occurs in less than 4 seconds, a counting rate of 100 counts per second would result in 400 counts during this interval. The standard deviation would be 20, and a 10σ deviation would be only 50% of the total count required to effect a scram. The relation between $N_{(j+1)}/N_j$ and $\Delta t_{j-(j+1)}$ as indicated by Eq. 3 can be derived for asymptotic periods as follows.

Consider the counting rate $C(t)$:

4. $C(t_{(j-1)}) = C(o)[\text{Exp } \alpha t_{(j-1)}]$.

If the reactor is on an asymptotic period

5. $C(t_{(j+1)})/C(t_j) = C(t_j)/C(t_{(j-1)}) = \ell^{\alpha\Delta t}$

where $\Delta t = \Delta t_{(j-1)-j} = \Delta t_{j-(j+1)}$. The number of counts accumulated in the interval from $t_{(j-1)}$ to t_j is

6. $$N_{(j-1)-j} = C(1)\int_{t_{(j-1)}}^{t_j} \ell^{\alpha t}\, dt$$

$$= \{C(o)/\alpha\}\{\text{Exp}[\alpha t_{(j-1)}]\}\{\text{Exp}[\alpha\Delta t]-1\}$$

Repeating the process to find $N_{j-(j+1)}$ for the t_j to $t_{(j+1)}$ interval, taking the ratio $N_{j-(j+1)}/N_{(j-1)-j}$, taking the natural logarithm and rearranging, we obtain Eq. 3.

If, as in the case for the conventional log N/Period measuring instruments, an erroneous period indication is acceptable for non-asymptotic periods, the period may be determined by using Eq. 3; otherwise better approximations must be developed.

The function of the safety circuit clearly is not compromised by the choice of indicating the doubling-time or period on a recorder or meter, since the doubling-time safety circuit operates strictly on count doubling-time information and not on perceived period.

Circuit Description

As shown in Fig. 1 the circuit is comprised of two Mostek MK505395, MOS six-decade Counter/Display chips and appropriate SSI gating. The MK50395 contains a six-decade counter, compare registers and storage latches. The counter, as well as the register, can be loaded digit by digit with BCD data. Multiplexing and de-multiplexing is controlled by a scan input. The count output and the data stored in the register comprise a digital comparator and have the capability of outputting functions of comparison. All these functions described above as well as the multiplexed output ability of the MK50395 are used in implementing the count doubling time safety circuit.

The circuit also contains a CMOS programmable timer, an external CMOS latch circuit, routing circuits, trip logic circuits and two, six-decade digital displays.

The signal from a conventional proportional counter and pulse amplifier system is routed to a commercial low level discriminator which inhibits low-level signals from gamma radiation and electronic noise and outputs a standard TTL compatible pulse for all input pulses above the preset level. Since this signal is used by the conventional low level reactor scram circuit it is isolated via an opto-isolator and line driver circuit.

The isolated pulse train is then routed via a cable to the count doubling time safety circuit, where the signal is terminated in a line-receiver. The signal is then amplified to a 12V level so as to be compatible with the +12V logic required by the MK50395 counters.

After amplification, the pulse train is routed to the N1 counter input and to a divide by two flip-flop. The output of this flip-flop is routed to the N2 counter input.

The pre-programmable timer is configured as an asynchronous monostable using its own chip RC oscillator. This signal is buffered and used as the scan input to the N1 and N2 counters at a frequency of 12.5 kHz. Since the internal multiplexing of the counter is synchronized to the scan input, both counters are commonly synchronized. The 12.5 kHz mono output is also divided by 2^{16} by the timer producing a 5.24 second timing pulse used as the basic timing interval Δt. The timer also contains another on-chip monostable which is configured to output a timing pulse of 570 µs width every 5.24 seconds. The width of this pulse must exceed six scan pulses (480 µs) in order to perform the output de-multiplexing properly.

A pre-start logic circuit is used to provide the N2 counter's register with an initial count for comparison against the N2 count. It also contains the necessary logic to initialize the timer, reset the counters and other actions required for proper operation of the counters.

*It should be noted that the "count doubling time" is not necessarily the same as the "count rate doubling time" usually referred to during reactor operations.

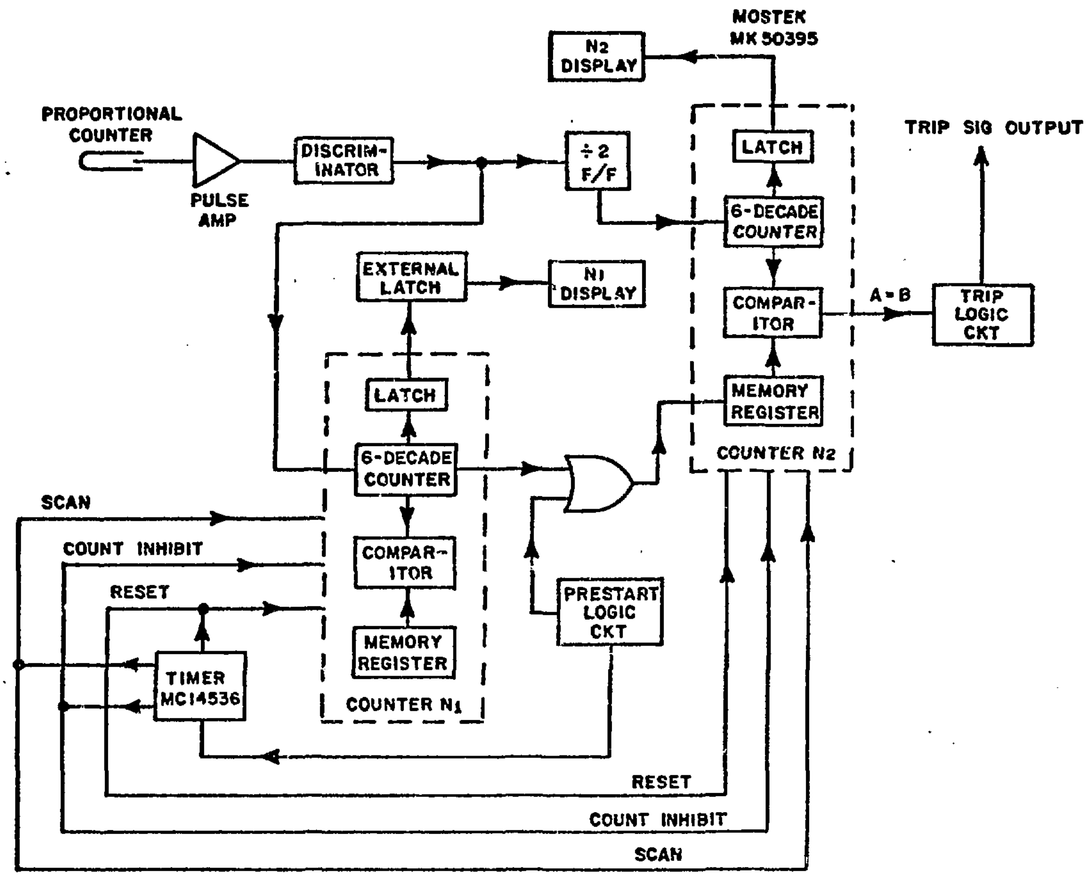

Figure 1. System block diagram.

After the initial count of 5.24 seconds, the N1 count is routed to N2 counter's register for comparison with N2's second count cycle. The count contained in N2's register is always one cycle behind the count input to this counter. Therefore, anytime N2's count exceeds that of its register count it senses that $[N_{j-(j+1)}]/[N_{(j-1)-j}] \geq 2$ and an A=B pulse is routed to the trip latch circuit, initiating a trip.

Between each timing cycle, that is during the 570 µs time period generated by the timer, the N2 register is updated by transfer of N1's counter contents, the A=B pulse is inhibited and the N1 and N2 display latches are updated.

It should be noted, however, that the initial 2 µs of this 570 µs time period are used exclusively to latch the previous count stored in N1's external latch into the N1 display. Immediately following this 2 µs period of time the previous actions described take place. This allows us to display the previous N1 count and the present N2 count which are counts used to calculate the reactor period as shown in Eq. 3.

It should be pointed out that the cycle is continuous once started and that the counts are automatically updated. If a trip should occur the trip latch will initiate a trip signal to the reactor. However, the cycle remains uninterrupted and, when the trip is cleared by the trip reset, the safety cycle is still in effect providing continuous monitoring.

Conclusion

The count doubling time monitor and trip circuit is an inexpensive, simple, reliable and fast safety device that prevents the reactor power level from rising too rapidly. The circuit uses counting techniques which offers the advantages of reliability, speed and freedom from spurious trips that so often plague conventional analog instrumentation. In conventional period circuitry the uncertainty in the value of the measured parameter is traded off against the circuit response speed. With the count doubling circuit the magnitude of the uncertainty in the value of the measured parameter is traded off against an allowed increase in power level. At low power levels the error voltages induced by the differentiation of the noise in the log signal is at its maximum. These error voltages have caused spurious scrams creating problems in reactor start-ups. The characteristics of the count doubling time circuit are particularly useful at low power levels as proper selection of the N_2/N_1 ratio can make the probability of spurious scrams negligible without compromising reactor safety. If period information is desired for display and recording purposes, an inexpensive, microporcessor based, circuit could be operated in parallel with the safety circuit. Such a circuit has been developed and tested and will be described in a later publication.