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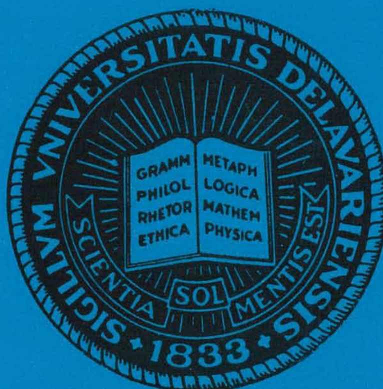

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The primary goal of this program, increasing the conversion efficiency of a thin-film cell based on CdS/Cu_2S, has been achieved. A number of $(CdZn)S/Cu_2S$ cells have been made with conversion efficiencies in excess of 10% when tested in collimated sunlight. The highest efficiency achieved was 10.2% for a cell with 16% Zinc which had the following parameters; V_{OC} = 0.60V, J_{SC} = 22.8 mA/cm^2 (pro-rated to 100 mW/cm^2,) FF = 74.9%. Further improvement in the performance of CdS/Cu_2S cells beyond the previously reported 9.2%, was found to be limited by deficiencies in the fundamental knowledge and control of the Cu_2S layer. A number of process changes in the production of CdS/Cu_2S cells have been explored and are reported on. Transient capacitance measurements on CdS/Cu_2S cells and further development of an integral encapsulation are also reported.

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1. Abstract

The primary goal of this program, increasing the conversion efficiency of a thin-film cell based on CdS/Cu_2S, has been achieved. A number of $(CdZn)S/Cu_2S$ cells have been made with conversion efficiencies in excess of 10% when tested in collimated sunlight. The highest efficiency achieved was 10.2% for a cell with 16% Zinc which had the following parameters; V_{OC} = 0.60V, J_{SC} = 22.8 mA/cm^2 (pro-rated to 100 mW/cm^2), FF = 74.9%. Further improvement in the performance of CdS/Cu_2S cells beyond the previously reported 9.2%, was found to be limited by deficiencies in the fundamental knowledge and control of the Cu_2S layer. A number of process changes in the production of CdS/Cu_2S cells have been explored and are reported on. Transient capacitance measurements on CdS/Cu_2S cells and further development of an integral encapsulation are also reported.

Page

2. Table of Contents

1. Abstract 2

2. Table of Contents 3

3. Introduction 4

4. Cell Production, Analysis and Testing 5

   4.1 Development CdS/Cu_2S Solar Cells 7

   4.2 Development (CdZn)S/Cu_2S Solar Cells 23

   4.3 Electro-Optical Analysis and Modeling 48

   4.4 Encapsulation for Improved Stability 55

5. References 57

6. Reports and Publications 58

Appendices 59

A. Comments on "Space Charge Limited Currents in Cu_xS/CdS Solar Cells."

B. Photocapacitance Study of Hole Traps in CdS/Cu_2S Cells. W. J. Manthey.

C. The Design & Fabrication of Thin Film CdS/Cu_2S Cells of 9.15% Conversion Efficiency. J. A. Bragagnolo, A. M. Barnett, J. E. Phillips, R. B. Hall, A. Rothwarf and J. D. Meakin.

D. Growth & Evaluation of CdS and (CdZn)S Films and the Fabrication of High Performance Photovoltaic Devices. R. B. Hall, R. W. Birkmire, E. Eser, T.L. Hench and J. D. Meakin.

E. Optical Absorbtion Coefficient Changes in Cu_2S as the Cause of Short Circuit Current Changes in Cu_2S/CdS Solar Cells. A. Rothwarf and H. Windawi.

F. Current-Voltage Analysis of the Cu_2S/CdS Solar Cell with an Interdigitated Grid. J. E. Phillips.

G. Thin-Film CdS/Cu_2S with High Open-Circuit Voltage and Low Reflection Losses. J. Bragagnolo, R. Birkmire and

3. Introduction

Work on the preceding contract (XR-9-8063-1) had established a good foundation in material preparation for (CdZn)S/Cu_2S solar cells. The highest efficiency achieved was 8.2% at a short-circuit current of 21 mA/cm^2 (pro-rated to 100 mW/cm^2). Building on this foundation, and adjusting the (CdZn)S growth conditions to produce films with the structure, resistivity and photoluminescent behavior known to be essential from the CdS/Cu_2S cell work, it has been possible to increase the conversion efficiency to 10.2% with an open circuit voltage of 0.60V and a short circuit current of 23 mA/cm^2 (pro-rated to 100 mW/cm^2).

Various process changes have been explored in an attempt to improve the CdS/Cu_2S cell beyond the previously achieved 9.2% efficiency level. The major obstacle to such progress is the short circuit current and it has been impossible to increase this beyond 25 mA/cm^2 while maintaining good voltage and fill factor. Detailed statistical data on the influence of various process changes on CdS/Cu_2S cells are reported. The present fundamental knowledge of the optical and electronic properties of Cu_2S is insufficient to direct further current enhancement efforts. It is submitted that a major research effort on Cu_2S should be made with the potential to significantly improve both the efficiency and stability of Cu_2S based cells.

Specific aspects of device operation have been explored using static and transient capacitance techniques. The nature of the CdS/Cu_2S junction has necessitated modification to the capacitance measurement system. A tentative model has been developed to explain the observed effect of bias light and temperature on capacitance.

Development of an integral encapsulant has been continued and some limited data on e-beam encapsulated micro cells are presented.

4. Cell Production, Testing and Analysis

The present program is organized into four tasks - CdS/Cu_2S Cell Development $(CdZn)S/Cu_2S$ Cell Development, Electro-Optical Analysis and Modeling, and Encapsulation for Improved Stability.

Previous development had resulted in a heavily textured CdS/Cu_2S cell of over 9% efficiency[4]. This cell was known to have an open circuit voltage below the ultimately achievable level for the CdS/Cu_2S heterojunction as a consequence of the large junction area. A development effort was therefore directed to reducing the junction area without suffering any loss in current or fill factor. This proved to be impossible and for reasons which remain obscure, a high voltage cell with the same current levels as the 9.2% cell has not been achieved. Measurements indicate that the optical losses of a lightly textured cell with an open circuit voltage of ~ 0.55 V are no greater than the heavily textured cell, nevertheless, the currents achievable fell below the required 25 mA/cm^2. Further basic understanding and control of the Cu_2S layer are seen as essential to make further significant improvements with CdS/Cu_2S.

Progress with the $(CdZn)S/Cu_2S$ cell has been substantial as a result of improving the properties of the (CdZn)S layer. Bimodal grain size distributions were eliminated and this, coupled with improved cell handling procedures, resulted in cells with over 10% conversion efficiency. Open circuit voltage instability was drastically reduced but further development work must be done in this area.

A strong foundation in cell modeling and analysis was established in previous contracts. Much of the recent improvement in cell performance can be traced directly to the benefit of having a comprehensible model of the cell

structure and operation, which can be continually checked against experimental observations. Attention this year has focused on a more detailed understanding of the defects active in the space charge region in the CdS. A variety of capacitance measurements have been carried over a broad temperature range.

Although the major development effort has been directed at improving the initial cell efficiency a preliminary attempt has been made to stabilize the cell against oxidation using an evaporated glass layer. A useful foundation has been laid for a future more intensive stabilization project.

4.1 Development of CdS/Cu_2S Solar Cells

In an attempt to increase the efficiency of the Cu_2S/CdS cells during the past year, four distinct methods of preparing the Cu_2S were tried. These methods were:

1. dry process

   (evaporated CuCl on CdS reacted to Cu_2S)

2. light wet on dry process

   (a dilute concentration wet barrier process was added to the dry)

3. standard wet on dry process

   (same as 2, with standard concentration barrier)

4. standard wet process.

The dry process and the light wet on dry process achieved an efficiency in the 8 to 8.5% range. The standard wet on dry and standard wet process both were limited to the 8.5 to 9.0% range in efficiency. A number of cells were made with the latter two processes to establish yield and control.

I. Dry process Cu_2S/CdS Solar Cells

Thirty-two cells with efficiencies over 7% were made with the dry process from 18 different dry process pieces and 15 different CdS substrates. All pieces were given a 12 to 40 second etch in 20 to 30% HCl at 60°C prior to CuCl evaporation and reaction. Cu_2S thicknesses ranged from 1200 to 2800 Å. In addition, some of the cells were given an evaporated Cu layer, in order to improve the Cu_2S stoichometry and hence the light generated current.

As shown in Table 1* cells without the Cu treatment reached a J_L of 21.8 mA/cm^2 compared to a J_L of 22.1 mA/cm^2 with the Cu treatment. Although the evaporated Cu may improve yield and reproducibility, cells with equivalent J_L can be made without the Cu process. Table 1 also shows a broad maximum of J_L vs Cu_2S thickness centered around 2000 Å.

The cell parameters at maximum efficiency are shown in Table 2. The two parameters that limit the dry process in efficiency here are light generated current ($J_L \leq 22$ mA/cm^2) and series resistance ($R_S \geq 2 \Omega$-cm^2).

With a drop in current of about 10 to 12% and a loss in fill factor of about 2 to 5%, the increase of V_{OC} by 8% still leads to a net drop in efficiency compared to the standard wet process.

The improvements in fill factor and light generated current that result from adding a wet process step, suggest that the failure of the dry process is due to lack of Cu_2S in the rough grain boundary structure of the CdS. EBIC evidence for this is given in reference 1, Figure 2.

* In tables 1 to 5 the following conditions apply

1. All cell tests are at 87.5 mW/cm^2 in an ELH simulator.
2. All cell results are given at maximum efficiency.
3. J_L is normalized to 100 mW/cm^2.
4. V_{OC} is calculated form J_O at a J_L of 25 mA/cm^2.
5. "Successful" AR coating is one which did not decrease the efficiency of the solar cell.

II. Light Wet on Dry Process.

Twenty-six cells with efficiencies of 7% or higher were made with this process from eight different pieces and five different CdS substrates. All pieces were given a 20 second etch in 20 to 25% HCl at 60°C prior to CuCl evaporations. After the dry process Cu_2S was formed, these samples were barriered in a wet barrier bath whose CuCl concentration had been reduced to .05 g/liter from the usual value of 6 gm/liter. Barrier times ranged from 5 to 60 seconds.

There was no relationship between either Cu_2S thickness (1500 Å to 2000 Å as measured electrochemically) or barrier time and any of the cell performance parameters.

Table 3 shows the maximum efficiency cell results for this process. Note that R_S is lower and the fill factor is improved over the dry process cells. Also note that the V_{OC} is about the same. This is probably due to the wet process Cu_2S connecting regions of dry process Cu_2S without penetrating too deeply down grain boundaries. Low J_L still limited these cells so that their efficiency is lower than the standard wet process.

III. Standard Wet on Dry Process

In order to increase the efficiency of the dry process cells, a one second standard wet barrier process was added to the dry. This lowered the V_{OC} to the 0.51 t 0.53V range, but increased J_L to the 23 to 25 mA/cm^2 range which is comparable to the standard wet process cell.

Table 4 shows a listing of all the cells made by this process that had a "successful" AR coating. No relationship between the Cu_2S thickness (as measured by electrochemical analysis) and J_L was seen. For example, Cu_2S thicknesses from 1200 to 3700 Å gave $J_L \sim 23$ mA/cm^2.

This process yielded 70% of the cells over 7% efficiency, 40% over 8%, and 20% over 8.5%. This is somewhat poorer than the standard SEP wet process, but further experience could improve this yield.

IV. Standard Wet (SEP) Process

Table 5 gives a listing of all standard process (substrate evaluation process, SEP) 10 second barrier cells that had a "successful" AR coating during the first quarter of 1980.

The cell efficiencies are comparable to the standard wet on dry process but due to more experience, the yield was better.

95% over 7% efficiency

45% over 8% efficiency

25% over 8.5% efficiency.

Conclusions

Although these four processes did not span all the types of Cu_2S processing that could be done on evaporated CdS, it appears that the limiting efficiency is near 9.5% and is being controlled by the V_{OC} and J_L maxima listed.

The primary obstacle to higher efficiency is the ceiling on J_L of ~ 25 mA/cm^2. All available evidence is that the open circuit votlage for the CdS/Cu_2S

TABLE 1

Dry Process Pieces with Cell Over 7% Efficiency

Cell #	Maximum Efficiency %	J_L/100mW mA/cm	Cu_2S Thickness Å	
21112.12	8.32	22.1	1900	evap. Cu
20968.12	8.01	20.5	1600	
20960.22	7.89	21.2	1800	
21106.12	7.82	20.3	2200	evap. Cu
21007.12	7.66	19.4	1600	
21125.22	7.56	22.1	1800	evap. Cu
20939.12	7.51	18.8	1500	
21044.12	7.41	20.1	~1800*	
20939.21	7.38	19.3	1900	
20966.12	7.31	18.6	1400	
21002.21	7.30	21.8	2100	
21033.21	7.27	19.9	1700	
21111.22	7.25	20.2	2800	evap. Cu
20952.12	7.21	17.8	1200	
21054.12	7.17	21.2	2100	
20966.21	7.11	18.1	1600	
20939.22	7.10	19.1	1600	
20952.21	7.08	18.3	1700	

* = estimated

COLUMN COUNT ROW	SUBSTRATE	CELL #	EFF(%)	J_L (mA/cm^2)	V_{OC}(V)	FF(%)	RS(Ω.cm^2)	Gs(℧cm^2)
1	21112.0	124.	8.32000	22.0900	0.554300	69.3000	3.05000	1.96000
2	21112.0	123.	8.03000	21.1000	0.553700	70.3000	2.68000	2.04000
3	20968.0	121.	8.01000	20.5400	0.551000	72.0000	2.11000	1.74000
4	21112.0	121.	7.93000	20.0700	0.556500	72.5000	2.52000	1.11000
5	20960.0	222.	7.89000	21.2200	0.552600	68.8000	2.61000	2.99000
6	21112.0	122.	7.85000	20.2700	0.562400	70.6000	2.62000	2.20000
7	21106.0	124.	7.82000	20.3300	0.544500	72.2000	2.50000	1.09000
8	20960.0	221.	7.81000	19.2600	0.557500	74.2000	1.69000	1.33000
9	21106.0	122.	7.74000	20.7200	0.539200	70.8000	2.79000	1.29000
10	21007.0	122.	7.66000	19.4100	0.560800	72.1000	2.39000	1.59000
11	21125.0	224.	7.56000	22.0700	0.541100	65.2000	3.97000	3.03000
12	20937.0	122.	7.51000	18.8100	0.565100	72.3000	2.56000	1.28000
13	21044.0	123.	7.41000	20.0500	0.521200	72.5000	2.07000	1.19000
14	20939.0	213.	7.38000	19.2800	0.559100	70.1000	2.92000	1.92000
15	20966.0	124.	7.31000	18.6000	0.559400	71.9000	2.23000	1.86000
16	21002.0	213.	7.30000	21.7800	0.495400	69.2000	2.27000	2.30000
17	20939.0	124.	7.28000	19.0500	0.561600	69.8000	2.92000	2.18000
18	21033.0	213.	7.27000	19.8500	0.553500	68.0000	3.56000	2.25000
19	21111.0	221.	7.25000	20.1500	0.548000	67.7000	3.01000	3.20000
20	20952.0	124.	7.21000	17.7800	0.561600	73.8000	2.09000	1.13000
21	21054.0	123.	7.20000	18.9700	0.529200	73.6000	1.54000	1.54000
22	21111.0	224.	7.18000	19.5800	0.543200	69.5000	2.84000	2.30000
23	21054.0	122.	7.17000	21.1500	0.516500	67.5000	2.93000	2.84000
24	20960.0	224.	7.13000	19.2300	0.553300	68.8000	2.88000	2.74000
25	20966.0	211.	7.11000	18.0500	0.561300	71.9000	2.25000	1.89000
26	20939.0	223.	7.10000	19.1000	0.557800	68.6000	3.05000	2.71000
27	21007.0	124.	7.09000	17.8200	0.562100	72.8000	2.09000	1.70000
28	20952.0	211.	7.08000	18.2500	0.550700	71.9000	2.59000	1.20000
29	21106.0	123.	7.07000	19.1900	0.553500	68.6000	3.42000	2.20000
30	21054.0	121.	7.03000	19.1800	0.522800	72.0000	1.79000	2.02000
31	20968.0	123.	7.01000	18.8000	0.558900	68.6000	2.70000	3.17000
32	20966.0	213.	7.00000	19.1600	0.562200	66.8000	3.94000	2.52000

TABLE 2. Dry Process Cells with Efficiency Over 7%.

COLUMN COUNT ROW	SUBSTRATE	CELL #	EFF(%)	J_L (mA/cm^2)	V_{oc}(V)	FF(%)	RS($\Omega.cm^2$)	Gs(Ω[illegible]
1	21007.0	221.	8.26000	21.1400	0.550900	72.3000	2.31000	1.[illegible]
2	21027.0	122.	8.20000	20.5900	0.557800	72.8000	2.37000	1.[illegible]0
3	21026.0	212.	8.07000	19.7100	0.566700	73.6000	2.16000	1.070[illegible]
4	21027.0	124.	8.05000	20.4500	0.551200	72.8000	2.39000	0.920[illegible]
5	21026.0	214.	8.03000	20.1000	0.568000	72.0000	2.41000	1.710[illegible]
6	21011.0	124.	8.02000	19.5200	0.564300	74.4000	1.92000	1.04000
7	21011.0	122.	7.85000	19.7100	0.558700	72.8000	2.50000	0.97000
8	21007.0	213.	7.81000	19.8900	0.565400	71.1000	2.94000	1.440[illegible]
9	21007.0	222.	7.78000	19.6800	0.563500	71.9000	2.47000	1.650[illegible]
10	21007.0	211.	7.77000	19.8700	0.568200	70.6000	2.23000	2.72000
11	21007.0	214.	7.74000	19.7100	0.570600	70.6000	2.95000	1.85000
12	21007.0	212.	7.73000	19.1800	0.569000	72.6000	2.48000	1.370[illegible]
13	21007.0	224.	7.67000	19.5200	0.557100	72.2000	2.63000	1.160[illegible]
14	21011.0	121.	7.65000	19.0700	0.560600	73.2000	2.48000	0.92000
15	21011.0	213.	7.65000	18.6400	0.561800	74.7000	2.03000	0.76000
16	21007.0	223.	7.63000	18.7700	0.566600	73.5000	2.20000	1.220[illegible]
17	21011.0	211.	7.63000	18.3900	0.561000	75.6000	1.77000	0.650[illegible]
18	21011.0	214.	7.63000	19.7700	0.554900	71.4000	2.31000	2.040[illegible]
19	21026.0	211.	7.48000	19.9000	0.565300	68.4000	3.27000	2.62000
20	21011.0	223.	7.41000	18.7500	0.548100	73.8000	1.95000	1.100[illegible]
21	21011.0	224.	7.38000	19.2200	0.546700	72.0000	2.47000	1.360
22	21027.0	123.	7.24000	18.2500	0.556500	73.1000	2.38000	1.070
23	21009.0	211.	7.21000	18.3400	0.553300	72.8000	2.55000	0.97000
24	21027.0	121.	7.18000	19.3300	0.559400	68.6000	2.67000	3.25000
25	21011.0	221.	7.15000	18.7700	0.539100	72.6000	2.05000	1.520
26	21009.0	212.	6.95000	17.5100	0.552800	73.8000	2.09000	1.100

TABLE 3. Light Wet on Dry Process Cells with Efficiencies of 7% or Greater.

COLUMN COUNT ROW	SUBSTRATE	CELL #	EFF(%)	J_L (mA/cm^2)	V_{OC}(V)	FF(%)	RS($\Omega \cdot cm^2$)	Gs($\mho/cm^2$)
1	21105.0	213.	8.96000	24.1100	0.522000	72.1000	1.81000	1.60000
2	21110.0	224.	8.96000	23.9100	0.514700	73.7000	1.39000	1.29000
3	21103.0	213.	8.87000	23.6700	0.519400	73.0000	1.76000	1.03000
4	21103.0	211.	8.83000	23.9700	0.522000	71.5000	2.12000	1.28000
5	21119.0	213.	8.79000	25.0200	0.519000	68.9000	2.11000	3.29000
6	21103.0	223.	8.78000	24.1800	0.523300	70.3000	2.47000	1.37000
7	21114.0	213.	8.78000	23.2600	0.519700	73.6000	1.64000	0.94000
8	21103.0	212.	8.75000	24.1000	0.520700	70.7000	2.22000	1.62000
9	21119.0	212.	8.74000	24.7300	0.520600	69.1000	2.15000	3.07000
10	21114.0	211.	8.72000	22.8800	0.523500	73.9000	1.44000	1.30000
11	21112.0	214.	8.71000	23.2900	0.520100	72.9000	1.71000	1.29000
12	21114.0	212.	8.70000	23.1800	0.518000	73.6000	1.41000	1.48000
13	21112.0	213.	8.65000	23.5400	0.515900	72.3000	1.63000	1.79000
14	21113.0	223.	8.63000	23.9300	0.507100	72.1000	1.52000	1.99000
15	21110.0	214.	8.60000	23.5200	0.517700	71.7000	1.86000	1.72000
16	21103.0	123.	8.59000	23.1900	0.521600	72.1000	1.83000	1.63000
17	21105.0	123.	8.56000	23.5800	0.514900	71.6000	1.81000	1.88000
18	21103.0	222.	8.54000	23.3400	0.523500	71.0000	2.15000	1.71000
19	21103.0	121.	8.52000	23.1100	0.518700	72.2000	1.66000	1.90000
20	21113.0	221.	8.49000	23.9400	0.501700	71.6000	1.77000	1.62000
21	21103.0	214.	8.48000	22.6300	0.522200	72.9000	1.82000	1.16000
22	21114.0	214.	8.47000	22.6500	0.517600	73.4000	1.49000	1.45000
23	21103.0	221.	8.45000	22.7700	0.526200	71.8000	1.86000	1.93000
24	21109.0	121.	8.44000	23.3700	0.508800	72.1000	1.64000	1.82000
25	21105.0	124.	8.40000	23.5200	0.511700	71.0000	1.97000	1.90000
26	21110.0	221.	8.40000	23.1000	0.517200	71.5000	1.98000	1.68000
27	21105.0	121.	8.39000	23.9300	0.511400	69.7000	2.14000	2.45000
28	21113.0	123.	8.39000	23.1800	0.506300	72.5000	1.73000	1.20000
29	21119.0	214.	8.36000	23.8200	0.523800	68.5000	2.04000	3.89000
30	21103.0	224.	8.35000	21.6200	0.532300	73.8000	1.64000	1.21000
31	21113.0	224.	8.32000	23.8600	0.509300	69.8000	1.80000	3.15000
32	21103.0	124.	8.31000	21.8600	0.525900	73.4000	1.88000	0.85000
33	21113.0	214.	8.30000	24.0200	0.509300	69.2000	1.89000	3.39000
34	21110.0	222.	8.26000	23.5000	0.515000	69.6000	1.90000	3.18000
35	21121.0	214.	8.24000	23.0700	0.516800	70.3000	2.50000	1.33000
36	21105.0	224.	8.20000	22.6200	0.517800	71.3000	2.02000	1.78000
37	21103.0	122.	8.19000	22.4000	0.516800	72.0000	1.95000	1.45000
38	21105.0	122.	8.15000	23.1000	0.511300	70.3000	2.04000	2.30000
39	21112.0	212.	8.12000	22.9100	0.518200	69.6000	2.41000	2.06000
40	21113.0	212.	8.12000	22.4500	0.516800	71.3000	2.17000	1.45000
41	21113.0	211.	8.10000	23.0700	0.520300	69.0000	1.87000	3.79000
42	21113.0	124.	8.00000	22.9600	0.514200	69.2000	1.98000	3.30000
43	21114.0	224.	7.97000	22.2200	0.502300	72.7000	1.34000	1.91000
44	21092.0	222.	7.92000	23.1200	0.496100	70.2000	2.12000	1.73000
45	21109.0	212.	7.91000	22.2900	0.524800	69.2000	2.17000	3.11000
46	21113.0	121.	7.87000	22.0700	0.507700	71.6000	1.94000	1.56000
47	21105.0	221.	7.77000	22.0200	0.515500	69.9000	2.33000	2.13000
48	21113.0	122.	7.77000	22.4200	0.506300	69.9000	2.17000	2.25000
49	21092.0	221.	7.76000	23.0400	0.494500	69.3000	2.39000	1.75000
50	21111.0	213.	7.75000	21.7100	0.509500	71.4000	2.19000	1.24000
51	21101.0	213.	7.75000	21.4700	0.517100	71.2000	2.22000	1.53000
52	21092.0	212.	7.73000	22.8500	0.508900	68.1000	2.53000	2.88000
53	21121.0	213.	7.73000	22.7700	0.520100	67.0000	2.44000	4.13000
54	21111.0	211.	7.72000	21.8600	0.505800	71.1000	2.22000	1.30000
55	21114.0	222.	7.72000	21.8600	0.500700	72.0000	1.47000	2.16000
56	21113.0	222.	7.69000	21.1500	0.511700	72.4000	2.01000	1.05000
57	21092.0	214.	7.67000	22.7700	0.507600	68.0000	2.44000	3.14000
58	21101.0	212.	7.65000	20.3700	0.525200	73.1000	1.82000	1.31000
59	21101.0	124.	7.62000	19.5200	0.535800	74.4000	1.56000	1.13000
60	21110.0	213.	7.60000	23.0500	0.520700	65.2000	3.05000	4.32000

TABLE 4. All Cells from the Standard Wet on Dry Process Ordered with Respect to Efficiency.

	SUBSTRATE	CELL #	EFF(%)	J_L (mA/cm^2)	V_{OC}(V)	FF(%)	RS(Ω.cm^2)	Gs(℧cm…
61	21112.0	211.	7.60000	22.2600	0.514400	68.0000	2.69000	2.[illegible]0
62	21101.0	122.	7.52000	19.4200	0.533400	74.2000	1.79000	0.8900
63	21094.0	214.	7.49000	21.9100	0.507500	69.0000	2.28000	2.7800
64	21121.0	121.	7.38000	21.6800	0.520000	67.0000	3.44000	2.0900
65	21105.0	214.	7.33000	22.9800	0.528200	62.9000	2.68000	7.06000
66	21113.0	213.	7.33000	21.7400	0.521900	66.5000	2.87000	3.7500
67	21094.0	212.	7.31000	19.8200	0.515800	73.2000	1.52000	1.5600
68	21114.0	221.	7.29000	20.9900	0.498200	71.3000	1.62000	2.2800
69	21114.0	223.	7.23000	21.3600	0.499500	69.5000	1.69000	3.41000
70	21121.0	124.	7.22000	21.0100	0.525200	67.2000	3.34000	2.46000
71	21108.0	224.	7.13000	20.5300	0.525200	68.0000	2.87000	2.8100
72	21108.0	122.	7.01000	20.4900	0.520100	67.6000	3.16000	2.4500
73	21108.0	121.	6.86000	20.1500	0.522700	67.0000	3.54000	2.27000
74	21095.0	221.	6.82000	19.0900	0.511800	71.7000	2.00000	1.67000
75	21095.0	124.	6.80000	22.3000	0.498900	63.4000	3.28000	4.9400
76	21121.0	223.	6.71000	18.4500	0.516500	72.4000	2.03000	1.3200
77	21092.0	211.	6.68000	21.5800	0.507900	63.4000	3.31000	5.1600
78	21101.0	123.	6.66000	19.2100	0.507300	70.2000	2.51000	1.68000
79	21121.0	222.	6.64000	18.3000	0.520200	71.7000	2.08000	1.660
80	21121.0	211.	6.62000	19.5900	0.518700	67.4000	2.65000	3.500
81	21101.0	121.	6.56000	19.2100	0.517600	68.1000	3.27000	2.070
82	21108.0	222.	6.50000	19.4700	0.520400	66.3000	3.66000	2.69000
83	21121.0	221.	6.45000	18.0600	0.517600	71.0000	2.54000	1.44000
84	21105.0	223.	6.31000	18.3700	0.525500	67.9000	2.18000	3.860
85	21110.0	211.	6.31000	22.8600	0.517300	56.7000	5.28000	7.580
86	21108.0	124.	6.30000	21.5700	0.519900	59.2000	4.90000	6.06000
87	21105.0	222.	6.10000	21.7800	0.524700	57.0000	3.56000	9.99000
88	21108.0	221.	5.74000	18.2700	0.523600	62.8000	4.94000	3.550
89	21108.0	123.	5.72000	20.7100	0.524100	56.4000	5.89000	7.170
90	21095.0	123.	5.45000	18.1700	0.526500	60.4000	4.92000	5.4000
91	21105.0	211.	5.41000	19.1300	0.534700	56.8000	4.29000	8.83000
92	21108.0	223.	5.29000	16.7000	0.528200	63.1000	4.90000	3.6500
93	21110.0	212.	4.54000	14.0800	0.508100	66.8000	3.90000	2.420
94	21109.0	211.	4.45000	13.7700	0.514900	66.2000	4.35000	2.460
95	21095.0	224.	4.40000	14.9500	0.522400	60.4000	4.49000	5.52000
96	21095.0	223.	4.38000	14.0300	0.538400	61.9000	3.98000	4.98000
97	21109.0	213.	4.28000	14.7400	0.515100	60.3000	6.20000	4.110
98	21105.0	212.	4.20000	14.4700	0.519300	59.8000	7.28000	3.480
99	21110.0	223.	3.62000	10.1600	0.515200	73.2000	2.62000	0.78000
100	21119.0	211.	0.04000	0.0000	0.000000	25.2000	9.99000	9.99000
101	21109.0	123.	0.02000	0.0000	0.000000	24.9000	9.99000	9.990
102	21109.0	124.	0.02000	0.0000	0.000000	25.4000	9.99000	9.990

TABLE 4 Continued: All Cells from the Standard Wet on Dry Process Ordered with Respect to Efficiency.

COLUMN COUNT ROW	SUBSTRATE	CELL #	EFF(%)	J_L (mA/cm^2)	V_{oc}(V)	FF(%)	RS(Ω.cm^2)	G_s(mΩ·cm^2
1	21113.0	112.	8.90000	23.1400	0.523800	75.0000	1.27000	0.90000
2	21105.0	114.	8.85000	22.8100	0.530200	74.2000	1.46000	1.15000
3	21114.0	114.	8.82000	23.4300	0.518700	73.6000	1.46000	1.34000
4	21122.0	114.	8.81000	24.7800	0.520100	69.4000	2.34000	2.28000
5	21102.0	111.	8.80000	23.9300	0.518500	71.9000	1.84000	1.61000
6	21102.0	113.	8.79000	23.9100	0.521900	71.4000	2.15000	1.29000
7	21094.0	111.	8.77000	24.7900	0.508800	70.5000	2.07000	1.82000
8	21110.0	112.	8.75000	22.7400	0.523600	74.5000	1.34000	1.10000
9	21119.0	111.	8.73000	23.6700	0.518300	72.1000	1.89000	1.35000
10	21114.0	112.	8.72000	24.3200	0.520200	70.0000	2.22000	2.15000
11	21127.0	113.	8.69000	23.8100	0.526800	70.5000	2.06000	2.41000
12	21128.0	111.	8.68000	24.4500	0.522400	69.2000	2.20000	2.90000
13	21106.0	112.	8.61000	23.3000	0.519500	72.2000	1.97000	1.21000
14	21106.0	114.	8.57000	22.8600	0.518100	73.4000	1.59000	1.22000
15	21092.0	112.	8.55000	23.8300	0.509800	71.3000	2.07000	1.26000
16	21109.0	112.	8.53000	22.6100	0.517900	73.9000	1.61000	0.83000
17	21108.0	112.	8.51000	23.0900	0.518100	72.3000	1.60000	1.93000
18	21112.0	114.	8.50000	23.8200	0.526100	69.1000	2.42000	2.58000
19	21122.0	112.	8.45000	24.7300	0.518000	67.4000	2.47000	3.66000
20	21120.0	113.	8.44000	23.3800	0.513000	71.4000	2.08000	1.36000
21	21088.0	111.	8.35000	23.1000	0.517800	71.0000	2.21000	1.53000
22	21101.0	113.	8.35000	22.5800	0.517300	72.6000	1.90000	1.08000
23	21131.0	111.	8.34000	22.9000	0.529200	70.1000	2.40000	2.08000
24	21103.0	114.	8.32000	23.2700	0.515800	70.6000	1.84000	2.58000
25	21113.0	114.	8.30000	23.1900	0.526000	69.5000	1.84000	3.57000
26	21092.0	114.	8.25000	22.5400	0.509100	72.9000	1.90000	0.66000
27	21088.0	113.	8.24000	22.7200	0.517300	71.3000	2.20000	1.33000
28	21106.0	113.	8.24000	21.8500	0.516400	74.2000	1.51000	0.86000
29	21125.0	114.	8.15000	23.1800	0.526500	68.3000	2.53000	3.06000
30	21103.0	111.	8.14000	22.0200	0.519600	72.3000	2.01000	1.14000
31	21110.0	114.	8.14000	22.1600	0.523400	71.6000	1.90000	2.00000
32	21125.0	111.	8.13000	22.6900	0.528200	69.3000	2.43000	2.57000
33	21115.0	112.	8.09000	21.3300	0.531900	72.8000	1.62000	1.90000
34	21105.0	112.	8.07000	21.1200	0.525100	74.1000	1.63000	0.94000
35	21108.0	111.	8.02000	21.7800	0.513400	73.0000	1.70000	1.26000
36	21111.0	114.	8.01000	21.5700	0.516900	73.3000	1.54000	1.46000
37	21100.0	111.	7.99000	22.4900	0.519700	69.7000	2.61000	1.73000
38	21093.0	111.	7.96000	21.9100	0.508100	72.7000	1.76000	1.14000
39	21102.0	114.	7.93000	22.7500	0.519300	68.6000	2.27000	3.24000
40	21125.0	113.	7.93000	22.4100	0.532800	68.0000	2.93000	2.66000
41	21092.0	113.	7.91000	21.6700	0.508100	73.1000	1.72000	0.99000
42	21120.0	114.	7.90000	23.1700	0.509900	68.4000	2.15000	3.48000
43	21120.0	111.	7.88000	23.2000	0.507200	68.3000	2.63000	2.32000
44	21095.0	113.	7.85000	23.5400	0.516800	66.0000	3.27000	2.91000
45	21085.0	113.	7.84000	21.3500	0.512000	73.1000	1.59000	1.39000
46	21110.0	113.	7.83000	21.8300	0.511300	71.5000	2.07000	1.44000
47	21131.0	112.	7.82000	22.5600	0.528500	67.2000	3.06000	2.89000
48	21120.0	112.	7.81000	23.7400	0.504900	66.6000	2.89000	2.96000
49	21085.0	111.	7.80000	21.6500	0.513600	71.5000	2.13000	1.36000
50	21093.0	113.	7.80000	21.8600	0.507800	71.6000	2.13000	1.17000
51	21093.0	114.	7.78000	22.3400	0.509000	69.8000	2.28000	2.09000
52	21092.0	111.	7.72000	21.6400	0.511100	72.5000	2.73000	0.67000
53	21088.0	114.	7.71000	21.8600	0.512300	70.4000	1.95000	2.50000
54	21093.0	112.	7.68000	21.5100	0.510600	71.3000	2.21000	1.30000
55	21121.0	113.	7.68000	21.9900	0.525400	68.2000	2.52000	3.22000
56	21106.0	111.	7.66000	21.4400	0.506500	71.9000	1.97000	1.27000
57	21115.0	111.	7.66000	21.5500	0.535000	68.3000	2.38000	3.60000
58	21085.0	114.	7.65000	21.4700	0.508100	71.4000	2.22000	1.13000
59	21088.0	112.	7.65000	21.4600	0.511900	71.2000	1.89000	2.10000
60	21100.0	113.	7.62000	21.6800	0.521400	69.1000	2.30000	2.94000

TABLE 5. All Standard Process SEP Cells Made During January, 1980 Through March, 1980 Ordered with Respect to Efficiency.

	SUBSTRATE	CELL #	EFF(%)	J_L (mA/cm^2)	V_{oc}(V)	FF(%)	RS($\Omega.cm^2$)	Gs ($m\Omega cm^2$)
61	21130.0	114.	7.59000	23.8900	0.507800	64.4000	3.12000	4.51
62	21103.0	114.	7.56000	21.9800	0.501000	70.0000	2.31000	1.72000
63	21121.0	114.	7.51000	21.3700	0.514700	69.9000	2.12000	2.56000
64	21121.0	111.	7.48000	21.7700	0.516100	68.3000	2.43000	3.17000
65	21110.0	111.	7.38000	20.5300	0.509700	72.2000	1.82000	1.57000
66	21100.0	112.	7.34000	20.4100	0.519400	70.8000	2.52000	1.41000
67	21095.0	111.	7.29000	21.8500	0.512000	66.9000	3.08000	2.81000
68	21112.0	112.	7.28000	20.6300	0.505100	71.5000	1.86000	1.82000
69	21087.0	114.	7.25000	22.3400	0.505500	66.0000	2.90000	3.69000
70	21087.0	112.	7.15000	21.3500	0.498000	68.9000	2.39000	2.39000
71	21121.0	112.	7.13000	20.8200	0.508100	69.2000	2.21000	2.78000
72	21115.0	114.	7.04000	21.6200	0.534200	63.3000	3.98000	4.51000
73	21085.0	112.	7.00000	19.3800	0.510900	72.5000	1.81000	1.46000
74	21128.0	113.	6.98000	19.8300	0.534000	68.1000	2.16000	3.93000
75	21109.0	114.	6.93000	21.1800	0.519300	65.2000	3.02000	4.43000
76	21087.0	113.	6.43000	20.9100	0.496100	64.4000	2.78000	5.07000
77	21130.0	112.	6.14000	18.8500	0.525500	64.6000	3.67000	4.02000

TABLE 5 Continued: All Standard Process SEP Cells Made During January, 1980 Through March, 1980 Ordered with Respect to Efficiency.

heterojunction is limited to 0.55V. The known optical losses do not match the achieved currents and it is considered unlikely that further improvements in CdS/Cu_2S cell performance will be possible until better fundamental understanding and control of Cu_2S is achieved.

Other Process Studies

In addition to the Cu_2S formation procedures explored during the year a number of other investigations were conducted. These are described in the following sections.

Growth of CdS on the Smooth Side of the Copper Foil.

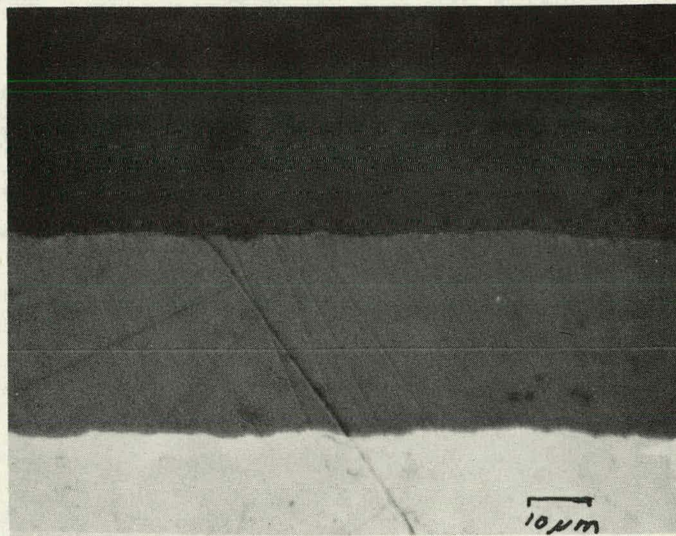
CdS was grown on the smooth side of the copper foil rather than the usual matte side in an attempt to reduce the grid spacing which is effectively increased by the roughness of the CdS surface. Figure 1 shows cross-sections of CdS grown on both the matte and smooth side of the copper substrate. The surface of the CdS on the smooth side is much flatter than on the matte and thus the effective grid spacing should be reduced. Twenty-seven substrates were grown on the smooth side to determine optimal growth conditions and to evaluate cell performance. The following results were obtained:

1. Adherance of the CdS was not as good as on the matte side and difficulties in cell fabrication were encountered. Also, the curl of the substrate, due to the thermal expansion mismatch between the CdS and copper, was more severe since the natural curl of the copper foil was in the same direction.
2. Resistivity and photoluminescence characteristics of the CdS were similar to those of CdS grown on the rough side.

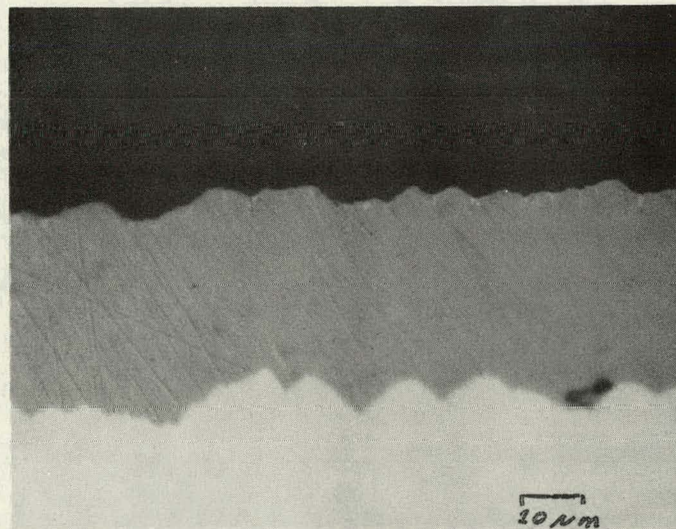
3. Grain sizes were somewhat smaller than on the rough side CdS and were in the range of 2-2.5 μm.

4. Cell results were similar to cells fabricated on the rough side CdS for both wet and dry processed cells. See Table 6. The improvement in fill factor anticipated due to an effective reduction in grid spacing was not realized.

5. The total reflectivity for both rough and smooth side cells that were wet barriered and given an antireflection coating was identical. The average solar weighted reflection was 6%.



(a)



(b)

Figure 1. Optical micrographs of a cross-section of CdS grown on: (a) the smooth side of the copper, (b) the matte side of the copper.

TABLE 6

SMOOTH SIDE COPPER CELLS

CELL #	V_{OC}(V) (at 25mA/cm^2)	J_L (mA/cm^2) (at 100mW/cm^2)	FF(%)	Eff(%)	COMMENT
21085.213	0.516	22.51	70.1	8.0	Wet - no AR Highest Efficiency
21054.112	0.465	24.88	62.5	7.95	Wet - AR Highest current
21044.123	0.521	20.05	72.5	7.41	Dry - AR Highest Efficiency

The growth of CdS on the smooth side of the copper substrate was abandoned since no improvement in cell performance was realized and extra difficulties in cell fabrication were created.

Multilayer Grid

Preliminary experiments have been performed using a multilayer grid structure to reduce the amount of gold being utilized. Between 0.2 and 0.5 μm of gold were deposited to give good ohmic contact to the Cu_2S. A layer of nickel, 0.2 to 0.5 μm thick, is then deposited to act as a diffusion barrier between the gold and the final copper layer. The copper is 2.5 μm thick and is needed to minimize the series resistance of the grid structure. Depositions were conducted sequentially without breaking vacuum using a turret e-gun system. Cells fabricated using this grid structure had in general poor fill factors and the I-V characteristics suggest high Cu_2S stiochiometry. Examination of a cross-section of a grid line showed that copper was being deposited beyond the Au-Ni layers and was in contact with the Cu_2S. It is believed that the evaporation mask sagged during

the copper deposition due to radiant heating from the copper source. This problem should be solved by a new grid-mask mounting system currently being developed coupled with better control of the copper deposition.

H_2 Plasma Treatments

Preliminary experiments were performed on the use of H_2 plasmas to modify the stoichiometry of the Cu_2S for cell optimization. The goals were two fold; (i) minimize the time required for optimizing cells, and (ii) separate the atmosphere and temperature effects in the current heat treatment optimization procedure. A detailed report of these experiments can be found in reference 2.

To summarize the results, both RF and DC plasmas were used. After H_2 plasma treatment, the cells showed a collapsed I-V curve indicative of highly stoichiometric Cu_2S. A good fill factor could be recovered by an air or O_2 plasma treatment. The light generated current for the plasma treated cells was always lower than would be expected by conventional reducing heat treatments.

Further work to optimize the plasma reduction of Cu_2S has not been pursued, since no improvement of cell performance was realized and also additional equipment would be required. However, plasma reduction may be important in the development of commercial production technology, since it has the potential of significantly reducing the amount of time necessary to optimize cell performance.

4.2 $(CdZn)S/Cu_2S$ Solar Cell Development

As of the beginning of the contract year the best $Cd_{1-x}Zn_xS/Cu_2S$ cell had a conversion efficiency of 8.2% at an open circuit voltage of 572mV (zinc concentration x = .09.) Table 7 shows specific data for that cell in comparison to the cell performance parameters of the best CdS cell, and the design parameters for a (CdZn)S cell operating at 600mV.

TABLE 7

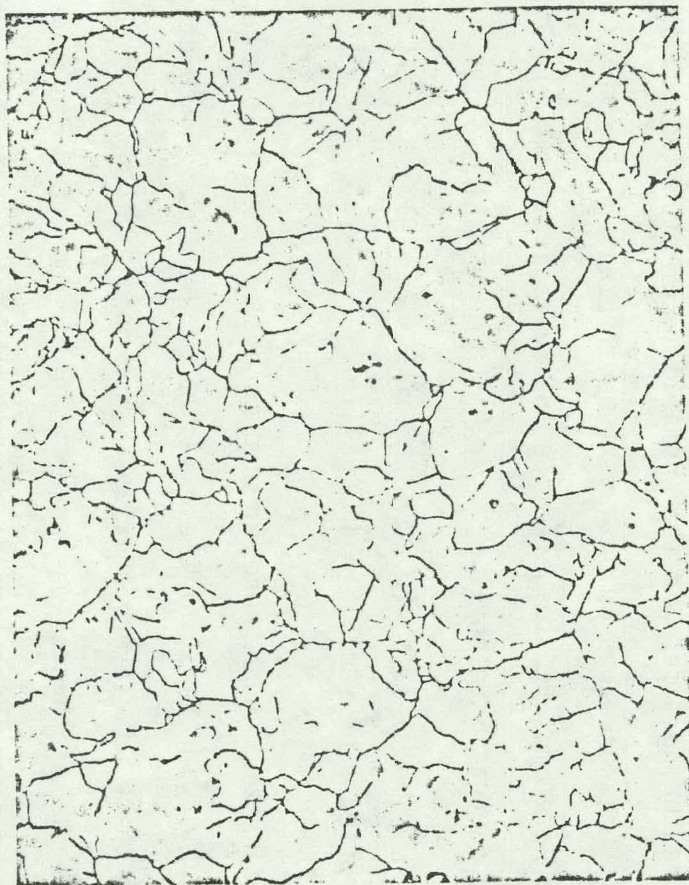
Best Performance CdS and (CdZn)S Cells - September 1979

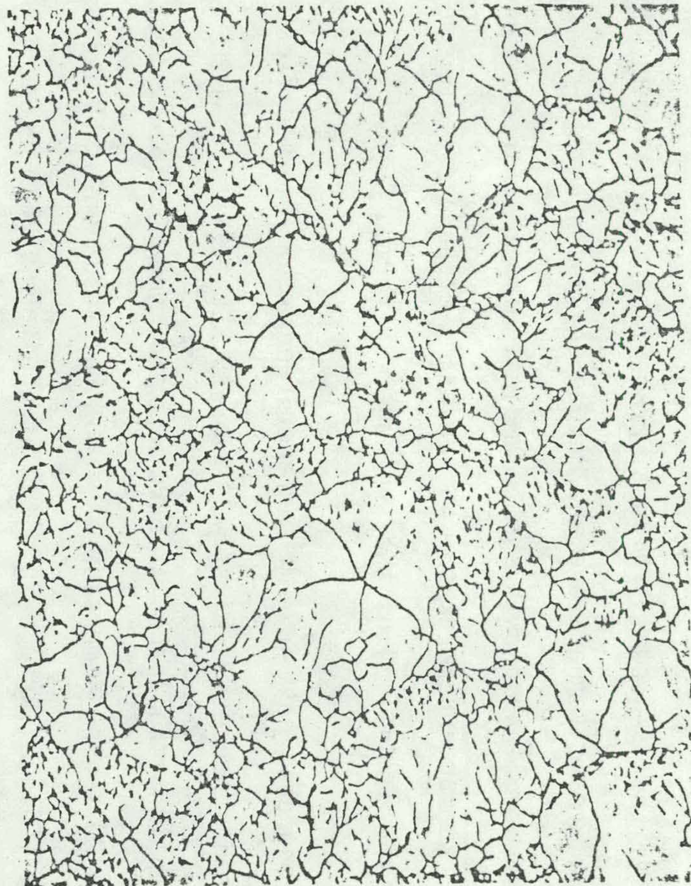
	V_{OC} (mV)	J_L ($\frac{mA}{cm^2}$)	FF(%)	Eff(%)	G_{SH} (m /cm^2)
(CdZn)S x = 0.09 (Best Device)	572	20.9	68.5	8.2	3.20
CdS (Best Device)	516	24.8	71.4	9.2	1.34
(CdZn)S (Design)	600	25.5	71	10.9 11.5	

The two specific device parametrs which fell below design were the light generated current and the fill factor. The light generated current for the best $(CdZn)S/Cu_2S$ device was about 4 mA/cm^2 less than that observed on the best reported CdS/Cu_2S device[4]. The fill factor was lower than design largely as a consequence of high device shunt conductance. Additionally, these devices were found to be unstable as exemplified by the fact that V_{OC} would decay in excess of 100 mV after 15 minutes of illumination. The degree of instability was found to depend on the method of Cu_2S formation.

Figure 2 is an SEM micrograph revealing a feature of the (CdZn)S film quality which differs from that observed in CdS yielding high efficiency cells. The grain structure, revealed by forming and then a removing Cu_2S layer, indicated a bimodal distribution of grain sizes. This bimodal structure is deleterious as it reduces device V_{oc} due to enhanced junction area in the small grained regions, and because the small grained areas result in a highly intrusive Cu_2S morphology.

It was the issue of Cu_2S morphology which directed the initial effort to address the problems of low fill factor (high shunt conductances) and device stability. To a first order the Cu_2S morphology depends on the method of Cu_2S formation and the quality of the (CdZn)S film. The formation of Cu_2S by vacuum evaporation(5) on IEC (CdZn)S has yielded devices which indicate no V_{oc} decay after 30 minutes of illumination. However, device efficiency was only 4%, 35% less than achieved on the same (CdZn)S substrate using Cu_2S formed by the wet process. Specifically, the achieved light generated currents (13 mA/cm^2) were 3-4 mA/cm^2 below that realized with wet process Cu_2S, and the fill factors were $\lesssim$ 65%. Although promising from a stability standpoint, development of this formation process seemed inappropriate for the present. The formation of Cu_2S by the dry process ion exchange yielded devices with conversion efficiencies in excess of 6%(1). The increase in V_{oc} attending the reduction in junction area, which is realized using the dry process, was observed, although the light generated currents were typically 15% less than achieved with the wet process. Furthermore, despite the less intrusive morphology obtained with the dry process, the subsequently fabricated devices were still found to be unstable, albeit less so than with the wet process. Therefore, it is decided to deal with the other aspect influencing Cu_2S morphology, the (CdZn)S film quality.





10μm

Figure 2. SEM micrograph shows the grain revealed film surface of; a) CdS, and b) (CdZn)S.

The Cu_2S morphology is affected by two aspects of (CdZn)S film quality: the as-grown structural properties, and the post-growth surface preparation. Specifically, the as-grown structural properties are determined by substrate effects, (substrate temperature and morphology,) source effects (growth rate, beam homogeneity,) and growth system ambient (impurity incorporation.) Any post-growth surface preparation, as for example surface texturing, also influences the morphology of the subsequently formed Cu_2S.

With regard to post-growth surface preparation two modifications were made to the existing process. Firstly, prior to the texturing step, a one minute rinsing step in microcleaner at 60°C was employed to cleanse the surface. Secondly, a 20 second immersion in a 25% HCl solution at 60°C was used to texture the (CdZn)S surface in place of the former one second immersion in a 55% HCl solution at 60°C. This latter modification was employed to reduce both errors in texturing time, and the possibility of etch induced shunts. Optical reflectivity measurements on both textured (CdZn)S and textured (CdZn)S with a Cu_2S layer were employed to determine the sufficient texturing time using the reduced concentration etch[1].

Substrate Effects on (CdZn)S Film Quality

Two separate avenues were pursued to explore substrate effects on (CdZn)S films quality. The first of these was to grow a 10-20μm thick (CdZn)S film on a 20-25μm thick CdS layer, previously grown on a zinc plated copper substrate. This bilayer film approach was undertaken in order to promote uniform (CdZn)S grain sizes by providing similar structured, large grain CdS as the substrate for the (CdZn)S. Figure 3 shows the SEM micrographs of the grain structure of

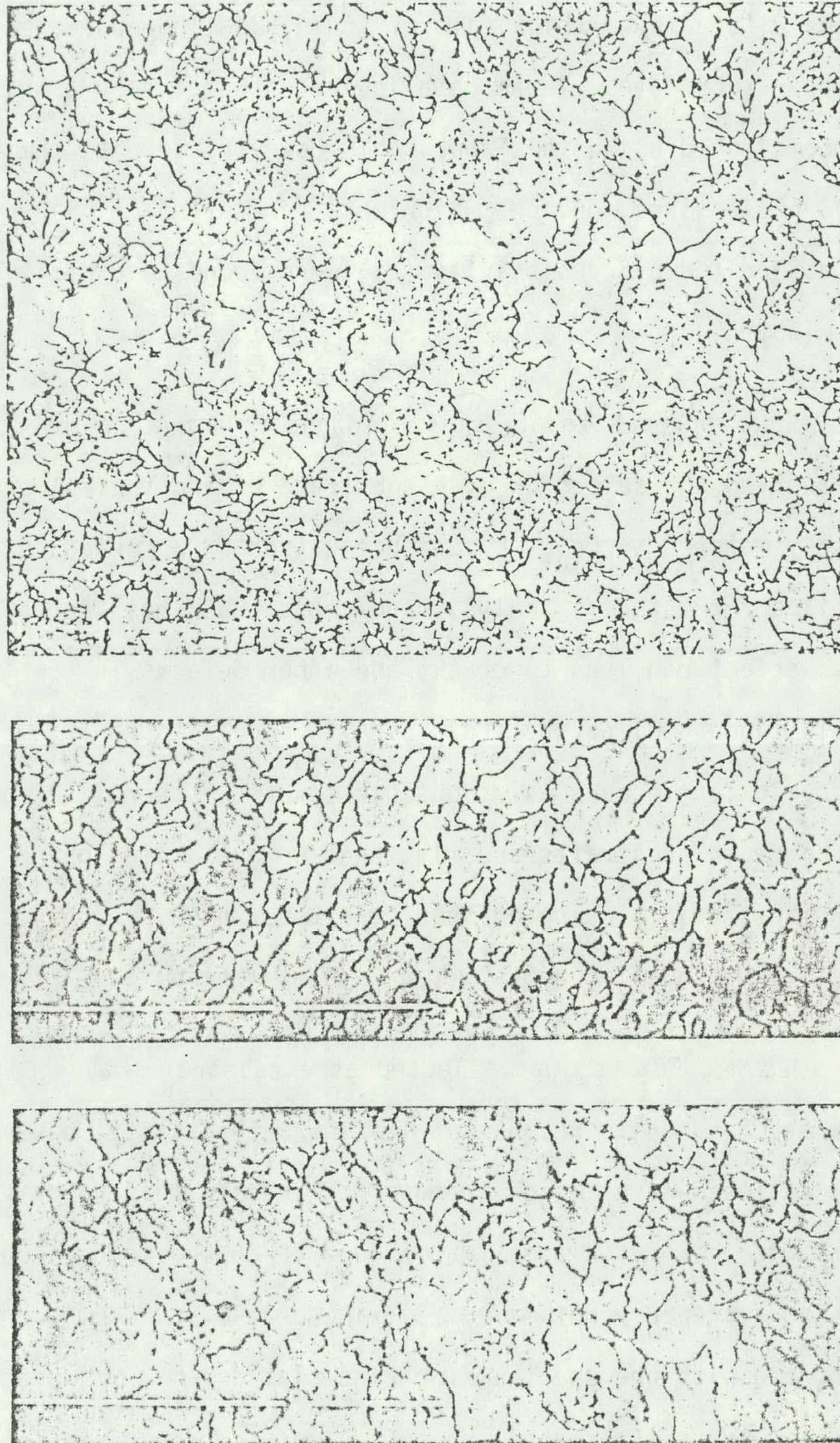


Figure 3. SEM micrograph shows the grain revealed surfaces of: a) a 20μm thick single layer (CdZn)S film, b) a 17μm thick single layer of CdS, and c) same as (b) with 16μm thick film of (CdZn)S deposited on it.

a) a single layer (CdZn)S film, b) a 17μm thick single layer of CdS, and c) same as (b) with a 16μm thick film of (CdZn)S, all prepared on the same zinc plated copper substrate. These data indicate that indeed a uniform grain size can be accomplished using this approach. However, despite the uniform structure of (CdZn)S grain sizes, devices which were fabricated on bilayers having the desired CdS and (CdZn)S resistivity (2), were found to exhibit V_{OC} decay ($\sim$60 mV in 30 minutes.)

The second approach to affecting (CdZn)S film quality by considering substrate effects involved the selection of a substrate having thermal expansion properties more closely matched to CdS. Experience gained as a consequence of preparing (CdZn)S films for material analysis indicates that they are more brittle than CdS. This effect can lead to cracks and other defects in the (CdZn)S films. For example, upon cooling the (CdZn)S Cu/Zn couple to room temperature after CdS deposition, curling occurs as a consequence of the thermal expansion mismatch. Samples from such substrates are flattened several times prior to the formation of Cu_2S. It is this flexing of the (CdZn)S Cu/Zn couple that could lead to defects yielding shunting paths after Cu_2S formation.

NiFe (42% N_i, 58% Fe) was selected as a substrate having a suitable thermal expansion match to CdS. Because of its low reflectivity, however, it is necessary to employ an inter-layer which promotes the substrate reflectivity that is necessary for optimal device performance[6]. Figure 4 shows a comparison of the reflectivity spectrum for a properly optimized (3) zinc-plated (~0.5μm), copper-plated (~4.0μm) NiFe substrate with the spectrum for zinc plated (~0.3μm) copper (rough side). Both samples were heat-treated for sufficient time to ensure no further spectral change occurred as a consequence of copper/zinc interdiffusion. The solar weighte

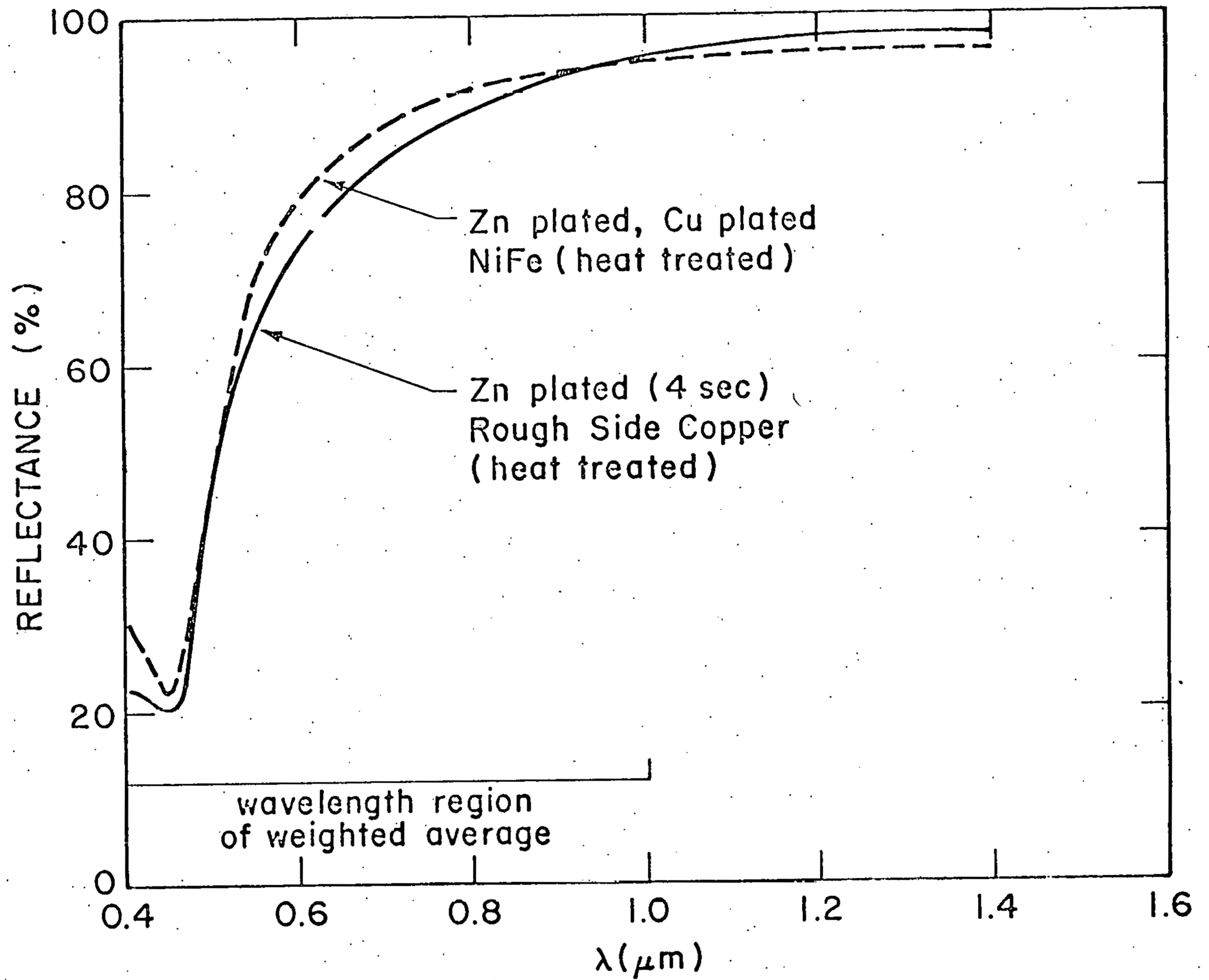


Figure 4. Reflectivity Spectra for optimized zinc-plated, copper plated NiFe substrate and zinc plated rough side copper,

average reflectance from the NiFe (Cu/Zn) substrate was 78% as compared to 75% from the Cu(Zn) substrate. Results of devices prepared on these substrates will be presented later.

The initial depositions of (CdZn)S on NiFe with thin ($\lesssim 1$ μm) Cu-Zn layers yielded films with unformly small (< 1 μm) grain sizes. Devices fabricated on this material had fill factors $\lesssim$ 65%, and low light generated currents, mostly attributable to inadequate substrate reflection. These devices exhibited conversion efficiencies of only 4.5%, but were found to hold at a constant V_{OC} (580 mV) for 30 minutes at 45°C. Utilization of the bilayer approach on NiFe substrates resulted in larger (CdZn)S grains ($\sim$ 1-2 μm), but did not result in appreciable device efficiency gains.

Effects of Growth System Improvements on (CdZn)S Film Quality

In order to be able to prepare bilayer films without breaking vacuum between depositions the (CdZn)S growth bell jar was modified. In addition to routine maintenance and a particular attention to vacuum integrity, several system improvements were implemented. These included the installation of two separate sources for the sequential growth of CdS and (CdZn)S, and the installation of the capability to control the temperature of the substrate using a thermocouple spot welded directly to it.

After the system improvements were implemented, several bilayer films on copper substrates were prepared. The efficiency results of cells fabricated on this material did not exceed those prepared prior to system improvements, and the devices still exhibited V_{OC} decay.

Several single layer (CdZn)S films were prepared on both NiFe and copper substrates. The striking feature about these films was that they exhibited a uniform distribution of grain sizes (~1-2 μm). Figure 5 and 6 show the current voltage curves under sunlight of the most efficient devices prepared using wet process formed Cu_2S on the NiFe (Cu/Zn) and Cu/Zn substrates, respectively, from this set. The observed conversion efficiencies were 8.7% (at 590 mV) on the NiFe substrate and 9.1% (at 633 mV) on the copper substrate at zinc compositions of 11 and 23% respectively. Although the open circuit voltage of the device on the copper substrate decayed 30 mV in 30 minutes under illumination, the device on NiFe decayed less than 3 mV in the same time.

Decision Point for High Efficiency (CdZn)S/Cu_2S Cells - Near Term

Figure 7 shows the options that were pursued as a means of fabricating a (CdZn)S/Cu_2S solar cell with the desired Cu_2S morphology. The figure illustrates the first four layers of the (CdZn)S/Cu_2S device, and excludes the transparent grid and anti-reflection coating. Toward the end of planning an effort to achieve the most efficient (CdZn)S/Cu_2S device using present technology, a selection process from the available options was undertaken. For the substrate and inter-layer the conventional zinc-plated copper substrate was selected. Although very promising, the process for obtaining the proper inter-layer on NiFe is not under sufficient control. Furthermore, because of the lower thermal conductivity of NiFe, and the design of the present substrate heater assembly, there are thermal gradients across the substrate during growth[3]. As a consequence of inconclusive results, ITO as the inter-layer was rejected for the present.

Initially, both the single and bilayer approaches for (CdZn)S film growth were considered, but the recent achievement of uniform sized grains (1-2 μm)

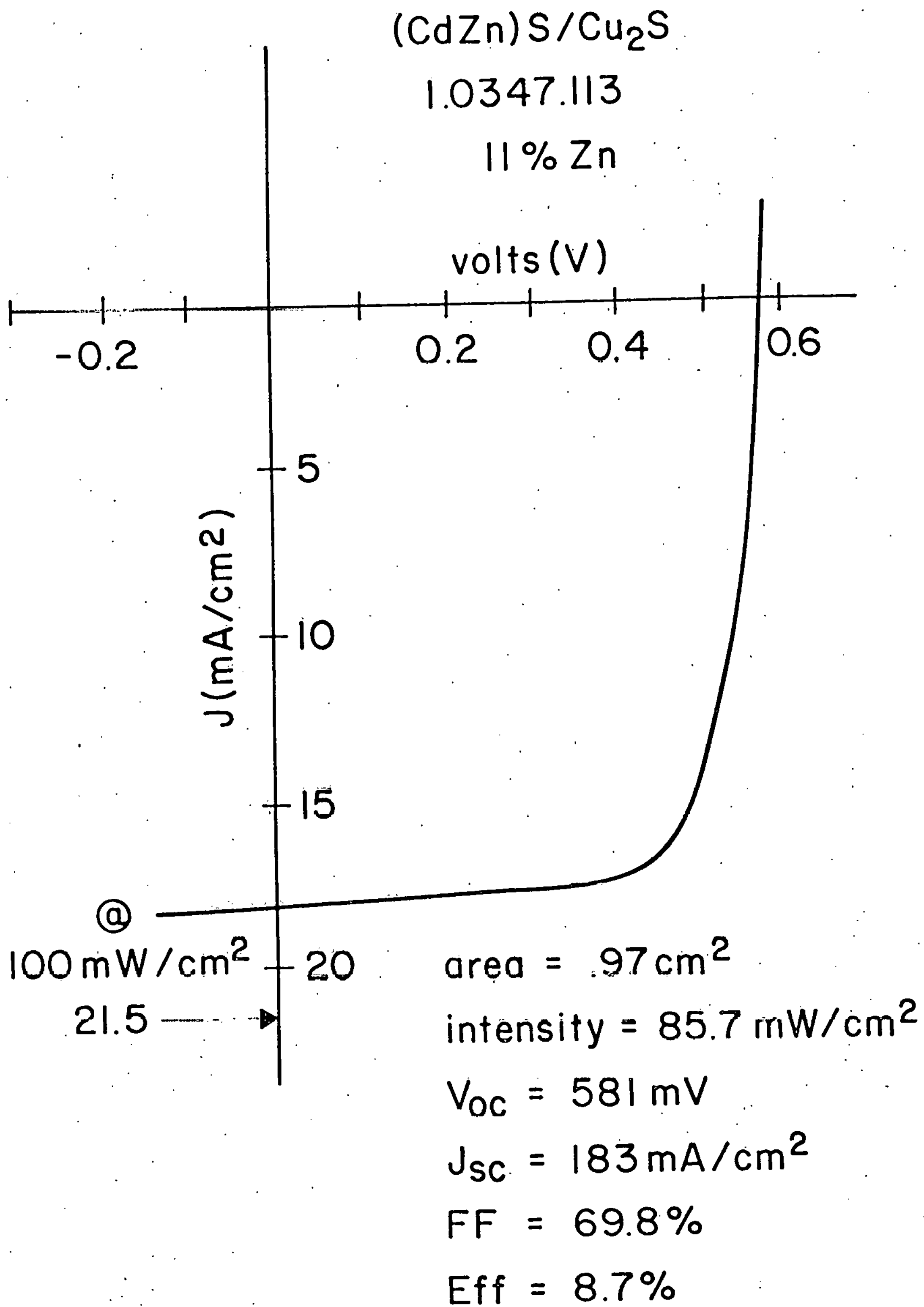


Figure 5. I-V curve for $(CdZn)S/Cu_2S$ junction on a NiFe substrate tested under sunlight.

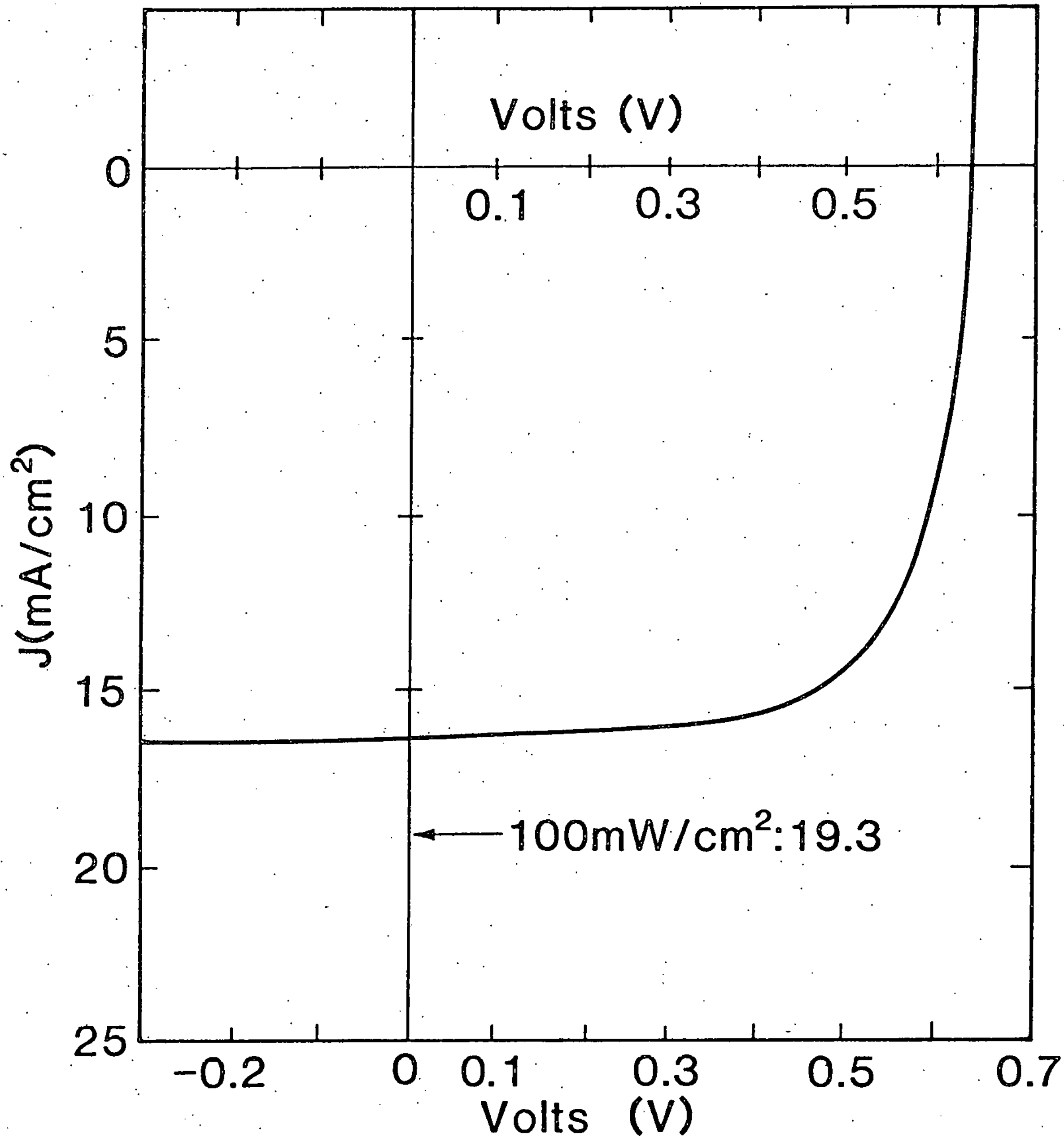


Figure 6. I-V curve for single-layer-(CdZn)S/Cu_2S junction on copper tested under sunlight.

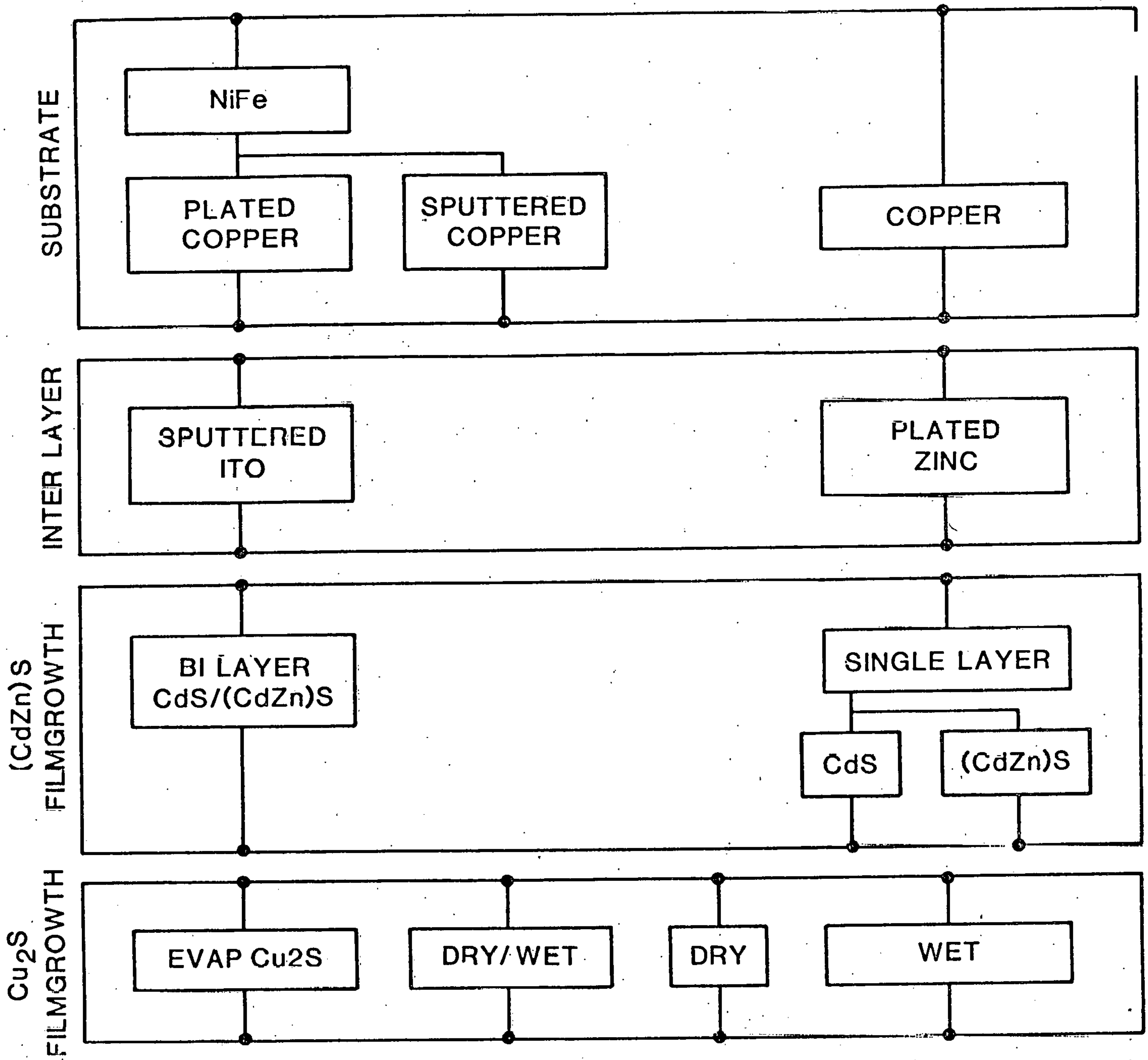


Figure 7. Diagram depicting options pursued for fabrication of $(CdZn)S/Cu_2S$ cell with desired Cu_2S morphology.

with films deposited directly on the metallic substrate eliminated the need for the bilayer approach.

With regard to Cu_2S formation, evaporated Cu_2S and straight dry process Cu_2S were rejected, the former because of limited experience, the latter because of low light generated currents. The wet-on-dry process developed under Task 1 was eliminated since it was concluded that no overall improvement in device efficiency was accomplished. Thus the conventional wet process formed Cu_2S was selected. A determination was made as to the sensitivity of the light generated current to Cu_2S wet process formation time. Three pieces for the same substrate were barriered for 10, 15 and 20 seconds, respectively. The subsequently fabricated devices indicated a definite fall-off in device performance for the longest barrier time. However, only a small different in V_{OC}, and no significant change in J_L was noted for the two shorter times: 20.1 $\pm$ 0.5 mA/cm^2 at 10 seconds and 19.5 $\pm$ 0.3 mA/cm^2 for 15 seconds. A barrier time of 10 seconds was chosen for the ensuing experiments.

As previously reported[1] the pressure in the bell jar during (CdZn)S depositions is typically 1-2 x 10^{-4} torr, about a factor of ten greater than during CdS deposition. The concentric source used for the deposition of (CdZn)S films is large and requires more power to achieve the desired growth rates. To the extent that the additional heat load could result in high bell jar pressures during film deposition, an alternative "stack" source was designed to require less power. Its essential features were that it was smaller (the same outer dimensions as the conventional CdS source,) and places the ZnS above the CdS in a cylindrical configuration, thus allowing the potential for separate temperature control of the CdS and ZnS. Initial runs with this source with no separate

temperature control indicated its parity with the concentric source with respect to film quality. There was, however, no appreciable reduction in bell jar pressure during (CdZn)S depositions. This aspect will be pursued more thoroughly in the future.

High Efficiency (CdZn)S/Cu_2S Devices

The description of the material and the process steps for the fabrication of high efficiency (CdZn)S/Cu_2S cells is as follows. (CdZn)S films 20-30 μm thick were grown at a rate in the range of 1.0 - 1.5 m/min. on a zinc-plated, copper substrate held at between 210-220°C. The as grown $Cd_{1-x}Zn_xS$ films had $.1 < x < .2$, resistivities between 1-20 ohm.cm, and all exhibited a relatively unform distribution of grain sizes between 2-3 μm. Samples to be made into cells were cleaned in microcleaner at 60°C prior to the application of the screen-printed tab insulator layer and prior to surface texturing. Surface texturing was accomplished by immersion for 20 seconds in a 25% (by volume) HCl solution held at 60°C. Cu_2S formation was accomplished by a 10 second immersion in the conventional IEC[7] bath which had had hydrazine added to it immediately before sample processing. Samples comprising four individual cells were subsequently heat treated for 16 hours at 170°C in flowing hydrogen prior to the application of the 32.5 line/cm gold grid lines and the tabs. The samples were cut into cells, and tested prior to the application by e-gun vaporization of a 700nm thick Ta_2O_5 anti-reflection layer. During the entire processing sequence particular care was taken by all personnel involved to minimize the exposure of the samples to air.

Figures 8 and 9 show the histograms for the optimized light generated current densities (normalized to 100 mW/cm^2 light intensity,) and optimized conversion efficiencies for 64 cells fabricated as described above from 16 different (CdZn)S

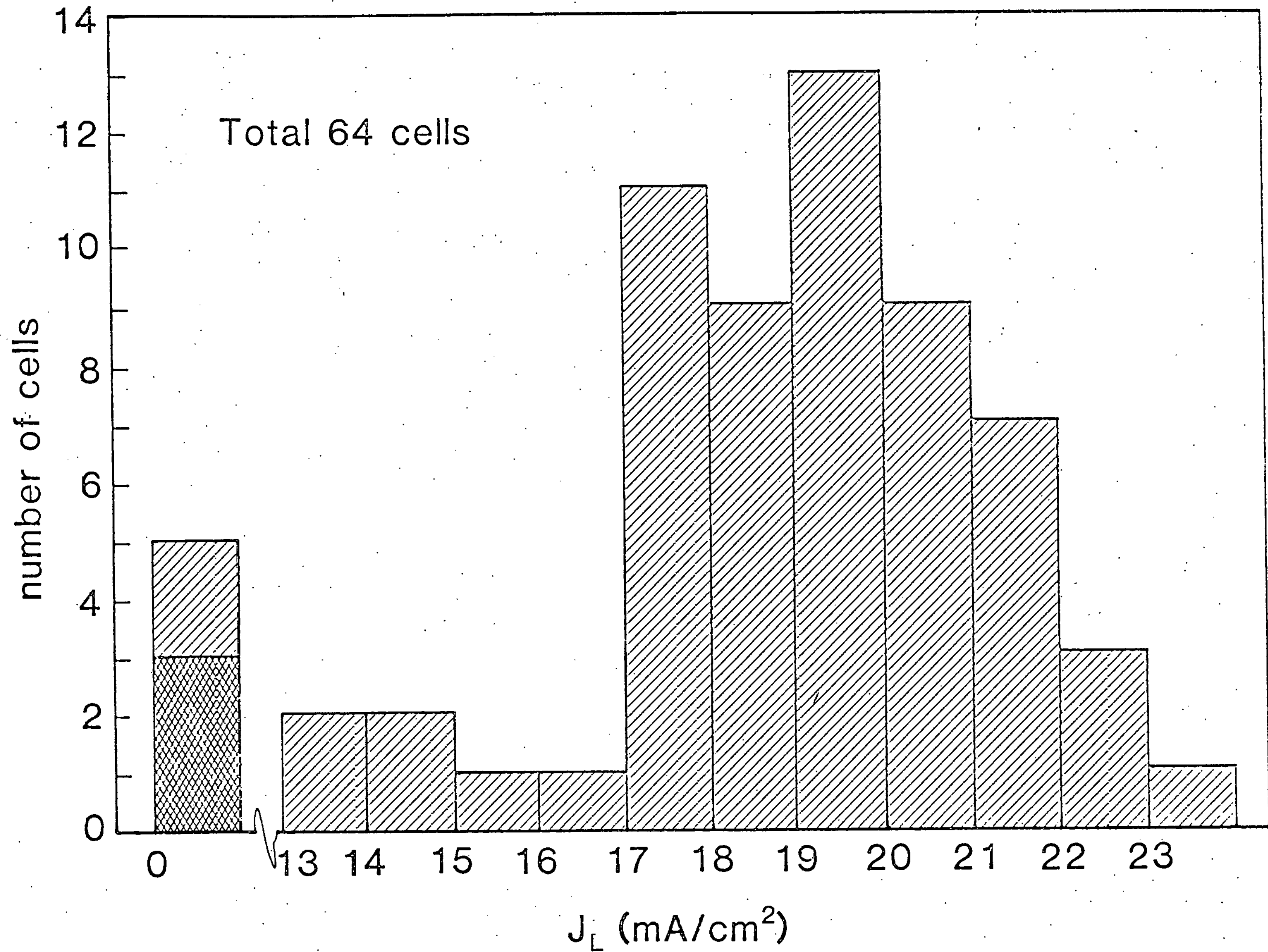


Figure 8. Histogram of optimized light generated current densities for (CdZn)S/Cu_2S cells made from 16 zinc plated (300nm)-copper substrates.

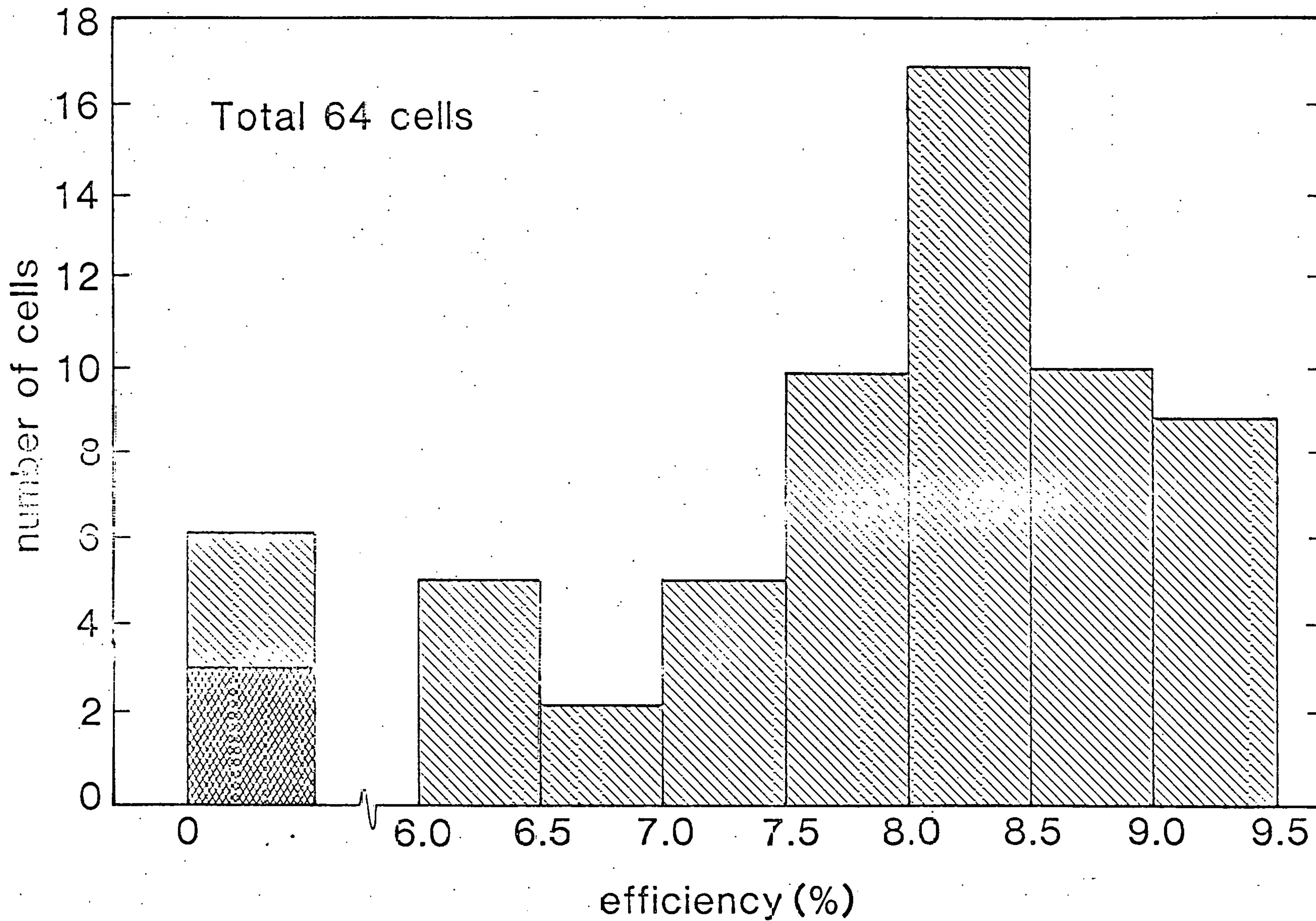


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Figure 9. Histogram of optimized efficiencies for same cell set described in figure 8.

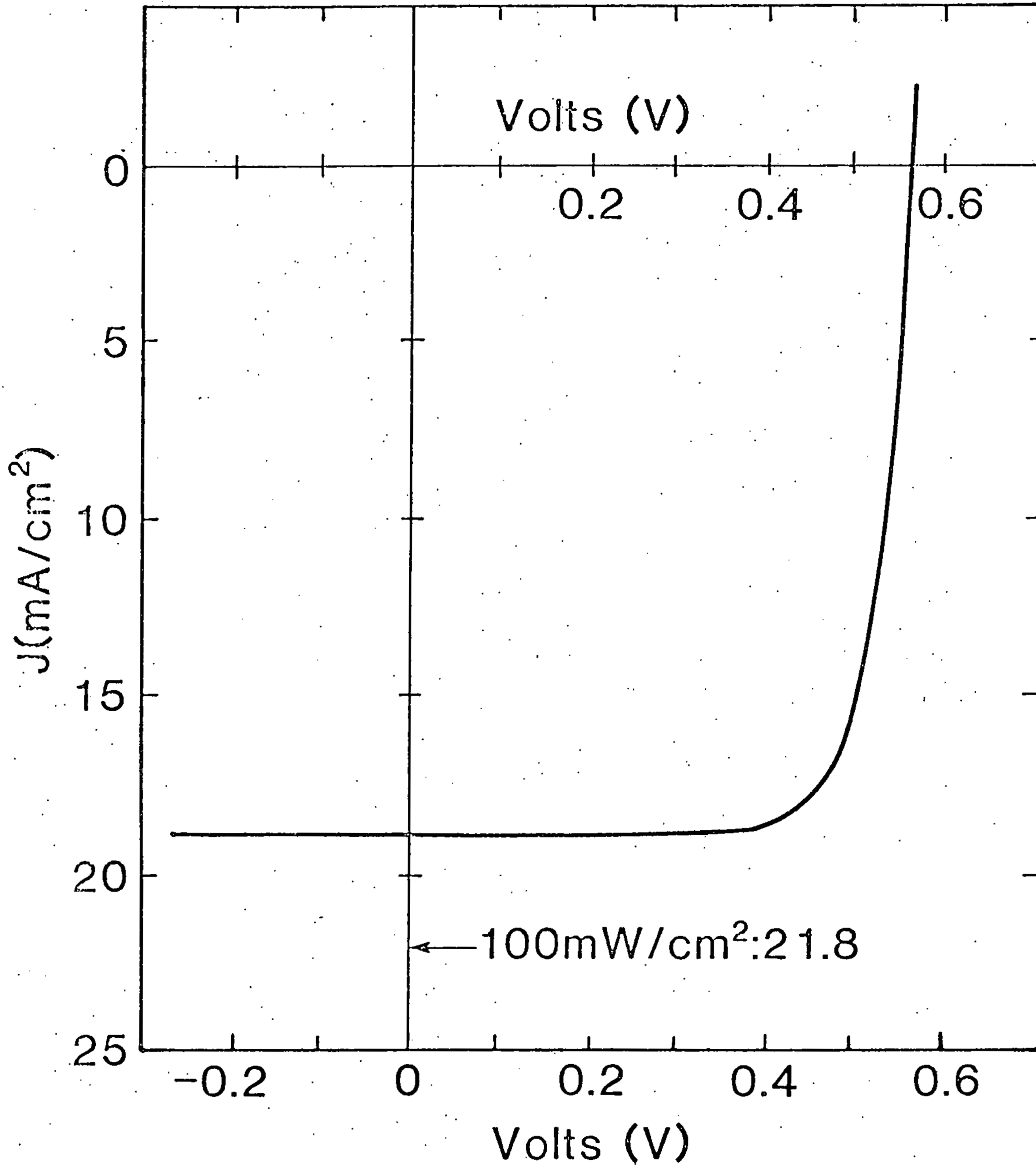

Figure 10. I-V curve for most efficient cell from set described in Figure 8.

growth runs. The zinc plating time for the entire set was 8 seconds ($\sim$ 3000 nm equivalent thickness). Of the set, only three were shorted and half exceeded 8%. The current-voltage characteristic for the most efficient cell tested under the simulator from this set is shown in Figure 10.

As has been previously reported(3) an increase in the zinc-plated copper substrate reflectivity is realized as a consequence of reducing the zinc plating thickness. Accompanying this for the present cell design is an increase in the light generated current. A shift was, therefore, made to thinner zinc plating. In addition, a procedure was instituted to accelerate cell optimization while at the same time minimizing handling prior to initial cell testing by an additional 44 hour heat treatment at 170°C in flowing hydrogen prior to the application of the anti-reflection layer. At this point the samples were cut into four individual cells and initially tested. Figures 11 and 12 show the histograms for the optimized light generated current densities (normalized to 100 mW/cm^2 light intensity,) and the optimized conversion efficiencies of 84 cells fabricated as described above from nine different substrates prepared on copper substrates with 4 second zinc plate ($\sim$ 1500 nm equivalent thickness.) Under the simulator 31 of the cells exhibited conversion efficiencies in excess of 9%, 19 over 9.5%, and 4 over 10%. Table 8 shows the performance of cells tested under collimated sunlight, including two with conversion efficiencies over 10%. Figure 13 shows the current voltage characteristic of the best cell tested under sunlight conditions.

Table 9 is a listing by efficiency of 64 cells made on 8 second zinc plate. Table 10 is a listing by efficiency of the 84 cells made on 4 second zinc plate.

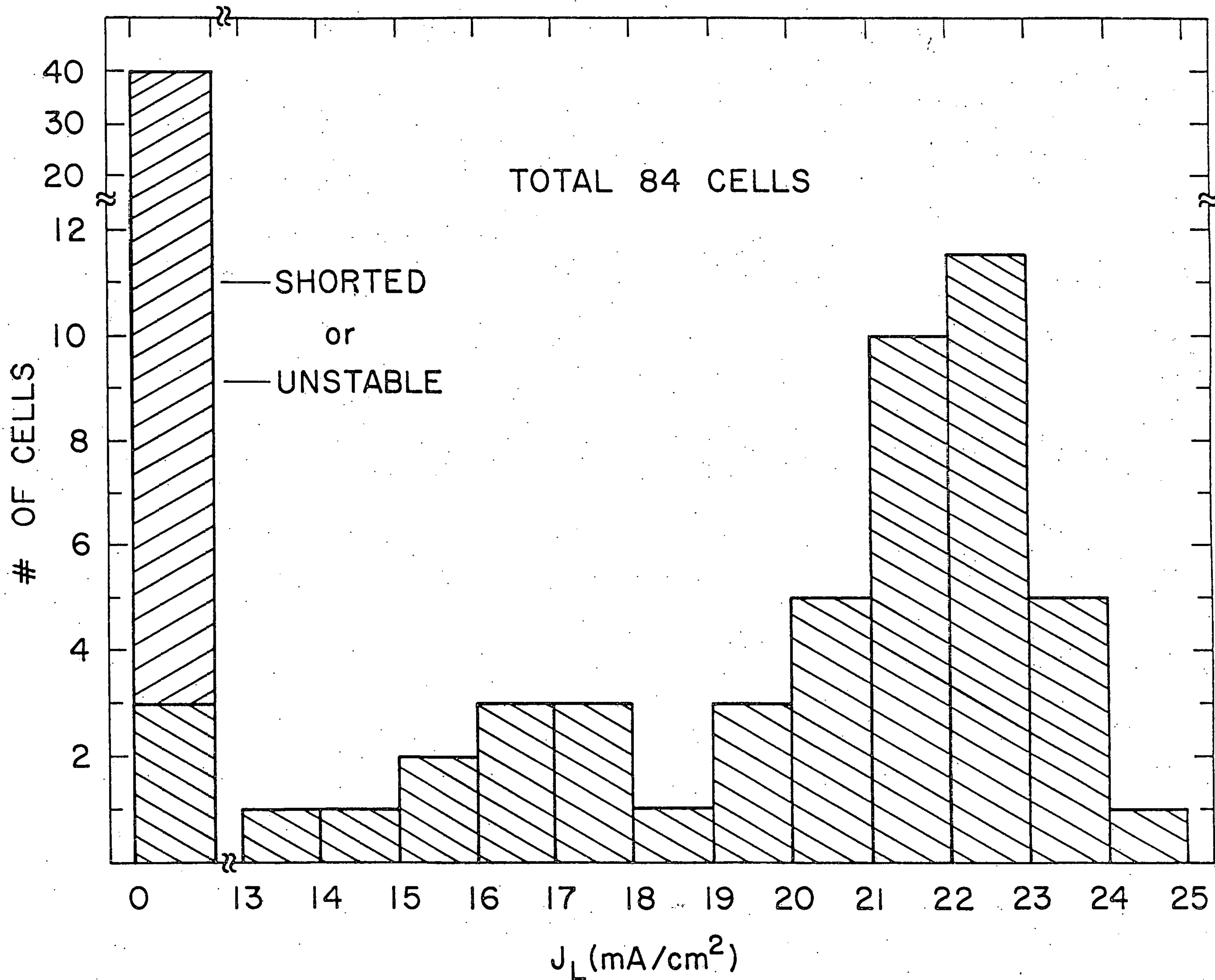

Figure 11. Histogram of optimized light generated current densities for (CdZn)S/Cu_2S cells made from 9 zinc-plated (150nm)-copper substrates which were facricated using a procedure to minimize handling prior to initial testing.

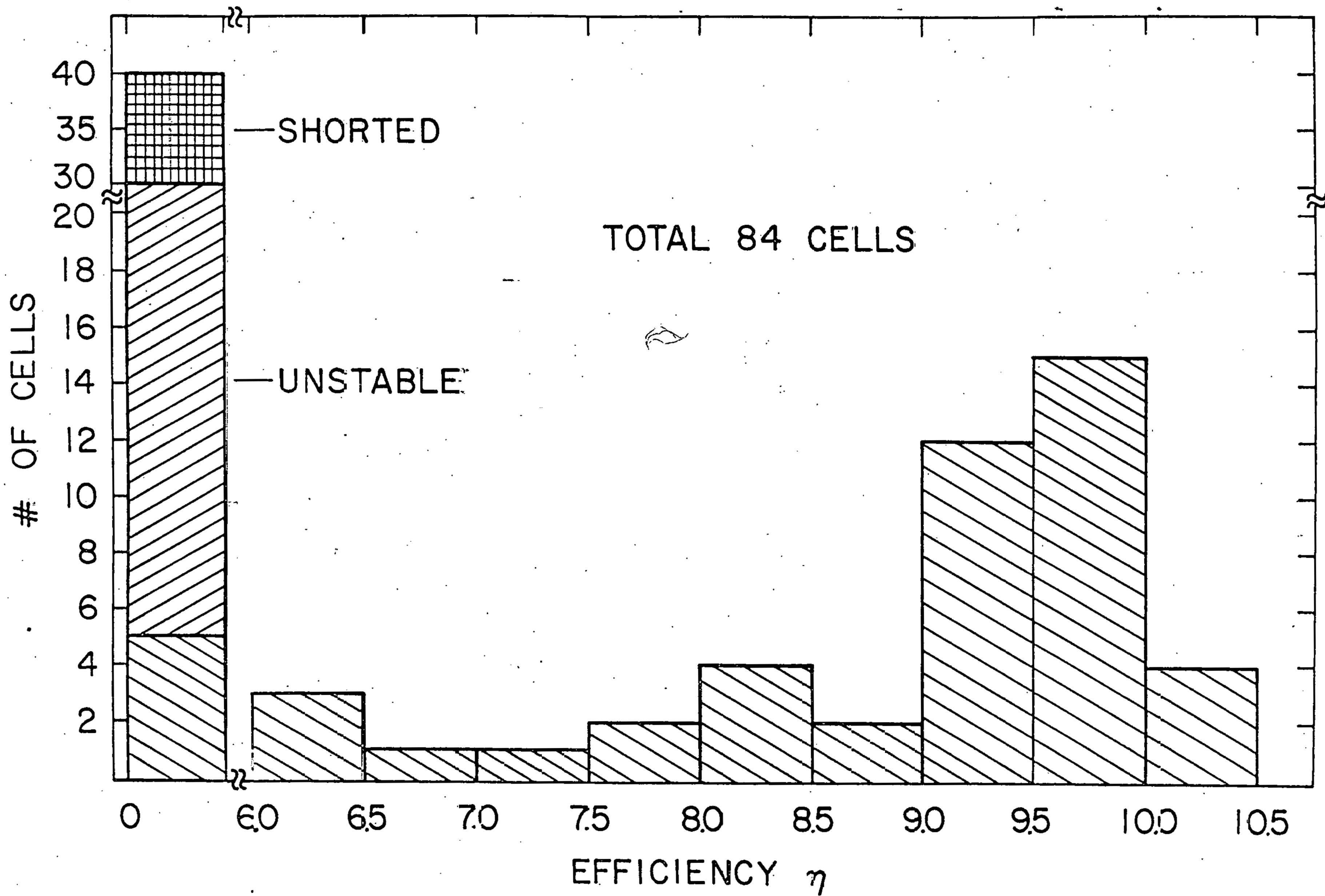

Figure 12. Histogram of optimized efficiencies for same cell set described in Figure 11.

TABLE 8

SUNLIGHT TESTING - 8/16/80

Cell #	Intensity (mW/cm^2)	J_{SC} (mA/cm^2)	V_{OC} (V)	FF (%)	Eff. (%)	J_L(100mW/cm^2) (mA/cm^2)
1.395.211	81.2	18.5	.599	74.8	10.2	22.8
1.408.114	82.0	21.1	.561	69.7	10.1	25.9
1.389.224	81.1	17.4	.590	76.9	9.70	21.4
1.395.214	80.5	17.1	.601	75.6	9.66	21.2
1.395.213	82.0	18.9	.593	70.7	9.64	23.1

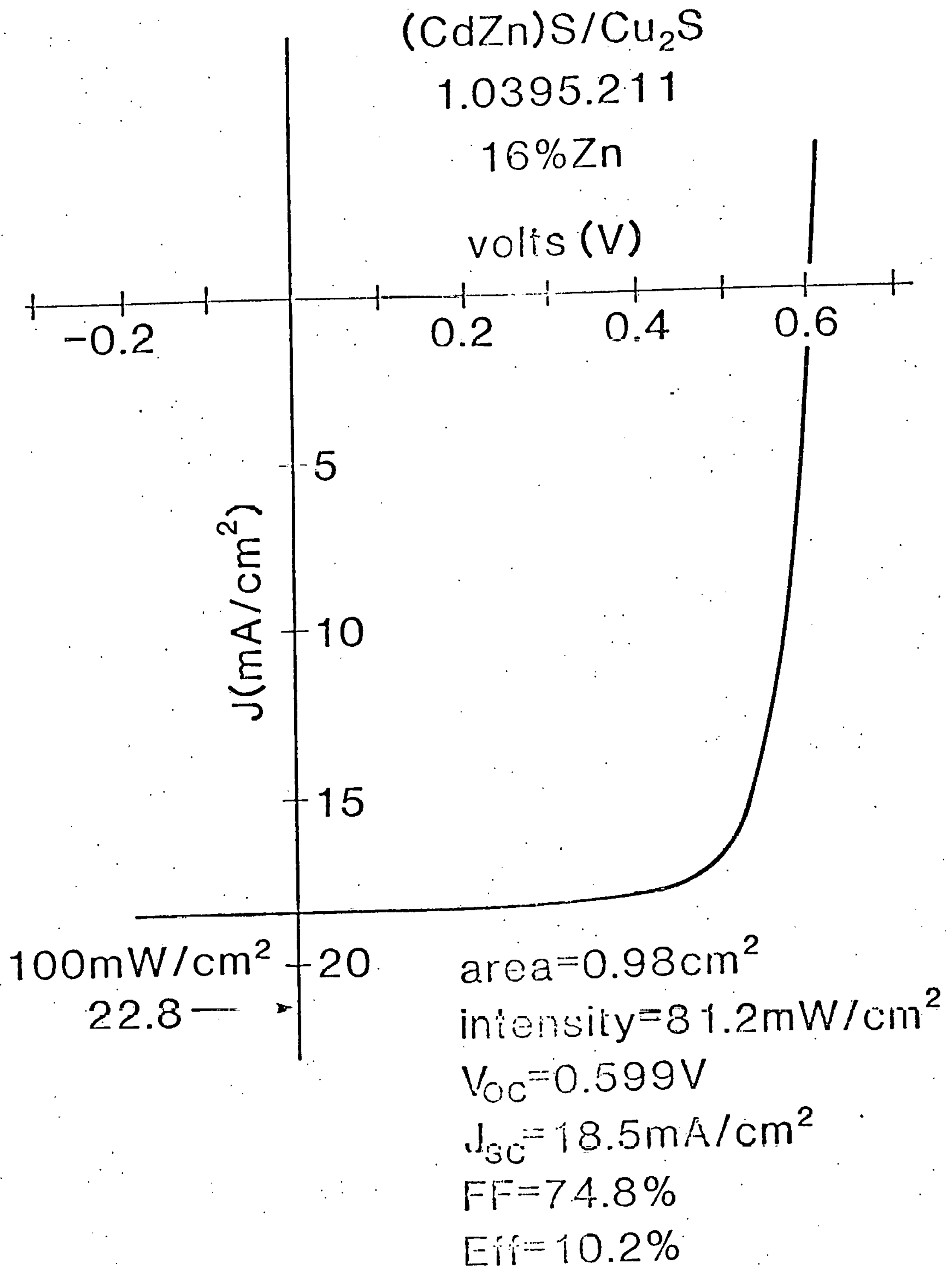

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Figure 13. I-V curve of outdoor test for most efficient cell from set described in Figure 11.

COUNT	CELL #	EFF(%)	J_L (mA/cm^2)	Voc(V)	FF(%)	Rs(Ωcm^2)	Gs($\mho \cdot cm^{-2}$)
00001	10372.114	9.39	21.89	.5751	75.7	1.66	.73
00002	10376.111	9.38	21.13	.5890	76.5	1.64	.56
00003	10376.112	9.22	21.79	.5788	74.3	2.05	1.00
00004	10372.113	9.21	21.89	.5748	74.5	1.62	1.50
00005	10376.113	9.12	21.36	.5847	74.2	2.16	.98
00006	10376.114	9.08	21.50	.5797	74.1	2.01	1.19
00007	10385.114	9.02	20.55	.5879	76.0	1.60	.91
00008	10372.111	8.99	23.10	.5610	70.7	2.30	2.44
00009	10382.114	8.99	20.23	.5986	75.7	1.80	.97
00010	10364.112	8.93	21.85	.5732	72.4	2.75	.82
00011	10364.114	8.86	21.51	.5769	72.7	2.35	1.43
00012	10364.113	8.77	21.53	.5687	72.9	2.44	1.04
00013	10385.113	8.72	19.54	.5947	76.6	1.29	1.12
00014	10353.114	8.70	19.13	.6429	72.5	2.39	2.29
00015	10370.113	8.66	19.67	.6128	73.4	2.39	1.58
00016	10361.114	8.63	20.63	.5922	72.1	2.77	1.50
00017	10385.111	8.61	19.60	.5959	75.2	2.17	.77
00018	10365.114	8.56	21.81	.5778	69.4	3.44	1.77
00019	10361.113	8.53	20.65	.5884	71.7	2.90	1.48
00020	10385.112	8.53	19.21	.5975	75.8	2.01	.71
00021	10373.114	8.47	20.31	.5926	72.1	2.19	2.30
00022	10361.112	8.36	19.95	.5933	72.2	2.93	1.34
00023	10353.112	8.35	18.57	.6306	73.1	2.50	1.81
00024	10371.114	8.35	20.18	.6032	70.4	2.94	2.40
00025	10378.114	8.29	18.95	.5922	75.5	1.66	1.16
00026	10373.113	8.26	19.94	.5901	71.9	2.79	1.64
00027	10353.113	8.23	17.82	.6310	75.1	1.69	1.65
00028	10371.113	8.21	20.03	.6030	69.8	3.37	2.24
00029	10372.112	8.20	19.61	.5696	75.0	1.73	1.07
00030	10370.112	8.19	18.57	.6019	75.0	1.81	1.36
00031	10365.113	8.16	20.77	.5818	69.1	3.87	1.50
00032	10353.111	8.11	17.92	.6358	73.1	2.57	1.80
00033	10382.112	8.10	17.82	.6078	76.6	1.53	1.01
00034	10382.113	8.09	18.03	.6031	76.1	1.72	.97
00035	10378.111	8.05	18.19	.5986	75.6	1.90	.97
00036	10364.111	7.79	18.49	.5738	75.2	1.78	1.03
00037	10370.111	7.76	18.21	.5940	73.7	2.27	1.46
00038	10378.113	7.73	19.04	.5739	72.5	2.54	1.44
00039	10365.112	7.70	19.50	.5858	69.2	3.91	1.68
00040	10373.111	7.67	17.51	.6026	74.6	2.03	1.35
00041	10365.111	7.66	20.02	.5841	67.5	4.01	2.50
00042	10373.112	7.53	17.21	.6037	74.5	2.15	1.30
00043	10363.111	7.49	17.90	.5744	74.7	2.08	.95
00044	10381.112	7.46	17.62	.5965	72.9	2.95	1.21
00045	10363.112	7.43	18.70	.5833	70.2	2.67	2.62
00046	10381.114	7.33	17.29	.5922	73.6	2.57	1.22
00047	10371.112	7.29	17.76	.6019	70.4	3.49	1.96
00048	10361.111	7.19	17.27	.5913	72.6	2.59	1.66
00049	10378.112	7.17	17.14	.5918	72.8	2.35	1.76
00050	10363.114	7.09	17.19	.5765	73.6	2.54	1.06
00051	10370.114	6.99	19.23	.5966	63.7	4.11	4.91
00052	10359.111	6.85	18.95	.5591	67.0	3.53	3.19
00053	10371.111	6.75	17.58	.6126	65.5	3.95	4.07
00054	10363.113	6.34	16.45	.5765	69.5	2.58	2.93
00055	10383.114	6.22	14.15	.5986	76.0	1.73	.99
00056	10359.112	6.05	15.66	.5749	69.9	3.03	2.35
00057	10383.112	6.05	13.75	.5950	76.6	1.66	.81
00058	10383.111	5.96	13.27	.6129	76.0	2.62	.64
00059	10383.113	5.57	12.53	.6081	76.1	2.04	.85
00060	10359.113	5.54	14.29	.5674	71.3	2.86	1.30
00061	10359.114	4.22	10.75	.5748	72.1	2.87	1.46
00062	10381.111	0.01	0.00	.0000	25.7	9.99	9.99
00063	10381.113	0.00	0.00	.0000	0.0	9.99	9.99
00064	10382.111	0.00	0.00	.0000	0.0	9.99	9.99

Table 9. Cell characteristics for (CdZn)S/Cu_2S on 8 second zinc plate.

COUNT	CELL #	EFF(%)	J_L (mA/cm^2)	Voc (V)	FF(%)	Rs (Ωcm^2)	Gs ($\mho \cdot cm^{-2}$)
00001	10408.114	10.20	24.59	.5735	73.1	2.02	1.43
00002	10395.211	10.08	22.13	.6141	75.3	1.75	1.32
00003	10408.112	10.03	23.51	.5732	75.3	1.58	.95
00004	10408.213	9.98	22.80	.5797	76.5	1.33	.84
00005	10389.211	9.93	22.24	.6010	75.3	1.78	1.10
00006	10395.214	9.93	21.95	.6062	75.7	1.45	1.43
00007	10389.214	9.85	23.03	.5950	73.0	2.19	1.69
00008	10390.211	9.81	23.28	.5867	72.9	2.15	1.69
00009	10389.121	9.80	21.49	.6072	76.3	1.61	.95
00010	10403.121	9.80	22.70	.5841	74.9	1.71	1.18
00011	10408.221	9.77	22.62	.5758	76.0	1.33	1.06
00012	10389.213	9.76	21.75	.6068	75.1	2.15	.83
00013	10395.123	9.71	21.47	.6187	74.4	2.06	1.50
00014	10389.123	9.69	21.50	.6053	75.7	1.63	1.21
00015	10389.124	9.66	21.54	.6072	75.0	2.13	.92
00016	10408.111	9.62	22.77	.5734	74.8	1.54	1.41
00017	10395.121	9.59	21.35	.6157	74.3	1.93	1.66
00018	10389.224	9.58	21.15	.6044	76.1	1.49	1.17
00019	10389.223	9.56	21.42	.6026	75.3	1.84	1.12
00020	10408.113	9.56	23.37	.5784	71.9	2.20	2.09
00021	10408.211	9.54	22.03	.5777	76.0	1.39	1.02
00022	10408.212	9.53	21.58	.5793	77.4	.91	1.03
00023	10395.122	9.46	21.81	.6110	72.4	2.38	2.04
00024	10389.212	9.43	21.79	.5987	73.5	2.18	1.51
00025	10395.213	9.41	22.47	.6068	70.6	2.17	3.30
00026	10390.214	9.39	23.74	.5899	68.7	1.70	5.03
00027	10408.224	9.39	22.75	.5693	73.6	1.99	1.29
00028	10389.221	9.37	21.33	.6014	74.3	2.16	1.17
00029	10403.124	9.34	22.19	.5854	73.1	2.18	1.56
00030	10403.123	9.32	21.68	.5883	74.3	2.07	1.11
00031	10404.213	9.32	20.63	.6206	74.3	1.79	1.91
00032	10390.212	9.25	21.10	.5913	75.4	1.65	1.19
00033	10408.223	9.23	21.75	.5774	74.7	1.62	1.40
00034	10395.124	9.04	20.73	.6122	72.9	1.61	2.72
00035	10389.122	8.97	19.26	.6105	77.7	1.27	.77
00036	10404.122	8.92	19.54	.6220	74.9	2.18	1.22
00037	10404.211	8.75	19.22	.6209	75.0	1.65	1.70
00038	10408.122	8.74	22.50	.5541	71.4	2.42	1.69
00039	10405.114	8.33	18.11	.6230	75.5	1.96	1.19
00040	10390.124	8.29	19.25	.5890	74.7	2.09	1.05
00041	10404.113	8.29	17.63	.6349	75.9	2.03	1.10
00042	10405.113	8.11	17.73	.6228	75.3	2.09	1.17
00043	10390.123	7.88	20.40	.5982	66.9	2.61	4.69
00044	10405.112	7.71	17.14	.6206	74.5	1.93	1.61
00045	10403.122	7.06	16.65	.5985	73.1	2.09	1.91
00046	10404.111	6.94	15.07	.6367	74.7	1.74	1.66
00047	10408.121	6.36	16.07	.5661	72.4	2.26	1.80
00048	10390.121	6.08	16.82	.6051	63.0	5.10	4.43
00049	10405.111	5.40	12.01	.6214	75.4	1.89	1.16
00050	10404.214	4.99	12.42	.6253	67.7	2.25	3.28
00051	10390.224	4.58	15.15	.5507	59.0	7.26	4.47
00052	10404.114	4.58	10.13	.6352	74.8	1.99	1.21
00053	10390.222	1.88	0.00	.0000	45.8	9.99	9.99
00054	10390.223	1.45	0.00	.0000	38.9	9.99	9.99
00055	10395.223	1.21	0.00	.0000	42.3	9.99	9.99
00056	10390.221	1.03	0.00	.0000	35.2	9.99	9.99
00057	10390.122	0.22	0.00	.0000	25.2	9.99	9.99
00058	10406.111	0.04	0.00	.0000	24.8	9.99	9.99
00059	10395.224	0.02	0.00	.0000	25.4	9.99	9.99
00060	10408.222	0.02	0.00	.0000	26.1	9.99	9.99
00061	10389.222	0.01	0.00	.0000	25.4	9.99	9.99
00062	10408.214	0.01	0.00	.0000	25.1	9.99	9.99
00063	10390.213	0.00	0.00	.0000	0.0	9.99	9.99
00064	10395.212	0.00	0.00	.0000	0.0	9.99	9.99
00065	10395.221	0.00	0.00	.0000	0.0	9.99	9.99
00066	10395.222	0.00	0.00	.0000	0.0	9.99	9.99
00067	10404.112	0.00	0.00	.0000	0.0	9.99	9.99
00068	10404.121	0.00	0.00	.0000	0.0	9.99	9.99
00069	10404.123	0.00	0.00	.0000	0.0	9.99	9.99
00070	10404.124	0.00	0.00	.0000	0.0	9.99	9.99
00071	10404.212	0.00	0.00	.0000	0.0	9.99	9.99
00072	10406.112	0.00	0.00	.0000	0.0	9.99	9.99
00073	10406.113	0.00	0.00	.0000	0.0	9.99	9.99
00074	10406.114	0.00	0.00	.0000	0.0	9.99	9.99

Table 10. Cell characteristics for $(CdZn)S/Cu_2S$ on 4 second zinc plate

COUNT	CELL #	EFF(%)	J_L (mA/cm^2)	Voc(V)	FF(%)	Rs(Ωcm^2)	Gs($\sigma . cm^{-2}$)
00075	10406.121	0.00	0.00	.0000	0.0	9.99	9.99
00076	10406.122	0.00	0.00	.0000	0.0	9.99	9.99
00077	10406.123	0.00	0.00	.0000	0.0	9.99	9.99
00078	10406.124	0.00	0.00	.0000	0.0	9.99	9.99
00079	10407.111	0.00	0.00	.0000	0.0	9.99	9.99
00080	10407.112	0.00	0.00	.0000	0.0	9.99	9.99
00081	10407.113	0.00	0.00	.0000	0.0	9.99	9.99
00082	10407.114	0.00	0.00	.0000	0.0	9.99	9.99
00083	10408.123	0.00	0.00	.0000	0.0	9.99	9.99
00084	10408.124	0.00	0.00	.0000	0.0	9.99	9.99

Table 10 Continued

4.3 Electro-Optic Analysis and Modeling

Several experiments on the cells have involved photocapacitance and dark capacitance measurements, taking advantage of improvements in the accuracy, repeatability and ease of use resulting from modification and expansion of the capacitance measuring facility. Thus, data have been obtained on diffusion of compensating ions into the CdS by heat treatment; differences in wet-process and dry-process cells (as well as Au/CdS Schottky barriers) interpreted in terms of junction geometry and possible differences in impurity levels in the CdS, and effects of heat treatment on interface recombination. Dynamics of the hole trapping have been investigated by means of transient photocapacitance, combined with its temperature dependence, and the results show that the trapping is much weaker than anticipated, and probably occurs mostly in the high-field region near the junction. Planned capacitance experiments should further clarify the details of the operation of the CdS/Cu_2S junction.

1. Capacitance measurement

In order to augment the circuits for measuring capacitance and conductance of solar cells[1], an HP 4274A Multi-frequency LCR Meter and an HP-85 Desktop Computer have been purchased and installed. Besides enhancing the precision and accuracy of C and G measurements because of smaller, better defined phase angle error, this combination allows measurement of frequency dependence between 100Hz and 100kHz and automation of measurements and data handling.

Comparison of the results from the LCR meter for CdS/Cu_2S cells at f = 10kHz with those from the custom-made circuits and lock-in amplifier used

previously show agreement for C within about $\pm$ 4% both in light and dark. Agreement in G is considerably poorer, especially in the light. Work is going on aimed at automating the measurements.

Wet and dry process CdS/Cu_2S cells

In order to clarify the effect on the junction of these cells of the two different methods of producing Cu_2S, dark capacitance measurements have been made on a series of cells made by the dry process and differing in heat treatment. Before heat treatment, C_{dark}/A = 112 nF/cm^2, and after 32 hr in H_2 at 170°C, C_{dark}/A = 2.5 nF/cm^2. Unlike the dry-process cell described earlier, whose capacitance showed a strong dependence on DC bias V over a range of reverse bias, the present heat-treated cells had a practically constant capacitance in the dark out to at least -2 V. Further experiments are planned for the purpose of determining whether this behavior is typical.

Photocapacitance analysis

From measurements of photocapacitance decay in CdS/Cu_2S cell 21065.111, transient behavior of trapped holes in CdS has been analyzed, taking into account the $\exp(-\alpha x)$ dependence of hole generation on optical absorption in the CdS at distance x from the junction. See Appendix (B). Figure 14 shows variation of conductance G with temperature in the same cell. The variation of C and G differs from what is observed in p-n junctions where optical effects are not a factor[8]. This is related to the temperature variation of the absorption coefficient α and the hole emission rate.

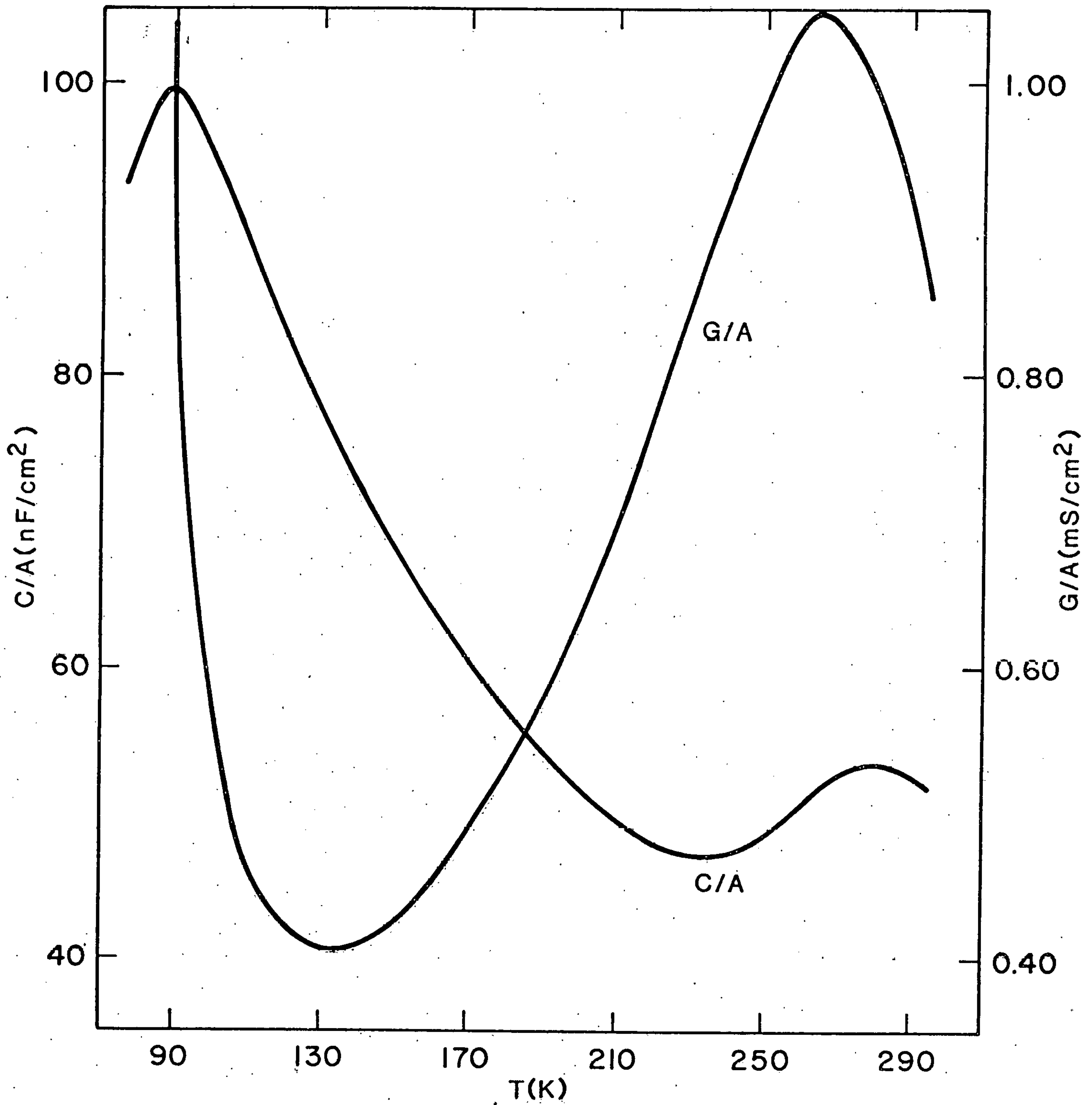

Figure 14. Capacitance C and conductance G per unit area for cell #21065.111 under intense blue light, as a function of temperature.

A further application of the model explains the observation that, on recent, good quality CdS/Cu_2S cells, attempts have not been successful to obtain S_I/μ_2 and η_Q from plots of ξ^{-1} (reciprocal electric field) versus η_c^{-1} (reciprocal collection efficiency) according to the method used earlier[9]. This is observed both in cells which have undergone extensive heat treatments to optimize efficiency and in cells tested between heat treatments to determine their effect on S_I/μ_2. Figure 15 shows a plot of C^{-1} (assumed proportional to ξ^{-1} - see below) versus η_c^{-1} for one of the latter type of cell.

It was found that, although C varied by a factor as large as 2 or 4 while illumination intensity varied from .01 AM1 to 1.5 AM1, η_c was almost constant. The standard treatment gives, for electric field at the junction,

$$\xi(0) = - \frac{2(V_D - V)}{\varepsilon\varepsilon_o} (\frac{C}{A}),$$

where V_D is diffusion voltage and V is applied DC voltage. Thus the observed variation of C should be accompanied by a proportional variation of ξ, and this must cause η_c to vary.

However, as is shown in Appendix B, theoretical treatment of photocapacitance when α in CdS is large is consistent with the observation of η_c remaining constant while ϕ varies. This treatment gives for dependence on C of the electric field at the junction

$$\xi (0) = - (V_D - V) [\alpha + (2 + \frac{\alpha\varepsilon\varepsilon_o}{C/A}) \frac{C_\infty^2}{CA}],$$

where C_∞ is dark capacitance. Even at fairly small ϕ, $(C_\infty/C)^2 \sim 1/10$ or smaller for well heat-treated cells, so that the preceding equation reduces to

$$\xi(0) \approx - \alpha (V_D - V).$$

Thus electric field at the junction is not affected by ϕ, even though C is.

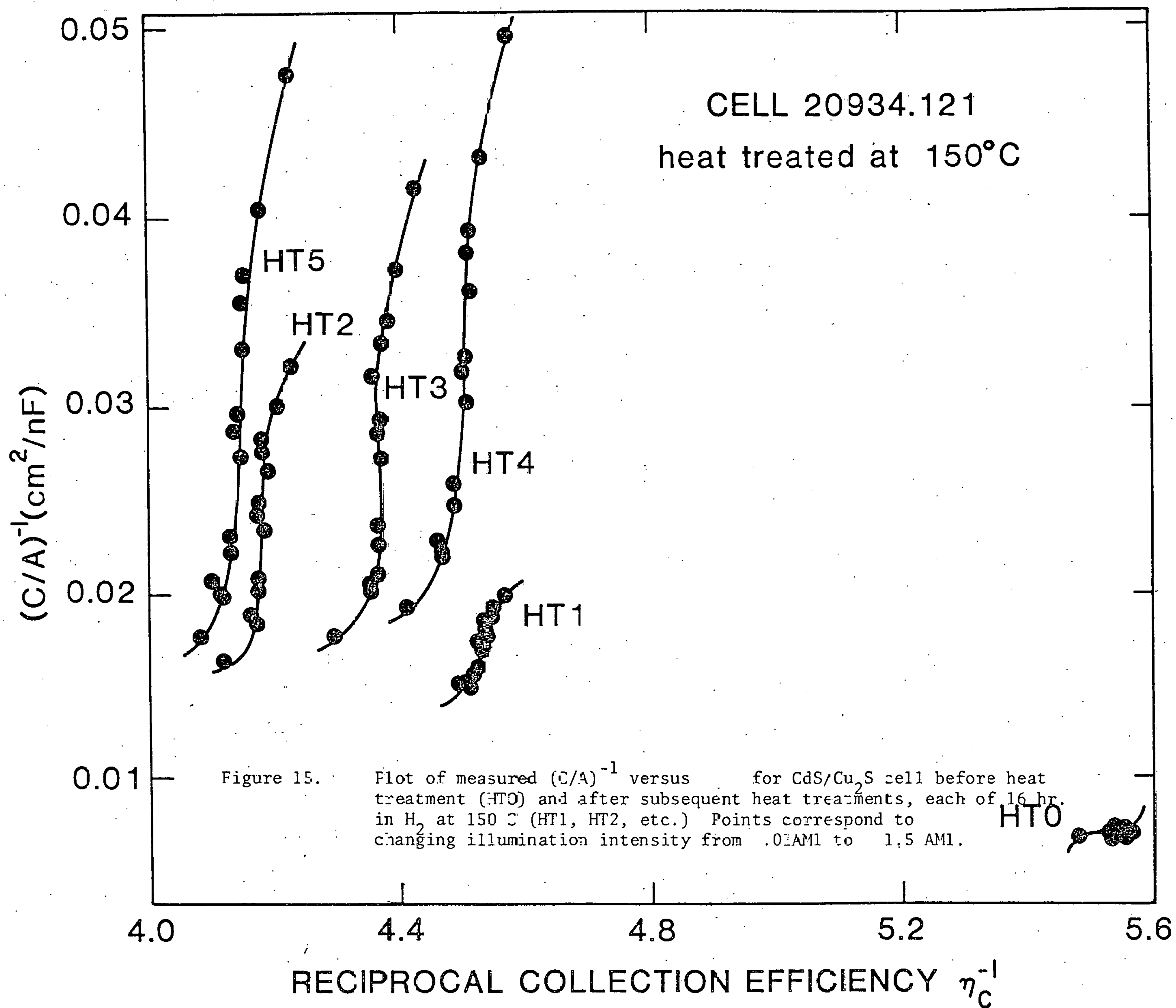

Figure 15. Plot of measured $(C/A)^{-1}$ versus for CdS/Cu_2S cell before heat treatment (HT0) and after subsequent heat treatments, each of 16 hr. in H_2 at 150 C (HT1, HT2, etc.) Points correspond to changing illumination intensity from .01AM1 to 1.5 AM1.

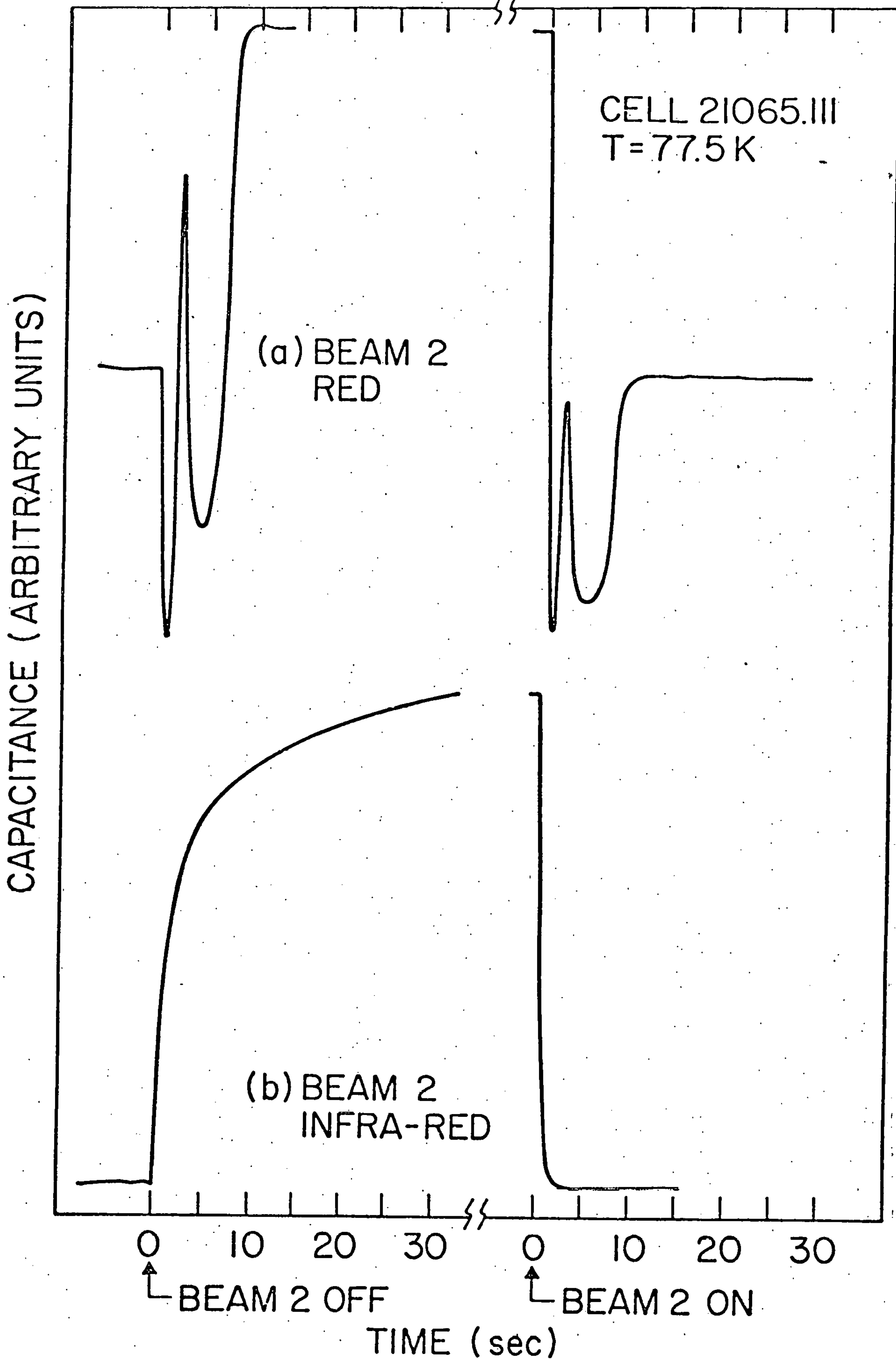

Figure 16. Transient response of capacitance of CdS/Cu_2S cell under continuous excitation by beam 1 (365 585nm) while turning on & off beam 2: 810nm. a) beam 2: 650 nm

The conclusion is that, in recent CdS/Cu_2S cells, it probably is impractical to obtain S_I/μ_2 from ξ^{-1} versus η_c^{-1} plots. Further measurement of the dependence of η_c on ϕ, particularly at different wavelengths, are needed to determine whether this is the result of a very small S_I, a very large μ_2 (approaching V_{th}/ξ, where v_{th} is thermal velocity), or some other reason.

Two-beam photocapacitance measurements have been initiated, in which short-wavelength excitation (beam 1, in a band between about 365 and 585 nm) strikes the cell continuously while a long-wavelength beam (beam 2, with cut-off wavelength λ_{cut}) is turned on and off. Changes with time of the quenching effect described previously (10), in combination with the effects described in Appendix B, will clarify the action of hole traps in CdS.

Figure 16 shows that the response of cell 21065.111 to chopped red light, with $\lambda_{cut} \approx 650$ nm, was rather complex. Four excursions of C in alternating directions were observed following both turning on and turning off beam 2. This indicates interaction of several levels with each other and with the conduction band of CdS. Work is progressing on the analysis of the mechanisms involved. Transient measurements in the immediate future will mainly use a beam 2 with a larger λ_{cut} of 810 nm. As Figure 16 shows, this results in much simpler behavior, and should give more readily accessible information on the electro-optical behavior of the cell.

4.4 Encapsulation for Improved Stability

The encapsulation task was directed towards the development of e-beam evaporated glass layers. During the initial phase, a certain number of regular 1 cm x 1 cm Cu_2S/CdS cells were encapsulated by IEC 9658 glass of 5 μm thickness. The aging tests conducted on these cells showed that the encapsulating layer did not work properly. The microscopic (SEM) analysis of the encapsulated cells showed the presence of large numbers of crack and growth defects in the glass layers(1).

A series of trial depositions were made on the matte and smooth side of electro-cleaned copper foil (substrate used in CdS evaporation) to determine the optimum glass deposition parameters. SEM examination showed that the best films, in terms of the structure, are obtained when the deposition rate and substrate temperature are respectively 5 Å/sec and 150°C(2).

Stability tests were then conducted on an array of microdevices prepared with partial support from ILZRO.* This array consisted of 256 devices of 1 mm x 0.25 mm on a square substrate of 25 x 25 mm. For the preparation of this array a CdS film was deposited on an Fe-Ni/Cu/ITO substrate. Because of the similar thermal expansion coefficient between Fe-Ni and CdS, bending of the array during heating/cooling cycles were greatly reduced. Furthermore, to reduce preferential growth defects on the glass layer, the devices had highly polished surfaces. The characteristics of 24 glass covered and 24 bare devices were monitored during heat treatments, in air, at 60°C and 80°C. The average relative decrease in J_{SC} was found to be the same for encapsulated and bare devices. Subsequent SEM investigation(3) showed that loss of hermeticity was due to the

* The support from the International Lead Zinc Research Organization is gratefully acknowledged.

cracks along the edges of the glass layer. The probable cause of these cracks is the fact that the edges of the edge of the mask used during glass deposition is in contact with the surface of the array. As a result, when the mask is removed, the glass layer is cracked at the edges. Besides these edge cracks, the glass layers were found to be defect free over the entire surface of the devices. Future work will be concentrated on depositing the glass layers using masks which are not in contact with the array surface.

References

1. IEC Quarterly Report XS-9-8309-1-01. 1980.

2. IEC Quarterly Report XS-9-8309-1-02. 1980.

3. IEC Quarterly Report XS-9-8309-1-03. 1980.

4. J. A. Bragagnolo, A. M. Barnett, J. E. Phillips, R. B. Hall, A. Rothwarf, J. D. Meakin, "The Design and Fabrication of Thin-Film CdS/Cu_2S Cells of 9.15% Efficiency." IEEE Trans. Electron Devices, ED-27 pp 645-651. 1980.

5. Evaporated Cu_2S was generously supplied by Dr. T. Vanderwel of McMaster University, Canada.

6. J. A. Bragagnolo, "Photon Loss Analysis in Thin-Film CdS/Cu_2S Photovoltaic Devices." 13th IEEE Photovoltaic Specialists Conference, pp. 412-416. 1978.

7. IEC Final Report EG-77-C-03-1576-FR. 1979.

8. G. C. Miller, D. V. Lang and L. C. Kimerling, Annual Review of Materials Science 7, 377. 1977.

9. A. Rothwarf, J. E. Phillips and N. C. Wyeth. 13th IEEE Photovoltaic Specialists Conference. pp 399-405. 1978.

10. IEC Final Report XR-9-8063-1 FR. 1979.

6. Report and Publications

Reports

Quarterly Progress Reports

September-December, 1979
XS-9-8309-1-01
December, 1979-March, 1980
XS-9-8309-1-02
March-June, 1980
XS-9-8309-1-03

Publications

1. The Design and Fabrication of Thin Film CdS/Cu_2S Cells of 9.15% Efficiency.
J. A. Bragagnolo, A. M. Barnett, J. E. Phillips, R. B. Hall, A. Rothwarf and J. D. Meakin. IEEE Trans. Electron Devices, ED-27, pp 645-651. 1980.

2. Growth and Evaluation of CdS and (CdZn)S Films for Fabrication of High Performance Photovoltaic Devices.
R. B. Hall, R. W. Birkmire, E. Eser, T. L. Hench and J. D. Meakin. Conference Record 14th IEEE Photovoltaic Specialist Conference, pp 706-711. 1980.

3. Optical Absorption Coefficient Changes in Cu_2S as the Cause of Short Circuit Current Changes in Cu_2S/CdS Solar Cells.
A. Rothwarf and H. Windawi. 14th IEEE Photovoltaic Specialist Conference, pp 722-727. 1980.

4. Current-Voltage Analysis of the Cu_2S/CdS Solar Cell with the Interdigitated Grid.
J. E. Phillips. 14th IEEE Photovoltaic Specialist Conference, pp 734-737. 1980.

5. Thin Film CdS/Cu_2S Cells with High Open Circuit Voltage and Low Reflection Losses.
J. A. Bragagnolo, R. W. Birkmire and J. E. Phillips. 14th IEEE Photovoltaic Specialist Conference, pp 1400-1401. 1980.

Appendix A

Comment on "Space-charge Limited Currents in Cu_xS/CdS Solar Cells"
J. Electronic Materials Vol. 9, 467, 1980.

A recent paper by Partain *et al*[1] interprets the electrical properties of CdS/Cu_2S solar cells in terms of space-charge-limited currents (SCLC) with trapping by specific electron traps. Their conclusions are totally at variance with the cell model that forms the basis for research and development at IEC. The present note points out a number of errors and inconsistencies in the work of Partain *et al*[1], revealing that SCLC effects are not properly invoked.

As is well known[2], the linear variation of log J with V characteristic of a simple diode is not always seen in CdS/Cu_2S solar cells. Instead, especially in cells of low efficiency, there is a discontinuity of slope, typically around 0.3V in the light, and this has been interpreted at IEC[3] by means of an equivalent circuit containing two diodes with different diode factors. The interpretation of Partain *et al*[1] rests on identifying this discontinuity in slope of log J versus log V with a superficially similar feature observed in many solids where conduction is by SCLC. Taking the reservoir of conduction electrons as given by an unspecified process, they model the behavior of the cell by equations appropriate to a different type of system.

No mention is made by Partain *et al*[1] of the well-known instability of the dark J-V curve. Since they do not specify the time elapsed between their readings, one can only interpret their values of J in the dark as having fallen

by an uncertain amount as a result of this instability. A reduction of this type, faster at high V, has been found at IEC in CdS/Cu_2S held at constant forward bias in the dark. Failure to recognize this instability vitiates the results of Partain et al[1], as their V_{TFL} can move in an uncontrolled manner.

Other inconsistencies are seen in their derived behavior of the trapped hole density, p_{to}. They assume that a change in slope of their plots occurs at V_{TFL}, the trap-filled-limit voltage of SCLC theory, and derive p_{to} as a function of heat-treatment time, finding that it decreases rapidly for the first 150 minutes of H_2 heat treatment. This is inconsistent with the known increase with heat treatment in density of the impurities which trap holes[4] in CdS.

In the same way, Partain et al[1] derive a slight decrease in p_{to} upon illumination at AM1. This is in contrast to the known effect of hole trapping caused by white-light excitation. The equations they use, based on a multi-trap SCLC model, could equally well fit any diode curve. They switch to a single-trap SCLC model to fit plots of log J vs. log V in the dark at three different temperatures. In spite of their use of four adjustable parameters for each plot, the fit is only moderately good and certainly cannot be interpreted as confirming their model.

Contrary to the claim of Partain et al[1], there is no significant agreement with the results of Grill et al[5] who used DLTS to obtain energies and densities of eight or nine electron traps in CdS. Since any nine different numbers within a range have an average fractional spacing 1/8 of the range, Partain et al's claim that their energies agree with those of Grill et al within 15% seems puzzling at best. Table 1 allows one to judge this and their claim to agreement in the results for N_t.

In summary, the observed behavior of the CdS/Cu_2S system is not explained by SCLC. Identification of V_{TFL} with the voltage at which the slope of log J - log V plots change is not in accord with observation nor with the interpretation of SCLC theory. Electrical properties of CdS/Cu_2S solar cells such as the dark-light crossover and evolution with heat treatment can be understood much more easily in terms of the model developed at IEC and its physical interpretation is much more realistic than SCLC as applied by Partain et al[1].

TABLE 1

Trap No.	Results of Grill *et al* $E_c - E_T$ (eV)	N_t (cm^{-3})	Results of Partain *et al* $E_c - E_T$ (eV)	N_t (cm^{-3})
0	.210	10^{13}	.17	5.0×10^{14}
1	.270	10^{12}		
2	.330	10^{12}	.31	1.1×10^{15}
3	.360	6×10^{13}		
4	.420	10^{13}	.44	6.0×10^{14}
5	not well resolved	———		
6	.625	$10^{14} - 10^{15}$		
7	not well resolved	———		
8	.735	$10^{14} - 10^{15}$		

References

1. L. D. Partain, G. A. Armantrout, J. Leong and P. Warter, J. Electronic Mats. 9, 467 (1980).

2. A. Rothwarf and K. W. Boer, Prog. Sol. St. Chem. 10, 71 (1975).

3. H. Hadley and J. Phillips, p. 134 in Cadmium Sulfide Solar Cells & Other Abrupt Heterojunctions, NSF Workshop, Newark, Delaware, 1975 and Semi-Annual Rept. For July 1 - Dec. 31, 1977, CdS/Cu_2S Hetero-Junction Cell Research, EG-CC-7-03-1576, IEC, Newark, DE., May 1978.

4. G. A. Sullivan, Phys. Rev. 184, 796 (1969)

5. C. Grill, G. Bastide, G. Sagnes and M. Rouseyre, J. Appl. Phys. 50, 1375 (1979).

Appendix B

Photocapacitance Study of Hole Traps in CdS/Cu_2S Solar Cells

W. J. Manthey

INTRODUCTION

Current collection efficiency in heat-treated CdS/Cu_2S solar cells is substantially higher under AM1 illumination than at lower intensities[1]. This effect is attributed to an increase in electric field at the Cu_2S-CdS junction, caused by hole trapping in the CdS. Electrostatic theory gives the dependence of the capacitance of this junction on electric field and hence on trapped hole density.

The experiment described in this report used variation of capacitance following abrupt changes in illumination, as a probe of the dynamics of hole trapping. The hole traps are, as usual, assumed to be Cu impurity ions diffused across the junction from the Cu_2S into the CdS[2]. They act as acceptors and, in the dark, compensate the native donors, resulting in a much smaller capacitance in the dark because of the widening of the depletion region accompanying the decrease in net fixed positive charge density in CdS near the junction. When the cell is illuminated, this charge compensation is partially cancelled, because the short-wavelength component of the light generates electron-hole pairs in the CdS and the holes are trapped.

Here we investigate mainly the behavior of the hole traps following an abrupt cut-off of blue light. This allowed measurement of emission rates of

the trapped holes and their temperature variation. Possible mechanisms for the hole emission and their significance to the junction field are discussed.

EXPERIMENTAL PROCEDURE

Measurements performed on a typical IEC CdS/Cu_2S cell, 21065.111, (AM1 values: J_{SC} = 15.45 mA/cm^2, V_{OC} = .512 V, FF = 61%) which had been heat treated in H_2 at 170°C for 16 hr, at 150°C for 197 hr, and at 130°C for 16 hr. Capacitance, conductance, and sometimes current were measured with the set-up described earlier[3] in the dark, at AM1, and under blue light, over a range of temperatures from 77.5 to 297K. Blue excitation consisted of intense light from a tungsten-halogen lamp passed through glass color filters so as to produce a band between about 365 and 585 nm. This excitation was chosen for optimum photocapacitance response - that is, large increase over dark capacitance.

Temperature was maintained in a cryostat using an inert exchange gas in thermal contact with liquid nitrogen and a heater contolled within 1 or 2K using a Pt resistance thermometer. In measuring temperature variation of capacitance density C/A, conductance density G/A, and short-circuit current density $J_{SC} = I_{SC}/A$ (where A = .96 cm^2 is cell area), the cell was cooled to liquid nitrogen temperature in the dark, held there for at least 30 minutes, then brought back to room temperature. This procedure was repeated under AM1 illumination, obtained by adjusting the lamp until measured J_{SC} at room temperature matched the result obtained in the solar simulator.

To cover the eventuality that C passed through an extremum, temperature was varied up and down in a progressively narrower range until a steady-state

extreme value was reached. This brought the accuracy of the temperature to about $\pm$ 3K. Variation of C/A and G/A with temperature was also observed under blue light. Here intensity was set as high as possible, so as to give J_{sc} about 1.5 times the AM1 value.

In order to observe C/A decay, an electrically operated shutter (opening time 3.0 msec, closing time 4.2 msec) was inserted into the optical path. Outputs of the lock-in amplifier proportional to C and G were fed into a strip-chart recorder moving at 15 cm/min. Rise time following turning on the light was too short to be read accurately, so that only decay time following turning off the light has been analyzed. Each run took about 25 minutes. Two runs were made at each of the following temperatures: 77.5, 85.0, 97.1, 117.0, 190.0 and 293.0K. Only the C decay at DC bias V = 0.6V has been thoroughly analyzed here, although G decay was also recorded at this bias, as well as C decay at zero bias.

RESULTS

Capacitance in the dark at zero bias is small and almost independent of temperature, dropping from 3.3 nF/cm^2 at 297K to 3.0 nF/cm^2 at 78K. Conductance in the dark is also small, about 0.2 mS/cm^2 at 297K, and its change with temperature was not accurately determined.

Under illumination, the values and their thermal variation are much larger. C_{AM1}/A = 47.8 nF/cm^2 at 297K. Figure 1 shows schematically the temperature dependence of C_{Am1} and I_{sc} over the accessible range. The maximum in capacitance at 85K and the minimum at 223K are accurate within 2 or 3K, but the location of the other features may owe something to thermal lag. Current, after rising slightly upon cooling below room temperature, then falls steadily to a value

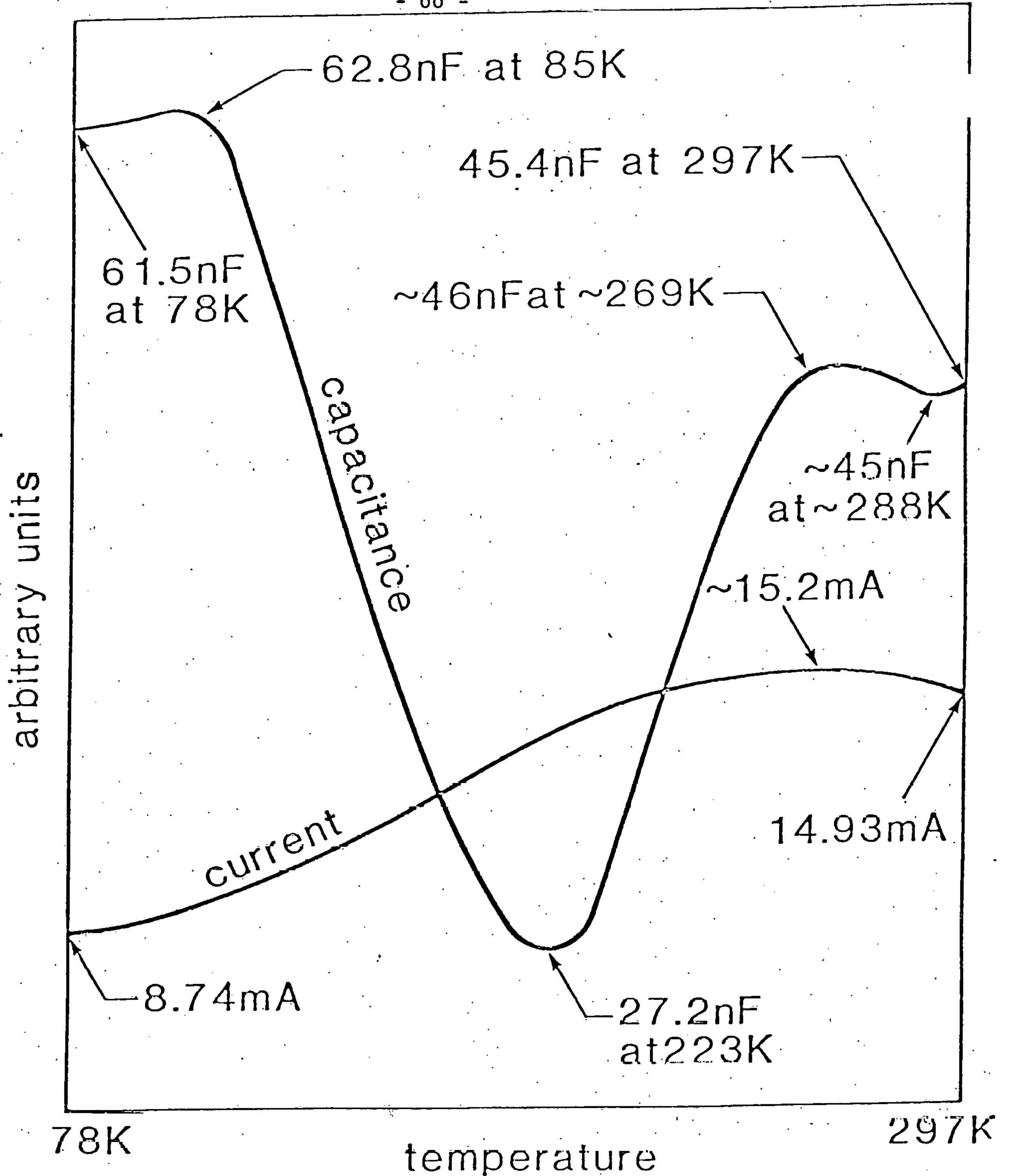

Figure 1. Cell 21065.111. Schematic temperature variation of photocapacitan and short-circuit current under AM1 excitation.

at liquid nitrogen temperature a little above one-half its origial value. Variation of G/A is quite different from that of C/A, and rises from about .85 mS/cm^2 at room temperature to 1.07 mS/cm^2 at 260K, falling to .41 mS/cm^2 at 130K, and then rising sharply to about 1.3 mS/cm^2 at liquid-nitrogen temperature.

Figure 2 shows the same data for C_{AM1}/A, along with capacitance behavior under blue light. The observation that the extrema at 85 and 223K under AM1 are matched pretty closely under blue light, indicates that the capacitance variation is not strongly wavelength dependent.

Variation of C with V in the dark at room temperature is, as expected, very slow. It is not quite as slow as liquid nitrogen temperature, and the following effective donor densities can be estimated from slopes of $(A/C)^2$ vs. V plots:

$N_D^* = 2 \times 10^{16}\ cm^{-3}$ at 297K

$N_D^* = 3 \times 10^{15}\ cm^{-3}$ at 78K

However, it is possible that a steady state was not achieved at the lower temperature, and this would result in an unrealistically high value of N_D^*.

Figure 3 shows time decay of the capacitance at 6 temperatures. Although decay rate increases as temperature goes from 77.5K to 190.0K, it is notable that the increase is not nearly as rapid as would be expected for a process involving an energy level far above the valence band (a "deep level"). Decay of G/A appeared qualitatively similar, and no analysis of this has been attempted.

ANALYSIS

Hole traps in this system consist of impurities diffused into the CdS from the Cu_2S during heat treatment[2]. Over a certain range of X, the distance

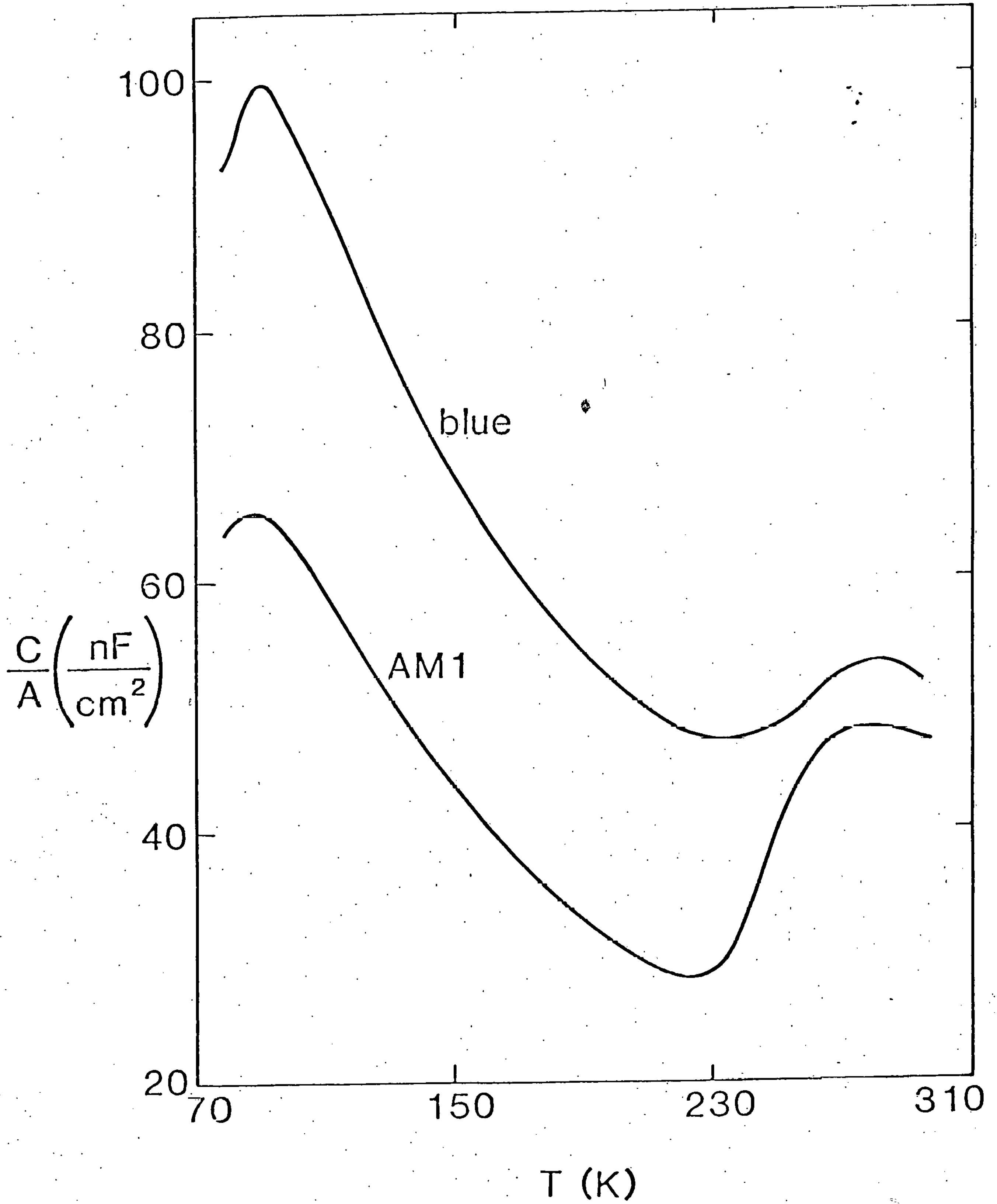

Figure 2. Cell 21065.111. Temperature variation of photocapacitance under AM1 and blue excitation, IEC80307

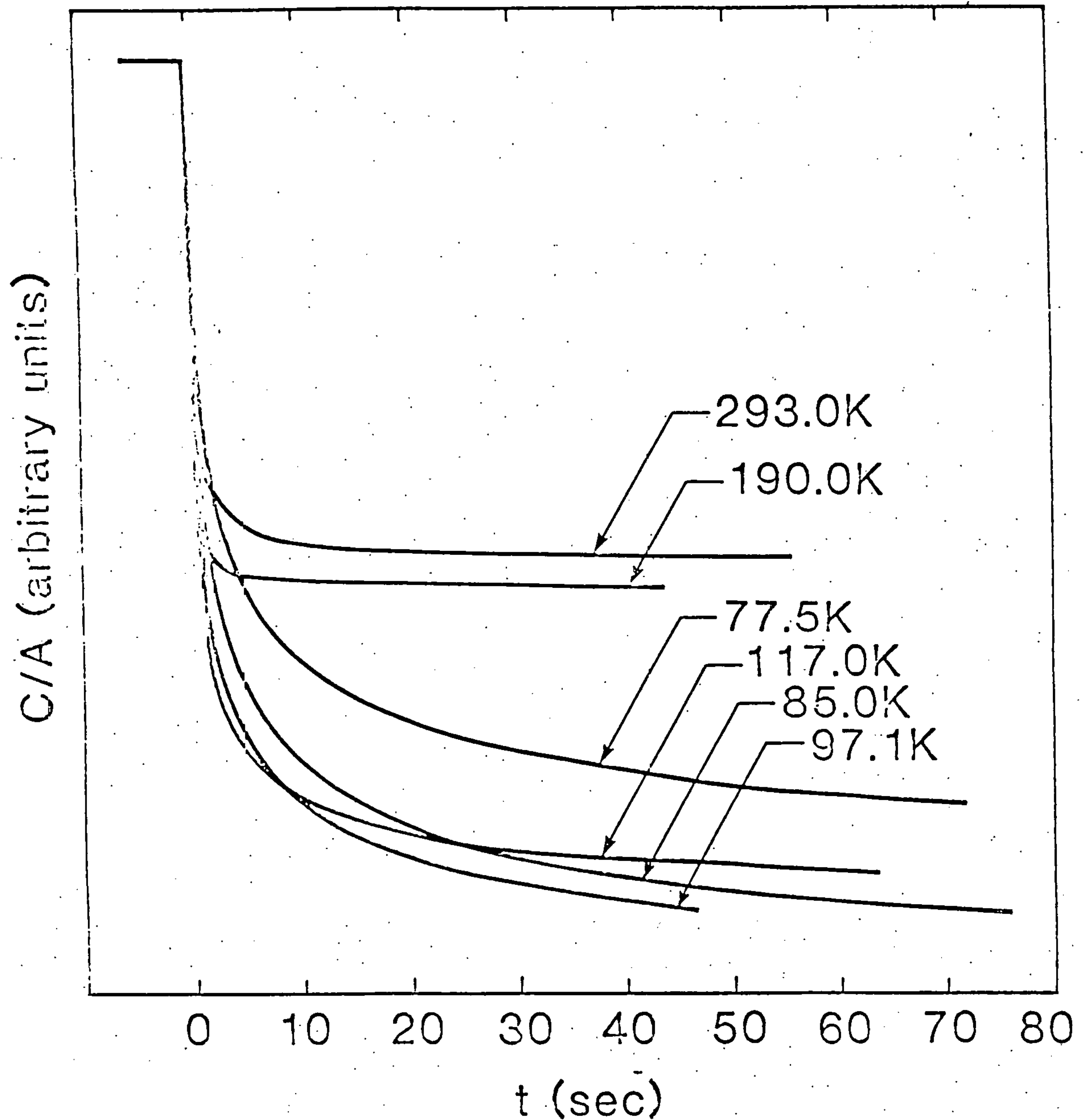

Figure 3. Cell 21065.111. Time decay at six temperatures of photocapacitance after shutting off blue light at t = 0.

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from the junction into the CdS, hole trap concentration N_T may vary as erfc (X) or some other rapidly varying function. However, wc can assume that, after heat treatment as extensive as used here, N_T is uniform over the range of interest of X. It is further assumed that the hole traps are acceptors - that is, they are negatively charged when the system is in equilibrium (in the dark) and uncharged when they contain trapped holes.

The observed weak temperature dependence of the capacitance decay rate strongly suggests that a mechanism is active other than thermal emission from the impurity level to the valence band of the CdS. The following treatment of variations of P_T, trapped hole density, is based only on a temperature dependent decay coefficient e_p, without any assumptions concerning the nature of the decay mechanism. Specifically, tunneling with or without high field effects is not ruled out, except where we assume a particular temperature dependence of e_p, in equation (17) and the calculation of ΔE_T and σ_p.

Under illumination, holes in CdS are generated and trapped at rate G and recombine at rate $e_p P_T$. Thus the net increases per second at any X is[4]

$$\frac{dp_T}{dt} = G - e_p P_T \qquad (1)$$

If P_T reaches a steady-state value of P_{TO}, and the illumination is then turned off so that G = 0, the concentration remaining after time t is

$$P_T\ (X) = P_{TO}\ (X)\ \exp\ (-e_p t) \qquad (2)$$

where the X dependence is explicitly indicated.

In most earlier studies of capacitance transients,[5-10] it was assumed that either C or C^2 varied linearly with P_T, so that, with $C = C_\infty$ at long times, the quantity $C - C_\infty$ or $C^2 - C_\infty^2$ approached zero exponentially. That this time dependence is not experienced in the present experiment is shown in Figure 4, since the data do not produce straight-line plots. The theoretical analysis which follows shows that strong optical absorption in CdS causes trapped holes to be concentrated mainly very near the Cu_2S-CdS junction, and that this leads to a different relation of C to P_T.

Replace G in equation (1) with $\alpha\Phi_{eff}$, where α is the absorption coefficient for photons arriving at rate Φ_{eff}, which are "effective" in generating holes to be trapped. At X = 0 and at steady state where $dp_T/dX = 0$, equation (1) then becomes:

$$P_{TO}\ (0) = \frac{\alpha\Phi_{eff}}{e_p}$$

Within the depletion region, $0 < X < w$, this can be replaced by:

$$P_{TO}\ (X) = P_{TO}\ (0)\ \exp\ (-\alpha X) = \frac{\alpha\Phi_{eff}}{e_p}\ \exp\ (-\alpha X) \qquad (4)$$

where the exponential dependence of absorption has been used. Thus

$$\begin{aligned} P_T\ (X,\ t) &= P_{TO}\ (0)\ \exp\ (-\alpha X)\ \exp\ (-e_p t) \\ &= \frac{\alpha\Phi_{eff}}{e_p}\ \exp\ (-\alpha X)\ \exp\ (-e_p t) \end{aligned} \qquad (5)$$

Charge density under illumination is thus $N_D - N_T + P_T\ (X)$, shown schematically at the bottom of Figure 5. Here N_D and N_T are, respectively, the densities of donors and acceptors in CdS. The maximum $P_T\ (0)$ is N_T, although

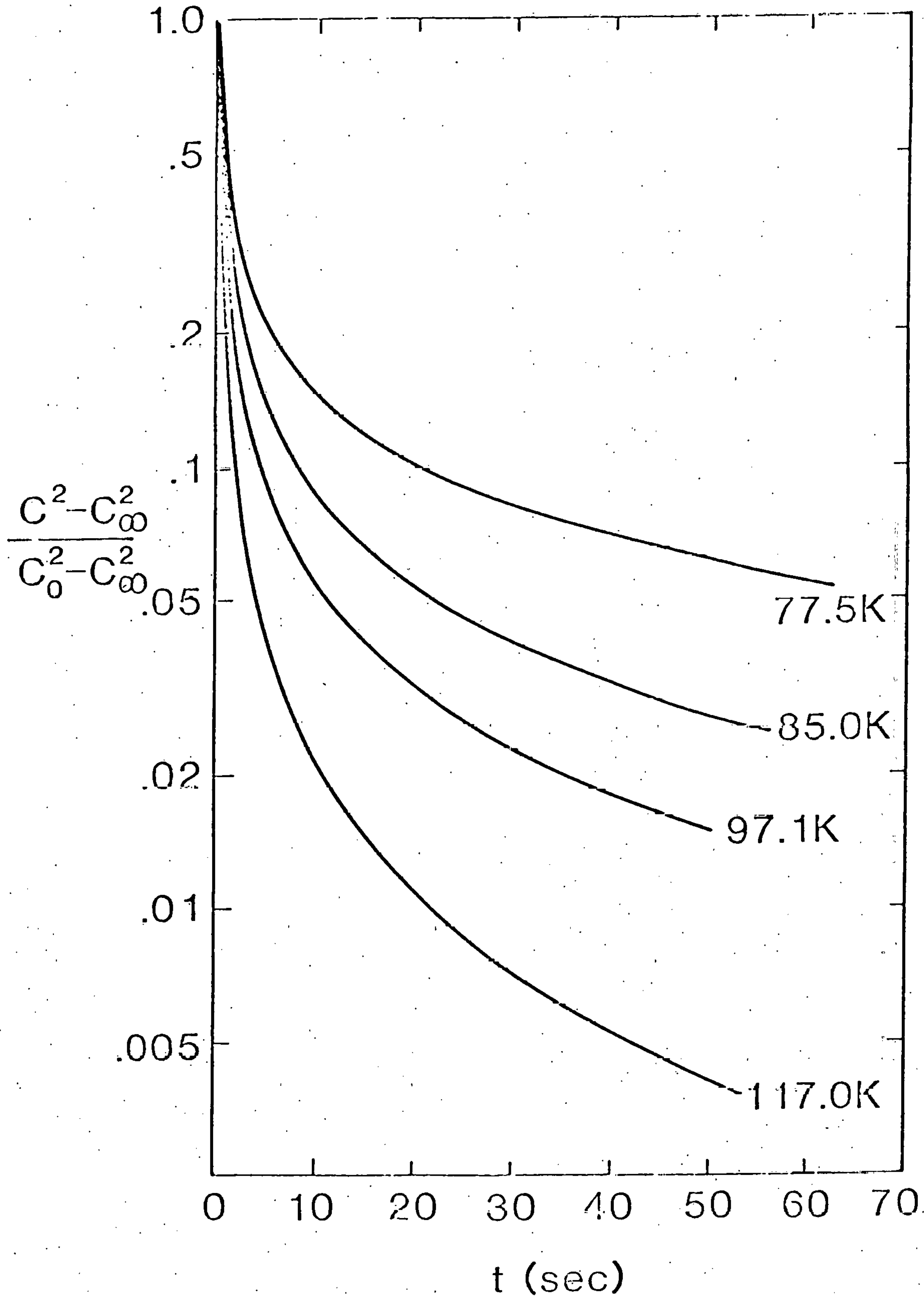

Figure 4. Same data as in Figure 3 at four lowest temperatures. Semilog plot of time variation of $C^2 - C_\infty^2$ normalized to its initial value.

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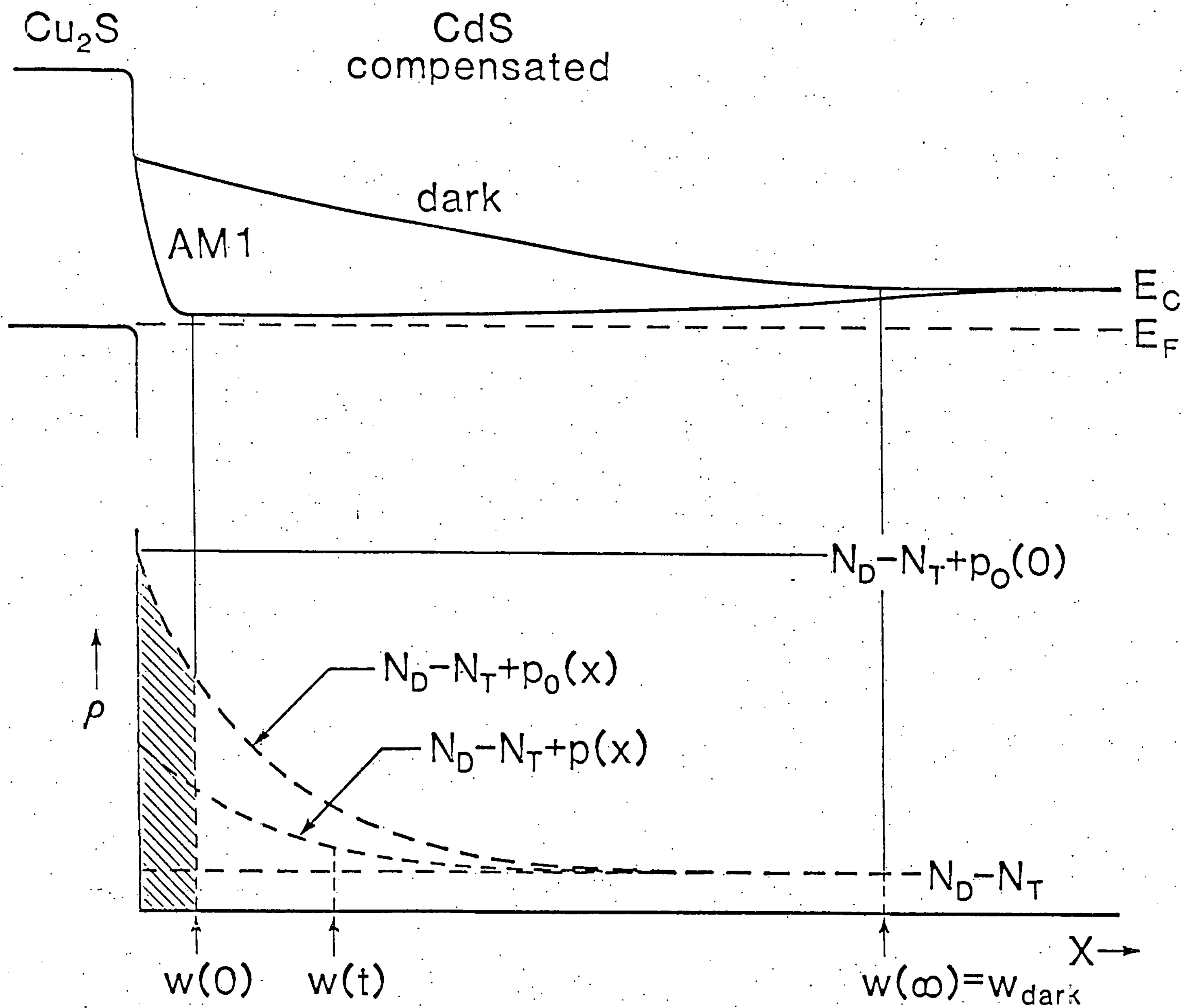

Figure 5. Partial energy band diagram and charge-density distribution (schematic) in CdS of a CdS/Cu_2S cell, showing transition from AM1 excitation until $t = 0$ to steady state in the dark as $t \rightarrow \infty$. The conduction band edge in compensated CdS pulls up from the Fermi level at E_F as the net fixed positive charge density from $N_D - N_T + P_{To}$ (X) at $t = 0$ to $N_D - N_T$ as $t \rightarrow \infty$, increasing depletion widith from w (0) to w (∞).

IEC80311

much smaller values are possible - for example, only one of several acceptors may be able to trap holes. The upper part of Figure 5 shows the effect on the conduction band of the decay of P_T. Notice that the Fermi level E_F adjusts its location to maintain zero net charge for $X > w$.

As usual, we assume acceptor density in Cu_2S to be so large that its contribution to the depletion layer width w and to the total voltage drop $V_D - V$ is negligible. Then Poisson's equation

$$\frac{d\mathcal{E}}{dX} = \frac{q}{\varepsilon\varepsilon_0}[N_D - N_T + P_T(0)\exp(-\alpha X)] \qquad (6)$$

gives upon integration the electric field within the depletion region:

$$\mathcal{E}(X) = \frac{q}{\varepsilon\varepsilon_0}\left[(N_D - N_T)(X-w) - \frac{P_T(0)}{\alpha}(e^{-\alpha X} - e^{-\alpha w})\right],\ X < w \qquad (7)$$

A second integration gives total voltage drop across the depletion region:

$$V_D - V = \frac{q(N_D - N_T)w^2}{2\varepsilon\varepsilon_0} + \frac{q P_T(0)}{\alpha^2\varepsilon\varepsilon_0}[1 - (1 + \alpha w)e^{-\alpha w}] \qquad (8)$$

where V_D is diffusion voltage and V is the externally applied bias voltage. Solving for the (time dependent) hole density at the junction, and calling w_∞ the depletion width at long time, where $t \to \infty$ and $P_T(0) \to 0$, we get

$$P_T(0) = \frac{\alpha^2\varepsilon\varepsilon_0(V_D - V)/q}{1-(1 + \alpha W)\, e^{-\alpha w}}\left(1 - \frac{w^2}{w_\infty{}^2}\right) \qquad (9)$$

This is related to capacitance by the usual equation:

$$w = \frac{\varepsilon\varepsilon_0}{C/A},\ \text{and}\ w_\infty = \frac{\varepsilon\varepsilon_0}{C_\infty/A} \qquad (10)$$

where C_∞ is simply the capacitance in the dark.

Two limiting cases, for weak and strong absorption, may be distinguished:
1) For weak absorption, $\alpha w << 1$, where hole trapping is almost constant over the depletion region, one returns to the familiar results for the abrupt junction with constant charge density:

$$V_D - V = \frac{q\varepsilon\varepsilon_o}{2} [N_D - N_T + P_T (0)] (C/A)^2 \qquad (11)$$

$$\mathcal{E}(0) = - \frac{2(V_D - V)}{\varepsilon\varepsilon_o} (\frac{C}{A}) \qquad (12)$$

$$P_T (0) = \frac{2(V_D - V)}{q\,\varepsilon\varepsilon_o} [(\frac{C}{A})^2 - (\frac{C_\infty}{A})^2], \quad \alpha w << 1 \qquad (13)$$

The last equation would predict straight lines in a plot of the type of Figure 4, in case absorption was weak enough for P_T to be uniform over the depletion region.
2) For strong absorption, $\alpha w <<1$, where hole density at the edge of the depletion region has dropped almost to zero,

$$V_D - V \frac{q\,\varepsilon\varepsilon_o}{2} (N_D - N_T) (\frac{A}{C})^2 + \frac{q\,P_T(0)}{\alpha^2 \varepsilon\varepsilon_o} \qquad (14)$$

$$\mathcal{E}(0) = - (V_D - V) [\alpha + \frac{(C_\infty /A)^2}{\varepsilon\varepsilon_o (C/A)} (2 - \frac{\alpha\;\varepsilon\varepsilon_o}{(C/A)})] \qquad (15)$$

$$P_T (0) = \frac{\alpha^2 \varepsilon\varepsilon_o}{q} (V_D - V) (1 - \frac{C_\infty^2}{C^2}), \quad \alpha w >> 1 \qquad (16)$$

Figure 6 shows photocapacitance decay plotted according to the last equation as ln $[P_T (0)/\alpha^2]$ vs t, for $\varepsilon = 10$, $V_D = .75V$. The observation that the data closely fit straight lines supports the interpretation proposed here, that exponentially decaying trapped hole density, $P_T (X) = P_{To} (X) \exp(-e_p t)$, is related to decaying photocapacitance by junction theory which takes into account a finite absorption length α^{-1}.

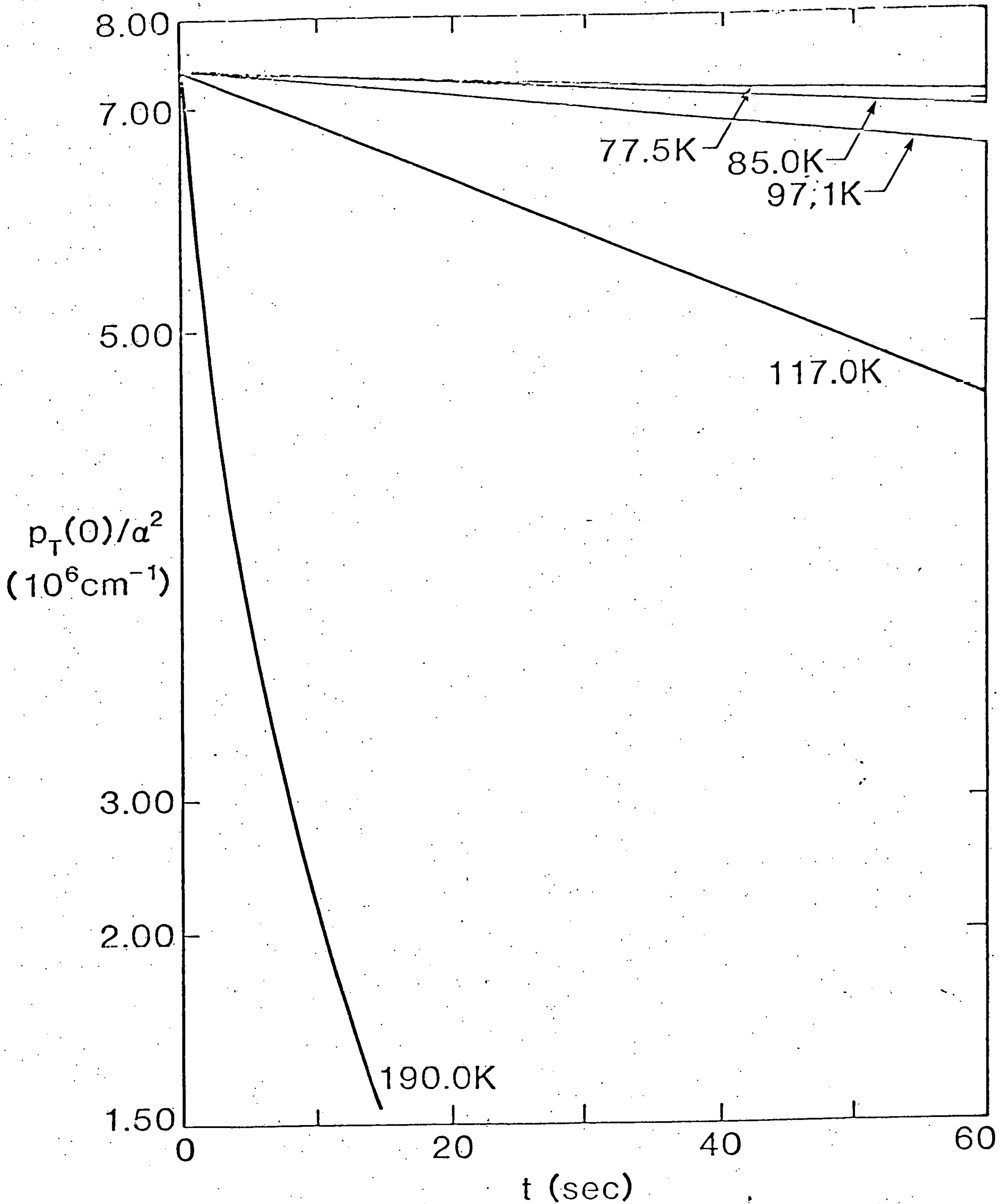

Figure 6. Same data as in Figure 3 at five lowest temperatures. Semilog plot of time variation of reduced trapped hole density at the junction, proportional to $1/C_\infty^2 - 1/C^2$.

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Table 1 gives slopes and coefficients of determination for each temperature. Equally good straight lines can be obtained by plotting the data according to the exact expression for P_T (0), equation (9), provided that α is adjusted to a high enough value. That is, if α is set lower than 5 x 10^5 cm^{-1}, the data for 77.5K (for example) produce a plot of ln [P_T (0)/α^2] vs t with noticeably decreasing absolute value of slope, similar to Figure 4. In contrast, when α reaches 5 or 6 x 10^5 cm^{-1}, a straight line results indistinguishable in slope from that in Figure 6, which corresponds to $\alpha = \infty$. The reason is that the minimum depletion width at that temperature is w = 14 μm, so that, for α = 5 x 10^{-5} cm^{-1}, the denominator of equation (9) is very close to unity.

TABLE 1

Striaght-line Fits to Curves in Figure 6

T (K)	P_{T0} (0)/α^2 = intercept (10^6 cm^{-1})	e_p = slope (sec^{-1})	r^2
77.5	6.6032	.0007160	.974
85.0	6.6049	.0009862	.991
97.1	6.6020	.001932	.996
117.0	6.6069	.008321	.9995
190.0	6.6068	.10645	.947
293.0	6.6052	.08831	.995

Thus, a value of α about 8 times the maximum value measured by Dutton[11] in pure single crystals of CdS is required to fit the data. The discrepancy may result from the presence here of an overlying layer of Cu_2S or from the

polycrystalline nature of the CdS. Also, some of the hole generation in CdS may result from transitions involving Cu impurity levels in addition to band-to-band transitions. Or, the fact that tunnelling in steady-state conditions may decrease P_{TO} for very small X may produce an effect $\alpha' > \alpha$.

Using $\alpha = 6 \times 10^5$ cm^{-1}, $\varepsilon = 10$, and $C_\infty = 0$, a maximum value for $P_{TO}(0)$ is obtained from equation (16) of $\sim 3 \times 10^{18}$ cm^{-3}. This is larger by a factor of ~ 10 than the value obtained by Sullivan[12] for the solubility of Cu in CdS at 170°C. This may point to hole trapping by mechanisms more complicated than those caused by the presence of Cu impurities, or may come from the same effect as the apparent overestimating of α.

If loss of holes is by thermal emission from a level in the band gap of CdS to its valence band, the slow temperature variation of decay rate implies that the level must be much shallower than expected. Such a process would depend on temperature according to[13]

$$e_p = \sigma_p \frac{\langle V_p \rangle}{g} N_V \exp(-\Delta E_T/kT) \qquad (17)$$

where σ_p is capture cross-section, $\langle V_p \rangle$ is thermal velocity, proportional to $T^{1/2}$, and N_V is density of states, proportional to $T^{3/2}$, all for holes in the valence band, g is a degeneracy factor, and $\Delta E_T = E_T - E_V$ is trap depth measured from the band.

In Figure 7, ln $(T^{-2}e_p)$ is plotted in the usual way against 1/T. From the slope of a straight line fitted to the data for the 5 lowest temperatures, we obtain $\Delta E_T = .038$ eV. If the effective mass of holes in the valence band is five times the free electron mass,[14] we get $\sigma_p \sim 2 \times 10^{-27}$ cm^2. This is much

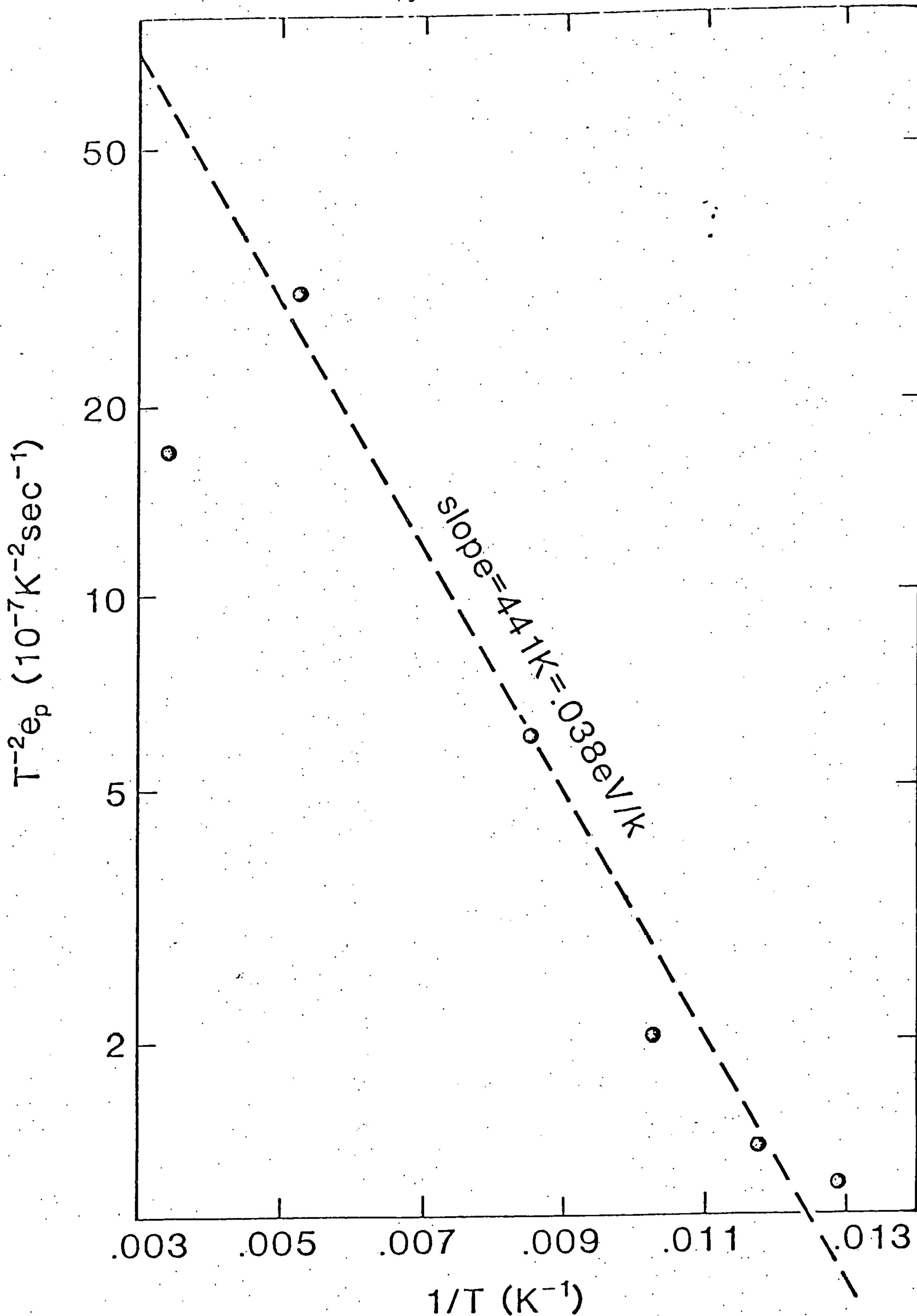

Figure 7. Semilog plot of $T^{-2}e_p$ vs 1/T, using slopes of straight lines in Figure 6 and at T = 293K. Straight line fitted to five rightmost points.

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smaller than expected, especially for a shallow level. The discrepancies in ΔE_T and σ_p make it unlikely that the mechanism involved is simply thermal excitation from an impurity state to the valence band in CdS. It is emphasized that this does not compromise the observation of decay times slowly varying with temperature, whether according to Figure 3, 4, or 6, nor the likelihood that decay is primarily by a single rate-limiting step, as indicated by the linearity of the plots in Figure 6 and Table 1.

One might speculate that holes generated in the CdS could be initially trapped in a deep state, after which they relax rapidly to a state .038 eV above the valence band. If the latter state had a very low cross-section, its rate for transitions to the valence band could vary slowly with temperature.

A more probably mechanism is tunneling. Since the region of hole trapping is very thin, of the order α^{-1}, transitions involving the valence band of the Cu_2S seem possible. According to equation (15), the electric field at the junction is $\sim 7 \times 10^5$ V/cm, and this might be able to produce high-field effects - that is, trapped holes in the CdS could pull free electrons from the Cu_2S. Note that the present model predicts a dependence of ξ on C quite different from that in[4], so that electric field is expected to have a slightly stronger effect on collection efficiency, but to vary much more slowly with illumination intensity.

Temperature variation of photocapacitance, as shown in Figures 1 and 2, is probably also a manifestation of optical absooption in CdS. Dutton[11] fitted the temperature variation of α in CdS at different energies of absorbed light $h\upsilon < E_{oo}$ with the formula

$$\alpha = \alpha_o \exp\left[-\frac{\beta}{k}\left(E_{oo} - CT - h\upsilon\right)/T\right] \qquad (18)$$

where E_{oo} is the band gap at T = 0, k is Boltzmann's constant, and α_o, β, and C are adjustable parameters. Using equation (17) for e_p, we find that $P_{To}(0) = \alpha\phi_{eff}/e_p$ has a minimum at

$$T_{min} = [\beta(E_{oo} - h\nu) - \Delta E_T]/2k \qquad (19)$$

Since C increases with P_T, one would expect a minimum in C also, above which temperature P_T would increase because of increasing absorption, and below which temperature P_T would increase because of decreasing decay rate. The minimum in C at 223K would lie between these.

SUMMARY

The photocapacitance decay experiments reported here support the importance of strong optical absorption in CdS to the current collection efficiency of the CdS/Cu_2S cell. The optical absorption model predicts exponential decay of $(1/C_\infty{}^2 - 1/C^2)$, and this is in fact observed, rather than exponential decay of $C^2 - C_\infty{}^2$ predicted by other models.

It appears that a single rate-limiting process is active over the temperature range studied, although it is not clear what this process is. Decay rate varies much more slowly with temperature than anticipated. This means that if the decay process is simply thermal emission to the valence band of the CdS, the trap energy must be very shallow and the cross-section extremely small. The possibility of other processes should be investigated, especially cross-junction tunneling of holes from traps in the CdS to the valence band of the Cu_2S.

The optical absorption model also provides a possible explanation for the strong minimum observed in photocapacitance at 223K and for slowing its increase at lower temperatures. Electric field is expected to be stronger than predicted by other models, and to be less directly coupled to capacitance.

REFERENCES

1. A. Rothwarf, Solar Cells, to be published January 1981.

2. L. R. Shiozawa, G. A. Sullivan and F. Augustine, Conf. Rec. 7th IEEE Photov. Spec. Conf., 1968, p. 36.

3. W. J. Manthey and N. C. Wyeth, Solar Cells 1, 321 (1980).

4. A. Rothwarf, J. Phillips and N. C. Wyeth, Conf. Rec. 13th IEEE Photov. Spec. Conf., 1978, p. 399.

5. J. Oualid, D. Sarti, J. Gervais and S. Martinuzzi, J. Phys. C 12, 2313 (1979).

6. J. Oualid, J. L. Granier and D. Sarti, J. Phys. C 12, 5323 (1979).

7. C. T. Sah, IEEE Trans. on El. Dev., ED-24, 410 (1977).

8. C. T. Sah, L. Forbes, L. L. Rosier and A. F. Tasch, Sol. St. Elec., 13, 759 (1970).

9. C. Merlet, G. Bastide, G. Sagnes and M. Rouzeyre, Rev. Phys. Appl. 13, 565 (1978).

10. T. Suda and S. Kurita, J. Appl. Phys., 50, 483 (1979).

11. D. Dutton, Phys. Rev., 112, 785 (1958).

12. G. A. Sullivan, Phys. Rev., 184, 796 (1969).

13. G. L. Miller, D. V. Lang and L. C. Kimerling, Ann. Rev. Mater. Sci., 7, 377 (1977).

14. B. Segall and D. T. F. Marple, p. 319 in M. Aven & J. S. Prener, Physics & Chemistry of II-VI Compounds, North Holland Pub. Co., Amsterdam 1967.

Appendix C

The Design and Fabrication of Thin-Film CdS/Cu_2S Cells of 9.15-Percent Conversion Efficiency

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Abstract—Thin-film polycrystalline CdS/Cu_2S cells with energy conversion efficiencies in sunlight of up to 9.15 percent and areas of ~1 cm^2 have been developed. The improvement over previously achieved efficiencies is due to the development of techniques to separately measure and minimize fill factor losses. Specific design and fabrication changes based on a detailed quantitative analysis of the cell operation, were introduced to correct series resistance, shunt conductance and field effect losses. Further increases in efficiency can be expected from the development of a planar junction thin-film CdS/Cu_2S cell.

I. Introduction

THE DIRECT conversion of sunlight to electricity using photovoltaic systems has the potential of providing significant amounts of energy from an inexhaustible source by means of a pollution-free process. Requirements of performance and cost for the active photovoltaic components of flat-plate arrays have been obtained from systems studies [1], [2]. There is now a measure of agreement, that thin-film polycrystalline solar cells can be developed that will be capable of producing electrical power at a cost competitive with more conventional techniques and a device based on the CdS/Cu_2S cell is a leading contender for this achievement.

The importance of demonstrating conversion efficiencies in excess of 10 percent in order to minimize area-related costs, has been underlined by the above studies. Between 1954, when a photovoltaic effect in a junction made by depositing a thin film of copper on a CdS crystal was first reported by Reynolds [3] and 1972, CdS/Cu_2S conversion efficiencies in sunlight of between 5-6 percent were reported by many investigators with a limited number of them reporting efficiencies up to 7 percent [4].

In 1972 a program was initiated at the Institute of Energy Conversion (IEC), University of Delaware, to evaluate the potential of the CdS/Cu_2S cell as a terrestrial photovoltaic converter. Improved control of materials and processes at IEC raised the reproducible conversion efficiency of the type of CdS/Cu_2S cell designed by the Clevite Corporation [5], to close to 7 percent by 1975 [6]. Improvements of energy conversion efficiencies beyond 7 percent, obtained after 1975 at IEC, were based on the development of the loss minimization method [7]. This method rests on the quantitative analysis of energy losses in a given cell design, both using experimental measurements and theoretical analysis. Information deriving from the loss analysis is utilized to make changes in cell processing until the achieved efficiency is within 5 percent of the limiting efficiency computed for the cell design under development. Although some uncertainty exists in the evaluation

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TABLE I
CONVERSION EFFICIENCY CALCULATION FOR VARIOUS CdS/Cu_2S CELL DESIGNS AND EXPERIMENTAL RESULTS ON HIGHEST EFFICIENCY CELL OF EACH TYPE IN SUNLIGHT*

Cell Design	J_{sc} [mA/cm^2]	V_{oc} [V]	FF [%]	η[%]
1. No Losses	35	0.58	81	16.4
2. Solution Grown Cu_2S				
Laminated Grid	20	0.51	69	7.1
Exp. December 1975	20.1	0.50	68	6.8
3. Hybrid Grid	23	0.51	71	8.3
Exp. July 1976	21.4	0.50	72.6	7.77
4. Evaporated Grid + AR	25	0.51	73	9.3
Exp. May 1977	25	0.515	66.9	8.55
Exp. April 1978	24.8	0.516	71.4	9.15
5. Planar two layer AR	25	0.55	73	10.0
(Cu_2S-Solid State Formation)	27	0.55	76	11.3

*Calculations are based upon an assumed AM1 intensity of 100 mW/cm^2 and Experimental J_{sc} values have been prorated linearly to 100 mW/cm^2 intensity.

of some of the loss mechanisms, it is possible to identify the major losses limiting the magnitude of the short-circuit current (J_{sc}), open-circuit voltage (V_{oc}), and fill factor (FF).

Application of the loss minimization method has led to the systematic development of CdS/Cu_2S cells with conversion efficiencies of 7.77 percent in 1976 [8] and 8.5 percent in in 1977 [9] (Table I). However, unexpected losses in fill factor prevented the latter cell from reaching its calculated limit of 9.3-percent efficiency.

In this paper, we report the improvements in cell processing and analysis which led to the development of thin-film polycrystalline CdS/Cu_2S cells with terrestrial energy conversion efficiency in sunlight of up to 9.15 percent. Further analysis indicates that significant improvements in open-circuit voltage as well as continued improvements in short-circuit current and fill factor can lead to the development of a CdS/Cu_2S thin-film solar cell with an energy conversion efficiency in excess of 10 percent.

II. CELL STRUCTURE AND DESIGN ANALYSIS

The design and fabrication of the CdS/Cu_2S cell were initially developed by the Clevite Corporation [5] and further developed by the Institute of Energy Conversion by the application of the loss minimization method [7]-[9]. Cells are fabricated using a 7.5-cm by 7.5-cm substrate of electroformed copper, approximately 25 μm thick, which is plated with 0.1-0.4 μm of Zn. CdS is vapor deposited onto the substrate held at 220°C, from a graphite source at a temperature of ~1100°C. The CdS layers obtained are typically 30 μm thick, with 5-μm grain size and 1-10-Ω · cm resistivity, although cells have been made with thickness ranging from 8-50 μm. After cutting into 3.8-cm by 2.5-cm pieces and etching the CdS in hydrochloric acid, a heavily textured light-trapping Cu_2S layer about 1000 Å thick is topotaxially grown by reaction in a cuprous-ion solution. The top electrical contact is formed by evaporating a highly transmitting (~96-percent) Au grid onto the Cu_2S surface. Finally, after cutting into 1-cm^2 cells, an antireflecting SiO_2 quarter-wave coating is vapor deposited. Further details pertaining to cell fabrication are given elsewhere [9], [10].

The loss minimization method used to develop the present cell design and fabrication process is based on a detailed analysis of the photon and carrier losses at each stage of the absorption-generation-collection sequence. The cell in use in 1975 (design 2, Table I) had a grid and encapsulant structure made by bonding a preformed gold-plated copper grid of 81-percent transparency and a protective plastic cover onto the Cu_2S, causing a J_{sc} loss of 26 percent. These losses were initially reduced by the development of a new top contact combining a vapor-deposited current-collection grid with a second bonded grid to yield a 10-percent decrease in grid shading (design 3). As a result of the above change, an increase in J_{sc} from 20.1 to 22.3 mA/cm^2 and an increase in efficiency from 6.8 to 7.8 percent were achieved in July 1976 (Table I).

Loss analysis showed that further improvements resulting in efficiencies up to 9.3 percent could be achieved by developing an all vapor-deposited high-transmission grid and a single-layer antireflection coating to increase the short-circuit current density (design 4). Further gains in J_{sc} from 22.3 to 25.1 mA/cm^2 were obtained in March 1977 with the new top surface technology [9]. However, the achieved 67-percent FF was substantially below the limit for this cell, thus limiting the efficiency to 8.55 percent. Analysis of fill factor losses for that cell design led to the identification of three types of losses: 1) field dependence of the light-generated current, 2) series resistance, and 3) shunt conductance. The magnitude of the various losses has been estimated [7] using typical values of the cell parameters yielding a design limit of 73 percent for the fill factor.

While the above analysis provides a good estimate of the achievable fill factor for a given cell design, the minimization of fill factor losses for an individual device requires the measurement of each separate loss component before corrective action can be taken. The techniques used in this work to separate, quantify, and reduce losses at the maximum power point will now be described.

III. FILL FACTOR LOSS ANALYSIS AND MINIMIZATION

Several models have been proposed to explain the behavior of the CdS/Cu_2S cell [11]-[14]. The development of high-efficiency CdS/Cu_2S cells at the Institute of Energy Conversion has been successfully guided since 1976 by the consistent application of the interface recombination model [15]. The current-voltage relation based on a generalized superposition principle [16] is given by

$$J = J_0 \{\exp [q(V - JAR_s)/KT] - 1\} + (G_{sh}/A)(V - JAR_s) - J_L(V) \quad (1)$$

where J_0 is the saturation current density, q the electronic charge, R_s and G_{sh} the series resistance and shunt conductance of the cell, and A is the cell area. The light-generated current density J_L is given by

$$J_L(V) = J_{L0}\mu_2 F_2/(\mu_2 F_2 + S_I) \quad (2)$$

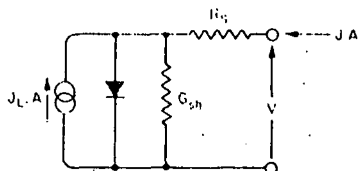

Fig. 1. Equivalent circuit representation for the CdS/Cu_2S cell.

where J_{LO} is the current incident on the junction from the Cu_2S side, μ_2 the electron mobility in CdS, F_2 the electric field at the junction, and S_I the interface recombination velocity.

A. Resistive Losses

In order to separately measure the contributions from series resistance and shunt conductance to fill factor losses, the CdS/Cu_2S cell was modeled by an equivalent circuit with lumped parameters representing resistive losses, diode properties, and photocurrent generation (Fig. 1). In addition to interface recombination, other mechanisms in the cell (e.g., CdS photoresistance, contact resistance, shunt diode, and Cu_2S sheet-resistance effects) are voltage dependent and cannot be represented by constant, lumped circuit elements. If their magnitude is small, however, linearization leads to an accurate approximation with a current-voltage relation in the form of (1). By writing this equation at open-circuit voltage, short-circuit current, and maximum power and using the relation $(dJ/dV)_{mp} = J_{mp}/V_{mp}$, valid at maximum power, a system of four simultaneous equations is obtained. If V_{oc}, J_{sc}, V_{mp}, and J_{mp} are obtained from the I-V characteristic of the cell, this system can be solved numerically for J_0, J_L, R_sA, and G_{sh}/A. For high-efficiency CdS/Cu_2S cells, a simple diode is present with a diode factor of 1, and I-V values obtained from (1) using the equivalent parameters thus calculated fit the measured curve well (see Fig. 4). The fit is exact at open circuit, short circuit, and maximum power.

Calculated values of the fill factor for various values of R_sA and G_{sh}/A for typical values of $J_0 = 7 \times 10^{-8}$ mA/cm^2 and 9 mA/cm^2 $\leqslant J_L \leqslant$ 27 mA/cm^2 are shown in Fig. 2. Analysis shows that in order to achieve $FF \geqslant$ 70 percent one must have $R_sA \leqslant 2\ \Omega \cdot \mathrm{cm}^2$ *and* $G_{sh}/A \leqslant 2 \times 10^{-3}/\Omega \cdot \mathrm{cm}^2$. A cell optimization procedure which is described below was used to determine appropriate heat treatments to correct either excessive series resistance or shunt conductance. The primary contribution to R_s has been shown to arise from the sheet resistance of the Cu_2S layer. A reducing heat treatment such as is needed to increase the short-circuit current, concurrently increases the Cu_2S resistivity to maximum value $\sim 10^{-1}\ \Omega \cdot$ cm. Computation using published analyses for optimum grid spacing [17] shows that a 32-line/cm grid should produce an R_sA contribution of $0.8\ \Omega \cdot \mathrm{cm}^2$ for Cu_2S thicknesses of 10^{-5} cm. Measurements on actual cells indicated that other factors such as grid imperfections and contributions from the CdS depletion layer were increasing R_sA above the anticipated values. Accordingly, busbars perpendicular to the main grid line were added to give a degree of current path redundancy, and the thickness of the gold grid lines was increased from 2.5 to 5.0 μm. The CdS contribution was minimized by not exceeding a total heat-treatment time (normally at 170°C) of approximately 150 h, thus avoiding excessive copper compensation of CdS.

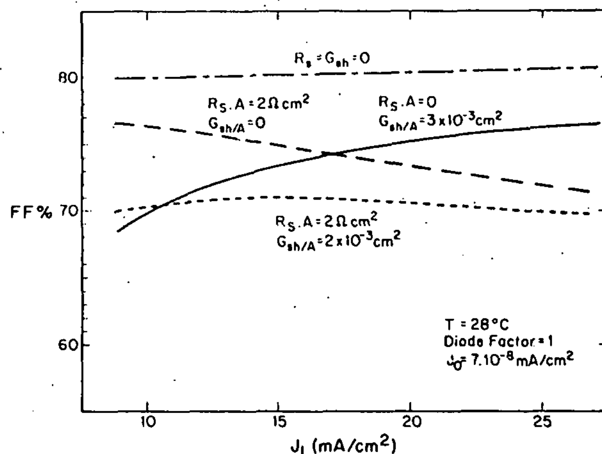

Fig. 2. Calculated values of the fill factor for the equivalent circuit representation of the CdS/Cu_2S cell.

Some cells showed a shunt conductance in excess of $2 \times 10^{-3}/\Omega \cdot \mathrm{cm}^2$ which previous research [9] had identified as arising from direct contact between the gold grid and exposed CdS. Heat treatment in a vacuum of 200 mtorr for 15 h at 170°C was effective in reducing the shunt conductance to acceptable values. Formation of either $CdSO_4$ or CdO is a plausible model for the elimination of the shunt conductance path by blocking the CdS/Au interface.

B. Field-Dependent Losses

If there is significant voltage dependence of the light generated current, the effect on the current-voltage behavior is manifest as a loss in fill factor. An on-line technique was developed to separate junction field effects from purely resistive losses. In this method [18] current-voltage data are obtained under illumination with either red- or blue-rich light of intensity equivalent to AM1. Cells with substantial field-dependent loss of fill factor (>3 percent) show a decrease in fill factor $\geqslant$10 percent upon red-rich illumination as compared to AM1.

During this study it was found that CdS layers leading to cells with minimal voltage dependence could be obtained by careful control of growth conditions. The key parameter controlling this effect is F_2 (2) which depends on the density of trapped holes in the CdS junction region and eventually on the defect structure of the as-grown CdS. A method of characterizing CdS before the preparation of cells was developed based on photoluminescence at 77 K. Material which results in negligible voltage dependent J_L shows strong exciton and green edge [19] luminescence at 488 and 520 nm. In contrast, CdS leading to cells with marked field dependence shows only a broad band of luminescence at about 620 nm.

Application of the above techniques to the analysis of fill factor losses in each individual cell, followed by the heat treatments described, consistently yielded FF values of over 70 percent at peak efficiency. The procedures developed for the simultaneous optimization of all factors controlling conversion efficiency will be described in what follows.

TABLE II
OPTIMIZATION SEQUENCE FOR CELL 680-A13. SIMULATED TESTS AT AN EQUIVALENT INTENSITY OF 83 mW/cm²

V_{oc} (V)	J_{sc} [mA/cm²]	V_{mp} (V)	J_{mp} [mA/cm²]	FF [%]	EFF [%]	R_sA [Ωcm²]	G_{sh}/A [10^{-3}/Ωcm²]	J_L [mA/cm²]	J_o [10^{-8} mA/cm²]	Treatment
.507	18.3	.409	16.4	72.0	8.06	1.55	2.27	18.4	5.64	1) Initial
.509	15.8	.413	14.5	74.5	7.24	1.62	0.83	15.8	4.68	2) LP-VHT
.505	19.4	.402	17.3	71.2	8.40	1.30	2.21	19.5	6.46	3) CO-HT
.511	16.7	.411	15.2	73.5	7.54	1.83	1.07	16.70	4.55	4) LP-VHT
.511	15.9	.412	14.0	71.0	6.95	1.84	2.49	16.0	4.13	5) Bus bars added
.512	16.9	.409	15.1	71.6	7.47	2.03	1.85	17.0	4.32	6) AR coating added
.502	20.6	.413	18.2	72.6	9.05	0.83	3.22	20.7	7.55	7) CO-HT
.505	21.0	.411	18.7	72.6	9.27	1.11	2.69	21.0	6.96	8) H_2/Ar-HT

IV. CELL OPTIMIZATION

In order to maximize cell efficiency several design and processing changes were introduced. First, the thickness of the electroplated zinc layer serving as an ohmic contact to the CdS was reduced from 0.4 to 0.1–0.2 μm. This resulted in an increase in the reflectance of the brass formed at the surface of the substrate sheet by interdiffusion of zinc and copper with shorter heat treatment [20]. While the achievable J_L depends on other factors besides substrate reflectance, increases in current leading to a maximum of 27.6 mA/cm², prorated to 100-mW/cm² intensity, were observed.

A strong relation between J_L and the Cu_2S stoichiometry has been observed [21] and may result from minority-carrier diffusion length [21] or absorption coefficient [22], [23] changes. Heat treatments in a reducing hydrogen–argon atmosphere have been previously used to achieve optimum stoichiometry [8]. It was found, however, that a 16-h hydrogen–argon treatment at 170°C generally caused unacceptable increases in G_{sh}/A. Use of carbon monoxide as the reducing atmosphere was shown to successfully achieve optimum stoichiometry while minimizing shunt losses. This effect might be due to the absence of water among the reaction products of the Cu_xS reduction by carbon monoxide. A heat treatment in carbon monoxide for 16 h at 170°C was used prior to the evaporation of the gold grid lines to insure good contact and adhesion of the lines to the Cu_2S layer. By promoting compensation of the CdS by copper diffusion and good Cu_2S stoichiometry, this preheat treatment minimizes the handling of the gridded cell, thus avoiding the consequent grid damage.

Based on the preceding analysis, a cell optimization flowchart was developed and used to achieve efficiencies over 9 percent (Fig. 3). Gridded cells were heat treated at 170°C in 16-h increments until the open-circuit voltage and light-generated current exceeded the indicated limits. Busbars and the antireflection coatings were then added and the heat treatments continued until no improvement was observed in any equivalent circuit parameter. The type of heat treatment to be given was selected according to the shunt conductance. Excessively high shunt conductance was cured by a 16-h vacuum heat treatment (HP-VHT) at 170°C and 200 mtorr. Heat treatment was at 50 mtorr (LP-VHT) for a marginal shunt conductance. When $G_{sh}/A > 2 \times 10^{-3}/\Omega \cdot cm^2$ reducing heat treatments at 170°C in carbon monoxide for 16 h were used to increase the light-generated current. Hydrogen–argon heat treatments at 170°C for 1 h were occasionally used after carbon monoxide to obtain further current increases without loss in fill factor.

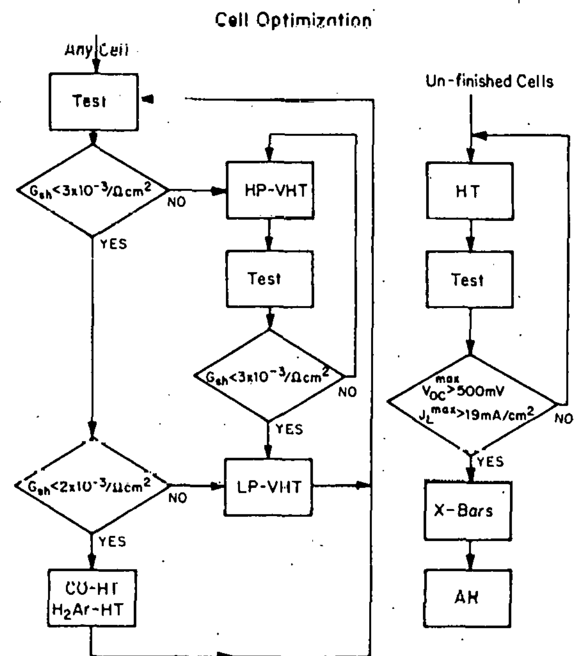

Fig. 3. Flowchart for cell optimization. (See text.)

A typical optimization sequence for a high-efficiency CdS/Cu_2S cell and the equivalent circuit parameters calculated after each optimization step are shown in Table II. Fig. 4 illustrates the effect of the various heat treatments on the current-voltage characteristics of the same cell. Calculated values using (1) and the corresponding parameters from Table III have been plotted as dots on curve 1, Fig. 4. The good agreement with measured values indicates that high-efficiency CdS/Cu_2S cells are well represented by the model used.

During the cell optimization effort 215 cells were made on 16 substrates. Over 75 percent of the cells exceeded 5-percent

TABLE III
PERFORMANCE FIGURE FOR SEVEN CELLS PRODUCED FROM 16 CdS SUBSTRATES HAVING EFFICIENCIES IN EXCESS OF 9 PERCENT. SIMULATED TESTS AT AN EQUIVALENT INTENSITY OF 83 mW/cm²

Cell	V_{oc} [mV]	J_{SC} [mA/cm²]	FF [%]	η [%]	R_s [Ω-cm²]	G_{sh} [10^{-3}/Ωcm²]	J_L [mA/cm²]	J_o [10^{-8}mA/cm²]
680 A13	505	21.0	72.6	9.27	1.11	2.69	21.1	7.0
695 A14	492	21.5	72.4	9.24	1.14	2.51	21.6	11.9
690 B13	504	20.7	73.2	9.19	1.45	1.43	20.7	7.4
680 A14	503	21.1	71.9	9.17	1.54	2.16	21.1	7.7
690 A14	506	20.9	71.8	9.17	1.67	1.95	21.0	6.8
675 B22	515	20.9	70.3	9.11	2.25	1.90	21.0	4.8
690 A13	502	21.0	71.5	9.07	1.63	2.21	21.1	7.9

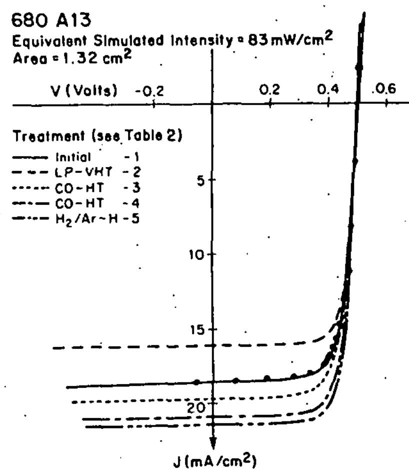

Fig. 4. Effect of heat treatments on the current-voltage curves of cell 680-A13. Curves 1 to 5 measured after 1), 2), 3), 7) and 8) (Table III), respectively. Calculated values are indicated by dots.

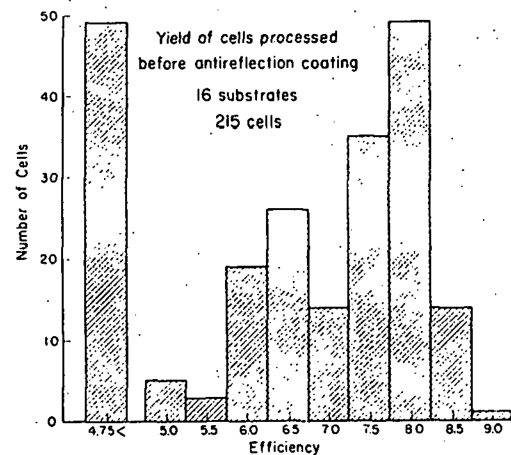

Fig. 5. Histogram of the efficiency of 215 cells produced from 16 CdS substrates.

efficiency before application of an antireflection coating, Fig. 5. Sixty five cells were then coated with a single-layer silicon monoxide antireflection layer. The resulting distribution of efficiencies is shown in Fig. 6. Of the 65 cells, 92 percent exceeded 7-percent efficiency, 72 percent exceeded 8-percent efficiency, and 11 percent exceeded 9-percent efficiency. These figures are for sunlight efficiencies computed from simulator tests. Over 35 actual sunlight tests were conducted during the cell optimization program to establish the relation between simulator and sunlight efficiencies.

The highest efficiency cell as measured in direct sunlight was cell number 690 B13. This cell under a sunlight intensity of over 87 mW/cm² achieved an energy conversion efficiency of 9.15 percent. The current-voltage curve for this cell is given in Fig. 7. The heat-treatment sequence followed to achieve maximum efficiency consisted of 1) one HP-VHT, 2) two LP-VHT, 3) one carbon monoxide heat treatment, 4) one hydrogen-argon heat treatment, and 5) six carbon monoxide heat treatments. Table III gives the performance figures for the seven cells which exceeded 9-percent efficiency as computed from the W-1 simulator tests. Climatic conditions precluded testing all cells at their peak efficiency in direct sunlight.

The separate contributions of the equivalent series resistance

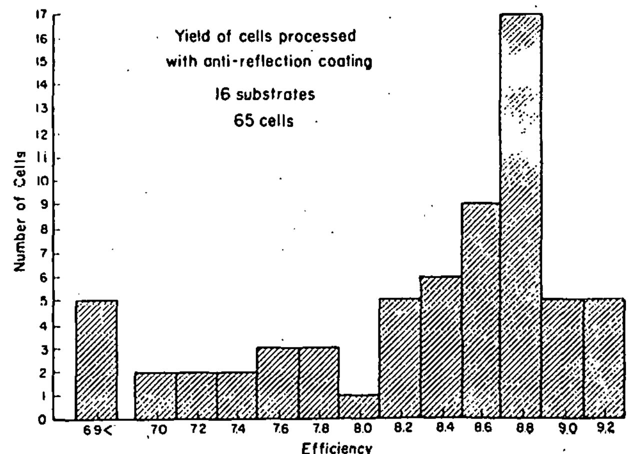

Fig. 6. Histogram of the efficiency of 65 antireflection coated cells produced from 16 CdS substrates.

and shunt conductance to the fill factor losses of cell 690-B13, measured at peak efficiency under sunlight (Fig. 7), have been calculated using the equivalent-circuit representation. In Table IV, the calculated values are compared with the achievable values estimated for this cell generation [7]. The discrepancy can be attributed to residual field effects included in R_sA as

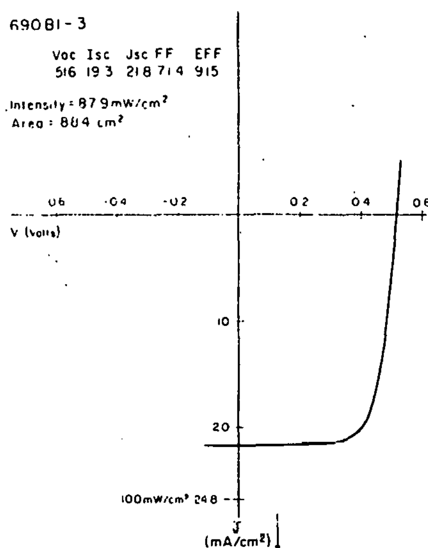

Fig. 7. Current-voltage curve of cell 690 B13 with a sunlight conversion efficiency of 9.15 percent.

TABLE IV
ESTIMATED AND ACHIEVED VALUES OF FILL FACTOR LOSSES

	Estimated Loss (%)	*Achieved Loss (%)
Series Resistance	3	8
Field Effect	3	
Shunt Conductance	2	2
Fill Factor (%)	73.0	71.4

*Cell 690 B13 at maximum efficiency under sunlight, (Figure 7). Equivalent circuit parameters: $R_s \times A = 2.07\ \Omega cm^2$, $G_{sh}/A = 1.34 \times 10^{-3}/\ cm^2$, $J_L = 21.9\ mA/cm^2$, $J_o = 4.90 \times 10^{-8}\ mA/cm^2$.

well as to the uncertainty in estimating the Cu_2S and CdS contributions. More detailed measurements of the Cu_2S sheet resistivity as well as J_L (V) measurements can contribute to the separation of the above effects.

V. SUMMARY AND FUTURE WORK

The application of loss minimization techniques to specific designs of CdS/Cu_2S thin-film photovoltaic cells has successfully identified those areas where design changes can lead to an improvement in energy-conversion efficiency. Based on this method, a new technology to deposit the top grid and AR coating onto the Cu_2S and new analysis and processing techniques to separately measure and minimize fill factor losses have been developed. This has led to reproducible improvement in demonstrated solar cell efficiencies, measured in direct sunlight, from the original level of 6.8 percent achieved in December 1975 to 9.15 percent presently reported.

Cells of the present design are believed to be limited to efficiencies of about 9.3 percent. While the heavy texture of the Cu_2S layer is a key factor in the high photon-collection efficiency of this cell [23], the extra junction area caused by the texturing and penetration of Cu_2S down CdS grain boundaries limits the achievable open-circuit voltage to ~0.51 V.

A smoother CdS/Cu_2S junction can be obtained if the Cu_2S is grown by solid-state reaction between CuCl and CdS [24]. This process eliminates grain boundary penetration and offers the possibility of separating open-circuit voltage and photon losses into two distinct problems. This cell design has led to open-circuit voltages of ~0.57 V [25] but a quantitative photon loss analysis has shown that the light-generated current is limited by reflection losses. The development of a photon efficient planar junction cell is expected to lead to achievement of energy conversion efficiencies in the range of 10-11 percent (Table I).

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REFERENCES

[1] General Electric Space Division, "Conceptual design and systems analysis of photovoltaic systems," U.S. ERDA Tech. Rep. EY-76-C-04-3686, 1977.
[2] Spectrolab, Inc., "Photovoltaic systems concept study," U.S. ERDA Tech. Rep. E(11-1)-2748, 1977.
[3] D. C. Reynolds, "Photovoltaic effect in cadmium sulfide," *Phys. Rev.*, vol. 96, p. 533, 1954.
[4] A. G. Stanley, "Cadmium sulfide solar cells," in *Applied Solid State Science*, vol. 5. New York: Academic Press, 1975, pp. 151-366 (a review of CdS/Cu_2S research through 1973).
[5] L. R. Shiozawa, F. Augustine, G. A. Sullivan, J. M. Smith, III, and W. R. Cook, Jr., Clevite Final Rep. ARL 69-0155, 1969.
[6] Institute of Energy Conversion, Univ. Delaware, "Research directed to a stable high efficiency CdS solar cells," NSF/RANN/AER Tech. Rep. 72-03478 A04 PR 75/4, 1975.
[7] A. Rothwarf and A. M. Barnett, "Design analysis of the thin-film CdS/Cu_2S solar cell," *IEEE Trans. Electron Devices*, vol. ED-24, pp. 381-387, 1977.
[8] A. M. Barnett, W. E. Devaney, G. M. Storti, and J. D. Meakin, "Increases in energy conversion efficiency for thin-film polycrystalline CdS/Cu_2S photovoltaic cells," *IEEE Trans. Electron Devices*, vol. ED-25, pp. 377-379, 1977.
[9] W. E. Devaney, A. M. Barnett, G. M. Storti, and J. D. Meakin, "The design and fabrication of CdS/Cu_2S cells of 8.5 percent conversion efficiency," *IEEE Trans. Electron Devices*, vol. ED-26, pp. 205-210, 1979.
[10] R. B. Hall and J. D. Meakin, "The design and fabrication of high efficiency thin film CdS/Cu_2S solar cells," *J. Vac. Sci. Technol.*, to be published.
[11] A. Amith, "Thin-film CdS/Cu_2S heterojunctions: Dark I-V characteristics and heat treatment," *J. Appl. Phys.*, vol. 50, p. 1160, 1979.
[12] K. W. Böer, "The physics of solar cells," *J. Appl. Phys.*, vol. 50, pp. 5356-5370, 1979.
[13] W. G. Haines, "Parameters controlling the photovoltaic properties of the copper sulfide/cadmium sulfide heterojunction," Ph.D. dissertation, Stanford Univ., Stanford, CA, 1979.
[14] T. S. TeVelde, "Mathematical analysis of a heterojunction, applied to the Cu_2S/CdS solar cell," *Solid-State Electron.*, vol. 16, p. 1305, 1973.
[15] A. Rothwarf, "Photovoltaics in heterojunctions, particularly CdS/Cu_2S," in *Proc. Int. Workshop on Cadmium Sulfide Solar Cells and Other Abrupt Heterojunctions* (Univ. Delaware, Newark), May 1975, Tech. Rep. NSF-RANN AER 75-15858, p. 9-50.
[16] A. Rothwarf, "The superposition principle for current in solar cells," in *Proc. 13th IEEE Photovoltaic Specialists Conf.*, pp. 1312-1317, 1978.
[17] N. C. Wyeth, "Sheet resistance component of series resistance in a solar cell as a function of grid geometry," *Solid-State Electron.*, vol. 20, pp. 629-634, 1977.
[18] A. Rothwarf, J. Phillips, and N. C. Wyeth, "Junction field and recombination phenomena in the CdS/Cu_2S solar cell: Theory and

experiment," in *Proc. 13th IEEE Photovoltaic Specialists Conf.*, pp. 399-405, 1978.

[19] R. E. Halsted, "Radiative recombination in the band edge region," in *Physics and Chemistry of II-VI Compounds*. Amsterdam, The Netherlands: North Holland, pp. 385–431, 1967.

[20] J. A. Bragagnolo. "Photon loss analysis of thin film CdS/Cu_2S photovoltaic devices," in *Proc. 13th IEEE Photovoltaic Specialists Conf.*, pp. 412–416, 1978.

[21] W. Palz, J. Besson, T. Nguyen Duy, and J. Vedel, "New results on solar cells," in *Proc. 9th IEEE Photovoltaic Specialists Conf.*, p. 91, 1972.

[22] L. C. Burton and H. Windawi, "Thermally induced changes of Cu_xS films and effect on CdS/Cu_2S solar cell response," *J. Appl. Phys.*, 47, p. 4621, 1976.

[23] F. Guastavino, H. Luquet, and J. Bougnot, "Etude des phenomenes de transport dans le Cu_xS ($1.79 < x < 2.00$) en fonction d l'ecart a la stoechiometrie," in *Proc. Photovoltaic Power and Its Application in Space and on Earth, Int. Congr., The Sun in the Service of Mankind* (Paris, France), p. 190, 1973.

[24] T. S. TeVelde and J. Dieleman, "Photovoltaic efficiencies of Cu_2S phases in the topotaxial heterojunction Cu_2S/CdS," *Phillips Res. Rep.*, vol. 28, p. 573, 1973.

[25] J. A. Bragagnolo, "Photon loss analysis and design of thin film planar junction CdS/Cu_2S devices," in *Proc. 2nd European Community Photovoltaics Solar Energy Conf.* (Berlin, Germany), p. 882, Apr. 1979.

Appendix D

GROWTH AND EVALUATION OF CdS AND (CdZn)S FILMS FOR THE FABRICATION OF HIGH PERFORMANCE PHOTOVOLTAIC DEVICES

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ABSTRACT

Research directed at the optimization of thin film CdS/Cu_2S and $(CdZn)S/Cu_2S$ solar cells has led to the identification of specific CdS and (CdZn)S material characteristics which are necessary for the fabrication of high performance cells. Three film properties, resistivity, photoluminescence spectral characteristics, and microstructure, have been examined and their relationship to cell performance is discussed. Specific criteria for evaluating CdS films for solar cell fabrication are presented in terms of resistivity and photoluminescence. The preliminary conclusions for microstructural effects are also described as well as the extension of this study to (CdZn)S films.

INTRODUCTION

The progressive development of CdS/Cu_2S and $(CdZn)S/Cu_2S$ solar cells has been the result of device design modifications made to optimize specific cell parameters (1,2). The evaluation of these designs and their potential success depends upon the availability of CdS and (CdZn)S films having the appropriate properties. Although the performance of the device is always the final measure of proper material, it is desirable to develop criteria, based on measured material properties, which allow the preselection of CdS and (CdZn)S films for the fabrication of cells. In addition, the understanding of these material properties provides information about the operation of the device on the one hand, and the potential for directing the parameters of film growth on the other.

Figure 1, for example, shows a schematic representation of the relationships that are sought between CdS growth parameters, measured material properties of the CdS, and cell parameters of subsequently fabricated CdS/Cu_2S devices. In general only empirical relationships can be directly established between film growth conditions and cell performance. Full understanding and control requires that a model relating specific material properties to both cell performance and growth parameters be developed and confirmed. In this paper photoluminescence, resistivity and grain structure are identified as three critical material properties of CdS films, and the manner in which each has been found to affect cell performance is discussed. A specific set of criteria used at the Institute of Energy Conversion (IEC) for the evaluation of CdS films is presented and each is discussed in terms of measured material properties and the current models for the operation of the cell (3). Additionally, the applicability of the criteria to films of (CdZn)S is discussed.

Relationships between measured material properties and cell parameters have been established which can be interpreted in terms of a quantitative model but a corresponding relationship has not yet been established between material properties and growth parameters. A major effort is currently under way at IEC to determine this relationship. The problem is highly complex due to the large number of parameters that influence film growth and the modeling necessary to understand the specific kinetics of the CdS film formation at relatively high deposition rates. Numerous and sophisticated material analysis techniques are required to identify basic film characteristics.

EXPERIMENTAL

The films of CdS and (CdZn)S are prepared by physical vapor deposition to a thickness of 30 μm on a 37 μm sheet of electroformed copper plated with 0.4 μm of zinc. The CdS or (CdZn)S deposition occurs at an elevated substrate temperature which is controlled using a thermocouple spot welded to the substrate. The CdS powder or CdS-ZnS powders are evaporated from a cylindrical graphite source bottle heated by a tantalum heater. The source temperature is monitored by a thermocouple located in a cavity which protrudes into the center of the powder. A concentric two chamber source bottle is used for (CdZn)S (4).

The controllable growth parameters are the substrate and the source material temperatures. The range of substrate temperatures that yield CdS and (CdZn)S films leading to good solar cells extends from approximately 200 to 260°C. A decreasing sticking coefficient (5) and high CdS resistivity precludes employing substrate temperatures greater than 260°C, and at temperatures much below 180°C x-ray diffraction reveals large amounts of metallic cadmium in the films. The range of source temperatures utilized extends from 850 - 1150°C. Over this temperature range and for the system geometry employed, the average rate of film growth (defined as average thickness of CdS deposited on the substrate divided by the total time

for film growth) extends from 0.2 to 4.5 μm/min.

Small sections from each of the as-grown CdS and (CdZn)S films are used for the measurement of film resistivity, photoluminescence and grain size. In addition, solar cell devices are fabricated (6) using the textured surface, solution grown Cu_2S cell design (2). The CdS was considered acceptable if a light generated current, J_L, of 20 mA/cm^2 (at 100 mW/cm^2) and an open circuit voltage of 510 mV (normalized to J_L of 20 mA/cm^2) could be obtained on any test device fabricated from the substrate.

The transverse film resistivity is determined from the resistance between the copper substrate and a pressure contact made by a 4×10^{-3} cm^2 indium dot on the film surface. The resistivity is recorded only if the current-voltage curve is linear; the average resistance from two indium dots is used, giving typically a measurements precision of ± 20%. The photoluminescence emission spectra from 450 to 850 nm is measured in Perkin Elmer MPF-44 A Fluorescence Spectrophotometer at 77°K using 340 nm excitation light.

The analysis of film grain size is made using scanning electron microscopy. The grain boundaries are revealed by forming Cu_2S on the surface of the CdS or (CdZn)S film using a CuCl solution, then stripping the Cu_2S with KCN (7). Preferential Cu_2S formation in the grain boundaries results in the formation of readily visible crevices in the boundaries. Standard quantitative metallographic techniques were used to determine the average linear intercept grain size in the plane parallel to the substrate (8,9).

DISCUSSION

Relationship of CdS Material Properties to Cell Parameters

1. Resistivity. The optimum limits on CdS resistivity which have been derived (3) assuming a CdS mobility of 100 cm^{2}v^{-1}sec^{-1} are $1 \le \rho \le 10$ ohm-cm. The upper resistivity limit is established to minimize reduction in short circuit current. The lower resistivity limit is established to minimize losses in V_{oc} by ensuring that the major portion of the diffusion voltage occurs in the CdS and assumes a Cu_2S acceptor concentration of approximately 10^{18} cm^{-3}. In practice, it has been found that even with measured resistivities as low as 0.3 ohm-cm the open circuit voltage can exceed 0.510 volts. According to the model (3), this implies that either the CdS mobility is larger (~ 300 cm^{2}v^{-1}sec^{-1}), or the Cu_2S acceptor concentrator is in excess of 10^{18}cm^{-3}.

2. Photoluminescence. Photoluminescence has been found to be a valuable evaluator of CdS films. Its particular advantage, as compared to resistivity, is that it probes the top 100 nm of the film, in which the subsequent junction with Cu_2S is formed. Figure 2 shows the 77°K photoluminescence spectrum of a good quality as-grown CdS film. The two peaks observed in the vicinity of 488 and 522 nm in the CdS, have been extensively investigated in CdS single crystals (10). The higher energy peak is an excitonic transition. The lower energy band, the green edge emission, is attributed to the recombination of a free electron with a hole bound to a native defect, particularly the cadmium vacancy, or an impurity acceptor.

In general it is found that when the edge emission peak is absent from the CdS photoluminescence spectrum, the resulting V_{oc} is lower than 0.510 volts. For example, Figure 3 shows a typical photoluminescence spectrum with only the exciton peak present. The best V_{oc}(at J_L = 20 mA/cm^2) for cells produced from this material was 0.489 volts. According to the model (3) a reduction in V_{oc} is expected when the junction barrier height is reduced as a consequence of a decrease in the ratio of N_A/N_D, where N_A is the Cu_2S acceptor density and N_D is the CdS donor density. If the edge emission does involve a cadmium vacancy, then its absence could suggest an excess of cadmium, presumably as interstitial donors which would reduce V_{oc} by increasing N_D. When there is no edge emission observed, the film resistivity is in general less than 1 ohm-cm.

The presence of the long wavelength band in the CdS photoluminescence spectra is accompanied by a spectrally dependent fill factor. Table I presents the fill factor data for cells made on CdS which exhibited the long wavelength emission band as shown in Figure 4.

Table I

Influence of Spectral Content on Fill Factor at A Fixed J_L

J_L(mA/cm^2)	V_{oc}(volts) @20 mA/cm^2	FF(%)	Illumination
17.0	.514	67.9	AMI
17.0	.502	68.1	Blue rich
17.6	.515	51.2	Orange rich
17.6	.514	45.5	Red rich

These data were obtained using suitable cut-off filters to have either blue rich, orange rich or red rich light incident on the cell at an intensity to give a fixed light generated current. It is apparent that the defect or defects, responsible for the long wavelength emission influences the space charge in the CdS depletion region in the light (2). An actual identification of the centers responsible has not yet been made.

Photoluminescence spectra have been used to identify systematic difficulties in the CdS growth system. For example, the use of certain grades of graphite for the source bottle yielded CdS films of the desired resistivities but unacceptable photoluminescence. The cells produced using these films had generally poor performance characteristics. It is believed that impurities are incorporated in the films which result in impurity states in the CdS as well as altered growth

characteristics of the films. An acceptable grade graphite has been identified as Union Carbide AGSX.

3. Structure Analysis. Typical grain structures in vapor deposited CdS films giving good solar cells are shown in Figure 5a. In general, the average grain size of such films is 1 to 3 μm. Preliminary results indicate that cell parameters are insensitive to grain size within this range. However, under certain conditions a bimodal grain size distribution such as that shown in Figure 5b has been observed, and cells prepared on this material are found to be of low quality. In addition, these films generally do not meet the photoluminescence and resistivity criteria discussed in the following section. The bimodal grain distribution is rarely observed in CdS films, but has been a significant problem with the (CdZn)S films.

4. Selection Criteria. Figure 6 shows a schematic representation of the criteria which are applied to films of CdS grown at IEC. The first box lists the range of growth parameters presently employed to prepare material having a high probability of satisfying the selection criteria. A high yield of CdS films has been achieved that satisfy all criteria and give test cells with short circuit currents in excess of 20 mA/cm^2 and open circuit voltages in excess of 0.510 volts.

5. Application to (CdZn)S. The set of criteria shown in Figure 6 has also provided useful guidelines for the evaluation of (CdZn)S films. By adjusting growth parameters it has been possible to achieve low resistivity films, less than 20 ohm-cm, having zinc compositions up to 20%. In addition it has been found that post deposition heat treatments in a H_2 atmosphere reduced the resistivity (11) of those films which initially fail that criterion. In general, the average (CdZn)S grain sizes have been somewhat lower than in CdS, and as already mentioned, the bimodal distribution is found frequently. Work is in progress to identify conditions necessary to grow (CdZn)S films with average grain size in excess of 1 μm, and without the bimodal distribution. Photoluminescence is also being developed as an evaluative probe for the (CdZn)S. To date it is not clear what are the necessary photoluminescence characteristics but the shift in the position of the exciton peak has been utilized as a means to determine the zinc concentration.

CONCLUSION

Specific material properties of CdS and (CdZn)S films provide useful guidelines in evaluating their suitability for the production of high efficiency solar cells. Film resistivity, photoluminescence and grain size have been investigated to date.

Identifiable characteristics have been determined which discriminate between films that will produce poor cells from those which have the potential to yield cells with conversion efficiencies in excess of 8%. It is expected that the development of additional material measurements will further refine the ability to select optimum CdS as well as (CdZn)S. A quantitative model (3) has been used to interpret the relationships between the measured material properties and cell parameters. It is anticipated that future work will establish a model to determine the relationships between specific material characteristics and the growth parameters.

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The authors wish to acknowledge valuable discussions with Drs. B. Baron and J. A. Bragagnolo, and the contributions of the entire Photovoltaic Group at the Institute of Energy Conversion.

REFERENCES

1. A. Rothwarf and A. M. Barnett, IEEE Trans. on Electron Devices, Vol. ED-24 381 (1977).
2. J. A. Bragagnolo, A. M. Barnett, J. E. Phillips, R. B. Hall, A. Rothwarf and J. D. Meakin, accepted for publication - IEEE Trans. on Devices, Special Edition, 1980.
3. A. Rothwarf, Proc. 2nd E.C. Photovoltaic Solar Energy Conference, Berlin, 1979, p. 370.
4. T. L. Hench and R. B. Hall, Proc. 2nd E.C. Photovoltaic Energy Conference, Berlin, 1979, p. 379.
5. W. H. Bloss, H. W. Schock, F. Pfisterer, G. H. Hewig, Proc. of International Conference on Thin and Thick Film Technology, Augsburg, 1977, p. 241.
6. R. B. Hall and J. D. Meakin, Thin Solid Films, 63 203 (1979).
7. B. Baron, A. W. Catalano and E. A. Fagen, 13th IEEE Photovoltaic Specialist Conference, Washington, 1978, p. 406.
8. E. Eser, unpublished.
9. E. E. Underwood, "Applications of Quantitative Metallography" Metals Handbook, Vol. 8, Amer. Society for Metals (1973).
10. R. E. Halsted, Physics and Chemistry of II-VI Compounds, M. Aven and J. S. Prener, Eds., North Holland Publishing Company, Amsterdam, 1967, Chapter 8.
11. T. A. Chynoweth and R. H. Bube - to be published J. Appl. Phys. (1980).

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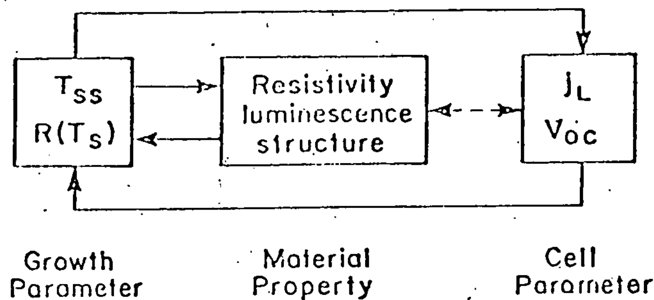


Figure 1 Schematic of relationships between growth parameters, material properties and cell parameters.

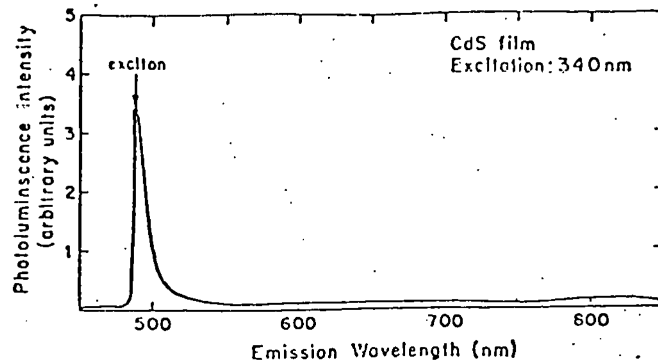


Figure 3 Photoluminescence spectrum of CdS film which yielded cells with low V_{OC}. The spectrum was obtained with the sample at 77°K.

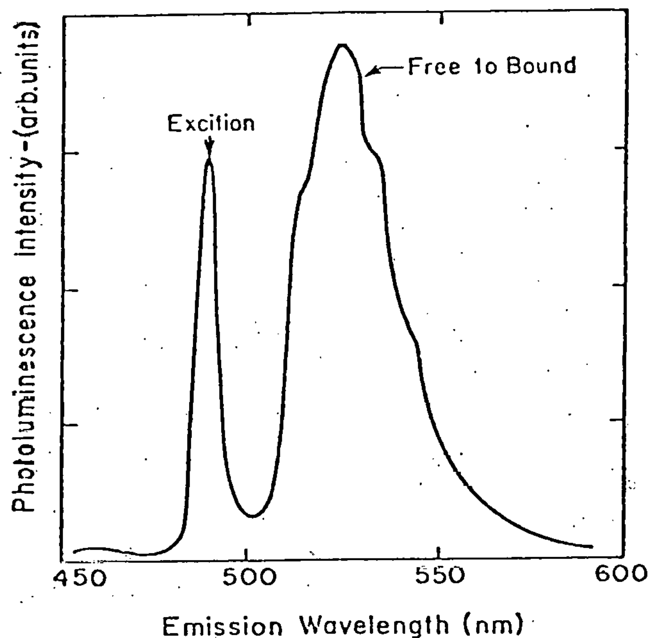


Figure 2 Photoluminescence spectrum of a typical CdS film used to prepare high efficiency CdS/Cu_2S solar cells. The spectrum was obtained with the samples at 77°K under 340 nm excitation.

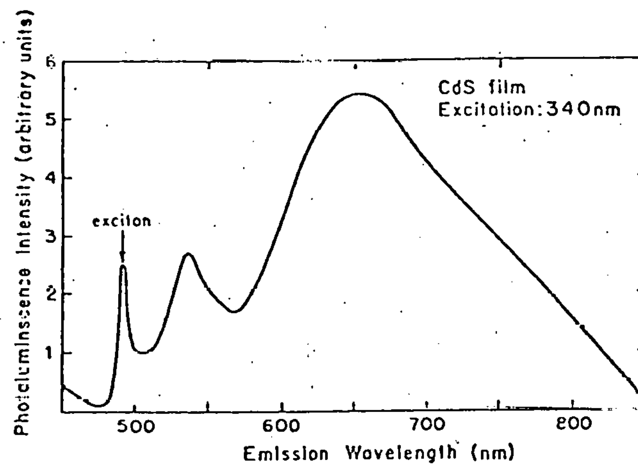
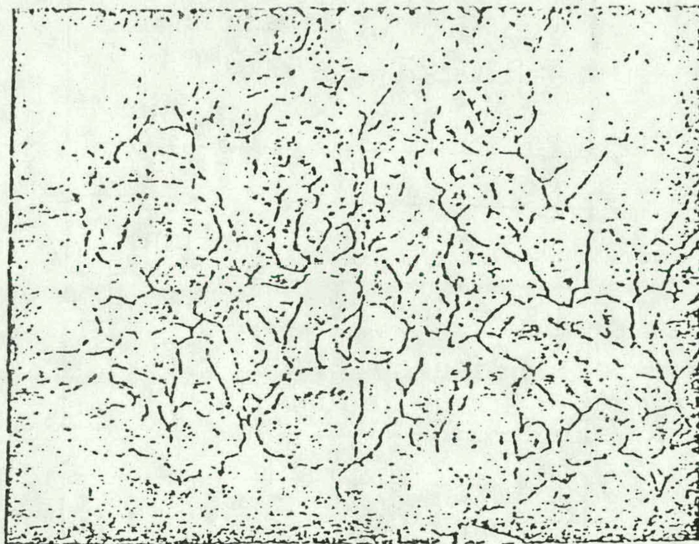
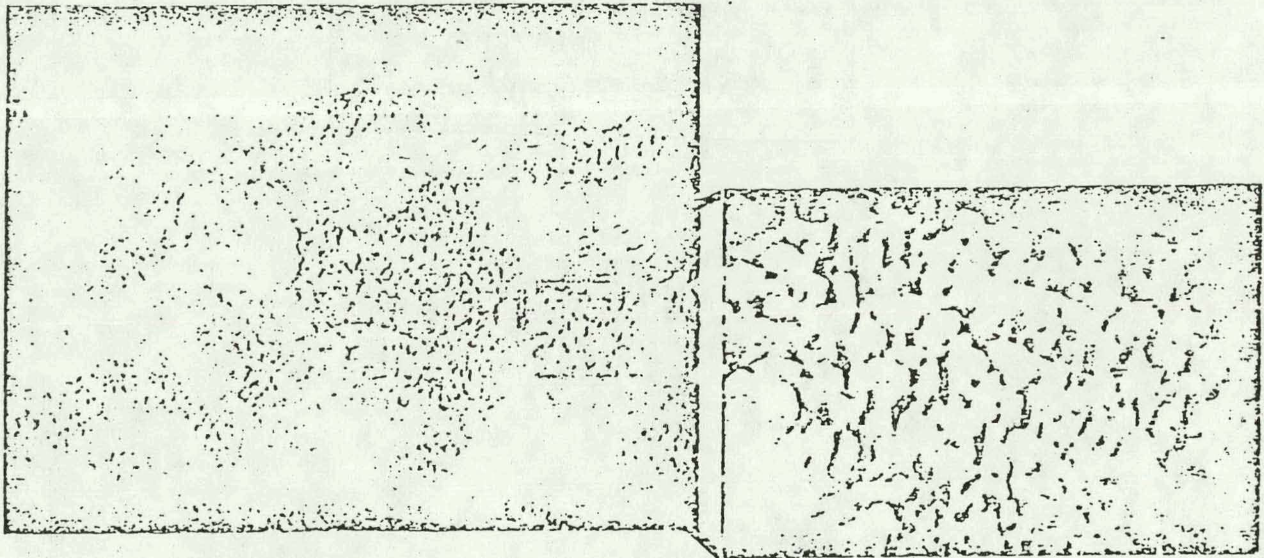


Figure 4 Photoluminescence spectrum of CdS film which yielded cells having a spectrally dependent fill factor. The spectrum was obtained with the sample at 77°K.



(a)

10 μm



(b)

Figure 5 SEM of CdS film showing grain structure of (a) film used to prepare high efficiency CdS/Cu_2S cells, and (b) film exhibiting bimodal grain structure found to yield poor cells.

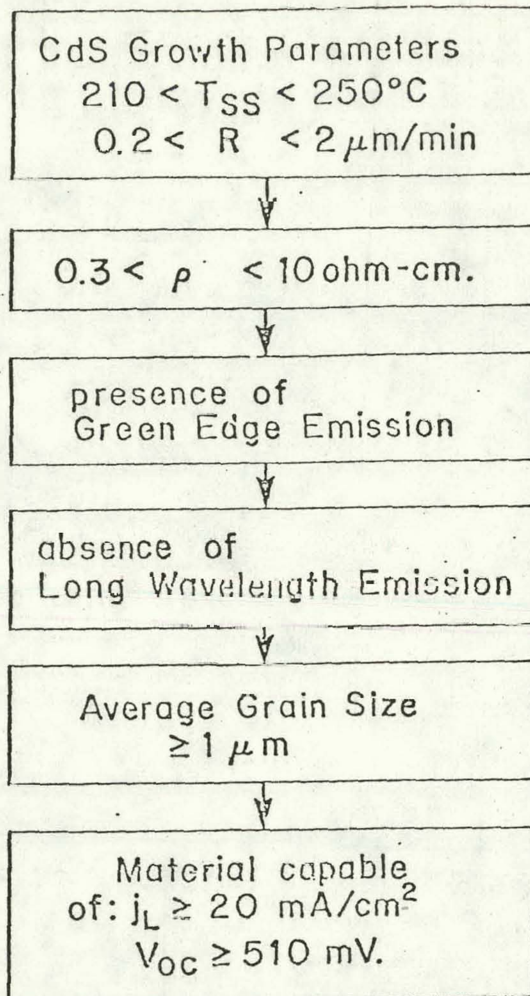


Figure 6 Schematic of evaluation criteria employed for selection of CdS films suitable for solar cell fabrication.

Appendix E

Optical Absorption Coefficient Changes in Cu_2S as the Cause of Short Circuit Current Changes in Cu_2S/CdS Solar Cells

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It is well established that the short circuit current in Cu_2S/CdS cells changes dramatically with the sheet resistance of the Cu_2S layer, and that j_{SC} and ρ/d can be cycled up and down with heat treatments in oxidizing and reducing atmospheres. High ρ/d yields higher j_{SC}. The formation of a copper oxide on the surface and its removal during the heating cycles with an attendant change in the stoichiometry of the Cu_xS layer has been established by direct electrochemical measurements. It is also well known that optical absorption in Cu_xS changes during the heat treatments in parallel with the stoichiometry. What hasn't been established quantitatively is the exact physical phenomena controlling j_{SC}. The following mechanisms have been proposed at various times.

1. Changes in crystallographic phase from chalcocite for high x and ρ/d to a chalcocite-djurleite mixture for lower x, and ρ/d, with lower absorption coefficient and hence lower j_{SC}[1]
2. Changes in the magnitude of the diffusion length of Cu_xS due to changes in the mobility of the electrons or due to changes in the minority

in working cells. The expression assumed for α in degenerate Cu_xS was

$$\alpha\ (h\nu) = A(h\nu)\ (h\nu - Eg - B_s E_F')^s$$

where $\alpha(h\nu)$ is the wavelength or photon energy dependent absorption coefficient $A(h\nu)$ a wavelength dependent factor, $h\nu$ the energy of the incident photon, E_g the band gap of the absorbing semiconductor, E_F' the position of the Fermi level above the conduction band minimum in n-type material or below the valence band maximum in p-type material, B_s a constant which depends upon the effective masses[10] and s an exponent which is 1/2 for direct gap material and 2 for indirect gap, B_s is 1 for indirect gap material and $B_s = (1 + \frac{m_h}{m_e})$ for direct gap material. Fig. 1 shows the direct transition case and why $B_s > 1$. Fig 2 shows the experimental data for α, and ρ/d and also the calculated values for $s = 1/2$, $B_s = 1, 1.5, 2.0$ and $s = 2$ cases at a wavelength of 0.65 μm.

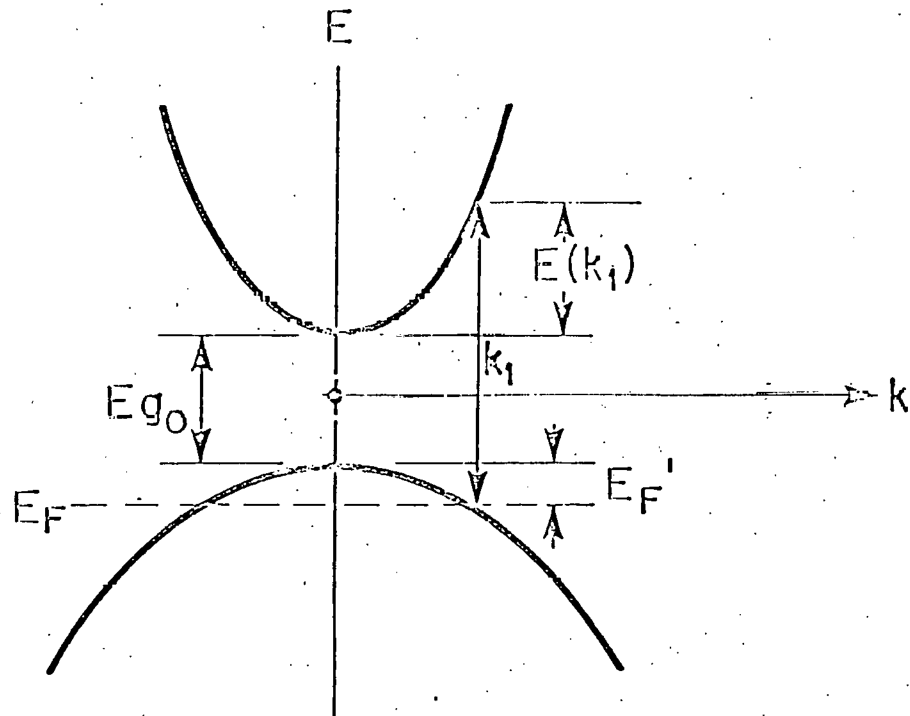
Agreement with the direct gap case $s = 1/2$, $B = 2$ is better than for the indirect gap case both from Fig. 2 and from the variation of α^2 with $h\nu$. However, the inhomogeneous nature of the sample e.g. the thickness variations in Cu_xS due to formation of Cu_xS in grain boundaries makes the conclusion ot direct nature somewhat tentative.

Calculation of the change in short circuit current that would accompany the changes in absorption seen experimentally were carried out taking into account the 80-90% reflection from the back contact and a significant light trapping at the front surface that is consistent with the measured reflectivity of actual cells. The calculated changed in j_{SC} for an AM1 spectrum range up to 20-30% for variations in α of 20% at short wavelengths to 50% at long wavelengths. These values agree very well with the changes in j_{sc} seen in actual cells.

Our conclusions based upon the experimentally measured changes in absorption in samples prepared by the same techniques as the cells are: (1) That the changes in α are sufficient to account for the observed short circuit current behavior in cells without invoking other possible mechanisms; (2) The changes in α observed are consistent with the Cu_xS being degenerate and do not require invoking a mixed phase of chalcocite and djurleite; (3) The Cu_xS absorption data and its variation with sheet resistance agree more closely with a direct band gap material than with an indirect band gap material.

References

1. W. Palz et al, Proceedings of 9th IEEE Photovoltaic Specialists Conference, Silver Spring, MD, May 1975, p. 91.
2. A. Rothwarf, International Workshop on Cadmium Sulfide Solar Cells and Other Abrupt Heterojunctions, University of Delaware, May 1975 NSF-RANN AER 75-15858, p. 9.
3. F. Pfiesterer, H.W. Schock, G.H. Hewig, Photovoltaic Solar Energy Conference, Berlin, April 1979.
4. T.S. te Velde, Solid State Electronics 16, 1305 (1973).
5. F. Massicot, Phys. Stat. Sol (a) 11, 531 (1972).
6. L.C. Burton, H.M. Windawi, J. Appl. Phys. 47, 4621-26, 1976.
7. T. Peterson, J. Washburn, Phys. Status Solidi, 22, 721 (1974).
8. J.A. Van Vechten, Ref. 2, p. 191.
9. A. Rothwarf, Photovoltaic Solar Energy Conference, Berlin, April 1979.
10. V.I. Fistul, "Heavily Doped Semiconductors," Plenum Press, N.Y. 1969.



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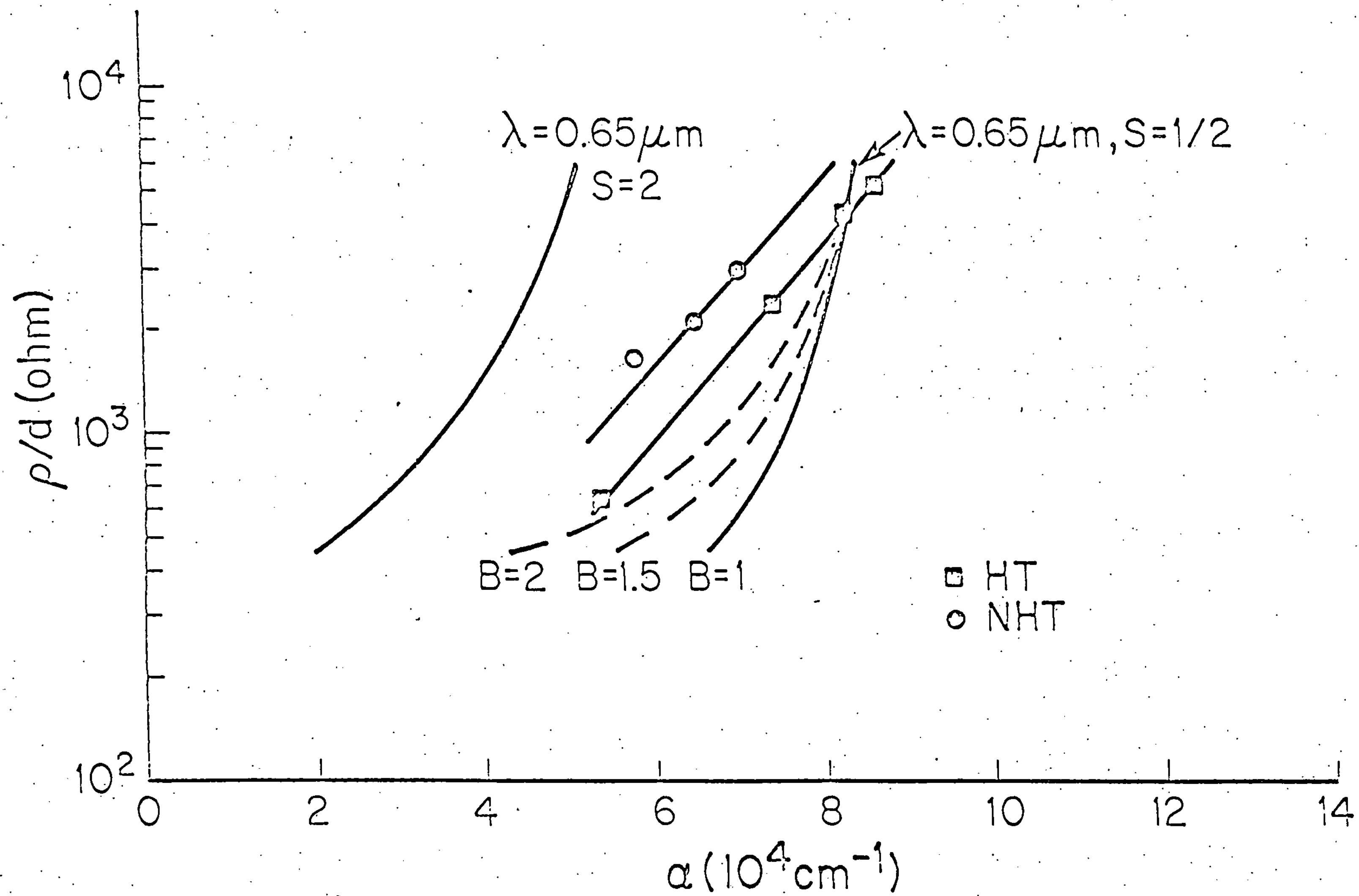
λ=0.65μm
S=2
λ=0.65μm, S=1/2
ρ/d (ohm)
B=2
B=1.5
B=1
HT
NHT
α (10⁴cm⁻¹)
IEC79009

Appendix F

Current-Voltage Analysis of the Cu_2S/CdS Solar Cell With An Interdigitated Grid

by

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ABSTRACT

The various heat treatments used to optimize the efficiency of the Cu_2S/CdS solar cell cause changes in the stoichiometry of the Cu_2S. These stoichiometry changes modify the resistivity of the Cu_2S and hence the series resistance losses due to the top semiconducting layer of the solar cell. During these heat treatments, changes are also occurring in the CdS depletion region. Because both the Cu_2S and CdS are being modified during the optimization process, it is difficult to separate the causes of fill factor and efficiency changes in the Cu_2S/CdS solar cells by examination of only the current-voltage characteristic under illumination. Also, the dark current-voltage characteristic cannot be used to separate these effects, because the junction properties are light dependent. Discrimination between various efficiency controlling mechanisms can be achieved by replacing the standard single bus bar and parallel wire grid structure with two separate bus bars to which alternate grid wires are connected. This changes the solar cell into a three terminal device which can measure both the sheet resistance and the fill factor loss due to the Cu_2S.

INTRODUCTION

The techniques for measuring the fill factor reduction due to the resistive losses of the top semiconducting layer of a solar cell can generally be divided into two categories. The first category consists of methods that rely on varying of the light flux incident on the solar cell (1,2,3), and monitoring the resultant changes in electrical characteristics. The second category is based on detailed analysis of the current-voltage characteristic (4,5).

Both procedures rely on assumptions that are usually not valid in the case of the CdS/Cu_2S solar cell. The methods that use the variations of light intensity assume that the light modifies only the light generated current of the solar cell. This is not the case in CdS/Cu_2S cells, because the CdS is photoconductive and changes in the light intensity modify both the resistive losses of the CdS and the characteristics of the CdS/Cu_2S junction (6). Those techniques that use an examination of the voltage-current characteristic assume that the deviations from ideal diode behavior are solely caused by the resistive losses of the top semiconducting layer. In the case of the CdS/Cu_2S cell this is not necessarily true and the major deviations may be the result of field dependent interface recombination (3).

In order to quantify the fill factor losses due to the Cu_2S layer on an operating CdS/Cu_2S solar cell, it was necessary to develop an experimental method that neither varies the light intensity nor assumes that deviations from ideal diode behavior are due solely to the Cu_2S layer. In addition, because the Cu_2S undergoes significant changes in resistivity during optimization (6), the method should also be able to provide an unambiguous measurement of the instantaneous Cu_2S fill factor losses.

The necessary conditions for measuring the Cu_2S losses can be met by applying an interdigitated grid consists of two sets of interleaved parallel grid wires connected to a tab or bus bar at opposite ends of the cell (see Figure 1). Testing a cell of this type with each tab individually and with both tabs connected together, gives a set of current-voltage characteristics that differ only in effective grid spacing. This grid structure also modifies the solar cell to give a three terminal device that allows (with proper precautions) the measurement of the current-voltage characteristics of the Cu_2S decoupled from the rest of the cell. This is shown schematically in Figure 2.

Because the interdigitated grid enables the current-voltage characteristic to be measured on solar cells that are identical except for the spacing between grid wires, it is a simple matter to calculate the contribution to fill factor loss caused by the Cu_2S layer ($\Delta FF'$). The effective series resistance of the top semiconducting layer is proportional to the square of the spacing between grid lines (4,5) ($R_s \alpha l^2$) and the resulting fill factor loss is proportional to the series resistance (3). From the fill factors measured at effective grid spacings of L and 2L the loss in fill factor at these two spacings can be deduced as follows:

$$\Delta FF'_{(1+2)} = \frac{FF_{(1+2)} - FF_{(1 \text{ or } 2)}}{3} \qquad (1)$$

$$FF_{(1 \text{ or } 2)} = \frac{4\,[FF_{(1+2)} - FF_{(1 \text{ or } 2)}]}{3} \qquad (2)$$

As an example, Figures 3 and 4 show the voltage-current characteristics of CdS/Cu_2S solar cell with the interdigitated grid both before and after a reducing atmosphere heat treatment (H_2 was used as the reducing gas). Table 1 summarizes the results of the measurements. Although the heat treatment has detectably increased the resistive losses due to the Cu_2S, it can be seen that these are not the major fill factor losses in this cell. Some estimate of the uniformity and integrity of the grid structure can be gained by comparing the fill factor of tab 1 to that of tab 2.

Cu_2S Sheet Resistance

The Cu_2S sheet resistance can be found by measuring the current-voltage characteristic between the two grids with an appropriate bias voltage to the back contact to block leakage currents across the junction (Figure 5). If the measurements are carried out in the dark and under illumination, current flow through the photoconducting CdS can be detected. The Cu_2S sheet resistance ($R_\square$) is given by the slope of the voltage-current curve.

$$\frac{dV}{dJ} = R_\square / L^2 \qquad (3)$$

A set of measurments are given in Table 2 in which over 145 voltage-current points were used for each regression. The current density (J) ranged from $-8\ mA/cm^2$ to $+8\ mA/cm^2$. The following formula was fitted to the data

$$V = V_o + (R_\square / L^2)\,J + C_1\,J^2 + C_2\,J^3 \qquad (4)$$

The offset voltage between the grids at zero current (V_o) was caused by the current from the bias voltage and the light generated current flowing through the Cu_2S layer. Higher order terms in J were used to determine if there was any non-ohmic behavior between the grid wires and the Cu_2S. The measurements do not reveal sensitivity to either bias voltage or light, neither do they show any indications on non-linearity in the voltage-current characteristic. A measure of the lack of non-linearity is given by the high coefficient of r^2, J, with C_1 and C_2 effectively zero. It is concluded that the technique is measuring the true sheet resistance of the Cu_2S layer, and it free from errors caused by current flow through the CdS/Cu_2S junction. This follows from the lack of variation in $R_\square$ at various junction bias voltages.

Summary

By replacing the standard single bus bar and parallel grid wire structure of a solar cell with two separate bus bars to which alternate grid wires are connected (interdigitated grid), the sheet resistance of the top semiconducting layer and the fill factor loss caused by it can be accurately measured on a cell operating under standard illumination conditions.

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References

1. Wolf, M. and Rauschenback H., Advanced Energy Conversion, 3, 445 (1963)
2. Fang, C. R. and Hauser, J. R. Record of 13th IEEE Photovoltaic Specialists Conf., 1306 (1978)
3. Rothwarf, A., Barnett, A. M., IEEE Trans. Electron Devices ED-24, 381 (1977)
4. Wolf, M., Proc. IRE, 48, 1246 (1960)
5. Wyeth, N. C., Solid State Electronics, 20, 629 (1977)
6. Stanley, A. G., Applied Solid State Sci. 5, 251-366, Academic Press 1975. Contains a review of CdS/Cu_2S research through 1973.

Table 1

Influence of heat treatment on the series resistance loss in fill factor due to Cu_2S

CELL 2-0345-12-1

Fill Factor (%)

	Measured	Loss due to Cu_2S, ΔFF'	Achievable without Cu_2S loss, ΔFF'	Maximum Achievable without loss	Loss due to other Mechanisms
before heat treatment	71.8	0.8 ± .01	72.6 ± .01	80.2	7.6 ± .1
after heat treatment	71.4	2.0 ± .2	73.4 ± .2	80.1	6.7 ± .2

Table 2

Sheet resistance measurements for CdS/Cu_2S solar cell 2-0999-21-2 with interdigitated grid. C_1 and C_2 are found to be ≤0.005. See text.

L = .03175 cm

Bias (mV)	Illumination	# of I-V points used	V_o (mV)	$R_\square/L^2$ ($\Omega\ cm^2$)	r^2 (%)	$R_\square$ ($K\Omega/\square$)
0	0	145	.05	7.13	99.9	7.07
-200	0	155	.41	7.16	100.0	7.10
-500	0	165	1.16	7.17	100.0	7.11
0	AM1	174	38.26	7.18	100.0	7.12
-100	AM1	184	39.22	7.21	100.0	7.15
-500	AM1	184	40.35	7.23	100.0	7.17

Average $R_\square$ = 7.12 ± .05 ($K\Omega/\square$)

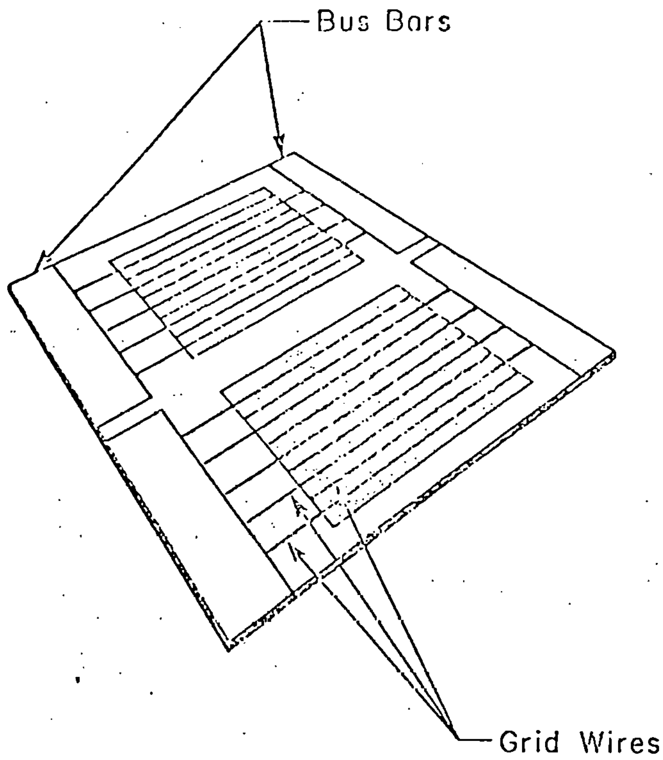

Figure 1

CdS/Cu_2S Solar Cells with an Interdigitated Grid

Cell No. 2-0940-21-1 Date: 7/17/79
area = 1.13 cm^2

	V_{oc} (V)	I_{sc} (mA)	FF (%)	Grid Spacing (cm)
Tab 1+2	.497	14.8	71.8	.0317
Tab 1	.496	14.7	69.0	.0635
Tab 2	.497	14.7	69.8	.0635

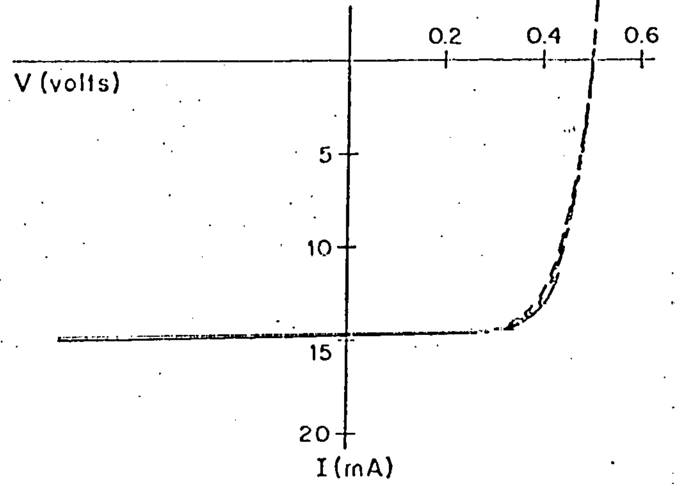

Figure 3

Current-voltage characteristics before heat treatments

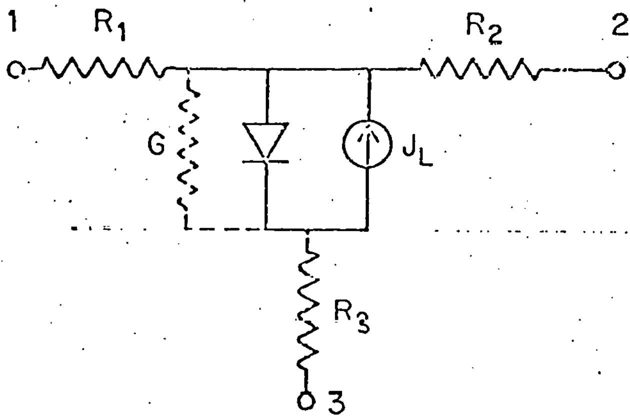

Figure 2

Three Terminal Equivalent circuit representation of a solar cell with an Interdigitated Grid.

Cell No. 2-0948-21-1 Date: 7/20/79
area = 1.13 cm^2

	V_{oc} (V)	I_{sc} (mA)	FF (%)	Grid Spacing (cm)
Tab 1+2	.493	16.4	71.4	.0317
Tab 1	.493	16.5	64.6	.0635
Tab 2	.493	16.5	66.0	.0635

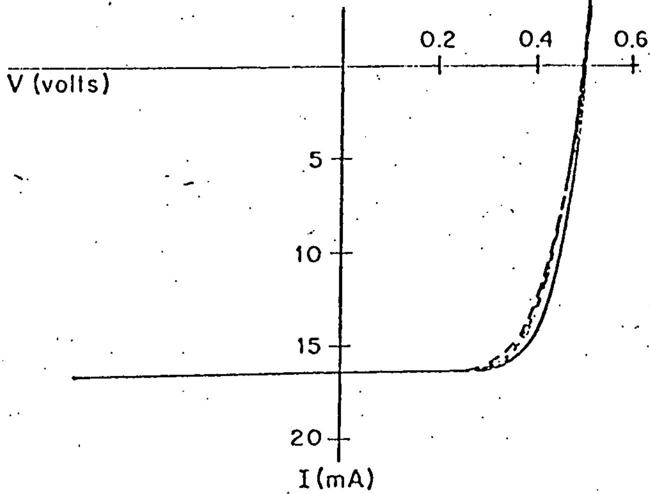

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Figure 4

Current-voltage Characteristics after heat treatments

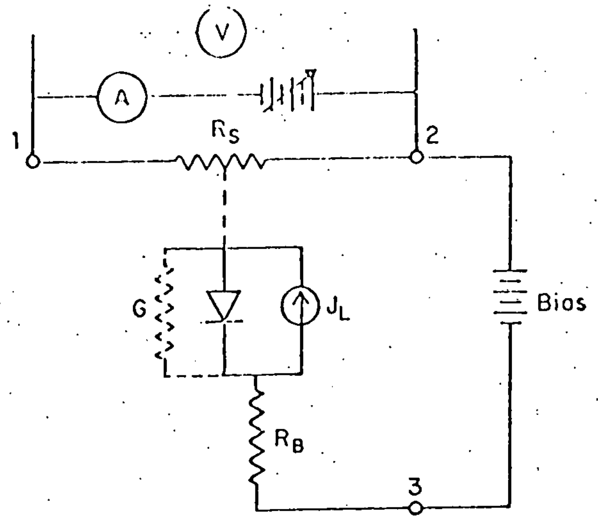

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Figure 5

Schematic of the circuit used to measure sheet resistance of the Cu_2S

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Appendix G

THIN-FILM CdS/Cu_2S CELLS WITH HIGH OPEN-CIRCUIT VOLTAGE AND LOW REFLECTION LOSSES

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ABSTRACT

A CdS texturing process and a Cu_2S formation procedure have been combined to give CdS/Cu_2S cells with low reflectance losses but with high open circuit voltages in excess of 0.54 V. As a consequence conversion efficiencies of 10% are anticipated.

1. INTRODUCTION

Thin-film polycrystalline planar junction CdS/Cu_2S solar cells with open-circuit voltages (V_{OC}) of up to 570 mV have been previously obtained by solid-state reaction growth of Cu_2S on unetched CdS layers (1). However, as the morphology of the Cu_2S layer is made smoother (Fig.1), increased reflection losses limit the light-generated current J_L of planar junction cells to about 80% of that in high efficiency textured cells. In order to achieve the potential efficiency of the planar junction cell design, estimated at over 10% (2), it is necessary to reduce the reflection losses to the levels measured in textured cells (3). In this work, we report the development of a CdS texturing process that yields "planar", high V_{OC}, CdS/Cu_2S cells with the required low reflection losses.

2. Cu_2S LAYER MORPHOLOGY

The morphology of the solution grown Cu_2S surface in a textured CdS/Cu_2S cell is shown in Fig. 2. The Cu_2S forms along the surface of the CdS and also penetrates down the CdS grain boundaries. The low $V_{OC} \leq 520$ mV of textured cells relative to planar cells is a consequence of the substantially larger junction area caused by both the grain boundary intrusions and the fine light trapping surface. A quantitative photon loss analysis (1) shows that the Cu_2S texture contributes to the photon economy of high efficiency cells in two major ways: 1) Multiple reflections of incoming light rays lower the front surface reflectance and 2) Diffuse light scattering at the Cu_2S surface and CdS/substrate interface and the acute angle of incidence of reflected light on the outer surface of the Cu_2S layer decreases the re-emission of unabsorbed light (light trapping).

In order to increase Cu_2S absorption in the planar cell it is essential to reduce re-emission losses by enhancing diffuse internal reflection. It can be shown (1) that only the small scale (0.5-1.0 μm) pyramidal structure of the Cu_2S layer is necessary to accomplish the above reduction in reflection losses. By tailoring of the fine texture coupled to the use of the non-intrusive solid-state Cu_2S growth process we have simultaneously minimized both reflection and V_{OC} losses. The proper CdS texture was obtained by reducing the HCl concentration in the etching solution from 55% by volume, as used for the conventional textured cell (1), to 25% and increasing the etching time from 2 to 20-40 sec at 60°C, at which point the desired total reflectance was achieved. The morphology of the Cu_2S surface of cells made by solid-state Cu_2S growth on lightly etched CdS is shown in Figure 3 (compare with Figure 1), where both the grain boundary and fine structure are reduced relative to the conventional textured cell (Figure 2). Use of the conventional 55% HCl etch with the solid state Cu_2S growth process yielded a Cu_2S layer with excessively thin regions, leading to cells with high resistive and J_L losses.

3. REFLECTANCE, V_{OC} AND J_L

Reflectance spectra of gridded CdS/Cu_2S devices with various Cu_2S layer morphologies are shown in Figure 4. The light texture introduced by the new process (Figure 3) is sufficient to reduce reflection losses to the level typical of conventionally textured cells. In fact, use of this process with the Cu_2S solution growth technique yields cells with the same photon economy as the conventional cell but with a substantially reduced frequency of shunt and short-circuit paths.

Values of J_L and V_{OC} (normalized to J_L = 25 mA/cm^2) achieved with the various structures are shown in Table 1. The data shows that an all evaporated thin-film CdS/Cu_2S cell can achieve efficiencies over 9% if a fill factor ~ 72% (typical of high efficiency textured cells) can be obtained with the V_{OC} and J_L values reported here. The J_L values ($\geq$ 25 mA/cm^2) necessary to exceed 10% efficiency have not yet been achieved, but the solution of the reflection loss problem is a major advance. The best J_L achieved to date is 22.2 mA/cm^2 which is within 11% of the goal. Ongoing development of the optimum Cu_2S stoichiometry and thickness and improved substrate reflectivity are expected to yield cells of over 10% conversion efficiency.

REFERENCES

1. J. A. Bragagnolo, Proceedings of the 2nd E.C. Photovoltaic Solar Energy Conference, p. 882 (1979).

References cont'd

2. A. Rothwarf and A. M. Barnett, IEEE Trans. Elec. Devices, Vol. ED24, p. 381 (1977).
3. J. A. Bragagnolo, 13th IEEE Photovoltaic Specialists Conference, p. 412 (1978).

TABLE I

Cell	HCl Concentration [% by volume]	Etching Time [sec]	Cu_2S Growth	V_{oc}* [mV]	J_L† (AM1) [mA/cm^2]
690.B13	55	2	Solution	516	24.8
20948.121	-	-	Solid State	550	18.7
20968.121	20	25	Solid State	558	22.2
21057.121	20	40	Solution	517	24.7

Typical values of V_{oc} and J_L achievable with various cell morphologies

* Normalized to J_L = 25 mA/cm^2

† Experimental J_L values prorated linearly to 100 mW/cm^2 intensity

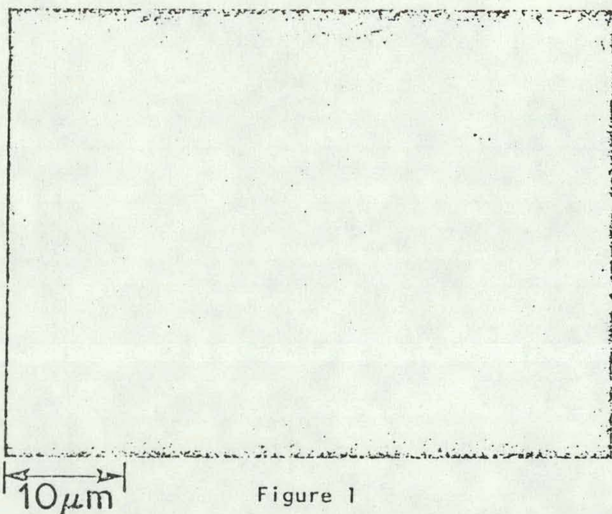

Figure 1

SEM view of the top surface of a planar cell with solid state grown Cu_2S (mag. 2000 X)

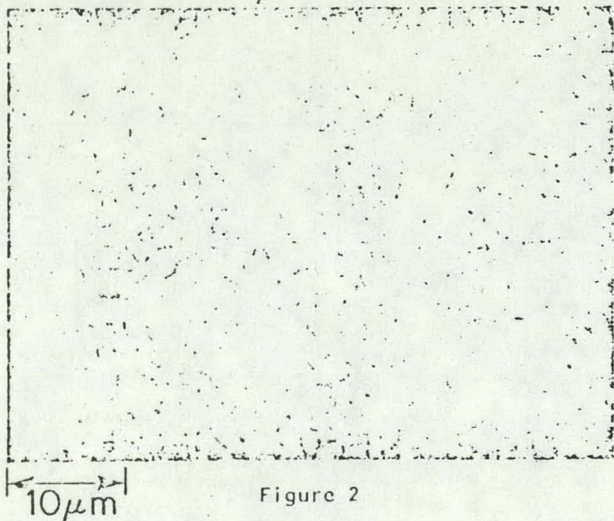

Figure 2

SEM view of the top surface of a conventionally textured cell with solution grown Cu_2S layer (mag. 2000 X)

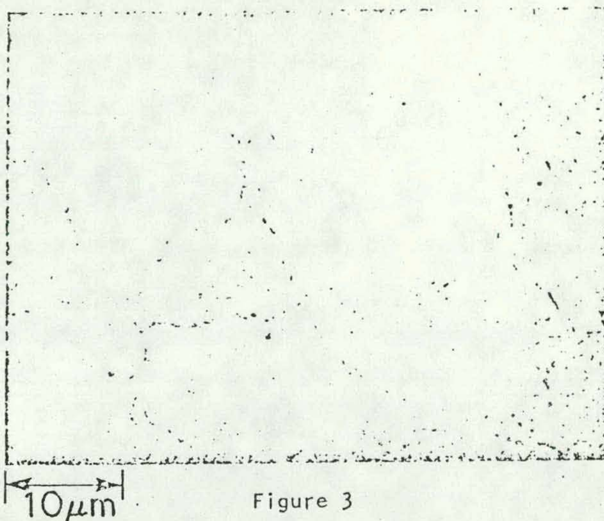

Figure 3

SEM view of a lightly textured cell with solid state grown Cu_2S (mag. 2000 X)

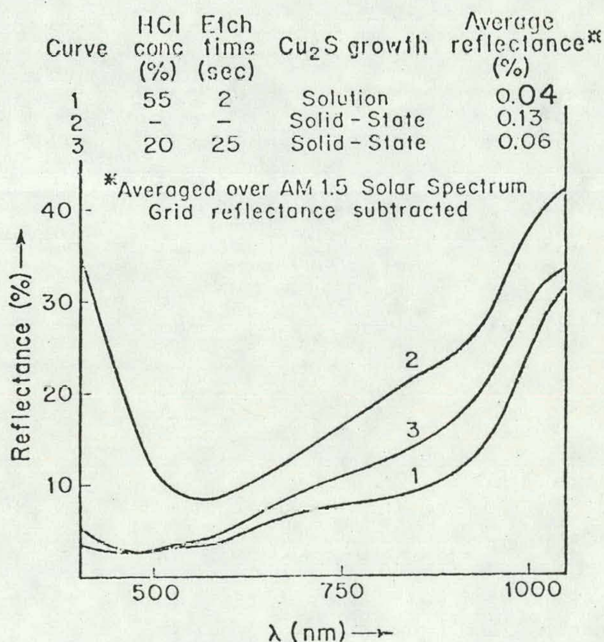

Figure 4

Reflectance spectra of gridded cells with various Cu_2S layer morphologies