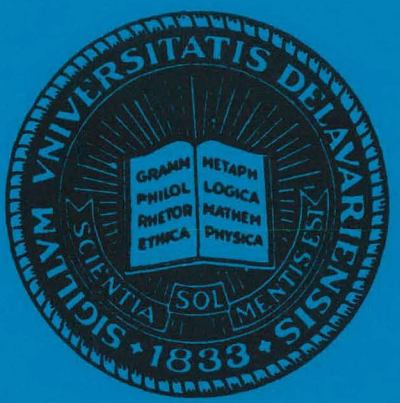
CADMIUM SULFIDE - COPPER SULFIDE HETEROJUNCTION CELL RESEARCH

Quarterly Progress Report

September 1, 1979 - November 30, 1979

XS-9-8309-1

May 1980



Institute of Energy Conversion
University of Delaware
Newark, Delaware 19711

Supported by the Solar Energy Research Institute, Report No. XS-9-8309-1-01

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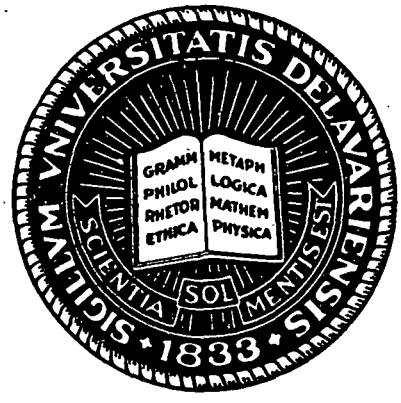

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1. ABSTRACT

Development of the CdS/Cu_2S cell has focused on the planar junction design with an enhanced open circuit voltage. Various techniques have been tried in an attempt to improve the short circuit current. The maximum achieved is $\sim$ 22 mA/cm^2 compared to $\sim$ 25 mA/cm^2 for the traditional solution reaction cell. The highest efficiency achieved to data at open circuit voltages above 0.54 V is 8.26%. The conditions have been established for (CdZn)S deposition and composition to give open circuit voltages of 0.62 V. The influence of texturing on reflectivity has been established and some progress made in reducing the excessive intrusions previously noted in this material. The best efficiency achieved during the quarter in actual sunlight testing was 8.04% at an open circuit voltage of 0.59 V. A paper analyzing the relation between Cu_2S stoichiometry and optical and electronic properties is being prepared for the Photovoltaic Specialists Conference. Further measurements on capacitance and photocapacitance are reported. Trial encapsulations using Electron Beam deposited glass and the results of attempts to deposit defect free coatings are described.

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2.1 LIST OF ILLUSTRATIONS

3. INTRODUCTION

The goal of the CdS/Cu_2S development efforts is to improve the short circuit current of planar junction, high voltage cells to the levels achieved with the conventional solution reaction-textured cell. A number of techniques have been attempted during this quarter but as yet parity has not been achieved. In general the currents in cells produced by either the solid state reaction alone or the solid state reaction in combination with a short solution reaction, are about 10% below the levels achievable by solution reaction only. Utilizing the short solution reaction following a standard solid state Cu_2S formation an efficiency of 8.26% has been achieved at an open circuit voltage of 0.54 V and a short circuit current at 100 mW/cm^2 of just over 21 mA/cm^2. Direct evidence for the effects of the solution reaction have been obtained using electron beam induced current imaging. The EBIC images show that the solid state reaction leaves regions of low response at the CdS grain boundaries, these are converted to regions of enhanced response by the solution reaction.

The zinc content and deposition conditions necessary to achieve 0.62 V open circuit voltage with (CdZn)S have been established. A study of the rate of reaction of this material in the dilute HCl texturing solution has shown that a reaction time of 10 seconds is sufficient to reduce the reflectivity to the minimum achievable. Producing the Cu_2S layer by solid state reaction has been shown to eliminate the grosser intrusion features and as a result some improvement in open circuit voltage stability has been shown. Macroscopic defects such as cracking in the mixed sulfide seem to be more

prevalent than in CdS and experiments have been designed to determine whether an expansion matching substrate will help reduce these flaws.

Fully automated data acquisition and analysis is being used to provide performance feedback to the cell development efforts. All current voltage curves of over 55% fill factor are fitted to a diode equation and the lumped series and shunt resistance computed. For efficient storage and retrieval of test data the parameters of the diode fit are stored on magnetic tape. An interdigitated grid has been designed and masks obtained to allow unequivocal measurements of the Cu_2S sheet resistance. A review of all available experimental data on the influence of Cu_2S stoichiometry on absorption and other parameters has been carried out. The results are being prepared for presentation at the next Photovoltaic Specialists Meeting. Further studies have been made of capacitance of various cells and the influence of heat treatment.

A number of cells have been coated with glass using electron beam deposition techniques and their behavior upon exposure to air monitored for up to two months. An initial rapid drop in efficiency is followed by a very slow decline. Microscopy has shown a number of defects in these glass layers and various techniques are being attempted to produce more defect free material.

4.1 Task 1 Development of CdS/Cu_2S Solar Cells

At the end of the previous contract it had been established that the front surface of the planar junction cell could be lightly textured without degrading the achievable open circuit voltage.[1] The highest efficiency cell of this type with the Cu_2S made by a solid state reaction was 7.81% under ELH simulation. Work has continued on the lightly etched cell with various approaches being tried to improve the current while maintaining the open circuit voltage and fill factor.

4.1.1 Phase 1 Improved Light Trapping in Cu_2S

The extent of light trapping with Cu_2S depends on the AR coating, the front surface texturing and substrate reflectivity. Texturing using 25% HCl at 60°C appears to produce a close to optimum front surface structure and good anti-reflection has been achieved with a two layer coating of TiO_x and SiO_2. The proccdure for depositing these films is as follows:

TiO_x. This is deposited by DC Magnetron sputtering from an 8" Ti target. The background pressure is 2.0 mTorr of 6% oxygen in Argon and the power consumption is 840 Watts. Under these conditions a film of 570 Å thickness and refractive idea of 2.35 is deposited in ∿ 5 minutes.

SiO_2. This is deposited by RF Magnetron sputtering from an 8" SiO_2 target in Argon at 2.0 mTorr. The RF power in 700 watts. Films of 980 Å thickness with a refractive index of 1.47 grown in 2¼ minutes.

The two layers are deposited sequentially without breaking vacuum.

The amount of light that is available for trapping on the second pass through the Cu_2S is controlled by the reflectivity of the substrate. Previous work had shown that a thin layer of zinc provided good adhesion and ohmic contact to the CdS and after heat treatment inter-diffusion with the copper gives an α-brass resulting in high reflectivity above ∿ 500 nm.[2] The reflectivity of copper in this region is higher than brass and silver shows almost 100% reflectivity. Two modified substrate configurations were therefore explored namely an ITO layer on copper and silver plated copper.

Figure 1 shows that the silver plated copper resulted in reduced reflectivity immediately after CdS deposition presumably because of silver sulfide formation during the initial stages of CdS deposition. Experiments with ITO resulted in some increase in J_L but a substantial reduction in yield of usable substitutes was noted. The major problem encountered was shorting which would indicate that there were pinholes and defects in the CdS films. Table I summarizes the ITO experiments. Standard substrate practice has therefore been maintained with an 8 second zinc plating time yielding a Zn thickness of ∿ 0.2 μm.

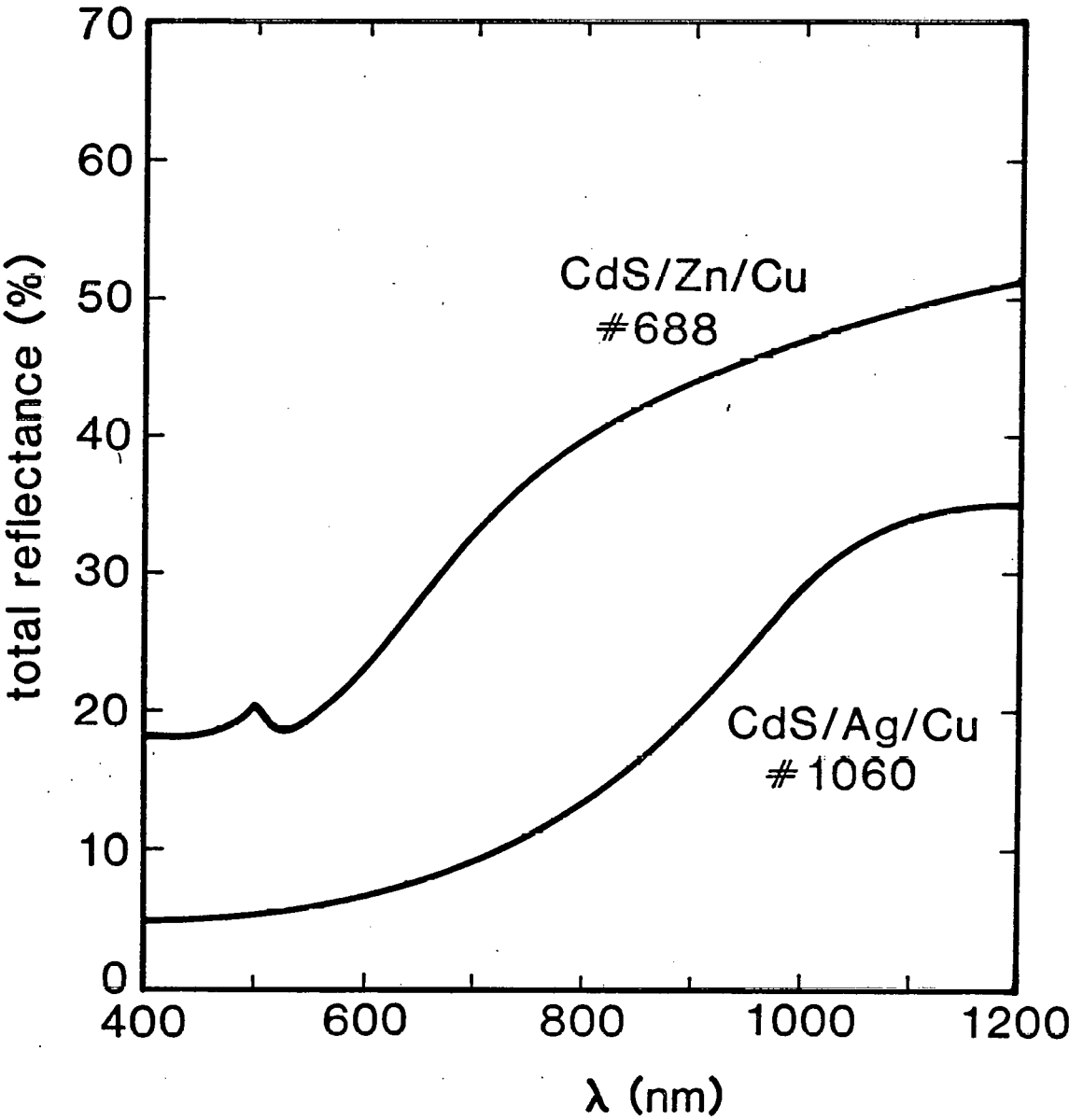


Figure 1 Total reflectivity from CdS substrates deposited on zinc or silver-plated copper.

Fig 1

Table 1

Yield and current generating capacity of CdS/Cu_2S cells deposited on standard zinc plated copper and ITO coated copper.

Zinc Plated Copper

Piece Number*	Maximum J_L ($\sim$ 100 mW/cm^2)	Comments
21044.11	24.2 mA/cm^2	Best of 4 cells
21040.11	22.2 mA/cm^2	Best of 4 cells
21041.11	21.9 mA/cm^2	Best of 4 cells
21042.11	21.8 mA/cm^2	Best of 4 cells

ITO Coated Copper

21046.11	21.7	3 cells shorted

* Each piece should produce 4 cells

4.1.2 Phase 2 Maximize J_{sc} by Cu_2S Control

The solid state reaction to produce Cu_2S on textured CdS has failed to result in currents which equal those achieved with the solution reaction. Table 2 shows the maximum currents achieved with the two processes during the reporting period and a direct comparison of cells produced on a single substrate is given in Table 3. It is seen that a difference of 10-12% in J_L exists between the two processes.

Table 2

Maximum Light Generated Currents at 100 mW/cm^2
September 1 - November 30, 1979

Cell #	J_L (mA/cm^2)
Solid State Process	
20468.121	22.2
20469.222	21.8
21002.213	21.8
21044.123	21.4
Solution Process	
21054.112	24.9
21057.121	24.7
21062.112	24.5
21044.112	24.2

Table 3

Direct comparison of solid state & solution process cells on substrate #20948. Light generated current at 100 mW/cm^2 without an anti-reflective coating.

Cell #	J_L (mA/cm^2)
Solid State Process	
221	18.9
222	17.9
Solution Process	
114	20.9
113	20.1
211	20.1

4.1.3 Phase 3 Optimize V_{oc}, FF for J_{sc} > 26 mA/cm^2

A procedure has been developed which promises to result in enhanced currents while maintaining the higher voltages of the solid state Cu_2S process. The technique is to follow the solid state reaction with a short reaction in the cuprous chloride solution. Preliminary EBIC imaging, Figure 2, shows that the initial Cu_2S has regions of very low response at the CdS grain boundaries. Subsequent solution reaction results in enhanced EBIC response in the boundary regions.

The best cells made during this reporting period by the single and two stage process respectively have achieved efficiencies of 8.01 and 8.26%. Complete production and performance details are given in Table 4. The slightly lower voltages for the solid state reaction cell giving the highest efficiency probably reflects the rather low resistivity of that particular CdS substrate.

Table 4

Performance and production data for CdS/Cu_2S cells produced by solid state reaction with CuCl only or with an additional reaction in a CuCl solution

Cells 20968.12X

Solid state reaction only

CdS — Resistivity 0.9 Ω-cm. Thickness 30.8 μm. Source temperature 1040°C. Substrate temperature 240°C. Etched for 25 seconds in 20% HCl at 60°C.

Cu_2S — Thickness 1611 Å

Heat treatment to optimum performance for cell 20968.121

16 hours at 170°C in CO prior to gridding
84 hours at 150°C in H_2 prior to double layer AR
32 hours at 130°C in vacuo
94 hours at 130°C in H_2

ELH Simulation at 96 mW/cm^2

Cell #	V_{oc} (V)	J_{sc} (mA/cm^2)	FF (%)	η (%)	J_L (at 100 mW/cm^2)
121	0.544	19.65	72.0	8.01	20.54
122	0.515	16.95	62.3	6.22	19.77
123	0.548	17.90	68.6	7.01	18.80
124	0.526	18.23	62.0	6.20	19.41

Cells 21007.22X

Solid state and solution reaction

CdS — Resistivity 2.9 Ω-cm. Thickness 21.8 μm. Source temperature 980°C. Substrate temperature 210°C. Etched for 20 seconds in 20% HCl at 60°C.

Cu_2S — Solid state thickness 1519 Å.
Solution reaction 10 seconds.

Heat treatment to optimum performance for cell 21007.221

5 hours at 170°C in CO prior to gridding.
121 hours at 150°C in H_2 prior to double layer AR
16 hours at 150°C in H_2

ELH Simulation at 87.5 mW/cm^2

Cell #	V_{oc} (V)	J_{sc} (mA/cm^2)	FF %	η (%)	J_L (at 100 mW/cm^2)
221	0.542	18.45	72.3	8.26	21.14
222	0.552	17.15	71.9	7.78	19.68
223	0.545	17.45	72.2	7.85	20.00
224	0.546	17.03	72.2	7.67	19.52

Solid State Reaction

Solid State + Solution Reaction

Figure 2 Electron Beam Induced Current Images from Solid State Reaction only and with solution reaction x 2500.

4.2 Task 2 (CdZn)S Material and Cell Development

4.2.1 Phase 1 Develop Non-Intrusive Cu_2S Morphology

Several samples were prepared to reveal the morphology of Cu_2S formed on (CdZn)S by the solution process (wet), and by the solid state reaction process (dry). The initial results for the wet process indicate that the morphological features of the Cu_2S formed on (CdZn)S were qualitatively different than observed on good quality grade CdS. In particular a predominance of spike intrusions which extend 4-8 μm into the (CdZn)S, and the persistence of intrusions formed around material "spits" deposited during film growth are evident. Additionally, localized regions in which there exist a host of sub-micron, semi-spherical intrusions are observed. Figure 3 shows the SEM of the top surface of a typical (CdZn)S film with its grain boundaries revealed. The revealing of the grain boundaries is accomplished by forming Cu_2S (by wet process) on the surface of the (CdZn)S, then stripping the Cu_2S with KCN (3). The picture reveals the existence of a bimodal distribution of grain sizes. On the one hand, there are regions which exhibit grain sizes in the 2-4 μm range, while on the other there are regions which are dominated by sub-micron grain sizes. It appears that it is these latter sub-micron grain size regions which result in the sub-micron size semi-spherical Cu_2S intrusion morphology. In general the grain structure of CdS film does not exhibit these small grain regions, nor the semi-spherical intrusions. The expected consequences of these small grained regions on (CdZn)S/Cu_2S device characteristics include the reduction in open circuit voltage owing to the increased area of the junction, and the reduction in current collection efficiency because of grain boundary losses.

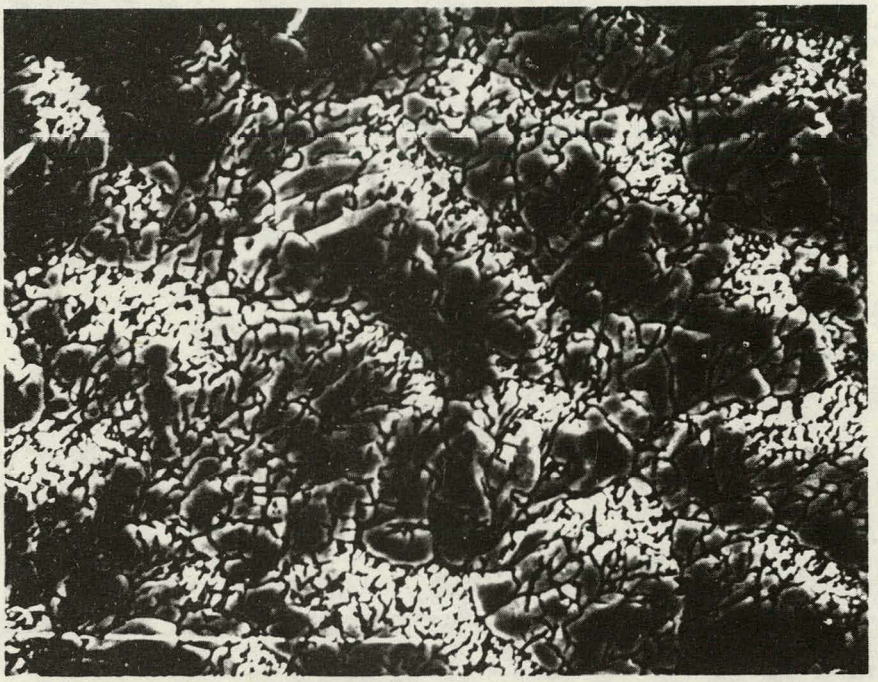


Figure 3 Scanning Electron Micrograph of (CdZn)S Substrate #10304 after removal of a Cu_2S layer. x 2000

The initial results on the morphology of Cu_2S formed by the dry process indicate that the wall-like intrusions still persist, but that the spike and spit intrusions are absent. Despite the reductions in the variety and penetration depth of Cu_2S intrusions, a decay in V_{OC} with time is observed. There is additional evidence of microscopic cracks in the (CdZn)S films, which appear to occur either as the result of handling during processing, or as a consequence of mechanical stress present owing to the mismatch in thermal expansion between the (CdZn)S and the copper substrate.

4.2.2 Phase 2 Material Fabrication

It was necessary to establish the appropriate deposition conditions to achieve the V_{OC} value required (620 mV) for the present cell design. To minimize the number of variables affecting film composition, structure and electrical properties, it was decided to determine and then keep constant, the set of source bottle parameters which would ensure an average film growth rate between 1.6 and 2.0 μm/min. and a zinc concentration between 12 and 15%. These conditions were achieved with the concentric source bottle temperature held at 1060°C; the total orifice area of the ZnS chamber was 0.2 cm^2, the CdS chamber orifice was 0.014 cm^2, and the exit orifice was 0.32 cm^2. With the source bottle conditions set, the substrate temperature remained as the variable used to affect average grain size, composition and electrical conductivity.

Table 4 shows the V_{OC} data for two sets of cells prepared from the same (CdZn)S substrate. The 21 μm thick (CdZn)S substrate has a zinc concentration of 12% and resistivity 3.7 ohm-cm. Prior to Cu_2S formation

the (CdZn)S substrate was textured in 25% HCl at 60°C for 20 and 25 seconds for the dry and wet formed Cu_2S, respectively. The cells had between 50 to 70 hours of heat treatment at 170°C in an hydrogen environment and a final hydrogen heat treatment at 200°C for 16 hours. The difference in observed open circuit voltage would require the difference in junction area to be a factor of seven between the wet and dry formed Cu_2S.

Figure 4 shows the plot of thickness removed as a function of the (CdZn)S texturing time in the 25% HCl etch held at 60°C. The (CdZn)S film

Table 4

Open Circuit Voltage Achieved on (CdZn)S Substrate #10298 by Solution and Solid State Cu_2S Formation

	Cu_2S		
Cell #	Formation	Thickness (Å)	V_{oc}(mV)
111	Wet	3178	560
113	Wet	3178	565
114	Wet	3178	563
221	Dry	1424	621
222	Dry	1424	619
223	Dry	1424	614

(10295) was grown on a substrate held at 225°C. The thickness removed is the equivalent planar thickness assuming 100% dense (CdZn)S. The average texturing rate is 0.021 μm/sec which is about half the rate observed for CdS films. For comparison a data point for the old 55% HCl for two seconds texturing etch is presented. The reduced HCl concentration gives better repreducibility and reduces the amount of material removed to give the necessary reflection reduction. The effects of this texture as a function of texturing time will be presented in the following Section.

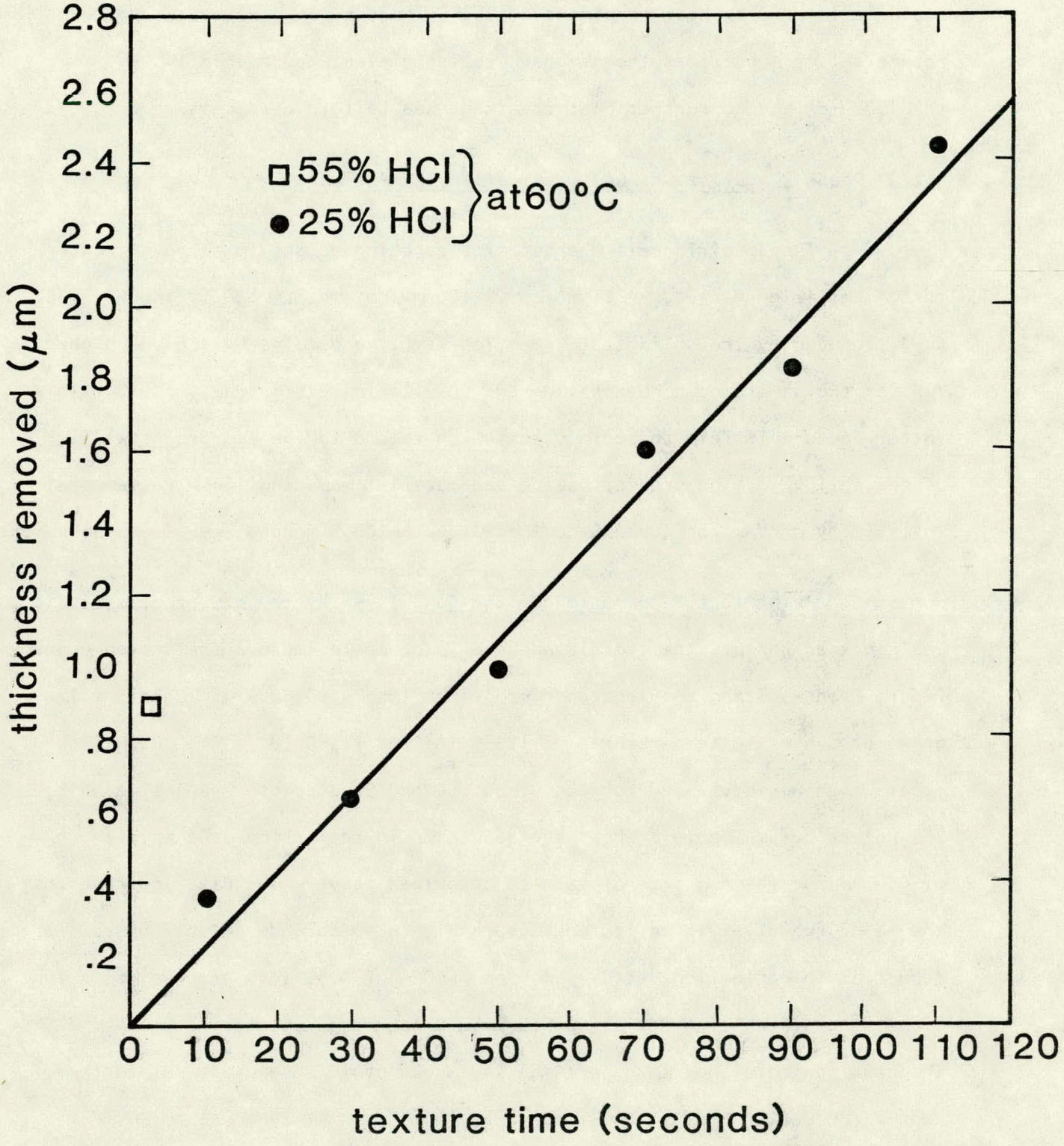


Figure 4 Thickness of (CdZn)S removed as a function of etching time in HCl.

As was previously reported[2] the as-grown (CdZn)S resistivity could be lowered by heat treatment at 250°C in hydrogen. However, for the recent set of substrates the as-grown resistivities were typically less than 20 Ω-cm and no further heat treatment was felt to be necessary.

4.2.3 Phase 3 Device Design, Fabrication and Analysis

The specific cell characteristics being sought to achieve greater than 9% efficiency are $J_L \simeq 21$ mA/cm^2 @ 100 mW/cm^2, $V_{oc} = 620$ mV and FF $\geq$ 72%. Cu_2S produced by the solid state reaction is being used as this gives higher V_{oc} for the same zinc concentration and results in less intrusive Cu_2S. This latter feature is felt to be important with regard to the temporal stability of the cell V_{oc}. The present device and material modeling link the temporal instability of V_{oc} for (CdZn)S devices with the Cu_2S morphology (i.e. intrusions).[1]

Prior to the formation of the Cu_2S layer by the dry process, it is desirable to texture the (CdZn)S surface in order to improve the photon economy. Figure 5 shows Scanning Electron Micrographs (mag x 10,000) of (CdZn)S films grown at substrate temperatures of 195°C (A) and 225°C (B). The (CdZn)S surfaces which were textured for 0, 10, 30, 50 and 90 seconds, respectively in 25% HCl at 60°C. Table 5 shows the reduction in reflection at a wavelength of 0.4 μm for the two sets of samples described above. The data indicate that the major reduction in reflection occurs within 10 seconds. Table 6 shows the reduction in reflection at 0.4 μm from 1600 Å of Cu_2S (dry process) as a function of texturing time for a (CdZn)S film prepared on substrates held at 225°C. The data indicate that texture times in excess of 10 seconds do not further reduce reflection from the Cu_2S surface.

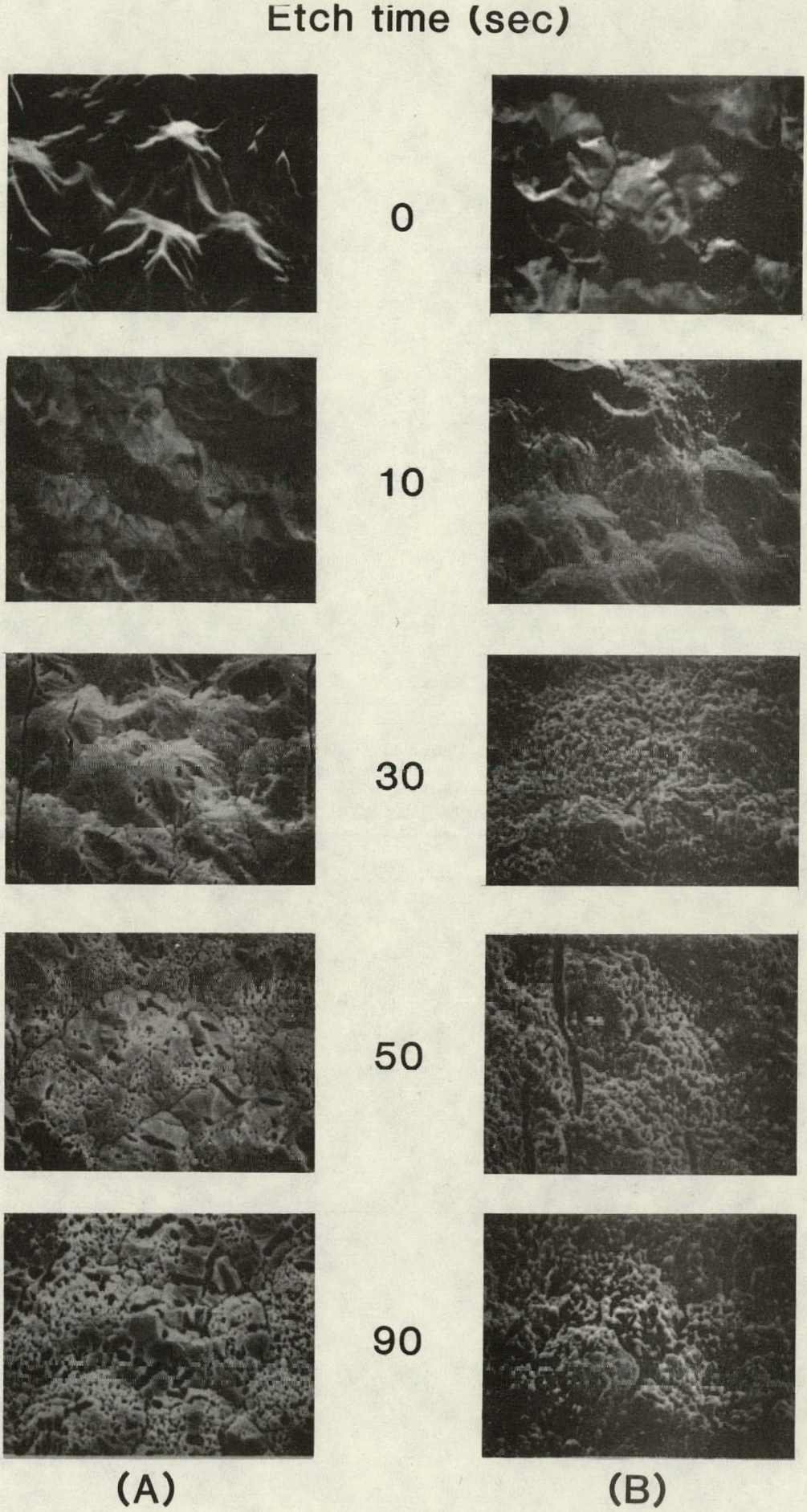


Figure 5 Scanning Electron Micrographs of (CdZn)S substrates deposited at 195°C and 225°C as a function of the indicated etching times (seconds).

Table 5

Influence of Etching Time on (CdZn)S Reflectivity at 0.4 μm

Sample #	T_{ss} (°C)	Texture Time (seconds)	R @ 0.4 μm
1-292-a	195	0	.222
-b	"	10	.147
-c	"	30	.113
-d	"	50	.099
-e	"	90	.079
1-296-a	225	0	.217
-b	"	10	.147
-c	"	30	.103
-d	"	50	.071
-e	"	90	.047

Table 6

Influence of Etching Time of (CdZn)S on Reflectivity at 0.4 μm From a Cu_2S Surface Layer

Sample #	T_{ss} (°C)	Texture Time	R @ 0.4 μm
1-298-a	225	0	.305
-b	"	10	.120
-c	"	20	.120
1-299-a	225	0	.295
-b	"	15	.133
-c	"	30	.134

Having selected a suitable set of (CdZn)S deposition conditions, and focused in on an appropriate texture time, a set of cells was prepared. As in Task I a substrate evaluation procedure was employed in order to select proper (CdZn)S film. The selection criteria were that J_L @ 100 mW/cm^2 be greater than 18 mA/cm^2 (no A-R) and $V_{OC} \geq 560$ mV for (CdZn)S/Cu_2S junctions formed by the wet process.

Table 7 shows the cell data for four sets of cells (no A-R) prepared on the same (CdZn)S substrate (10298). The 21.4 μm thick (CdZn)S film had a zinc composition of 12% and as-grown resistivity of 3.7 ohm-cm. The purpose of these sets was to compare wet versus dry on the same (CdZn)S and to examine the J_L and V_{OC} dependence on texturing time within the time range dictated by the reflectivity data. The V_{OC} and J_L data for the untextured (CdZn)S with dry Cu_2S indicate a fair amount of scatter in comparison with the other sets. It is apparent that, in addition to providing a light trapping junction, the texture etch cleans the (CdZn)S providing a more uniform surface onto which the Cu_2S is formed, nevertheless the data for dry Cu_2S indicates that there is no significant loss in V_{OC} as a consequence of the texturing. The comparison between solution and solid state reaction cells shows an open circuit voltage gain of 50-60 mV for the latter technique. If this V_{OC} difference is due to a junction area effect, then the junction area for (CdZn)S Cu_2S (wet) must be seven times greater than for (CdZn)S/Cu_2S (dry).

Inspection of the light generated current values for the different dry Cu_2S cell sets shows that there is an improvement in current as a consequence of texturing. In fact the improvement in light generated current given as

Table 7

Cell Performance for Solution and Solid State Reaction Cells on (CdZn)S Substrate #10298

Cell #	Texture Time (sec)	Cu_2S Thickness (nm)	Max. J_L@ 100 mW/cm^2 (mA/cm^2)	Max. V_{oc}@ 25 mA/cm^2 (mV)	η (%)
			Solution Reaction		
113	25	317.8	17.9	.588	6.9
114	"	"	18.2	.586	6.7
111	"	"	18.1	.583	6.7
			Solid State Reaction		
121	0	168.5	12.3	.644	5.2
122	"	"	11.7	.606	4.1
123	"	"	9.6	.612	3.5
211	"	151.1	14.5	.633	6.0
213	"	"	15.1	.634	5.9
212	"	"	13.2	.638	5.7
221	20	142.4	15.6	.642	6.2
224	"	"	15.5	.633	6.0
222	"	"	15.1	.641	5.8
223	"	"	15.5	.637	5.6

$$\frac{J_L \text{ (textured)} - J_L \text{ (untextured)}}{J_L \text{ (untextured)}} \quad \frac{15.5 - 12.3}{12.3} \simeq 26\%$$

is in approximate agreement with the increase in absorbed light due to the reduction of reflection, which is

$$\frac{[1 - R \text{ (textured)}] - [1 - R \text{ (untextured)}]}{[1 - R \text{ (untextured)}]} = \frac{.87 - .70}{.70} \simeq 24\%$$

Despite the improvement in V_{oc} and apparent reduction in Cu_2S intrusion density, these devices still exhibit a V_{oc} which decay with time (e.g. $\Delta V_{oc}/\Delta t \simeq 2.5$ mV/min @ 28°C). It is therefore concluded that while Cu_2S formed by the dry process does influence the Cu_2S morphology, the defects responsible for the V_{oc} temporal instability are not being eliminated. It has been observed that the (CdZn)S films are more brittle than CdS films and it is suggested that cracks in the film are being caused by handling. As a consequence of the thermal expansion mismatch between (CdZn)S and copper the substrate assumes a tubular shape after deposition. During subsequent handling accompanying device fabrication, the substrate receives quite severe handling. Possible substrate alternatives with more suitable thermal expansion matches will be sought.

During this past quarter a (CdZn)S/Cu_2S cells with Cu_2S formed by the wet process was tested under outdoor illumination. The 22 μm thick (CdZn)S film (#10296) with a resistivity of 8 ohm-cm was textured in 25% HCl at 60°C for 40 seconds prior to the application of Cu_2S. Figure 6 shows the I-V curve for the outdoor test. The open circuit voltage was 586 mV, the fill factor 65.7% and current under 88.5 mW/cm^2 outdoor insolation was 18.5 mA/cm^2 for a conversion efficiency of 8.04%.

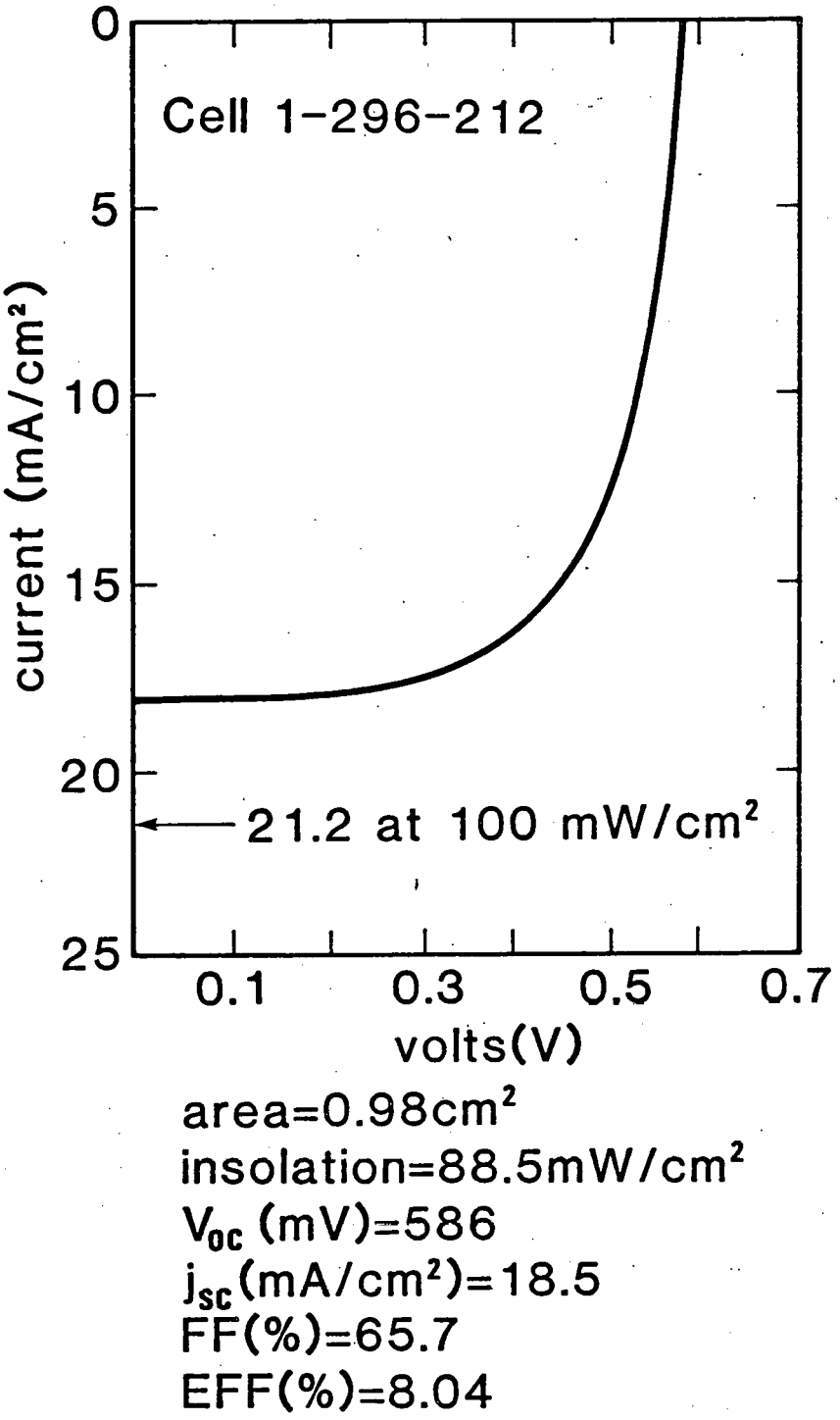


Figure 6 Current-voltage curve for (CdZn)S/Cu_2S cell # 10296.212 under natural sunlight.

4.3 Task 3 Electro-Optic Analysis Modeling

4.3.1 Phase 1 Feedback Analysis

Rapid feedback to the solar cell development efforts is achieved using digital data acquisition and analysis for the basic current-voltage testing. Daily updates of cell performance are maintained and provided to the cell production group. All current-voltage curves of over 55% fill factor are fitted to a modified diode equation and the lumped series and shunt resistance contributions calculated. The data is then stored on a central file using the parameters from this diode fitting procedure. During the quarter the software capability was extended to handle the interdigitated grid devices.

4.3.2 Phase 2 Quantify Effects of 2D Current Flow

Experimental investigation of the influence of two dimensional current flow in the Cu_2S layer will be carried out using an interdigitated grid device. This cell will have interleaved parallel grid wires in two sets connected to a current collection busbar at each end of the cell. Using this device it will be possible to measure cell behavior utilizing each grid separately and in combination thus giving cell performance at 2 grid spacings. In addition it will be possible to measure the current-voltage behavior of the Cu_2S alone by measuring the current flow from one grid to the other. Appropriate voltage biasing will be used to present parallel current flow through the heterojunction.

4.3.3 Phase 3 Theoretical Modeling and Analysis-Parameter Interactions

A review of the available data on the influence of Cu_2S stoichiometry on carrier behavior and optical absorption is being carried out. A paper describing the results is being prepared for the 14th IEEE Photovoltaic Specialist Conference.

4.3.4 Phase 4 Influence Defect Levels in CdS and $J_L(V)$

A number of cells have been submitted to multiple heat treatments at various temperatures in order to form the junction, to adjust the stoichiometry of the Cu_xS, and to cause diffusion of Cu ions into the CdS. As a means of investigating these effects in more detail, experiments have been performed consisting of repeated measurements, at successive stages of heat treatment of photocapacitance and $J_L(V)$, along with the usual I-V curves. Here we will describe the photocapacitance measurements.

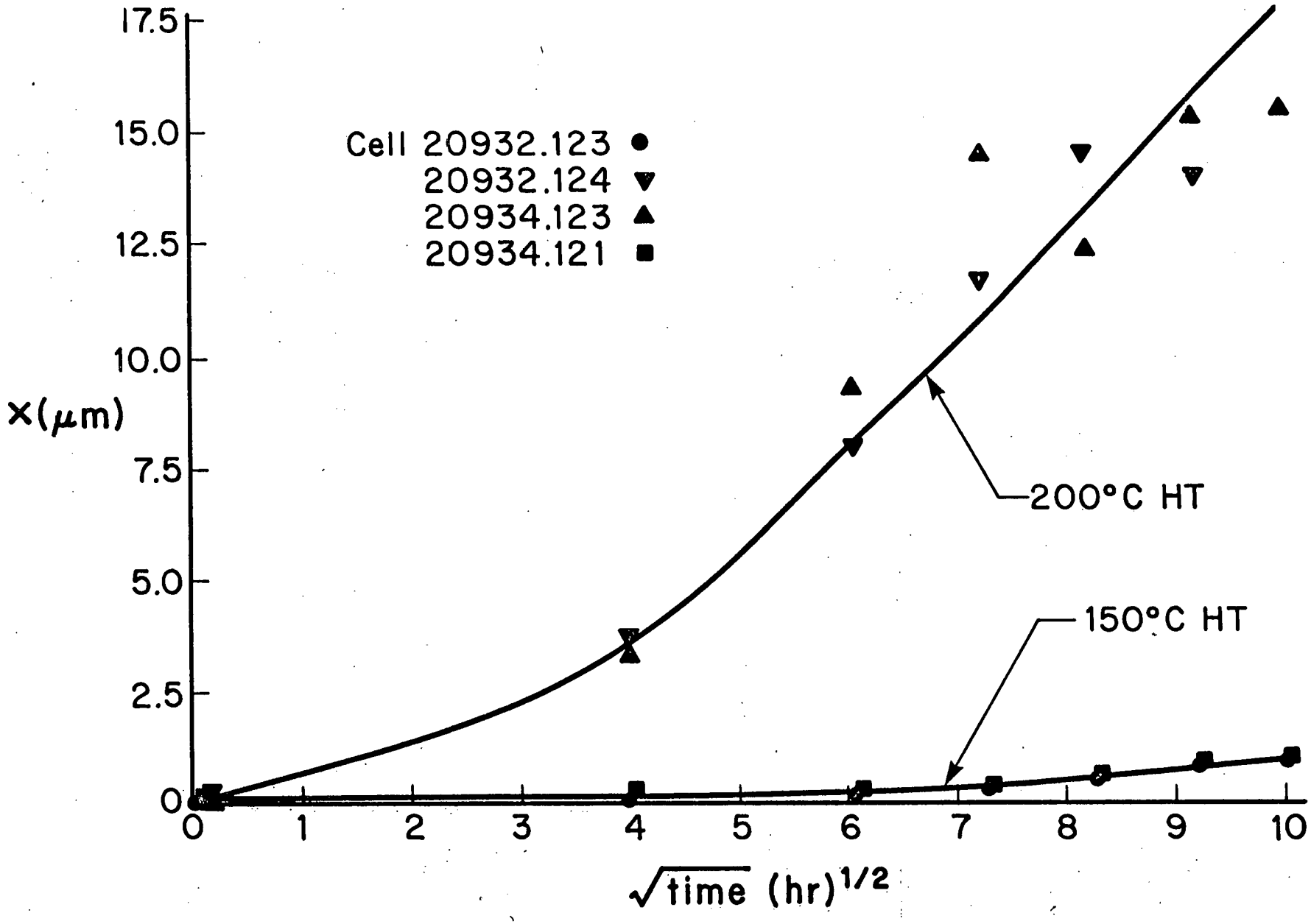
Two groups of cells (solution process) were followed through a series of heat treatments. In both cases, values of capacitance C in the dark and at AM1 were first measured before the cells experienced any heat treatment. They were subjected to 16-hour heat treatments in H_2. In the first group, the heat treatment temperature was 150°C, and C was measured as a function of DC bias V and white-light illumination intensity Φ after each of four heat treatments. In the second group, the heat treatment temperature was 200°C for two cells and 150°C for the other two, and C and cell current I was measured as a function of Φ after each of six heat treatments. Results are treated below under four headings:

1. Variation of $(C/A)_{dark}$ with heat treatment at two temperatures was measured in order to follow diffusion of Cu into the CdS. If one disregards the topography of the CdS-Cu_xS junction and assumes that it acts like a plane parallel capacitor, one can estimate the depths to which Cu ions diffuse into the CdS as plate separation

$$\chi = \frac{\varepsilon\varepsilon_o}{(C/A)_{dark}}$$

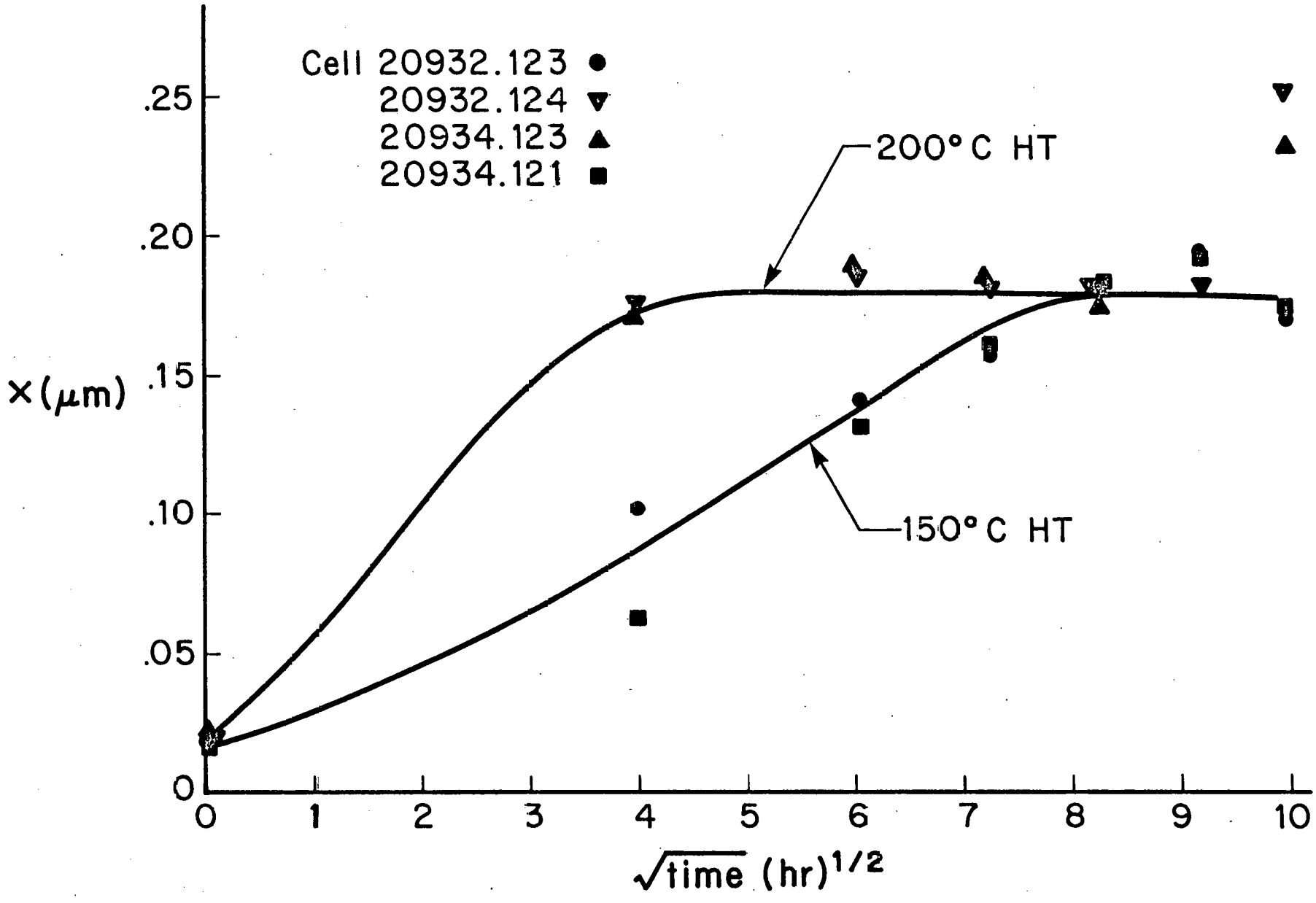
According to standard diffusion theory, χ should increase linearly with $t^{\frac{1}{2}}$, where t is the time of heat treatment. Figure 7 plots these variables for cells subjected to 150° C and 200° C heat treatments. The variation is obviously not linear and this is presumably the result of grain boundary effects. We can estimate the initial slope (near t = 0) to obtain diffusion coefficients of D 1 x 10^{-14} cm^2/sec of magnitude with those obtained by Sullivan [Ref: G. A. Sullivan, Phys. Rev. 184, 796 (1969)] in singel-crystal CdS. Further measurements of this type are to be done on planar cells to determine the influence of grain boundaries.

2. Variation of $(C/A)_{AM1}$ with heat treatment at two temperatures was measured to determine the effect of hole trapping and the consequent modulation of junction field by light. The results appear in Figure 8. In this plot, χ is more reasonably interpreted as depth of the conductive region produced by hole trapping behind the depletion region. The observation that χ approaches a limit of $\sim$ .18 μm after the third or fourth heat treatment at 150°C indicates that, in the region of strong optical absorption and consequent hole trapping in CdS, hole trap concentration becomes saturated after $\sim$ 65 hr. A single heat treatment at 200°C is enough to bring this concentration to its



Width of compensated region in the dark as it changes with time of HT in H_2

Figure 7 Width of compensated region as a function of heat treatment at 150 and 200°C.



Width of depletion layer at AM1
as it changes with time of HT in H_2

Figure 8. Width of depletion layer at AM1 as a function of heat treatment at 150 and 200°C.

limit. It is significant that the limiting value of $(C/A)_{AM1}$ (and therefore of χ) is apparently the same for the two temperatures, even though junction electric field ε is not, as shown by the $J_L(V)$ measurements.

3. Effective donor density N_D^* was estimated from slopes of $(A/C)^2$ plots against DC bias V at different Φ and t, in order to determine whether one can see the effects of compensating Cu ions in this way. In the cells before heat treatment, C was nearly constant with V at all Φ, indicating very large N_D^*, as anticipated. Probably the most significant feature was the observation that N_D^* reaches its minimum of $\sim 2 \times 10^{16}$ cm^{-3} at moderate values of Φ, often around 10% AM1, rather than at AM1, where one would anitcipate hole trapping to be most effective in reducing N_D^*. The explanation presumably requires consideration of effects of increasing injected current at higher Φ.

4. Variation of the relation between C and collection efficiency η with heat treatment was investigated by plotting ε^{-1} versus η_c^{-1}. As explained in earlier reports, straight lines can be fitted to these plots and the respective intercepts interpreted as the inverses of S_1/μ_2 and η_Q. Because of the very slow variation of η_c with Φ between $\sim$.01 AM1 and 1.5 AM1 seen in the present experiment, the straight-line fit was very poor until the cells had received at least four heat treatments. Consequently, the results are mainly qualitative. The 150°C cells gave a fairly high S_1/μ_2 at first (rough estimate 4000 V/cm), while the value drops after three or four heat treatments to $\sim$1500 V/cm, at which value it remains. The 200°C cells, in contrast, start low in S_1/μ_2 (rough estimate 500 V/cm) and later rise, reaching values above $\sim$3000 V/cm after the sixth heat treatment, and not showing any tendency to approach a limit. After the sixth heat treatment, the 150°C and 200°C cells showed, respectively, $\eta_Q \sim .25$ and .5.

4.4 Task 4 Develop Integral Encapsulation

During this period the efforts were concentrated on the structural characterization of e-beam evaporated 9658 glass films.

Four cells (21014.111, 112, 113, 114) prepared by standard wet method and double layer AR coated were encapsulated by 5 μm glass. The deposition parameters for the glass film were:

Rate = 50 Å/second

Substrate temperature = room temperature

Three of these cells were then exposed to laboratory air, under no-load condition and their efficiency measured periodically. Figure 9 shows the average efficiency vs. exposure time data. As can be seen the glass deposition results in a 13.4% decrease in the efficiency. Over a period of 16 days the efficiency further drops 18.2% (from the initial encapsulated value) with most of the change occurring in the first eight days. Investigation of the cell parameters (Table 8) shows that the degradation is mainly the result of an initial sharp drop in J_{sc} followed by a very slow decline. This suggests that the glass layer has structural defects permitting the oxidation of the Cu_2S layer.

The fourth cell (21014.111) which was not part of the exposure test was examined by Scanning Electron Microscopy to determine the defects causing loss of hermeticity. The micrographs in Figure 10 shows that these are of two types:

- Cracks in the glass layer probably due to residual stresses (Figure 10a).
- Cauliflower type of overgrowth (Figure 10b) loosely bound to the matrix which may pop out causing the exposure of the

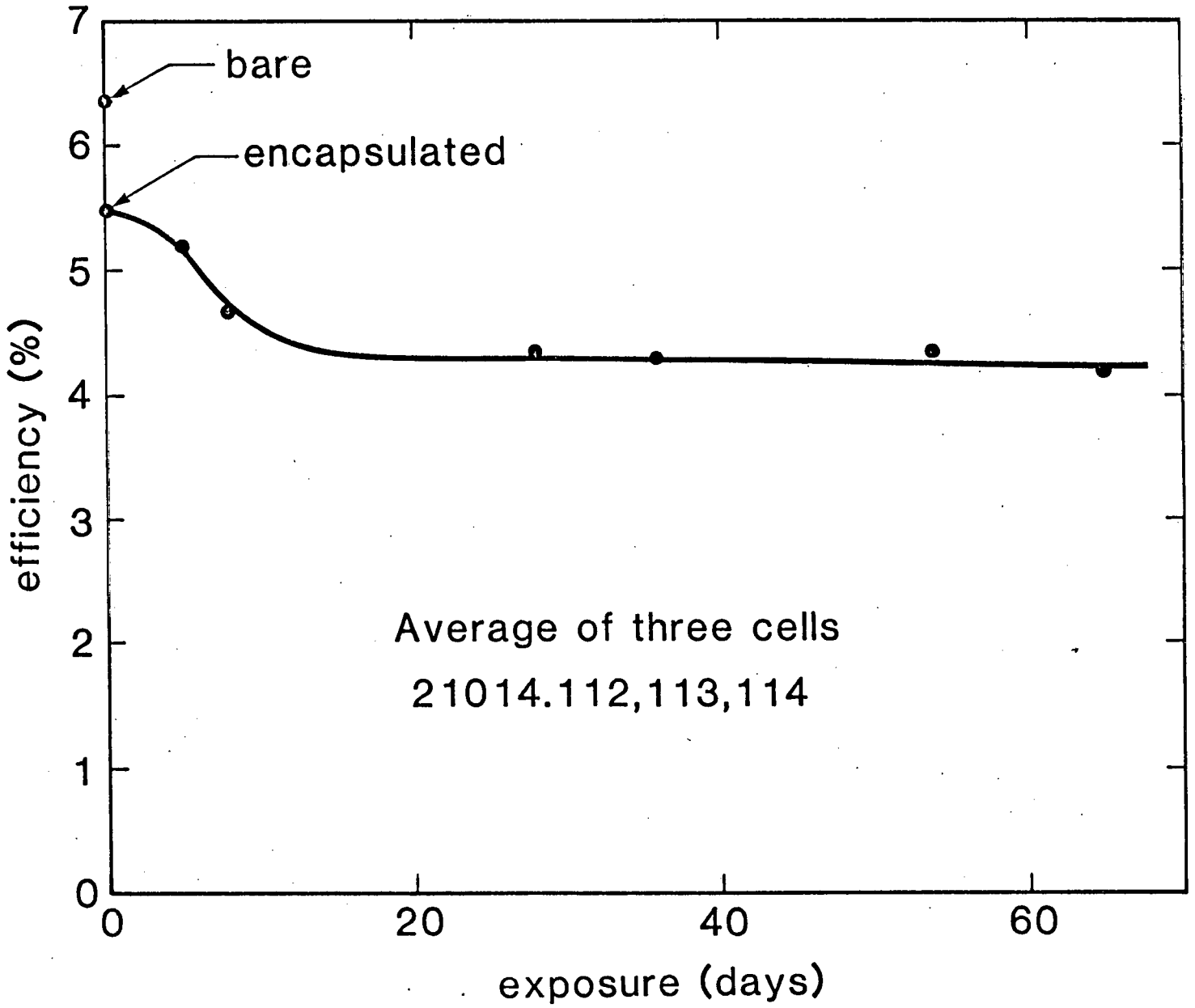
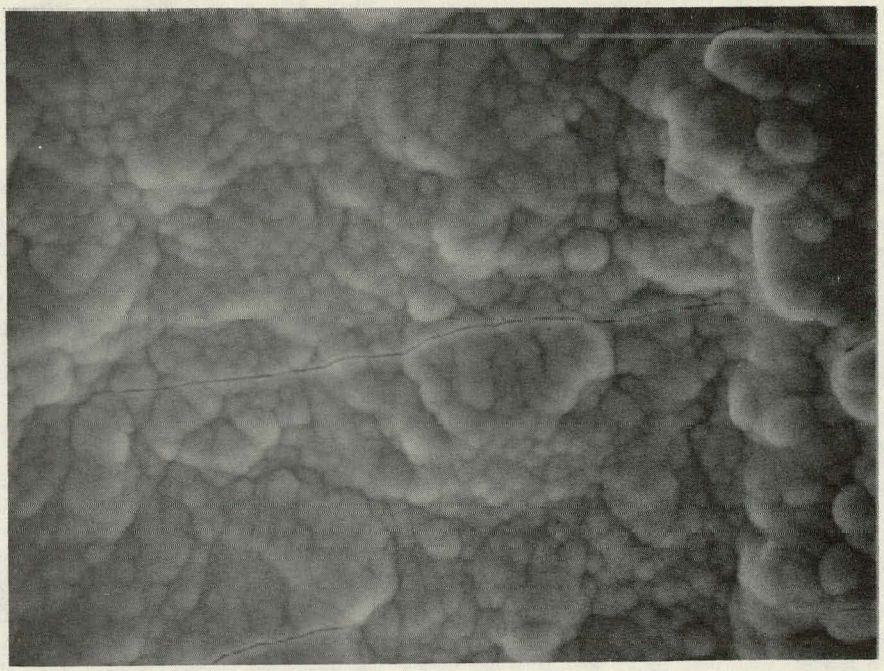
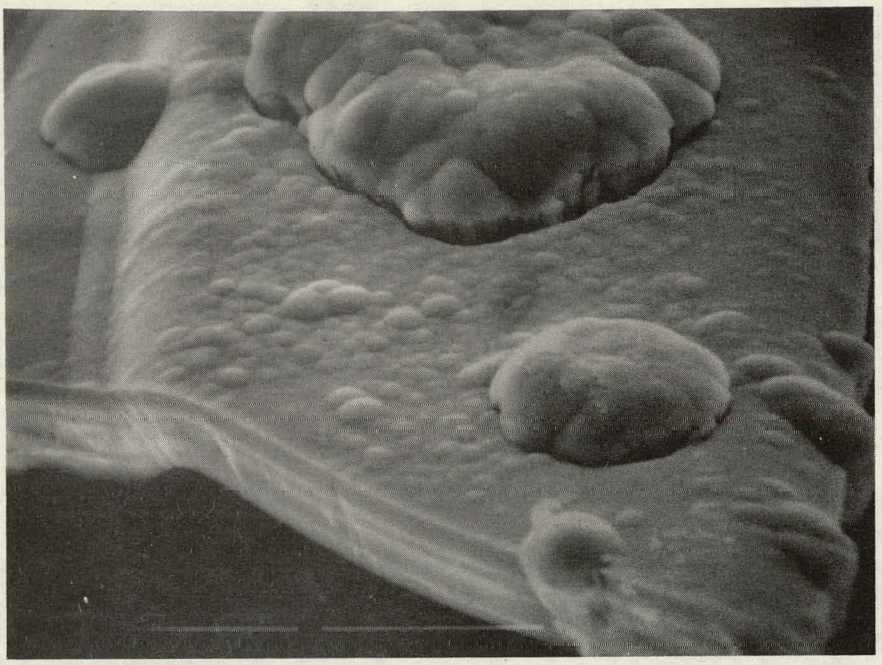


Figure 9 Effects of exposure on e-beam encapsulated CdS/Cu_2S cell.



(a) 0^{o} tilt



(b) 40^{o} tilt

Figure 10 Typical structural defects on the glass layer. Micron bar = 10 μm.

underlying Cu_2S layers.

This type of defect is believed to be the result of the extremely rough surface of the cell which promotes preferential nucleation and overgrowth.

It is well known that growth defects of the above type can be reduced by the appropriate choice of growth parameters. To determine the effect of the rate of deposition, glass layers were deposited onto the copper foil (used as substrate in Cu_2S/CdS cells) at a rate of 6.7 Å/sec. Micrographs of Figures 11(a) and 11(b) show these glass layers (1.2 μm thick) deposited respectively on the rough and smooth side of the electroformed copper foil. Nucleation and growth defects are still evident. However over an area of 1" x 1" stress cracking was not observed. Since 1.2 μm is too thick for elastic accommodation of the deposition stresses it is believed that by reducing the deposition rate stress cracking can be reduced. Further elimination on the growth defects can only be achieved by increasing the substrate temperature. To this end a substrate heater was installed into the deposition system.

During the next quarter experiments will be continued to determine the optimum glass deposition parameters using copper foil substrate. Experiments on actual cells will start after structurally satisfactory glass layers are obtained on copper substrates.

(a)

(b)

Figure 11 Structure of glass layers deposited on electro-formed copper foil. (a) rough side; (b) smooth side. Micron bar = 10 μm.

Table 8

Average Cell Parameters of Three Exposed Cells

Exposure (Days)	V_{oc} (V)	J_{sc} (mA/cm^2)	FF (%)	η (%)	Comment
0	.515	16.88	63.9	6.35	Before Encapsulation
0	.5161	15.86	58.8	5.50	After Encapsulation
5	.5166	15.11	58.4	5.21	
8	.5164	14.35	55.3	4.68	
28	.5171	13.88	53.4	4.37	
36	.5178	13.49	53.9	4.30	
54	.5168	13.30	59.0	4.36	
65	.5156	13.04	55.0	4.22	

5. References

1. IEC Final Report, XR-9-8063-1-FR, December 1979

2. IEC Progress Report, E(49-18) - 2538 PR 77/1 p. 26, July 1977.

3. B. Baron, A. W. Catalano and E. A. Fagen, 13th IEEE Photovoltaic Specialists Conference, Washington, 1978, p. 406.