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## Precursor Ion Damage and Single Event Gate Rupture in Thin Oxides

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35-word Abstract

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A clear difference between SEGR and ion damage is observed for thin thermal and nitrided oxides. Ion damage had no significant effect on SEGR thresholds. The data support a true single ion SEGR model.

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# Precursor Ion Damage and Single Event Gate Rupture in Thin Oxides

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## INTRODUCTION

Gate oxide electric fields are expected to increase to greater than 5 MV/cm as feature size approaches 0.1  $\mu\text{m}$  in advanced integrated circuit (IC) technologies. Work by Johnston, et al. [1] raised the concern that single event gate rupture (SEGR) may limit the scaling of advanced ICs for space applications. SEGR has also been observed in field programmable gate arrays [2], which rely on thin dielectrics for electrical programming at very high electric fields. At last year's conference, we presented data for SEGR in gate oxides ranging in thickness from 6 to 18 nm [3]. An inverse dependence was found for critical field to rupture as a function of ion linear energy transfer (LET), consistent with earlier work on SEGR for power MOSFETs with oxide thicknesses from 30 to 150 nm [4-6]. More importantly, we found that critical field to rupture increased with decreasing oxide thickness. This was correlated with the breakdown strength of the oxides measured through standard voltage ramp tests. This is consistent with work from other researchers, who demonstrated that breakdown strength increases in thin oxides due to reduced defect creation by hot carriers [7]. Our results showed that advanced technologies would be more SEGR resistant at a given electric field than previous models suggested.

Despite recent progress in this area, many questions remain to be resolved about the nature of SEGR in dielectrics and the role of ion damage on oxide reliability in space. It has been suggested that SEGR is not a true single ion effect, but is the result of many ion strikes [8]. This raises the possibility that the buildup of ion-induced damage may affect SEGR, possibly through the generation of precursor defects by the initial ion strike. Thus, the role of damage must be further investigated.

Many studies have shown that incorporating nitrogen near the oxide-silicon interface increases the resistance to charge trapping [9] and reliability [10] of thin oxides. This has been demonstrated in the absence of ion exposure through standard characterization and oxide reliability tests. If SEGR were strongly affected by pre-existing damage, we might expect nitrided

oxides to have improved resistance to SEGR over thermal oxides.

The focus of this effort is to further explore the mechanisms for SEGR in thin gate oxides. We examine the characteristics of heavy ion induced breakdown and compare them to ion induced damage in thin gate oxides. Further, we study the impact of precursor damage in oxides on SEGR threshold. Finally, we compare thermal and nitrided oxides to see if SEGR is improved by incorporating nitrogen in the oxide.

## TEST DEVICES AND APPROACH

Test devices used in this work were patterned polysilicon gate capacitors from a development process from Lucent Technologies. Oxides were grown via rapid thermal processing at 1000°C to a thickness of 7 nm with two different ambients: one set was grown in  $\text{O}_2$ , while the second set was grown in  $\text{N}_2\text{O}$ . The latter process results in a lightly nitrided oxide [9-11]. Each test chip contained an array of capacitor sizes. Devices were assembled into 24-pin ceramic dual-in-line packages. Results are reported here for capacitors with areas of 0.0004 and 0.0025  $\text{cm}^2$ .

Tests were conducted at the Brookhaven National Laboratories tandem van de Graaff accelerator using the following suite of ions: 1) 360 MeV Au, 2) 340 MeV I, and 3) 290 MeV Br. LETs were 80.6, 59.6, and 37.5 MeV- $\text{cm}^2/\text{mg}$ , respectively. In order to characterize breakdown, we measured capacitor gate leakage as a function of gate voltage using a hp4062 parametric analysis system. Typically, gate voltage was swept from 0 to 4 V (well below intrinsic breakdown for these devices) in 50 mV steps at a rate of 1.0 MV/cm/s. Current-voltage (IV) curves were measured before exposure and after multiple exposures to a flux of energetic heavy ions. Bias was held constant during each exposure and increased in steps between exposures until rupture was observed after an exposure. To characterize the effects of precursor damage, a second series of exposures was performed with capacitors held at a constant bias below the

SEGR threshold while fluence was increased in steps to more than  $10^8$  ions/cm $^2$ . IV curves were measured between each step.

## RESULTS

### Charge to Breakdown

A standard charge to breakdown measurement was performed on samples from each of the two gate oxide processes. The average voltage applied at the beginning of a stress of 100 mA/cm $^2$  was 7.8 V and 8.3 V for the thermal and nitrified oxides, respectively. The nitrified oxides in this study had a higher charge to breakdown than the thermal oxides as shown in Fig. 1, consistent with an improved reliability. Median charge to breakdown for the nitrified oxides was 16.8 coul/cm $^2$  compared to 12.5 coul/cm $^2$  for the thermal oxides.

### Characteristics of SEGR

A typical set of IV curves is shown in Fig. 2 for a thermal oxide exposed to a flux of 360 MeV Au ions as a function of bias. A constant fluence of  $10^6$  ions/cm $^2$  was used for each exposure under constant bias. As irradiation bias increased, a steady increase in low voltage leakage current was observed after each exposure. This indicates that some damage to the oxide is caused by ion flux. Gate rupture was characterized by a low resistance shunt resulting in a large increase in current at low voltage, as seen in the 3.7 V curve, and is clearly distinct from the prior IV curves.

This procedure was repeated for a minimum of three devices per oxide group with each ion species used in this study. Voltage to rupture was measured as a function of ion LET and type of oxide, as shown in

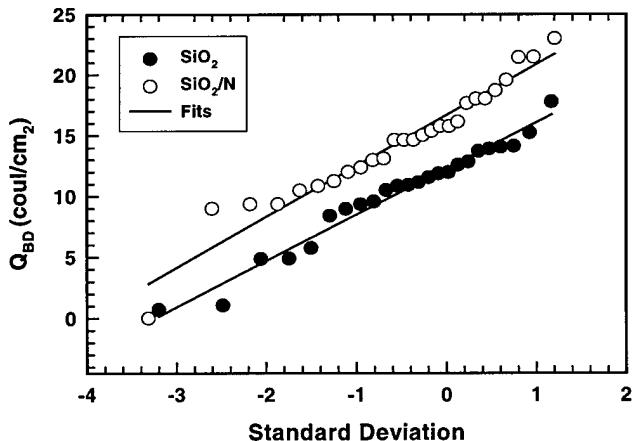


Fig. 1: Charge to breakdown for the nitrified and standard oxides used in this work.

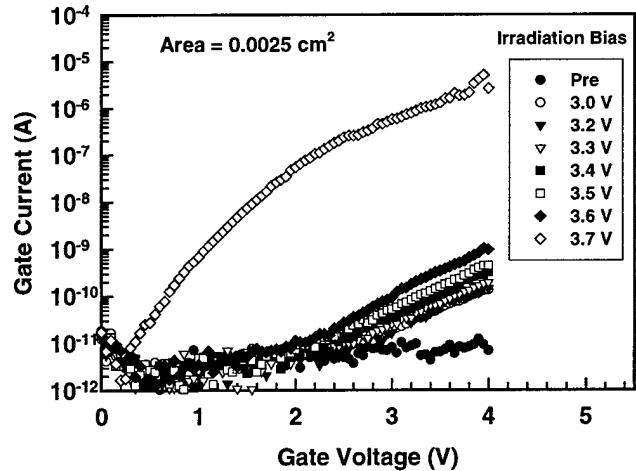


Fig. 2: IV curves for a 7-nm SiO<sub>2</sub> capacitor as a function of exposure to a fluence of 360 MeV Au ions. Bias during each exposure is indicated.

Fig. 3. Also plotted are data from our work last year with 6 to 18 nm gate oxides. Please note that, where no error bars are visible, the variation is less than the size of the symbol used in the plot. No significant difference was observed in critical voltage to rupture as a function of oxide treatment (O<sub>2</sub> vs. N<sub>2</sub>O). The 7-nm data are consistent with critical voltage to rupture observed in thin oxides in our previous work.

### Effects of Damage on SEGR

To test for the effects of ion damage on SEGR, devices were biased at a constant voltage below the critical voltage to rupture while fluence was increased in steps to  $10^8$  ion/cm $^2$  or greater. IV curves were measured between each increment in fluence. These stress tests were performed at gate biases of 2.5, 3.3,

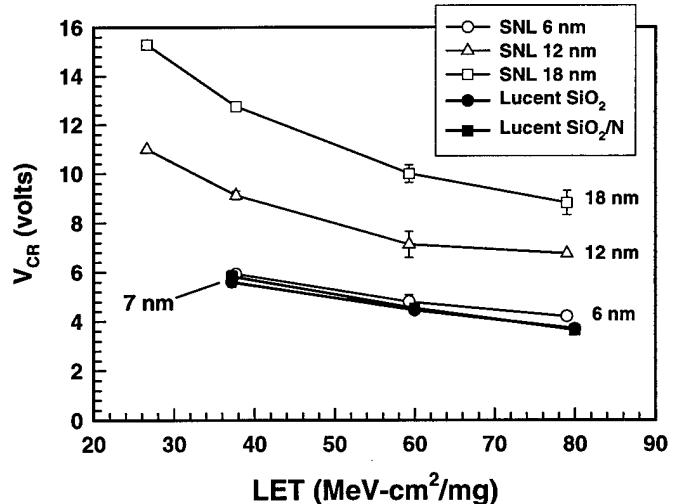


Fig. 3: Critical voltage to breakdown as a function of ion LET for capacitors from Lucent and Sandia. Solid symbols are data from this work, while open symbols are data from previous work for comparison [3].

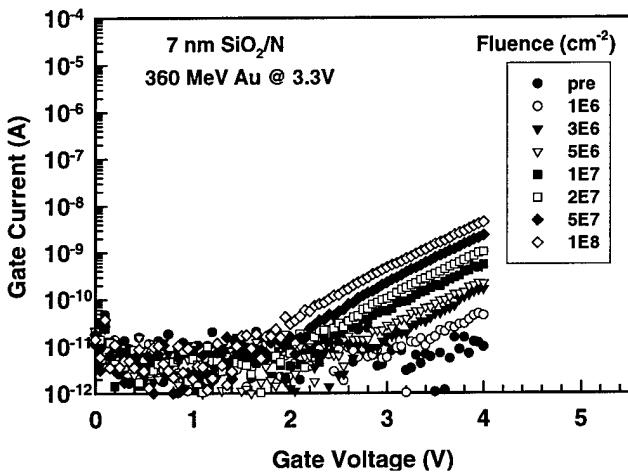


Fig. 4: Leakage currents increased in the nitrided oxide with increasing 360 MeV Au fluence while exposed with a bias of 3.3 V. No evidence of gate rupture was observed to the maximum fluence in these tests.

and 3.5 V for the nitrided oxides, and 0 and 3.5 V for the thermal oxide using 360 MeV Au ions, and at 5.2 V for the thermal oxide using Br ions.

Results are shown in Fig. 4 for a nitrided oxide at a gate bias of 3.3 V. Leakage increased with increasing fluence, but no evidence of gate rupture (i.e., low voltage leakage) was observed for this oxide. Note that gate rupture was measured at 3.7 V for this oxide in earlier SEGR tests at much lower total ion fluence. Results were similar for ion damage at the other biases.

After exposure to a fluence of  $10^8$  ions/cm $^2$  using 360 MeV Au, a standard SEGR test was performed on the device biased at 2.5 V. Bias was increased in 0.1 V steps from 3.0 V with additional fluences of  $10^6$  ions/cm $^2$  per step. As seen in Fig. 5, rupture was observed in this device at 3.7 V, consistent with the data plotted in Fig. 2 for devices with much lower fluence. Note that damage from the prior exposure of  $10^8$  ion/cm $^2$  can be seen in the curves at lower voltages in Fig. 5.

We can see the effect of precursor damage as a function of ion fluence by plotting leakage current at a given voltage. Such a plot for current at 4 V is shown in Fig. 6. For the nitrided oxides, increasing ion-induced damage was observed with increasing bias. The large increase in current at  $10^8$  ions/cm $^2$  for the nitrided oxide at 3.5 V bias (open squares) was due to an apparent breakdown. Note that damage buildup in the thermal oxide at 0 V (solid circles) was equivalent to the damage in the nitrided oxide biased at 2.5 V (open circles). No damage was observed with Br on the thermal oxides when biased at 5.2 V. The lower LET Br ion apparently causes less damage to the oxides than the higher LET Au ions, even when biased

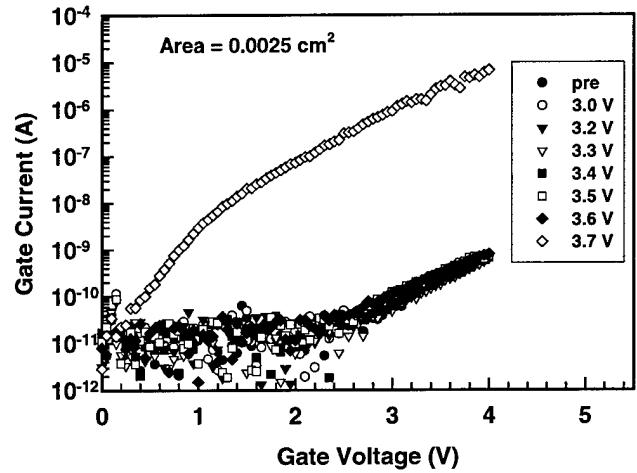


Fig. 5: Standard breakdown curves were measured on a nitrided oxide after exposure to a fluence of  $10^8$  ions/cm $^2$  360 MeV Au at a bias of 2.5 V.

close to the SEGR threshold (5.8 V in this case; see Fig. 3). This may mean that the ion damage observed in Fig. 6 is associated with displacement, as opposed to ionization, damage. We will explore this further in the full paper.

## DISCUSSION

The data in this work suggest that, at least to first order, single event gate rupture and damage in oxides due to ion irradiation are unrelated effects. The IV characteristic of SEGR exhibited a rapid increase in current at low voltages consistent with a low resistance shunt path through the oxide. On the other hand, damage due to ion irradiation showed a gradual increase in leakage current. Prior exposure to high ion fluence had no effect on SEGR in these devices, as seen in Fig. 5. Also, critical voltage to rupture was

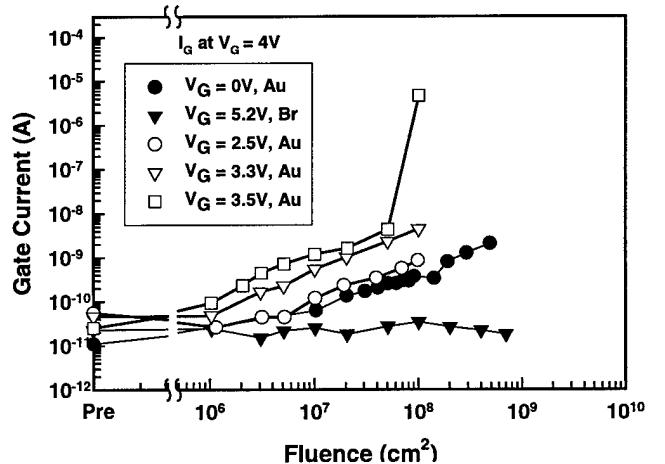


Fig. 6: Leakage current at 4 V as a function of ion fluence and bias for thermal oxides (solid symbols) and nitrided oxides (open symbols).

unchanged for thermal vs. nitrided oxides, as seen in Fig. 3. In one device, an oxide breakdown was observed at 3.5 V after a stress of  $10^8$  Au ions/cm<sup>2</sup>, in contrast to breakdown at 3.6 - 3.8 V observed at lower fluences. This may simply indicate that when biased close to the SEGR threshold significant ion damage may slightly reduce the SEGR threshold. Note that this breakdown occurred at extreme levels of fluence, well beyond where normal SEGR tests are performed and well beyond fluences that are encountered in space missions.

The fact that prior damage did not significantly affect critical voltage to rupture supports the hypothesis that SEGR is indeed a single ion effect, and is not dependent on prior ion strikes to condition the oxide. Wrobel [4] suggested that SEGR was a two step process: the first being the formation of a low resistance path through the oxide due to the high density plasma of the ion track through the oxide, and the second being the discharge of energy stored on the capacitor along this plasma wire. An alternate hypothesis for the first step is that the dense electron-hole plasma perturbs the local electric field at the cathode/oxide interface, resulting in charge injection into the oxide, which subsequently triggers rupture. Our data here cannot distinguish between these suggested mechanisms.

A difference in ion damage was noted between Br and Au ions. In space applications, the fluence of ions with LET of 80 MeV-cm<sup>2</sup>/mg or greater (comparable to 360-MeV Au) is on the order of .04 ions/cm<sup>2</sup>/year, while the fluence for ions with LET of 40 MeV-cm<sup>2</sup>/mg or greater (comparable to 290-MeV Br) is on the order of 0.4 ions/cm<sup>2</sup>/year. At these levels, it is unlikely that ion damage will significantly affect reliability in space. In the full paper we will present further data on ion damage in oxides, and will explore whether ion damage affects oxide reliability. We will also analyze the impact of energy deposition on damage in thin oxides through ionizing dose and non-ionizing energy loss (NIEL).

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## REFERENCES

- 1 A. H. Johnston, C. I. Lee, B. G. Rax, and D. C. Shaw, "Using Commercial Semiconductor Technologies in Space," Proceedings of the Third RADECS Conference, pp. 175-182 (1995).
- 2 G. M. Swift and R. Katz, "An Experimental Survey of Heavy Ion Induced Dielectric Rupture in Actel Field Programmable Gate Arrays (FPGAs)," IEEE Trans. Nucl. Sci. **NS-43**, pp. 967-972 (1996).
- 3 F. W. Sexton, D. M. Fleetwood, M. R. Shaneyfelt, P. E. Dodd, and G. L. Hash, "Single Event Gate Rupture in Thin Gate Oxides," IEEE Trans Nucl. Sci. **NS-44**, pp. 2345-2352 (1997).
- 4 T. F. Wrobel, "On Heavy Ion Induced Hard-Errors in Dielectric Structures," IEEE Trans Nucl. Sci. **NS-34**, pp. 1262-1268 (1987).
- 5 J. L. Titus and C. F. Wheatley, "Experimental Studies of Single-Event Gate Rupture and Burnout in Vertical Power MOSFETs," IEEE Trans. Nucl. Sci. **NS-43**, pp. 533-545 (1996).
- 6 C. F. Wheatley, J. L. Titus, and D. I. Burton, "Single-Event Gate Rupture in Vertical Power MOSFETs: An Original Empirical Expression," IEEE Trans. Nucl. Sci. **NS-41**, pp. 2152-2159 (1994).
- 7 D. J. DiMaria, E. Cartier, and D. A. Buchanan, "Anode Hole Injection and Trapping in Silicon Dioxide," J. Appl. Phys. **80** (1) pp. 304-317 (1996).
- 8 A. H. Johnston, "Radiation effects in advanced microelectronic technologies," presented at the 4<sup>th</sup> European Conf. On Radiations and Their Effects on Devices and Systems, Cannes, FR, September 15-19, 1997.
- 9 D. M. Fleetwood and N. S. Saks, "Oxide, Interface, and Border Traps in Thermal, N<sub>2</sub>O, and N<sub>2</sub>O-Nitrided Oxides," J. Appl. Phys. **79**, pp. 1583-1594 (1996).
- 10 M. Y. Hao, W. M. Chen, K. Lai, J. C. Lee, M. Gardner, and J. Fulford, "Correlation of Dielectric Breakdown with Hole Transport for Ultrathin Thermal Oxides and N<sub>2</sub>O Oxynitrides," Appl. Phys. Lett. **66**, pp. 1126-1128 (1995).
- 11 K. S. Krisch, L. Manchanda, F. H. Baumann, M. L. Green, D. Grasen, L. C. Feldman, and A. Ourmazd, "Impact of Boron Diffusion Through O<sub>2</sub> and N<sub>2</sub>O Gate Dielectrics on the Process Margin of Dual-Poly Low Power CMOS," IEDM Technical Digest, pp. 325-328 (1994).

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