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PROTOTYPE CIRCUIT BOARDS ASSEMBLED WITH NON-LEAD BEARING SOLDERS

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Abstract

The 91.84Sn-3.33Ag-4.83Bi and 96.5Sn-3.5Ag Pb-free solders were evaluated for surface mount circuit board interconnects. The 63Sn-37Pb solder provided the baseline data. All three solders exhibited suitable manufacturability per a defect analyses of circuit board test vehicles. Thermal cycling had no significant effect on the 91.84Sn-3.33Ag-4.83Bi solder joints. Some degradation in the form of grain boundary sliding was observed in 96.5Sn-3.5Ag and 63Sn-37Pb solder joints. The quality of the solder joint microstructures showed a slight degree of degradation under thermal shock exposure for all of the solders tested. Trends in the solder joint shear strengths could be traced to the presence of Pd in the solder, the source of which was the Pd/Ni finish on the circuit board conductor features. The higher, intrinsic strengths of the Pb-free solders encouraged the failure path to be located in proximity to the solder/substrate interface where Pd combined with Sn to form brittle $PdSn_4$ particles, resulting in reduced shear strengths.

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DISCLAIMER

Introduction

Lead-bearing solders have satisfied the electronics industry drivers of device miniaturization, greater functionality of package systems, and low cost manufacturing processes. However, it is becoming increasingly evident that the manufacturability and reliability margins offered by the Sn-Pb solders are shrinking with next-generation electronic packaging. In addition, increased emphasis is being placed on manufacturing processes and products that are more compatible with the environment. Minimizing the amount of hazardous materials in process waste streams has become an important objective. Likewise, new electronic products are being closely scrutinized for their impact on the environment, once that product has completed its useful life. Therefore, it is under these premises that the development of non-Pb-bearing solders has been pursued in a search for alternatives to the traditional 63Sn-37Pb (wt.%) alloy currently used in electronic products.

A study to identify Pb-free solder compositions that would be suitable for electronics applications was performed in two stages. First, candidate alloys were subjected to a series of laboratory "screening" tests in order to document their basic properties of (1) melting behavior, (2) solderability, and (3) mechanical strength. In the second phase of the investigation, the solders were used in the assembly of prototype, circuit board test vehicles. These test vehicles provided manufacturability information through defect analysis. The test vehicle solder joints were also exposed to accelerated tests of thermal cycling or thermal shock to estimate their reliability performance under anticipated service conditions.

Two alloy compositions were investigated: 96.5Sn-3.5Ag (wt.%) and 91.84Sn-3.33Ag-4.83Bi. The 96.5Sn-3.5Ag solder is the eutectic composition for that binary system, having a melting temperature of 221°C. The second alloy is an experimental solder developed at Sandia National Laboratories[1]. The solidus temperature of the 91.84Sn-3.33Ag-4.83Bi solder was 212°C; no separate liquidus temperature could be identified from thermal analysis scans performed at 1°C/min. The solidus temperatures of both Pb-free alloys were well above the 183°C value for the baseline 63Sn-37Pb solder.

Laboratory tests were performed on each of the Pb-free and 63Sn-37Pb solders to assess their solderability and solder joint shear strength properties. Solderability was evaluated using the meniscometer/wetting balance test[2]. This procedure measures the height (H) and weight (W) of the solder meniscus that forms on a flat plate coupon immersed edge-on into the solder bath. These parameters are then used to compute the solderability metric, the contact angle, θ_c:

$$\theta_c = \sin^{-1} \{[4W^2 - (\rho g P H^2)^2] / [4W^2 + (\rho g P H^2)^2]\} \qquad (1)$$

In equation (1), ρ is the solder density, g is the acceleration due to gravity, and P is the coupon perimeter contacting the solder bath. *The lower is the contact angle value, the better is the potential solderability.* The solderability data for the three alloys, determined for a test temperature of 260°C and using a rosin-based, mildly activated (RMA) flux, were: (1) 96.5Sn-3.5Ag, 36$\pm$3°; (2) 91.84Sn-3.33Ag-4.83Bi, 33$\pm$4°; and (3) 63Sn-37Pb, 17$\pm$4°. Although the values pertaining to the Pb-free solders were greater than that of the Sn-Pb solder, they were deemed acceptable so as to support a circuit board manufacturing process[3].

The shear strengths of the solders were measured by the ring-and-plug shear test. These measurements served to document the static mechanical behavior of the solders. The test sample geometry is shown in Fig. 1. The ring and plug were fabricated of OFHC Cu. The hole diameter of the ring and the diameter of the plug provided for a solder joint gap of 0.195 mm. Details of the test procedures are available in Reference 4. The shear strengths of the 91.84Sn-3.33Ag-4.83Bi, 96.5Sn-3.5Ag, and 63Sn-37Pb solders were measured as: 81$\pm$12 MPa, 55$\pm$1 MPa, and 38$\pm$2 MPa, respectively. The shear strength properties of the Pb-free solders were clearly superior to those of the 63Sn-37Pb alloy.

Prototype test vehicles that were of a Type I surface mount clock circuit design, were assembled with each of the two Pb-free solders and the baseline 63Sn-37Pb alloy. The circuit board layout and components were fully functional so that the electrical performance of the clock circuit could be monitored throughout the study. The assembled units were subjected to visual inspection at the as-fabricated level. Defect evaluation metrics included (1) solder

wetting/spreading on the circuit board pads and device I/O; (2) void formation; (3) part mis-registration over the circuit board pads; and (4) the formation of solder balls. Metallographic cross sections were also performed on selected solder joints. The latter evaluation was extended to test vehicles exposed to thermal cycling and thermal shock environments, as well. Mechanical shear tests were performed on selected components in order to document the strength of the solder joints in the as-fabricated condition as well as following environmental stress exposure.

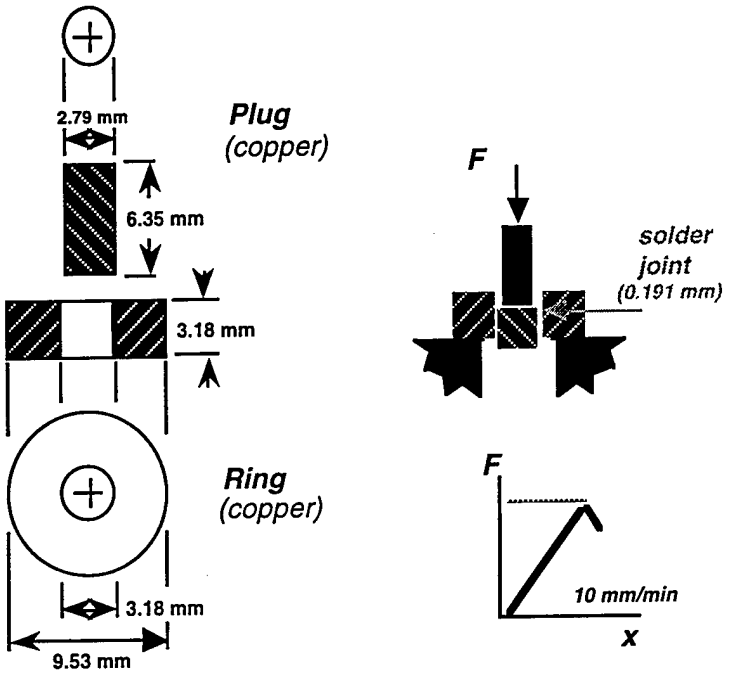


Fig. 1 Sample configuration for the ring-and-plug shear strength test.

Experimental Procedures

Solder Materials

Solder pastes of the 96.5Sn-3.5Ag (T_{eut} = 221°C) solder and baseline alloy 63Sn-37Pb (T_{eut} = 183°C) were obtained from a commercial supplier. The pastes contained an RMA flux and metal component of 90%; the metal particles had diameters of 40-50 μm. As an experimental alloy, the 91.84Sn-3.33Ag-4.83Bi ingot was blown into a powder having a 30-70 μm diameter range. The powder was added to an RMA flux vehicle to a level of 90.5%. The pastes were applied to the circuit board test vehicles by an automated printing process, using a 127 μm thick stencil.

Test vehicle

The test vehicle used in this study is shown in Fig. 2. Components were present on both the top and bottom sides of the circuit board. The board dimensions were 2.41 x 1.50 x 0.079 cm (thickness). The laminate was polyimide-quartz, having "1 oz." Cu features and covered with a dry solder mask. The Cu features were coated with an electroless Ni solderable finish, 3.8 μ (150 μin.) nominal thickness, followed by a protective finish of electroless Pd having a nominal thickness of 0.51 μ (20 μin). The circuit boards were baked at 120°C for 4 hours prior to assembly.

The top side of the test vehicle was populated with the following components: an 1825 chip capacitor (C6); four 0805 chip capacitors (C1, C2, C3, and C4); a beam-leaded transistor (Q1); three 1210 chip resistors (R1, R2, and R3); and a surface mount crystal resonator (Y1). The bottom side had the following components: 16 I/O small-outline integrated circuit package, SOIC (U1); a beam leaded transistor (Q2); an 1810 chip resistor (R4); a 1210 chip resistor (R5);

and a 1210 chip capacitor (C5). The chip capacitor and resistor terminations were coated with 100Sn finishes. The Y1 crystal resonator, Q1 and Q2 beam leaded transistors, and U1 integrated circuit package had their I/Os coated with 100Sn by hot dipping them in a 100Sn bath (270°C). An RMA flux was used in the process. The procedure was repeated three times to ensure complete removal of the Au plating[5].

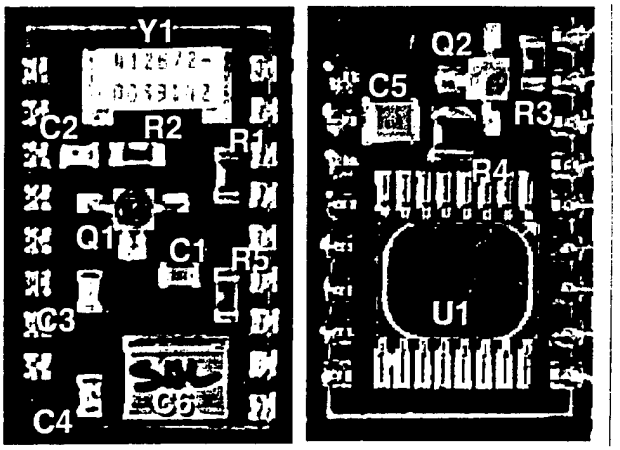


Fig. 2 Photograph of the top and bottom side of the populated test vehicle.

The test vehicles were soldered in a double reflow procedure in order to populate both sides of the circuit board (bottom side first, then top side). A 40/60 infrared/convection belt furnace was used with the chamber having a N_2 blanket. The furnace profiles were comprised of a pre-heat stage at temperatures in the range of 120-200°C and lasting for approximately 120 s. The reflow spike, peak temperature was set at 40°C above the liquidus temperature of the respective solder. The circuit boards remained above the solder liquidus temperature for a time duration of 30 s. No touch-up was permitted on the test vehicles once they were removed from the furnace. All boards were cleaned of flux residues using a certified semi-aqueous process.

Manufacturability assessment

The manufacturability assessment was described by quantitative figures-of-merit (FOMs) that were based upon defect counts taken from each of the circuit boards. The following guidelines were used:

Chip capacitors and Y1: Pad and termination wettability, scale of 0 (good) to 4 (poor); Voids, frequency count; Part registration, 0 (none) to 3 (severe) for each of lateral, longitudinal, and rotational vectors; and solder balls of 0 (numerous) to 5 (none).

SOT and SOIC: Pad and lead wettability, frequency count of pads having poor wettability; voids; mis-registration; and solder balls as noted above.

The final value of the FOM was determined by summing up the parameters from all of the test vehicles and dividing by the number of test vehicles.

Reliability assessment

An assessment of solder joint reliability began by exposing selected test vehicles to thermal cycle or thermal shock environments. The thermal cycle test was comprised of temperature limits of -55°C and 115°C; a ramp rate of 4°C/min; hold times of 30 min; for a total of 300 cycles. The thermal shock tests were performed with limits of -40°C and 115°C; near instantaneous temperature ramps (liquid-to-liquid transfer); 15 min hold times; for a total of 400 cycles.

The reliability assessment was based upon the integrity of the solder joints as determined by (1) visual inspection of metallographic cross sections and (2) the shear strength testing of

selected components. Figures-of-merit were assigned to metallographic observations of (1) void formation, 0 (numerous) to 5 (none); (2) solder fillet damage such as deformation or crack formation, 0 (numerous) to 5 (none); and (3) bond pad and device damage. The visual analysis was similarly applied to all of the solder joint configurations (leadless and leaded). Solder joint shear strength was determined as the maximum push-off load applied to the leadless chip capacitors (C1, C2, C3, C4, C5, and C6), chip resistors (R1, R2, R3, R4, and R5) as well as to the Y1 package. The tests were performed at a cross head speed of 10 mm/min.

Results and Discussion

Manufacturability assessment

Each of the three solders demonstrated excellent wetting of both the circuit board pads and device leads or terminations. Shown in Figs. 3 and 4 are optical micrographs of cross sections of as-fabricated Y1 and U1 solder joints, respectively. The solder joint in Fig. 3 was made with 91.84Sn-3.33Ag-4.83Bi solder; that in Fig. 4 was assembled with 96.5Sn-3.5Ag solder. It was observed that the Pd layer had been entirely dissolved into the molten solder at the time of assembly; therefore, the solders had wetted to the underlying Ni solderable finish. Palladium-tin intermetallic compound particles were observed to form intermittently along the solder/pad interface. A significant portion of the Ni solderable layer remained after the assembly process. Shown in Fig. 5 is an optical micrograph of the U1 solder joint made with the Sn-Ag-Bi alloy. It was observed that between 2.5 μm and 3.0 μm of the Ni layer was present. The Ni layer thickness that remained after processing with the Sn-Pb and Sn-Ag solders was somewhat less at 1.5 -2.0 μm. It is evident in this micrograph that a significant thickness of the underlying Cu layer was lost as part of the process used to deposit the Ni coating.

Dewetting was not observed on either the circuit board pad or device I/O for any test vehicles (FOM = 0). A few, isolated voids were recorded; but the FOM remained less than 0.5, indicating that the propensity for void formation was inconsequential for all solders. Package I/O mis-registration over the circuit board bonding pads was minor for the smaller 0805 chip capacitors (C1, C2, ...) and the chip resistors; the FOMs were in the range of 0.00-1.00 for all three orientations. However, the FOM became significantly greater for the larger packages that included the 1825 chip capacitor (0.00-1.40), the Q1 and Q2 beam leaded transistors (0.00-3.00), and the Y1 package (0.00-2.40). It should be noted that the magnitudes of the offsets would be inconsequential to the functionality of the solder joints. The greater level of part mis-registration for these larger packages was a consequence of their greater weight which hindered the molten solder surface tension from compensating for any placement mis-registration. It was

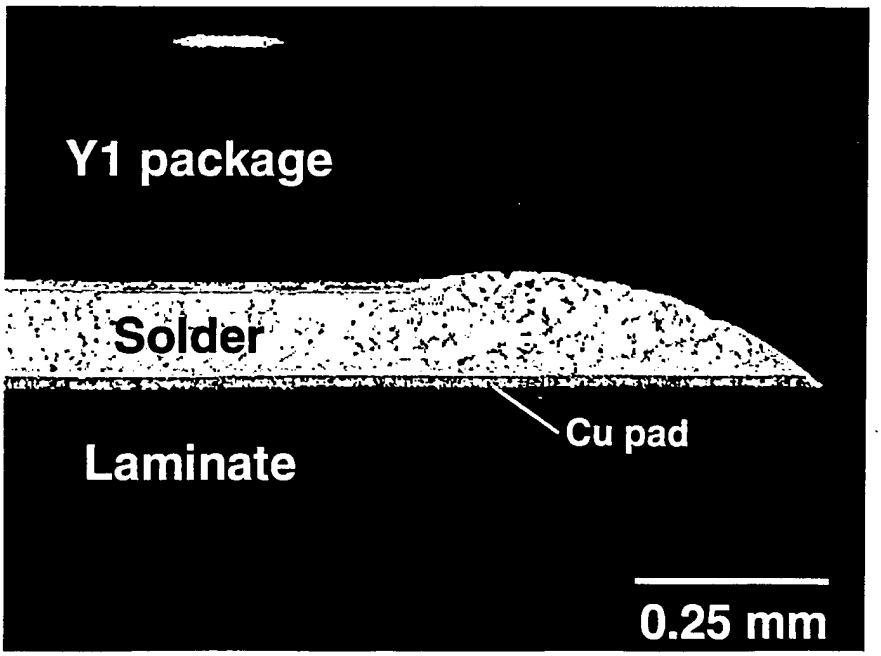
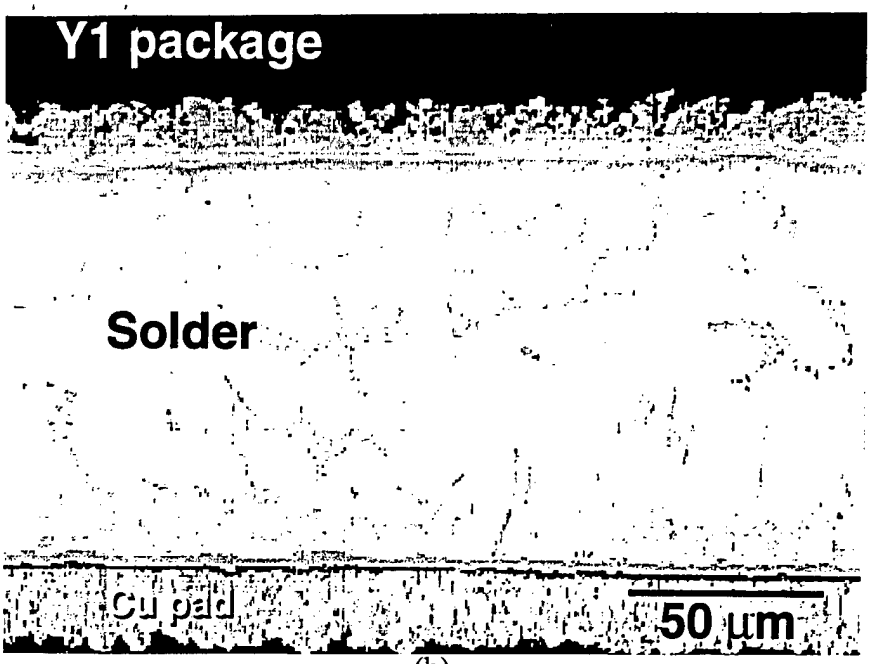


Fig. 3 (a)



(b)

Fig. 3 Optical micrographs of metallographic cross sections of an as-fabricated, Y1 solder joint made with the 91.84Sn-3.33Ag-4.83Bi solder at (a) low and (b) high magnification.

interesting to note that the degree of part mis-registration was not a function of the solder alloy, in spite of the different surface (interfacial) tensions between the three candidate solders. Finally, minimal solder ball formation was recorded from amongst all three solder alloys; the FOMs ranged from 4.4 (worst) to 5.0 and provided evidence as to the compatibility between the pastes and their respective process schedule.

Reliability assessment

The metallographic cross sections of the as-fabricated, thermal cycled, and thermal shocked test vehicles confirmed that all of the Pb-free solders exhibited excellent wetting of both the circuit board bonding pad and the particular package I/O. The cross sections of the as-fabricated units revealed some void formation in the solder joints. The FOMs recorded for the91.84Sn-3.33Ag-4.83Bi, 96.5Sn-3.5Ag, and 63Sn-37Pb solders were 4.5 ± 0.8, 4.3 ± 0.6, and 4.6 ± 0.8, respectively. However, these values did not indicate that the solder joint integrities would be jeopardized in any instance. No significant trends in void formation as a function of solder composition and/or package configuration were identified.

Close scrutiny was paid to the Cu pad/laminate interface of the as-fabricated, thermally shocked, and thermally cycled circuit boards. Because these solders, and in particular, the 91.84Sn-3.33Ag-4.83Bi alloy, were much stronger than the traditional 63Sn-37Pb solder, it was feared that residual stresses may move into those structures of the joint. The examination did not indicate that any damage had occurred at the Cu/laminate interface nor within the laminate structure.

The investigation of the solder joint cross sections was completed by assessing the extent of microstructural damage that was present at the time of manufacture as well as for those units following thermal shock or thermal cycle exposures. The FOMs from test vehicles in the as-fabricated condition as well as those metrics from test vehicles subjected to thermal cycling or thermal shock treatments are shown in Table I. Negligible damage in the as-fabricated solder joints was reflected by FOMs of 4.9 ± 0.3, 5.0 ± 0.0, and 5.0 ± 0.0 for the 91.84Sn-3.33Ag-4.83Bi, 96.5Sn-3.5Ag, and 63Sn-37Pb solders, respectively.

Thermal cycling did not cause significant microstructural damage in the case of the 91.84Sn-3.33Ag-4.83Bi solder. On the other hand, slight decreases were observed in the FOMs of the other two solders. In the case of the 96.5Sn-3.5Ag, some grain boundary sliding

appeared in the thermally cycled solder joints. Also, minor cracks were observed to have developed in the solder. The baseline 63Sn-37Pb solder joints exhibited light to moderate degrees of grain boundary and phase boundary sliding deformation in response to the temperature variations. These microstructural observations clearly indicated that the Pb-free solders resisted deformation to a degree that was equivalent to, or better than, the baseline 63Sn-37Pb solder. The thermal expansion coefficients were well matched between the ceramic

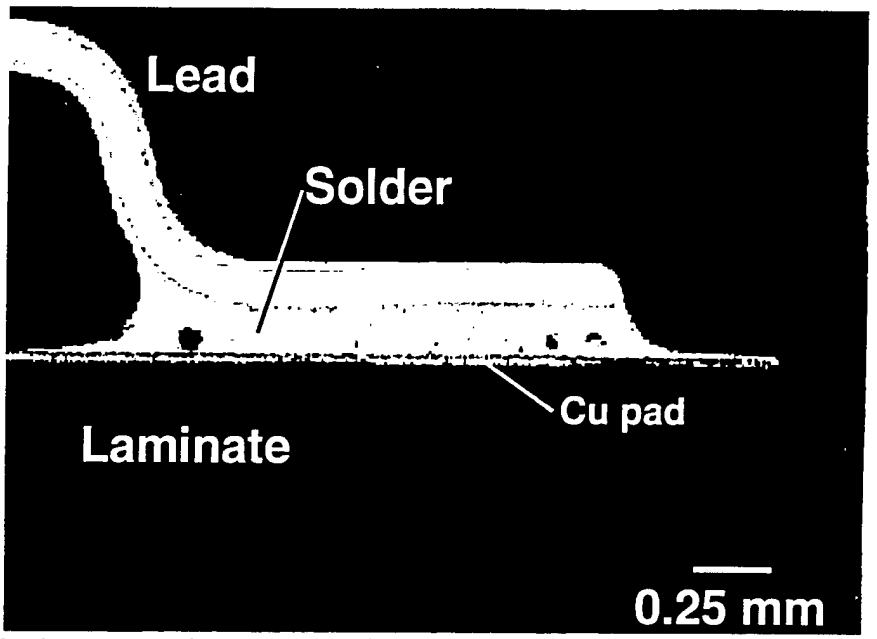


Fig. 4 Optical micrograph of metallographic cross section of an as-fabricated, U1 solder joint made with the 96.5Sn-3.5Ag solder.

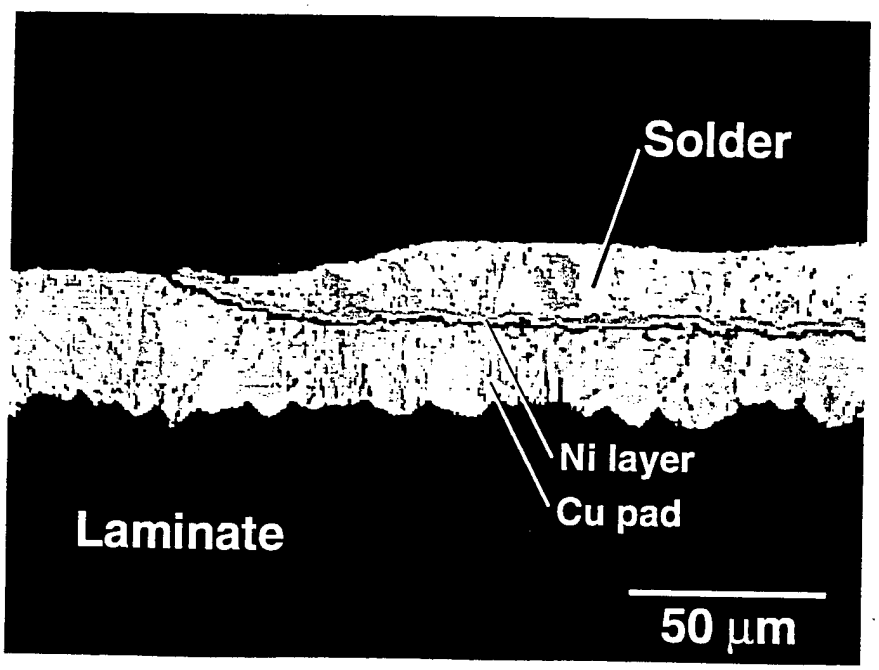


Fig. 5 Optical micrograph of the bonding pad of U1 solder joint made with the Sn-Ag-Bi alloy. The large, gray particles in the solder are the $PdSn_4$.

packages (5.0 ppm/C°) and polyimide-quartz laminate (8.0 ppm/C°). Therefore, the boundary sliding observed in the 96.5Sn-3.5Ag and 63Sn-37Pb solder joints was likely a consequence of a local thermal expansion mismatch mechanism; the fact that no such damage was observed in the

91.84Sn-3.33Ag-4.83Bi joints is an indication that this alloy has greater resistance to such deformation modes.

Table I Figures of Merit (FOMs) for Solder Fillet Damage
[0.0 (severe) < FOM < 5.0 (none)]

Test vehicle history	Fillet Damage FOM per Solder Alloy		
	91.84Sn-3.33Ag-4.83Bi	96.5Sn-3.5Ag	63Sn-37Pb
As-fabricated	4.9±0.3	5.0±0.0	5.0±0.0
Thermal cycle	4.9±0.2	4.6±0.6	4.5±0.5
Thermal shock	4.0±1.1	4.1±1.1	4.1±0.7

Thermal shock exposure caused a significantly greater degree of solder deformation in the joints of all of the candidate solders. Nearly equivalent drops in the FOMs to values of 4.1±0.7, 4.1±1.1, and 4.0±1.1 for the 91.84Sn-3.33Ag-4.83Bi, 96.5Sn-3.5Ag, and 63Sn-37Pb solders, respectively, were observed. The 91.84Sn-3.33Ag-4.83Bi solder exhibited largely surface cracks on the solder joint fillets. Surface cracks also appeared on the 96.5Sn-3.5Ag and 63Sn-37Pb solder fillets, along with some grain boundary and phase boundary sliding (63Sn-37Pb) deformation. These results indicate similar sensitivities by the solders to thermal shock environments. Since the thermal expansion mismatch was largely local in nature, the observed damage indicated a particularly heightened sensitivity by the solders to rapid temperature fluctuations. This sensitivity did not appear to be dependent upon the specific solder composition.

There was no indication of damage to the circuit board laminate, with any of the solders, following thermal cycling or thermal shock exposure.

Mechanical shear (push-off) tests were performed on selected leadless chip capacitors (C1-C6), chip resistors (R1-R5), and the Y1 package. The capacitors C1-C4 had the same configuration. Because no noticeable variation were observed amongst their strength data, the test values were combined into a single C' strength. The C5 and C6 test results were kept separate. Similarly, the strength data for resistor R1, R2, R3, and R5 were combined as R'. The push-off test data are illustrated in Table II. Because the C5 and C6 data showed trends similar to the combined C' results and the R4 data mimic the R' data, only the combined C' and R' strengths, along with the Y1 data, were listed in the table for the sake of brevity.

Table II Mechanical Strength (Load) of Solder Joints via the Shear Test
(±one standard deviation is in parenthesis below the mean value)

Test vehicle history	Shear Load (kg)								
	91.84Sn-3.33Ag-4.83Bi			96.5Sn-3.5Ag			63Sn-37Pb		
	C'	R'	Y	C'	R'	Y	C'	R'	Y
As-fab.	2.0 (0.8)	5.0 (2.9)	30.4 (2.8)	4.2 (1.7)	6.1 (1.9)	39.4 (8.6)	3.9 (1.4)	5.2 (2.0)	42.7 (3.9)
Th. cycle	1.8 (1.2)	5.5 (2.6)	48 (14)	2.7 (1.5)	6.2 (2.7)	34 (14)	3.6 (1.5)	5.2 (1.5)	33.1 (5.5)
Th. shock	1.5 (1.0)	4.6 (2.4)	42.3 (0.3)	1.2 (0.3)	5.6 (3.2)	41.8 (3.2)	3.8 (0.8)	5.5 (1.6)	39 ---

It is observed in the Table II data that the loads were similar between the three solder alloys. However, the ring-and-plug tests indicated that the solders exhibited a range of strength values from the highest strength of the 91.84Sn-3.33Ag-4.83Bi solder at 81±12 MPa, to the 96.5Sn-3.5Ag solder having a strength of 55±1 MPa, and the lowest strength belonging to the

63Sn-37Pb solder at 38±2 MPa. The following analysis was performed: Shear loads were calculated for the 63Sn-37Pb solder joints of each of the C' capacitors, the R' resistors, and Y1 package configurations. The C' and Y1 computed loads were based upon the ring-and-plug shear strength value (which agreed with published values) and a joint geometry having no fillets. The R' value was taken from a previous study[6]. The calculated loads were: C', 6.4 kg (no fillets); R', 4.5 kg (no fillets); and Y1, 33 kg. These loads were observed to be comparable to the data in Table II. Therefore, the Pb-free solders appeared to have suffered a strength decrease when introduced onto the circuit board test vehicles as compared to the ring-and-plug test results.

The reduced strengths of the component solder joints fabricated with the 91.84Sn-3.33Ag-4.83Bi and 96.5Sn-3.5Ag Pb-free solders was attributed to an effect by the Pd finish on the circuit board. The higher bulk strengths of these solders tend to drive the failure path under mechanical loads to occur at the solder/substrate interface[7]. The Pd layer of the Pd/Ni finish that was dissolved from the circuit board during soldering, remained in that very same region, having combined with Sn to form brittle $PdSn_4$ intermetallic compound particles. Those particles caused an apparent strength drop to solder joints by facilitating fracture there in the course of the test[8]. The lower bulk strength of the Sn-Pb solder allowed the failure path to remain away from the somewhat embrittled solder at the interface region; hence, only a modest difference of maximum shear load was observed.

A review was made of the impact of the thermal cycling and thermal shock environments on the strengths of the respective solder joints. Both the 91.84Sn-3.33Ag-4.83Bi and 96.5Sn-3.5Ag solders exhibited nominal strength drops in the C' data after thermal cycling and thermal shock exposures, more so after thermal shock tests and in particular, with the 96.5Sn-3.5Ag solder. No significant changes were observed with the R' and Y1 data, nor with any of the baseline 63Sn-37Pb strength data. These results suggest that the solder joints on the C' parts had become more sensitive to the (local) expansion mismatch stress that occurred during the temperature variations because of an increased concentration of Pd and thus, $PdSn_4$ intermetallic compound particles due to the reduced joint size. Damage to the solder was further hastened by the rapid temperature change used in the thermal shock environments. The same effect was not observed with 63Sn-37Pb solder because of the difference in preferred failure path caused by the lower bulk solder strength.

Conclusions

(1) Laboratory tests determined that the Pb-free solders 91.84Sn-3.33Ag-4.83Bi and 96.5Sn-3.5Ag had acceptable solderability performances for circuit board manufacturing, a point which was confirmed by defect analysis of assembled, prototype circuit boards later on.

[2] Thermal cycling had no significant effect on the microstructure of solder joints made with the 91.84Sn-3.33Ag-4.83Bi solder. Some degradation, in the form of grain boundary and phase boundary sliding, was observed in 96.5Sn-3.5Ag and 63Sn-37Pb (baseline) solder joints. Only the C' solder joints made with the two Pb-free solders exhibited a strength drop; all other joints (and those with the 63Sn-37Pb baseline alloy) exhibited no significant change in value.

(3) The quality of the solder joint microstructures showed a slight degree of degradation under thermal shock exposure for all of the solders tested. The shear strength data followed the same pattern as was observed after thermal cycling, except that the decreases in C' strengths with Pb-free solders were significantly greater.

(4) The shear strength trends were traced to the presence of Pd in the solder, a consequence of the Pd/Ni finish on the circuit board conductor features. The deformation/fracture behavior exhibited by the Pb-free solders encouraged the failure path to be located in proximity to the solder/substrate interface where Pd had combined with Sn to form brittle $PdSn_4$ particles that locally reduced the load-bearing capacity of the solders.

(5) All units remained electrically functional after thermal cycling and thermal shock exposures.

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