

SAND-98-0708C
SAND-98-0708C
CONF-980344--

**CHEMICAL SOLUTION DEPOSITION OF $\text{SrBi}_2\text{Ta}_2\text{O}_9$ (SBT)
FILMS FOR NON-VOLATILE MEMORY APPLICATIONS**

RECEIVED

MAR 25 1998

OSTI

**CHARLES D.E. LAKEMAN^a, TIMOTHY J. BOYLE^b, JUDITH A.
RUFFNER^b, MARK A. RODRIGUEZ^c**

^aTexas Instruments, Inc., P.O. Box 655012, Mail Stop 921, Dallas TX75265.;

^b Sandia National Laboratories, Advanced Materials Laboratory, 1001
University Blvd., SE, Albuquerque, NM 87106; ^cSandia National Laboratories
P.O. Box 5800, Mail Stop 1405, Albuquerque, NM 87185-1405

ABSTRACT

$\text{SrBi}_2\text{Ta}_2\text{O}_9$ (SBT) films have received considerable attention for use as non-volatile memory elements. We have developed a process to prepare SBT films with good ferroelectric properties at low temperatures. In this paper, we will present strategies used to optimize the properties of the films including film composition, the nature of the substrate (or bottom electrode) used, and the thermal processing cycle. Under appropriate conditions, $\sim 1700\text{\AA}$ films can be prepared which have a large switchable polarization ($2P_r > 10\mu\text{C}/\text{cm}^2$), and an operating voltage $\leq 2.0\text{V}$.

Keywords: $\text{SrBi}_2\text{Ta}_2\text{O}_9$ (SBT), thin film, substrate,, composition, processing

INTRODUCTION

In the search for ferroelectric materials for use as non-volatile memory elements, the bismuth layered perovskites, such as $\text{SrBi}_2\text{Ta}_2\text{O}_9$ (SBT) have emerged as leading candidates owing to their remarkable polarization fatigue resistance [1, 2, 3, 4]. Much research has been directed at tailoring processing conditions to optimize microstructure and properties for use in such devices [5]. Ideal target parameters are: switchable polarization, $2P_r \geq 10\mu\text{C}/\text{cm}^2$; coercive voltage, $V_c < 1\text{V}$; and operating voltage (defined as the voltage at which 80% of the switchable polarization can be switched) $\leq 2\text{V}$. These parameters indicate the need for thin films ($\leq 2000\text{\AA}$) for device applications. In addition, to be compatible with standard CMOS circuitry, maximum processing temperatures should not exceed 700°C .

In order to test the feasibility of SBT for such applications, many researchers have turned to chemical solution deposition (CSD) as a straightforward, rapid method of preparing thin films [6,7]. From the various deposition technologies available, several common features emerge: either complex solution preparation is required to solubilize all components, or high

DISTRIBUTION OF THIS DOCUMENT IS UNLIMITED

DTIC QUALITY INSPECTED 4

MASTER

19980422 040

DISCLAIMER

This report was prepared as an account of work sponsored by an agency of the United States Government. Neither the United States Government nor any agency thereof, nor any of their employees, makes any warranty, express or implied, or assumes any legal liability or responsibility for the accuracy, completeness, or usefulness of any information, apparatus, product, or process disclosed, or represents that its use would not infringe privately owned rights. Reference herein to any specific commercial product, process, or service by trade name, trademark, manufacturer, or otherwise does not necessarily constitute or imply its endorsement, recommendation, or favoring by the United States Government or any agency thereof. The views and opinions of authors expressed herein do not necessarily state or reflect those of the United States Government or any agency thereof.

processing temperatures (800°C) are needed to remove all organic components and form the required layered perovskite phase. Recently, a simple process has been reported, which employs readily available starting materials, and from which single phase, ferroelectric films can be formed on Pt/SiO₂/Si substrates at temperatures as low as 650°C [6]. In order to optimize properties, however, processing at 750°C was required. In this paper, we report experimental strategies to optimize the properties of SBT films prepared using this same process to make them compatible with the design parameters described above.

EXPERIMENTAL

SBT precursor solutions were prepared as described below. A complete description appears elsewhere [6]. Briefly, bismuth acetate (Bi(OAc)₃) was mixed and stirred with pyridine (Py). Separately, strontium acetate (Sr(OAc)₂) and tantalum ethoxide (Ta(OEt)₅) were mixed and dissolved in glacial acetic acid (HOAc). After stirring for ~10 minutes, the separate solutions were mixed together, whereupon the Bi(OAc)₃ dissolved. All solvents used in the process were dried using standard procedures, and all manipulations were carried out in a glove box under a dry argon atmosphere. Prior to deposition of any solution, substrates were cleaned with methanol followed by heating to 400°C for 10 minutes in air. After further stirring of the precursor solutions to ensure complete dissolution, films were deposited by spin-coating at 3000 - 7000 rpm onto modified Pt/SiO₂/Si wafers for 30s followed by drying on a hot-plate at 300°C for 5 minutes. After deposition of each layer the films were heated to the desired temperature (typically 700°C) for 30 minutes in flowing oxygen to crystallize the desired perovskite phase. Platinum top electrodes were sputter deposited through a shadow mask, and annealed at 550°C in air. Ferroelectric properties were measured using a Radiant Technologies RT-66A ferroelectric tester (Albuquerque, NM), and surface microstructures examined using contact mode atomic force microscopy (AFM, Nanoscope II, Digital Instruments, Santa Barbara, CA). Film thicknesses were measured using Dektak profilometry, and confirmed with scanning electron microscopy (SEM). Standard X-ray diffraction (XRD) was performed on thin films with Cu K_α radiation using a Siemens automated θ - θ powder diffractometer equipped with a diffracted-beam graphite monochromator and a scintillation detector. Parameters for standard scans were a 10-60° 2 θ range, 0.05° step-size and one second count-time.

RESULTS

Substrate

AFM micrographs for platinum electrodes on oxidized silicon wafers are shown in figure 1 (a), (b). Those wafers which had been annealed at 800°C had a larger grain size and a larger surface roughness than those annealed at

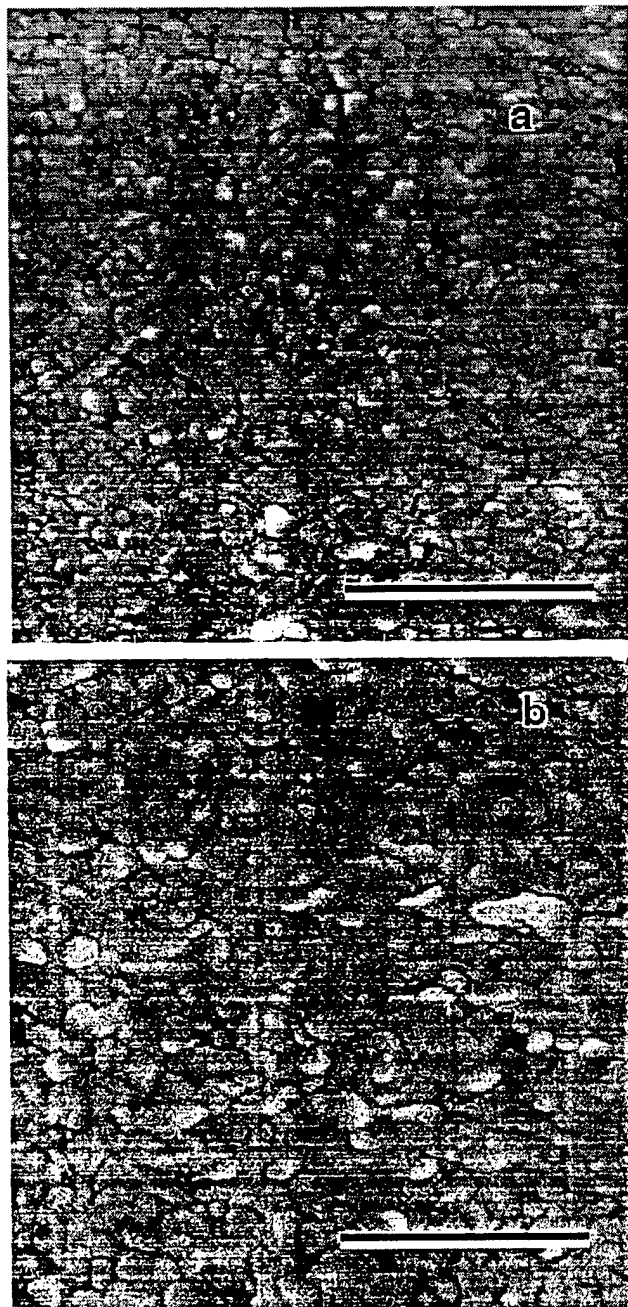


FIGURE 1. AFM micrographs for platinum electrodes on oxidized silicon wafers. Pt post-deposition anneal: a) 700°C; b) 800°C. Bar = 1 μ m.

700°C, though hillocks were not observed in either case. XRD data for the Pt electrodes indicates that heat treatment does not affect orientation, though the full width at half maximum (FWHM) value for the Pt (111) reflection decreases at higher annealing temperatures reflecting the increase in grain size.

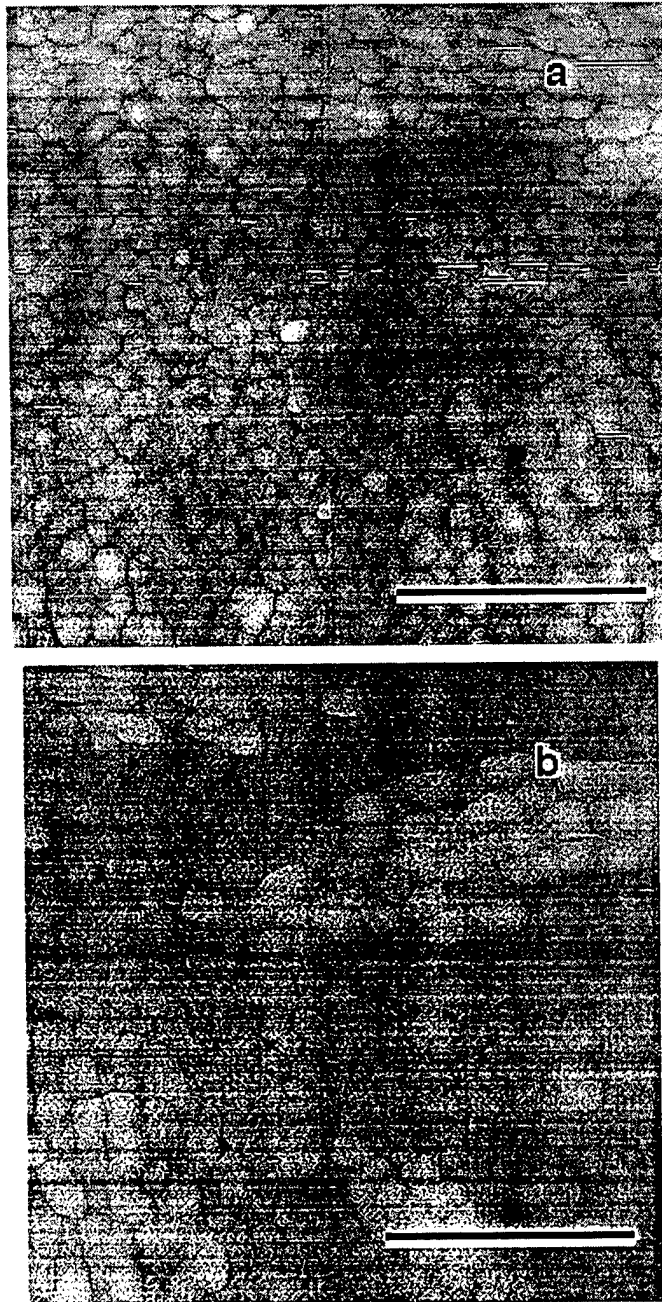


FIGURE 2. AFM micrographs for SBT films deposited onto platinum annealed at a) 700°C; b) 800°C. Bar = 1µm.

Not surprisingly, SBT films deposited onto substrates pre-heated at 800°C had a larger grain size than those deposited on substrates annealed at the lower temperature (Figure 2).

Figure 3 compares P-E polarization reversal behavior for ~5000Å SBT films of identical composition deposited onto substrates which had been pre-heated at

700°C or 800°C. It is apparent that annealing the platinum at higher temperatures results in films with higher measured polarization values, though coercive voltage values are similar for the two films. XRD data did not show significant orientation or texture differences.

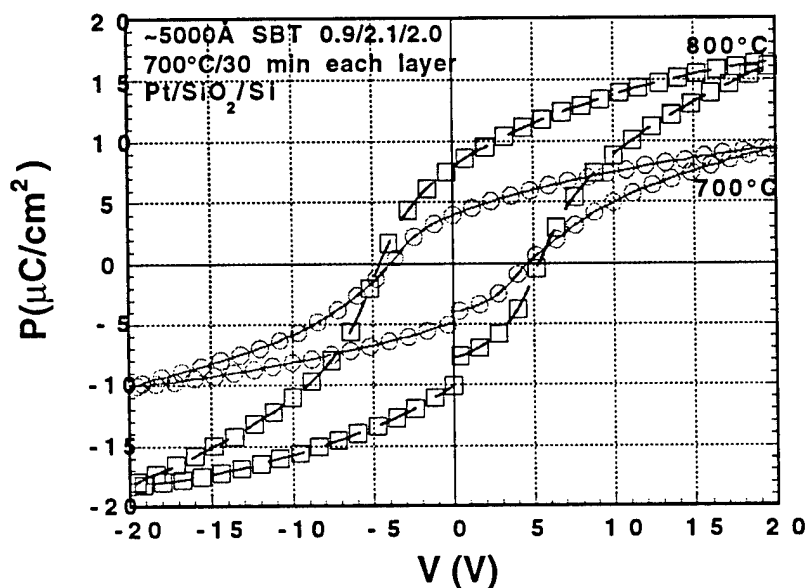


FIGURE 3. P-E polarization reversal behavior for $\sim 5000\text{\AA}$ SBT films deposited onto substrates heated at different temperatures.

Several other metallizations have also been studied as electrode systems. Figure 4 compares the ferroelectric switching behaviour of $2200\text{\AA}$ SBT 0.9/2.1/2.0 films deposited onto Pt, Ir, and IrO_2 -coated SiO_2/Si wafers. The Pt metallization was $2000\text{\AA}$ thick, and the Ir and IrO_2 were $3000\text{\AA}$ thick. Films deposited onto on Ir metallization had the highest P_r values, and the squarest loops. Again, XRD data do not indicate significant texture variations between the films deposited on different substrates, however, AFM data indicate that those grown on Ir electrodes had a larger and more uniform grain size than those on either Pt or IrO_2 . Data in the remainder of this paper are from films deposited onto Pt electrodes annealed at 800°C .

Composition

The SBT structure is flexible in that it allows stoichiometry variations for the Sr and Bi-sites. It has been demonstrated that Sr-deficiency can be compensated by additional Bi which occupies the vacant Sr sites [8]. This can affect the measured polarization and coercive field values, as shown in figure 4 for two-layer ($\sim 2200\text{\AA}$ total thickness) SBT films. Values of switchable polarization, $2P_r$, reach a maximum for the 10% Sr-deficient composition (SBT 0.9/2.1/2.0), and the coercive voltage for $2200\text{\AA}$ films decreases almost monotonically over

the entire composition range studied. However, even though the lowest value of V_c was measured for stoichiometric samples (SBT 1.0/2.0/2.0), measured $2P_r$ values at this compositions were too low for useful device application.

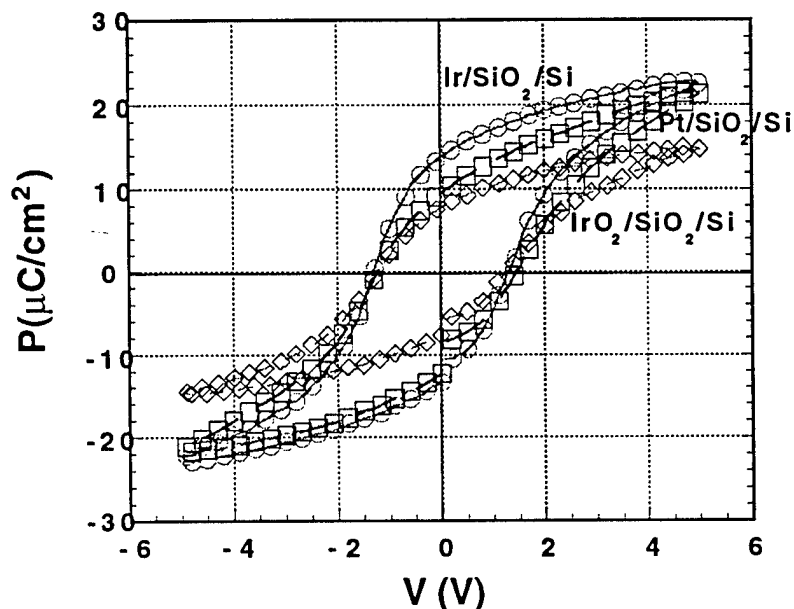


FIGURE 4. P-E hysteresis loops for 2200Å SBT 0.9/2.1/2.0 films deposited onto Pt, Ir, and IrO₂-coated SiO₂/Si wafers.

Processing

Following the deposition of top electrodes through a shadow mask, films were again annealed for 30 min. at 550 °C. Upon completion of the anneal the two films were cooled under different conditions. One film was rapidly quenched (≤ 15 s.) by quickly pulling the wafer from the furnace while the other was allowed to cool slowly over a 3 hour period to room temperature with the furnace. P-E hysteresis data are summarized in Table 1. There was an increase in both the saturation polarization and the remanent polarization values for films that were rapidly quenched compared with those that were cooled slowly, without any significant change in the resistivity. Furthermore, illumination of both devices with a UV-light source and an applied bias (± 7 V), a procedure known to de-pin domain walls [9], revealed that neither of the samples are in a pre-fatigued state. This suggests that the observed difference in ferroelectric behavior is not due to a conductive layer or charge trapping at domain walls in the SBT. We believe that the different P-E behaviors are due to competition

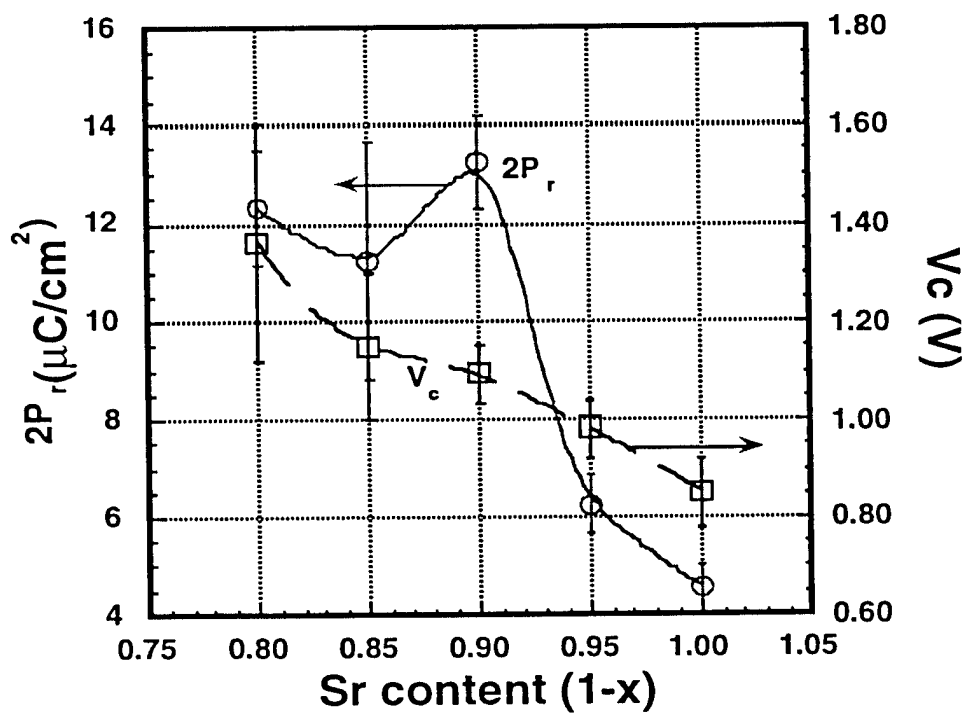
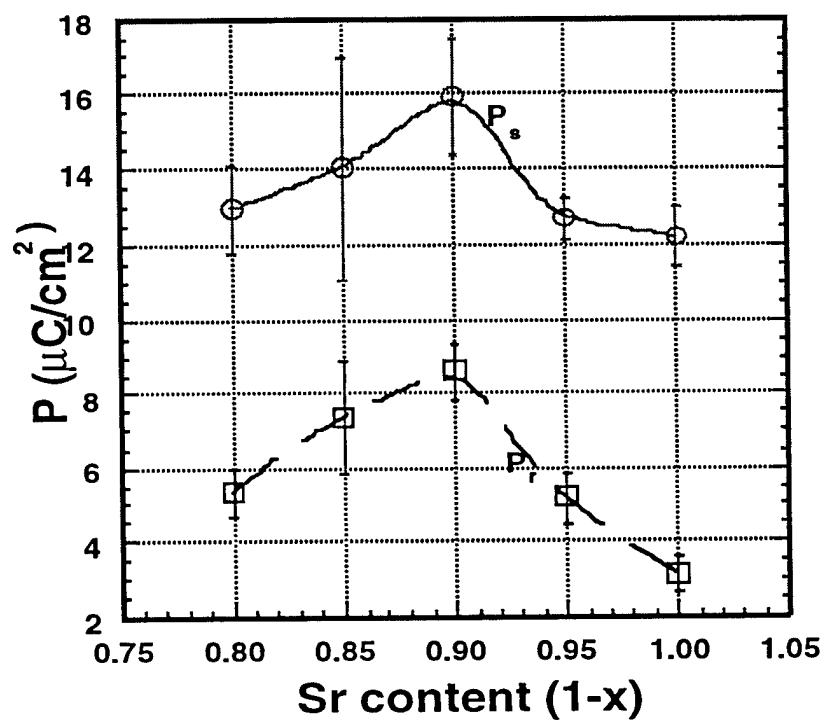


FIGURE 5. Measured polarization and coercive field values for $\sim 2200\text{\AA}$ SBT films on $\text{Pt}/\text{SiO}_2/\text{Si}$ substrate

between thermodynamic and kinetic phenomena at the ferroelectric-ferroelectric phase transition at $\sim 330^\circ\text{C}$, and work is in progress to understand this in more detail.

Property	quenched	slow-cooled
P_r ($\mu\text{C}/\text{cm}^2$)	7.0 ± 1.0	5.0 ± 1.0
P_s ($\mu\text{C}/\text{cm}^2$)	14.5 ± 2.5	13.5 ± 0.5
E_c (kV/cm)	50 ± 6	40 ± 10
ρ ($\Omega\text{-cm}$)	$\sim 1.8 \times 10^{10}$	$\sim 1.5 \times 10^{10}$

TABLE I Comparison of the ferroelectric properties of rapidly quenched and slowly cooled SBT films.

In order to minimize the operating voltage, films should be as thin as possible. This can be accomplished by increasing the spin-coating speed. Not surprisingly, thickness decreased monotonically with increasing spin-speed, to $\sim 1500\text{\AA}$ at a speed of 7500rpm for a 0.2M solution. However, at these thicknesses, yield decreased significantly, and work is in progress to improve this. The optimum P-V characteristics obtained for a film on a $\text{Pt}/\text{SiO}_2/\text{Si}$ substrate are shown in figure 6. With a thickness of $\sim 1700\text{\AA}$, $2P_r \sim 10\mu\text{C}/\text{cm}^2$, the applied voltage at which $0.80 \times 2P_{r\text{max}}$ is switched is $\sim 2.0\text{V}$.

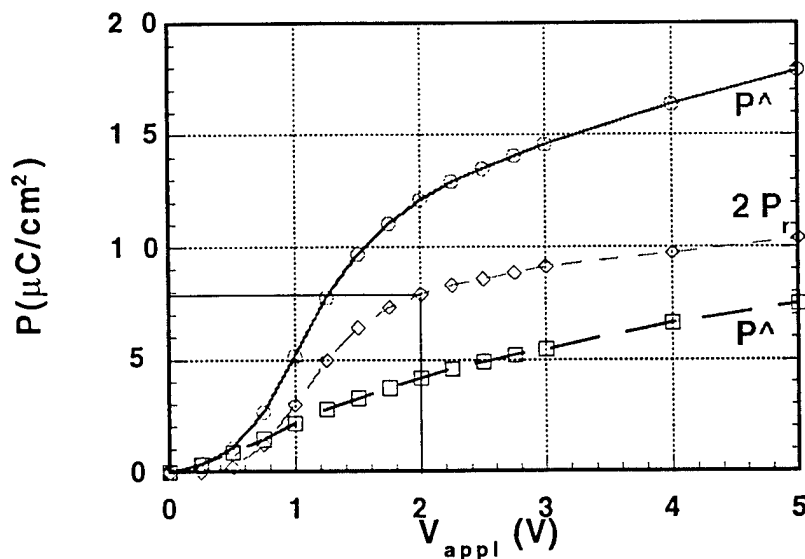


FIGURE 6. P-V characteristics for a $1700\text{\AA}$ SBT film on a $\text{Pt}/\text{SiO}_2/\text{Si}$ substrate.

SUMMARY

We have prepared $\text{SrBi}_2\text{Ta}_2\text{O}_9$ (SBT) films on a variety of substrates using a chemical solution deposition process followed by heating at 700°C . We have found that substrate microstructure, film composition and control over post-SMTE thermal processing can be optimized to tailor film properties to meet parameters suitable for integration.

ACKNOWLEDGEMENTS

This work was supported by Texas Instruments, Inc. and the United States Department of Energy under contract DE-AC04-94AL85000. Sandia is a multiprogram laboratory operated by Sandia Corporation, a Lockheed Martin Company, for the United States Department of Energy. We would like to acknowledge the assistance of B.A. Hernandez, and C.D. Buchheit of Sandia National Laboratories, and Drs. S. Summerfelt, T. Moise, and S. Yamanaka of Texas Instruments.

REFERENCES

1. See for example, Ferroelectric Thin Films IV and V, Mater. Res. Soc. Symp. Proc., **361** and **433**, (1995, and 1996).
 2. See also, Proc. IX ISIF, Santa Fe, NM, March 3 - 5, 1997, Eds D.B. Dimos, and B.A. Tuttle, in *Integrated Ferroelectrics*, **17**, **18**, (1997).
 3. R.E. Jones, P. Zurcher, P. Chu, D.J. Taylor, Y.T. Lii, B. Jiang, P.D. Maniar, and S.J. Gillespie, *Microelectronic Engineering*, **29**, 3, (1995).
 4. H.N. Al-Shareef, D. Dimos, T.J. Boyle, W.L. Warren, and B.A. Tuttle, *Appl. Phys. Lett.*, **68**, 690, (1996).
 5. T. Noguchi, T. Hase, and Y. Miyasaka, *Jpn. J. Appl. Phys.*, **35**, 4900, (1996).
 6. T.J. Boyle, C.D. Buchheit, M.A. Rodriguez, H.N. Al-Shareef, B.A. Hernandez, B. Scott, and J.W. Ziller, *J. Mater. Res.*, **11**, 2274, (1996).
 7. K. Amanuma, T. Hase, and Y. Miyasaka, in Ferroelectric Thin Films IV, Mater. Res. Soc. Symp. Proc., **361**, 21, (1995).
 8. T. Noguchi, T. Hase, and Y. Miyasaka, *Integrated Ferroelectrics*, **17**, 57, (1997).
 9. W.L. Warren, D.B. Dimos, B.A. Tuttle, R.D. Nasby, and G.E. Pike, *Appl. Phys. Lett.* **65**, 1018, (1994).
-

M98003352



Report Number (14) SAND--98-0708C
CONF-980344--

Publ. Date (11) 199803

Sponsor Code (18) DOE/DP, XF

UC Category (19) UC-700, DOE/ER

DOE