Importance of Ion Energy on SEU in CMOS SRAMs

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Abstract— The SEU responses of 16 Kbit to 1 Mbit SRAMs irradiated with low and high–energy heavy ions are reported. Standard low–energy heavy ion tests appear to be sufficiently conservative for technologies down to 0.5 μm.

I. Introduction

Single–event upsets (SEUs) are caused by the passage of energetic charged particles (such as protons, neutrons, or heavy ions) through a microelectronic device. Heavy–ion tests at accelerator facilities are frequently performed to study mechanisms of SEU, estimate on–orbit error rates, and qualify parts for use in space–based systems. In most facilities used for such SEU testing, the energy of the particles is on the order of a few (1–10) MeV per nucleon. In the actual space environment, the energy of particles is on the order of tens of MeV/nucleon to hundreds of GeV/nucleon, with a peak flux at a few hundred MeV/nucleon [1].

The lack of available accelerators capable of providing relativistic ions has limited the amount of high–energy data presented in the literature [2]. Recent SEU tests at high–energy accelerator facilities have indicated that there may be differences in device response to particles with the same linear energy transfer (LET) but different energies. Differences between low and high–energy ion tests have been seen to date in both the SEU threshold and saturation cross–section [3,4], single–event multiple–bit upset (MBU) occurrence [5], and unexplained inconsistencies in single–event burnout data [6]. However, the data are generally sparse, and in some cases, no appreciable difference has been observed between low and high–energy heavy ion data [7,8]. It is also not always clear whether identical parts, test procedures, and test equipment have been used to obtain the reported results. Nonetheless, the available results are worrisome in that they raise concerns about the fidelity of accelerator–based tests for simulating the response of parts to the real high–energy ion environment found in space [9].

The purpose of this work is to present and analyze a new set of high and low–energy heavy ion data, measured under well–controlled experimental conditions (i.e., same parts, procedures, and equipment). A variety of CMOS SRAM technologies and devices has been studied, with gate lengths ranging from 1 μm to 0.5 μm and integration level from 16 Kbit to 1 Mbit. Simulations of the ion track structure and device response are presented to probe the underlying physical mechanisms. Limitations of current device simulators for modeling realistic ion track structures are discussed.

II. Experimental Details

Test Procedure

Low–energy irradiations were performed using the Tandem Van de Graaff at Brookhaven National Laboratory, and high–energy irradiations were done at the GANIL double cyclotron facility in France. Because the goal of the experiment was to examine what might be small differences in the upset cross–section curve, we deemed it critical to try to remove potential sources of variation other than the ion energy. Each part was tested with the same procedure and equipment at both locations. In addition, for each device type, 2–4 parts were fully characterized at several angles to give an indication of part–to–part variation.

A secondary goal of the experiment was to compare SEU results obtained with CEA's equipment using a static test method to those obtained with Sandia's equipment using static and dynamic test methods. For the static test method, the SRAMs are written with a specific pattern, irradiated to a given fluence, and after the beam is turned off the parts are read and errors are counted. For dynamic tests, the parts are written with a pattern and continually read and checked for errors while the beam is on. If an error is detected the part is rewritten "on the fly." The beam is turned off only after a given number of errors has been detected or a given fluence has been reached. Previous experiments have shown SRAMs to have a greater sensitivity to SEU during dynamic operation than static operation [10]. Indeed, SEU in SRAMs may have some dependence on the operating frequency [11]; in the present work all dynamic tests were performed at 1 MHz.

DISCLAIMER

Devices Tested

Table 1 shows the mix of devices tested in this work. A variety of technologies was tested to determine if high–energy effects were specific to a given technology or more general in nature. The Matra MHS parts ranged from a 64 Kb rad–hard SRAM test vehicle in a 1–μm technology to a commercial 1 Mb SRAM processed in a 0.5–μm technology. The Sandia parts are 16 Kb SRAM test chips from Sandia's radiation–hardened 0.5–μm shallow–trench isolated CMOS6(r) technology. The 64 Kb and some of the 16 Kb SRAMs chosen for this test had feedback resistors, while the 1 Mb and 256 Kb SRAMs had no feedback resistors. Parts were tested at nominal (5 V) and worst–case (4.5 V) bias conditions using several vector sets. No significant differences were observed between results using different patterns, and only slight differences between nominal and worst–case bias.

III. Experimental Results

High vs. Low–Energy Comparison

Figure 1 shows the measured upset cross–section *vs.* LET of the Matra 256 Kb SRAM, for low and high–energy ions. The data shown here were taken using the static test method and CEA equipment. Almost no difference is observed in the upset cross–section curves measured with low and high–energy ions, and a single Weibull distribution fits all of the data. In fact, plotted against a linear LET axis, the differences are hardly noticeable, so we re–plot the data in Figure 2 using a log LET axis, along with data for a part from another lot (solid squares). Note that the variation in cross–section due to energy is roughly the same as the variation from lot to lot; there is little evidence of a high–energy effect for these devices. Data for all of the devices tested and new high–energy data at intermediate LETs (2–50 MeV–cm²/mg) will be presented in the full paper.

Table 1. SRAMs tested in this work.

Device	Device Type	Source	Technology
M65608E	1 Mbit SRAM	Matra MHS	0.5 μm, Rad Tolerant
M65608	1 Mbit SRAM	Matra MHS	0.5 μm, Commercial
HM65656	256 Kbit SRAM	Matra MHS	0.8 μm, Rad Tolerant
M65964	64 Kbit test SRAM	Matra MHS	1 μm, Rad Hard
TA786	16 Kbit test SRAM	Sandia	0.5 μm, Rad Hard

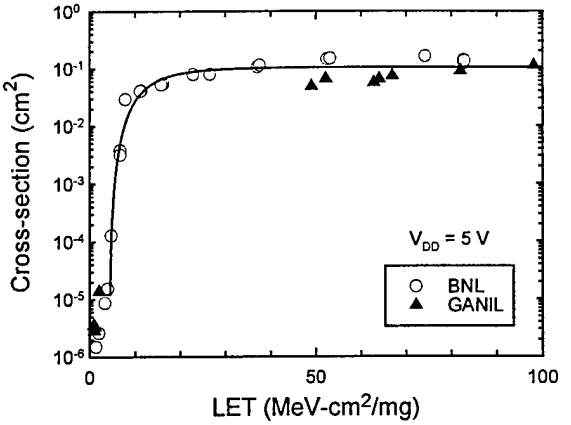

Figure 1. High–energy and low–energy upset cross–section curves for Matra 256 Kbit SRAM.

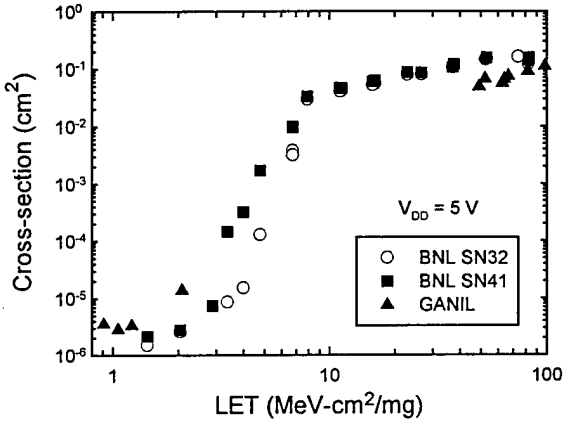

Figure 2. Comparison of high to low–energy variation with lot–to–lot variation at low energy.

Test Method Comparison

Figure 3 compares three different test method and equipment combinations. Low–energy ion data is shown for the Sandia 16 Kb SRAMs without feedback resistors using the static test method with both CEA and Sandia equipment, and using the dynamic test method with Sandia equipment. Results from all three tests appear to be equivalent, indicating no test equipment issues and little difference between static and dynamic results for these devices. Results of the test method comparison were similar for the Matra 256 Kb SRAMs.

IV. Heavy Ion Track Structure

Any differences observed in SEU response to low *vs.* high–energy ions are expected to be caused by the different radial and depth profiles of the generated carrier density along the ion track. For example, at a given LET, a high–energy cosmic ion track will have a much larger radius and much longer range. This might

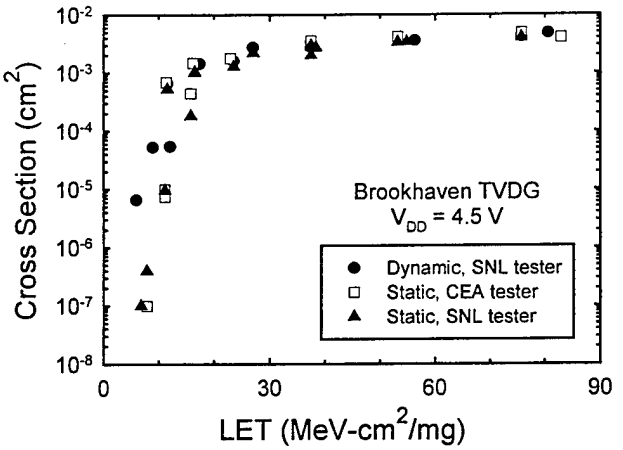

Figure 3. Comparison of Sandia 16 Kb SRAM cross–section curves for different test methods and equipment.

lead to different charge–collection properties, and hence, different SEU response.

Charge production around the path of an incident ion is accomplished by the release of energetic electrons (also referred to as delta rays) along the track, which subsequently travel away from the path and release further electron–hole pairs. The higher the energy of the incident ion, the higher the energy of the delta rays and the larger the radial extent of the induced charge distribution. The ion loses energy as it passes through the target, and the delta rays become less energetic, releasing charge nearer the ion path as the ion nears the end of its range. Incident ions therefore generate a characteristic cone–shaped charge plasma in the silicon. Both Monte Carlo and analytic models that describe ion tracks have been developed and used to study track structure effects [9,12–14]. We have developed an analytic track structure program (**R**adiation–**I**nduced **T**racks in **S**ilicon, or RITSI), based on the formalism described in [13] and [14]. A more complete description of this code will appear in the full paper.

Figure 4 compares the radial track structure of two ions with approximately the same incident LET of 4.5 MeV–cm²/mg: 15 MeV C and 4.8 GeV Fe (ranges in silicon are 14.5 μm and 2.7 mm, respectively). Generated charge density at the silicon surface is shown, as a function of radius from the center of the ion track. The maximum delta–ray radius at the surface of the 15 MeV C strike is about 0.14 μm, so beyond this point the carrier density falls to zero. For the 4.8 GeV Fe strike the maximum delta–ray radius is over 200 μm, so a low density of carriers (with respect to the central core of the track) exists out to this point. For the high–energy ion, the charge deposited beyond 0.14 μm amounts to about 25% of the total. Since the curves have the same integral charge, this means the high–energy ion has 25% less charge in the central region of the track (seen in Fig. 4 as the region between 0.01 μm and 0.1 μm where the iron curve drops below the carbon curve). If there were a difference in the SEU response to the two ions, one would expect the low–energy ion to be more upsetting since the track is more concentrated and can deposit a greater amount of charge in a small sensitive volume. For the high–energy ion, more charge is deposited at large distances where it may not be collected. Still, this is expected to be a small effect, since even for the high–energy ion, 85% of the charge is deposited within 2 μm of the ion path.

While similarities in radial track structure may argue against large differences between low and high–energy SEU results, there are cases where differences are likely. Due to the larger radial extent of the track, charge deposited by a single high–energy ion could be collected at neighboring sensitive junctions and induce multiple upsets. Furthermore, in grazing angle irradiations with high–energy ions, the greatly increased range along the particle path leads to many more cells being upset than would be seen with the shorter range of low–energy ions [5]. There may also be other cases where the larger range of high–energy ions leads to different results, such as devices sensitive to charge collection deep within the substrate, or cases where the ions must pass through a great deal of material to reach the sensitive region [15]. There may also be devices with low doping densities where even with low generated charge densities the larger radial extent of the track has some effect.

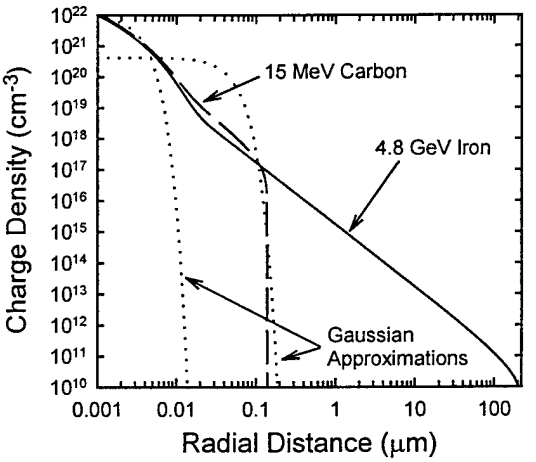

Figure 4. Radial track structure of low and high–energy ions with the same incident LET. Comparison with gaussian approximations to the center and edge regions. All curves have the same integral charge.

V. 3D Simulations

Previous studies have examined the effects of using different track structure descriptions for charge–collection simulations [16], but have not explicitly compared low–energy ions to high–energy ions. Many device simulation codes do not allow accurate description of ion track structures. The most common method is to describe the radial distribution of carriers as a gaussian function, which can not simultaneously fit the core density and the track radius, as shown in Figure 4. Blind use of a gaussian with a small or large radius (depending on ion energy) will lead to an inaccurate comparison of high and low–energy results. For example, Figure 5 shows simulated struck drain voltage transients for low and high–energy ion strikes to a CMOS6(r) SRAM cell. The simulated ions, 345 MeV Au and 5.7 GeV U, have about the same incident LET of 85–90 MeV–cm²/mg. The tracks were described in the DAVINCI device simulator as gaussians with a variable 1/e radius equal to the maximum delta ray range of each ion (as an illustration only). For the two gaussians to have the same integral charge when one has a much larger radius, the core concentration for the high–energy ion is *much* lower than for the low–energy ion. The core region of the two tracks will in fact be similar in density (Fig. 4). Thus, the results shown in Figure 5 greatly underestimate the charge-collection response to the high-energy ion, with the low–energy ion easily causing upset while the high–energy ion has almost no effect. This is clearly in contradiction with the experimental data of Figure 1, and expectations based on realistic track structures. In the full paper we will show results of device simulations using more realistic track structures generated by RITSI.

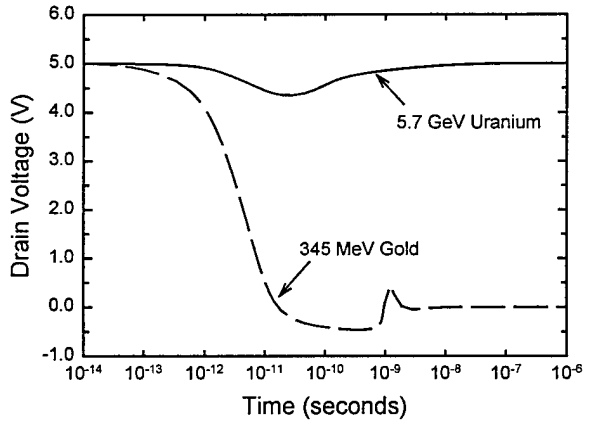

Figure 5. Simulated struck drain transients in CMOS6(r) SRAM cell using unrealistic gaussian track structure description for low and high–energy ions.

VI. Conclusions

Using carefully controlled experiments, we have demonstrated that for the technologies examined here, no significant difference is observed between low and high–energy heavy ion SEU data. This suggests that standard low–energy ion testing is sufficiently (and not overly) conservative for technologies down to 0.5 μm.

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