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The Self-Energized Credential System for the Plutonium Protection System

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THE SELF-ENERGIZED CREDENTIAL SYSTEM [illegible]
[illegible] PROTECTION SYSTEM

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ABSTRACT

The elements of the Self-Energized Credential System installed at Hanford, Washington, as part of the Physical Protection System operational demonstration [illegible] System concepts, electromagnetic fields, [illegible] are discussed.

NOTICE

[illegible]

This work was sponsored by the Department of Energy/Office of Safeguards and Security (DOE/OSS) as part of the overall Sandia Fixed Facility Physical Protection Program.

CONTENTS

ILLUSTRATIONS

FOREWORD

Development of the Self-Energized Credential System (SECS) was begun in late 1976 and the system was installed at Hanford, Washington, in early 1978. The system is distinguished by the two features that the credential is passive, and that the bearer does not have to alter natural movement in order to use the credential. The first feature makes the credential long lived, and the second makes it both unobtrusive and convenient.

The intended use of the SECS is to monitor the passage of credentials into or out of a controlled area. It is assumed that the credential is being worn by the bearer to whom the credential was issued. Such an assumption is reasonable when the SECS is used to enforce the safety "Two-Man Rule" in a hazardous work area, but the assumption must be verified by auxiliary means when the SECS is part of a physical security system.

The SECS is used as part of the Plutonium Protection System (PPS) demonstration at Hanford which is concerned both with physical security of material and the safety of personnel.[1] The SECS is used in three places in the PPS. One installation is near the entrance to the vault personnel corridor, the second is located within the identification booth along the same corridor, and the third is at the entrance to the MOC/MAC System area. This report provides a discussion of the concept and major features of the SECS followed by a detailed description of the component electronics.

THE SELF-ENERGIZED CREDENTIAL SYSTEM FOR THE PLUTONIUM PROTECTION SYSTEM

System Description

The concept of the SECS is set forth, the major components are identified, the coding method explained, and the results of testing for the effects of the system upon heart pacemakers are summarized.

Concept of Operation

The basic idea of the SECS is to use the coupling between a fixed loop and a moving loop to transfer power from the fixed to the moving loop in order to send an identification code back to the fixed loop. The fixed loop is large enough to provide a passageway through its interior and is referred to as the "portal" loop. The moving loop is wound on a frame which contains a printed circuit card on which the code is permanently stored to form a credential. The portal loop transmits a continuous tone at 110 kHz, and the credential transmits the code in bursts of a 55-kHz tone (Figure 1). A diplexer is used to separate the two signals at the portal loop. The 55-kHz tone burst is amplified, converted to binary form in the decoder, and tested to see if certain format and parity conditions are met. If the binary code is validated, it is made available for transmission to an operations center. Each of the major components will be treated fully in later sections after two topics of overall interest are treated.

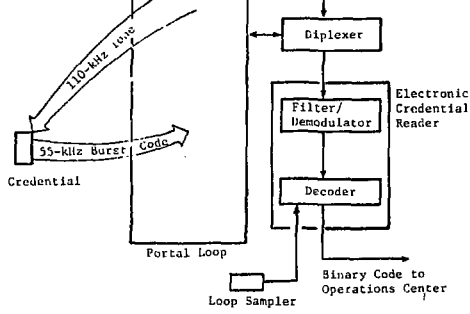

Figure 1. Major Components

Coding Considerations

A group of four hexadecimal (HD) digits was chosen for the code word in order to provide a useful number of codes that could be implemented within the limited size of a credential. The HD digits are grouped as two pairs with three sync bits and a parity bit added to each pair. The binary representation (Figure 2) is that of two EIA RS232-C format subwords within a 24-bit code.

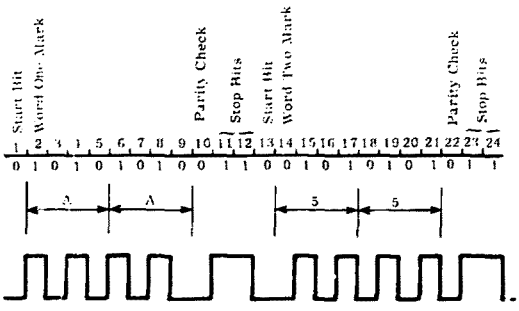

Figure 2. Code Structure

The length of the subword is set by the choice of electronic components in the decoder. The first digit in each HD pair is fixed as 1 and 0 respectively, so the first HD digit is always eight or greater and the third HD digit does not exceed seven. These fixed binary digits allow the decoder to distinguish between the two subwords, but reduce the number of available codes from 65,536 to 16,384. This number is further reduced because the bit stream in the decoder is not synchronized with code features from the credential. The decoder validates the internal structure of a code word by comparing successive 24-bit binary strings on a bit-by-bit basis. If the comparison fails, all bits are shifted one position, a new bit is introduced, and another comparison is attempted. The process is repeated as long as a credential is present, and if full comparison is not achieved, the code word is not transmitted to the Operations Center. This validation process gives rise to the possibility that one code word could have another code word imbedded within it but shifted over some number of bit positions. There are 96 pairs of such ambiguous code words (Appendix A) which leave a net of 16,192 available codes.

Physiological Effects

The possibility that the magnetic fields from the portal could be injurious caused Sandia to fund a study by the Illinois Institute of Technology Research Institute.[2] The first part of the study was to experimentally determine whether the portal would interfere with the normal operation of heart pacemakers. Eight pacemakers representing five different types from four manufacturers were used. The pacemakers were placed in a container filled with a fluid whose electrical properties had been adjusted to that of human tissue in the thoracic volume, and the pacemaker leads were arranged to simulate their placement in the body. The container was subjected to a variety of static and moving tests within the portal both with and without simulated cardiac waves, and the operation of two different types of pacemakers was altered. The portal field would have to be halved, approximately, to eliminate any possibility of interference. Consequently, it is recommended that persons wearing pacemakers be excluded from use of the SECS.

The second part of the study was a search through the literature of biological effects due to electromagnetic fields. The conclusion of the literature search is that the threshold for significant human biological effects due to brief repeated exposures to unmodulated magnetic fields near 100 kHz is probably in excess of 10^{-2} teslas. The maximum field density anywhere in the portal occurs adjacent to the portal frame and does not exceed 10^{-4} teslas. It appears that there is an adequate margin for safe use of the portal.

The next two sections of this report describe in detail the components associated with the portal and the credential, respectively.

Portal Components

Portal Loops

Two types of portal loops are used in the PPS, namely one walk-through loop and two wall-hung loops. The sizes of the loops were determined experimentally in order to operate the credential at a range of one meter.[3] Features of each portal are summarized in Table I below.

TABLE I

Portal Loop Description

Portal Type and Location	Loop Winding Dimensions, H x W x T (m)	Number of Turns	In-Situ Measured Parameters at 110 kHz		
			Inductance (mH)	Q	Peak Amperes
Walk-through in Vault Personnel Corridor	1.98 x 1.70 x 0.027	16	1.58	58	0.96
Wall Hung in Identification Booth	1.10 x 1.30 x 0.090	28	2.50	41	0.61
Wall Hung in MOC/MAC System Corridor	1.10 x 1.30 x 0.090	28	1.66	67	1.2

Analytical formulas have been derived to predict the field patterns near the loops (Appendix B), and measured field components were found to be in good agreement with predicted values for both types of portal loops.

110-kHz Driver

This unit is housed in an 8 x 4 x 8-inch cabinet and consists of three modules (Figure 3). The power supply module provides unfiltered ±30 volts to the rest of the circuitry. The control module begins with a 110-kHz Colpitts crystal oscillator, Q1, which is fine-tuned by C6. A sample of the output developed across the C10-L2 tank is fed to the source of a control FET, Q4. Unless a 5-volt level is applied to the gate of Q4 via J3, Q2, and Q3, the 110-kHz is fed to the level adjustment, R4, at the base of Q5. The collector of Q5 drives an emitter follower, Q5, in the driver module. The emitter follower is tuned by L5 to provide equal drive voltages to the complimentary output pairs, (Q1, Q2) and (Q3, Q4). The output, taken at J1, is sampled via R6-R7 to stabilize the emitter of Q5 in the control module. The value chosen for R8 in the control module is the value necessary to set zero volts upon pin 3 of J5/P5 when R4 is grounded. The output voltage and current are respectively monitored at J1 and J2.

Diplexer

The diplexer is the means by which the inductance of the portal loop is tuned to provide a resistive load to the driver; it also provides the initial tuning to separate the 55-kHz signal from the 110-kHz tone. The diplexer is mounted immediately adjacent to the portal loop, but may be connected to the filter/demodulator by up to 9 meters of RG 58/U coaxial cable. The portal loop inductance is series-resonated at 110 kHz by capacitors C1 through C6 (Figure 4). The capacitors have the same nominal value of six times the series-resonant capacitance of the loop. The separation of the 55-kHz signal begins by placing a 50-ohm load on the output port and adjusting L1 to block 110 kHz. The parallel tank consisting of L1 and the combination of (C7, C8) is placed at the junction of (C_2, C_3) to reduce the potential stress across L1. After the 50-ohm load is removed, L2 is adjusted to provide a shunt trap to ground.

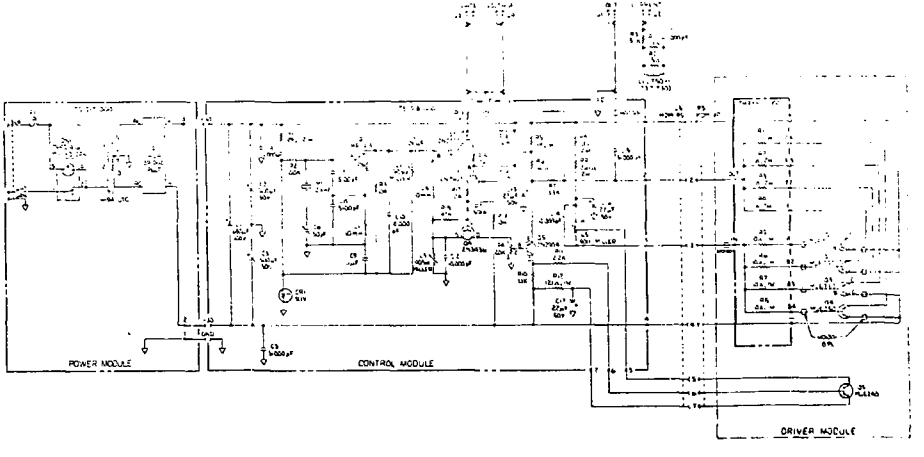

Figure 3. Schematic, Portal Loop Driver

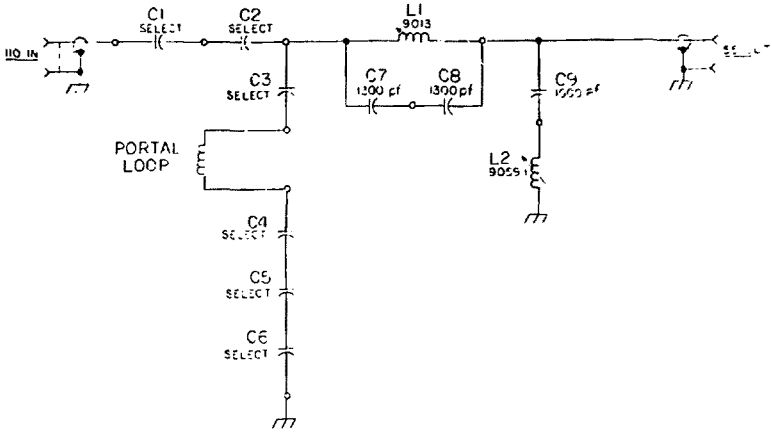

Figure 4. Schematic, Loop Diplexer

Electronic Credential Reader

This standard rack chassis, 5.25 x 19 x 19 inches, provides a common power supply to support the electronics necessary for decoding credential signals for as many as three portal diplexers. Two credential readers are used in the PPS. One reader is in the vault control room to service the portals in the vault personnel corridor and the identification booth, and the other reader is located in the MOC for the MOC/MAC portal. The credential signal from each portal is processed through a separate combination of filter/demodulator and decoder as explained below.

Filter/Demodulator

This circuitry (Figure 5) is located within a 3 x 2 x 4.5-inch shielded box at the rear of the credential reader. The circuits provide further separation of the 55-kHz signal with subsequent wave shaping to convert the burst code to a string of binary ones and zeros for use in the decoder.

The tuned circuits at the input are adjusted (Appendix C) to further isolate the 55-kHz signal and include the effects of the cable from the diplexer. The output of the 100X amplifier, AR1, is shunt-peaked by adjustment of L4 and evenly split along two paths at R6 and R7. The first two stages of AR2, and the low-pass filter which follows them, provide a level which is proportional to the mean of the peak of the positive signal envelope. The level is compared to the input signal in AR2-AR4 to eliminate noise bursts which may occur where binary zeros were intended in the code. At the same time, the 55-kHz signal is level-shifted so that it is no longer balanced around *zero but ranges from 0 to 5 volts. This signal is used to trigger the monostable multivibrator* in U1, and a third signal modification which occurs in AR2-4 must now be understood. A binary one, as transmitted from the credential, consists of 32 successive periods of a 55-kHz sinewave. The comparator action of AR2-4 converts this to a succession of 32 pulses with an individual pulse width of half the period of a 55-kHz sinewave. This would also be the output of U1, except that the combination of R21 and C11 provide a retrigger which does not allow the output of U1 to fall until after the 32nd pulse from AR2-4. This retrigger-feature is the means of converting a 55-kHz burst into a pulse of comparable width and provides the desired binary one. A nonzero output from U1 to the decoder is prohibited unless the mean positive signal level exceeds the threshold set by R14 at the input to AR2-3.

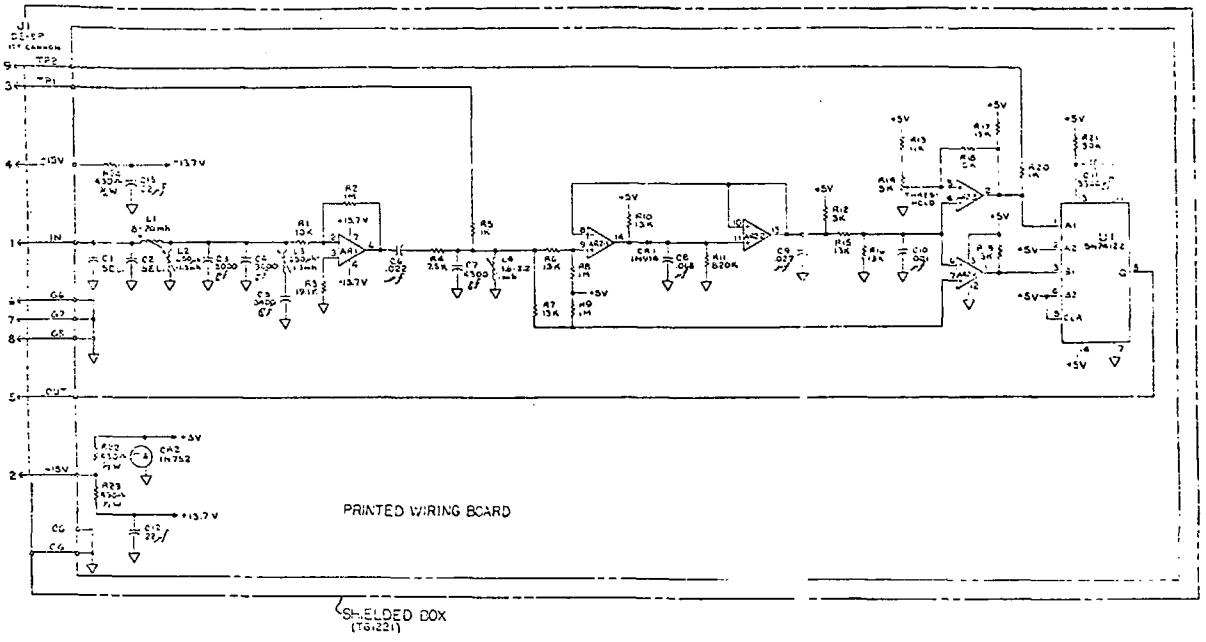

Figure 5. Schematic, Portal Filter/Demodulator

Decoder

The binary data stream and a 110-kHz tone from the loop sampler are the inputs to the decoder (Figure 6). The 110-kHz tone is divided by 64 to provide a reference clock of 1718.75 pulses per second which is the same as the credential bit rate and which is synchronized with the binary data stream. The data stream is admitted to a serial in-parallel out shift register (Register 1) under control of the clock. The serial output of Register 1 is clocked into Register 2, and after 48-bit periods, both registers may contain the same pattern of 24 bits. The 16 bits in each register which may represent the HD-code are parallel outputted to a comparator. The parities of bits 2 through 9 and bits 14 through 21 are computed, and unless both sets of HD-subwords have even parity the data valid signal from the error detector is inhibited. Simultaneously with this bit comparison and parity check process, the parallel 16-bit outputs from both registers are checked to see if fixed sync bits in Positions 2 and 14 are respectively 1 and 0. A sync bit error in either of the two words inhibits the data valid signal. The data valid signal is sent to the operations center only if both HD-code groups pass the sync checks and the parity check. The data valid signal also transfers the comparator output to a holding register to await a transmission request from the operations center. If the checking process is not successful, the process simply continues at the clock rate until either a data valid signal is generated or the credential is withdrawn. The minimum time required for checking is 48 bit periods or about 28 ms. However, the sync and parity bits may not be in their correct bit positions initially and 23 bit periods must be allowed to shift them from the most extreme wrong position. Another 24 bit periods must also be allowed for signal growth and decay as the credential moves through the portal, and the total time which should be allowed is 56 ms.

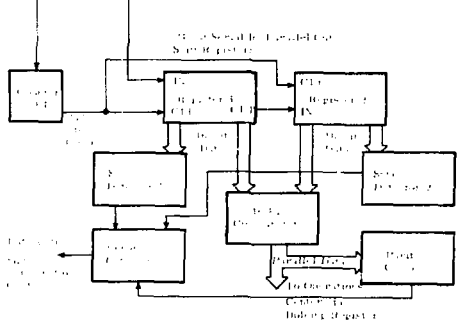

Figure 6. Block Diagram, Decoder

The operation of the credential electronics is discussed together with a description of its components. The credential measures 2.6 x 2.25 x 0.39 inches overall, weighs 1.2 ounces, and consists of three separate parts (Figure 7).

Housing and Loop

The credential housing consists of two parts, a housing and a cover (Figure 8). The 7-turn loop is wound in a channel on the edge of the housing. The inductance typically measures 620 μH over the frequency range from 55 to 110 kHz, but increases slightly to a typical value of 633 μH when the printed circuit board is placed within the housing. The loop resistance varies from 7.3 ohms to 13.1 ohms over the frequency range when the circuit board is in place. This resistance variation is included in the design process for the credential diplexer (Appendix D).

Circuit Board

All of the electronics are mounted on one side of a printed circuit board which is glued into the housing after being connected to the loop. The operation of electronics may be understood from the schematic (Figure 9) beginning with the 110-kHz voltage induced in the loop. This voltage is rectified by CR2, limited to 12 volts if necessary by CR1, and filtered by C3 to provide a potential to the zero CMOS units on the board. The 110-kHz voltage is divided by (C1, C2) and buffered by U3-1 to U2 where it is divided by two. The 55-kHz tone is sent to one input of a NAND-gate, U4-1. When a binary one is generated, by the digital multiplexer U1, a burst of 32 cycles of the 55-kHz is passed via U3-6 and a matching network to the loop for transmission to the portal.

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Figure 7. Electronic Credential

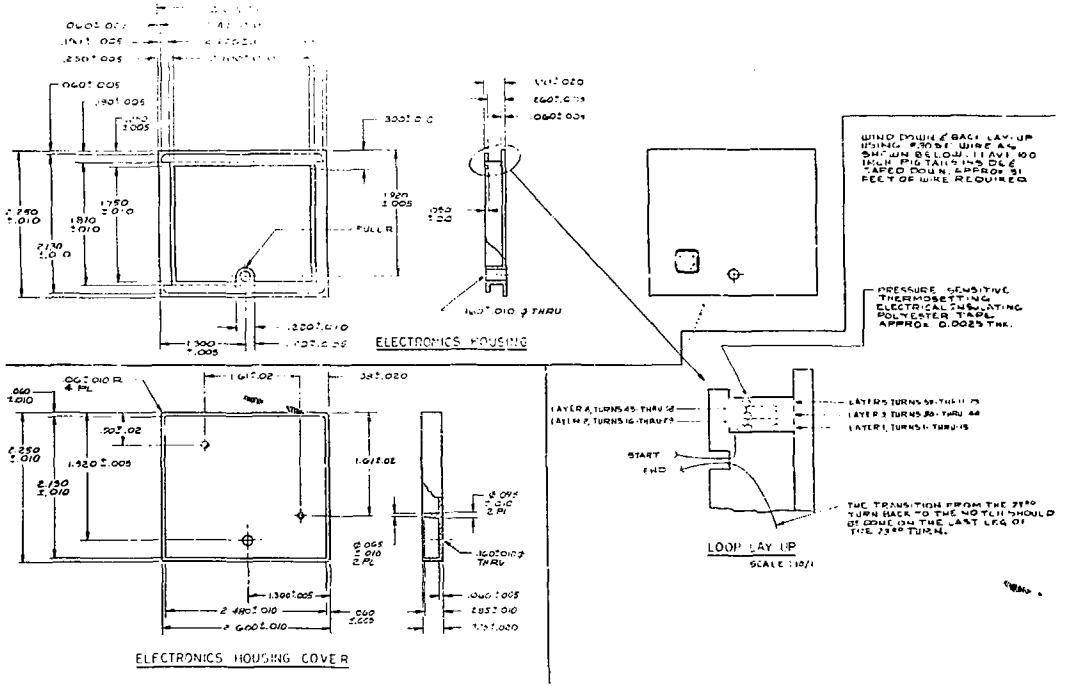

Figure 8. Electronic Credential Housing

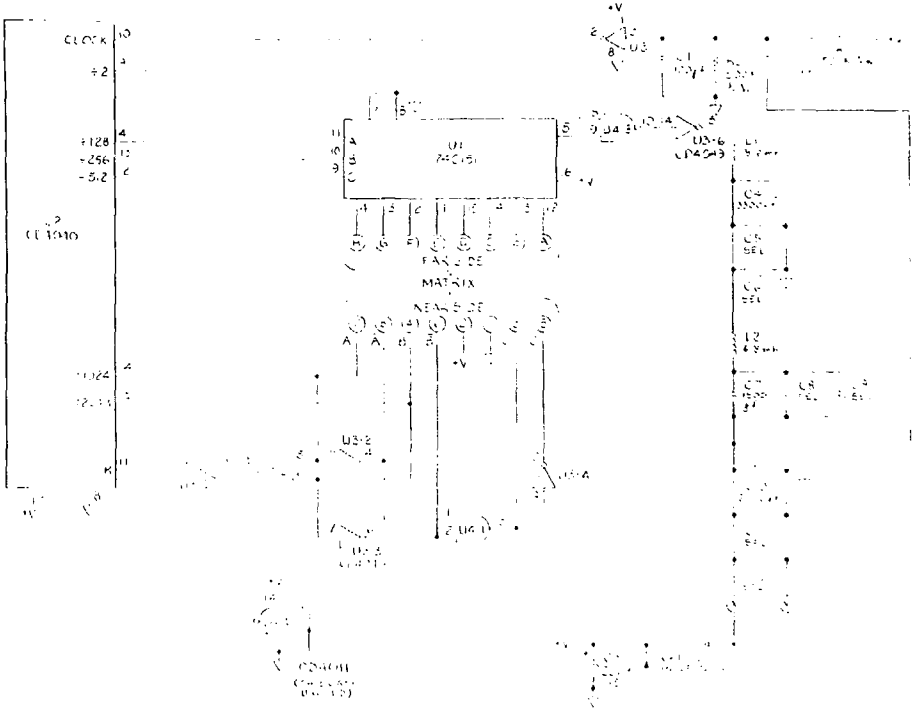

Figure 9. Schematic, Self-Centered Credential

Code Storage and Generation

The credential code is stored by connections within an 8 x 8 matrix (Appendix I.1). The code is generated from the matrix by the combination of the digital multiplexer, U1, and the 12-stage counter, U2. The successive data-select lines of U1 are controlled by dividing the 110-kHz tone by 128, 256, and 512 respectively. The complimentary logic within U1 causes the data input lines to be successively selected at a rate of 110 kHz divided by 64, and thus establish the credential bit rate as 1718.75 bits per second. Each of the eight data inputs to U1 is connected to a lettered column of the matrix, and the rows of the matrix are activated by coding signals from U2. In each column there are eight possible signals available, depending on which row is selected in that column. Code storage consists of making one solder connection from each column to a particular row on that column.

The coding signals upon the matrix rows are generated from the 10th and 11th stages of U2 together with two fixed signals. Row 1 is always tied to ground (zero), and Row 2 is always tied to -V (one). The output of the 10th stage of U2 is called Code Word A and changes every 8-bit counts. Code Word A may be represented, in units of 8-bit counts, as 010. Similarly, Code Word B is the output of the 11th stage of U2 and represented as 001. Clearly, it is necessary to reset U2 every 24 bits or Code Word B would appear as a one at the start of the second credential code. The Code Word C is generated by logically OR-ing A and B as shown on the schematic, Figure 9. The following tabulation illustrates the digital representation associated with each code word.

8-Bit Interval Number	Code Word and Matrix Row Number							
	Gnd(1)	-V(2)	A(7)	$\overline{A}$(8)	$\overline{B}$(4)	B(3)	C(3)	$\overline{C}$(5)
1	0	1	[illegible]	1	1	0	[illegible]	1
2	0	1	1	0	1	0	1	0
3	0	1	0	1	0	1	1	0

References

1. R. B. Cramer and W. L. Garner, Plutonium Protection System, Sandia Technology, SAND77-1750, Sandia Laboratories, Albuquerque, NM, September 1977.

2. IIT Research Institute, A Study of the Possible Effects of 110 kHz Electromagnetic Fields on Humans, SAND77-7028, Sandia Laboratories, Albuquerque, NM, September 1977.

3. D. E. Barnes et al, Self-Energized Credential System, Sandia Laboratories, Albuquerque, NM, SAND76-0540, December 1976.

APPENDIX A

Ambiguous Codes

The 192 ambiguous hexadecimal codes are listed below in ascending order.

8C1D	B074	CC0D	F034
C2D	075	C3D	035
C4D	076	C5D	036
C7D	077	C6D	037
D1C	175	D0C	134
D2C	175	D3C	135
D4C	176	D5C	136
BD7C	177	CD6C	137
	274		234
98AA	275	D81A	235
83B	276	81B	236
85A	277	87A	237
85P	374	87B	334
92A	375	91A	335
92B	376	91B	336
95A	377	97A	337
95B	470	97B	430
A38	471	C1B	431
A39	472	A19	432
A56	473	A78	433
A59	570	A79	530
B38	571	B18	531
B39	572	B1c	532
B58	573	B78	533
B59	570	B79	630
CC0D	671	C1D	631
C3D	672	C2D	632
C5D	673	C4D	633
C6D	770	C7D	730
D0C	771	D1C	731
D3C	772	D2C	732
D5C	773	D4C	733
4D6C	81A	DD7C	83A
	83B		83B
ACCD	87A	EC1D	85A
C3D	87B	C2D	85B
C5D	91A	C4D	93A
C6D	91B	C7D	93B
D0C	97A	D1C	95A
D3C	97B	D2C	95B
D5C	A18	D4C	A38
AD6C	A19	ED7C	A39
	A78		A58
	A79		A59
	B18		B38
	B19		B39
	B78		B58
	B79		B59
	C1D		COD
	C2D		C3D
	C4D		C5D
	C7D		C6D
	D1C		D0C
	D2C		D3C
	D4C		D5C
	BD7C		FD6C

APPENDIX B

Formulas for Induced Voltage

The components of the magnetic density vector generated by a rectangular loop are derived from the vector potential of a finite current element, and are used to compute the voltage induced in a nearby loop.

Vector Potential

The vector potential is derived for a finite current element in a form which is amenable for computation except at the ends of the element where the potential becomes unbounded.

Consider a conductor of infinitesimal cross section which is carrying a uniform current $i(t) = I\exp(-j\omega t)$. The conductor lies in the yz-plane and extends from $z' = -b$ to $z' = b$ along $y' = a$ (Figure B1). It is assumed that the current undergoes negligible phase shift along the element, that is, $4\pi b/\lambda \ll 1$, where λ is the wavelength. The retarded vector potential at the field point, $P(x, y, z)$, has a component only in the z-direction parallel to the current source. This component is given by the integral,

$$A_z = \frac{\mu I}{4\pi}\int_{-b}^{b}\frac{\exp\left[-j\omega(t - R/c)\right]}{R}\,dz' \quad \text{webers/meter.} \tag{B1}$$

The geometry requires that A_z have the same value at points symmetrically located on either side of the xy-plane. In Eq (B1), μ is the permeability of free space, ω is the angular frequency, c is the velocity of light, the prime denotes source coordinates, and R is the spherical radius from the source to the field-point,

$$R = \left\{\rho^2 + (z - z')^2\right\}^{1/2} \quad \text{meters} \tag{B2}$$

where

$$\rho^2 = x^2 + (y - y')^2 \quad \text{meters.} \tag{B3}$$

When R/c is very small, as in the present case where R is a meter or less, the retarded contribution is negligible and

$$A_z = \frac{\mu I}{4\pi}\,e^{-j\omega t}\int_{-b}^{b}\frac{dz'}{R} = \frac{\mu I}{4\pi}\ln\left\{\frac{z + b + \left[\rho^2 + (z - b)^2\right]^{1/2}}{z - b + \left[\rho^2 + (z - b)^2\right]^{1/2}}\right\}e^{-j\omega t} \quad \text{W/m}. \tag{B4}$$

It is not obvious that Eq (B4) is symmetrical about $z = 0$, but symmetry can be shown as follows. Substitute $-z$ throughout Eq (B4) and equate the argument to that of Eq (B4), cross multiply, simplify, and an identity will appear.

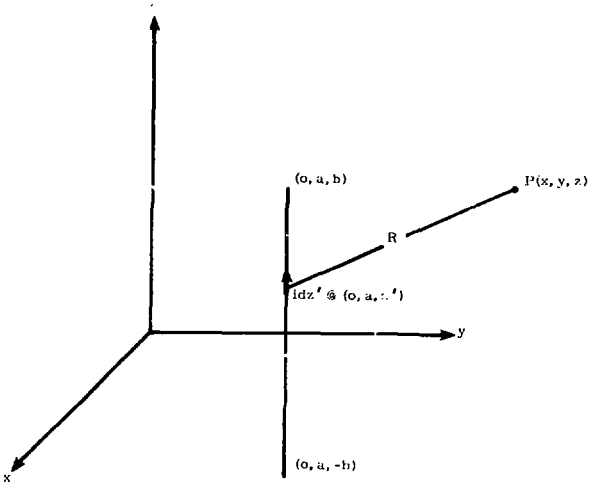

Figure B1. Geometry of Current Element and Field Point

When $\rho = 0$ the definition of R gives

$$R\Big|_{\rho=0} = |z - z'| \tag{B5}$$

and the vector potential becomes

$$A_z\Big|_{\rho=0} = \frac{\mu I}{4\pi} \ln \left\{ \frac{z - b}{|z - b|} \right\} \tag{B6}$$

and

$$\lim_{|z| \to 0} A_z \Big|_{\rho=0} = 0 \ . \tag{B7}$$

These results show that $A_z \geq 0$ everywhere but becomes unbounded at the ends of the current element where $\rho = 0$, and $|z| = b$.

The total vector potential from a rectangular loop is the sum of the potentials due to the four current elements which form the loop. Consider a loop of height 2h and width 2w (Figure B2), and let r_i denote the spherical radius from the i^{th} corner of the loop to the field point, namely,

$$r_1 = \left\{x^2 + (y + w)^2 + (z - h)^2\right\}^{1/2}, \quad r_2 = \left\{x^2 + (y + w)^2 + (z + h)^2\right\}^{1/2}$$

$$r_3 = \left\{x^2 + (y - w)^2 + (z + h)^2\right\}^{1/2}, \quad r_4 = \left\{x^2 + (y - w)^2 + (z - h)^2\right\}^{1/2} \quad \text{meter} \qquad \text{(B8)}$$

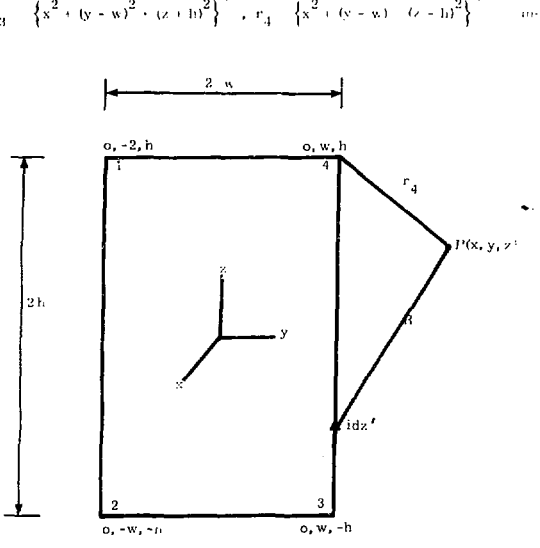

Figure B2. Geometry of Rectangular Loop and Field Point

In Eq (B8), substitute

$$y_1 = y_2 = y + w, \; y_3 = y_4 = y - w$$

$$z_1 = z_4 = z - h, \; z_2 = z_3 = z + h \qquad \text{(B9)}$$

to obtain the general form for the corner spherical radius:

$$r_i = \left\{x^2 + y_i^2 + z_i^2\right\}^{1/2}, \; i = 1, 2, 3, 4. \qquad \text{(B10)}$$

The components of the vector potential can now be written compactly by using Eq (B4) and omitting the time dependence exp (-jωt).

$$A_y = \frac{\mu I}{4\pi}\left\{\ln(r_2 + y_2) + \ln(r_4 + y_4) - \ln(r_1 + y_1) - \ln(r_3 + y_3)\right\} \tag{B11}$$

$$A_z = \frac{\mu I}{4\pi}\left\{\ln(r_2 + z_2) + \ln(r_4 + z_4) - \ln(r_1 + z_1) - \ln(r_3 + z_3)\right\} \quad . \tag{B12}$$

Components of Magnetic Density

The magnetic density vector is derived from the vector potential according to

$$\vec{B} = \text{curl}\,\vec{A} \qquad \text{teslas} \; . \tag{B13}$$

The components can be written in these compact forms:

$$B_x = \frac{\mu I}{4\pi}\sum_{n=1}^{4}\frac{(-1)^n}{r_n}\left\{\frac{y_n}{r_n + z_n} - \frac{z_n}{r_n + y_n}\right\} \quad , \tag{B14}$$

$$B_y = \frac{\mu Ix}{4\pi}\sum_{n=1}^{4}(-1)^{n+1}\Big/\left\{r_n(r_n + z_n)\right\} \; , \tag{B15}$$

$$B_z = \frac{\mu Ix}{4\pi}\sum_{n=1}^{4}(-1)^{n}\Big/\left\{r_n(r_n + y_n)\right\} \qquad \text{teslas.} \tag{B16}$$

Induced Voltage

Because the B-field components may vary in magnitude over the dimensions of even the smaller loop, it is necessary to compute the induced voltage as the time derivative of the average B-field normal to the plane of the loop which is being induced. Let the components of the unit vector normal to the surface of the induced loop be denoted by (u_x, u_y, u_z), and let "S" be the area per turn of the N-turn loop. The induced voltage is given by

$$V = \frac{\mu\omega NIS}{4\pi M}\sum_{m=1}^{M}\left\{u_x B_x + u_y B_y + u_z B_z\right\}_m \qquad \text{volts,} \tag{B17}$$

where M-sets of field points are chosen within the area of the loop. The use of M = 400 for the credential loop and M = 10,000 for the portal loop, the points being equally spaced in each case, has been sufficient to provide uncertainties of less than c ~ percent.

APPENDIX C

Filter/Demodulator Tuning Procedure

1. Connect the cable from the diplexer to the filter/demodulator, and a decade capacitor set to 2000 pF in the position C1, C2 (Figure 5).
2. Move the adjustment for each inductor, L1 through L4, near the center of its range.
3. With an oscilloscope at TP-1, adjust L3 to maximize the 110-kHz tone.
4. Place a credential near the portal so that AR1 is not overloaded and adjust the decade capacitor to maximize the 55-kHz signal. Remove the decade and replace it with C1 C2 one-half the decade value.
5. Adjust L2 to further increase the 55-kHz signal.
6. Adjust L4 to further increase the 55-kHz signal.
7. Use a delayed trigger on the oscilloscope, arrange to examine a 101 or 010 transition. Adjust L1 to provide minimum fall time consistent with acceptable decrease in the 55-kHz level.
8. Readjust L3 to improve rise and fall times if possible.

This alignment procedure will be required again if either the cable length, portal loop, portal diplexer, or filter/demodulator are changed.

APPENDIX D

Design of Coupling Diplexer

The design problem is to provide a few milliamperes of current at 76 kHz to a loop whose receiver is powered with several volts at 110 kHz. Part of the coupling scheme that we considered is shown in Figure D1 for convenient reference. The equivalent capacitance C_c is shunt-resonated with the loop to increase the 110-kHz potential with which to power the electronics. The circuit to the right of the loop is treated as follows: the branch via CR2 is replaced by R_{DC} = 10 kilohms, and the branch via C2 is replaced by an open circuit. The series equivalent at 76 kHz of the load combination of C_c, the loop, and R_{DC} is the load for the network to be designed.

$$Z_{LOAD} = Z_L = R_L + jX_L = C_c \left\| \left[R_{LOOP} + jX_{LOOP} \right] \right\| R_{DC} \quad . \tag{D2}$$

On the other side of the network, the network should present an input resistance,

$$Z_i = 5000 + jX_i \quad , \quad 0 < X_i < 5000 \Omega \quad . \tag{D3}$$

This value of Z_i requires only a modest current from CR5-6 and avoids a capacitive load. An L-section network is used to transform Z_L; its properties are reviewed below as we use it explained.

Consider the L-network placed between complex source and load impedances, $Z_S = R_S + jX_S$ and $Z_L = R_L + jX_L$ (Figure D2). The network presents to both the source and load impedances their respective conjugate impedances given by

$$Z_S = \frac{Z_1 (Z_2 + Z_L)}{Z_1 + Z_2 + Z_L} \quad , \text{ and } Z_L = Z_2 + \frac{Z_1 Z_S}{Z_1 + Z_S} \quad . \tag{D3}$$

Under the conditions that $R_S > R_L$ the network impedances found from these formulas are:

$$Z_1 = j \left\{ \frac{R_L X_S}{R_S - R_L} + \sqrt{\left(\frac{R_L X_S}{R_S - R_L} \right)^2 + \frac{R_L |Z_S|^2}{R_S - R_L}} \right\} \quad , \tag{D4}$$

and

$$Z_2 = j \left\{ -X_L \pm \sqrt{\frac{R_L |Z_S|^2}{R_S} - R_L^2} \right\} \quad . \tag{D5}$$

Both Z_1 and Z_2 are entirely imaginary, and it appears that there are four sets of (Z_1, Z_2) due to the sign choice before each radical. But Z_1 and Z_2 must have unlike signs in order for Eq (D5) to hold.

The design procedure is part of a badge design computer program listed in Appendix E and is summarized as follows:

1. Compute the total shunt capacitance $C_c = C_{10} + C_{11} + C_{12}$ necessary to resonate the loop inductance at 110 kHz.

2. Compute the series equivalent impedance at 55 kHz of the shunt combination of C_c, the loop, and $R_{DC} = 10,000$ ohms.

3. Take $Z_{source} = Z_s = 5000 + j2\pi (55,000) L_1$ where $L_1 = 6.8$ mH from the credential schematic. Solve for X_1 and X_2 from Eqs (D4, D5), using a choice of signs to make X_1 capacitive and X_2 inductive. Solve for $C_a = C_4 + C_5 + C_6$ from X_1. The required value of L_2 from X_2 is so small that it is realized by using a 8.2-mH inductor and series tuning it by the proper combination of $C_b = C_7 + C_8 + C_9$.

4. Replace U3-6 in Figure D1 by its output resistance of 330 ohms. Compute, at 110 kHz, the total impedance shunting C_c and recompute C_c to resonate the impedance.

5. Return to Step 2 and repeat three more times which is sufficient to provide values of C_a, C_b, and C_c stable to 10^{-4}.

6. Deduct 150 pF from C_c to adjust for the neglected branch via C_2 and stray shunt capacitance. A typical value of input impedance presented to U3-6 is $Z_1 = 5000 + j 1200$ ohms as required by Eq (D2). The results of the design procedure, C_a, C_b, and C_c, are not significantly changed as $5000 < R_{DC} < 20,000$ ohms or $300 <$ (output resistance of U3-6) < 2000 ohms. The badge design program is extensively annotated and includes the effects of inductor resistance variation with frequency.

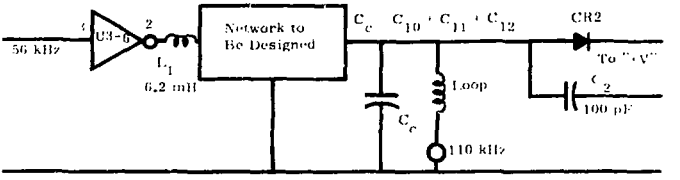

Figure D1. Partial Credential Schematic

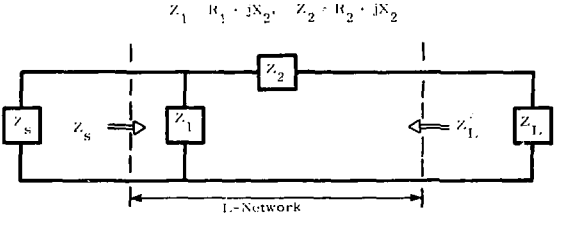

Figure D2. L-Network and Terminations

APPENDIX E

Code Storage on the Credential

The code is stored on the credential in an 8 x 8 matrix formed by nonplated-through holes at the intersection of eight horizontal conductors on the component side of the credential and eight vertical conductors on the rear side. The horizontal conductors or rows are numbered from top to bottom of the matrix and are connected to the coding signals discussed in the text in the following manner:

Coding Signal	Matrix Row No.
$\overline{A}$	8
A	7
$\overline{B}$	6
$\overline{C}$	5
B	4
C	3
+V	2
GND	1

The vertical conductors or columns are lettered H to A, from left to right, and are connected to the inputs of the digital multiplexer U1 as shown below.

Multiplexer Input	Matrix Column Letter
1	H
2	G
3	F
4	E
5	D
6	C
7	B
8	A

A coding signal is connected to a multiplexer input by soldering a through-wire to both sides of the appropriate matrix intersection. For example, to connect $\overline{B}$ to Input 5 requires that Row 6 be connected to Column D. A means must be provided, prior to soldering, for representation of the HD-code in terms of the various coding signals. This process will be explained with the use of a coding worksheet and an example.

The first step in the coding process is to write the HD-code in binary form consisting of 24 bits as explained in the text. The binary HD-code is organized into three groups of eight bits each corresponding to both the multiplexer inputs and to the three rows of a wire code table (Figure E1). Certain bits which are fixed are already filled in on the worksheet. As an example consider the HD-code in the text, AA55, and fill in Step 1 of Figure E2. Step 2 consists of entering a binary one or zero into the wire code table according to the column content in Step 1. The wire code is read by column, from the top down, converted to a matrix row number in Step 3, and the row number is listed for each column in Step 4.

Copies of the blank worksheet may be used for coding a small number of credentials. The entire coding process is included in a computer program, BDIPDES, which is part of the drawing set (Appendix F).

HID Code _____ Alpha or _____ Numeric

Step 1: Binary Representation — Even Parity

Bit Position	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24
Binary Code	0	1									1	1	0	0									1	1
Column Letter	H	G	F	E	D	C	B	A	H	G	F	E	D	C	B	A	H	G	F	E	D	C	B	A
	Row 1								Row 2								Row 3							

Step 2: Put Binary Code into Wire Code Table Below

	H	G	F	E	D	C	B	A
1	0	1						
2			1	1	0	0		
3							1	1

Step 3: Convert Wire Code to Matrix Row Number

Coding Signal	Wire Code	Matrix Row
GND	0 0 0	1
B	0 0 1	4
A	0 1 0	7
C	0 1 1	3
$\overline{C}$	1 0 0	5
$\overline{A}$	1 0 1	8
$\overline{B}$	1 1 0	6
-V	1 1 1	2

Step 4: Connect Column to Row in Credential Matrix

Column Letter	H	G	F	E	D	C	B	A
Row Number								

Figure E1. Credential Code Worksheet, Blank

HID Code AA55 (Alpha) or 10 10 5 5 (Numeric)

Step 1: Binary Representation

Even Parity

Bit Position	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24
Binary Code	0	1	**0**	**1**	**0**	**1**	**0**	**1**	**0**	**0**	1	1	0	0	**1**	**0**	**1**	**0**	**1**	**0**	**1**	**0**	1	1
Column Letter	H	G	F	E	D	C	B	A	H	G	F	E	D	C	B	A	H	G	F	E	D	C	B	A
	Row 1								Row 2								Row 3							

Step 2: Put Binary Code into Wire Code Table Below

1	0	1	**0**	**1**	**0**	**1**	**0**	**1**
2	**0**	**0**	1	1	0	0	**1**	**0**
3	**1**	**0**	**1**	**0**	**1**	**0**	1	1
	H	G	F	E	D	C	B	A

Step 3: Convert Wire Code to Matrix Row Number

Coding Signal	Wire Code	Matrix Row
GND	0 0 0	1
B	0 0 1	4
A	0 1 0	7
C	0 1 1	3

Coding Signal	Wire Code	Matrix Row
$\overline{C}$	1 0 0	5
$\overline{A}$	1 0 1	8
$\overline{B}$	1 1 0	6
+V	1 1 1	2

Step 4: Connect Column to Row in Credential Matrix

Column Letter	H	G	F	E	D	C	B	A
Row Number	**4**	**5**	**3**	**6**	**4**	**5**	**3**	**8**

Figure E2. Credential Code Worksheet with Example

APPENDIX F

List of Drawings

Drawing Number - Issue	Title
T44523-D	Loop-Diplexer
T44524-B	Schematic, Loop Diplexer
CK-T48659-C	Self-Energized Credential Schematic
T48659-C	Self-Energized Credential PWB
DD-T48659-A01C	Self-Energized Credential PWB, Front Side Master
DD-T48659-H01-C	Self-Energized Credential PWB, Rear Side Master
SS-T48659-B	Program BDIPDES
T49350-B	Loop Driver, Pwr Amp Vector Board
T49351-B	Assembly, Loop Driver
CK-T49351-B	Schematic, Portal Loop Driver
T51011-A	Bracket, Capacitor
T51012-A	Bracket, Coil
T51013-A	Power Supply Mounting Bracket
T51014-A	Power Transistor Mounting Cover
T51015-A	Front Panel
T51016-A	Transformer Mounting Bracket
T51017-B	Power Supply, Loop Driver
T51018-B	Printed Wiring Assembly, Loop Driver
T55409-A	Electronic Credential Housing
CE-T57241-A	Logic Diagram, Electronic Credential Reader
T58627-A	Schematic, Portal Filter/Demodulator
T58658-B	Assembly, Credential
T61221-A	Filter/Demodulator Box
T61222-A	Filter/Demodulator Assembly
T61230-A	Loop Sampler

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