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RADIATION DAMAGE TESTING OF TRANSISTORS FOR SSC FRONT-END ELECTRONICS

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Abstract

Over the ten year expected lifetime of a typical SSC detector operating at the design luminosity of 10^{33} cm^{-2}s^{-1}, the front-end electronics at large pseudorapidities may receive total doses as high as 20 MRad(Si) of ionizing radiation and 10^{16} neutrons/cm^2. Discrete JFETs and monolithic MOS and bipolar transistors have been irradiated at 10 MRad(Si) and 10^{14} neutrons/cm^2, and the effect on transfer characteristics and noise performance have been measured. All transistors were still functional after irradiation but suffered increased noise and the MOS transistors showed significant threshold shifts and increased leakage currents.

Introduction

At a luminosity of 10^{33} cm^{-2}s^{-1} the radiation doses inside a SSC detector may reach 20 MRad(Si) of ionizing radiation and 10^{16} neutrons/cm^2 over the ten year lifetime of the detector. The dose is strongly dependent on the geometry of the detector and the exact location of the electronics [1]. Any upgrades of the machine from the design luminosity will further increase the radiation levels inside the detector.

Over the last 30 years, the effects of radiation damage have been researched by the military and space-scientists, as well as in the high-energy physics community, and a large body of knowledge has been acquired [2,3]. This can be taken as the point of departure for the study of the specific SSC environment. Several industrial vendors have also developed the capability of manufacturing radiation-hardened devices, so the technological know-how for fabrication of SSC front-end electronics already exists.

The specific requirements of the SSC radiation environment, *i.e.* low dose rate but high total dose, are different from the military and space-science applications. This indicates that extensive study of avaliable fabrication processes must be made in order to evaluate their applicability for the SSC. General properties of radiation damage, such as the effect of low-temperature operation and short and long term annealing must also be investigated.

Argonne National Laboratory has several facilities that are well suited for radiation damage research. These facilities include a fast neutron generator, several cobalt-60 sources that can deliver up to 2 MRad(Si) per hour, and a 22-MeV electron linac. The facilities available for radiation damage research and testing are extensively described in [4].

At the Argonne radiation facilities the dose rates can be quite high, allowing the life-time dose at the SSC detector, *i.e.* the full ten years of operation, to be received during 4–8 hours of irradiation. This makes it easy to perform experiments which demands high total dose, but introduces dose rate effects that are difficult to predict. We do not make any attempt to take dose rate effects into account in this paper.

Measurements

Test samples of JFETs, bipolar, and MOS transistors were obtained from several manufacturers. The JFETs were commerciallly available discrete components, while the bipolar and MOS transistors were from custom rad-hard monolithic CMOS and BiCMOS processes. Both n- and p-channel devices were tested.

JFETs were irradiated with ionizing radiation at a total dose of 1 MRad(Si) and 12 MRad(Si) and neutrons at doses between 10^{13} and 10^{15} neutrons/cm^2. The transistors were biased at I_D = 1 mA and V_{GS} = 5 V, and irradiations were done both at room temperature and at liquid nitrogen

temperatues (120 K). DC characteristics, as well as small signal parameters and noise performance, were measured approximately one week after exposure to allow for all annealing effects to take place.

The monolithic MOS and bipolar transistors were biased at I_D (or I_C) = 100 μA and V_{GS} (or V_{CE}) = 5 V. Total doses received by the integrated devices were $\sim 10^{14}$ neutrons/cm^2 and 1 MRad(Si) to 10 MRad(Si). All irradiation and mesurements were done at room temperature.

Noise performance and forward β for the bipolar transistors, and g_m, noise characteristics, I-V curves (I_D vs. V_{GS} and V_{DS}), and V_{th} was measured for the MOS transistors.

Results

The results of radiation damage testing for JFETs have been extensively covered in [4]. The main findings included an increase in equivalent noise charge of 25 percent at 100 ns shaping time, and an increase in gate leakage current of one order of magnitude after 10^{14} neutrons/cm^2. The equivalent noise charge increased by less than 20 percent for 100 ns shaping time after 12 MRad(Si) of γ-rays.

Bipolar monolithic transistors suffered a reduction in forward β of between 15 and 25 percent, but still remained above 75 for both npn and pnp transistors for a dose of 10^{14} neutrons/cm^2. The $1/f$ noise increased by a factor of 4, but will have a very small effect at the frequency range of interest. 10 MRad(Si) of ionizing radiation caused the β to be reduced by 30–40 percent, bringing the pnp β down to approximately 50, while the npn β stayed above 75 (see Fig. 1). Ionizing radiation had a negligble effect on the equivalent input noise of the bipolar devices. Both the pnp and the npn transistors were still fully functional after irradiation and the decrease of β can be taken into account in the design process.

Radiation damage in MOS transistors is caused mainly by ionizing radiation that shifts the threshold voltages more negative, thus making the n-channel $|V_{th}|$ smaller and the p-channel $|V_{th}|$ larger. This is due to the build up of charge Q_{ss} in the gate oxide, which influences the threshold voltage according to

$$V_{th} = \Phi_{ms} + 2\Phi_f + \frac{Q_b}{C_{ox}} - \frac{Q_{ss}}{C_{ox}}.$$

The shift in V_{th} is up to 700 mV for 10 MRad(Si) of γ-rays for both n-channel and p-channel devices. An example of the threshold shift can be seen in Fig. 2. The same dose also causes the g_m to decrease by approximately a factor of 2 and increases the noise of both the n- and p-channel devices by a factor of 5.

A neutron dose of 4×10^{14} neutrons/cm^2 causes a threshold shift of $\sim$ 200 mV. The same dose leaves g_m and the noise of the n-channel transistors unchanged, while the noise of the p-channel transistors increased by a factor of two.

Conclusions

Radation damage testing has been done on discrete JFETs and monolithic bipolar and MOS transitors to evaluate their suitability for SSC front-end electronics. The transistors were exposed to total doses of up to 12 MRad(Si) of ionizing radiation and 10^{14} neutrons/cm^2. All transistors were found functional after irradiation.

JFETs are intrinsically the most radiation-hard devices and the samples tested were from a non rad hard commercial process. They suffered little or no degradation in DC characteristics and small-signal behavior, but noise increased between 20 and 25 percent.

The bipolar and MOS transistors were acquired from vendors with rad-hard CMOS and BiCMOS processes. Forward β of the bipolar devices decreased but remained over 75 for both neutron radiation and ionizing radiation, and noise performance was not affected. The MOS transistors suffered shifts in V_{th} of up to 700 mV, increased noise and decreased g_m.

Acknowledgements

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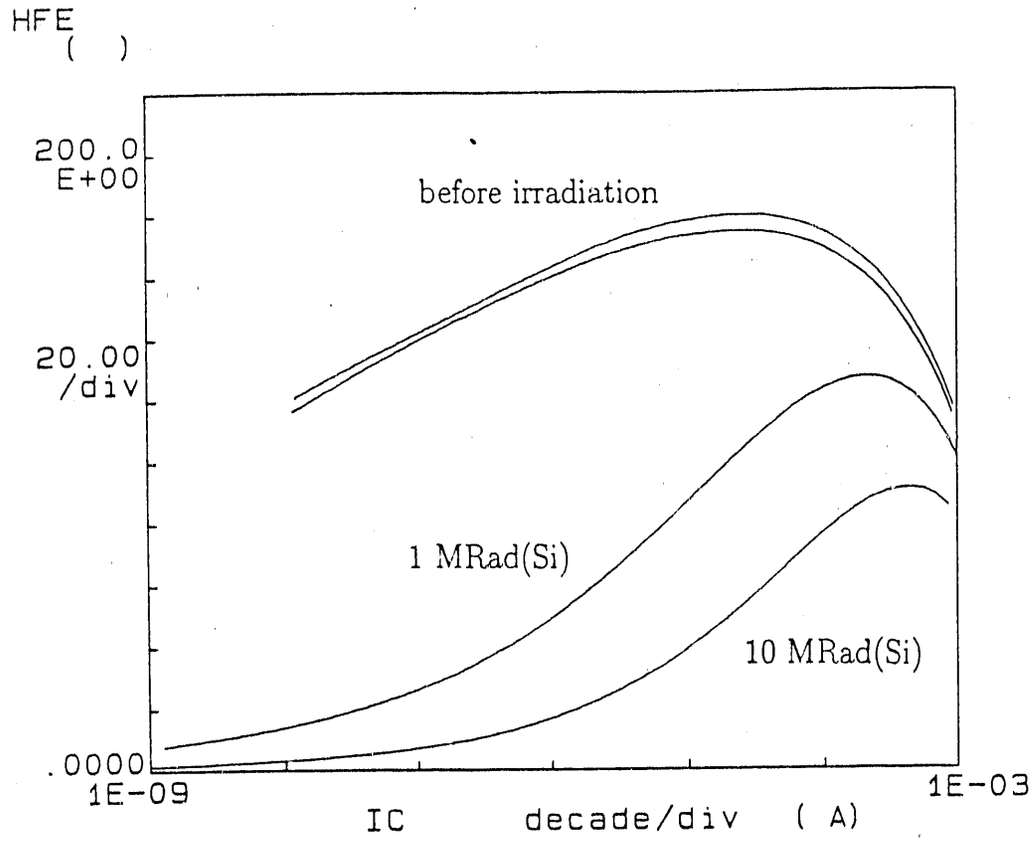

Figure 1: Forward β of npn bipolar transistor from Hughes' CBIT process (a 1.4 μm feature size BiCMOS process) before irradiation and after 1 MRad(Si) and 10 MRad(Si) of ionizing radiation.

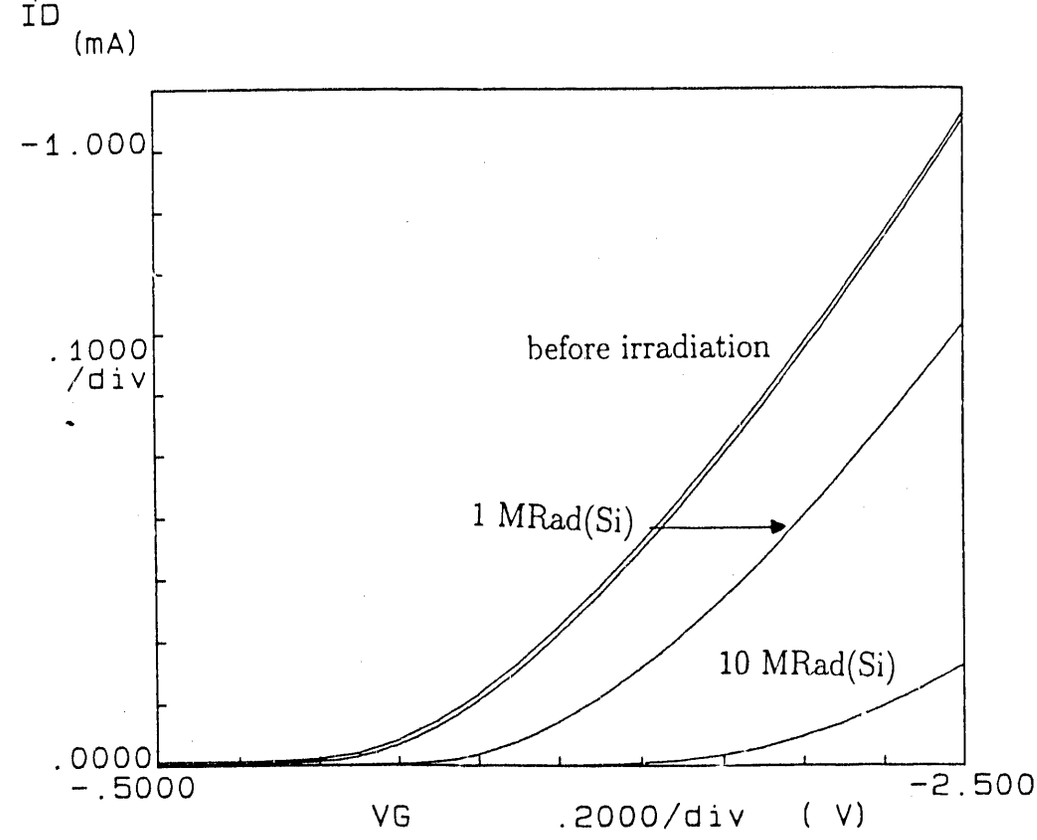

Figure 2: V_{th} of an p-channel MOS transistor from Hughes' CBIT process before irradiation and after 1 MRad(Si) and 10 MRad(Si) of ionizing radiation.

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