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## GaAs-BASED JFET AND PHEMT TECHNOLOGIES FOR ULTRA-LOW-POWER MICROWAVE CIRCUITS OPERATING AT FREQUENCIES UP TO 2.4 GHz

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In this work we report results of narrowband amplifiers designed for milliwatt and submilliwatt power consumption using JFET and PHEMT GaAs-based technologies. Enhancement-mode JFETs were used to design both a hybrid amplifier with off-chip matching as well as a MMIC with on-chip matching. The hybrid amplifier achieved 8-10 dB of gain at 2.4 GHz and 1 mW. The MMIC achieved 10 dB of gain at 2.4 GHz and 2 mW. Submilliwatt circuits were also explored by using 0.25  $\mu\text{m}$  PHEMTs. 25  $\mu\text{W}$  power levels were achieved with 5 dB of gain for a 215 MHz hybrid amplifier. These results significantly reduce power consumption levels achievable with the JFETs or prior MESFET, HFET, or Si bipolar results from other laboratories.

### INTRODUCTION

Low power circuitry is very important for battery powered electronic components. Low power operation of digital circuitry is often taken for granted due to the unique advantages offered by CMOS architecture. On the other hand, microwave circuits have no equivalent low power circuit configuration and require quiescent bias. For receiver applications, low power operation depends on the ability of a device to have adequate gain at low bias and low current levels. This in turn favors high performance GaAs devices for which gain can be adequate under current starved conditions.

Several reports of low power monolithic amplifier technology have been made, all close to the 1 mW level and at 1 GHz or below [1-3]. Commercial GaAs MESFET foundry technology was used to design and fabricate an amplifier with 15 dB of gain for 2-stages with 0.8 mW power at 1.25 GHz [1]. An HFET (heterostructure field effect transistor) amplifier MMIC (monolithic microwave integrated circuit) achieved 10 dB of gain at 0.5 mW and 900 MHz [2]. A Si bipolar amplifier IC was reported to operate at 0.5 mW and 150 MHz with 20 dB gain [3].

We have previously reported a 2.4 GHz amplifier with 10 dB of gain at 1.0 mW bias using a discrete n-channel JFET [4]. In this paper we report a JFET MMIC amplifier with comparable performance to the hybrid JFET amplifier at the 1-2 mW level. We also present the first work using pseudomorphic high electron mobility transistors (PHEMT) ultra-low power rf circuits. A hybrid amplifier using discrete PHEMTs operates as low as 25-150  $\mu\text{W}$  at 215 MHz with 5-10 dB of gain. To our knowledge these PHEMT results are the lowest power levels in any microwave technology at a comparable frequency.

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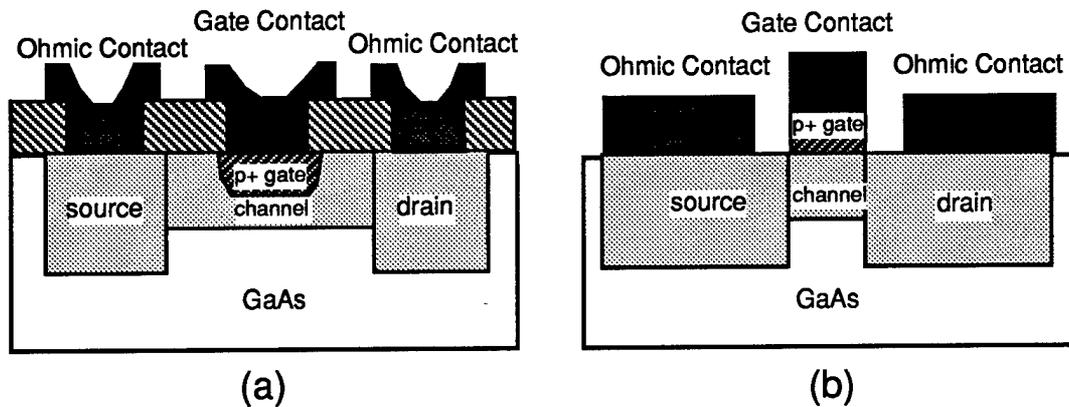


Figure 1. A comparison of conventional (a) and self-aligned (b) JFETs. The self-aligned JFET results in reduced parasitic gate capacitance.

### JFET MMIC

The JFET is the n-channel component of a complementary HFET technology developed in our laboratory [5]. Conventional JFETs are fabricated using diffusion to fabricate the  $p^+$  region and typically have inferior high frequency performance compared to MESFETs of the same gate length. For this work the JFET is an entirely implanted self-aligned device which has important advantages over both MESFETs and conventional JFETs. As shown in Figure 1, there is excess gate capacitance associated with conventional JFETs because of broadening of the  $p^+$  diffusion region and overhang of the gate metal which is not present in the self-aligned JFET. In the self-aligned JFET the  $p^+$  region is etched away coincident or undercut to the gate metal and the source and drain regions are ion implanted self-aligned to the gate. This leads to better high frequency performance of the self-aligned JFET compared to the conventional JFET. The self-aligned JFET also achieves comparable performance to MESFETs of the same gate length with the added advantage of a higher gate turn-on voltage. These and other attributes of the self-aligned JFET have been described previously [6, 7].

Low power digital applications require low bias voltages ( $V_{DS} \approx 1$  V), a small positive gate threshold, and large gate turn-on voltages ( $>1$  V). These design parameters are also ideal for low-power microwave applications. The voltages are very suitable for battery operation on a single cell and the positive gate threshold combined with the large positive gate turn-on voltage eliminates the need for a negative power supply as is commonly required with MESFETs. When measured at a 1 mW DC bias level ( $V_{DS} \approx 1$  V), the  $0.7 \times 100 \mu\text{m}^2$  device's microwave properties are impressive;  $f_t > 13$  GHz,  $f_{max} > 20$  GHz and a minimum noise figure of about 1.6 dB (with a 12 dB associated gain). A narrow-band amplifier was selected as a test vehicle since its successful implementation demonstrates the feasibility of most monolithic microwave integrated circuit (MMIC) functions. A hybrid amplifier built from a discrete JFET with external matching achieved 10 dB of gain at 2.4 GHz with 1 mW power consumption [4].

The hybrid amplifier was subsequently redesigned as a MMIC for on-chip matching using a 100  $\mu\text{m}$  thick GaAs substrate. Passive elements for designing the matching circuit included ion implanted GaAs resistors, SiN dielectric capacitors with 560 pF/mm<sup>2</sup> capacitance, airbridge inductors, and Au-plated (3  $\mu\text{m}$  thick) transmission lines. The

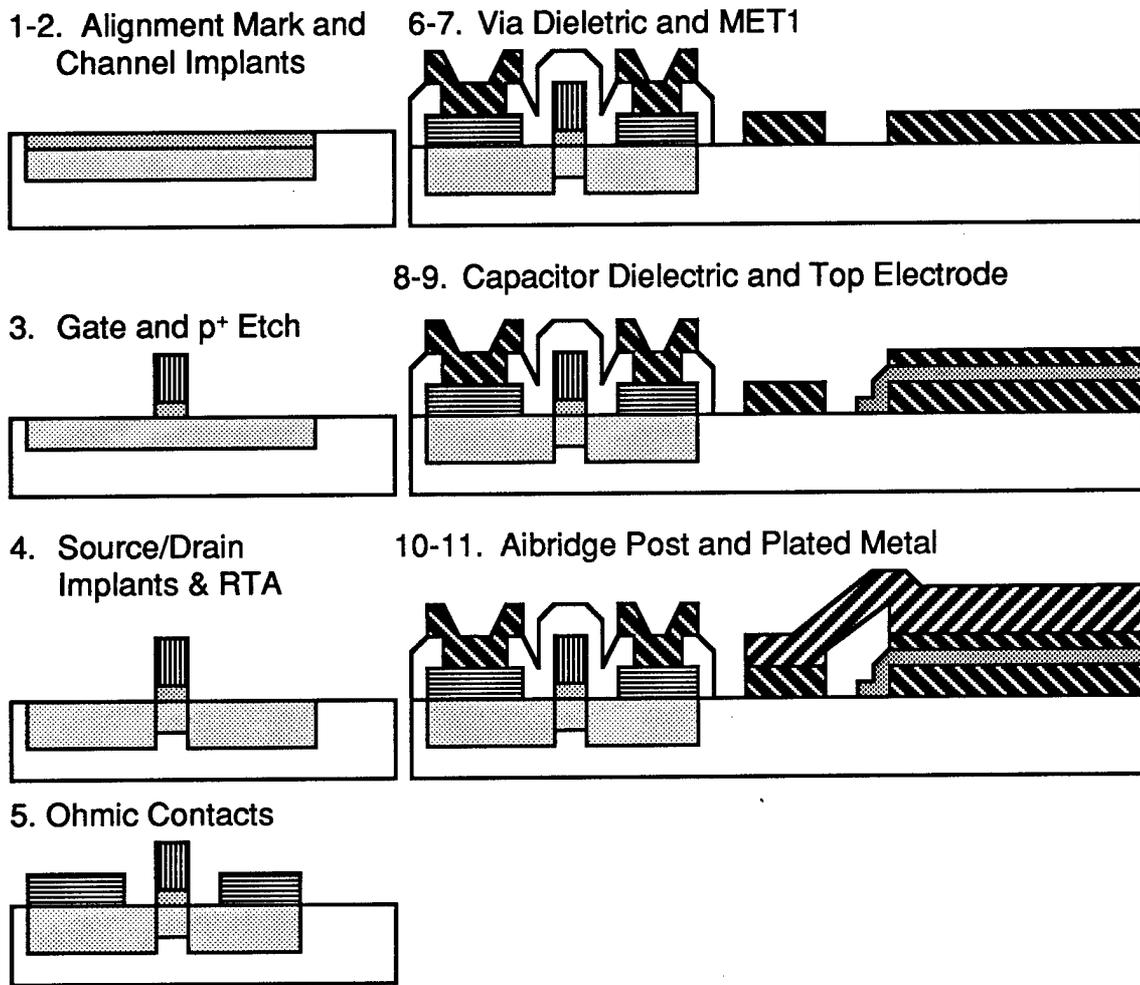


Figure 2. Process Sequence for JFET MMIC.

MMIC passive elements were introduced into the digital CHFET process at such points as to make the MMIC fully compatible with digital integrated circuit processing. Figure 2 illustrates the main processing steps for the JFET MMIC process. The process uses 12 mask levels. Steps 1-5 illustrate the JFET fabrication. After alignment mark formation, the channel implants are performed using Si ions for the channel, Mg for backside confinement, and Zn for the p<sup>+</sup> region of the JFET gate. In step 3, the W refractory gate is defined and the p<sup>+</sup> region is etched away in the source and drain regions of the JFET. The Si ion implants for the self-aligned source/drain regions and the implant activation rapid thermal anneal then follow. A single anneal is used for both the channel implant activation and the source/drain implant activation. JFET active regions are completed by ohmic contact formation. Steps 4 and 5 also serve to make the GaAs implanted resistors, with a sheet resistance of 400 Ω/square. Step 6 is used to passivate the JFETs with 4300 Å of SiN dielectric by plasma enhanced chemical vapor deposition (PECVD) and to open up via holes to the JFET gate and ohmic metals. Step 7 is the first metal (MET1) Ti/Pt/Au deposition. MET1 connects to the JFETs through the SiN vias and also directly to the

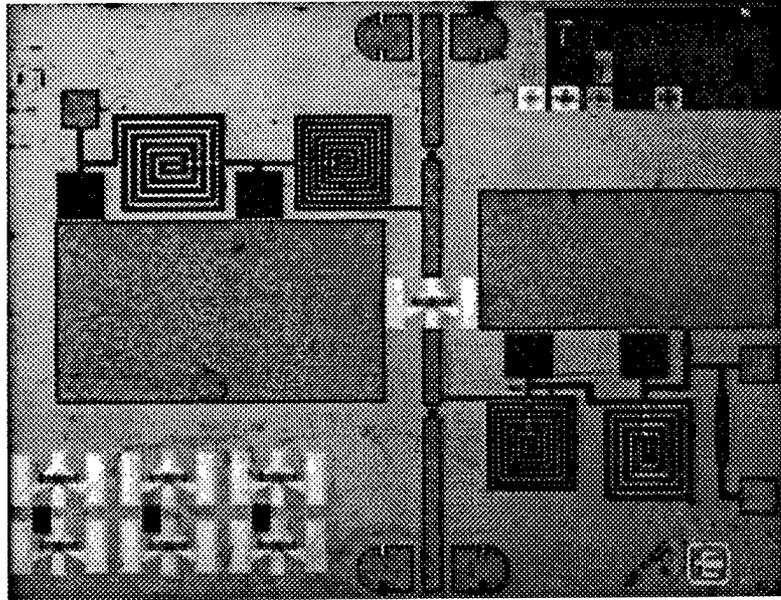


Figure 3. Microphotograph of the JFET MMIC.

GaAs substrate in the MMIC regions for the capacitors, transmission lines, and inductors. Step 8 is the PECVD deposition and patterning of a 1000 Å SiN capacitor dielectric. Step 9 is the metal patterning and deposition for the capacitor top electrode, a Ti/Pt/Au evaporation and liftoff. Step 10 is the photoresist patterning for the airbridge posts. Step 11 is the patterning and electroplating of the airbridge and transmission line metal. The final step consists wafer thinning, backside via formation (optional), and backside electroplating. For this first JFET MMIC the backside via process was omitted and frontside bond wires were used for grounding. After fabrication the MMIC was silver epoxied to a metal substrate along with chip capacitors for bias stability and alumina microstrip circuit adapters to facilitate microwave probing.

A picture of the completed JFET MMIC is shown in Figure 3. The chip dimensions are  $2.8 \times 2.3 \text{ mm}^2$ . The active device area covers only a small part of the chip area, which is largely determined by the passive elements and the transmission lines. The amplifiers design goals (based on on-wafer S-parameters of typical JFETs) were 2.4 GHz center frequency, 1-2 mW power consumption, 10 dB gain with 8 dB input/output return loss as in the amplifier based on the discrete JFET. The MMIC was designed for off chip bias control of the gate and drain so that it could be tested under various bias conditions. Microwave gain and return loss measurements were performed using an HP 8510C network analyzer using Cascade Microtech microwave probes calibrated using a TRL calibration. Shown in Figure 4 are plots of the gain (10.1 dB peak at 2.45 GHz, and input/output return loss ( $> 15 \text{ dB}$  at 2.45 GHz) all measured at 2 mW DC bias condition ( $V_{DS} = 2 \text{ V}$ ,  $I_D = 1 \text{ mA}$ ). At 1 mW the gain drops to 7-8 dB. Good agreement with the earlier hybrid amplifier and the MMIC design goals was achieved.

### PHEMT AMPLIFIER

The basic premise of designing ultra-low power microwave amplifiers is that one needs an intrinsically high gain device at the current and power levels desired. The options

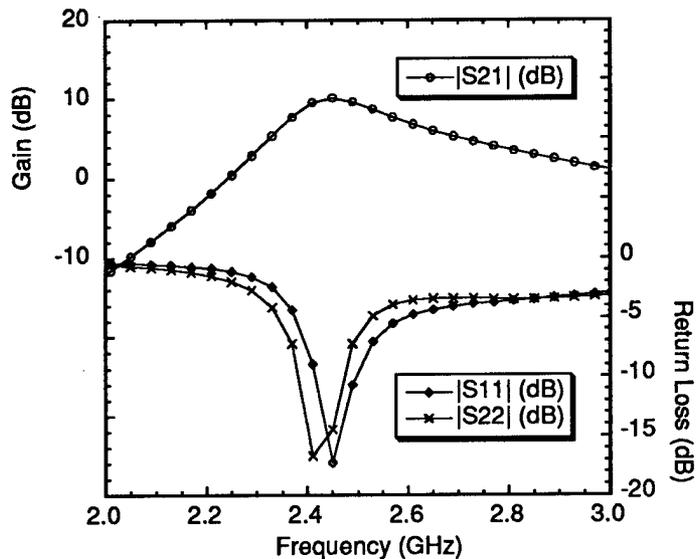


Figure 4. Measured gain and return loss of the JFET MMIC operated at a 2V, 1 mA (2 mW) bias level.

for doing this are to reduce the gate length of FETs or to use materials with superior transport properties such as GaAs PHEMTs, InP-substrate HEMTs or HBTs. In order to significantly reduce the power levels of microwave circuits (or possibly find fundamental limitations), we chose to explore the use of 0.25  $\mu\text{m}$  PHEMTs. The PHEMTs were grown and fabricated by conventional methods, therefore no explicit processing detail is given here. On-wafer S-parameter measurements of the completed PHEMT were taken and used as a basis of designing with discrete PHEMTs for hybrid amplifiers.

The hybrid amplifier was designed with simple reactive input and output matching networks. The amplifier frequency was chosen to be 215 MHz for arbitrary reasons, and no direct comparisons can be made to the 2.4 GHz results. Nevertheless, submilliwatt power levels have not been reported, to our knowledge, at this frequency or above. A split inductor design was selected in order to avoid the extremely small capacitors necessary in more conventional LC matching networks. Loss was introduced (by resistors) to achieve stability based on simulations. Both input and output matching networks are necessarily high-Q to achieve the required impedance transformation. Inductor Q limitations were found to be a severe design restriction. The design goal was 10 dB gain at 217 MHz with  $V_{\text{DS}} = 0.5$  V and  $I_{\text{D}} = 50$   $\mu\text{A}$  for a bias power level of 25  $\mu\text{W}$ .

Figure 5 shows the peak gain of the circuit at a variety of bias points. The measured gain fell short of 10 dB at the 25  $\mu\text{W}$  target. Measured gain of the amplifier ranged from 5 dB at 25  $\mu\text{W}$  to 10 dB at 150  $\mu\text{W}$  at 215 MHz. The first construction of the amplifier used chip inductors which resulted in only a few decibels of gain under the best of bias conditions. Substitution of hand-wound wire inductors resulted in some improvement. The present low gain is believed still due to the low Q of the inductors. Nevertheless, the power gain-power tradeoff of the 0.25  $\mu\text{m}$  PHEMT technology (215 MHz) compared to the Si bipolar technology (150 MHz) [3] is as follows: twenty times

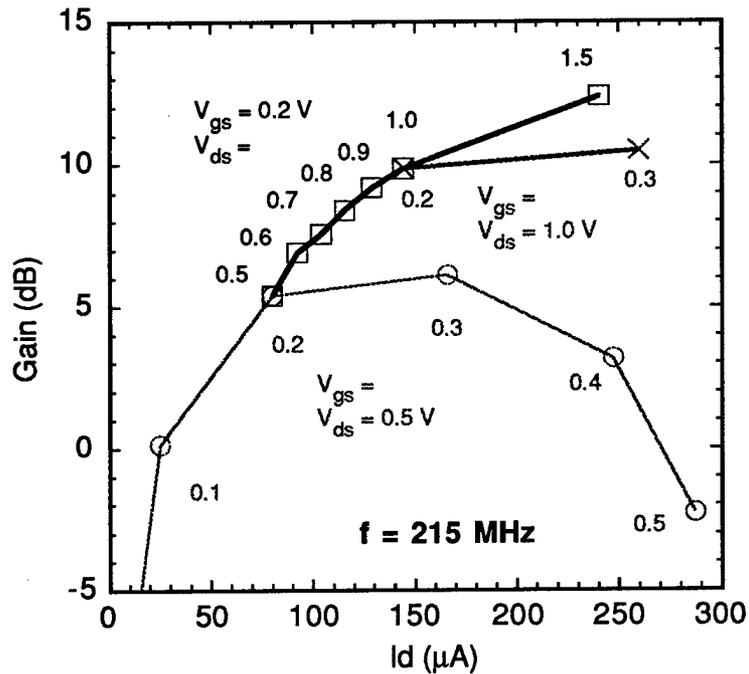


Figure 5. Measured peak gain of PHEMT amplifier at various bias conditions.

lower power with 15 dB less gain. For technologies requiring these power levels the PHEMT technology is a promising candidate.

## CONCLUSION

Ultra-low power microwave technology results have been presented for  $0.7\ \mu\text{m}$  JFETs and PHEMTs. The JFETs are compatible with a digital CHFET technology. A JFET MMIC amplifier was demonstrated which achieved 10 dB of gain at 2.4 GHz and 2 mW power consumption. Much lower power levels were achieved with  $0.25\ \mu\text{m}$  PHEMT technology. A 217 MHz amplifier achieved 5 dB gain with only  $25\ \mu\text{W}$  power or 10 dB gain with  $150\ \mu\text{W}$ .

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