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P. G. Carey, P. M. Smith, P. Wickboldt,
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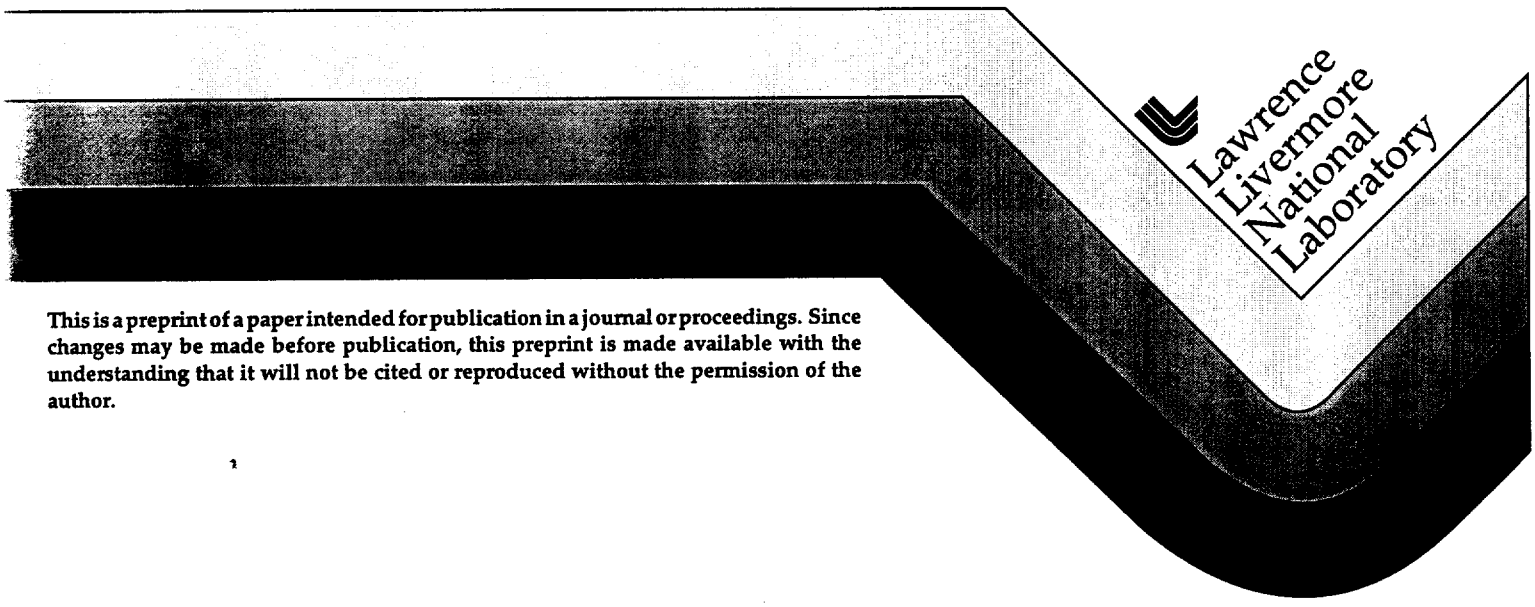

POLYSILICON TFT FABRICATION ON PLASTIC SUBSTRATES

Paul G. Carey, Patrick M. Smith, Paul Wickboldt,
Michael O. Thompson†, and Thomas W. Sigmon

Lawrence Livermore National Laboratory, 7000 East Ave., L-271, Livermore, CA 94551

†*permanent address: Dept. of MS&E, Bard Hall, Cornell University, Ithaca, NY 14853*

Abstract

Processing techniques utilizing low temperature depositions and pulsed lasers allow the fabrication of polysilicon thin film transistors (TFT's) on plastic substrates. By limiting the silicon, SiO_2, and aluminum deposition temperatures to 100°C, and by using pulsed laser crystallization and doping of the silicon, we have demonstrated functioning polysilicon TFT's fabricated on polyester substrates with channel mobilities of up to 7.5 cm^2/V-sec and I_{ON}/I_{OFF} current ratios of up to $1x10^6$.

I. Introduction

The low cost and excellent durability of plastic displays will dramatically increase the range of both military and consumer products into which displays will be incorporated. The weight and power requirements of portable electronics such as communications and computing equipment is significantly reduced by using reflective plastic displays. However, constructing an AMLCD on plastic has not been feasible using standard processing techniques, due to the temperature limitations required for commonly available plastics. For example, present day a-Si TFT processes call for 300°C SiN and 225°C to 250°C a-Si deposition steps, with poly-Si processes requiring even higher temperatures (400°C to 600°C).

Plastic substrates are desirable for displays because they are flexible, lighter, and less expensive than glass substrates. Glass displays of increasingly larger area have become extremely difficult to manufacture due to weight, breakage, and the stringent plate separation tolerances required for conventional AMLCD's. Plastic sheets are ideal substrates for low-cost, low-power reflective displays based on polymer-dispersed (PDLC) liquid crystal materials, which can be applied to large areas using simple spray or roll-coating processes.

We have developed a low-temperature low-thermal budget Si thin film transistor fabrication process that allows TFT's to be made on plastic substrates using processing temperatures less than or equal to 100°C. The fabrication process relies on excimer laser crystallization and doping techniques pioneered by our group at LLNL. The short laser pulse (~35ns) melts, dopes and recrystallizes the Si layer of the TFT in less than 100 ns, well before the underlying substrate can be heated. Thus the substrate remains at moderate temperatures while an initially poor quality a-Si film is crystallized and doped. We have exploited this low thermal budget process to produce poly-Si TFT's on plastic substrates that are unable to withstand sustained processing temperatures above 100°C.

Laser doping is clearly an enabling technology for producing Si TFT's on plastic due to its extremely low thermal budget. This technology may enable the manufacture of paper thin AMLCD's on low-cost, flexible substrates for use in hand held electronic applications.

II. Experimental

IIa. Device Fabrication

The substrate material is 175 μm thick polyethyleneterephthalate (polyester), chosen for its low cost, high optical transmission (~80%), and widespread availability. This substrate material poses severe temperature constraints on the processing because it is unable to withstand sustained temperatures

higher than 120°C. We have therefore limited our temperatures to less than or equal to 100°C in order to minimize shrinkage and allow alignment of multiple photolithography steps. Processing is performed on 4-inch (100 mm) diameter polyester wafers cut from rolls 24-inches wide.

Cross sections of our TFT device structure at various stages of fabrication are shown in Fig. 1 (a)-(c). This simple Al top gate device is ideally suited to laser crystallization and doping, requiring only 4 photolithography steps. The process begins with a 100°C plasma enhanced chemical vapor deposition (PECVD) step to deposit an oxide and an amorphous silicon (a-Si) layer. The silicon layer is then crystallized using the laser process described below. The bottom oxide serves as a thermal barrier between the a-Si and the polyester during laser processing. After this laser crystallization step, the device stack is completed by PECVD deposition of a gate oxide followed by Al sputtering to form the gate (see Fig. 1(a)).

The gate stack is patterned using standard silicon integrated circuit photolithographic and etching techniques modified for compatibility with plastic substrates. The TFT source and drain regions are doped using a second pulsed excimer laser processing step, Gas Immersion Laser Doping (GILD), a process developed at Stanford University and LLNL [1]. The top aluminum gate shields the TFT channel region as shown in Fig. 1(b).

The TFT device islands are then defined by plasma etching of the silicon, and an oxide contact isolation layer is deposited using 100°C PECVD. Source and drain contact holes are etched in the oxide, and the device is completed by depositing, patterning, and etching the Al interconnect metallization layer (see Fig. 1(c)).

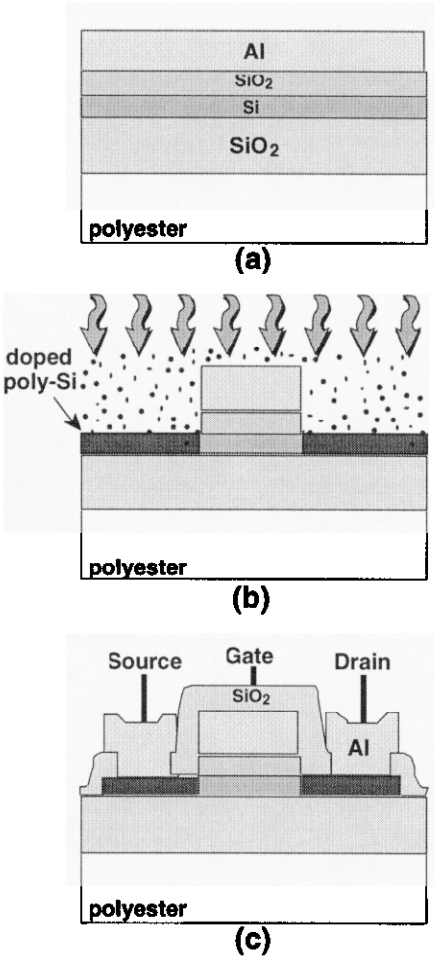

Fig. 1 - Cross sections of LLNL's 100°C silicon TFT on plastic process. This self-aligned Al top-gate structure requires 4 photomasking steps.

IIb. Laser Processing

The laser crystallization step has been studied by many groups and is used to create polycrystalline silicon at low substrate temperatures from a-Si deposited either by PECVD or low pressure chemical vapor deposition (LPCVD) (see, for example [2],[3],[4], or [5]). We use a XeCl pulsed excimer laser (λ=308 nm) with a temporal pulse length of 35 ns and a maximum repetition rate of 25 Hz to irradiate the a-Si. Our laser beam size can vary from 2x2 to 11x11 mm^2 at the wafer surface. Since PECVD deposited a-Si has a high hydrogen concentration (our 100°C deposited silicon has about 15% as determined by RBS measurements), multiple laser scans are used with increasing fluence for each scan (similar to the work by Mei *et al.* [6]). Low laser energy fluences promote hydrogen evolution from the a-Si layer, while higher fluences melt and crystallize the surface region and dehydrogenate the underlying region. The final melt depth and polysilicon grain size depend on the particular laser conditions and silicon layer thickness used. The laser system has been automated to facilitate laser scanning at multiple pulses and energies. For our wafers the typical laser

energy fluences range from 100 to 350 mJ/cm^2 and from 3 to 15 pulses at each energy. At least 3 energy fluences are used for the dehydrogenation and polysilicon formation.

Melting and crystallization of the silicon for each laser pulse is so rapid (<100 ns) that the plastic substrate remains at relatively low temperatures throughout the process. In Fig. 2 we show a thermal simulation of the heating in each layer of a silicon/oxide coated plastic substrate during the excimer laser crystallization process. This simulation uses a relatively high energy fluence of 350 mJ/cm^2 and confirms our experimental results that the plastic is undamaged by showing that the heating of the underlying polyester to above its softening point occurs for only a few tens of microseconds. The surface of the silicon region is above the melting point for poly-Si (1410°C), but the underlying barrier oxide protects the plastic and prevents it from seeing the extreme surface temperature. The extremely small thermal budget of this laser process thus prevents damage to the polyester.

Laser doping is performed in the same apparatus as the crystallization step except for the addition of a doping ambient. The GILD process accomplishes doping by melting the surface of the silicon in the presence of a doping gas ambient such as BF_3 (for p-type) or PF_5 (for n-type). Each laser pulse drives more dopant into the melted laser. Repeated melting of each wafer location by about doping 50 pulses creates low sheet resistance polysilicon. This technique is ideally suited for making low sheet resistance silicon on plastic substrates, and we have obtained values down to 500Ω/□ on polyester.

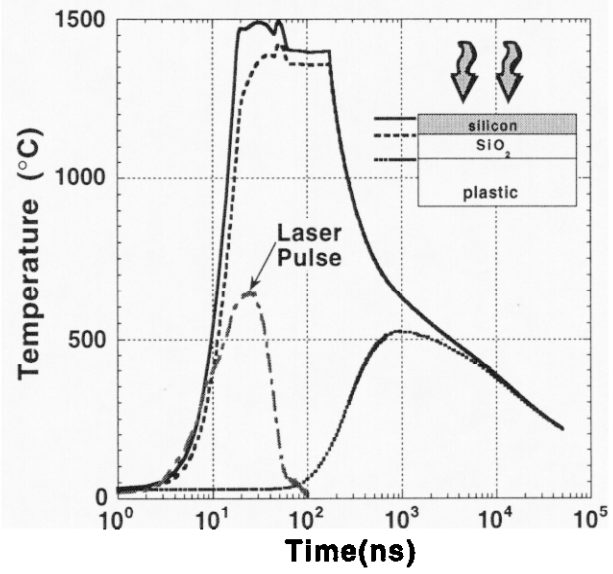

Fig. 2 - Simulation of the TFT source/drain region thermal history during the laser doping process. The curves match the layers shown in the inset. The XeCl excimer laser pulse intensity units are arbitrary.

III. Results and Discussion

The TFTs fabricated using this process show transistor behavior with I_{ON}/I_{OFF} current ratios greater than 10^6 as shown in Fig 3. This

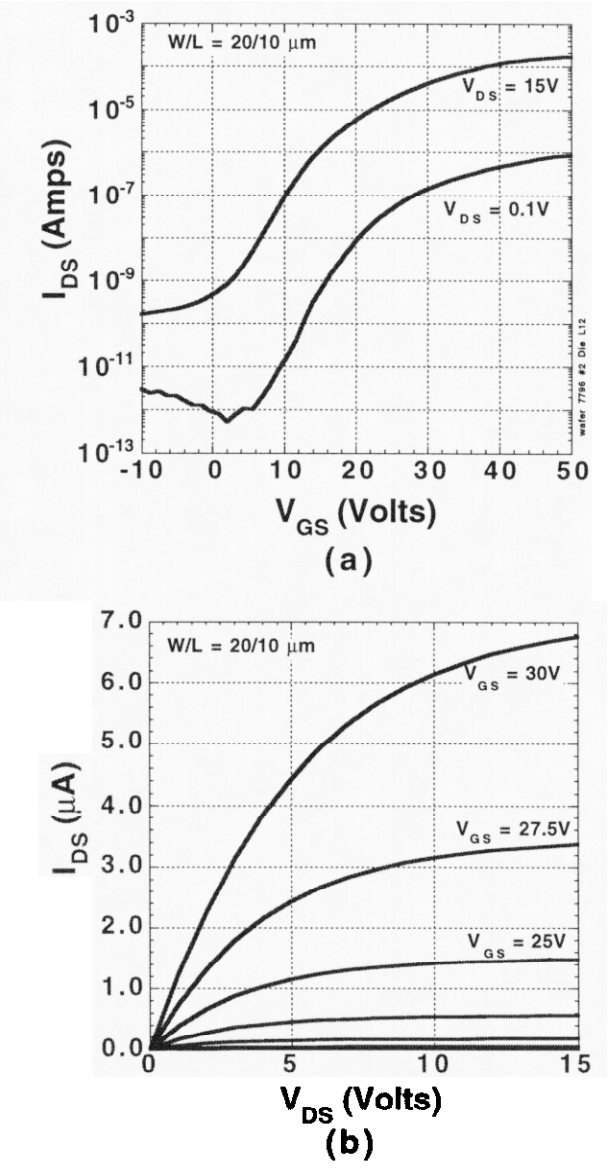

Fig. 3 - Current-Voltage characteristics of a poly-Si TFT fabricated at T_{MAX} = 100°C on polyester.

I_{ON}/I_{OFF} ratio is acceptable for pixel transistors in small display applications.

A summary of the TFT electrical parameters is given in TABLE I. These parameters compare favorably with the work presented in [7] where higher performance TFT's were made at substrate temperatures of T=250°C on polyimide and T=200°C on polyethersulfone using pulsed excimer laser crystallization and dopant activation.

TABLE I: A summary of the poly-Si TFT (W/L=20/10 μm) on plastic device performance.

Parameter	Value
I_{ON}/I_{OFF}	$>10^6$
I_{ON}	>100μA
I_{OFF}	<100pA
V_{TH}	~8V
μ_{EFF}	> 7.5 cm^2/V-sec
R_{SHEET} S/D	< 1 kΩ/□
$R_{CONTACT}$	$<1x10^{-4}$ Ω-cm^2

To date the device performance is adequate for small display applications despite the lack of a rehydrogenation step or higher temperature anneal. Process limitations imposed by the 100°C maximum temperature do not appear to significantly affect the source/drain sheet resistance values because the doping is accomplished by laser doping. Values below 1kΩ/□ are achieved. However, the TFT's and aluminum to silicon contacts would most likely improve with a higher temperature anneal. Further improvement in the gate oxide dielectric deposition at ≤100°C would also improve the TFT performance.

IV. Summary

We report functioning polysilicon channel TFT's fabricated on polyester substrates at a maximum temperature of 100°C. This process features pulsed laser crystallization and doping of the silicon layer and low temperature deposition of the silicon, SiO_2, and aluminum layers. These TFT's exhibit channel mobilities up to 7.5 cm^2/V-sec and I_{ON}/I_{OFF} current ratios up to $1x10^6$.

V. Acknowledgements

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References

[1] P. G. Carey, K. Bezjian, T. W. Sigmon, P. Gildea, and T. J. Magee, "Fabrication of submicrometer MOSFET's using gas immersion laser doping (GILD)," *IEEE Electron Dev. Lett.*, Vol. EDL-7, pp. 440-442, 1986.

[2] E. Fogarassy, H. Pattyn, M. Elliq, A. Slaoui, B. Prevot, R. Stuck, S. de Unamuno and E. L. Mathé, "Pulsed Laser Crystallization and Doping for the Fabrication of High-Quality Poly-Si TFT's," *Appl. Surf. Sci.*, vol. 69, pp. 231. 1993.

[3] M. Furuta, T. Kawamura, T. Yoshioka and Y. Miyata, "Bottom-Gate Poly-Si Thin Film Transistors Using XeCl Excimer Laser Annealing and Ion Doping Techniques," *IEEE Trans. Electron Devices*, Vol. 40, no. 11, pp. 1964, 1993.

[4] A. Kohno, T. Sameshima, N. Sano, M. Sekiya and M. Hara, "High Performance Poly-Si TFT's Fabricated Using Pulsed Laser Annealing and Remote Plasma CVD with Low Temperature Processing," *IEEE Trans. Electron Devices,* Vol. 42, no. 2, pp. 251, 1993.

[5] H. Kuriyama, "Excimer Laser Crystallization of Silicon Films for AMLCDs," Proceedings of *AMLCDs '95*, pp. 87, 1995.

[6] P. Mei, J. B. Boyce, M. Hack, R. A. Lujan, R. I. Johnson, G. B. Anderson, D. K. Fork and S. E. Ready, "Laser Dehydrogenation/Crystallization of Plasma-Enhanced Chemical Vapor Deposited Amorphous Silicon for Hybrid Thin Film Transistors," *Appl. Phys. Lett.*, Vol. 64, no. 9, pp. 1132, 1994.

[7] N.D. Young, R.M. Bunn, R.W. Wilks, D.J. McCulloch, G. Harkin, S.C. Deane, M.J. Edwards, and A.D. Pearson, "AMLCDs and electronics on polymer substrates," in EURO Display '96, pp. 555-558, 1996.

Technical Information Department • **Lawrence Livermore National Laboratory**
University of California • Livermore, California 94551