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ANALYSIS OF INDIUM-PHOSPHIDE/INDIUM
TIN OXIDE SOLAR CELLS

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ANALYSIS OF INDIUM-PHOSPHIDE/INDIUM TIN OXIDE SOLAR CELLS

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ABSTRACT

This paper is concerned with an investigation into the mechanisms underlying the operation of p-type indium-phosphide (InP)/n-type indium tin oxide (I.T.O.) solar cells. These have been fabricated by depositing thin films of I.T.O. onto InP substrates by both R.F. sputtering and ion-beam sputtering. In the former case, the data support the results of Bachmann *et al.* (1) whilst in the latter they resemble those of Tsai *et al.* (2). It is shown that the properties of these cells depend not only on the method of fabrication but also on several other complicating effects which occur before, during and after deposition of the I.T.O.

INTRODUCTION

Solar cells based on thermally deposited thin films of n-type cadmium-sulphide (CdS) on p-type InP single crystal substrates were first prepared by Wagner *et al.* (3) and the reasons for the high efficiencies are well understood. Efficient devices based on R.F. sputter deposited films of I.T.O. on InP single crystals have also been fabricated (4) despite there being an apparent lack of fundamental reasons why this should be so.

Recent publications, Tsai *et al.* (2) and Ashok *et al.* (5) claim that in the cases of both R.F. and ion-beam sputter deposition of I.T.O. films onto single crystal substrates, damage to the latter occurs which causes type conversion of the crystal surface and the consequent formation of a buried homojunction. The precise cause of the damage is not clear particularly in the case of R.F. sputtering, although there are several possibilities. It seems unlikely that damage to the substrate during the very early stages of film deposition could be similar to the mechanism of sputter etching, as has been suggested by (2). We have studied this aspect in some detail and from a variety of analyses have concluded that whilst the data reported in (2) and (5) above appear self-consistent and compatible with a buried homojunction model, this need not necessarily be expected to apply in all cases. At this stage, we have tentatively concluded that R.F. heating of the substrates causes a structural

adjustment of the surface rather than type conversion as reported in (2). The effects are probably less severe in our case since we use only one seventh the R.F. power density. Heated surfaces have been found to be depleted in phosphorous and this may be responsible for the observed crystallographic changes.

Further complications can arise due to the formation of native oxides on the InP in the short time which elapses between sample preparation and transfer to the deposition system. Bertrand (6) and Kazmerski *et al.* (7) have used Auger Electron Spectroscopy (AES) and X-ray Photoelectron Spectroscopy (XPS) to identify such layers and from these studies, plus the data reported here, it is clear that the preparation procedure may be much more important to the operation of the completed device than has previously been recognized. In addition to these effects, it is also possible that there is a loss of the dopant (zinc or cadmium in the present case) during fabrication although this has not as yet been observed. Spicer (8) has also shown that pinning of the surface Fermi level can occur when a small fraction of a monolayer of oxygen is adsorbed by InP. The role of this effect in device operation is not yet understood. In this paper, we discuss measurements made of surface composition, light and dark J-V characteristics, capacitance and conductance as functions of frequency for the two types of cell we have fabricated, and attempt to relate these to the various models of device operation suggested in the literature.

Substrate Preparation and Device Fabrication

Two types of InP substrate were used in this work; multi-crystal and single crystal. The former were supplied by R.S.R.E. Malvern; they were 2.5 cm diameter, 0.05 cm thick and zinc doped ($N_A-N_D \approx 3 \times 10^{16} \text{ cm}^{-3}$) with a resistivity of approximately $3 \Omega \text{ cm}$. These were randomly oriented having at least twenty individual crystallites in each substrate. Grain sizes varied from about 5 mm to $< 1 \text{ mm}$. The latter were supplied by Metals Research Ltd. and they were $\langle 111 \rangle$ oriented, 1 cm x 1 cm, 0.05 cm thick and cadmium doped ($N_A-N_D \approx 7 \times 10^{17} \text{ cm}^{-3}$) with a resistivity of $0.1 \Omega \text{ cm}$. Zinc doped single crystal substrates are also available and devices fabricated from these will be reported at a later date. The multi-crystal substrates (M.C.S.) were supplied in an

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as-sawn condition and the surface was polished to a 0.3 μ m finish with alumina powder, then etched in 0.5 v/o bromine/methanol for about 30 seconds to remove surface damage and finally immersed in a reducing solution of H₂O:HF:HCl in the proportions 10:1:1 by volume. The single crystal substrates (S.C.S.) were supplied in a highly polished condition which was much superior to that of the M.C.S. Before making electrical contact to them, however, they were given the same chemical treatment as the M.C.S.

A variety of contacting systems has been used with varying degrees of success. The most successful technique has been to evaporate separate films of zinc and gold (500Å and 5000Å) followed by sintering at 250°C in forming gas for one minute. The best contacts are formed when the composite film appears silver in colour rather than golden and these gave a contact resistance of approximately 15 Ω cm².

Devices based on the M.C.S. were formed by R.F. sputter depositing films of I.T.O. on the central 2.2 cm² of their surface (the sputtering parameters have been described previously (9)), whereas the S.C.S. devices were based on ion-beam sputtered I.T.O. In this case, an Ultek Cryogenic Pumping System incorporating an Ion Tech Ion Gun was used. The InP wafers were not ion-etched prior to deposition. Sputtering was carried out in purified argon at a pressure of 10⁻⁴ torr, using an accelerating voltage of 1400V and a beam current of 80mA. At the surface of the I.T.O., the beam diameter was 10 cm and the duration of sputtering was adjusted to give a thickness of about 750Å which acted as an anti-reflection coating. The films were deposited onto an area 0.9 cm x 0.9 cm of the S.C.S. The substrates were not deliberately heated above room temperature in either the case of R.F. or ion beam sputtering.

Top contact to the I.T.O. was made via gold plated copper foil grids which were pressed into contact using Cellotape (Scotch Tape) for the M.C.S. and Mylar for the S.C.S. This apparently crude procedure has given fill-factors only 30% less than good quality evaporated grids. In neither case is the grid geometry optimal for the I.T.O. resistivity.

Surface Analyses

After the standard substrate cleaning procedure described above, the substrates were examined by several techniques. Using reflection electron diffraction (RED) on individual grains of the M.C.S., excellent single crystal spot patterns were found; this indicating that if there were a contaminating surface layer it could not be thicker than about 100Å. AES and XPS, however, did indicate a contaminant layer with a very small amount of oxygen present, this presumably being an unavoidable consequence of the cleaning procedure and subsequent transfer to the spectrometer. The AES trace is shown in Figure 1. During sputter profiling, the oxygen signal changed very little and in reality was only just above the noise level initially. However, there was a shift of the

indium and phosphorous XPS peaks by approximately 0.1eV and 0.2eV respectively after a very short period of sputtering. Semi-quantitative analysis of the above data suggests that there are very thin layers of mixed indium and phosphorus oxides in the InP surface as previously suggested by Bertrand (6) and Kazmerski (7). Wager *et al.* (10) have examined freshly cleaned InP surfaces by ellipsometry and concluded that there is always an oxide layer 12-20Å thickness. This is quite consistent with the above observations. Examinations of substrates which had not been subjected to the reducing etch following the bromine/methanol etch showed a considerably greater shift of the indium and phosphorus XPS peaks during sputter profiling from which it may be concluded that even though the reducing etch does not totally eliminate contamination, it is beneficial.

It has previously been claimed (2) that during sputter deposition of a thin film onto a semi-conducting substrate, the latter suffers damage similar to that experienced by the target. In Figure 2, we show a scanning electron micrograph (SEM) of the surface of a chip subjected to sputter etching at normal power for ten minutes. EDAX analysis shows that the columns are increasingly rich in indium towards their tips, the spheres actually being metallic indium which has presumably been in a molten state. By comparison, the surface of a chip placed in the usual substrate position, but using an aluminum target, which is known to have a very low rate of erosion, and exposed to the R.F. plasma, showed no such features. On the other hand, it did show a change in the R.E.D. pattern. Superimposed upon, and passing through, the single crystal spot pattern were weak polycrystalline rings indicative of a change in the surface morphology. This change could also be effected by heating a chip in an inert atmosphere at temperatures as low as 150°C although the effect is strongly orientation dependent. This result strongly suggests that in our RF sputtering system, surface modification is thermal in origin (possibly RF heating) rather than particulate. When such surfaces were contacted, there was a total absence of any photovoltaic effect. Hence, we do not accept that type conversion is inevitable although it does seem probable that a modified surface layer will be present, its thickness and properties being dependent on the RF power. One possible cause of the surface effect may be loss of phosphorus during heating. It is claimed (11) that this commences at only 100°C. This being so it must already have taken place after contact sintering, even before deposition of the I.T.O. From the above reasoning, we conclude that the surface of the InP substrate upon which the I.T.O. is deposited must be somewhat ill-defined and as a consequence one should expect the differences in the detail of device operation to be strongly dependent on the substrate history.

Analysis of Devices

Current/voltage characteristics of the diode were obtained using an automated data acquisition system, a quartz-iodine lamp being used to simulate AM1. The comparison of individual cells against

a xenon arc simulator showed that the above system was surprisingly accurate, the difference in fill-factor being only about 0.1%. A comparison is shown in Figure 3 between M.C.S. and S.C.S. cells. The area of I.T.O. was 2.2 cm² and 0.81 cm² respectively. Although the efficiencies of these are quite reasonable considering their relatively large area, there is clearly scope for substantial improvement via a reduction of the series resistance. The ratio of J_{sc}/J_0 for these cells suggests that it should be possible to achieve a fill-factor of 80%.

Figure 4 shows a plot of $\log J_{sc} \sim V_{oc}$ for these two devices as measured at 20°C: the intensity of illumination was varied using fine wire meshes as neutral density filters. These curves were obtained at several higher temperatures and from the slope and intercept of each line the values of A and J_0 were determined. Arrhenius plots of the two sets of J_0 are shown in Figure 5 and these give activation energies of 0.820eV and 0.504eV respectively for the M.C.S. and S.C.S. devices respectively. The former value has also been obtained from an analysis of the dark characteristics. It is important to point out that at the lower temperatures, there was a discontinuity in the lines of $\log J_{sc} \sim V_{oc}$. Only the upper parts of the curve are shown; the lower portions clearly being indicative of a different forward current mechanism with values of A greater than 2.0. This has been reported for other devices (12).

Figures 6 and 7 show the usual plots of $1/C^2$ against reverse bias voltage from which it is clear that only the M.C.S. device prepared by R.F. sputtering can be represented by the abrupt junction depletion model. A plot was made of $1/C^3 \sim V$ (i.e., the linear graded junction model) for the S.C.S. device over the full bias range but this too was non-linear. However, when plotted over the range 0-1 Volt, it was clearly linear as seen in Figure 8, from which the built-in potential was calculated. Both types of cell had characteristics which were dependent on frequency but, for the M.C.S. device, at lower frequencies the value of the built-in potential was close to that obtained from the J_0 Arrhenius plot. Conductance data also showed frequency dispersion in reverse bias although in forward bias this disappeared and the conductance saturated at a value close to the reciprocal of the series resistance. No peaks in the conductance were observed from which it can be supposed that an inversion layer is not formed.

DISCUSSION AND CONCLUSIONS

The results presented here lead us to conclude that prior to depositing the ITO by either RF or ion beam sputtering, the surface of the InP must be modified due to: (i) the presence of a very thin surface oxide, probably P_2O_5 , in the thickness range 12-20Å, (ii) recrystallization of the surface due to loss of phosphorous during contact sintering. The substrates could be re-etched prior to deposition of the I.T.O. to remove the re-crystallized layer but it appears

that the influence of the RF sputtering process would still be felt once deposition commenced. This would not be the case, however, with ion-beam sputtering in which the heating effect is small but which apparently causes damage due to the high energy of the incident material. It would therefore, be interesting to fabricate devices using a range of beam energies.

In general, our data support the conclusion of Bachmann (1) that the RF sputtered devices behave like SIS or heterojunction cells. On the other hand, the ion-beam sputtered cells behave more like the buried homojunction devices described by Tsai *et al.* (2). In neither case has an efficiency as great as those reported by Bachmann been achieved although this seems to be more a technological matter of providing adequate contacting than a fundamental limitation of the junction. Although we have achieved considerably higher values of short circuit current density than Bachmann, the corresponding values of open circuit voltage are lower and one possible reason for this is that our M.C.S. cells may be more like genuine heterojunctions and our S.C.S. cells like homojunctions whereas his may be SIS devices. This being the case, it would be of interest to determine the optimum oxide thickness. It also implies that the chemically and structurally modified nature of the interfaces are not particularly damaging to our devices.

It is significant that the M.C.S. cells have a barrier height of 0.82eV which is similar to the values published elsewhere for sprayed ITO/InP cells (12) and for Al/InP Schottky barrier devices (13). The ideality factor appears to be invariant with temperature, above the discontinuity in the $\log J_{sc} \sim V_{oc}$ plot, and approaching unity. These results suggest the applicability of the Anderson heterojunction model. The separation of the Fermi level from the valence band edge is about 0.2eV so that the electron affinity mismatch plus any band-bending due to surface states or stored charge at the interface, need only amount to about 0.25eV for the model to be arithmetically reasonable. If the surface Fermi level is pinned 0.4eV below the conduction band minimum as suggested by Spicer *et al.* (8), the heterojunction model may not be applicable. Below the discontinuity in the $\log J_{sc} \sim V_{oc}$ plot, the forward current is more compatible with a tunnelling/recombination process.

The reasons for the frequency dependance of the reverse bias conductance are unknown at this stage but could be related to interface states or minority carrier generation rate, for example. Certainly the departure from linearity of the $1/C^2 \sim V$ plots for the S.C.S. cells implies a graded junction which, if caused by damage, would be expected to exhibit traps and time dependant effects. There is also a small frequency dispersion for the M.C.S. devices which we have concluded do not have a graded junction. This aspect should be informative in future.

Finally, we conclude that R.F. sputtering need not necessarily lead to damage of semiconducting substrates. This is an important result, not

only for solar cell technology but for the future of several devices whose fabrication may involve sputtering.

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Fig.1 A.E.S. of Chemically Etched InP.

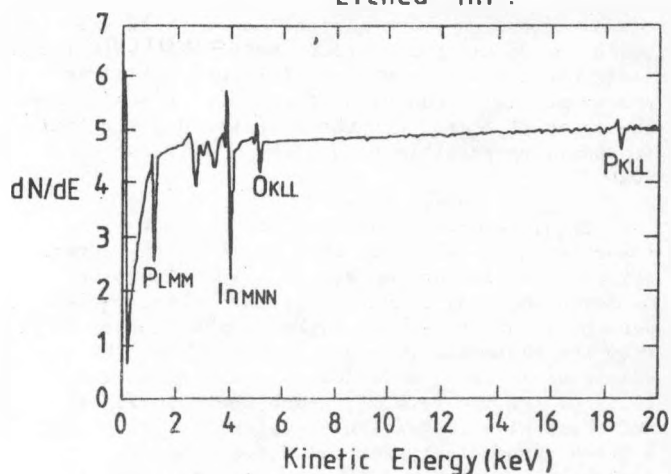


Fig. 1 The scan shows a small amount of oxygen contamination after the reducing etch, probably of the order of a few monolayers.

Fig.2 S.E.M. of Sputter Etched InP.

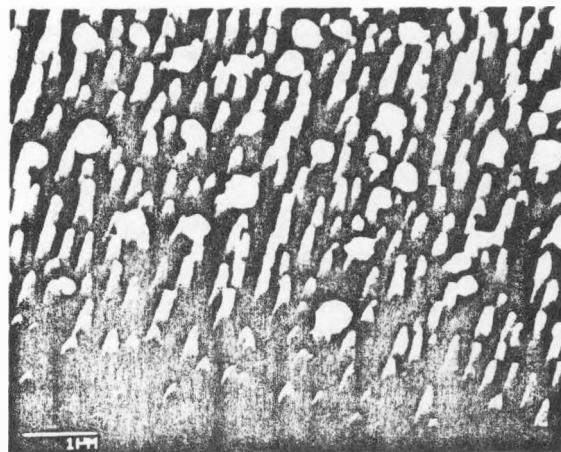


Fig. 2 The spheres on the top of the columns are metallic In. The columns are progressively more In rich nearer their tips.

Fig.3 J/V Characteristics of I.B. and R.F. Sputtered I.T.O. Cells

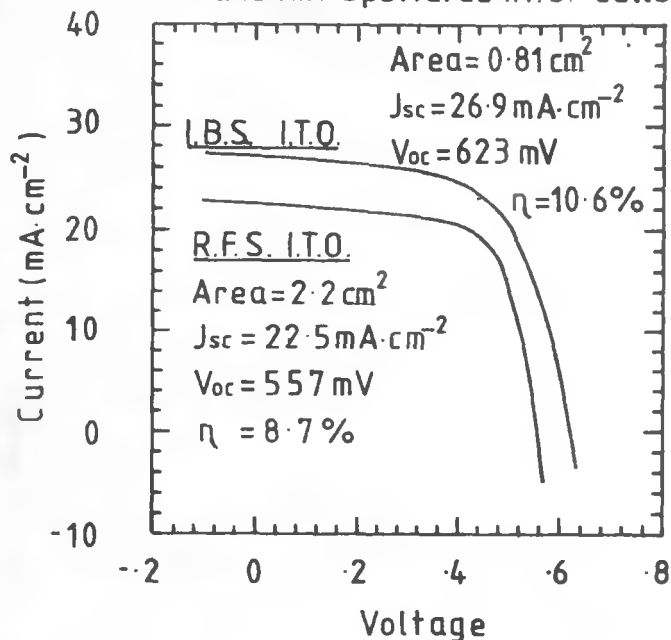


Fig. 3 The I.T.O. area of the R.F. sputtered I.T.O. cell is 2.2 cm^2 , and its efficiency is 8.4%. The corresponding values for the ion beam sputtered I.T.O. cell are 0.81 cm^2 and 10.6%.

Fig. 4 $\log J_{sc} \sim V_{oc}$ for R.F. and Ion Beam Sputtered I.T.O.

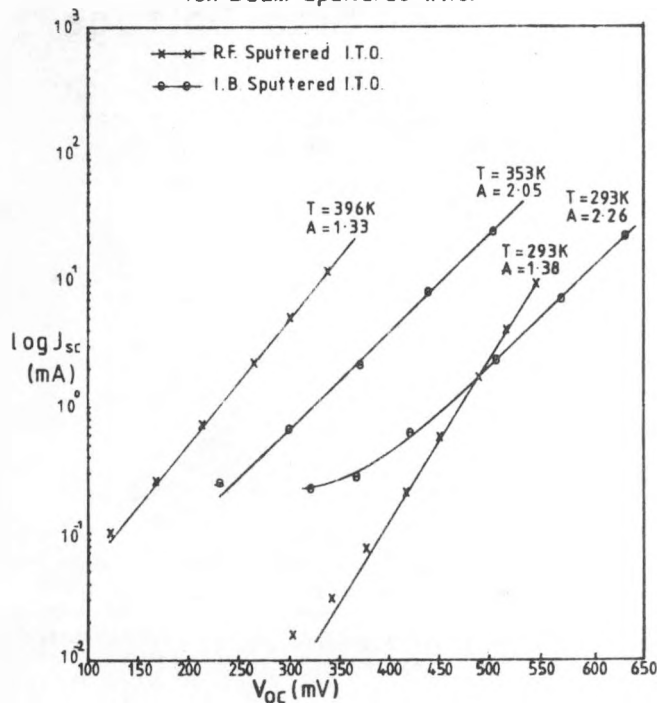


Fig. 5 Arrhenius plots of J_0 for MCS and SCS cells. The activation energies of these were 0.82 and 0.50 eV respectively.

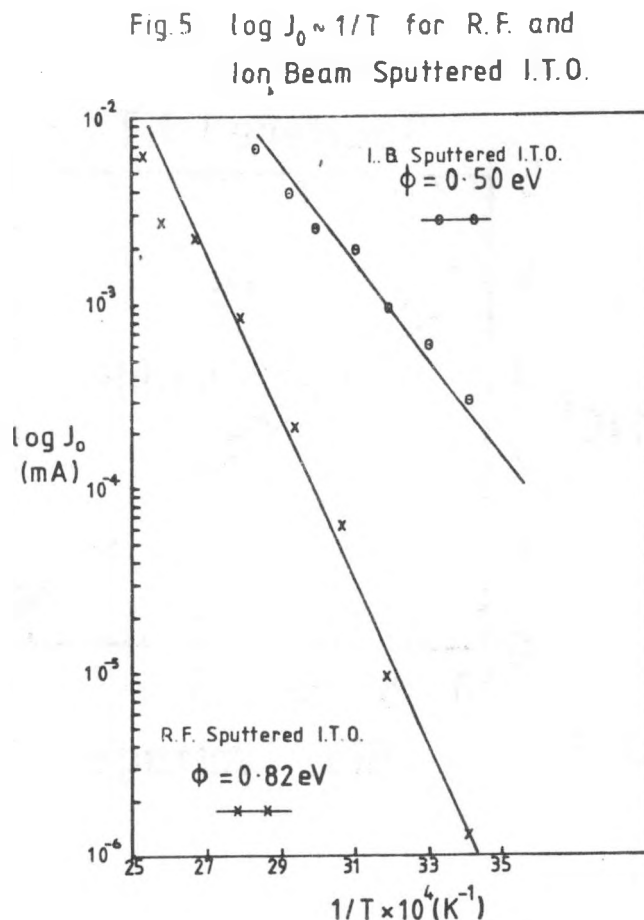


Fig. 4 Only the upper and lower limits of temperature are shown. For the M.C.S. cell the values of A and J_0 for $T=293\text{K}$ and $T=395\text{K}$ are 1.38 and 1.33, $1.3 \times 10^{-9} \text{ Acm}^{-2}$ and $8.2 \times 10^{-6} \text{ Acm}^{-2}$. For the S.C.S. cell, the corresponding values are for $T=293\text{K}$ and $T=353\text{K}$, 2.26 and 2.05, $3.1 \times 10^{-7} \text{ Acm}^{-2}$ and $6.8 \times 10^{-6} \text{ Acm}^{-2}$.

Fig. 6 $1/C^2 \sim V$ for R.F.
Sputtered I.T.O.

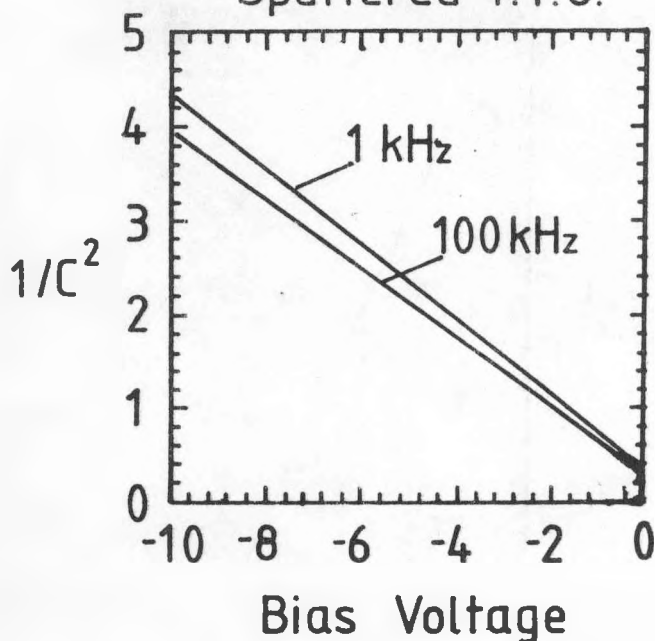


Fig. 6 These data were obtained over the frequency range 1-100kHz at five individual frequencies. Some dispersion is evident. The average value of the built-in voltage is 0.69 eV and the value of $N_A - N_D = 2.5 \times 10^{16} \text{ cm}^{-3}$. The value of the built-in voltage at 120Hz was 0.82 eV. Units are $\text{cm}^4 \text{ farad}^{-2} \times 10^{15}$.

Fig. 8 $1/C^3 \sim V$ for I.B.
Sputtered I.T.O.

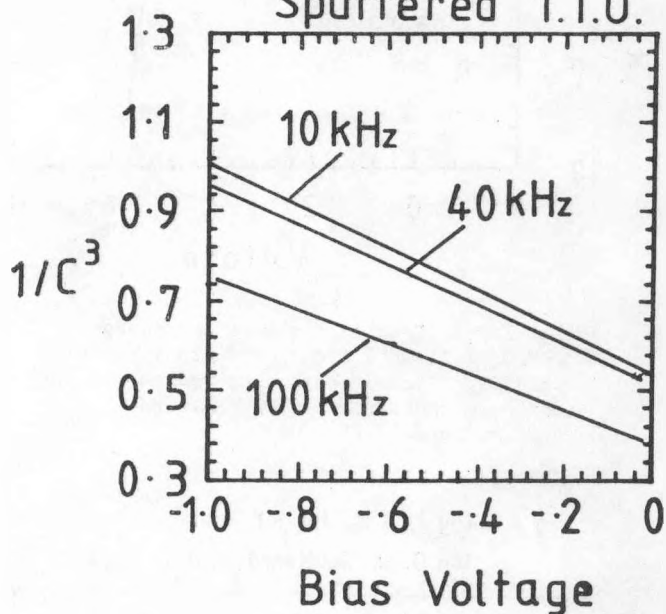


Fig. 7 $1/C^2 \sim V$ for I.B.
Sputtered I.T.O.

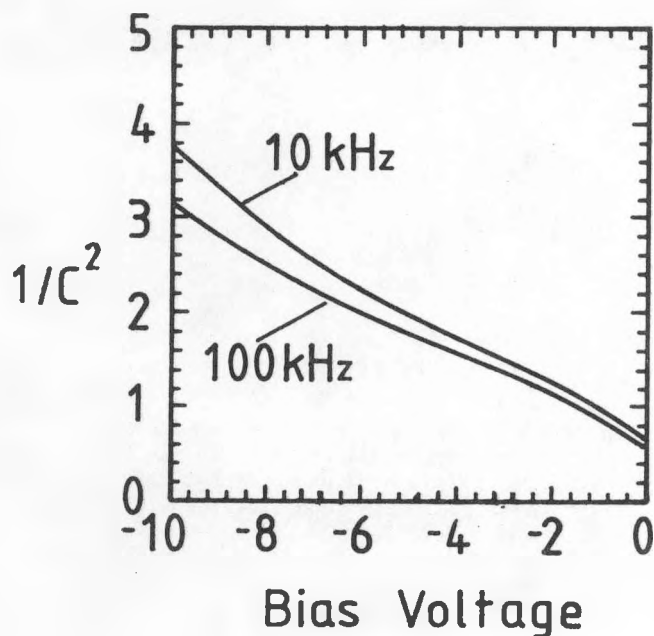


Fig. 8 The values of the built-in potential derived from these plots vary between 0.92-1.15 eV. The units are $\text{cm}^6 \text{ farad}^{-3} \times 10^{21}$.

Fig. 7 The data were obtained over the same range of reverse bias voltage as the M.C.S. cell shown in Fig. 6. On this occasion a graded junction is indicated. The units are $\text{cm}^4 \text{ farad}^{-2} \times 10^{14}$.