SERI/STR-211-2811
(DE85016879)

GaAs SOLAR CELL WITH LOW SURFACE RECOMBINATION

Final Subcontract Report

By
J. R. Shealy
P. A. McDonald
J. L. Benjamin
D. K. Wagner

May 1985

Work Performed Under Contract No. AC02-83CH10093

General Electric Company
Syracuse, New York

and

Solar Energy Research Institute
Golden, Colorado

Technical Information Center
Office of Scientific and Technical Information
United States Department of Energy

DISCLAIMER

This report was prepared as an account of work sponsored by an agency of the United States Government. Neither the United States Government nor any agency thereof, nor any of their employees, makes any warranty, express or implied, or assumes any legal liability or responsibility for the accuracy, completeness, or usefulness of any information, apparatus, product, or process disclosed, or represents that its use would not infringe privately owned rights. Reference herein to any specific commercial product, process, or service by trade name, trademark, manufacturer, or otherwise does not necessarily constitute or imply its endorsement, recommendation, or favoring by the United States Government or any agency thereof. The views and opinions of authors expressed herein do not necessarily state or reflect those of the United States Government or any agency thereof.

This report has been reproduced directly from the best available copy.

Available from the National Technical Information Service, U. S. Department of Commerce, Springfield, Virginia 22161.

Price: Printed Copy A02
Microfiche A01

Codes are used for pricing all publications. The code is determined by the number of pages in the publication. Information pertaining to the pricing codes can be found in the current issues of the following publications, which are generally available in most libraries: *Energy Research Abstracts (ERA); Government Reports Announcements* and Index *(GRA* and I); *Scientific and Technical Abstract Reports (STAR);* and publication NTIS-PR-360 available from NTIS at the above address.

Printed in the United States of America
USDOE Office of Scientific and Technical Information
Oak Ridge, Tennessee

SERI/STR-211-2811
(DE85016879)
Distribution Category UC-63

GaAs Solar Cell with Low Surface Recombination

Final Subcontract Report
May 1985

R. Shealy
P. A. McDonald
J. L. Benjamin
D. K. Wagner

General Electric Company
Power Electronics Semiconductor Dept.
Syracuse, New York

November 1985

Prepared under Subcontract No. XL-4-03032-1
SERI Technical Monitor: R. Mitchell

Solar Energy Research Institute
A Division of Midwest Research Institute

1617 Cole Boulevard
Golden, Colorado 80401

Prepared for the
U.S. Department of Energy
Contract No. DE-AC02-83CH10093

Outline

I. Introduction

II. Solar Cell Structures

- A. Homojunction
- B. Heteroface Solar Cell
- C. Graded Band Gap Cell

III. Si_3N_4 Deposition

IV. Cell Fabrication

- A. Si_3N_4 Process
- B. Al_2O_3 Process

V. Test Results

- A. I-V Under Illumination
- B. Spectral Response
- C. High Energy Illumination

VI. Conclusion

ABSTRACT

The fabrication of large-area solar cells (0.16 cm^2) on GaAs and AlGaAs structures with a new passivating coating, pyrolytic Si_3N_4, is demonstrated. Results in this study illustrate a near-oxide-free interface between GaAs and the Si_3N_4 coatings. These coatings were applied to three solar cell structures, a heteroface AlGaAs/GaAs cell, a graded band-gap AlGaAs cell, and a diffused homojunction cell. The results indicate that the pyrolytic Si_3N_4 coatings improve the surface (high energy) response of homojunction cells; however, they do not perform as well as cells with AlGaAs window layers on the surface. As a result, little improvement in the heteroface solar cell high-energy response was observed in this study. The best solar cells fabricated in this study with Si_3N_4 coatings were heteroface structures whose 1-sun, AMO conversion efficiences were as high as 14.6%.

Abstract

The fabrication of large area solar cells (0.16 cm^2) on GaAs and AlGaAs structures with a new passivating coating, pyrolytic Si_3N_4, is demonstrated. Results in this study illustrate a near oxide free interface between GaAs and the Si_3N_4 coatings. These coatings were applied to three solar cell structures, a heteroface AlGaAs/GaAs cell, a graded bandgap AlGaAs cell, and a diffused homojunction cell. The results indicate that the pyrolytic Si_3N_4 coatings improve the surface (high energy) response of homojunction cells, however they do not perform as well as cells with AlGaAs window layers on the surface. As a result, little improvement in the heteroface solar cell high energy response was observed in this study. The best solar cells fabricated in this study with Si_3N_4 coatings were heteroface structures whose 1 sun, AM0 conversion efficiences were as high as 14.6%.

I. Introduction

Because the high energy response of GaAs solar cells is often dominated by excessive surface recombination, which is presumed to be a consequence of the GaAs-native oxide interface, an attempt to produce a stable oxide free interface with a dielectric coating was made in this program. To achieve this, a pyrolytic Si_3N_4 process was developed for compound semiconductors where the deposition of Si_3N_4 occurs at sufficiently high temperature as to allow the thermal decomposition of the GaAs native oxide prior to the initiation of the deposition. This to our knowledge is the first report of such a high temperature process for GaAs. To evaluate the effectiveness of this coating, comparisons between the Si_3N_4 and evaporated Al_2O_3 were carried out on three device structures, namely a heteroface cell with AlGaAs window, a graded AlGaAs gap cell, and a homojunction cell. The results indicated some success on the surface response enhancement in the case of the homojunction, however, their performance does not rival the heteroface cell which indicates the Si_3N_4 is not as effective as an AlGaAs window.

II. Solar Cell Structures

The solar cell structures were produced, in the case of the homojunction, by Zn diffused (junction depth - 0.6μ), into a lightly doped, 10μ thick LPE layer (n $\sim 2(10^{15}cm^{-3})$. This cell structure was used because of its inherent sensitivity to carrier loss at the surface via surface recombination. This structure was designed such that the junction depth was comparable to the emitter diffusion length to increase the effects of the surface.

The solar cells which contained aluminum in their structures were produced by low pressure Organometallic Vapor Phase Epitaxy (OMVPE)[1]. These structures are illustrated in Figure 1 for the heteroface cell and the graded bandgap cell. The temperatures which appear in the figure are the growth temperatures for the p type emitter and n type base. As shown the base on each of these cells is identical, a 4 μm, $10^{17}cm^{-3}$ Se doped layer. The dopant H_2Se was chosen for the base as we have previously reported longer minority carrier diffusion length in this material as opposed to OMVPE layers doped with SiH_4 [2]. The AlGaAs emitters in each cell were doped with Zn using the Diethylzinc (DEZ) source. Finally, the group V to group III mole ratio was increased during the p type growth to increase the DEZ doping efficiency.

III. Si_3N_4 Deposition

Pyrolytic Si_3N_4 films were chosen in this study because of the potential to thermally remove the native oxide of the alloy on the surface prior to deposition. The deposition was carried out in a commercially available (Applied Materials) low pressure CVD system.

The gases were Dichlorosilane (SiH_2Cl_2) and Ammonia (NH_3) in a volume ratio 4.65:1, respectively. The deposition temperature and pressure was 665°C and 0.38 torr. Under these conditions the deposition rate was approximately 6Å/min. Depositions attempted at lower temperatures resulted in poorly nucleated, porous films with low index of refraction (<1.8).

Because of the high deposition temperature of this Si_3N_4 process compared to other deposition schemes for insulators on compound semiconductors (e.g. sputtering, evaporation, low temperature or plasma assisted CVD), experiments were carried out with lower temperature anneals (600°C) of the GaAs in N_2 prior to deposition. The deposition was initiated by the simultaneous ramping of the temperature to 665°C and introducing the reactants, NH_3 and SiH_2Cl_2.

The results of this process are illustrated by Auger sputter depth profiles shown in Figure 2. The depth resolution in these data was approximately 20Å which is comparable to the observed interface region between GaAs and Si_3N_4. As seen in this figure a relatively large amount of native oxide has been trapped at the interface, indicating the thermal anneal of GaAs under reduced N_2 pressure at 600°C does not effectively remove its native oxide. It is interesting to note that similar temperature treatments in a UHV environment (MBE apparatus) results in the complete removal of the native oxide on a GaAs surface. Attempts to remove the native oxide on GaAs by higher temperature anneals in excess of 600°C resulted in a pronounced surface decomposition of the GaAs prior to deposition. Poor quality, low index of refraction ($n = 1.6$) Si_3N_4 films were obtained when surface decomposition occurred.

Because for this process we demonstrated poor results using thermal annealing techniques in N_2, additional experiments were performed with ammonia gas present during the high temperature anneal (600°C). It was found that the surface decomposition was prevented by the slow formation of GaN at the surface. The Auger depth profile on samples which were annealed in ammonium and N_2 prior to deposition is given in Figure 3. As shown, the ammonia and N_2 anneal is effective at removing the native oxide in addition to preventing surface decomposition of the GaAs. However, a small amount of oxide is detected which corresponds to less than a monolayer of surface coverage. In either case, these interface illustrated in Figure 3 is superior to those obtained with conventional sputtering or plasma enhanced low temperature CVD Si_3N_4[3] unless an Ar sputter preclean step is used to remove the native oxide[3].

With an optimized deposition cycle, the pyrolytic Si_3N_4 films on GaAs have a high index of refraction ($n = 2.05$) and a low etch rate indicating a dense non-porous passivating layer. For example, in a buffered HF etch the pyrolytic Si_3N_4 have typically three orders of magnitude lower etch rate than plasma enhanced CVD films or sputtered films. Finally, the pyrolytic Si_3N_4 films are pinhole free at thicknesses to less than 200Å. As a result we expect the high temperature Si_3N_4 process with ammonia preanneal to produce a stable GaAs/insulator interface with reduced corrosion due to oxidation as a result of the moisture barrier on the GaAs surface.

IV. Cell Fabrication

The solar cell fabrication used in this study consisted of two processes, one incorporating pytolytic Si_3N_4, the other with e-beam evaporated Al_2O_3 coatings. These processes differ because in the case of using the higher temperature Si_3N_4 process, the Si_3N_4 deposition had to occur prior to any metal deposition. These processes are described below.

A. Si_3N_4

The first step in the solar cell device processing was mesa isolation. Device mesas were patterned using an AZ type positive photoresist. The etchant was phosphoric acid, hydrogen peroxide, methanol, and ethylene glycol, mixed 10:1:5:5 by volume. The conditions were a 2.5 minute etch at room temperature. This produced an etch depth of 1.5μ , sufficient to reach the base of the solar cell.

The entire wafer was then passivated by growing a 750Å film of pyrolytic Silicon Nitride, which also serves as an anti-reflection coating on the cell. Electrical contact was made through openings patterned in the nitride layer. This was done, using once again an AZ type positive photoresist to define the openings. The silicon nitride was etched using an O_2/CF_4 plasma (4% O_2 in CF_4). Etch conditions were 150 watts RF power, .7 torr gas pressure, 100°C wafer temperature and an etch time of 1 min. 30 seconds. Following this, for SC-458, the AlGaAs window layer was removed using a brief (5 sec.) etch made of H_3PO_4, H_2O_2:Ethylene Glycol:Methanol, mixed 50:1:25:25. The other wafers did not require this etch since they did not have window layers. Next the wafers were zinc diffused selectively through the small openings in the Si_3N_4 to produce low resistance contacts. The diffusion was carried out in an N_2 ambient at 650°C for 15 minutes using $ZnAs_2$ and InAs sources[4].

After zinc diffusion the p contact metallization pattern was applied using a standard liftoff technique. The p side metal consisted of 500Å Titanium, 500Å of platinum, and 1500Å gold. The wafers were then thinned to about 10 mils, after which the N side metallization was applied. This consisted of 500Å-Germanium, 1500Å gold, 1000Å tungsten and 5000Å gold. The metal contacts were sintered in an H_2 ambient at 415°C for 10 minutes. The wafers were scribed into individual devices for testing.

B. Al_2O_3 Process

The Al_2O_3 passivated devices were fabricated in a significantly different manner. The first step is the electrode finger pattern formation. This was done with photolithography and processed as a metal liftoff step. For epitaxial structures having an AlGaAs window layer, this had to be removed for proper metal contact. The AlGaAs was anodized by an etch of $NH_4OH:H_2O_2:H_2O$ mixed 1:2:161. This left a blue film of Al_2O_3. This was etched away with $HCl:H_2O$ mixed 1:3. This process was repeated until the window was removed. Following this the p contact metallization was applied. This consisted of 200Å Silver/50Å Manganese and 2000Å Silver. Then the backside metal was applied and the wafer sintered at 420°C for one minute. The wafer was repatterned with the finger pattern and 2μ of Ag was electrolytically plated on.

Then the devices were isolated by a mesa etch consisting of phosphoric acid, methanol, hydrogen peroxide mixed 1:3:1. The wafers were etched 2 min. at 20°C; this produced a 3μ mesa height. Next a 800Å Al_2O_3 antireflection coating was then E-Beam evaporated over the wafer surface. Holes were etched for electrical contact with the underlying metallization. This was done with a 1:1 mix of phosphoric acid in water, warmed to 75°C. Finally 2 micron of additional Silver was electrically plated onto the contacts.

V. Test Results

The solar cells were evaluated using the following techniques: illuminated I-V measurements at 1 sun, high energy illumination using Ar^+ laser, and spectral response measurement (low intensity). Electrical measurements including capacitance-voltage and conductance-voltage were done on different area diodes, however, no discernible differences on cells fabricated with the Si_3N_4 coating and without were evident with this data. In both processes the forward bias conductance-voltage relationships yield diode ideality factors consistently less than 2.0 (typically 1.5).

A. I-V Under Illumination

Comparison of the solar cell processes and structures were made under AMO, 1 sun illumination on 4 X 4 mm^2 devices. Smaller area devices with less complicated metal patterns consistently gave higher open circuit voltages and fill factors than those appearing in the data below. However, the data given in Figure 4 illustrates the performance of the large area cells can be satisfactory with AM0, 1 sun efficiencies approaching 17%. The maximum power point is shown in the figure by the cross hair, corresponding to a current of approximately 4 ma at 0.85 volts. The cells fill factor, open circuit voltage, and short circuit current are also given in the figure. Additional data taken under AM1 conditions of the solar cells delivered to SERI in this program appear in Figure 5.

The data in Figure 4 was taken on a cell fabricated with the Al_2O_3 process. Comparison of the cell structures process with Si_3N_4 and Al_2O_3 is given in Table I. The heteroface solar cells show little difference in performance with the two processes. Notable of the Si_3N_4 process is a larger short circuit current which is attributed to the better Si_3N_4 AR coating. The spectral response of the heteroface cells of either process were identical. The efficiency is somewhat higher in the Al_2O_3 process because of a lower fill factor and open circuit voltage seen in the Si_3N_4 coated cell. The origin of this reduced performance has not been determined.

The graded bandgap cells processing differed in that the Si_3N_4 process failed to remove the GaAs contact layer under the Si_3N_4 coating. This 2000Å thick absorbing layer reduced the high energy response of the cell considerably as reflected in the difference in short circuit current of the graded gap cell with the two processes. Even with Al_2O_3 process the graded gap cells' performance is inferior to the heteroface cell as we have previously reported[4].

The Zn diffused homojunction cells show comparable performance with both processes with a moderate enhancement of the high energy response on device coated with Si_3N_4. This improvement increased the short circuit curerent by 20%. However the diffusion lengths in the p^+ diffused region are sufficiently small to limit the collection of carriers near the surface. It is expected that shallower diffusions would improve the homojunction cells' performance and more clearly illustrate the enhanced surface response of homojunction cells coated with Si_3N_4.

B. Spectral Response

The spectral response of the three solar cell structures coated with Si_3N_4 are given in Figure 6. As previously mentioned, the heteroface cells' spectral response is essential identical for cells fabriated by either process. Hence, the pyrolytic Si_3N_4 process does not improve the high energy response of the cells with AlGaAs on the surface. The ammonia heat treatment prior to the deposition of Si_3N_4 apparently does not remove a native oxide on an AlGaAs surface. The high energy response of the graded bandgap and Zn diffused homojunction cells is essentially the same which indicates little carrier collection occurs in the emitter of these cells. However, at 450 nm, for example, the homojunction cells response was improved from .07 to 0.12 in quantum effficiency as a result of the Si_3N_4 coatings. This gives some indication of an improvement in carrier collection near the homojunction cell's surface with the Si_3N_4 process.

C. High Energy Illumination

The Blue response of the Si_3N_4 heteroface solar cell was measured using laser lines from an Ar^+ laser. The 501.7 nm, and 457.9 nm wavelengths were chosen to provide illumination intensities somewhat greater than one sun. The light passed through a variable attenuator that provided a 20:1 range of intensities. The illumination intensity was measured directly with a calorimeter type power meter. The intensity was further checked by illuminating a calibrated solar cell. The results are shown in Figure 7.

The short circuit current versus intensity was measured at several power levels using the variable attenuator. The response is seen to be essentially linear over the power range employed.

As a result, no improvement in high energy response of the heteroface cell is obtained at larger illumination intensities. These data suggest that the low quantum efficiency observed at higher energies is unrelated to the cell's surface, where a saturation of the carrier loss at the surface through interface states would be expected at some high illumination intensity.

VI. Conclusion

To summarize, a high temperature Si_3N_4 process was developed and applied to several solar cell structures. It was found that an ammonia bake at 600°C prior to the Si_3N_4 deposition prevents surface decomposition and removes the GaAs native oxide. This process when applied to AlGaAs heteroface cells results in little improvement of the cells performance. But it should be noted that the Si_3N_4 coatings do have passivating properties around the diodes periphery. This is clearly observable after moderate heat treatments (~400°C) are used to package the solar cells. The Si_3N_4 coated devices consistently showed less degradation during packaging than cells fabricated with Al_2O_3. Finally, with this new Si_3N_4 process, we demonstrate an improved high energy response of Zn diffused homojunction cells which indicated a reduction in surface recombination at the Si_3N_4/GaAs interface.

References

1) "Graded Band-Gap AlGaAs Solar Cells Grown by MOVPE", D. K. Wagner and J. R. Shealy, J. of Crystal Growth 68 (1984), p 474-476.

2) "Graded Band-Gap P/N AlGaAs Solar Cells Grown by OMVPE", D. K. Wagner and J. R. Shealy, Applied Phys. Lett., 45 (2) 162-164 (July 1984).

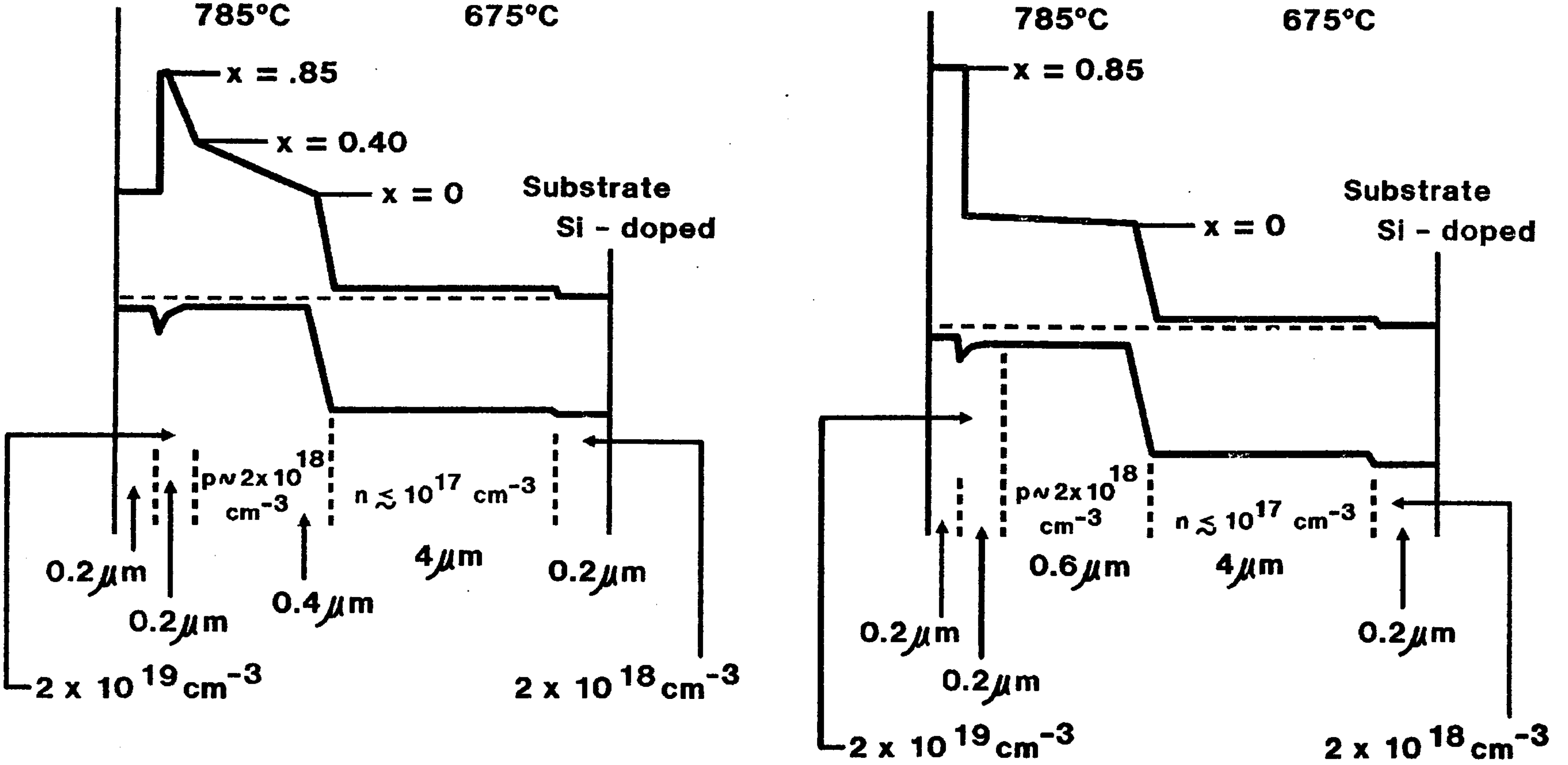
3) "Silicon Nitride Film Deposition by Hot-Wall Plasma-Enhanced CVD for GaAs LSI", Yasunobu Ishii, Tatsuo Aoki, and Shintaro Miyazawa, J. Vac. Sci. Technol. B2, 1 (1984), p 49-53.

4) "Graded Band-Gap AlGaAs Solar Cells Grown by Organometallic Vapor Phase Epitaxy", D. K. Wagner and J. R. Shealy, Proc. 7th IEEE Photovoltaic Specialists Conf., (May 1-4, 1984).

	I_{SC} (A/cm^2)	V_{oc} (Volts)	Fill Factor	η(AMO)
Heteroface Cell-SC 458				
Si_3N_4	29.5	0.95	0.70	14.6%
Al_2O_3	28.9	0.98	0.80	16.6%
Graded Bandgap Cell-SC 457				
Si_3N_4	14.5	0.78	0.76	8.6%
Al_2O_3	19.0	0.97	0.77	10.6%
Zn Diffused/LPE-L11				
Si_3N_4	15.0	0.63	0.74	5.4%
Al_2O_3	12.0	0.65	0.75	4.7%

Table I Comparison of Solar Cells Fabricated With Pyrolytic Si_3N_4 and Evaporated Al_2O_3 Coatings Under AM0, 1 Sun Illumination

FIGURE 1



SC457 Graded Band-Gap Cell

SC458 Heteroface Cell

FIGURE 2

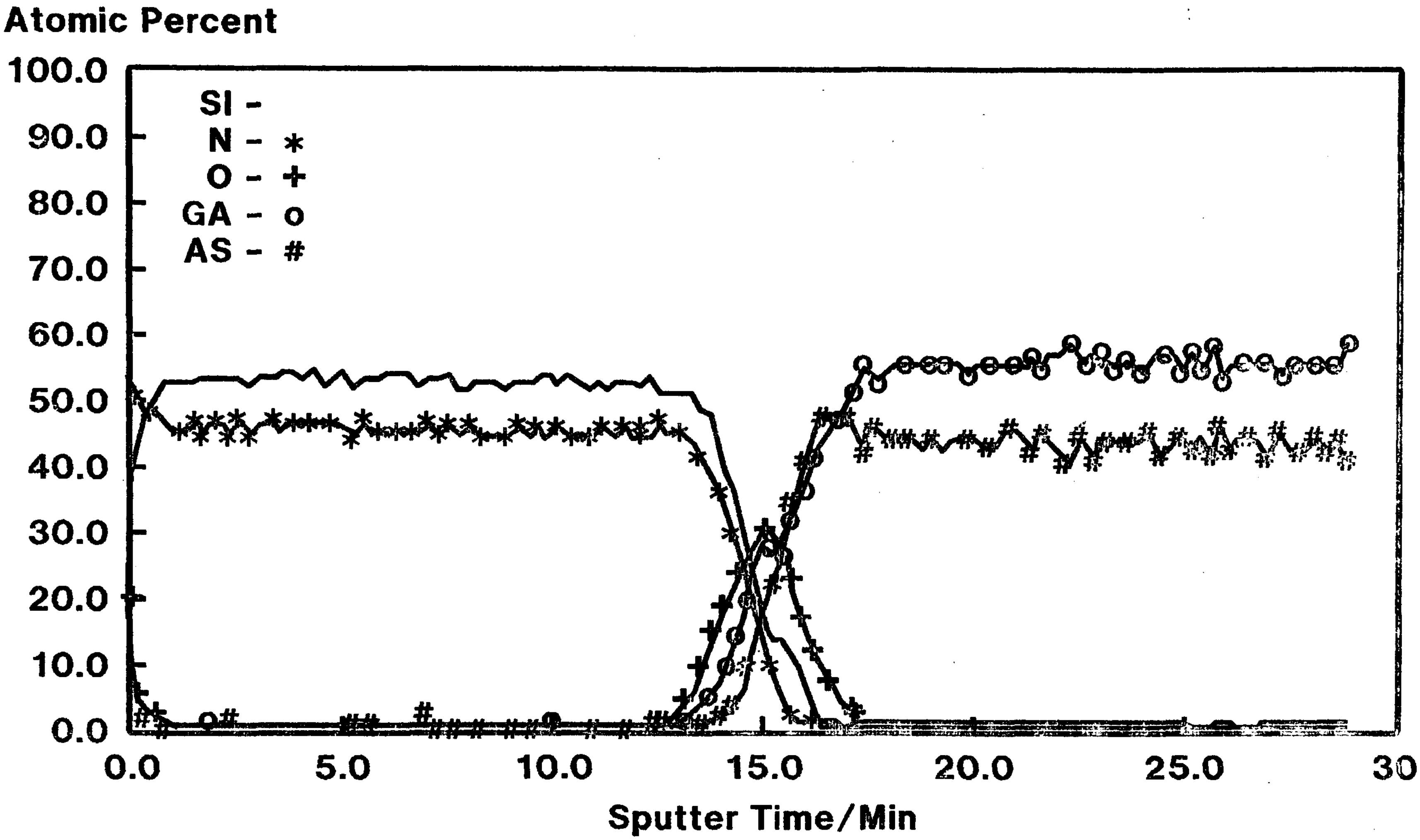

Atomic Percent
100.0
90.0
80.0
70.0
60.0
50.0
40.0
30.0
20.0
10.0
0.0
SI -
N - *
O - +
GA - o
AS - #
0.0
5.0
10.0
15.0
20.0
25.0
30
Sputter Time/Min

FIGURE 3

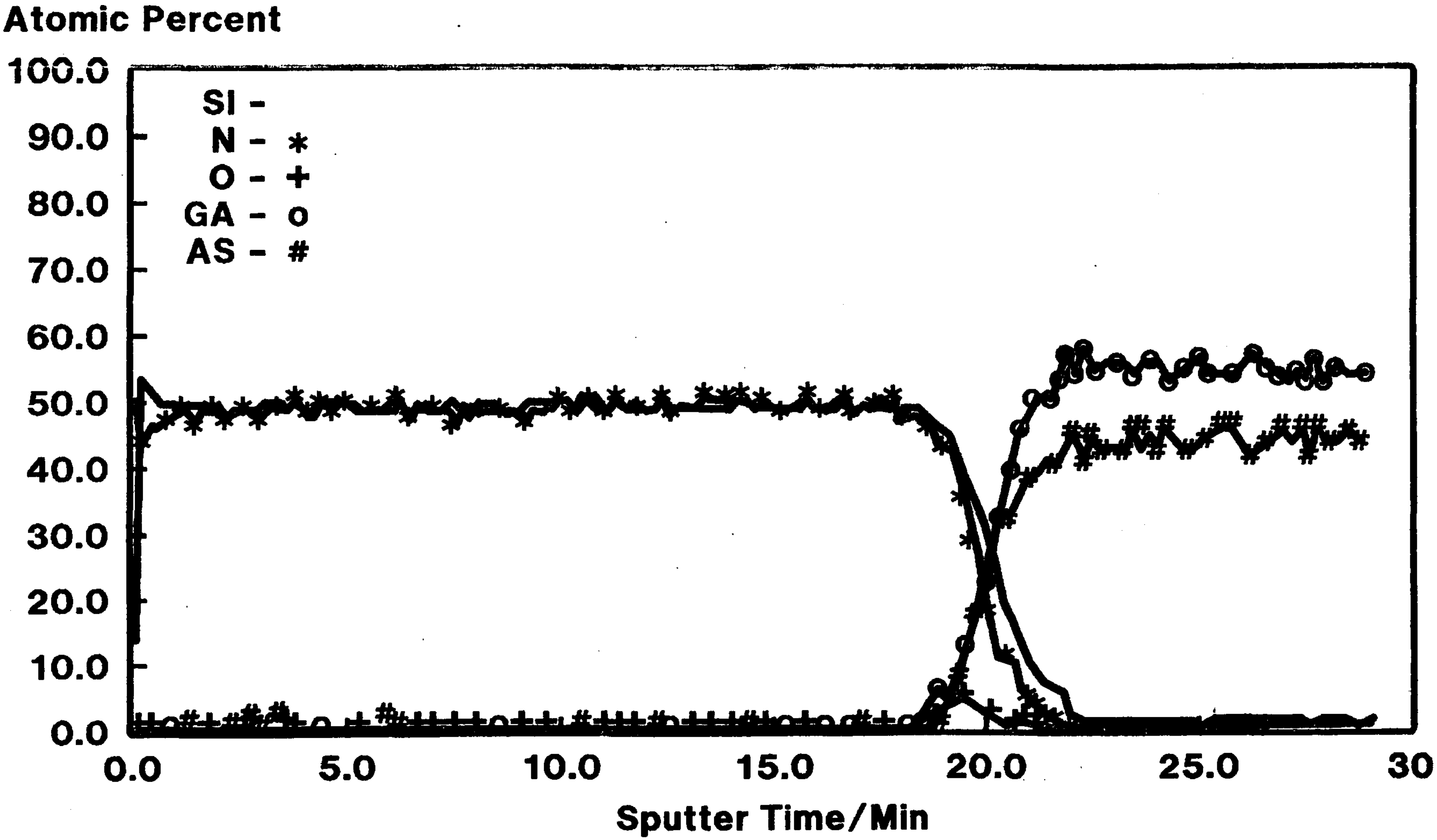
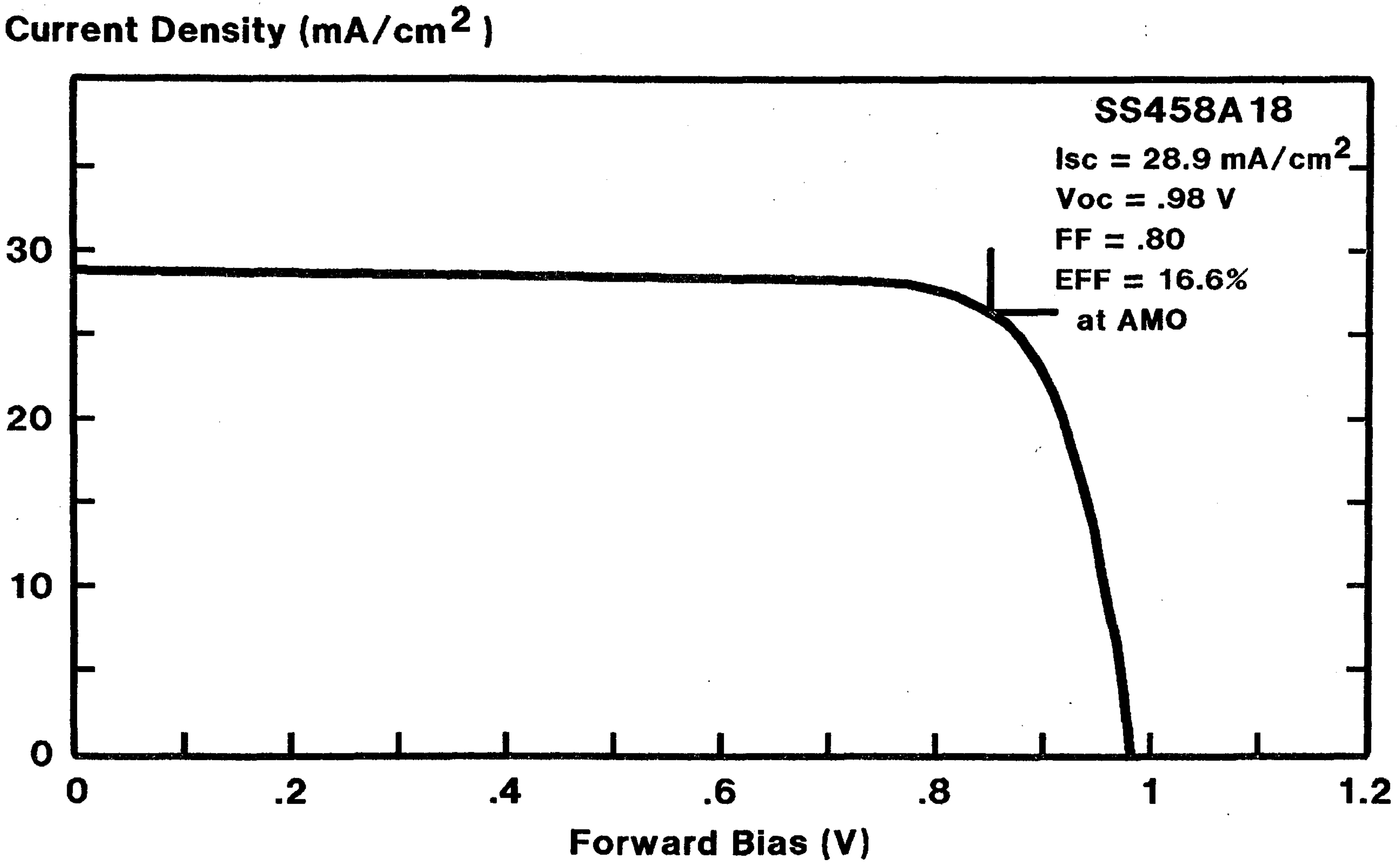
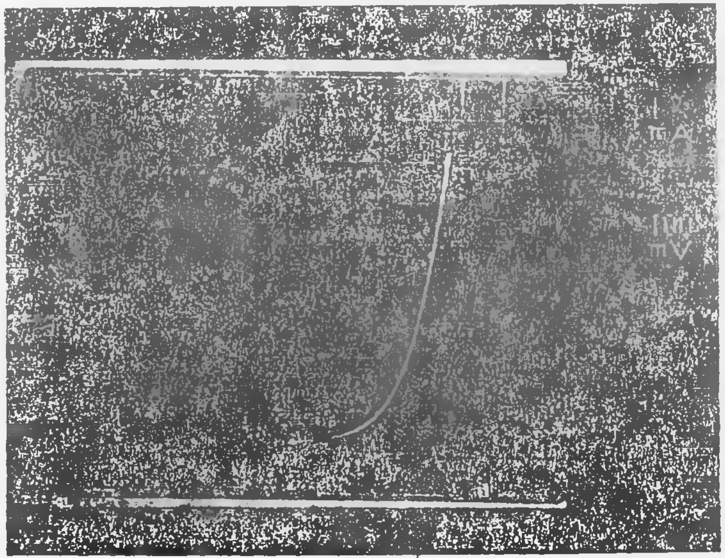

Atomic Percent
100.0
90.0
80.0
70.0
60.0
50.0
40.0
30.0
20.0
10.0
0.0
SI -
N - *
O - +
GA - o
AS - #
0.0
5.0
10.0
15.0
20.0
25.0
30
Sputter Time/Min

FIGURE 4

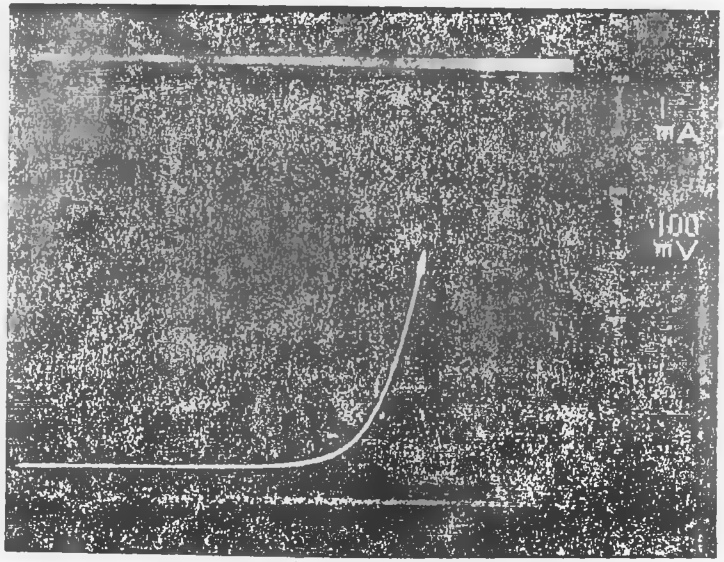

Current Density (mA/cm2)
SS458A18
Isc = 28.9 mA/cm2
Voc = .98 V
FF = .80
EFF = 16.6%
at AMO
30
20
10
0
0
.2
.4
.6
.8
1
1.2
Forward Bias (V)

HETEROFACE CELL

Figure 5A



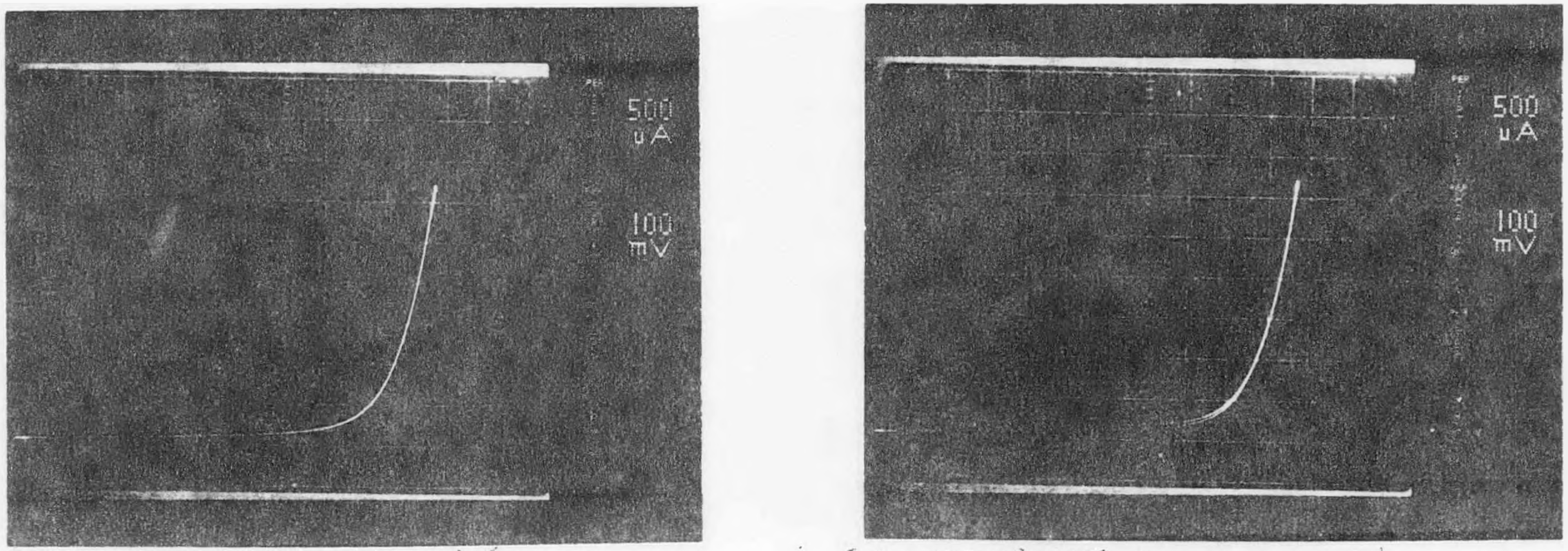
SC-458-1 4-19-85



SC-454-1

GRADED BANDGAP CELL

Figure 5B

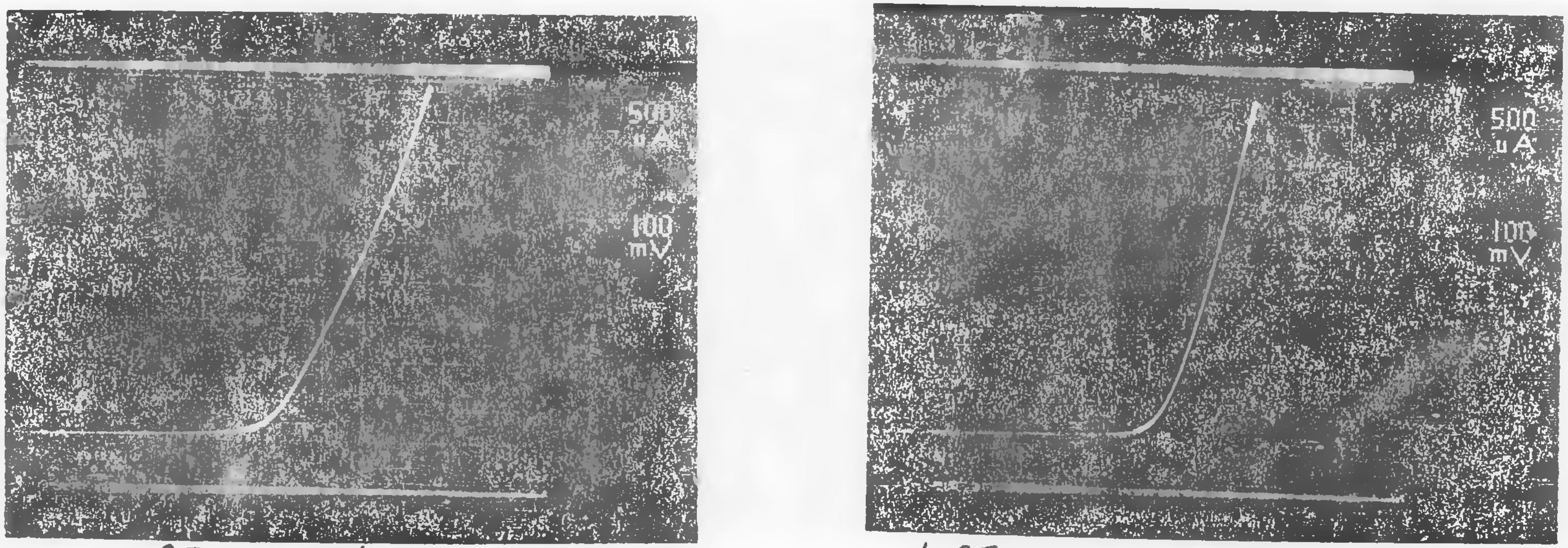


SC-457-13-2 4-19-85

SC-157031985-9 7 19-85

HOMOJUNCTION CELL

Figure 5C



LPE-L11-4

LPE-L11-2

FIGURE 6

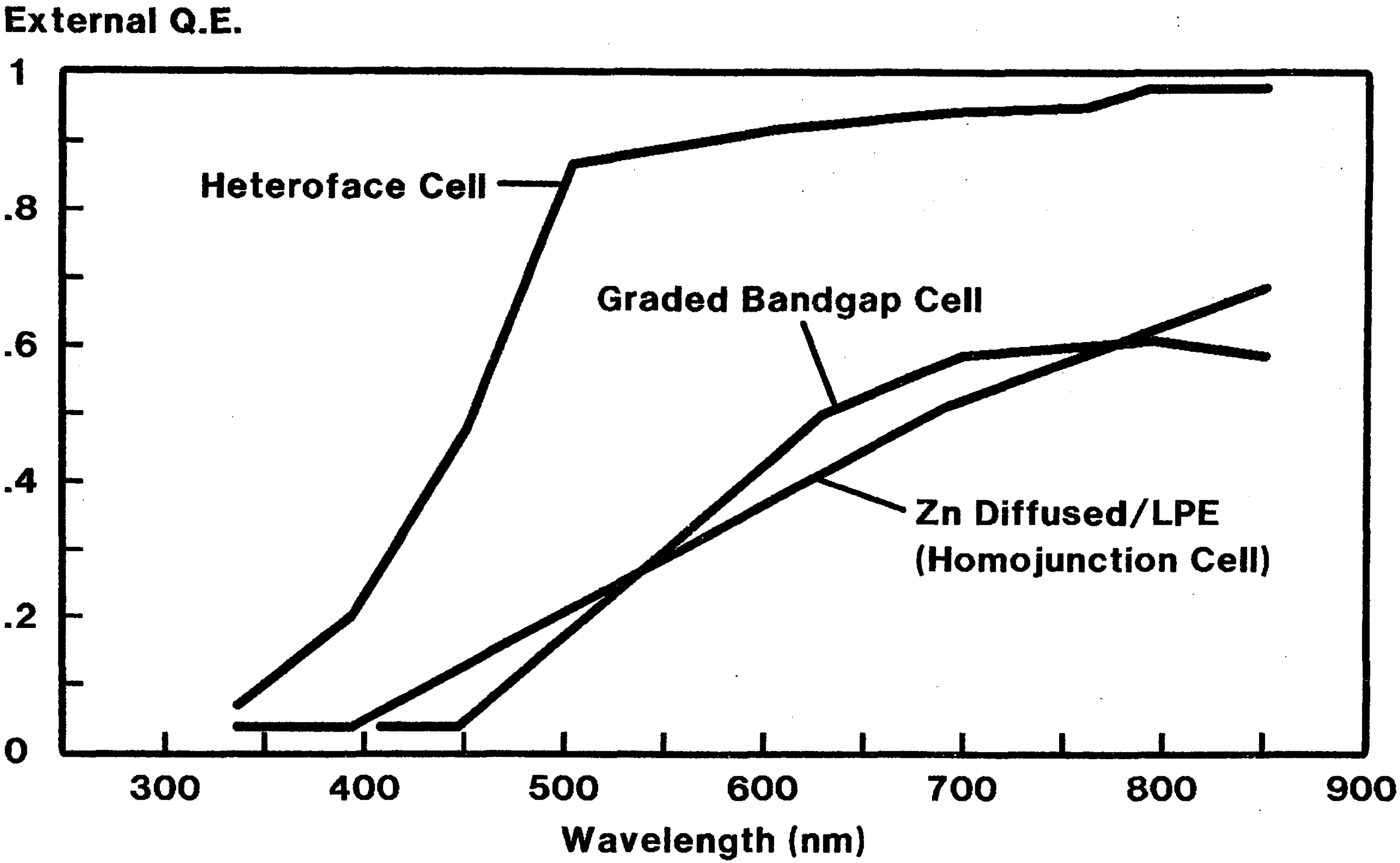

External Q.E.
1
.8
.6
.4
.2
0
Heteroface Cell
Graded Bandgap Cell
Zn Diffused/LPE
(Homojunction Cell)
300
400
500
600
700
800
900
Wavelength (nm)

FIGURE 7

Short Circuit Current Vs. Incident Light Intensity