SERI/TR-8021-1-T1
(DE83000997)

CADMIUM SULFIDE/COPPER TERNARY HETEROJUNCTION CELL RESEARCH

Final Report for the Period April 1, 1980—August 25, 1982

By
R. A. Mickelsen
Wen S. Chen

August 1982

Work Performed Under Contract No. AC02-77CH00178

Boeing Aerospace Company
Seattle, Washington

U.S. Department of Energy

Solar Energy

DISCLAIMER

DISCLAIMER

SERI/TR-8021-1-T1
(DE83000997)
Distribution Category UC-63

CADMIUM SULFIDE/COPPER TERNARY HETEROJUNCTION CELL RESEARCH

R. A. Mickelsen and Wen S. Chen
L. F. Buldhaupt, Program Manager

Final Report
April 1, 1980 - August 25, 1982

August 1982

Contract No. XJ-9-8021-1

Prepared For: Solar Energy Research Institute

Boeing Aerospace Company
P.O. Box 3999 MS 88-43
Seattle, Washington 98124

ABSTRACT

The properties of polycrystalline, thin-film $CuInSe_2/CdS$ and $CuInSe_2/Zn_xCd_{1-x}S$ solar cells prepared by vacuum evaporation techniques onto metallized alumina substrates are described. An efficiency of 10.6% for a 1 cm^2 area cell and 8.3% for an 8 cm^2 cell when tested under simulated AM1 illumination is reported. The mixed sulfide cells are described as exhibiting increased open circuit voltages, slightly higher short circuit currents, and improved efficiencies. Mixed sulfide film preparation by evaporation of CdS and ZnS powders from a single source and from two sources is discussed with preference given to the later technique. Selenide film preparation in a planetary or rotating substrate vacuum deposition apparatus is described. A 1 cm^2 area cell without AR-coating produced by the planetary approach is reported to demonstrate a 7.5% efficiency. The results of cell heat-treatment studies showing a strong environmental dependence are presented and indicate the desirability of an oxygen containing atmosphere. An automatic, computer controlled, cell measurement system for I-V, C-V, and spectral response analysis is described. The results of the cell analysis and cell modeling studies on both the plain CdS and mixed $Zn_xCd_{1-x}S$ thin-film devices are presented. Finally, data obtained from constant illumination and elevated temperature life-tests on the thin-film cells showing little degradation after 9300 hours is reported.

TABLE OF CONTENTS

LIST OF TABLES AND FIGURES

1.0 SUMMARY

This is the Final Report of a research program entitled "Cadmium Sulfide/Copper Ternary Heterojunction Cell Research" and covers the period April 1, 1980 - August 25, 1982. The work was supported under SERI Contract XJ-9-8021-1. Primary objectives of the program were the achievement of a stable, polycrystalline, thin-film photovoltaic solar cell based upon the CdS/CuInSe2 material system with an efficiency greater than 10%. These objectives have been successfully met. A 1 cm^2 area cell has been produced with an efficiency of 10.6% and a 9300 hour accelerated life-test has demonstrated excellent resistance of the $CuInSe_2$ thin-film cells to degradation.

While the basic cell structure was little changed from earlier devices, refinements to the design and film deposition processes were made during the course of the program and resulted in a gradual improvement in cell performance. Included in these cell advancements was a simpler, more transparent grid structure with an off-cell contact pad to avoid probe shadowing errors during cell testing. Due to a surface contaminate layer, problems were encountered with the adherence and stability of the aluminum grid contact but were resolved by the application of a brief sputter etch and glow discharge cleaning process.

All of the thin-film cells were fabricated with the two-layer selenide deposition process. Usually, the first, low resistivity layer was deposited at 350°C while the second, high resistivity layer was prepared at a 450°C substrate temperature. The transition between the two layers was accomplished by a 25-30% reduction in the copper deposition rate. The selenide preparation was monitored by post-deposition, hot-probe and resistivity measurements on the individual and composite layers. These measurements indicated extensive film interdiffusion, an apparent semiconductor type conversion (N to P), and an optimum resistivity range for maximum cell response.

An effective anti-reflection coating was prepared by vacuum evaporation of SiO in an oxygen partial pressure. These ~ 1000 Å thick SiO_x films resulted in a ~ 10% improvement in short circuit current and efficiency. Very stable and adherent oxide layers were achieved by cleaning the cells with vapor degreasing and glow discharge techniques and adjusting the SiO vapor source temperature.

A theoretically predicted voltage increase with the use of mixed $Zn_xCd_{1-x}S$ films was verified by fabricating cells with vacuum evaporated mixed sulfide layers. An open circuit voltage in excess of 430 mV was achieved for a Zn content of 20%(x = 0.2). Two methods were used for the mixed sulfide preparation, i.e., evaporation of the ZnS and CdS powders from a single graphite source containing composition controlling apertures and, secondly, two independently heated sources. The later technique was found preferable in terms of reproducibility, control, and film resistivity. As in the case of the plain CdS films, the final two-thirds of the mixed sulfide layer were doped with indium by co-evaporation.

The preparation of $CuInSe_2$ films by simultaneous elemental evaporation in a planetary or rotating substrate deposition apparatus was investigated for the purpose of allowing the future fabrication of a large quantity of small (1 cm^2) cells or very large area cells (25-100 cm^2). Serious experimental problems were encountered due to the requirement of high deposition temperatures and the presence of the high vapor pressure selenium material. These problems necessitated modifying the film deposition parameters as used in the standard, fixed substrate apparatus in order to produce selenide films with the desired electrical, compositional, and structural properties. With these modifications, a 1 cm^2 area non-AR coated cell achieved an efficiency of 7.5% under simulated AM1 illumination. While this high efficiency demonstrated the successful development of the planetary concept, the not easily resolvable experimental problems may severely limit the planned application of the method.

A number of cell heat treatment studies were conducted on non-AR coated, thin-film $CuInSe_2$/CdS and -$Zn_xCd_{1-x}S$ cells. These studies showed that the cell performance was significantly improved by heat treating for 10-60 minutes at 200-225^oC providing the bake environment contained oxygen. The effects of the heat treatment were also found to be non-reversible, e.g., baking in hydrogen did not return the cells to the unbaked condition. I-V, C-V, and spectral response measurements were used to monitor the cells response to heat treatment. It was found that the V_{OC}, F.F., I_{SC}, efficiency, and carrier density increased substantially but the R_S, A, I_O, depletion widths and depth from the junction decreased after even a short, 10 minute oxygen bake. In contrast, a hydrogen bake essentially resulted in only an increase in I_{SC} with the other cell parameters being little changed. In agreement with the increase in I_{SC}, the level of the spectral response curve (quantum efficiency) was shifted upward by heat treatment but did not change in shape.

An automatic, computer controlled system for light and dark I-V, C-V, and spectral response measurements on the thin-film cells was developed. This equipment greatly reduced the time for cell characterization, improved the measurement accuracy, and expanded the capability for cell analysis. The system was programmed to determine all of the important photovoltaic and capacitance parameters for the cell and diode structures. In the spectral response mode, the system was constructed to provide such parameters as spectral responsivity and quantum yield over the wavelength range from 440 nm to 1800 nm. After its development, the automatic system was extensively used for detailed cell characterization and modeling, determining the effects of cell processing variations which include the mixed sulfide layers, selenide deposition temperature, sulfide resistivity, and AR coatings, comparison of test results under different illumination conditions and for different laboratories, and cell life-testing. The spectral response measurements showed, for example, the expected wavelength drop-off at ~ 1200 nm corresponding to the selenide band-gap and the short wavelength cut-off at ~ 500 nm due to the sulfide absorption but, in addition, optical effects around 960 nm which correlated to a possible transition from the spin-orbit valence band to the lowest conduction band in $CuInSe_2$. The anticipated downward shift of the short wavelength cut-off for the mixed sulfide cells was also experimentally observed.

One unexpected result of the cell analysis activity was the finding of non-ohnic behavior at the selenide/molybdenum back contact. The effect was first detected by EBIC measurements on cell cross-sections conducted at SERI. Although a tentative correlation to some unusual cell characteristics could be made, it has not yet been established as to whether the contact is actually limiting cell performance. A series of metallization substitutes for molybdenum were briefly studied but none were found acceptable.

The stability of the thin-film $CuInSe_2$ cells was examined by conducting constant illumination (simulated AM1) life-tests. Non-AR coated or encapsulated cells were tested in an open laboratory environment and included varying cell loading and temperature conditions. After resolving a problem with the grid/CdS contact, the first test series was at 21°C for 500 hours with the three cells at the open circuit condition. Next, the test temperature was increased to 60°C and ran for ~ 1000 hours. For the third test in the test series, also at 60°C, two of the cells were connected with a 12 ohm load to approximate maximum power loading and the third cell was left

open-circuited. This test covered nearly 4200 hours. For the fourth and final test, the temperature was increased again to 80°C and was concluded after ~ 3600 hours. With an accumulated total of ~ 9300 hours of severe, accelerated aging, little degradation in the three photovoltaic parameters of V_{oc}, I_{sc}, and FF was detectable. Some decrease in FF after several thousand hours at 80°C was observed but was believed to have been caused by mechanical abuse.

2.0 INTRODUCTION

This is the final report of work on "Cadmium Sulfide/Copper Ternary Heterojunction Cell Research," SERI contract XJ-9-8021-1. The copper ternary is the semiconductor compound copper indium diselenide ($CuInSe_2$) and was the subject of three prior research programs (1, 2, 9). For the current program, the objective was to continue the development of a large area, low cost, stable polycrystalline thin-film photovoltaic solar cell based upon the $CdS/CuInSe_2$ material system. The program was directed towards achieving, at the earliest possible time, a 10% efficient thin-film cell on low cost substrates by low cost fabrication methods. Accordingly, the technical approach was to improve the performance and fabrication economics of earlier developed cells produced by vacuum evaporation techniques (simultaneous elemental evaporation for $CuInSe_2$) onto inexpensive substrates. The specific research tasks included: (1) Improving design features in the basic cell structure; (2) Exploring modified CdS materials; (3) Conducting detailed cell analysis and modeling; (4) Determining the effects of cell heat treatments; (5) Conducting constant illumination life testing on a small number of high efficiency cells; and (6) Developing processes for large area cell fabrication.

The first reported experimental example of a $CdS/CuInSe_2$ heterojunction solar cell was fabricated using a single crystal of $CuInSe_2$ and a vacuum deposited CdS film (3-5). This single crystal device exhibited a uniform photovoltaic quantum efficiency of 70% between wavelengths of 0.55 to 1.25 microns. For an incident solar intensity of 92 mW/cm^2, the device produced a photocurrent of 38 mA/cm^2, an open circuit voltage of 0.49 V, and a conversion efficiency of 12%. Other than the Si, GaAs, $Cu_2S/CdZnS$ and InP/CdS semiconductor systems, this is the only case of a solid state photovoltaic device with a demonstrated efficiency greater than 10%.

Following the development of a single crystal cell, polycrystalline thin-film cells were prepared using vacuum evaporation techniques for both the CdS and $CuInSe_2$ layers (6-8). The $CuInSe_2$ films used in the cells were formed by codeposition of the $CuInSe_2$ and Se in order to form controlled resistivity P-type layers.

These cells have shown photocurrents of 28 mA/cm^2 open circuit voltages of 0.49 V, and efficiencies of 6.6% when tested with a light intensity of 100 mW/cm^2. The cells

have been approximately 1 cm^2 in area and have not been coated with any anti-reflection layers.

As established in a previous study, the elemental evaporation process for the selenide film formation is believed to possess a number of favorable features, including semiconductor film quality and suitability for scale up to high volume production (2). It is the approach Boeing has taken to further the development of this attractive thin-film solar cell. By utilizing these films to fabricate solar cell devices, a cell efficiency of 10% has been achieved. Cell performance of this magnitude is viewed as being very encouraging and is also felt to provide an indication regarding the future potential of the planned technical approach.

3.0 TECHNICAL DISCUSSION

3.1 Base Cell Fabrication and Improvement

The structure of the base $CuInSe_2$/Cds thin-film solar cell remained essentially unchanged during the course of the program and is shown in cross-section without an AR-coating in Figure 3.1-1. Studies and slight variations were made, however, as the program progressed which were directed towards improving the cell performance. A detailed description of the cell fabrication process and the improvements will be presented in this report section.

The flow process for cell fabrication was as follows: (1) Substrate cleaning; (2) Base metallization deposition; (3) $CuInSe_2$ deposition; (4) CdS deposition; (5) Grid contact deposition; (6) Photolithographic definition of the individual cells on the substrate; (7) Dicing the substrate to separate the cells; (8) Cell heat treatment; and (9) AR-coating deposition.

In order to simplify the dicing operation, the 2" x 2" x 0.025" polycrystalline alumina substrates (MRC Superstrates) were first laser scored on the back side. The substrates were then cleaned in a heated detergent solution (Alconox), rinsed in hot water and cold DI water, and finally, blown dry with high purity nitrogen gas.

The base metallization was applied by RF sputtering of Mo in Ar. Deposition time was 60 minutes and produced a Mo film with a ~ 1.5_{μ}m thickness and a sheet resistivity of ~ 150 m$\Omega/\square$. A strip approximately 0.5" wide was masked off to allow electrical measurements on the selenide and sulfide layers. Following the Mo deposition, the substrates were stored in a desiccator until needed for cell fabrication.

Selenide and sulfide film depositions were made in the same vacuum evaporation chamber without breaking vacuum between the two deposits. The chamber was a conventional liquid nitrogen trapped, diffusion pumped system with a stainless steel bell-jar. The deposition apparatus for the selenide film preparation (Figure 3.1-2) and the film deposition controllers (EIES for Cu and In and a quartz crystal for Se) were as described in a previous report (9). Minor modifications were made to the apparatus as shown in Figure 3.1-3 to include two, independently powered In boats and only a single Se boat.

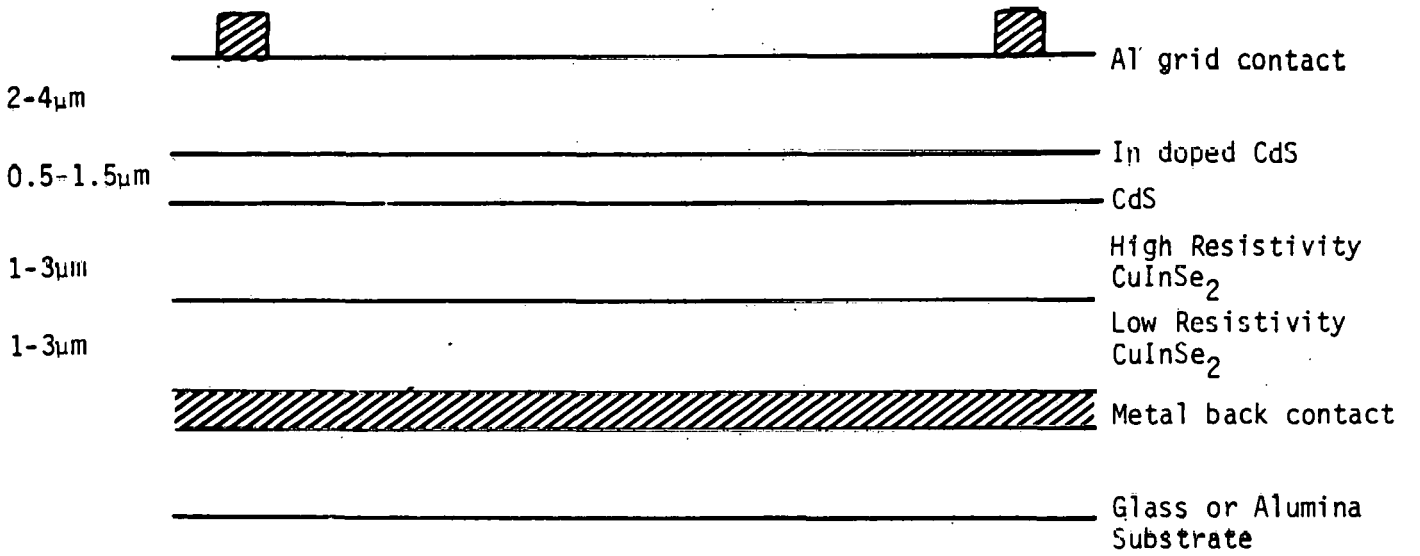


Figure 3.1-1 $CdS/CuInSe_2$ Cell Structure

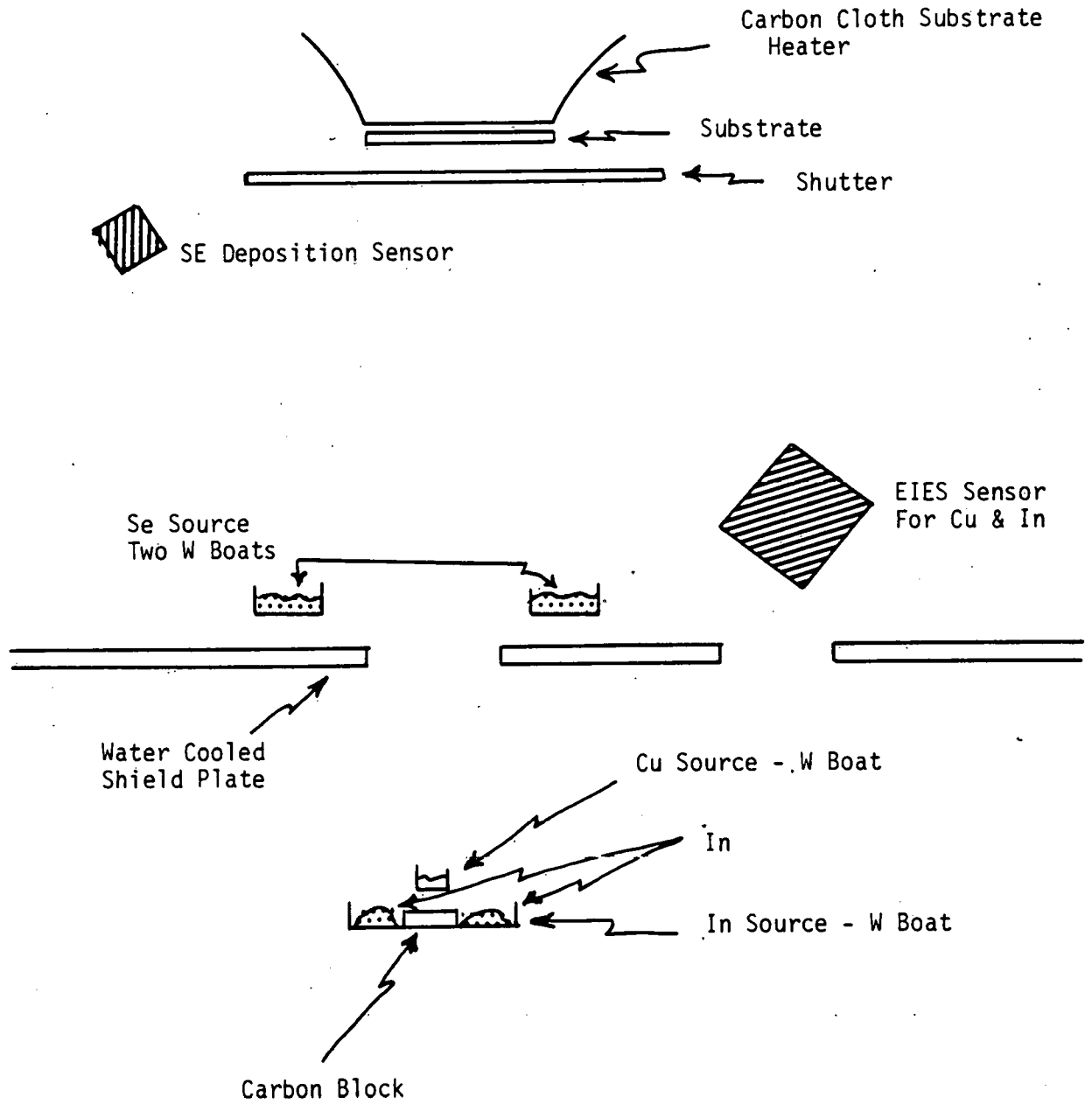


Figure 3.1-2. System Configuration for Preparing $CuInSe_2$ Films Using EIES Deposition Controller

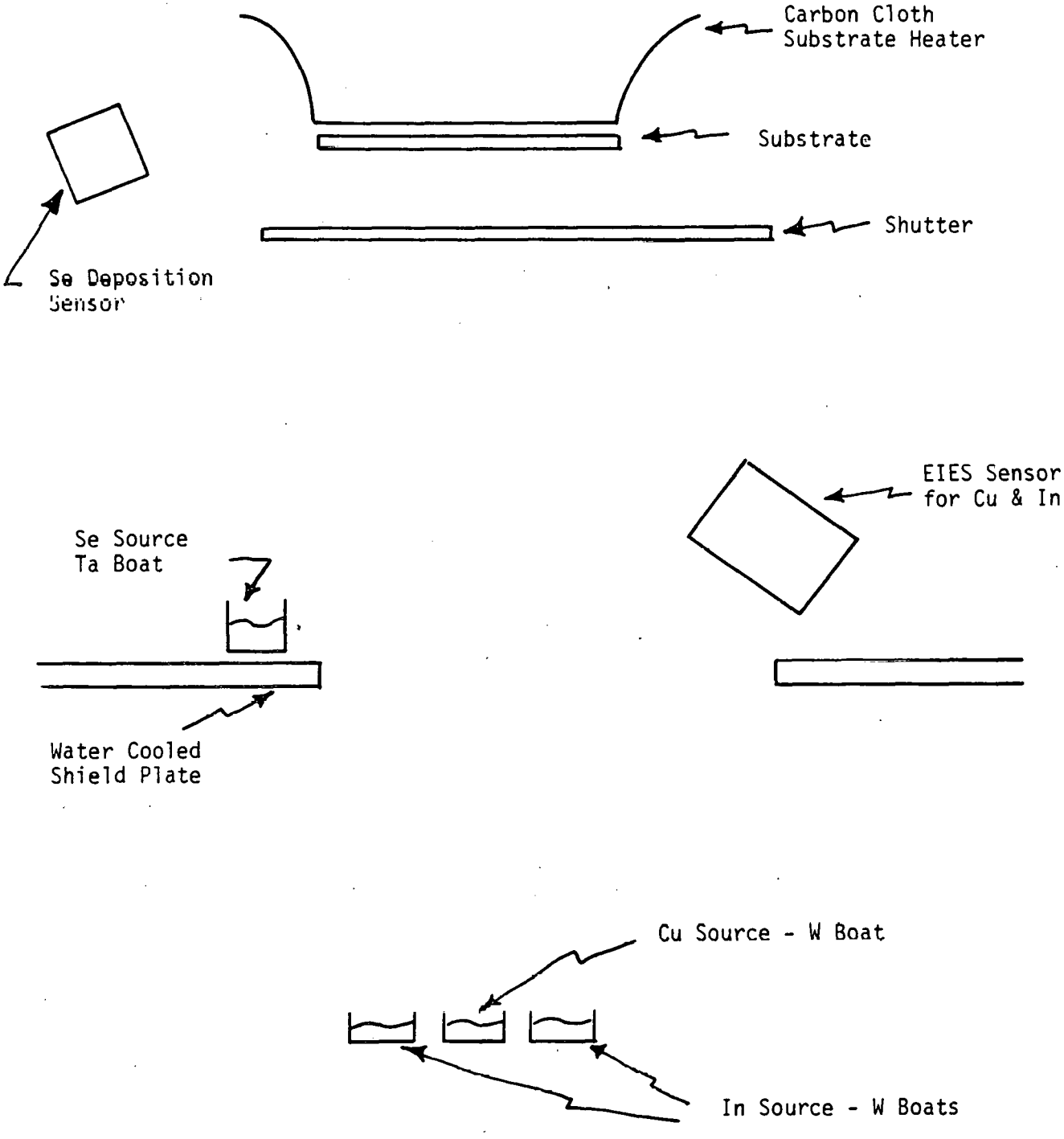


Figure 3.1-3 Deposition Fixturing for Preparing $CuInSe_2$ Thin-Films by Elemental Evaporation

The standard selenide deposition process consisted of an initial Cu rich, low resistivity layer followed by a high resistivity deposit. In practice, the first 2/3 of the deposit was of the low resistivity type and then the Cu deposition rate was reduced by 25-30% for the final third. Typical deposition times were 45 to 60 minutes and the total selenide thickness was 3.5-4.5 μm. Substrate temperatures for the first and second selenide layers were 350°C and 450°C, respectively. At these temperatures, the film properties were found to be quite insensitive to the Se deposition rate. Chamber pressure during the selenide deposition was in the range of 3-8 x 10^{-6} torr.

While the sheet resistivities of the composite and second selenide layers were beyond the range of a four-point probe, the first layer resistivity varied from about 500 Ω/□ to 2K Ω/□. It was difficult to make definitive conclusions regarding the electrical properties of the selenide film samples deposited into the unmetallized side-strip on each substrate. In spite of these layers being masked from the direct CdS deposition, their electrical properties were significantly altered whenever CdS was deposited. For example, Cu nodules were formed in the first, low resistivity layer and resulted in a substantial increase in resistivity. The resistivities of the composite and second layers appeared, in contrast, to be reduced by orders of magnitude by the CdS deposition. These effects seemed to be quite consistent and repeatable. Consequently, electrical resistivity and hot-probe measurements on the layers were continued to be used as a monitor for controlling and adjusting the film composition (Cu/In ratio).

The composition of the three selenide layers (first, composite, and second) were analyzed by EDAX techniques. Results from the EDAX measurements on the deposited films and on a $CuInSe_2$ standard provided by Prof. Loferski of Brown University are shown in Table 3.1-1. In general, it can be seen that the composite or cell layer is fairly close to the stoichiometric composition. There was, however, a slight deficiency in both Cu and Se which is an agreement with a highly compensated, high resistivity film layer.

The EDAX data for the films deposited within a small time frame were compared to the film deposition values in terms of In to Cu weight ratios. Results of this comparison are presented in Table 3.1-2. The ratios obtained from EDAX measurements and those calculated using the In and Cu deposition rates are seen to agree quite well. There had been some concern as to the possible loss of In at the high substrate temperature (450°C) but this does not appear to have occurred.

TABLE 3.1-1 EDAX Measured Compositions for Vacuum Deposited $CuInSe_2$ Thin-Film Layers

Sample ID	Weight Percent Copper	Indium	Selenium
$CuInSe_2$ Stnd (Start)	18.9	34.2	46.9
	19.0	35.2	46.0
691-1	19.4	37.4	43.2
691-1+2	18.2	39.2	42.6
691-2	15.0	42.5	42.6
795-1	20.0	32.8	46.5
795-1+2	18.9	35.7	45.5
795-2	14.2	38.7	47.1
796-1	20.8	32.9	46.4
796-1+2	18.5	35.5	46.0
796-2	15.1	38.8	46.1
797-1	19.9	33.9	46.2
797-1+2	18.5	35.9	45.6
797-2	14.8	37.4	47.7
798-1	19.3	36.1	44.7
798-1+2	17.7	37.2	45.2
798-2	15.3	38.3	46.5
799-1	18.8	37.0	44.2
799-1+2	17.8	39.7	42.5
799-2	15.3	41.9	42.9
801-1	20.3	33.8	46.1
801-1+2	18.7	36.2	45.4
801-2	15.3	38.5	46.2
802-1	19.0	35.5	45.5
802-1+2	17.3	37.4	45.4
802-2	13.2	38.6	48.2
803-1	19.7	35.0	45.3
803-1+2	17.7	36.6	45.7
803-2	14.4	39.2	46.3
804-1	20.4	33.6	46.0
804-1+2	18.0	36.3	45.8
804-2	14.2	38.9	46.9
805-1	19.9	37.4	42.8
805-1+2	17.9	40.0	42.1
805-2	14.8	42.0	43.2

TABLE 3.1-1 EDAX Measured Compositions for Vacuum Deposited $CuInSe_2$ Thin-Film Layers (Continued)

Sample ID	Weight Percent Copper	Indium	Selenium
806-1	19.0	34.5	46.4
806-1+2	18.1	36.3	45.7
806-2	14.5	37.7	47.8
807-1	20.7	35.9	44.1
807-1+2	18.5	41.4	40.2
807-2	15.1	40.2	44.7
$CuInSe_2$ (Finish)	19.0	34.4	46.7
	19.0	34.4	46.7

TABLE 3.1-2 In/Cu Weight Ratios in Vacuum Deposited $CuInSe_2$ Thin-Film Layers

	Layer 1		Layer 2		Composite From Time		Total	
Depo No.	Rates	EDAX	Rates	EDAX	Rates	EDAX	Rates	EDAX
795	1.64	1.64	2.64	2.73	1.96	1.99	1.86	1.89
796	1.66	1.58	2.64	2.57	1.98	1.91	1.89	1.92
797	1.74	1.70	2.53	2.53	2.00	1.98	1.93	1.94
798	1.79	1.87	2.53	2.50	2.03	2.08	1.97	2.10
799	1.79	1.97	2.53	2.74	2.03	2.22	1.97	2.23
801	1.74	1.67	2.53	2.52	2.00	1.95	1.93	1.94
802	1.84	1.87	2.89	2.92	2.13	2.16	2.02	2.16
803	1.79	1.78	2.76	2.72	2.11	2.09	2.01	2.07
804	1.74	1.65	2.76	2.74	2.08	2.01	1.96	2.02
805	1.74	1.88	2.76	2.84	2.08	2.20	1.97	2.23
806	1.74	1.82	2.64	2.60	2.04	2.08	1.95	2.01
807	1.69	1.73	2.64	2.66	2.00	2.04	1.91	2.24

Two ratios were calculated for the composite layer. The first was based upon the deposition time of the two individual layers at their programmed deposition rates while the second applied to the total In and Cu film thickness or weight. These numbers were then compared to the EDAX measurements for the appropriate individual layers and the actual composite, respectively. Again, the agreement is good. The small deviations in some of the deposition rate values are believed to be due to the inaccuracy in rate control over the relatively long, one hour deposit. The number comparisons would also seem to suggest extensive interdiffusion between the two deposited layers.

Diffusion processes between the two selenide layers and between the selenide and sulfide films appeared to be a key element in the achievement of the high efficiency cells. These effects were monitored with simple hot-probe measurements on the three selenide film samples deposited on the unmetallized side-strip and on the selenide layer in regions of the metallized cell area after the CdS was removed by chemical etching. Typically, these tests showed that the low resistivity first layer was always P-type material while the high resistivity second layer was N-type. Providing the proper Cu/In deposition rates for the two layers were utilized, the side-strip composite layer also showed a high resistivity, N-type response. It would be expected that this structure would result in a poor performance, buried homojunction cell. However, the hot-probe measurement on the selenide layer in the cell area which had been coated with CdS indicated the presence of a P-type material. It is believed that Cu diffusion into the CdS is responsible for this apparent type conversion leading to a high efficiency heterojunction device. Out diffusion of Cu would create the Cu vacancies considered to be the most probable acceptor in $CuInSe_2$. An optimum range in the magnitude of the hot-probe response, which was indicative of resistivity and controlled by the Cu/In deposition rates, was experimentally established. Cells with selenide layers on either side of this range possessed lower efficiencies. The lower resistivity cells displayed strong cross-over characteristics in the light and dark I-V curves while the higher resistivity samples exhibited lower V_{oc} values.

Following the selenide deposition, the substrates were cooled for deposition of the CdS film. The standard substrate temperature used throughout the program for the CdS deposits was 200°C. Deposition rates were 0.5 to 1.2 μm per minute and film thicknesses were 2.5-3.5 μm. In was co-evaporated with the CdS to dope the deposits.

Since it was observed that lower performance cells were produced when the initial sulfide deposit was In doped, only the last 2/3 of the layer was doped with an estimated 1-3% In. The doped film sheet resistivity was maintained in the range of 30 to 80 Ω/□ while the undoped material resistivity was 20-50 Ω-cm.

At the beginning of the program, the CdS powder (GE electronic grade, type 118-2) after pre-sintering at 1050°C for four hours in forming gas, was evaporated from a tantalum foil baffle-box. The source was later changed to an apertured, graphite crucible in order to allow higher source temperatures for lower resistivity deposits, reduce particulate emission, and prepare for the mixed ZnCdS depositions. The graphite source was heated with a temperature controlled vacuum furnace (Luxel, model Radak II).

It was anticipated that the use of lower resistivity CdS at the heterojunction would result in an increase in V_{oc}. Some evidence for this was found for cells prepared at different CdS source temperatures. The effect was, however, small as discussed in section 3.5. Another low resistivity approach briefly studied was $CdCl_2$ doped films prepared by adding the chloride powder to the CdS powder. Even though very low resistivity films were achieved (less than 0.5Ω-cm for a 0.2% chloride concentration), the cell performance was not measurably improved.

The next cell fabrication step was CdS surface cleaning prior to the deposition of the aluminum film grid contact. It was found by Auger and ESCA techniques conducted after the first cell life-test measurements that the as-deposited CdS surface was grossly contaminated with Na, Cl, O, and C. The contamination resulted in a blistering of the Al film contact, especially on the open circuit loaded cells, during the constant illumination tests. A brief (30 sec.) RF sputter etch with argon was found to very effective in removing the contamination without adversely affecting the cell performance and resolved the contact blistering problem.

The etched substrates were transferred from the sputter/sputter-etch chamber to another vacuum evaporation system equipped with an electron gun vaporization source for the Al grid deposition. After evacuating the chamber to less than 5×10^{-6} torr, the substrates were exposed to glow discharge cleaning as a means to further improve the Al film adherence. The discharge gas was Ar/5% O_2 at a pressure of 20-30 microns. Cleaning time was two minutes and the applied dc voltage was 2 KV.

Following cleaning, the chamber was re-evacuated to ~ 3 x 10^{-6} torr and the Al film deposited at a rate of 50 Å/sec for a 2 µm thick layer.

A metal, stencil mask held in intimate contact to the cell surface with small magnets was used to define the grid structure. The structure at the beginning consisted of 10 equally spaced lines of 50 µm widths connected with a central 0.8 mm wide bus bar covering a 0.8 cm by 0.8 cm area for a 1 cm^2 cell. The calculated optical transparency of the grid was 93-95%. Four of the 1 cm^2 cells were formed on each substrate. Later, a revision to the grid design was made. The grid line spacing was increased to only 5 lines/cm with a line width of 75 µm. The grid lines were interconnected by a tapered, central bus bar that terminated in a pad off the cell area in order to avoid the previous problem of probe shadowing during cell testing. Transmission of the grid was approximately 95% and two 1 cm^2 area cells were included on each substrate.

At the time of the grid mask revision, provisions were made for a large cell (2 cm x 4 cm) and twelve small (2.5 mm x 2.5 mm) samples on each substrate in addition to the two 1 cm^2 cells. The grid for the large cell was also based upon a tapered central bus bar and 100 µm width lines with a 5 line/cm spacing and a transmission of 92%.

To accurately define each cell/cell area and to remove shunts originating from the CdS contacting the Mo metallization around the substrate borders, the grid coated substrates were subjected to a photolithographic process. A liquid, positive photoresist (Shipley 1375) was applied and spun at ~3000 RPM for ~ 30 sec.

The resist was exposed through a glass mask negative with a standard mask aligner and then developed. To enhance the chemical resistance of the resist to the acid etchant, the substrates were hard baked for ~ 20 minutes at 120°C in an air circulating oven. The CdS etchant was a 50% by volume solution of HCl in DI water heated ~60°C. Etching time was typically around 5 sec. to remove a 2-4 µm thick deposit. Evidence for selenide etching was never detected.

After etching, the substrates were rinsed in running DI water, the resist removed by the spraying of acetone, again rinsed in DI water, and finally, blown dry with high purity nitrogen gas. No detrimental effects on cell performance were observed as a result of exposure to the solvents and aqueous based solutions used in the photolith-

ography. After adequate drying, the cell characteristics remained quite stable in room ambient and, consequently, were simply stored in this ambient.

Prior to heat-treatment, the substrates were diced into the individual 1 cm^2 cells, the 8 cm^2 cell, and the unmetallized side-strip. The heat-treatment was performed in a tube furnace maintained at temperatures of 200-225°C. Either air or, more preferably, flowing oxygen was used as the bake environment. The normal procedure was to measure the cell characteristics (light I-V), insert the cells into the furnace for 10-15 minutes, withdraw the cells, cool, and re-measure. This procedure was repeated until the cell characteristics appeared to saturate or not be changed by the treatment. Typically, the total bake time was 30 to 60 minutes.

Although used only on the highest efficiency cell samples, the final fabrication process was the deposition of an anti-reflection (AR) coating. The AR-coating was a SiO_x thin-film prepared by evaporating SiO in an oxygen partial pressure. Deposition parameters were a rate of 10 Å/sec., 8×10^{-5} torr oxygen partial pressure, and a thickness of 1000 Å. From these parameters, the film index of refraction was assumed to be ~ 1.6 and the single layer coating reduced the total reflectance to ~4-5% in the active cell response spectral region.

Problems initially were encountered with the stability and adherence of the SiO_x films over the CdS surface areas. Upon exposure of the oxide films to high humidity, they frequently buckled and separated from the CdS. These problems were corrected by: 1) Vapor degreasing the cells for 10 minutes in trichloroethylene; 2) Glow-discharge cleaning for one minute using the equipment and process parameters as for the grid deposition; and 3) Installing a 1/16 inch diameter aperture in the exit port of the SiO baffle-box vapor source to increase the source temperature while maintaining the same deposition rate. The higher source temperature altered the vapor and resulting film composition (and stress) such as to produce a more mechanical and environmental stable deposit.

3.2 Mixed Zn CdS Film Deposition

In making a heterojunction with $CuInSe_2$, the mixed sulfide, $Zn_xCd_{1-x}S$, with a proper composition should minimize the difference in lattice constant and in electron affinity between the two materials. Minimization of these differences should lead to a

reduced interface recombination rate and to an increase in the built-in voltage, thus leading to higher V_{oc}. Improvements have been observed in $Cu_2S/ZnCdS$ (10) and $CuInSe_2/ZnCdS$(11) cells.

In order to specify the composition of the mixed sulfide giving the best match of lattice constant and electron affinity with the $CuInSe_2$, the $Zn_xCd_{1-x}S$ properties should be known. In the following table, the lattice constant, a, energy band-gap, E_g, and electron affinity, χ, of the CdS, ZnS, and $CuInSe_2$ are listed.

Table 3.2-1 Lattice constant, energy band-gap, and electron affinity of CdS, ZnS, and $CuInSe_2$

Material	a(Å)	E_g(eV)	χ (eV)
CdS[11]	5.850*	2.42	4.5
ZnS[11]	5.393*	3.58	3.9
$CuInSe_2$	5.785	1.04	4.3[12]

*$\sqrt{2}$ a

The composition dependence of the lattice constant for the mixed sulfide can be calculated from Vegard's law, which gives

$$\sqrt{2}\,a\,(Zn_xCd_{1-x}S) = 5.850 - x(5.850 - 5.393)\ \text{Å}.$$

For equalizing the lattice constant of the $CuInSe_2$ and $Zn_xCd_{1-x}S$, the x value should be 0.142 or an admixture of ~14% ZnS to CdS.

Since the quoted electron affinity data are unreliable, the mixed sulfide composition is more difficult to specify for χ-matching. If we take $\chi = 4.5$eV for CdS, the χ_{ZnS} can be found by assuming a fixed band edge due to the common anion and

$$\chi_{ZnS} = \chi_{CdS} - (E_{g_{ZnS}} - E_{g_{CdS}})$$

$$= 4.5 - (3.58 - 2.42) = 3.34\ \text{eV}$$

By linear interpolation, the χ of the mixed sulfide can be obtained as

$$\chi_{Zn_xCd_{1-x}S} = \chi_{CdS} - x(\chi_{CdS} - \chi_{ZnS})$$

$$= 4.5 - x(4.5 - 3.34)\ eV$$

To equalize $\chi_{Zn_xCd_{1-x}S}$ with χ_{CuInSe_2}, the x value should be 0.17. From these estimations, optimum composition of the mixed sulfide for both lattice constant and electron affinity match should be at $Zn_{0.15}Cd_{0.85}S$. Thus, techniques to deposit mixed sulfide films with Zn concentrations of 15-30% were then studied.

To be compatible with the selenide deposition, only vacuum evaporation of the CdS and ZnS powdered materials was considered. For the majority of the depositions, an aperture controlled, two chamber graphite vaporization source patterned after the units developed at the University of Delaware for Cu_2S/ZnCdS thin-film cells was used (12). The source structure is shown in Figure 3.2-1 and was heated by the temperature controlled Luxel vacuum furnace. Dimensions for the overall source were 1.7 inches high by approximately 0.8 inches in diameter. Quartz wool was loosely packed above the ZnS and the top section of the CdS container. Film compositions were varied by adjusting the diameter of the exit port aperture and the CdS aperture. Typical results from a series of 3 μm thick deposits made onto a 200°C heated alumina substrate are presented in Table 3.2-2.

With repeated depositions of the mixed sulfide films, several significant problems became apparent. For example, there was a high degree of variability in the deposited films with respect to appearance and sheet resistivity. According to photoluminescence measurements of the exciton peak, these results were caused by varying Zn content. Further work demonstrated the sensitivity of film composition to source parameters such as the amount of CdS and ZnS powders loaded into the source, packing of the quartz wool, etc. Attempts made to fix these parameters were found to be only partially successful.

Another identified problem area related to the use of high source temperatures for the purpose of lowering the mixed sulfide resistivity. High temperatures resulted in a greatly increased chamber pressure and in the EIES sensor on the channel monitoring In (4510 Å wavelength). Since Cd has emission lines in this region, it was suspected that Cd vapor was responsible for the observed signal. Although the EIES was not used during the sulfide deposition, the concern was that material would be transported through the light pipe tubing and coat the feed-through window. Such a coating would

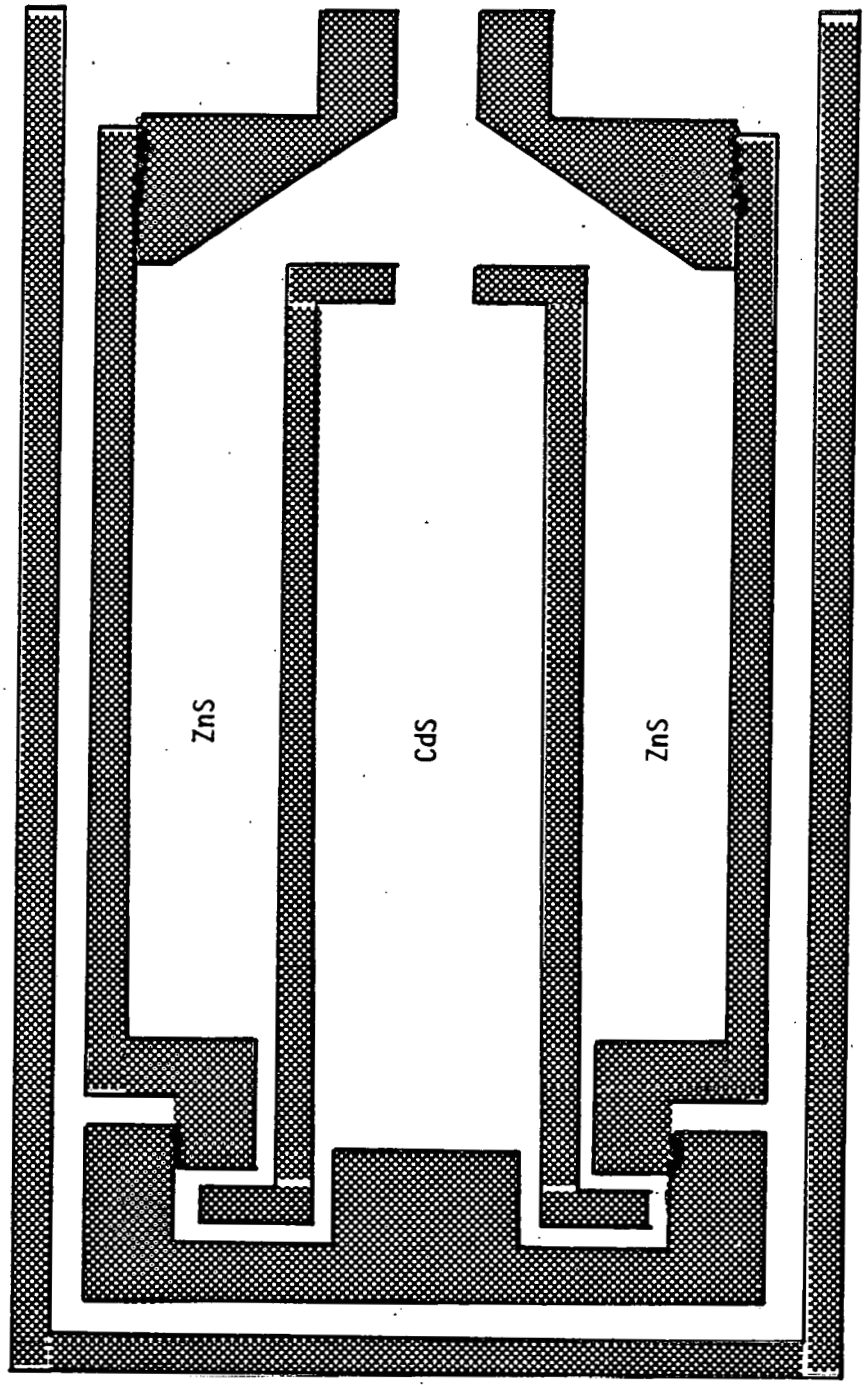


Figure 3.2-1. Graphite Source for Deposition of Mixed CdZnS Films

TABLE 3.2-2

Zinc Content of Mixed ZnCdS Thin-Film
Prepared With Apertured Vapor Source

Film No.	Source Temp. (°C)	Diameter CdS Aperature (in.)	Diameter Exit Aperature (in.)	Zn Content, First Half of Deposit (%)	Zn Content, Second Half of Deposit (%)
1	1160	0.070	0.20	19	22
2	1180	0.10	0.20	23	23
3	1210	0.060	0.10	--	26
4	1210	0.070	0.10	22	19.5
5	1210	0.080	0.10	17	--

then cause measurement errors in subsequent $CuInSe_2$ depositions. After several sulfide deposits, a coating was, in fact, found on the window.

A final problem concerned the normal fall-off in deposition rate with time at a fixed source temperature. Because of the interrelationship between the sulfide deposition rate and the necessary In dopant deposition rate the common procedure was to slightly increase the source temperature to maintain a constant sulfide rate. Subsequent measurements of Zn content showed, however, a large variation between the initial and final layers (as much as a factor of two). This variability was reduced by adopting a constant source temperature but required unpredictable adjustments to the In dopant deposition rates.

In summary, the results with single apertured source for preparing the mixed sulfide films for the present applications were quite disappointing. Not all of the above mentioned problems were adequately resolved at the same time, the reproducibility was not especially good, and the film resistivities were frequently high. For films of 15-25% Zn content, resistivities less than approximately 100Ω-cm for 3 μm thick layers could only be achieved at very high source temperatures (~1270°C). However, such temperatures produced the high chamber pressures and excessive deposition rates. Lowering the deposition rate by increasing the source to substrate distance or by reducing the aperture sizes were both unsuccessful. In the first instance, there was insufficient material for the desired film thickness while operation with small exit apertures resulted in ZnS condensation inside the exit aperture cap.

In view of all of the described process deficiencies with no readily apparent solutions, it was decided late in the program to investigate the use of independent ZnS and CdS sources. This approach would also allow the option of using graded Zn composition layers if the resistivity of the high Zn content films could not be reduced to levels needed for low series of resistance.

For the two source process, CdS was evaporated from an apertured graphite crucible heated with the temperature controlled furnace and ZnS evaporated from a tantalum foil baffle-box placed in close proximity to the CdS (~1 inch spacing). The ZnS deposition rate was first established using a quartz crystal monitor while the CdS was being maintained at a temperature producing insignificant evaporation. The CdS temperature was then increased to the desired deposition value and was found

sufficiently repeatable to achieve controllable composition deposits. This process appeared to work considerably better than the single source method and was used in the fabrication of high efficiency mixed sulfide cells where the Zn content was approximately 20%.

As in the case of the plan CdS cells, the mixed sulfide films were deposited at a substrate temperature of 200°C, the film thickness was 2-3 μm, and the last 2/3 of the deposit was doped by co-evaporation of In (1-3% by weight). Completion of the cells by deposition of the aluminum film grid contact, cell heat-treatment, and SiO_x AR-coating (when used) was also identical to the standard CdS cells.

3.3 Planetary Film Depositions

The preparation of $CuInSe_2$ thin-film with a planetary or rotating substrate vacuum deposition apparatus was investigated during the last year of the program. This effort was motivated by the belief that, if the process could be successfully developed, it would permit fabrication of a large number of small cells (1 cm^2 area) as needed for a comprehensive life-test program, fabrication of a small number of very large cells (25-100 cm^2 area), and elimination of the film composition gradients (especially variations in the Cu/In ratio) across the substrate surface.

The planetary fixture, which is shown in Figure 3.3-1, was constructed on a specially designed feed-through collar. It contained three planets with each capable of holding 18, 2" x 2" substrates. The collar was placed upon the base-plate of a liquid nitrogen trapped, oil diffusion pumped, vacuum deposition coater. Fixture components and the stainless steel bell-jar were water cooled since IR lamps were used for substrate heating and were expected to generate a considerable heat load during the 350°C/ 450°C selenide deposition. The elemental vapor sources mounted within the fixture and the film evaporation monitoring methods were similar to those used in the standard, fixed substrate apparatus. That is, boat vaporization sources, a quartz crystal monitor for Se, and an EIES monitor for Cu and In. A provided fixture thermocouple and temperature controller were used to control the temperature of the rotating substrates after it had been calibrated against thermocouples attached to alumina substrates positioned at various points in stationary planets.

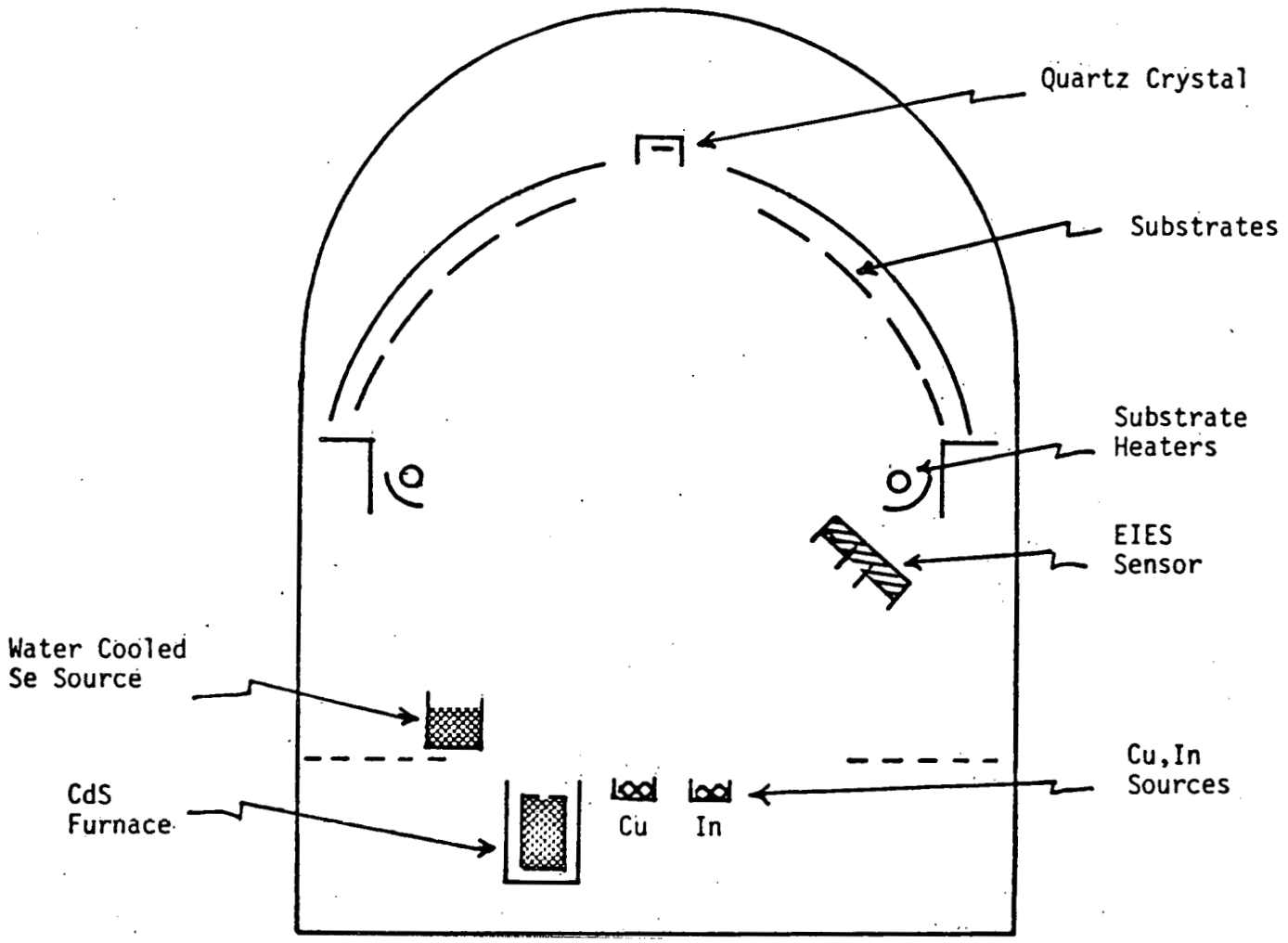


Figure 3.3-1 SCHEMATIC OF PLANETARY SYSTEM

It was soon obvious that, with the lamp method for substrate heating, the temperature values would play a dominant role in the planetary process development. Problems caused by the attainment of very high substrate temperatures with radiant heating and compounded by the presence of the high vapor pressure Se, made it mandatory to reduce the substrate temperature to as low as possible. To determine how far the temperature could be lowered without seriously degrading cell performance, a series of cells were fabricated in the fixed substrate system using selenide substrate temperature as a process variable. It was determined that a 50°C reduction in temperature for both selenide layers produced cells with characteristics comparable to the higher temperature, standard deposits. Equipped with these cell results, the decision was made to develop the planetary process around the 300°C/400°C temperature settings.

Even at lower temperatures, problems continued to be encountered in developing the planetary technique. Their description and experimentally derived solutions have been discussed in previous quarterly reports. With the exception of one, all were satisfactorily resolved. The one remaining deficiency was the accurate monitoring of the true Se deposition rate to which the substrates were exposed during the selenide deposition.

In spite of all the processing difficulties, it was found that good quality $CuInSe_2$ film material could be prepared by the planetary approach. The composition and electrical properties of some of the planetary deposited films are listed in Table 3.3-1. As shown by the values contained in the table, EDAX measurements indicate a general deficiency in Cu and excess in In with the exception of run No. 23 which was close to the stoichiometric composition. For films produced previously with the fixed substrate equipment, the EDAX compositions were typically 17-18% Cu, 36% In, and 46% Se. Film resistivities and carrier type (hot probe) were also comparable to those prepared with the standard process.

The results of reflection electron diffraction on the selenide film of run No. 23 are presented in Table 3.3-2 along with the ASTM-X ray diffraction data for $CuInSe_2$. Agreement with the ASTM values is seen to be good and confirms the formation of the desired selenide material. Several points should, however, be noted. First is the chalcopyrite line at a d-spacing of 2.52 Å. Second is the very, very weak line at a d-spacing of about 2.84Å. This line, although not in the ASTM index, could be a

TABLE 3.3-1 Properties of $CuInSe_2$ Thin-Films Prepared With Planetary Evaporation Equipment. Substrate Temperature - 300°C

	EDAX Composition			Sheet Resistivity	Conductivity
Run No.	Cu	In	Se	(Ω/□)	Type
9	13.8	40.4	45.9	-1.5×10^7	N
11	14.4	39.6	46.0	$- 7 \times 10^9$	N
12	13.6	39.9	46.6	-1.5×10^9	N
15	16.9	37.5	45.6	$- 4 \times 10^7$	N
23	19.5	34.4	46.2	1K	P
Standard	19.0	34.6	46.4		

TABLE 3.3-2 Reflection Electron Diffraction Data for $CuInSe_2$ Thin-Film Prepared with Planetary Evaporation Equipment. Substrate Temperature - 300°C, Run No. 23

RED Data		ASTM Index $CuInSe_2$		
Relative Intensity	d-Spacing (Å)	Intensity I/I_1(%)	d-Spacing (Å)	(h k l)
VS	3.34	70	3.34	112
VVW	2.84	--	(2.89)	(200,004)
VW	2.52	15	2.52	211
S	2.03	100	2.04	204,220
S	1.73	85	1.743	116,312
M	1.66	--	(1.67)	(224)
VVW	1.49	6	1.480	305,325
W	1.44	25	1.446	400
M	1.31	35	1.327	316,332
VVW	1.19	2	1.200	415
M	1.17	60	1.181	424
VW	1.11	25	1.114	336,512
W	0.97	30	0.9777	516,532
W	0.90	30	0.9140	620,064
VW	0.87	20	0.8821	3211
VW	0.80	30	0.8097	712,552

reflection from the 200,004 planes and has been reported by Lesueur, et al. (13). We have seen this weak line previously but have attributed it to the presence of $Cu_{2-x}Se$ (2.88 Å). Third is the line at a 1.66 Å d-spacing which is observed in nearly all of our selenide deposits and in those reported by Kazmerski. The very strong (112) orientation of the deposited films is believed responsible for this diffraction line.

From all indications, the selenide deposits at the 300°C substrate temperature should be usable for the first, low-temperature layer in the $CuInSe_2$/CdS cell. Accordingly, an attempt was then made to establish the deposition conditions at a 400°C temperature and the combination of the two layers.

Preparation of selenide films at 400°C with the desired properties was accomplished but it was not possible to utilize the two-temperature combination. The Se monitoring problem mentioned previously was believed to be the limiting factor. Consequently, it was necessary to select only a single, constant temperature (400°C) for the selenide film deposition with the planetary equipment.

To summarize, the following general observations can be made about $CuInSe_2$ films produced in the planetary system. The films appeared to be more sensitive to Se evaporization rate than in the fixed substrate system. With a substrate temperature of 400°C, both P and N-type material were produced with the proper electrical properties. The material preparation conditions in the planetary system differed, however, significantly from those in the fixed substrate system. For instance, the substrate temperature was held fixed at 400°C rather than a two-temperature process (350°C/450°C) and the Se as well as the Cu deposition rates were adjusted to prepare the two selenide layers deposited for cell fabrication.

Although the evolved selenide preparation parameters were different than planned or used in the standard equipment, the planetary deposits appeared suitable for device studies and, near the program completion, were used to form cell samples. Since a sulfide deposition process in the planetary had not been established, the selenide coated substrates (Mo metallized) were transferred to the fixed substrate system for sulfide deposition. A mixed $Zn_xCd_{1-x}S(x\sim0.2)$ was deposited using the two source deposition process and the normal cell fabrication procedures. After baking in oxygen, the non-AR coated 1 cm^2 area cell achieved an efficiency of 7.5% under simulated AM1 illumination. This highly encouraging result is felt to demonstrate the success of

the planetary approach and the transfer of technology (with some modification) between the two vacuum deposition systems/approaches.

3.4 Effects of Cell Heat Treatment

Cell performances have shown significant improvement after heat treatment in an oxygen containing atmosphere. In this section the environmental effects of heat treatment to the cell response and the possible mechanism are discussed.

To determine the cell response after heat treatment in various ambients, small diodes (2.5 x 2.5mm with 2.0 x 0.75mm Aℓ top contact) have been made from a same substrate. Samples with two diodes on each piece were cut from the substrate and were annealed in a tube furnace at 200°C for 10 minutes under H_2/Ar, air and H_2 ambients. Samples were sealed in glass tubes of less than 10^{-4} Torr pressure for treatment in vacuum environment.

Before and after the heat treatment, photovoltaic characteristics (V_{oc}, I_{sc} and F.F.) of each diode under AM1 illumination were recorded. Results were summarized in Table 3.4-1. Characteristics of these diodes were about the same with V_{oc} ~ 340-350mV, I_{sc} ~ 1.5mA and F.F. ~ 0.6 before heat treatment. As indicated, the short circuit currents after heat treatments in all cases increased from ~1.5mA to ~1.6mA. However, the open circuit voltages and fill factors increased only for samples annealed in forming gas (H_2/Ar) or air. The sample treated in vacuum (heated and cooled in the vacuum sealed glass tube) had a V_{oc} and F.F. appreciably lower than the values before heat treatment. The V_{oc} and F.F. of the sample annealed in hydrogen and cooled down in air showed essentially no improvement.

The degradations in V_{oc} and F.F. of samples (#3 and #4) annealed in vacuum and hydrogen were unexpected. In order to eliminate doubts as to possible property differences from sample-to-sample, the two adjacent diodes separated by only a few millimeters were cut out from the same sample piece and annealed separately. Results are shown in the Table, sample 5 and 6. Before the heat treatment, the photovoltaic properties of the two diodes (A and B) on sample #5 were nearly identical. After the first annealing, the photovoltaic performance of diode 5A (in H_2/Ar) improved while the V_{oc} and F.F. of diode 5B (in vacuum) degraded. Although the diode showed slight further improvement after a second treatment in H_2/Ar, the

TABLE 3.4-1. Dependence of Photovoltaic Response on Heat Treatments in H_2/Ar, Air, Vacuum, and H_2

Sample		Ambient	Temp. °C	Time Min.	V_{oc} mV	I_{sc} mA	F.F.	Note
1	A				346	1.5	0.59	*
	B				353	1.55	0.60	
	A	H_2Ar	200	10	370	1.6	0.64	
	B	H_2/Ar	200	10	370	1.6	0.65	
2	A				330	1.5	0.52	*
	B				350	1.5	0.60	
	A	Air	200	10	380	1.6	0.67	
	B	Air	200	10	370	1.6	0.68	
3	A				350	1.5	0.62	*
	B				350	1.55	0.61	
	A	Vac. (10^{-4} Torr)	200	10	300	1.65	0.46	
	B	Vac. (10^{-4} Torr)	200	10	300	1.6	0.48	
4	A				340	1.55	0.59	*
	B				340	1.5	0.60	
	A	H_2	200	10	340	1.7	0.58	
	B	H_2	200	10	350	1.65	0.59	
5	A				330	1.55	0.59	*
	B				325	1.60	0.58	
	A	H_2/Ar	200	10	340	1.75	0.61	
	B	Vac. (10^{-4} Torr	200	10	290	1.75	0.52	First anneal
	A	H_2/Air	200	5	360	1.70	0.64	Second anneal
	B	Air	200	5	370	1.70	0.63	
6	A				330	1.6	0.58	
	B				333	1.65	0.59	
	A	H_2/Ar	200	10	360	1.7	0.63	First anneal
	B	H_2	200	10	324	1.73	0.55	
	A	H_2/Ar	200	5	365	1.7	0.64	Second anneal
	B	H_2/Ar	200	5	340	1.7	0.59	
	A	H_2/Ar	200	3	370	1.6	0.67	Third anneal
	B	O_2	200	3	365	1.7	0.64	

* Before heat treatment

diode 5B exhibited almost equal performance to 5A after brief heating in air to recover from the first vacuum bake.

Similar results were observed for sample 6 whereas the diode 6A was annealed in H_2/Ar and the diode 6B was in H_2. Only after being annealed in O_2, had diode 6B fully recovered from the first H_2 bake.

It seemed from this initial heat treatment study that the improvement of the short circuit current was purely a thermal effect independent of the environment while the effect on V_{oc} and F.F. did highly depend upon ambient. Annealing cells in H_2/Ar (our H_2/Ar gas passes through a long plastic tube and may have contained some oxygen) and air improved V_{oc} and F.F., but when done in vacuum and H_2, both V_{oc} and F.F. degraded. The degradation in vacuum and H_2 can, however, be recovered by a subsequent anneal in air or O_2.

The improvement of the V_{oc} and F.F. after heat treatment in an oxygen containing atmosphere might be due to the formation of oxides which could passivate the cell junction edge and reduce the leakage current. The natural oxides at the junction edge could be reduced by heat treatment in vacuum or reducing ambient to increase the leakage current and, hence, to degrade the V_{oc} and F.F. The short circuit current improvement may be due to thermal induced interdiffusion, thermal annealing out of a stress induced defect center, etc.

An experiment has been performed to determine the effects of heat treatment to the aluminum contact and on the V_{oc} increasing due to a possible cell edge passivation. A sample piece of selenide blank covered with CdS film from a substrate on which a control cell had been made and had demonstrated over 7% efficiency, was processed to make two cells according to the following steps:

(1) Deposit the Al-grid contact of one cell;
(2) Heat treat the whole piece at 200°C in oxygen for 20 minutes;
(3) Deposit the second cell Al-grid contact; and
(4) Photolithographically delineate the two cells by etching the CdS film.

Since the edges of the two cells were not exposed to high temperature oxidation environment, we expected that the V_{oc}'s of the two cells would be lower than the control cell, if the hypothesis of edge passivation due to oxidation was true. Morever, the performance of the cell with annealed Al contact would be better than the other cell without annealed contact, if the effect of heat treatment was to improve the contact property.

The experimental measurements revealed, however, that the performance (V_{oc}, I_{sc}, and F.F.) of the two cells were comparable to the control cell and there was no difference between the two test cells. From this experiment, it seemed that the edge passivation hypothesis could not be supported and contact annealing was not a necessary step.

In order to examine the effects on cell performance of heat treatment in oxidizing and reducing environments, a cell with an initial efficiency of 1.53% was baked alternately in flowing hydrogen and oxygen at 200°C. The three cell parameters, V_{oc}, I_{sc}, F.F., after each bake were recorded and are shown in Figure 3.4-1. As shown, except after the initial 15 min. H_2 bake, all three parameters increased after baking in oxygen and remained constant or slightly decreased when then baked in hydrogen. The cell performance steadily increased after baking in the oxidizing environment and did not increase when heat treated in the reducing environment to the values before the O_2 bake. This non-reversible effect of heat treatment in oxidizing and reducing ambients also disclaims the cell edge passivation hypothesis.

Cell characteristics were measured before and after thermal annealing in order to determine the mechanism active during heat treatment and their relationship to cell performance.

The photovoltaic response under simulated AM1 illumination of the as-deposited cell (1 cm^2) was:

V_{oc} = 335 mV
I_{sc} = 22 mA
η = 4.14%
F.F. = 0.56

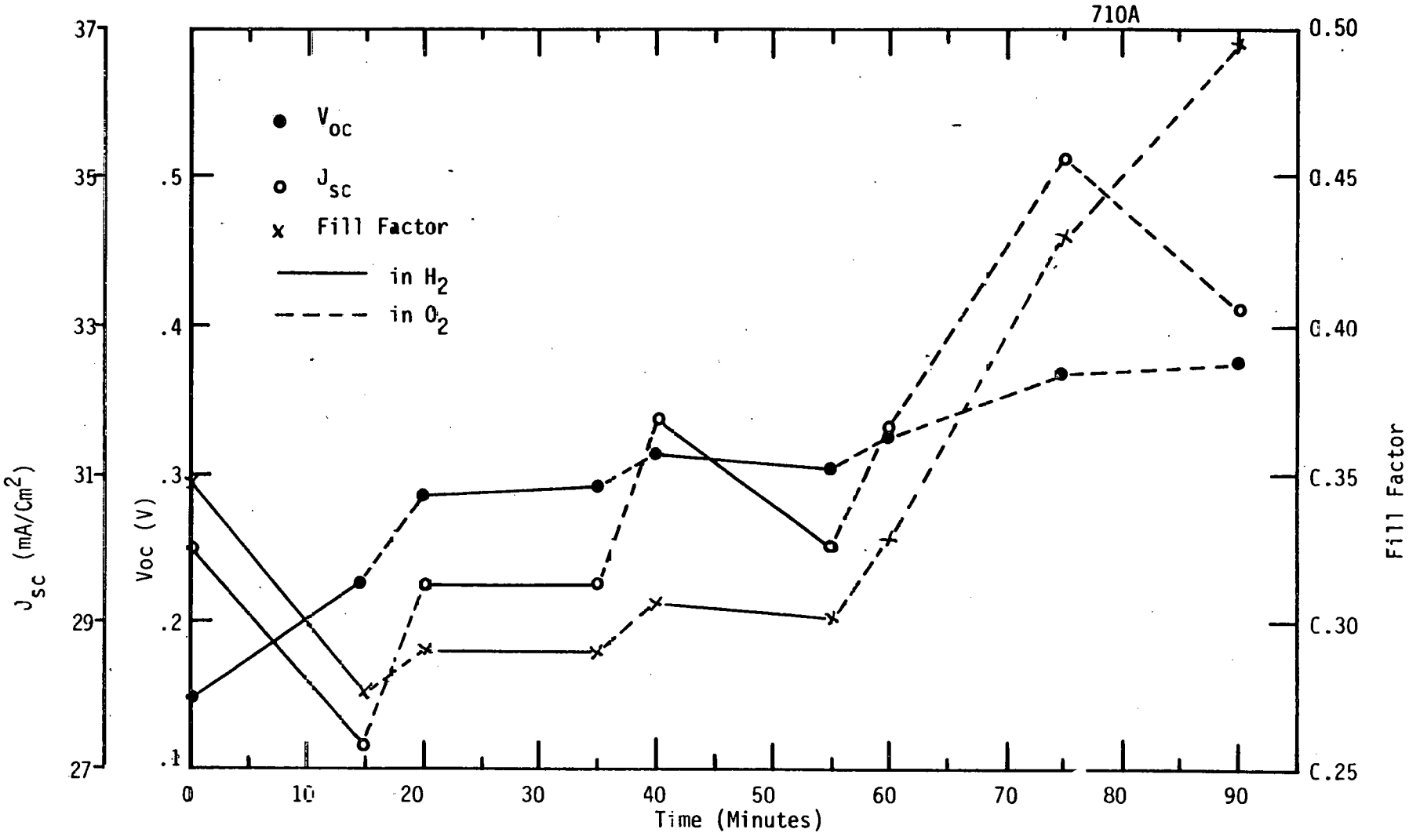


Figure 3.4-1. The variation of V_{oc}, J_{sc} and F.F. with alternating heat treatment in H_2 and O_2 at 200°C.

The cell response increased to:

V_{oc} = 355 mV
I_{sc} = 31 mA
η = 6.63%
F.F. = 0.6

after heat treatment at 200°C for 20 minutes in O_2.

The light and dark diode characteristics are shown in Figure 3.4.2. As noted in the figure, the dark I-V curve of the unbaked cell (dotted line) had an inflection point at a current level near 12 mA and the light I-V curve crossed over with the dark curve in the first quadrant. After the heat treatment, the inflection point and cross-over of the I-V characteristics disappeared and the cell response improved.

The change of the dark I-V characteristics before and after heat treatment can better be seen in the semi-log plot, Figure 3.4.3. For the forward bias, non-exponential I-V characteristics were observed in the low and high current region for the unbaked cell. In the current range from 4×10^{-4} - 6×10^{-3} A, exponential diode characteristics could be fitted with A = 1.97 and $J_o = 1.2 \times 10^{-5}$ A/cm^2. After heat treatment, the forward current varied exponentially over three decades with bias voltage with A = 1.54 and $J_o = 2.5 \times 10^{-6}$ A/cm^2. The reverse current decreased almost one order after the heat treatment.

The cell dark capacitance was measured as a function of bias voltage before and after heat treatment. Results are shown in Figures 3.4.4 and 3.4.5. The C-V characteristics were quite complicated due to the layer structure of the cell. In general, the capacitance was much higher after the heat treatment. For example, at zero bias, the capacitance after heat treatment was 14.2 nF compared to 8.1 nF before baking. If we assumed that the CdS was heavily doped and there was only one junction ($CdS/CuInSe_2$) present, the carrier density and layer thickness of the $CuInSe_2$ layer (N_A) = 2.33×10^{14} cm^{-3}) had a thickness of 1.8 μm before heat treatment. This value was not consistent with the film deposition value ($\lesssim$ 1 μm). However, after heat treatment, the thickness of the layer ($N_A = 7.9 \times 10^{14}$ cm^{-3}) was reduced to a value of 0.78 μm which then agreed with the deposition thickness.

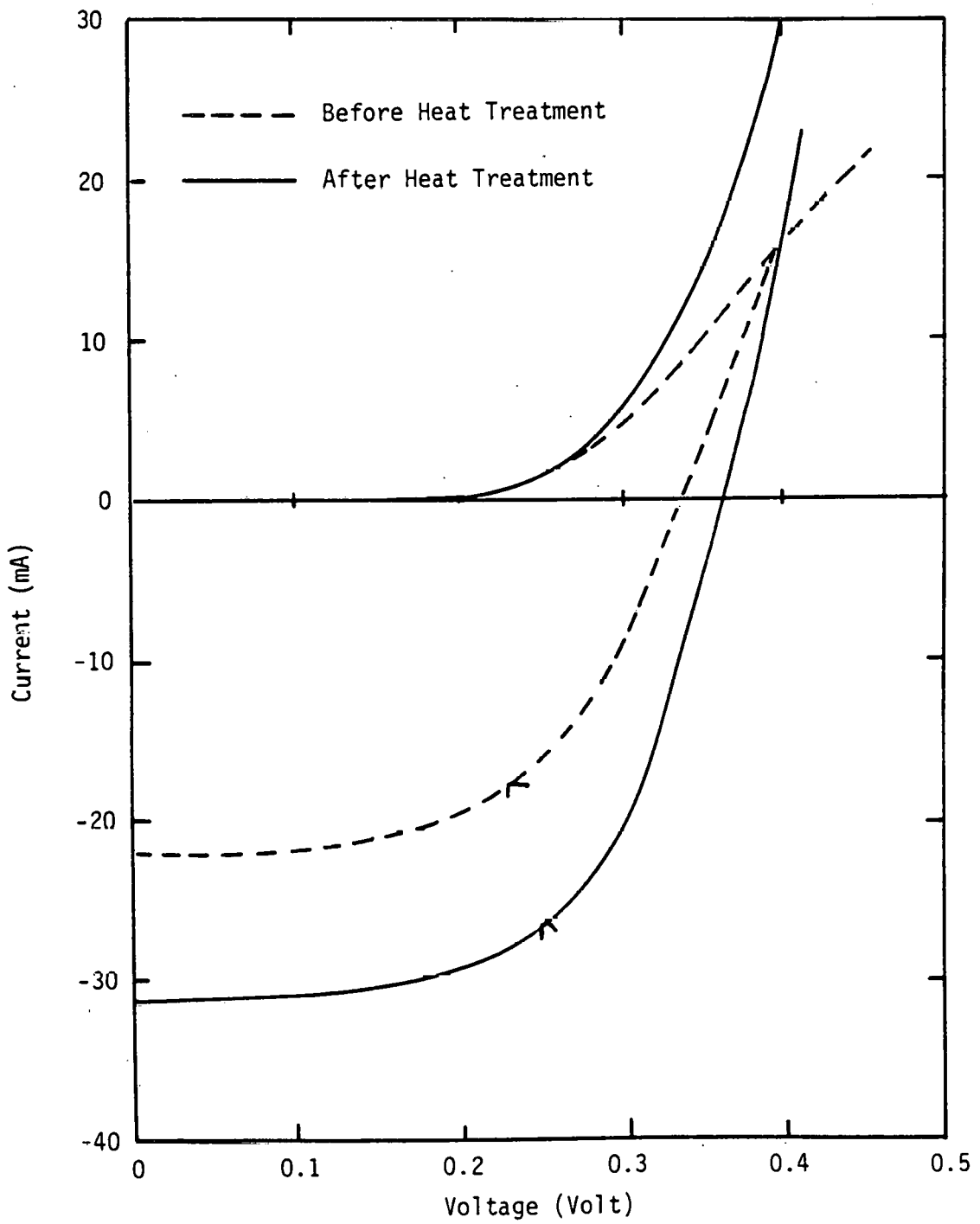


Figure 3.4-2 Light and Dark Characteristics Before and After Heat Treatment

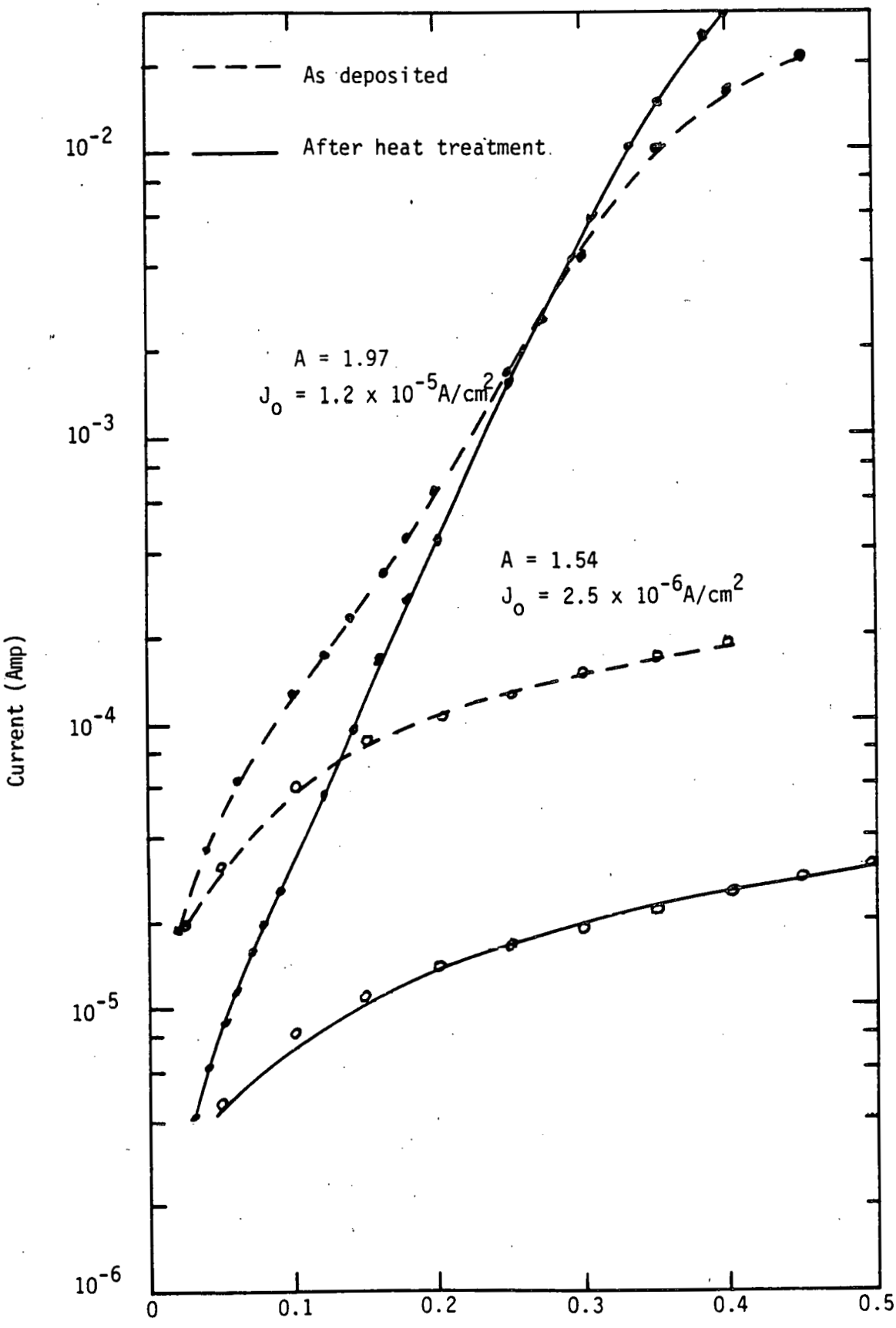


Figure 3.4-3 Semilogorithmic Plot of Dark I-V Characteristics Before and After Heat Treatment

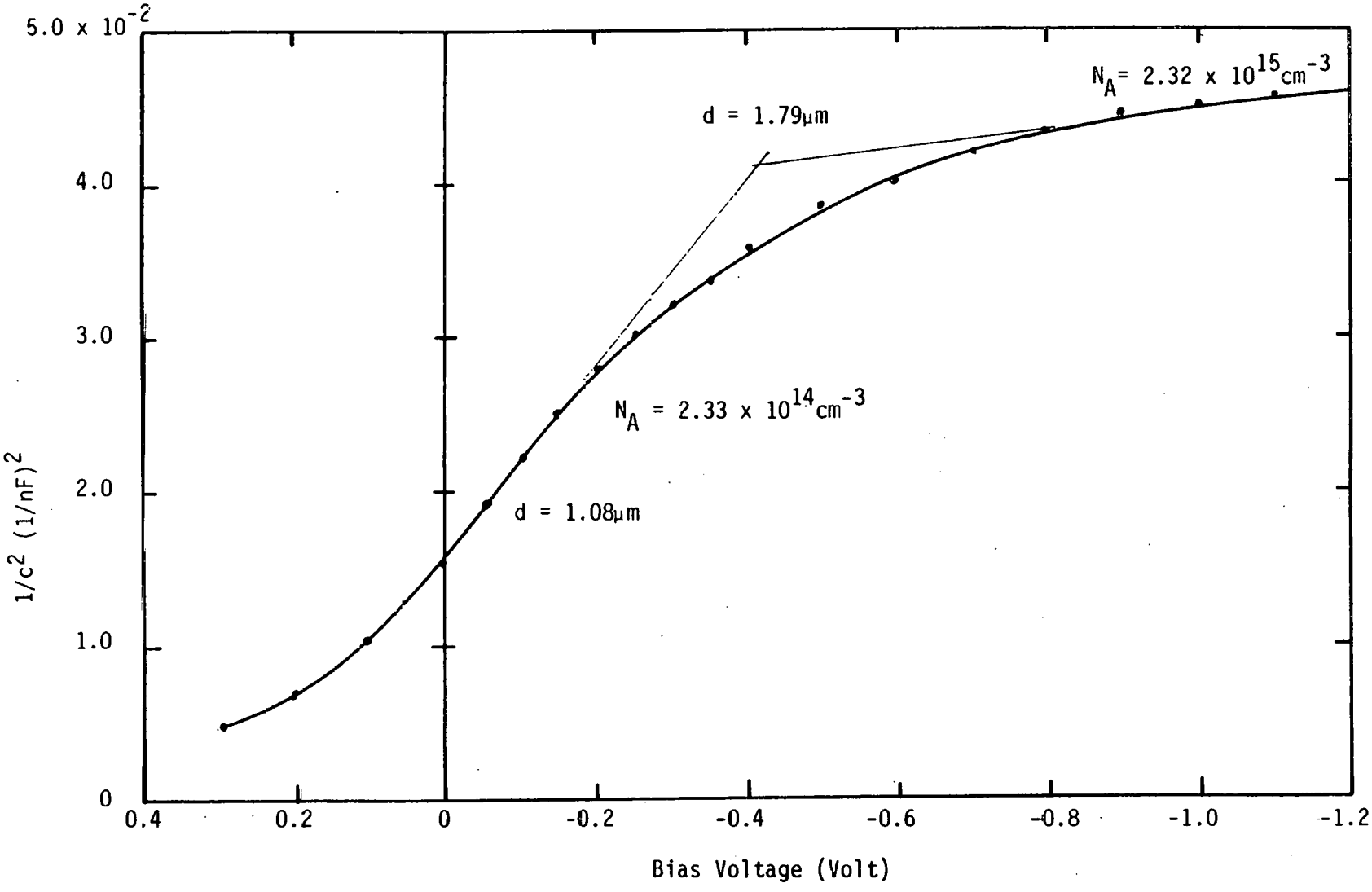


Figure 3.4-4 Cell Dark C-V Characteristics Before Heat Treatment

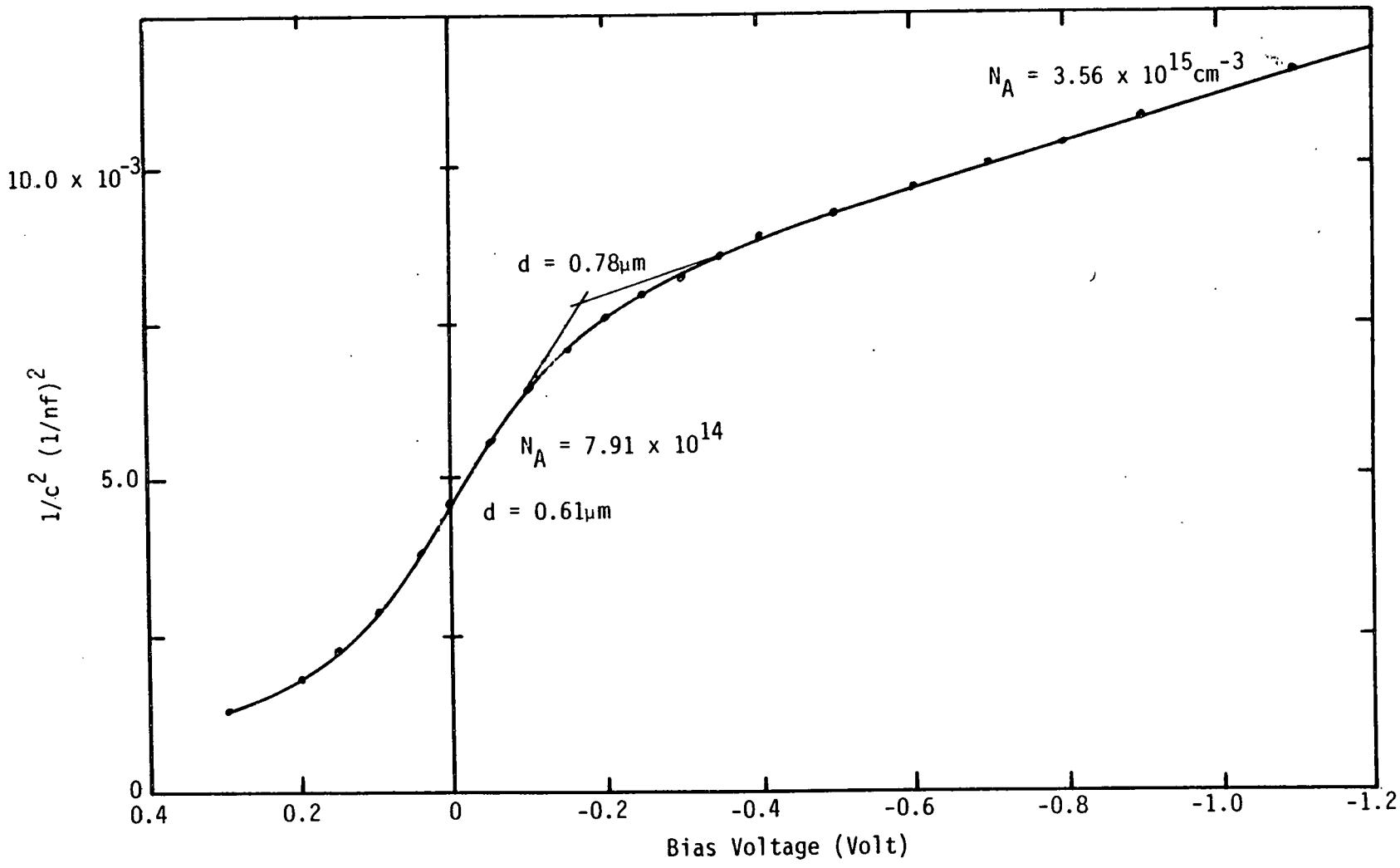


Figure 3.4-5 Cell Dark C-V Characteristics After Heat Treatment

The reasons for the cell non-exponential forward dark I-V characteristics (an inflection point and tendency to saturate at large forward bias), the smaller capacitance, and the larger layer thickness before annealing is presently unknown.

Since manual data taking was a tedious and time consuming job, detailed measurements of cell characteristics during heat treatments were only done after the completion of automatic measurement system near the end of the program.

Four cells were prepared from two substrates (two cells from each substrate) and divided into two groups. Each group consisted of two cells (one cell from each substrate). The two groups were heat treated in oxygen and hydrogen separately at 200°C in 10 minute steps. Before and after each step of heat treatment, cell characteristics (light and dark I-V, C-V, and spectral response) were measured.

Results of a typical set of measurements from one cell after a first bake in O_2 for 10 minutes are shown in Figures 3.4-6 to 3.4-9. In Table 3.4-2, the light I-V measurements are summarized. The light intensities, except for the 100 mW/cm^2 case, were not calibrated. Measurements at these uncalibrated intensities were used to obtain the diode quality factor (A-Fac.) and reverse saturation current from the V_{oc}-I_{sc} data. The light I-V curves are shown in Figure 3.4-6. In Figure 3.4-7, the cell dark current is semilogrithmically ploted versus voltage in both directions. For this particular cell, two I-V mechanisms were clearly seen. The diode quality factor and reverse saturation current obtained from a single roughly fitted straight line (as shown by dotted line in Figure 3.4-7) were quite different from the V_{oc}-I_{sc} measurement. The results of the capacitance measurements are presented in a $1/C^2$ versus voltage plot as shown in Figure 3.4-8. Typically, three segments of straight lines could be fitted. If we assume the junction to be one sided in $CuIuSe_2$ and the relative dielectric constant of $CuInSe_2$ to be 12, the doping densities, barrier heights and the depletion width at zero voltage for these three regions can be calculated as indicated at the side of the figure. From the interception of these straight lines, the widths of these regions from the junction can be obtained. As shown in the figure the widths of region (3) and region (2) were 0.685 μm and 1.24 μm, respectively. The spectral response of the quantum efficiency is shown in Figure 3.4-9. The short and long wavelength cut-offs correspond to the CdS and $CuInSe_2$ band gaps, respectively. The structure at 960 nm may be due to the spin-orbit split valance band to conduction band transition as discussed in Sec. 3.5.4.

Table 3.4-2. A Summarization of Cell Light I-V Measurements After 10 Minutes Bake in Oxygen at 200°

TEST 738B2
7/9/1982 07:16:00
BAC SAMPLE: 738B
TEMPERATURE: 25.0 Deg C
Total Area 1.000 cm^2
The base is P type
REMARK: IS BAKE IN 02 AT 200 DEG C FOR 10 MIN

CURVE#	INTENSITY (mW/cm^2)	EFFICIENCY (%)	VOC (Volt)	ISC (Amp)	VMAX (Volt)	IMAX (Amp)	FILL FACTOR
1	100.00	6.59	.3736	3.3491E-02	.252	2.615E-02	.5264
2	50.00	6.81	.3505	1.7571E-02	.244	1.397E-02	.5529
3	25.00	7.76	.3314	1.0478E-02	.236	8.210E-03	.5589
4	10.00	6.21	.2915	3.9675E-03	.208	2.989E-03	.5367
5	0.00	0.00	.0001	2.2126E-07	0.000	0.000E+00	0.0000

A_FAC= 1.5017 Io= 2.0230E-06 Amp SIGMA=3.222E-02

INTENSITY1 (mW/cm^2)	INTENSITY2 (mW/cm^2)	DELTA_I (Amp)	Rs (Ohm)
100.00	50.00	7.028E-03	2.490
100.00	50.00	1.054E-02	2.268
100.00	50.00	1.406E-02	2.184
100.00	50.00	1.757E-02	2.114
100.00	25.00	4.191E-03	2.865
100.00	25.00	6.287E-03	2.605
100.00	25.00	8.382E-03	2.423
100.00	25.00	1.048E-02	2.323
100.00	10.00	1.587E-03	3.597
100.00	10.00	2.380E-03	3.419
100.00	10.00	3.174E-03	3.088
100.00	10.00	3.967E-03	2.941

SHUNT= 893.8 Ohm SIGMA=5.5787E-04
SHUNT= 871.5 Ohm SIGMA=4.4245E-04
SHUNT= 856.5 Ohm SIGMA=3.5277E-04
SHUNT= 842.6 Ohm SIGMA=2.9350E-04

AVERAGE SHUNT Rsh= 866.1 Ohm

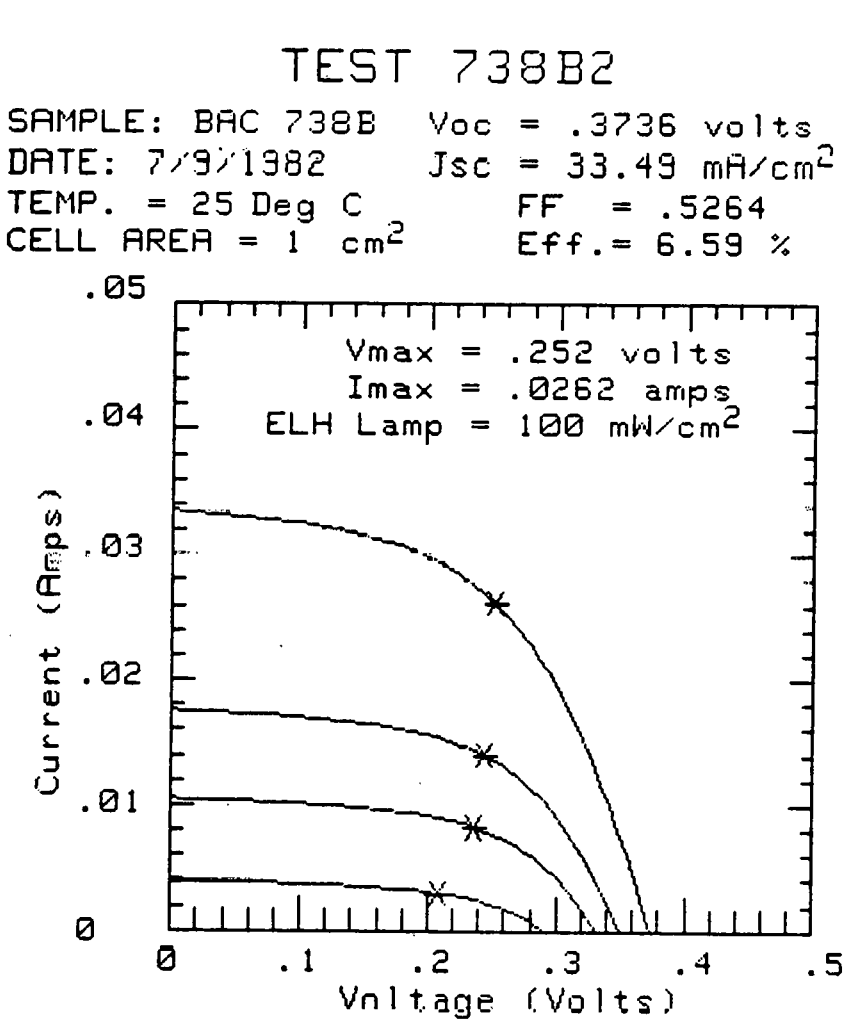


Figure 3.4-6 Cell Photovoltaic Response After 10 Minutes Bake in Oxygen at 200°C

DIODE QUALITY FACTOR =2.67E+00

DIODE SATURATION CURRENT =3.42E-05 Amp

SHUNT RESISTANCE =7.64E+02 Ohm

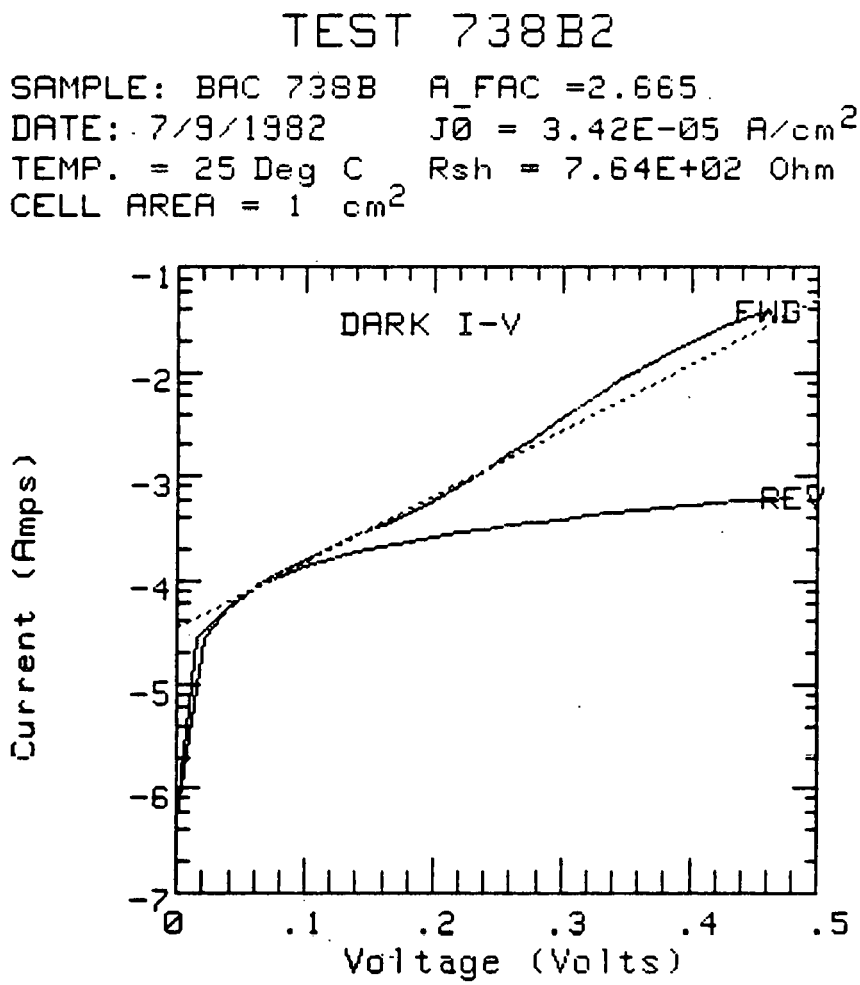


Figure 3.4-7 Cell Dark I-V Characteristics After 10 Minutes Treatment in Oxygen at 200°C

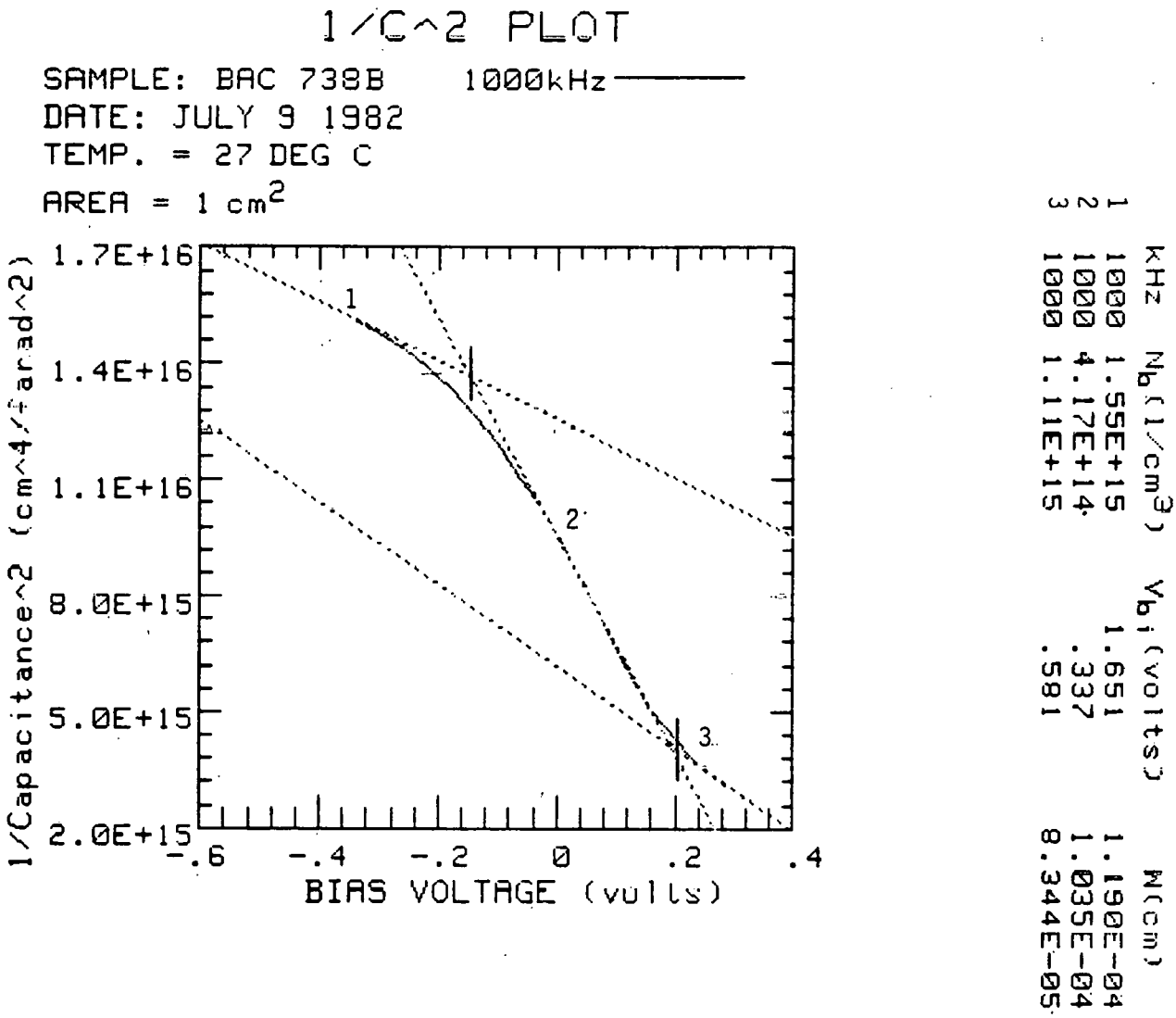


Figure 3.4-8 Cell Capacitance Characteristics After 10 Minutes Bake in Oxygen at 200°C

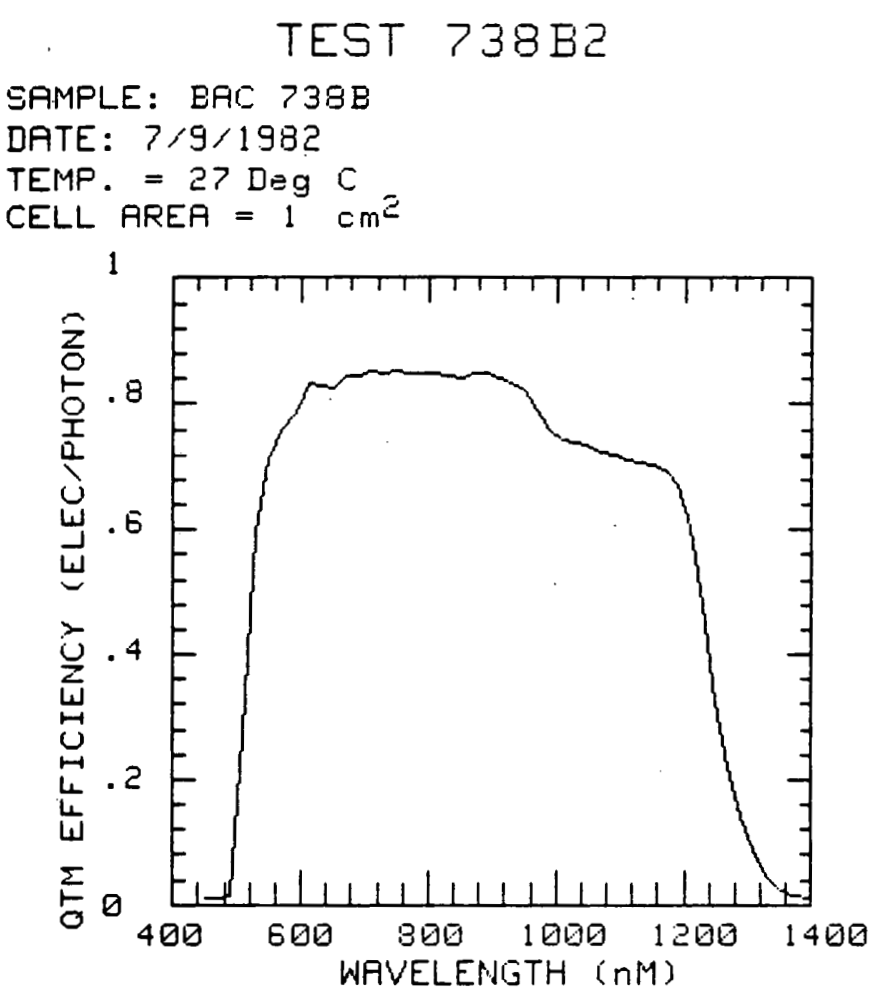


Figure 3.4-9 Cell Spectral Response of Quantum Efficiency After Bake in Oxygen for 10 Minutes at 200°C

The results of the photovoltaic responses, diode properties and capacitance characteristics of these four cells before and after each step of heat treatments are summarized in Table 3.4-3 to Table 3.4-6. No structural change was observed in the spectral response results. Only the level changes corresponding to the I_{sc} variations due to the heat treatments.

The above results are seen to agree with the earlier measurements. Cells baked in oxygen show a steady increase of V_{oc}, I_{sc}, F.F. and η, and a decrease of R_s (Table 3.4-3(A) and -5(A). The dark I-V characteristics of cell 738A and B showed two-diode mechanisms. Therefore, the diode quality factors from the dark I-V curves were much higher than the values from the V_{oc}-I_{sc} measurement. The cells 682A and B initially had high series resistances. The short circuit currents of these two cells were less than the photogenerated currents. Hence, the initial diode factors and reverse saturation currents measured from V_{oc}-I_{sc} curve were much less than the values from the dark I-V curves. However, both the diode quality factors and reverse saturation currents decreased during oxygen heat treatments (Table 3.4-3(B) and -5(B). The capacitance measurements during oxygen heat treatments (Table 3.4-3(C) and -5(C)) showed that: (1) the carrier densities in all three regions increased during the bakes; (2) the depletion widths at zero bias and the depths from the junction of region 2 and region 3 are reduced by the heat treatments.

In contrast, cells baked in hydrogen (Table 3.4-4 and -6) show the increase of I_{sc}, nearly constant or small increase of V_{oc}, and reduction of F.F. At the same time, no appreciable change of R_s, diode quality factors and reverse saturation currents were observed. The same was done in the capacitance measurements. After 30 min. heat treatments in hydrogen, both cells, 738A and 682A, had a 10 min. treatment in oxygen. An appreciable increase of V_{oc}, F.F., and N_b, but a reduction of R_s, A, I_o, depletion widths and depth of regions 2 and 3 from the junction were observed.

These results clearly indicate that oxygen is an essential ingredient for improving the cell response during heat treatment. The detailed mechanism(s) involved at present is still unknown and will require further analysis of these data.

Table 3.4-3. Results of Cell 738B Heat Treatment in Oxygen at 200°C

(A) Photovoltaic Responses

Condition	η (%)	V_{oc}(V)	I_{sc}(mA)	F.F.	R_s(ohm)	R_{sh}(ohm)
Initial	5.56	0.361	30.26	0.509	2.86	4.58×10^{2}
O_2 10 min.	6.59	0.374	33.49	0.526	2.26	8.66×10^{2}
O_2 10 min.	7.04	0.379	33.95	0.548	2.03	1.37×10^{3}
O_2 10 min.	7.44	0.381	34.54	0.565	1.88	1.03×10^{3}
O_2 10 min.	7.56	0.388	34.46	0.566	1.93	9.95×10^{2}

(B) Diode Properties

Condition	From V_{oc}-I_{sc} Meas.		From Dark I-V Meas.	
	A	I_o (A)	A	I_o (A)
Initial	1.55	3.23×10^{-6}	3.77	1.40×10^{-4}
O_2 10 min.	1.50	2.02×10^{-6}	2.67	3.42×10^{-5}
O_2 10 min.	1.46	1.38×10^{-6}	2.94	3.09×10^{-5}
O_2 10 min.	1.37	6.82×10^{-7}	1.99	8.11×10^{-6}
O_2 10 min.	1.40	7.11×10^{-7}	1.91	5.57×10^{-6}

(C) Capacitance Characterstics

Condition	N_b (10^{14} cm^{-3})			V_{bi} (V)			Depletion Width(V=0) μm	(μm) Depth from Junction	
	Reg. (1)	Reg. (2)	Reg. (3)	Reg. (1)	Reg. (2)	Ref. (3)		Reg. (2)	Reg. (3)
Initial	4.76	2.19	4.96	1.01	0.30	0.52	1.35	1.92	1.04
O_2 10 min	15.5	4.17	11.1	1.65	0.34	0.58	1.04	1.24	0.69
O_2 10 min	12.4	4.41	11.8	1.24	0.34	0.61	1.01	1.22	0.69
O_2 10 min	13.3	4.55	13.5	1.23	0.32	0.58	0.96	1.17	0.63
O_2 10 min	12.6	4.97	13.3	1.08	0.33	0.58	0.94	1.15	0.62

Table 3.4-4. Results of Cell 738A Heat Treatment in Hydrogen at 200°C. Last step in Oxygen

(A) Photovoltaic Responses

Condition	n (%)	V_{oc}(V)	I_{sc}(mA)	F.F.	R_s(ohm)	R_{sh}(ohm)
Initial	6.13	0.370	30.26	0.548	2.59	1.25×10^{3}
H_2 10 min.	5.78	0.365	30.69	0.516	2.50	2.94×10^{3}
H_2 10 min.	5.87	0.366	31.24	0.514	2.52	3.50×10^{3}
H_2 10 min.	6.27	0.372	32.39	0.520	2.51	6.85×10^{3}
O_2 10 min.	7.44	0.381	34.30	0.570	1.84	8.65×10^{3}

(B) Diode Properties

Condition	From V_{oc}-I_{sc} Meas.		From Dark I-V Meas.	
	A	I_o (A)	A	I_o (A)
Initial	1.39	9.09×10^{-7}	3.26	6.34×10^{-5}
H_2 10 min.	1.51	2.38×10^{-6}	2.03	1.17×10^{-5}
H_2 10 min.	1.52	2.61×10^{-6}	2.00	1.10×10^{-5}
H_2 10 min.	1.45	1.44×10^{-6}	1.88	6.44×10^{-5}
O_2 10 min.	1.38	7.05×10^{-7}	1.65	2.40×10^{-6}

(C) Capacitance Characterstics

Condition	N_b (10^{14} cm^{-3})			V_{bi} (V)			Depletion Width(V=0) μm	(μm) Depth from Junction	
	Reg. (1)	Reg. (2)	Reg. (3)	Reg. (1)	Reg. (2)	Ref. (3)		Reg. (2)	Reg. (3)
Initial	4.65	1.66	4.87	1.17	0.22	0.44	1.33	2.06	0.92
H_2 10 min	12.1	2.38	5.34	2.53	0.37	0.60	1.47	1.70	1.00
H_2 10 min	10.7	2.78	9.56	1.61	0.31	0.65	1.21	1.47	0.80
H_2 10 min	11.9	2.18	6.03	2.36	0.34	0.59	1.43	1.66	0.93
O_2 10 min	14.6	3.29	12.9	1.68	0.28	0.60	1.07	1.28	0.66

Table 3.4-5. Results of Cell 682B Heat Treatment in Oxygen at 200°C

(A) Photovoltaic Responses

Condition	η (%)	V_{oc}(V)	I_{sc}(mA)	F.F.	R_s(ohm)	R_{sh}(ohm)
Initial	4.19	0.312	32.55	0.412	4.42	3.74×10^{3}
O_2 10 min.	6.77	0.377	35.35	0.509	2.92	2.60×10^{3}
O_2 10 min.	7.20	0.379	35.39	0.537	2.32	1.26×10^{3}
O_2 10 min.	7.33	0.384	35.68	0.536	2.55	1.61×10^{3}
O_2 10 min.	7.54	0.388	35.60	0.546	2.44	1.74×10^{3}

(B) Diode Properties

Condition	From V_{oc}-I_{sc} Meas.		From Dark I-V Meas.	
	A	I_o (A)	A	I_o (A)
Initial	0.65	2.32×10^{-10}	1.91	4.73×10^{-6}
O_2 10 min.	1.18	1.30×10^{-7}	1.65	1.70×10^{-6}
O_2 10 min.	1.24	2.29×10^{-7}	1.88	4.39×10^{-6}
O_2 10 min.	1.19	1.23×10^{-7}	1.73	2.16×10^{-6}
O_2 10 min.	1.19	1.07×10^{-7}	1.70	1.69×10^{-6}

(C) Capacitance Characterstics

Condition	N_b (10^{14} cm^{-3})			V_{bi} (V)			Depletion Width(V=0) μm	(μm) Depth from Junction	
	Reg. (1)	Reg. (2)	Reg. (3)	Reg. (1)	Reg. (2)	Ref. (3)		Reg. (2)	Reg. (3)
Initial			Not Measured						
O_2 10 min	2.61	0.62	1.95	1.82	0.33	0.67	2.65	3.17	1.84
O_2 10 min	6.73	1.0	3.30	2.59	0.30	0.55	1.99	2.29	1.19
O_2 10 min	10.7	1.27	4.33	3.31	0.29	0.53	1.73	2.07	1.01
O_2 10 min	6.88	0.88	3.78	2.84	0.27	0.55	1.99	2.38	1.16

Table 3.4-6. Results of Cell 638A Heat Treatment in Hydrogen at 200°C. Last step in Oxygen

(A) Photovoltaic Responses

Condition	η (%)	V_{oc}(V)	I_{sc}(mA)	F.F.	R_s(ohm)	R_{sh}(ohm)
Initial	2.14	0.238	23.98	0.374	4.75	3.2×10^{4}
H_2 10 min.	3.27	0.293	26.36	0.417	4.43	1.13×10^{4}
H_2 10 min.	3.80	0.311	27.82	0.439	3.78	5.25×10^{3}
H_2 10 min.	3.60	0.307	27.27	0.430	4.21	4.81×10^{3}
O_2 10 min.	4.59	0.328	29.90	0.468	3.74	1.44×10^{5}

(B) Diode Properties

Condition	From V_{oc}-I_{sc} Meas.		From Dark I-V Meas.	
	A	I_o (A)	A	I_o (A)
Initial	0.70	3.7×10^{-8}	1.79	9.37×10^{-6}
H_2 10 min.	1.01	2.82×10^{-7}	1.67	5.72×10^{-6}
H_2 10 min.	1.20	1.16×10^{-6}	1.82	8.80×10^{-6}
H_2 10 min.	1.10	4.78×10^{-7}	1.81	7.77×10^{-6}
O_2 10 min.	1.17	5.01×10^{-7}	1.50	2.32×10^{-6}

(C) Capacitance Characterstics

Condition	N_b (10^{14} cm^{-3})			V_{bi} (V)			Depletion Width(V=0) μm	(μm) Depth from Junction	
	Reg. (1)	Reg. (2)	Reg. (3)	Reg. (1)	Reg. (2)	Ref. (3)		Reg. (2)	Reg. (3)
Initial			Not Measured						
H_2 10 min	3.63	5.34	1.68	3.80	0.46	1.12	3.38	3.78	2.75
H_2 10 min	3.36	5.30	1.53	3.97	0.47	1.04	3.42	3.79	2.75
H_2 10 min	3.60	4.81	1.37	3.77	0.42	0.89	3.40	3.77	2.63
O_2 10 min	3.71	4.31	1.31	3.88	0.37	0.76	3.35	3.77	2.45

3.5 Cell Analysis and Modeling

3.5.1 Automatic Measurement System

In order to expand our cell analysis capability, an automatic measurement system has been set up as shown in Figure 3.5.1-1. The system can automatically measure the cell characteristics, compute the cell parameters, and store the information.

The measurement and control processor programmed by the desktop computer controls the necessary equipment to perform a designated measurement. Data taken from the equipment is fed back to the computer for computation and then stored either on tape or a flexible disc. Graphic presentations are prepared by a digital plotter.

The I-V measurement system as shown in Figure 3.5.1-2 is capable of taking I-V data either in dark or under illumination. The cell under test can be connected either to a curve tracer for a quick check or to the digital system for accurate measurement. A two channel digital electrometer (Keithley Model 619) is used to monitor the low currents (<15mA) of the test cell and a secondary standard cell. The voltage drop across a 0.25 ohm resistor is used to measure high current through the test cell. Software provided by SERI was modified to fit our computer system to control the measurement as well as to compute the cell parameters. The cell reverse saturation current, J_o, diode quality factor, A, series resistance, and shunt resistance can be determined from either dark measurement or I_{sc}-V_{oc} measurement. The cell photovoltaic characteristics are measured under simulated AM1 light from a ELH lamp which is constantly monitored by a secondary standard cell. Cell responses such as V_{oc}, J_{sc}, maximum power point, F.F. and efficiency are calculated by the computer.

The C-V measurements are programmed to measure the cell capacitance and conductance in parallel mode as functions of bias voltages and frequencies (from 10 KHz to 10 MHz). The system is shown schematically in Figure 3.5.1-3. The bias voltage is supplied from the analog output of the measurement and control unit. Results are presented in C-V, GV, I/C^2-V and I/C^3-V plots. Straight line fitting along the selected segments of I/C^2-V and I/C^3-V curves is analyzed by the computer. Results of the fitting give the doping density, or the gradient of the doping density, the barrier height, and the depletion width at zero bias voltage.

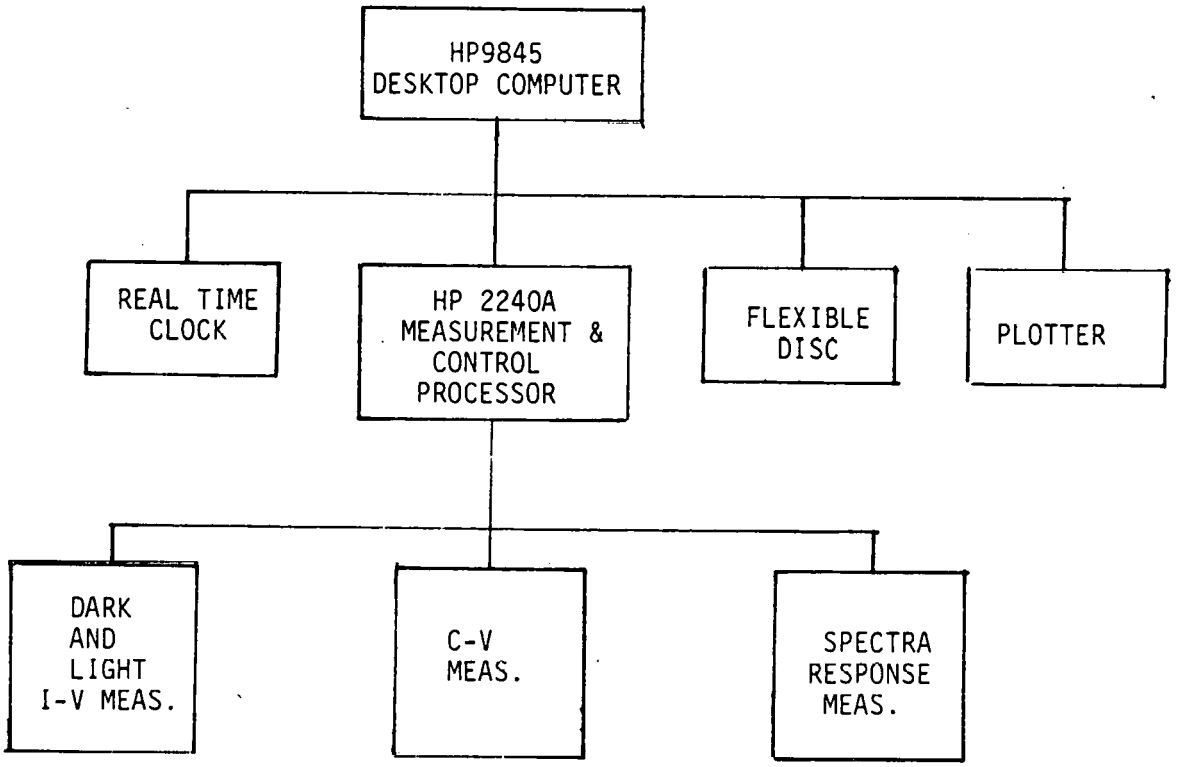


Figure 3.5.1-1. SCHEMATIC DIAGRAM OF THE AUTOMATIC MEASUREMENT AND CONTROL SYSTEM

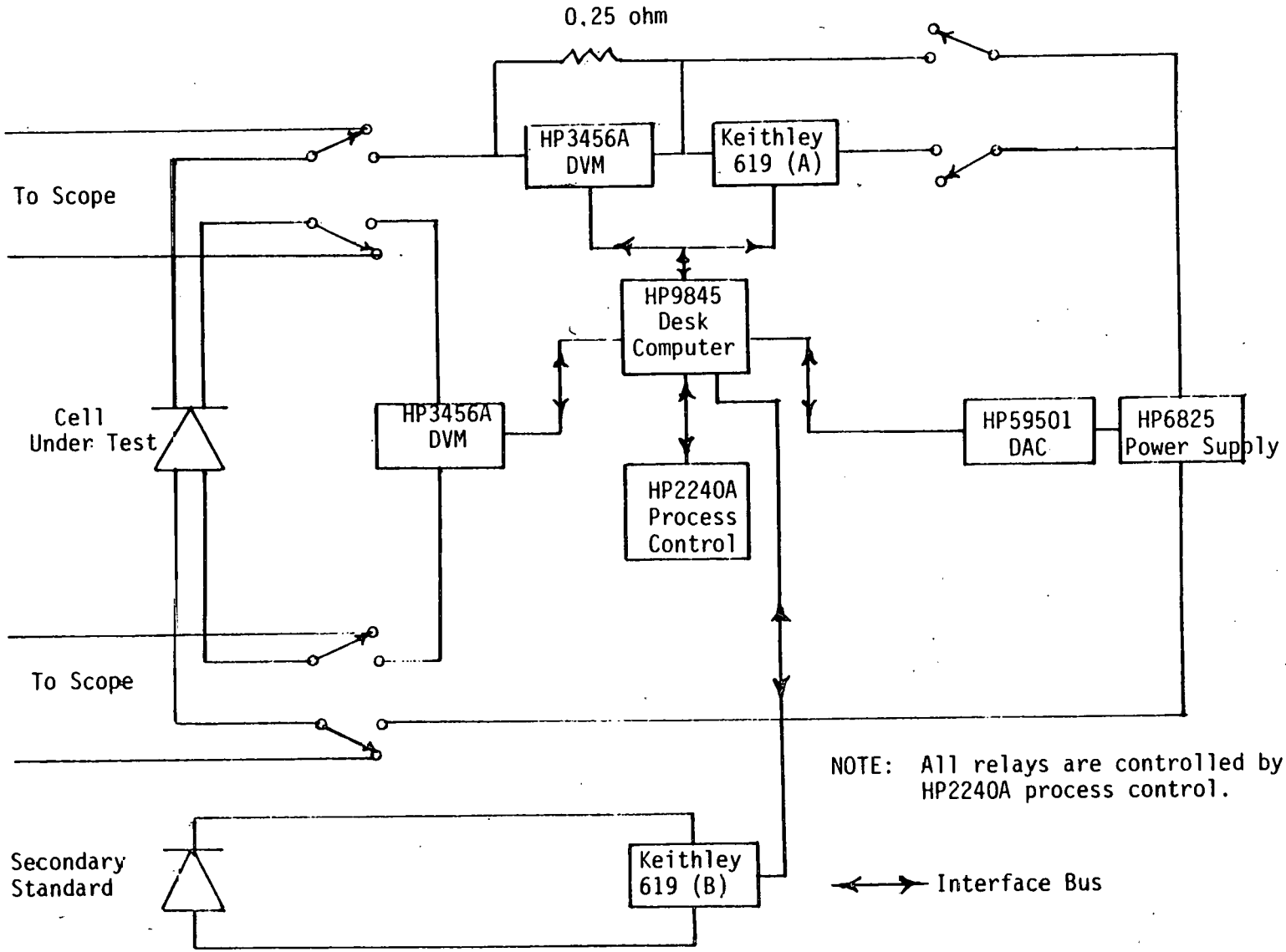


FIGURE 3.5.1-2. SCHEMATIC DIAGRAM OF LIGHT AND DARK I-V MEASUREMENT SYSTEM

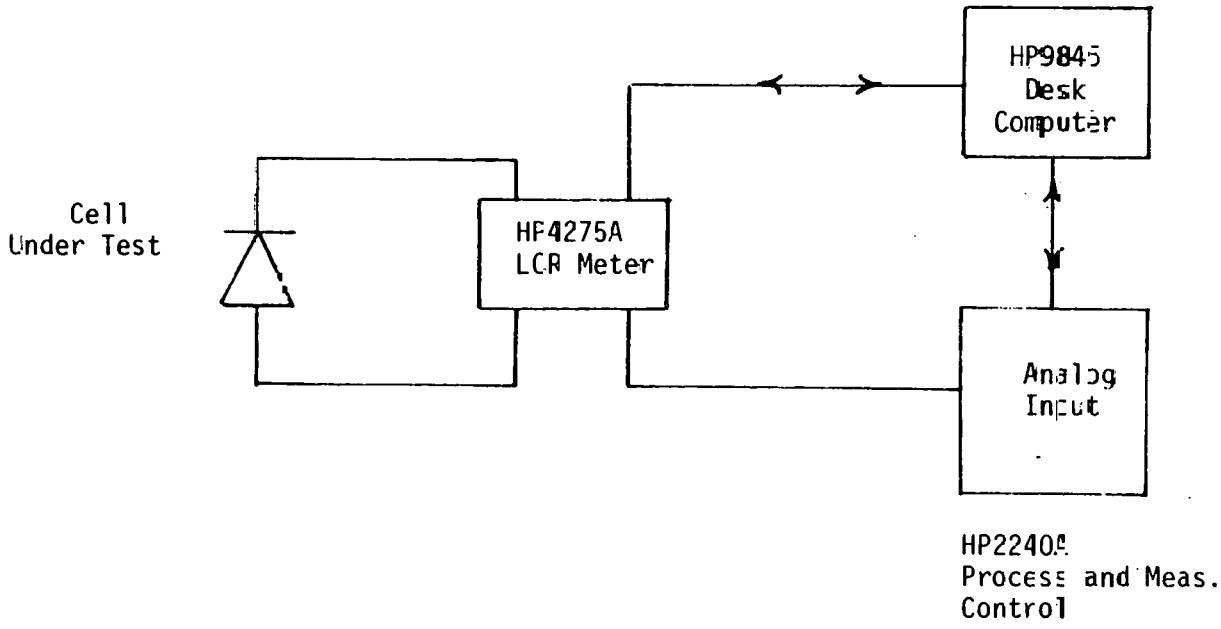


FIGURE 3.5.1-3. SCHEMATIC DIAGRAM OF CAPACITANCE MEASUREMENT SYSTEM

A cell spectral response measurement system has also been developed. A schematic diagram of the system is shown in Figure 3.5.1-4. Light from a DC powered tungsten source passes through a monochromator with two interchangeable gratings and a collimating lens and is intercepted by a light-chopping blade placed at 45° to the path of the incoming light beam. The transmitted beam illuminates the cell under test. The beam reflected from the chopper is monitored by a calibrated photovoltaic detector (either Si or Ge) to give a continuous measurement of the light intensity. All controls as well as data acquisitions and calculations are provided by a process measurement controller and a H-P desk computer. The system can measure the cell response within the wavelength range from 440 nm to 1800 nm. Typically, the cell spectra responsivity (Amp/W) and quantum efficiency (electrons/photon) are measured from 450 nm to 1400 nm. Integration of the measured cell responsivity over a AM1 solar spectrum can be performed by the computer to compare the short circuit current to the measured I_{sc} under ELH lamp.

3.5.2 CdS/$CuInSe_2$ Cells

Cell performance was greatly improved during the early part of this program with an efficiency of 9.67% under simulated AM1 illumination (ELH lamp. Standard Si-cell as reference) being achieved.

The as deposited cell had an efficiency of about 5% with V_{oc} = 325mV and J_{sc} = 31mA/cm^2. Immediately after 20 minute 200°C heat treatment in H_2/Ar, the cell performance improved to V_{oc} = 375mV, J_{sc} = 34mA/cm^2, η = 7.83% and F.F. = 0.61. Thereafter, the cell efficiency showed continuous improvement with time. After 25 days it reached a stable value of 8.85% as shown in Figure 3.5.2-1. The improvement of efficiency is mainly caused by a slowly increasing open circuit voltage and fill factor. The photovoltaic characteristics at the steady state are shown in Figure 3.5.2-2, which gives

$$V_{oc} = 396\text{mV} \qquad J_{sc} = 35\text{mA/cm}^2$$
$$\eta = 8.85\% \qquad \text{F.F.} = 0.64$$

The average total reflectance of the cell structure had been previously measured to be ~14% which was mainly from the front CdS surface (n = 2.2 - 2.3). A quarter-

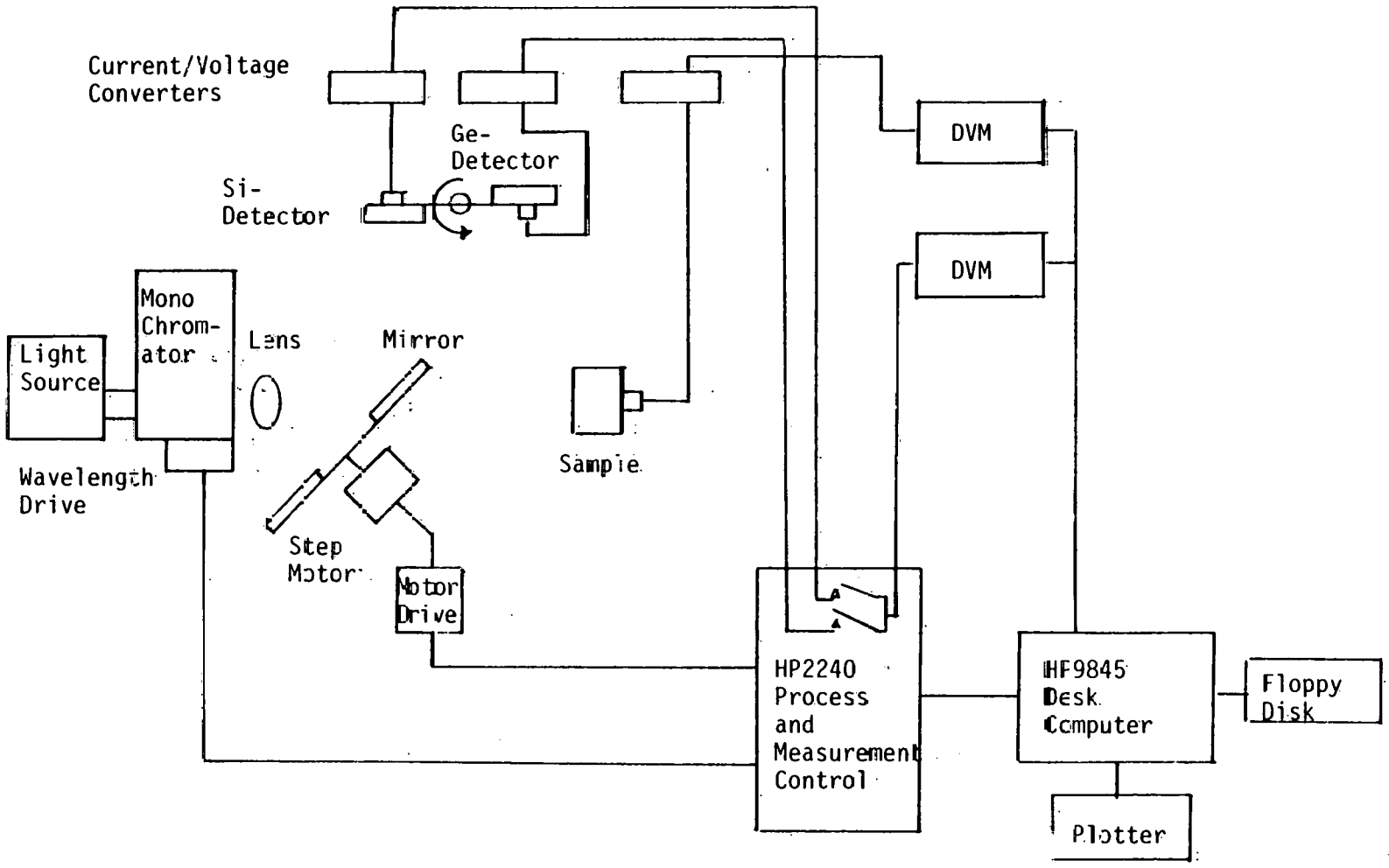


Figure 3.5.1-4 Schematic Diagram of Spectra Response Measurement System

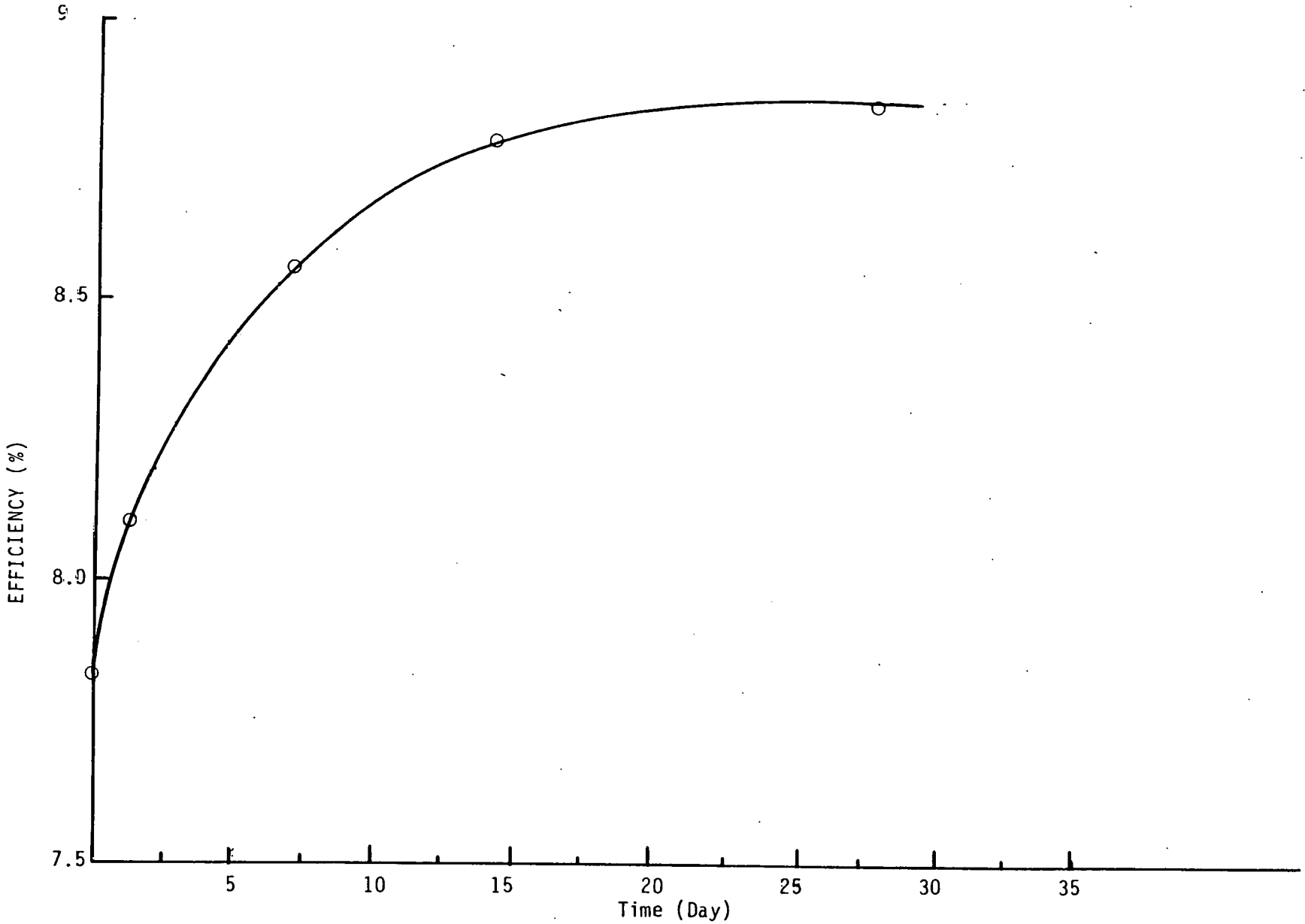


Figure 3.5.2-1 Efficiency as Function of Time Following Heat Treatment

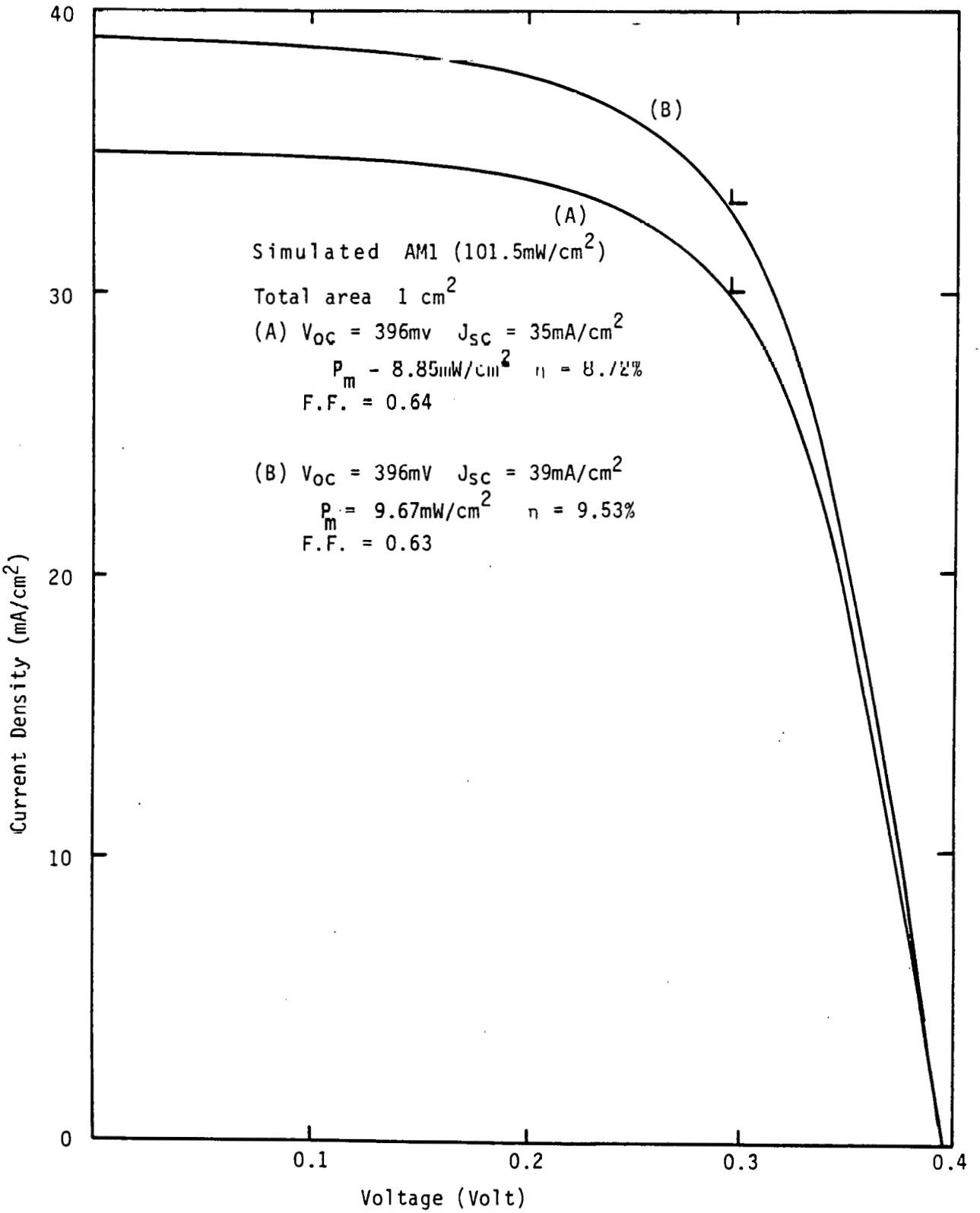


Figure 3.5.2-2 Photovoltaic Characteristics of a High Efficiency Cell Under Simulated AM1 (101.5mW/cm^2) illumination: (A) Without Antireflection Coating; (B) With SiO_x Coating

wavelength antireflection coating of SiO_x (n ~ 1.55) was designed for a wavelength of 0.85 m and evaporated onto the high efficiency cell. The light I-V characteristics with the SiO coating is shown in Figure 3.5.2-2 curve (B). The short circuit current increased from 35mA/cm^2 (without coating) to 39mA/cm^2, or more than a 10% improvement. The total area performances of the final cell were:

V_{oc}	= 396mV	J_{sc}	= 39mA/cm^2
V_{mp}	= 293mV	J_{mp}	= 33mA/cm^2
η	= 9.67%	F.F.	= 0.63

These measurements were made under ELH lamp simulated AM1 illumination. Excluding the 5% grid shading area, the active area efficiency was 10.15%. A similar cell from another substrate which showed 9.28% under the same illumination was measured under Seattle clear day sunlight (2:15 pm, 6/19/80). The intensity was measured to be 92.5mW/cm^2 by a standard Si cell. The cell characteristics were

V_{oc}	= 380mV	J_{sc}	= 35mA/cm^2
V_{mp}	= 280mV	J_{mp}	= 30mA/cm^2
P_m	= 8.4mW/cm^2		
η	= 9.1%	F.F	= 0.63

The efficiency under sunlight was 2% less than the measurement under the ELH lamp.

The two respresentative high efficiency cells, cell no. 442 η = 9.67% and cell no. 475 η = 9.28% measured at our laboratory, were measured under Xenon lamp solar simulator at NASA Lewis Research Center. With the best available reference cell (Cu_2S/CdS cell with Kapton cover) whose spectral response resembles the response of our cells, the measured photovoltaic performance were:

9.28% Cell (475)		9.67% Cell (442)	
I_{sc}	= 39.3mA	I_{sc}	= 38.8mA
V_{oc}	= 391mV	V_{oc}	= 404mV
I_{max}	= 33.5mA	I_{max}	= 298mV
V_{max}	= 286mV	P_{max}	= 9.89mW
P_{max}	= 9.58mW	F.F.	= 0.630

F.F. = 0.624 Eff. = 9.89%

Eff. = 9.58%

These devices exhibited spectral characteristics similar to those reported previously[14]. As shown in Figure 3.5.2-3, the quantum efficiency as a function of wavelength measured at NASA Lewis Center was fairly flat at least within the measurement range $0.6 \lesssim \lambda \lesssim 1.0$ m.

The dark I-V characteristics of the high efficiency cell in a semilog plot was a straight line which saves the diode factor, A, 1.285 and the reverse saturation current, J_o, 1.8×10^{-7} A/cm^2.

The response of the high efficiency cell without SiO coating as a function of light intensity was measured by a set of neutral density filters (various thickness of Mo on glass). These filters have a nearly flat transmittance over the $0.5 < \lambda < 2.0$ μm in contrast to the previous Kodak gelatin filters which work only in the visible range. The measured fill factor as a function of light intensity in terms of J_L/J_o is shown as black dots in Figure 3.5.2-4. The intensity range was from 100mW/cm^2 ($J_L/J_o = 1.94 \times 10^5$) down to < 10mW/cm^2 ($J_L/J_o = 10^4$).

The smooth curve is the calculated F.F. as a function of J_L/J_o using the measured values of $R_s = 1.2\Omega$, $R_p \sim 10^5\Omega$, A = 1.85, $J_o = 1.8 \times 10^{-7}$ A/cm^2 and T = 300°K from Mitchell's theory[15]. The experimental and calculated values agree very well indicating the fill factor was limited by the series resistance. If the series resistance could be reduced to 0.5 Ω(as indicated in the upper curve in Figure 3.5.2-4), the fill factor could be increased to 0.69 at the AM1 condition. Actually, small diodes with high fill factor of 0.68 were observed. If the high 0.69 fill factor could be realized in the existing high efficiency cell (η= 9.67%) the total area efficiency could be increased to 10.59%.

We also observed that the open circuit voltage of our cells could be improved by 20mV by lowering the CdS resistivity to ~ 10-20 ohm-cm by raising the CdS source temperature (as shown by comparing Figure 3.5.2-5 and Figure 3.5.2-6). Such a trend is consistent with theoretical expectations and it would be highly interesting to extend these studies to increase the V_{oc} and thus to improve the efficiency if some means

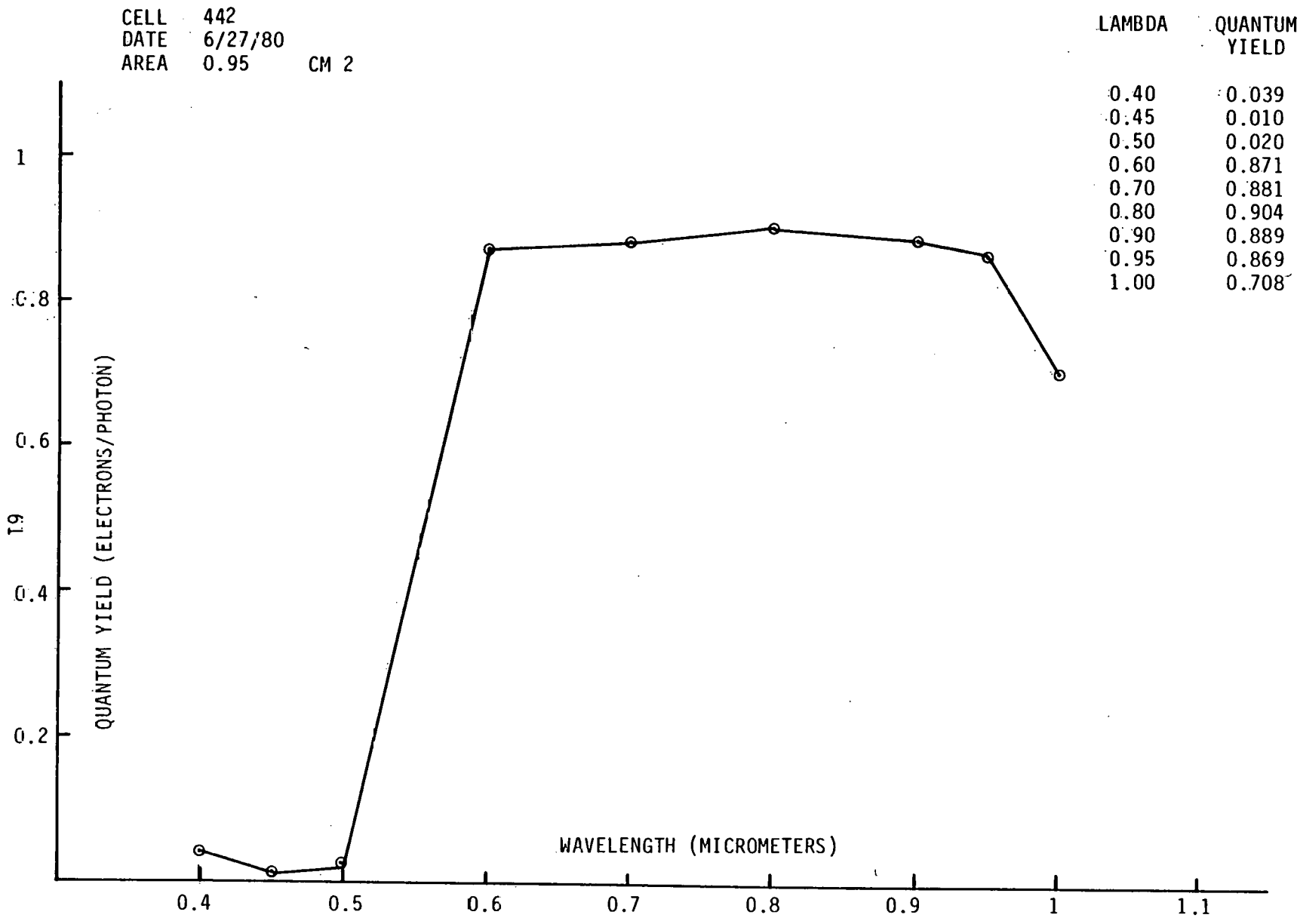


Figure 3.5.2-3 Quantum Efficiency as a Function of Wavelength for the High Efficiency Cell

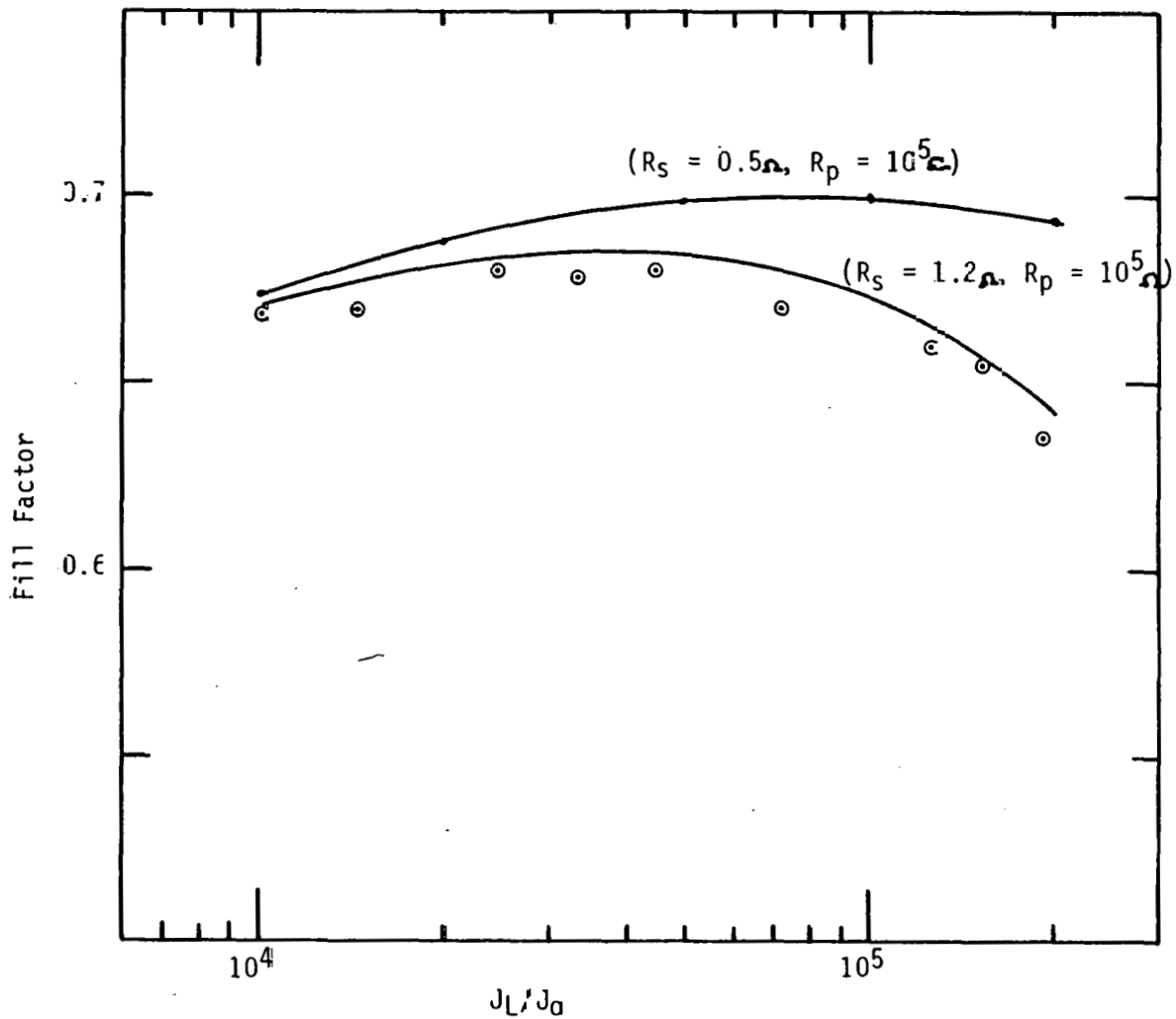


Figure 3.5.2-4 Experimental and Calculated Values of Fill Factor as a Function of J_L/J_0 for the High Efficiency Cell with $R_S = 1.2\Omega$, $R_p \sim 10^5\Omega$, and $J_0 = 1.8 \times 10^{-7} A/cm^2$, $A = 1.285$, and $T = 300^0K$

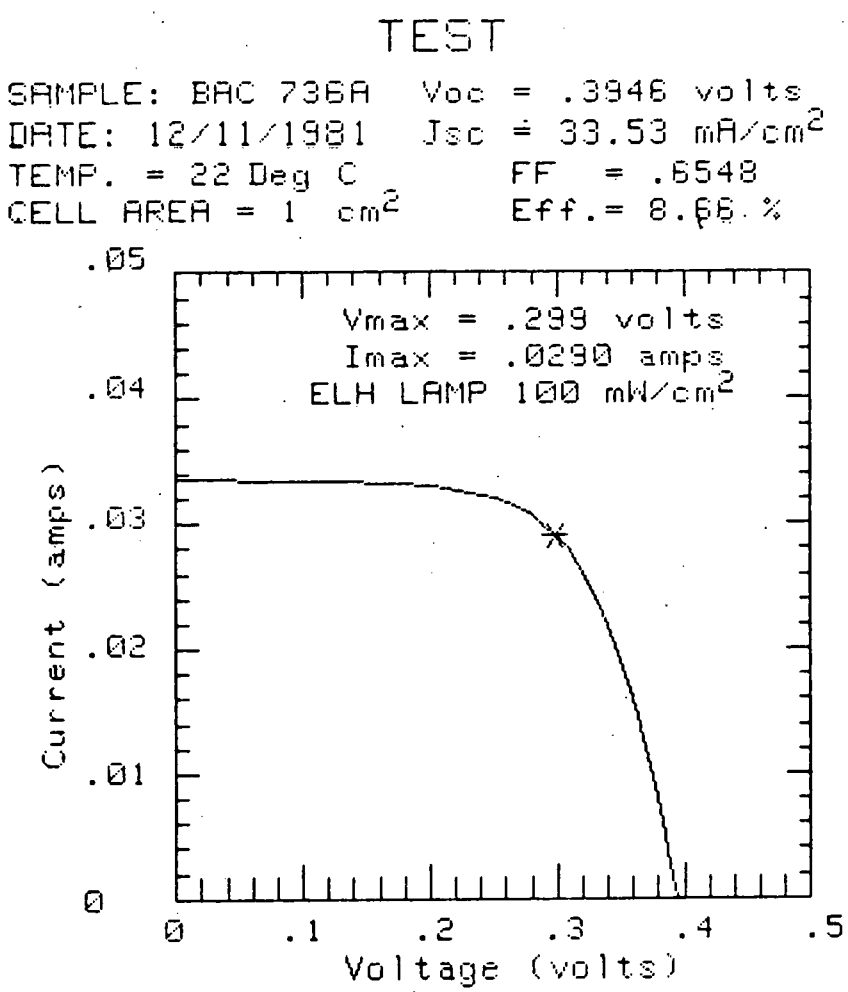


Figure 3.5.2-5 Photovoltaic characteristics of cell with $CuInSe_2$ film deposited at two temperatures, 350°C and 450°C. CdS source temperature: 1025°C

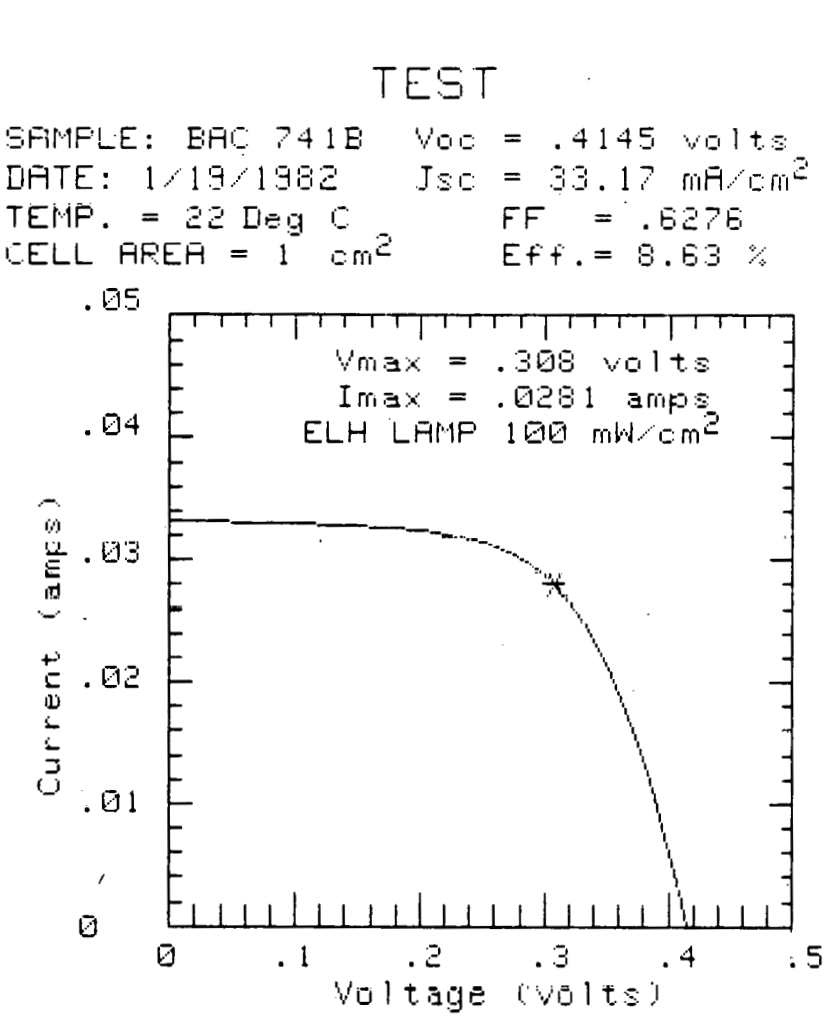


Figure 3.5.2-6 Photovoltaic characteristics of cell with $CuInSe_2$ film deposited at two temperatures, 350°C and 450°C (standard process). CdS source temperature: 1210°C.

(other than In doping) could be developed to prepare the CdS layers with appreciably lower resistivities (~0.1 ohm-cm).

Cell characteristics were measured with different selenide deposition temperatures (350^{o}-450^{o}C) with fixed CdS source temperature. The typical photovoltaic responses are shown in Figure 3.5.2-7 to Figure 3.5.2-9.

Cells made with selenide deposited at 350^{o}C showed low open circuit voltage and short circuit current (Figure 3.5.2-7). The cell performance was improved by still depositing the selenide at 350^{o}C but subsequently in-situ baked at 450^{o}C for 10 minutes before applying the CdS (Figure 3.5.2-8). Selenide films deposited at two temperatures, i.e., 300^{o}C followed by 400^{o}C gave cell performances (Figure 3.5.2-9) comparable to cells prepared with the standard two-temperature (350^{o}C/450^{o}C) selenide film (Figure 3.5.2-6).

The lower temperature process was adopted in the planetary system. A 7.5% cell was made in the planetary system with selenide film deposited at 400^{o}C. The photovoltaic response is shown in Figure 3.5.2-10. The higher V_{oc} of this cell (as compared to Figure 3.5.2-9) is due to the mixed sulfide window material. The J_{sc} could be improved by optimizing the selenide film composition.

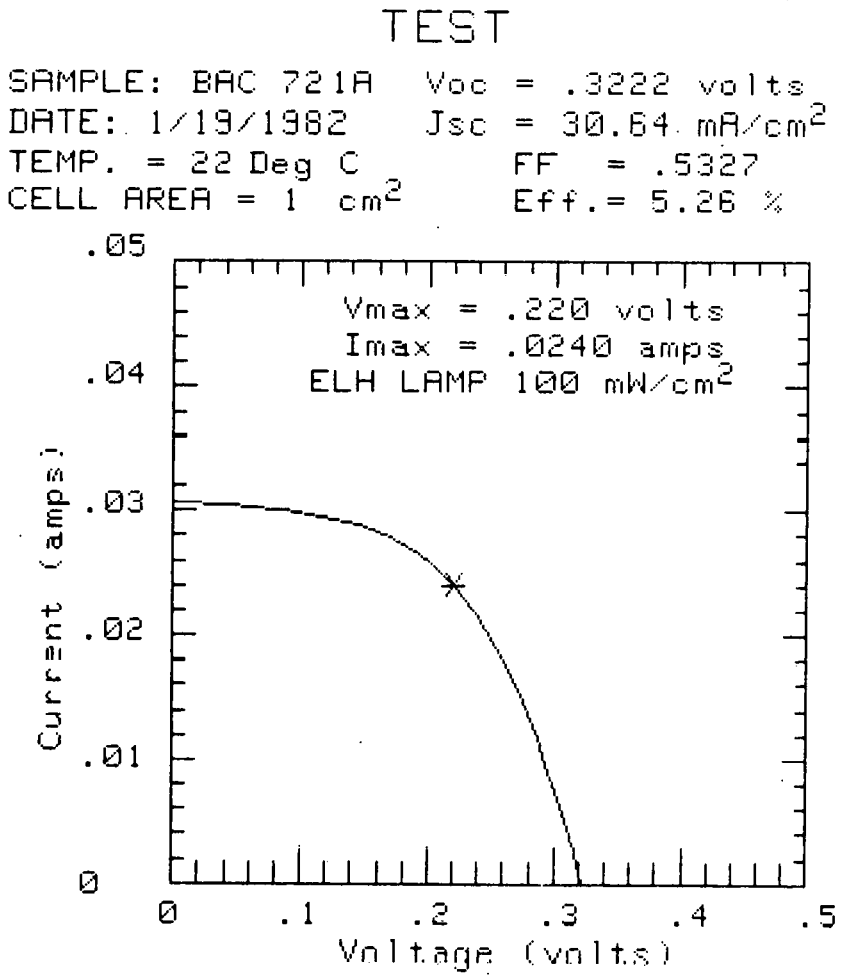


Figure 3.5.2-7 Photovoltaic characteristics of cell with $CuInSe_2$ film deposited at 350^0C

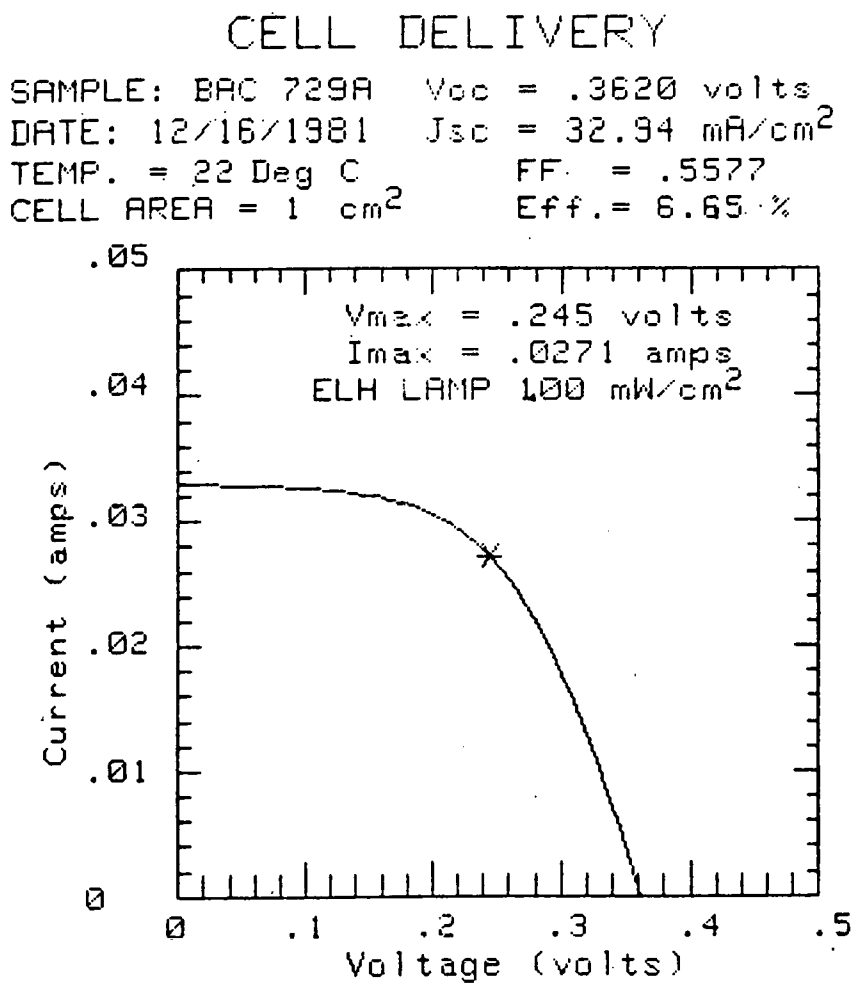


Figure 3.5.2-8 Photovoltaic characteristics of cell with $CuInSe_2$ film deposited at 350°C and in situ baked at 450°C for 10 min.

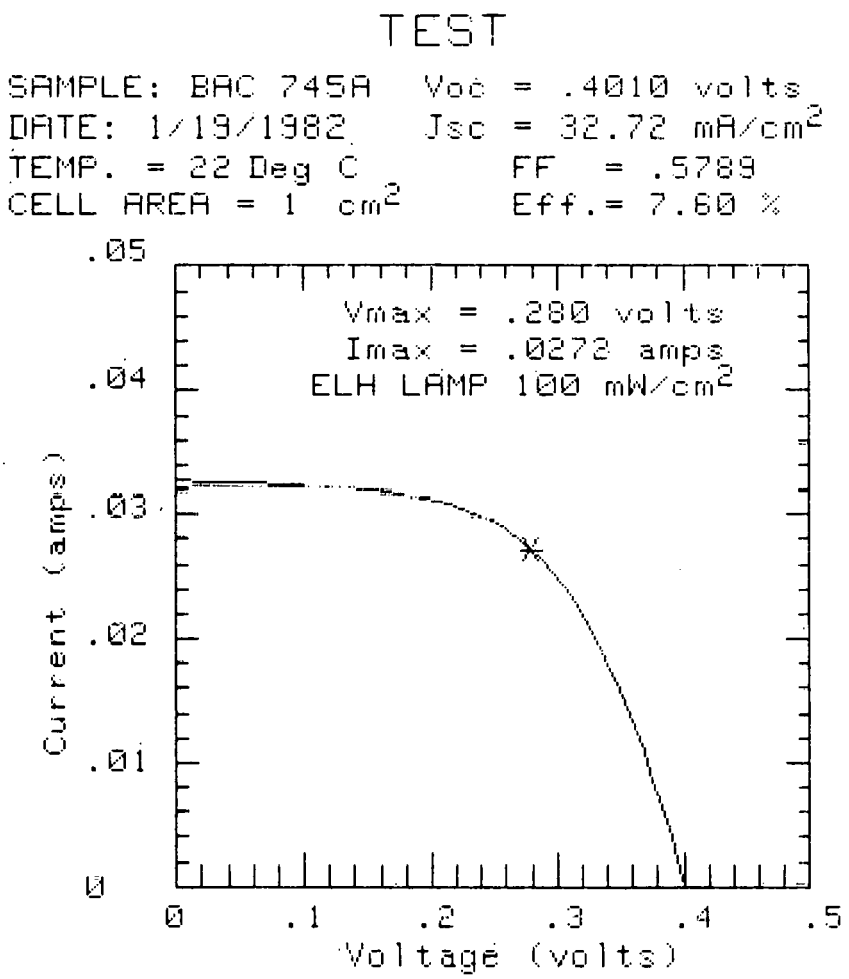


Figure 3.5.2-9 Photovoltaic characteristics of cell with $CuInSe_2$ film deposited at two temperatures, 300°C and 400°C.

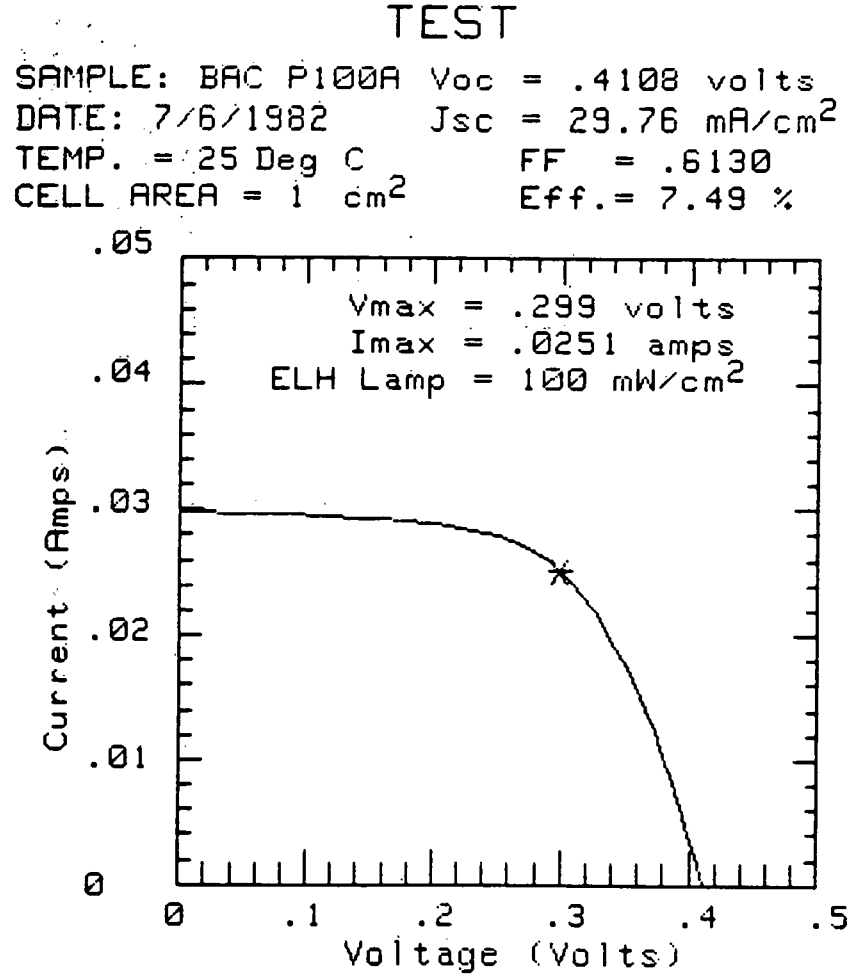


Figure 3.5.2-10 The Photovoltaic Response of Cell With $CuInSe_2$ Film Deposited in Planetary System at 400°C

3.5.3 $Zn_xCd_{1-x}S/CuInSe_2$ Cells

The benefits of using the mixed sulfide ($Zn_xCd_{1-x}S$) film as window material has been discussed in Section 3.2.

An encouraging improvement of cell performance was observed by incorporation of the mixed sulfide with Zn content about 15% in the cell. Open circuit voltage over 0.41 volt together with fill factor as high as 0.654 were obtained. Typical cell characteristics under simulated AM1 illumination are shown in Figures 3.5.3-1 and -2.

The 1 cm^2 cell had open circuit voltage of 0.410V with short circuit current comparable to earlier cells. The open circuit voltage did not degrade with time in contrast to the $Cu_2S/ZnCdS$ cell. The fill factor of this cell (0.654) was the highest value ever obtained. Although the series resistance (1.3 ohm) was about the same as earlier cells, analysis revealed that the cell had $J_o = 1.5 \times 10^{-7}$ A/cm^2 and diode factor, A, of 1.3. The higher voltage and better fill factor were derived by lowering the J_o as a result of using the mixed sulfide which had better lattice and electron affinity matching with the $CuInSe_2$. This cell exhibited an efficiency of 8.85%.

Large 8 cm^2 cells with efficiency over 7% without antireflection coating were produced. The 8 cm^2 cells produced in the same substrate as the above 1 cm^2 cell had the following performance

$$V_{oc} = 0.412$$
$$I_{sc} = 250mA$$
$$\eta = 7.63\%$$
$$F.F. = 0.59$$

under simulated AM1 illumination. The 8 cm^2 cell thus had about the same V_{oc} as the 1 cm^2 cell. Since the grid transparencies of the two cells were different, the calculated active area short circuit current densities are shown in Table 3.5.3-1.

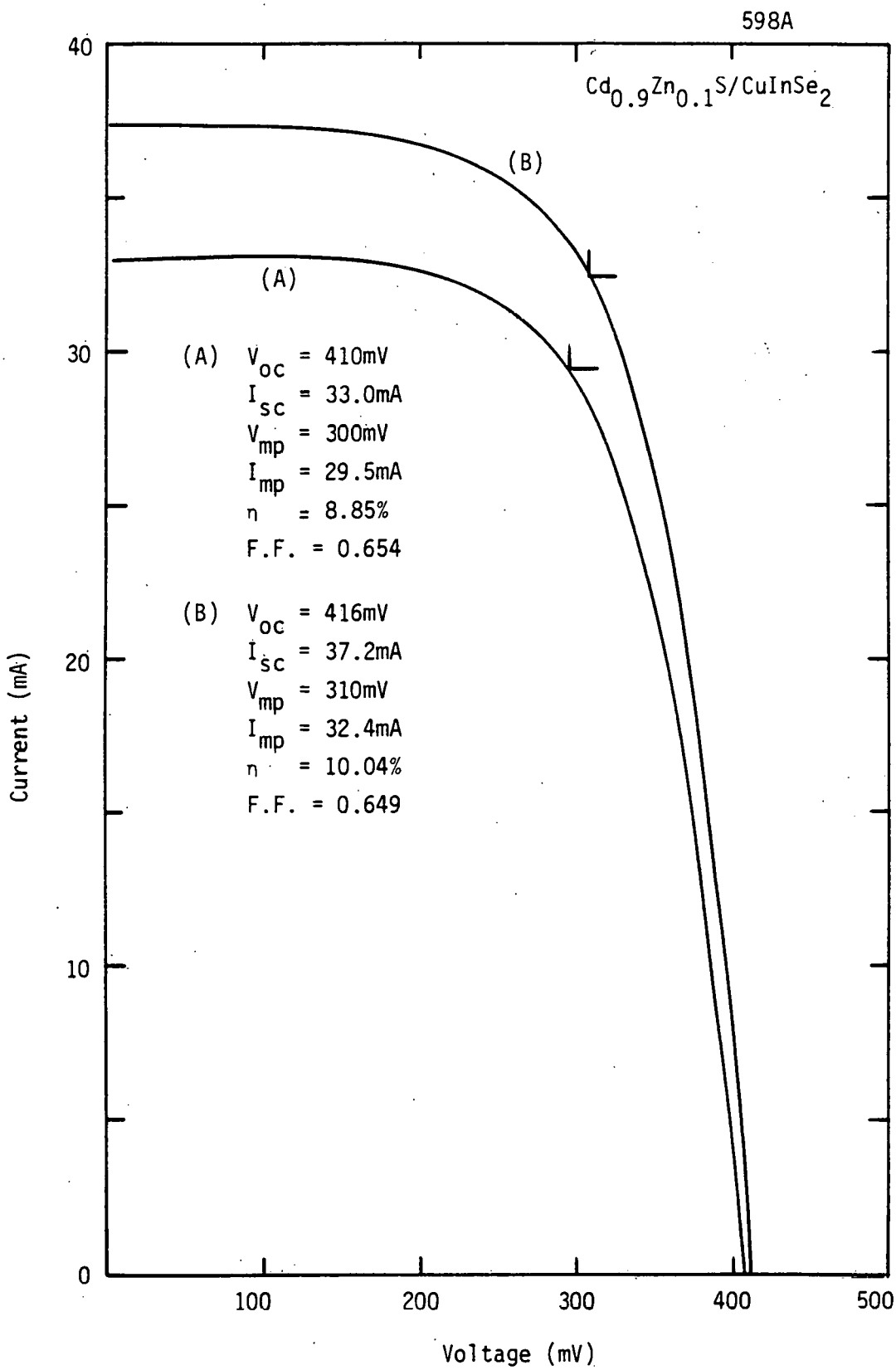


Figure 3.5.3-1 Photovoltaic Characteristics of a High Efficiency $1cm^2$ Cell Under Simulated AM1 Illumination: (A) Without Antireflection coating; (B) With 950Å SiOx

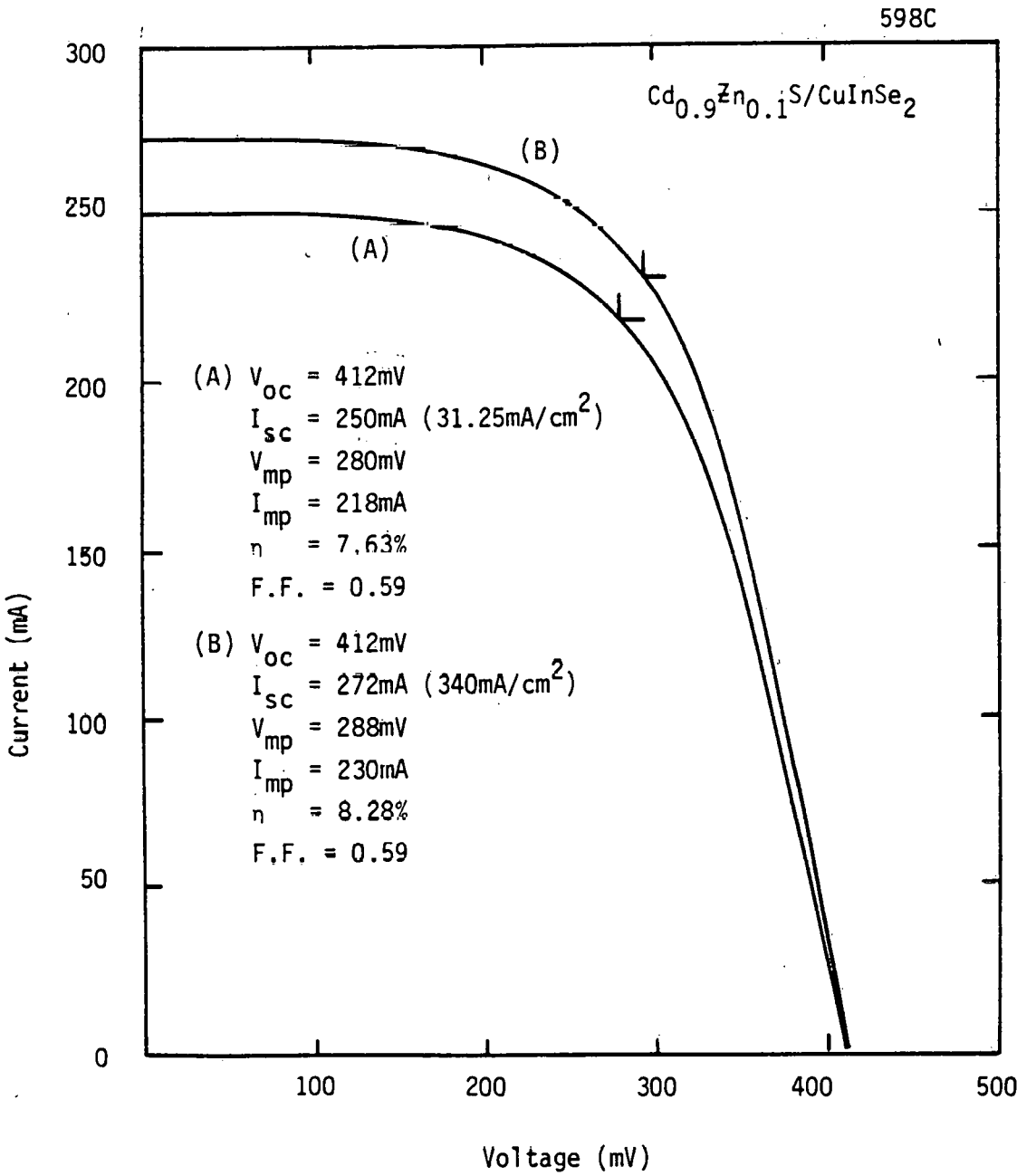


Figure 3.5.3-2 Photovoltaic Characteristics of a High Efficiency 8cm^2 Cell Under Simulated AM1 Illumination: (A) Without Antireflection Coating; (B) With 1000Å SiOx Coating

TABLE 3.5.3-1 Short Circuit Current Densities for 1 cm^2 and 8 cm^2 Area Thin-Film Cells

Area	I_{sc} (total area)	Grid Transparency	J_{sc} (active area)
1 cm^2	33mA	95.4%	34.59mA/cm^2
8 cm^2	250mA	91.5%	34.15mA/cm^2

The near identical J_{sc} (active area) of these two cells demonstrated that the mixed sulfide and selenide films were uniform and large area cells can be produced without a loss in performance. The lower efficiency of the 8 cm^2 cell (7.25%) was mainly caused by series resistance from the base metallization which lowered the fill factor to 0.60.

The efficiency of these cells with AR coatings measured in our laboratory reached 10.04% (1 cm^2 cell) and 8.28% (8 cm^2 cell). The high efficiency 1 cm^2 cell has been measured at SERI. Their results are summarized as: (SERI M&E Report No. 201)

J_{sc}(mA/cm^2)	V_{oc}(mV)	F.F.(%)	η (%)	Notes
36.30	417.6	65.1	9.81	Filtered Zenon
39.44	423.8	64.6	10.79	ELH Lamp
36.33	418.1	65.3	9.93	After 1 hour filtered Zenon

Our measurements were, thus, seen to agree very well with the SERI results and confirmed the high performance of the device.

With the Zn-content in the sulfide near the calculated optimum composition, we expected the improvement of V_{oc} to be larger than that obtained. As observed in development of the Cu_2S/ZnCdS cell, the dominant mechanism in improvement of V_{oc} is the electron affinity match between the two materials. As indicated in the last section, the estimated sulfide composition having a χ-match may be unreliable. In fact, if we use the χ values of CdS and ZnS (Table 3.2-1), the χ value of the mixed sulfide from a linear interpolation should be:

$$\chi_{Zn_xCd_{1-x}S} = 4.5 - x(4.5 - 3.9)\ eV$$

Accordingly, the composition of the mixed sulfide having χ-match with the selenide should have a x value of about 0.33 instead of 0.17. This value agrees, possibly only by coincidence, with the reported composition of mixed sulfide, $Zn_{0.3}Cd_{0.7}S$, used on a thin-film $CuInSe_2$ heterojunction cell which has shown the highest V_{oc}, 0.53V.[11] This indicated that a broad range of sulfide composition with $x > 0.15$ should be investigated for optimizing the χ-match to improve the V_{oc}.

The Zn content in the sulfide layer was subsequently increased to about 25%. In general, the high Zn content sulfide cells exhibited higher open circuit voltage and poor fill factor. In some cases, however, the cell open circuit voltage did not improve in comparison to the pure CdS cell.

By analyzing the mixed sulfide layer, we found that the Zn content increased with film thickness and only the top surface was about 25%. The unimproved cell open circuit voltage was possibly due to the low Zn content of the initial mixed sulfide layer near the junction. The low fill factor could have been caused by excessive series resistance from the high sheet resistivity, high Zn content layer at the upper surface.

The best cell made from the graphite apertured sulfide vapor source had the photovoltaic response as shown in Figure 3.5.3-3 with

V_{oc} = 423mV J_{sc} = 33.65mA/cm^2
F.F. = 0.60 η = 8.55%

under simulated AM1 illumination.

The Zn content of the mixed sulfide near the junction of this cell could not be determined because of the variation of Zn with sulfide thickness. The V_{oc} of this cell was about 10mV higher than typical pure CdS cell. The diode quality factor (1.21) measured from the I_{sc}-V_{oc} characteristics was comparable to the regular CdS cell whereas the reverse saturation current (3.8×10^{-8} Amp/cm^2) was about one order lower than the regular cell. The lower fill factor and higher equivalent series resistance (2.07 ohms) were caused by the higher mixed sulfide resistivity.

Cell efficiency improved to 10.60% later in the program by adopting the two source process for depositing the mixed sulfide layer with Zn content about 20% (as discussed

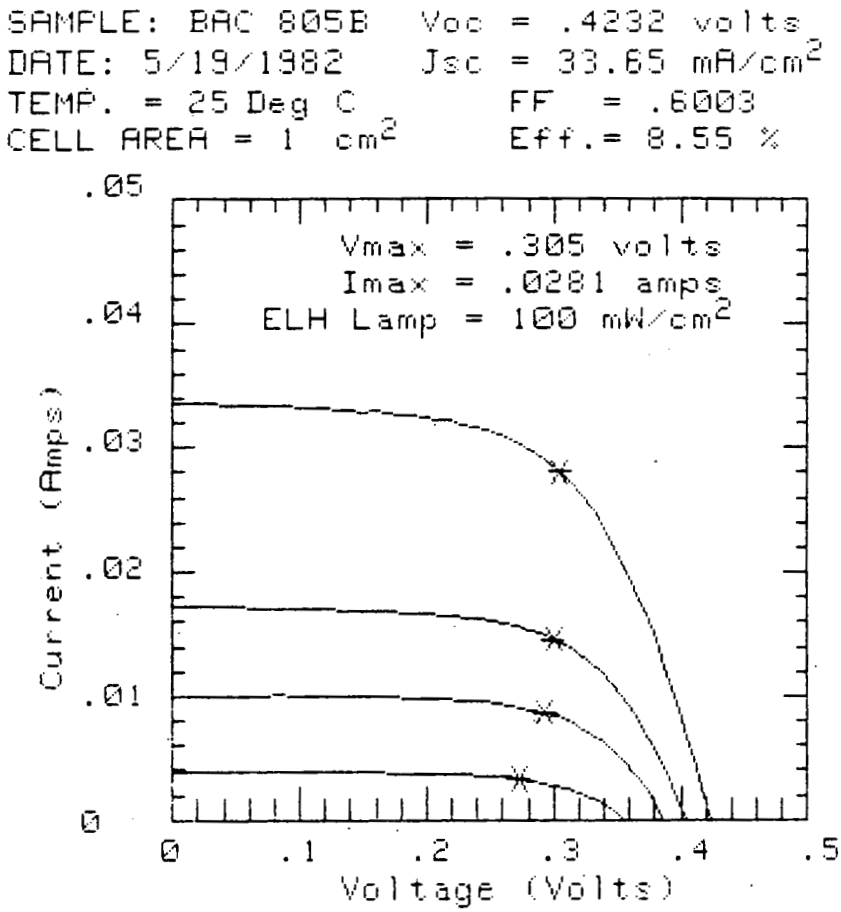


Figure 3.5.3-3 Typical Photovoltaic Characteristic of a Non-AR Coated Mixed Sulfide Cell

in section 3.2). The cell after heat treatment in oxygen for 55 minutes at 225°C had an efficiency of 9.39% with V_{oc} = 0.4283V, J_{sc} = 33.72mA/cm^2 and F.F. = 0.6501.

After anti-reflection coating, the cell efficiency reached 10.60% with V_{oc} = 0.4314, J_{sc} = 38.96mA/cm^2 and F.F. = 0.6309. The cell photovoltaic responses before and after anti-reflection coating are shown in Figures 3.5.3-4 and 3.5.3-5. The open circuit voltage was appreciably improved to greater than 0.43 volts as compared to those with pure CdS layer.

3.5.4 Cell Spectral Response

The cell spectral response measurement system has been described in Sec. 3.5.1. Typical spectra dependences of non-AR coated cell responsivity and quantum efficiency are shown in Figures 3.5.4-1 and 3.5.4-2. The low wavelength cut-off at ~500 nm corresponds to the CdS absorption edge (2.42 eV) and the long wavelength drop-off at ~1200 nm corresponds to the band-gap (1.04 eV) of the $CuInSe_2$. The quantum efficiency was quite uniform at a value of ~0.81 in the wavelength range from 600 nm to 900 nm. The decreases of responsivity and quantum efficiency near 960 nm were observed on measurements of 12 high efficiency cells. This was also noticed in an earlier cell measured at NASA-Lewis (Figure 3.5.2-3). The structure near 960 nm may be the result of a transition from the spin-orbit valence band to the lowest conduction band in $CuInSe_2$. The reported energy gap from the spin-orbit split valence band to the conduction band ($E_g + \Delta_{so}$) is 1.27 eV (976 nm) which agrees very well to our observed value. This effect has also been seen in InP/CdS solar cells[16].

Integration of the measured cell responsivity over a reported AM1 solar spectrum[17] finds the short circuit current to be 31.26mA (as shown in the bottom of Figure 3.5.4-2) which is very close to the measured I_{sc} (32.52mA) under the ELH lamp simulator.

As discussed in Section 3.2, the use of $Zn_xCd_{1-x}S$ as window layer in making heterojunctions with $CuInSe_2$ should increase the open circuit voltage through minimizing the differences of electron affinities and lattice constants. In addition, due to the larger band-gap of mixed sulfide the photogenerated current should also increase. The widening of the spectra response window by using the mixed sulfide can be clearly observed in the quantum efficiency measurement. As shown in Figure 3.5.4-3 the low wavelength cutoff has shifted to shorter wavelengths (~0.48μm, ~2.58 eV) which corresponds to the band-gap of the mixed sulfide.

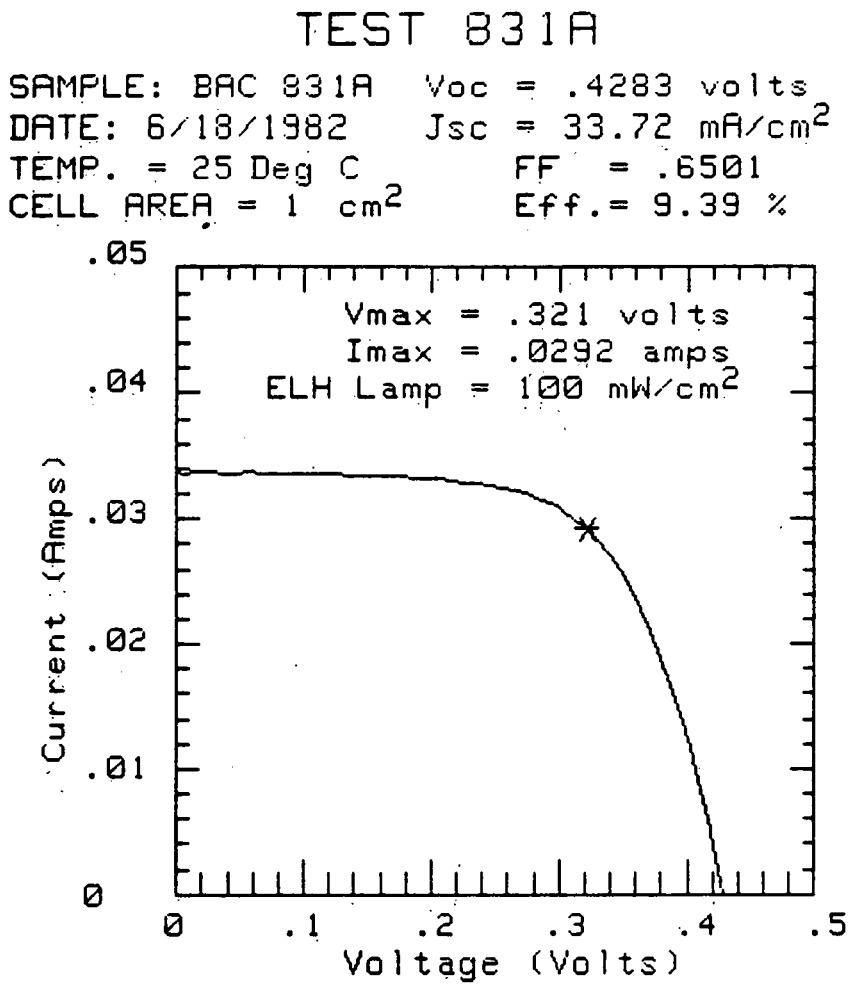


Figure 3.5.3-4 Photovoltaic Response of a High Efficiency Cell With Zn Content About 20% in the Mixed Sulfide Layer (Before AR Coating)

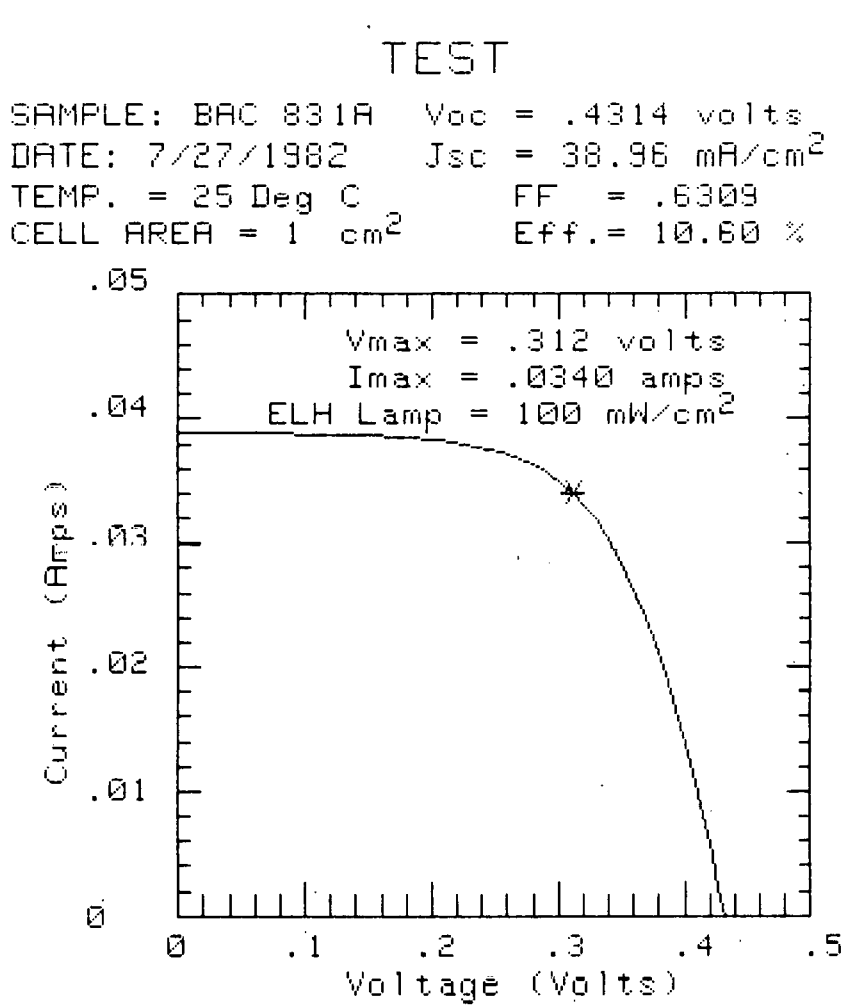


Figure 3.5.3-5 Photovoltaic Reponse of the Same Cell Shown in Figure 3.5.3-4 After AR Coating

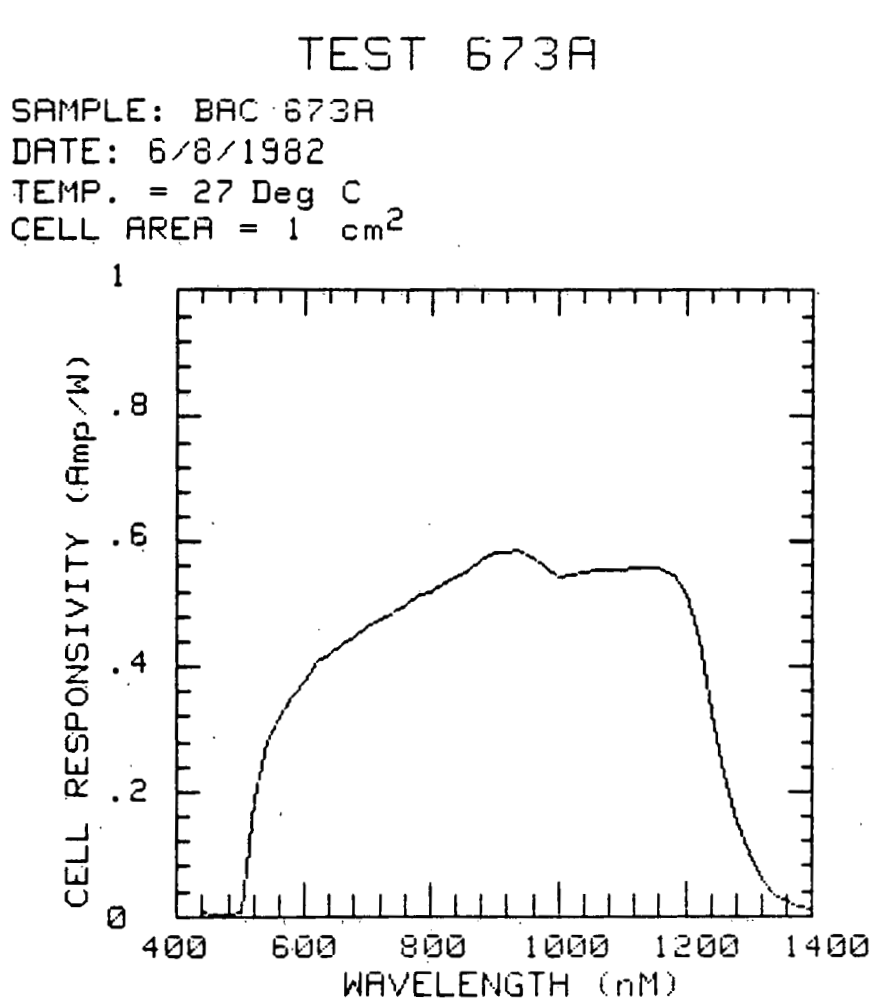
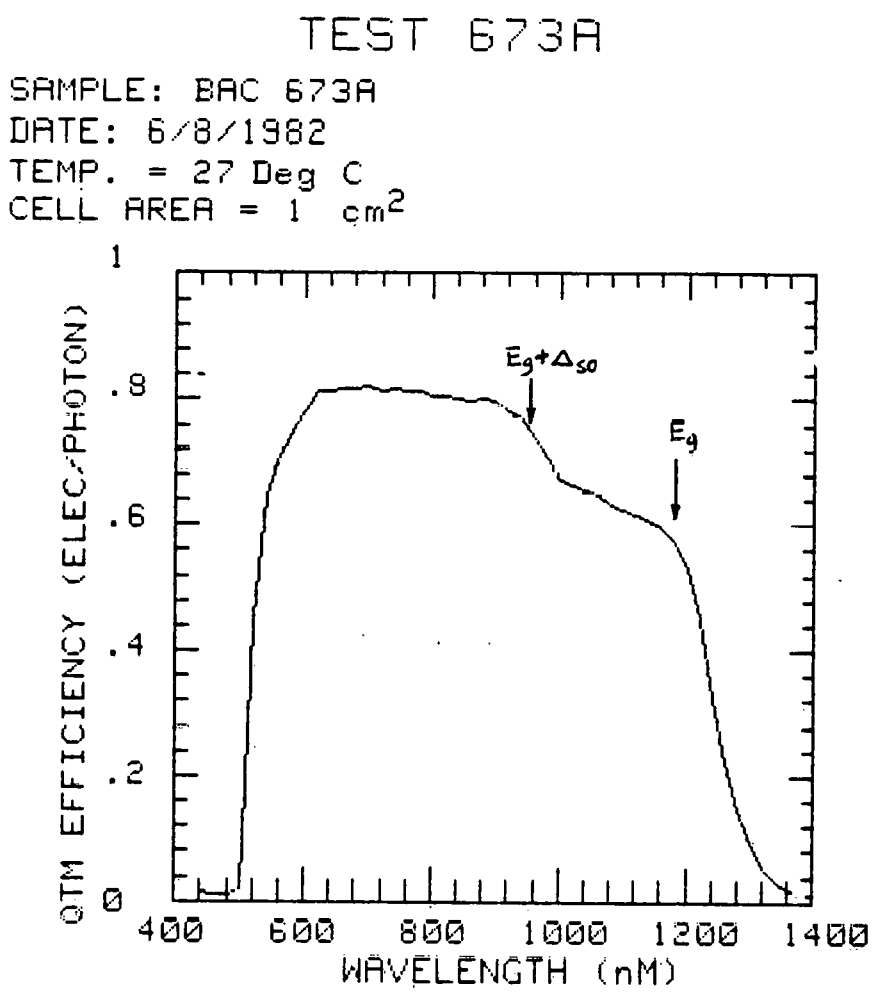


Figure 3.5.4-1 Spectral Dependence of Cell Responsivity

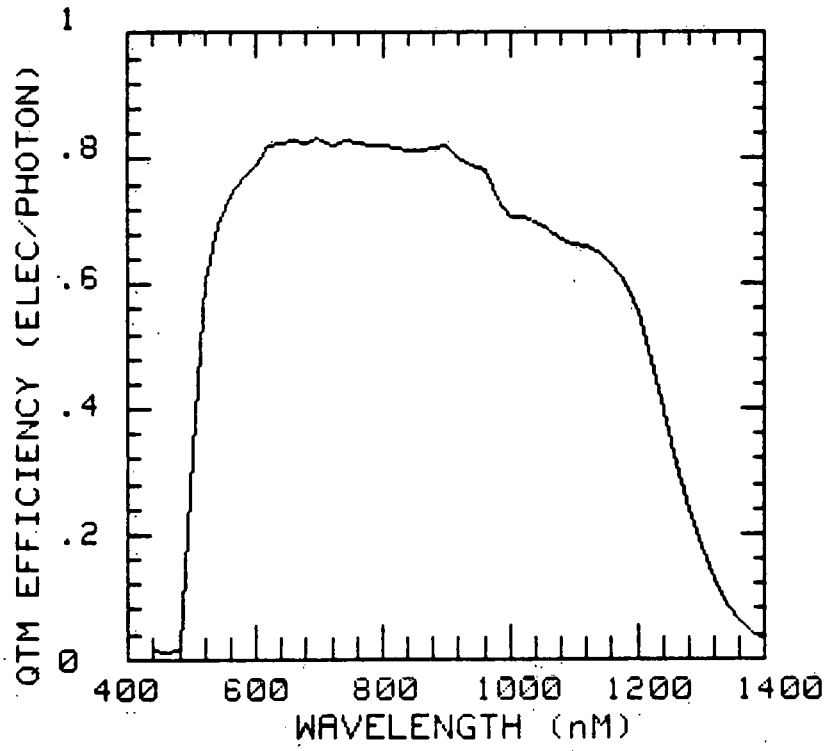


LAMBDA (nM)	Isc (mA)	Isc Increment (mA)
540.00	1.089	1.089
640.00	6.383	5.294
740.00	12.209	5.905
840.00	20.218	7.930
940.00	23.002	2.784
1040.00	26.107	3.105
1140.00	28.817	2.710
1240.00	30.724	1.907
1340.00	31.245	.522
1400.00	31.257	.012

Figure 3.5.4-2 Spectral Dependence of Cell Quantum Efficiency. The Lower Table is the Calculated I_{SC} by Integrating the Cell Responsivity Over a Solar Spectrum

TEST 682A

SAMPLE: BAC 682
DATE: 6/8/1982
TEMP. = 27 Deg C
CELL AREA = 1 cm^2



LAMBDA (nM)	Isc (mA)	Isc Increment (mA)
540.00	1.755	1.755
640.00	7.180	5.426
740.00	13.157	5.976
840.00	21.208	8.051
940.00	24.051	2.843
1040.00	27.321	3.270
1140.00	30.209	2.888
1240.00	32.238	2.029
1340.00	33.044	.806
1400.00	33.078	.034

Figure 3.5.4-3 Spectral Dependence of Quantum Efficiency of a $Zn_xCd_{1-x}S/CuInSe_2$ Cell

3.5.5 $CuInSe_2$/Mo Contact

Thin-film cell samples were submitted to SERI for detailed analysis. These cells had the cross-section exposed by fracturing the alumina substrate. On performing EBIC analysis, it was determined that the selenide/Mo interface exhibited a Schottky barrier type contact with a substantial electron beam induced response (Figure 3.5.5-1)[18].

The existence of this barrier may be consistent with an anomalous I-V characteristic displayed by several of our cell samples. That is, in the first quadrant of the I-V characteristic, there sometimes was a strong inflexion of the curve. An example of this behavior is shown in Figure 3.5.5-2. In an extreme case or at cryogenic temperatures, the current became nearly horizontal with the voltage axis.

Similar results have been reported for silicon cells and have been attributed to an non-ohmic back contact (19). In the case of the silicon cells, one effect of this contact is the reduction in V_{OC}. It should be noted, however, that the current inflexion in our cells either disappeared completely or moved to very high current values after cell heat treatment as shown in Figure 3.5.5-3. The influence of heat treatment is difficult to associate with the selenide/Mo contact since the substrate temperature was 350°C/450°C for the selenide deposition while heat treatment was performed at only 200°C.

The above results seemed to have sufficient importance to warrant experiments directed towards improving the back cell contact. These were done using a variety of metallization systems as substitutes for Mo. For these tests, half of the Mo metallized substrates were coated with the trial metallizations so that direct comparisons with the standard cell performance could be made. A listing of the trial metal systems is contained in Table 3.5.5-1.

The results of these experimental depositions showed, in all instances, that the selenide film properties had been affected by the substitite metallizations and the cell performance was degraded. The effects were so significant on some of the deposits that the selenide layer was converted from P-type to N-type material. Only in the case of Mo did the selenide properties on the bare alumina appear the same as those over a metallization. Consequently, none of these metallizations seem superior than Mo and all would require alteration of the selenide deposition parameters for

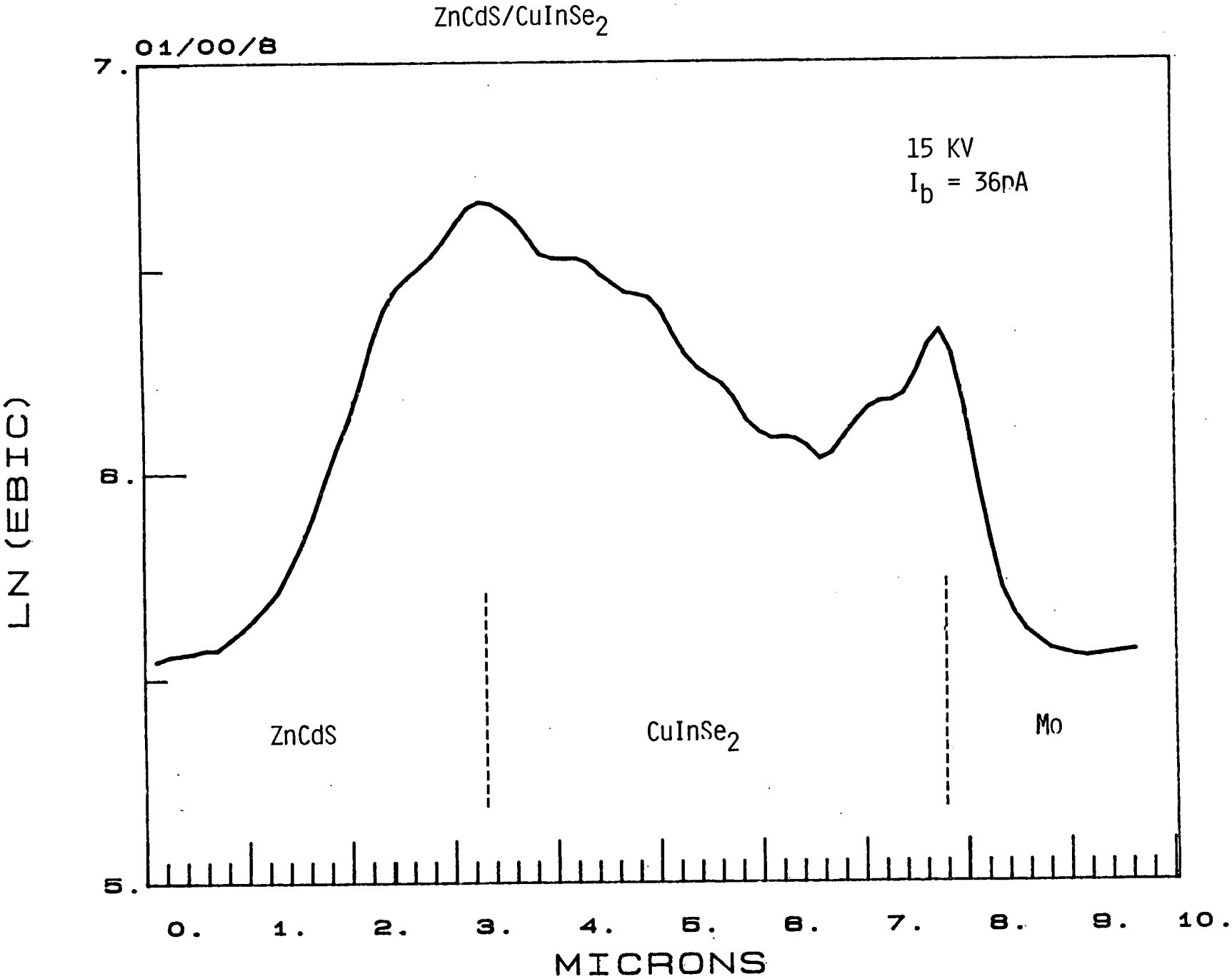


Figure 3.5.5-1 EBIC Response of a $CuInSe_2$/ZnCdS Thin-Film Cell

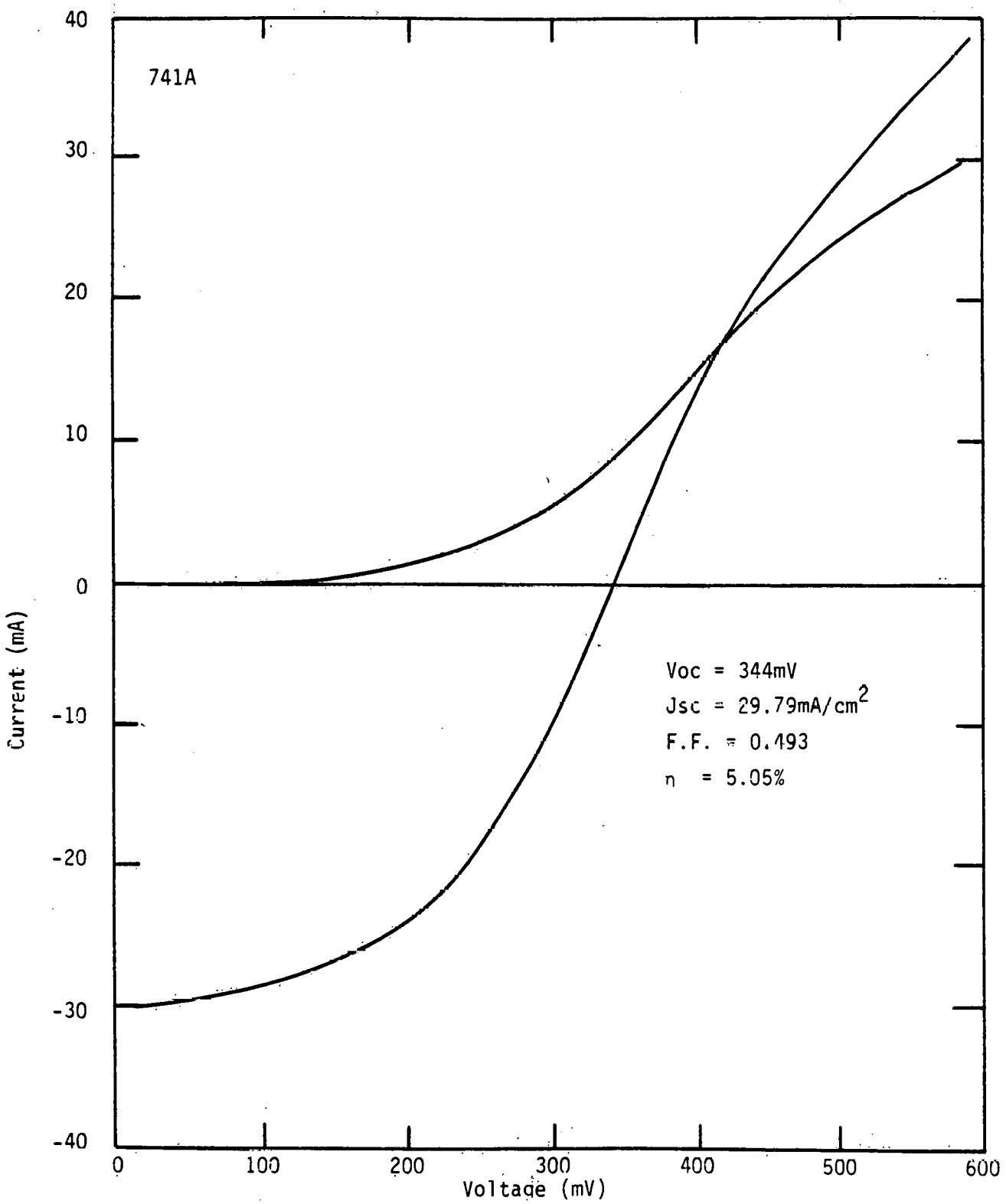


Figure 3.5.5.2 Dark and Light I-V Characteristics of a Cell Before Heat Treatment

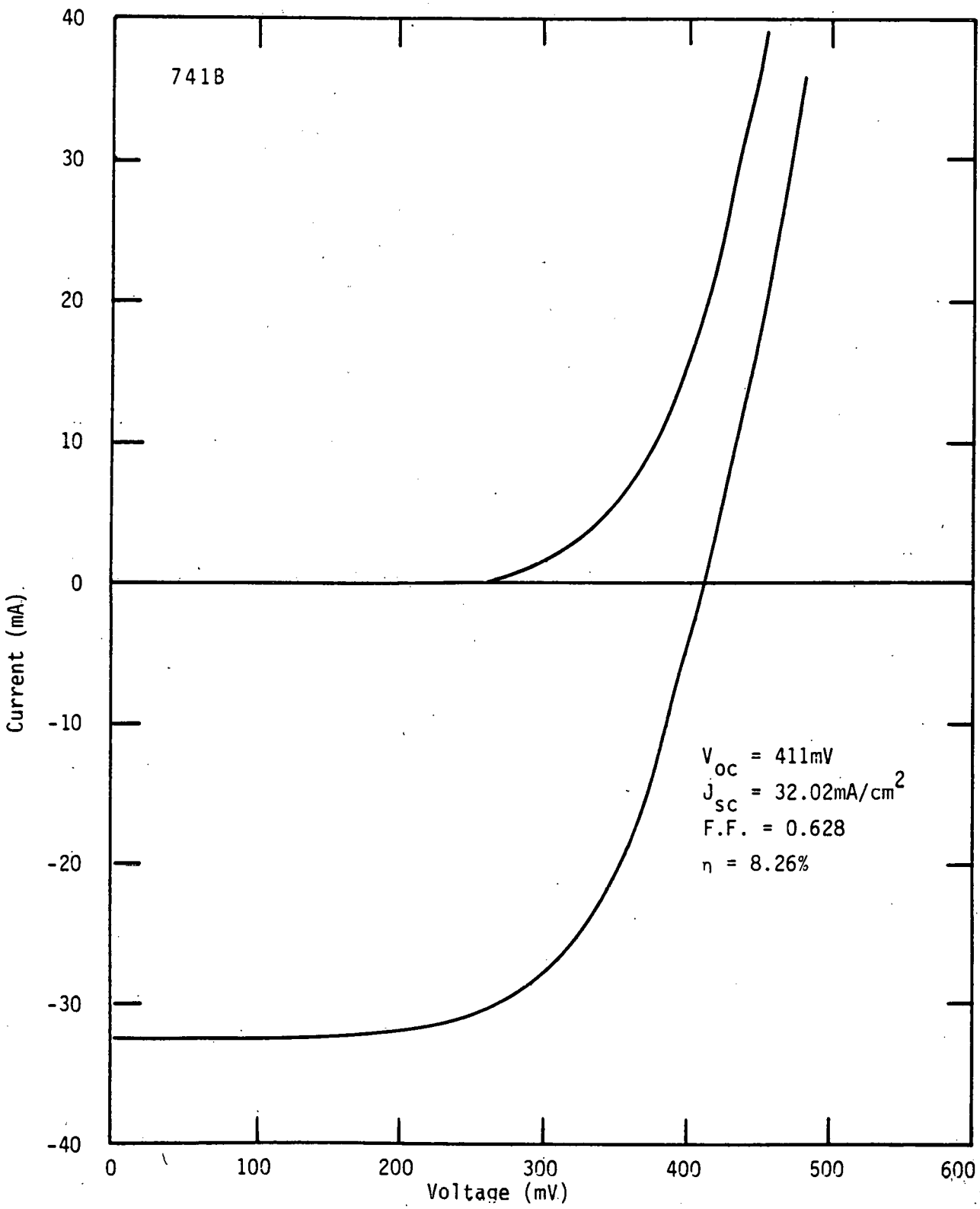


Figure 3.5.5-3 Dark and Light I-V Characteristics of a Similar Cell after Heat Treatment

Table 3.5.5-1 Alternate Cell Base Metallization Systems Studied

Metallization	Results
Mo/Au (300-1500Å)	Selenide properties altered and degraded cell performance
Mo/Ti (200Å)/Pd (500Å)	"
Mo/Ti (200Å)/Pt (500Å)	"
Mo/Ti (500Å)	"
Mo/Ai (1000Å)	"

reasonable device performance. Since these adjustments would likely be very time consuming and the significance of Mo contact to cell operation was still in doubt, we did not continue research in this direction. Further research to theoretically determine the effect of Mo-contact to the cell performance should first be conducted.

3.6 Constant Illumination Life Testing

In advance of a detailed life test program on the $CuInSe_2$/CdS thin-film solar cells, we believed that a constant illumination and temperature test under different cell loading conditions would provide valuable, quantitative information concerning the cell stability. Hence, a very simple testing station was constructed. It consisted of a heavy metal plate which could be maintained at a constant temperature (21^{o}) by water flowing in attached metal tubing. Up to ten cells could be placed on this plate and held down by pressure contacts which also allowed the I-V characterization and loading of each individual cell. Two ELH lamps were positioned over the cells and adjusted to yield a reasonably uniform intensity of $100mW/cm^2$ according to a silicon standard cell. Since the cells had been previously found to be quite stable in normal laboratory atmosphere, no attempt was made to control the test environment, i.e., it was simply conducted on a completely open bench top located within the lab. Figure 3.6-1 depicts, in a schematic form, the constructed constant illumination test station.

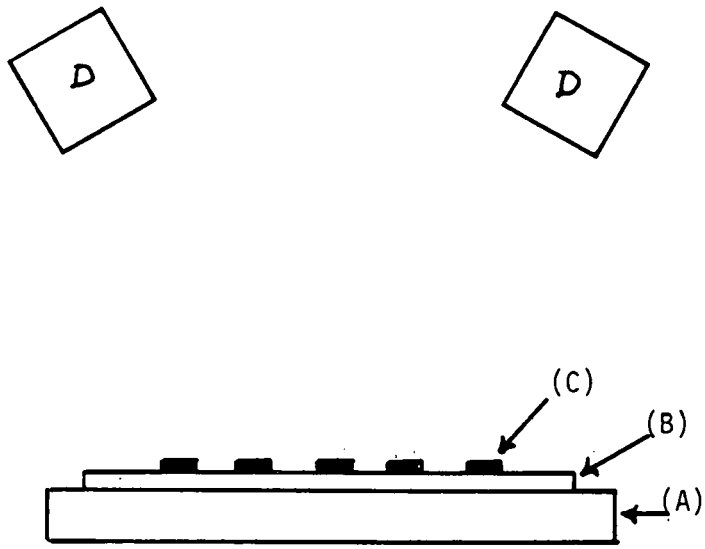
For the first test, ten existing cells were selected which had efficiencies of approximately 7.5% without AR coating. These cells were mounted on the test plate and the light I-V characteristics recorded for simulated AMI illumination. This characterization was done by placing the plate within our standard I-V test fixture. After the initial I-V curve had been determined for each cell, the cells were connected for the loading conditions. Three cells were short circuited, three had a $10\,\Omega$ load, and four were left in the open circuit condition. The test plate was then returned to the life test station and the test started.

When the cells had been exposed to the constant illumination for a set number of hours, the test plate was again transferred to the standard test fixture and the light I-V curves re-measured. The time between removing the cells from the constant illumination station and measuring the I-V parameters was not tightly controlled but usually all testing was completed within one hour.

THIS PAGE

WAS INTENTIONALLY

LEFT BLANK



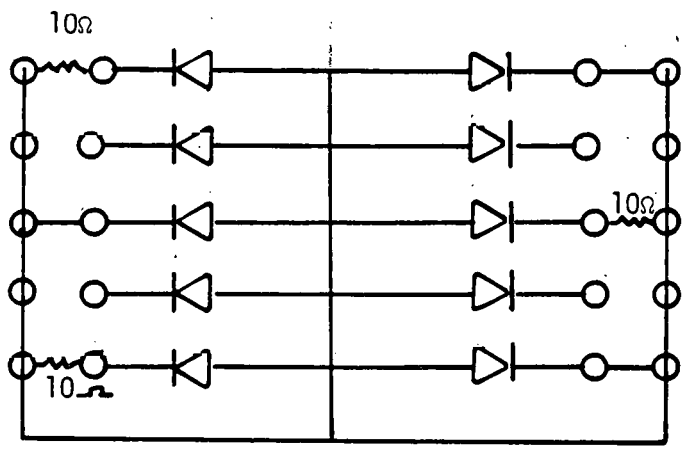
(a) Constant illumination test station

(A) Water-cooled plate

(B) Sample mount plate

(C) Samples

(D) ELH Lamps - individually adjustable



(b) Configuration of sample mounting.

Fig. 3.6 -1 Schematic diagram of constant illumination test station.

Upon monitoring the test results in terms of V_{oc}, I_{sc}, and FF, it soon became apparent that an instability problem existed. While the V_{oc} and I_{sc} appeared stable, the fill factor, especially on the open circuit loaded cells, was obviously degrading even after only some 24 hours of testing. The testing was continued, however, until nearly 240 hours had been accumulated. At this time, all three cell parameters had seriously degraded for the open circuit loaded cells and degration was also noticeable in the other devices.

A microscopic examination of the tested cell samples revealed a blistering of the aluminum film grid contact. This blistering was especially prominent on the open circuit loaded cells.

Following the development of the sputter etch process to improve the grid/CdS contact, three cells were prepared using the process and a second life test program was begun on them. Since open circuit was found to be the most severe condition, the devices were tested in this mode.

The second life test was run for 500 hours and the results are presented in Figure 3.6-2. As shown by the depicted data, the short circuit current and open circuit voltage were remarkably stable. Although the stability of fill factor was substantially improved in comparison to the first test, there still appeared to be some degradation.

Testing of the three cells under open circuit conditions was continued but at an elevated temperature. For these additional measurements, the test plate on which the cells were mounted was maintained at 60°C. When the cells had been exposed to constant illumination (simulated AMI) for a set number of hours, the test plate was cooled down to ~21°C and transferred to the standard test station for an I-V curve measurement.

The life test at 60°C was run for 990 hours and the results are presented in Figure 3.6-3. At the beginning of the test, the three cells had approximately the same V_{oc}, I_{sc}, and F.F. values as at the end of the 500 hour, 21°C test. During the first 200 hours at 60°C, the fill factors continued the decreasing trend of the previous test. It was then found that this degradation of fill factor was caused by the mechanical pressure probes making a high resistance contact to the aluminum grid. After re-adjusting these probes, the fill factors were restored to their original high values.

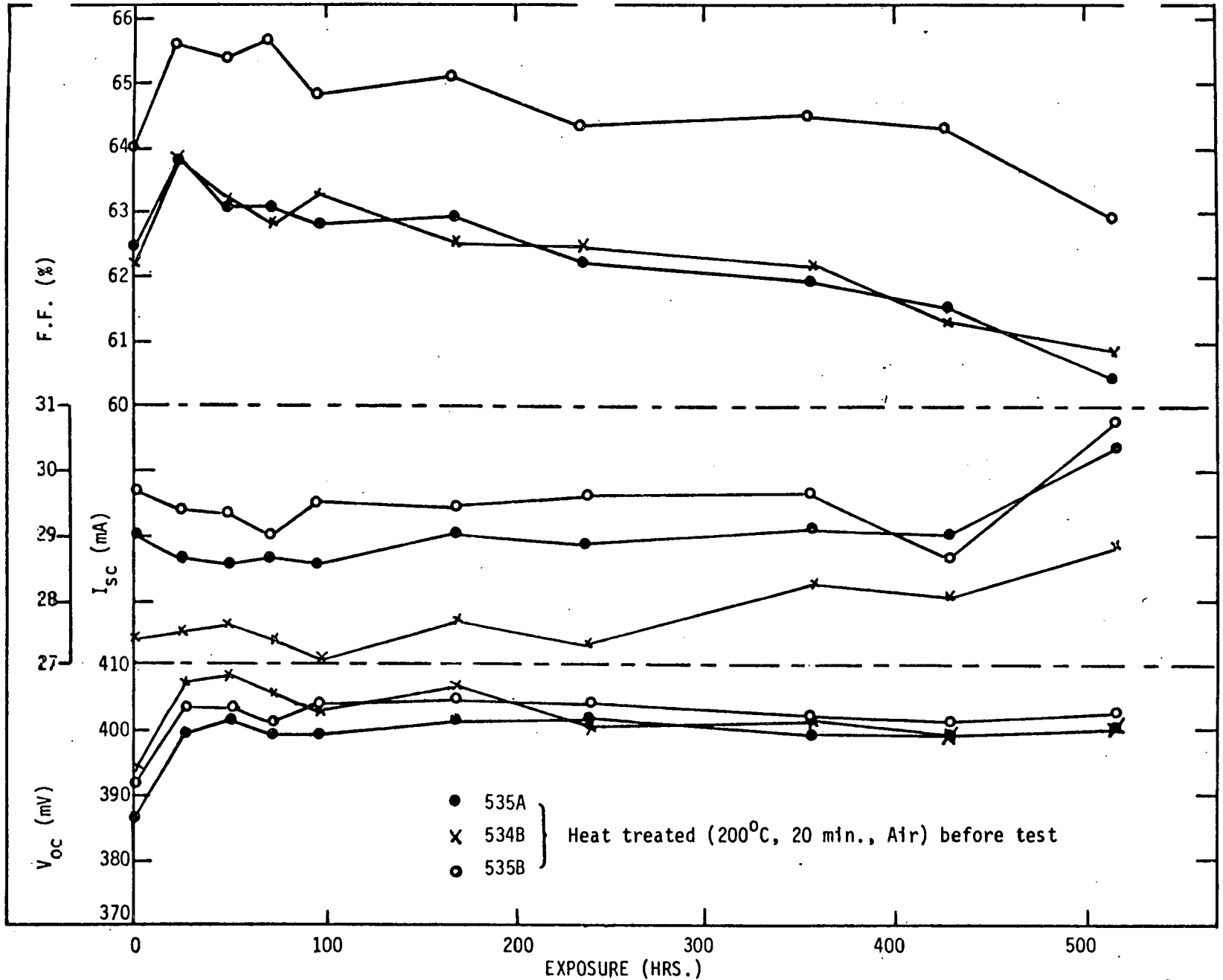


Fig. 3.6-2 Change in V_{oc}, I_{sc} and F.F. during continuous illumination
Load: Open circuit Temperature: 21°C Illumination: ~ AM1 ELH

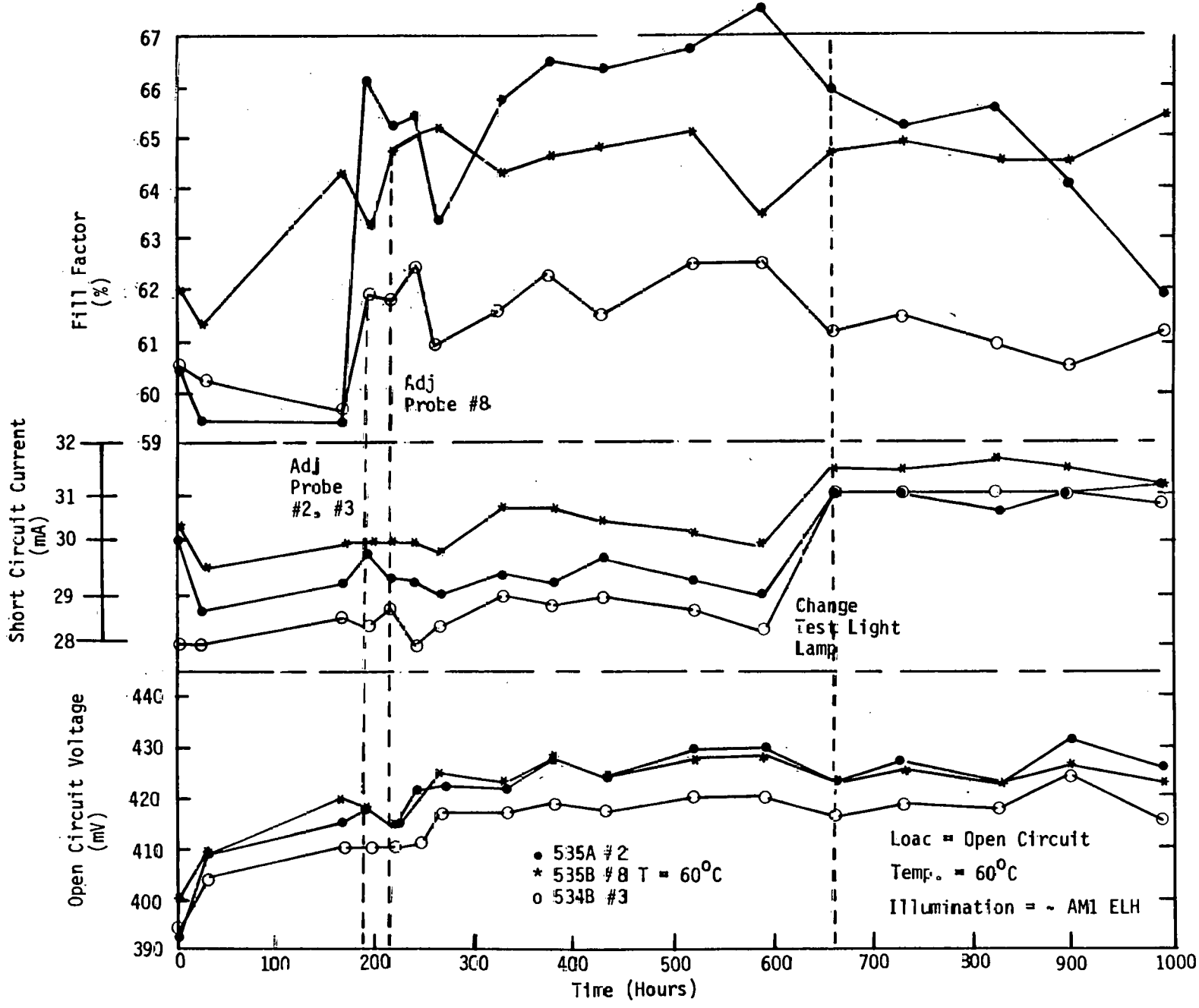


Figure 3.6-3 Change in V_{oc}, I_{sc} and F.F. of 1-cm^2 $CuInSe_2$/CdS Thin-Film Cells During Continuous Illumination Life Test Illumination: Simulated AM1; Temperature: 60°C

Thereafter, the probes were adjusted before each measurement. However, the observed fluctuations in F.F. may largely be attributed to the probe contact condition. The open circuit voltages showed a gradual increasing trend during the first several hundred hours but stabilized after approximately 600 hours of testing. The gradual increase in V_{oc}'s may indicate the initial heat treatments had not been optimized. Thus, testing at 60°C may actually be considered as a continuation of the heat treatment.

Figure 3.6-3 further shows that the short circuit currents remained relatively constant during the 60°C test. The downward trend after 400 hours of testing was due to aging of the ELH measurement lamp. After changing the lamp and recalibrating with a Si standard cell, the apparent decrease in short circuit current disappeared.

Testing of the same three thin-film $CuInSe_2/CdS$ cells under maximum power loading condition at 60°C was next conducted. Two cells were installed with a 12 ohm load to approximate maximum power loading and the third cell was left in the open circuit condition. Nearly 4200 hours were accumulated during the test and the results are shown in Figure 3.6-4. While there is the expected scatter in the experimental data, it can be seen that all three cell parameters (V_{oc}, I_{sc}, and F.F.) for the three cells were extremely stable.

Since degradation in cell performance could not be detected after many thousands of hours at 60°C, it was decided to increase the test temperature to 80°C. A fourth cell was also added to the test program. Initially, two cells were left open circuit and two had the 12 ohm load. However, the contacting probes for cell loading were observed to be damaging the cells and, after about 1500 hours, only open circuit testing was conducted. The 80°C test results are shown in Figure 3.6-5. Definitive conclusions regarding the cell stability at 80°C are somewhat difficult to make at this time. In general, the stability continues to look quite good but there appears to be a downward trend in the cell performance, particularly after 2000 hours. Microscopic examination of the cells has revealed considerable mechanical damage caused by the repeated probing for loading and cell measurements. For example, there were several areas where the selenide/sulfide layers had been fractured creating voids in the film layers to the Mo metallization. These voids were most severe on the two cells which had experienced the 12 ohm loading conditions. As can be seen, these same two cells exhibited the greatest decrease in fill factor. Whether shunting effects associated

Figure 3.6-4 Thin-Film Cell Parameters as a Function of Time During Constant Illumination Life Test. Illumination: Simulated AM1; Temperature: 60°C

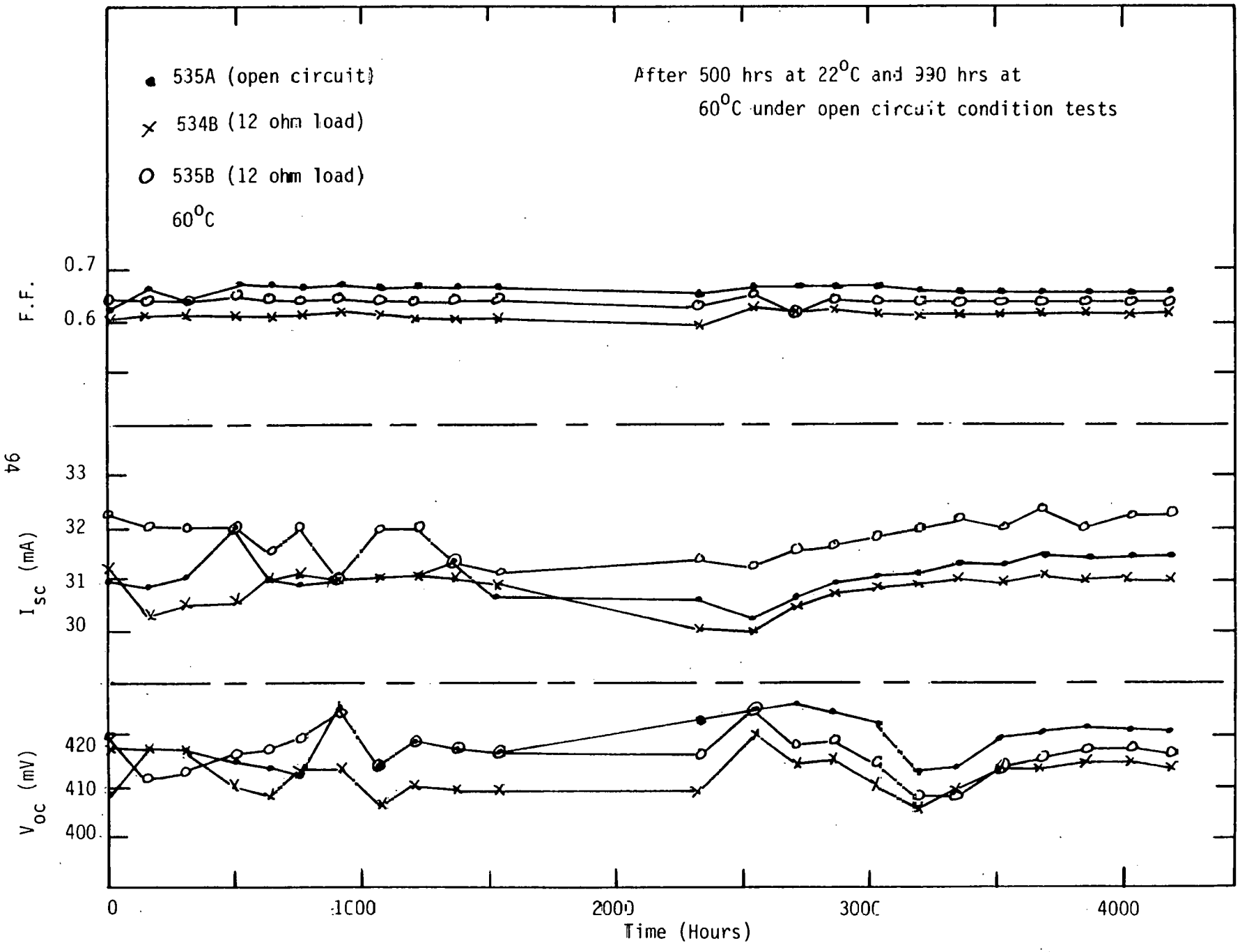
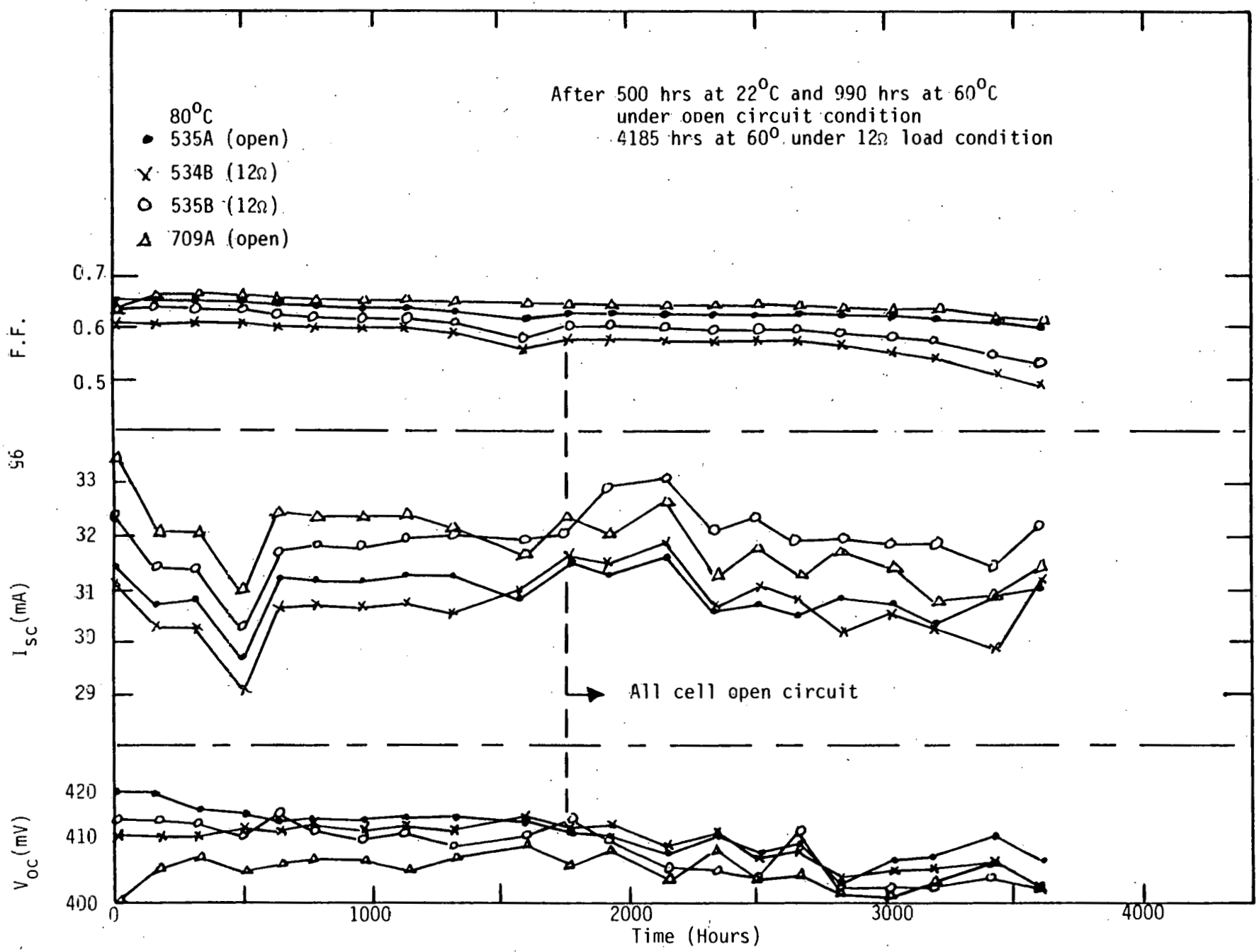


Figure 3.6-5 Thin-Film Cell Parameters as a ... ion of Time During Constant Illumination Life Test. Illumination: Simulated AM1; Temperature: 80°C



with the voids and exposed junctions is responsible for the observed performance is not known. Based upon the experience acquired during these tests, in future life tests we would, however, attempt to improve the contacting method in order to minimize or avoid the mechanical damage. Even with this damage, the stability of the cells under extremely severe test conditions is still regarded as being excellent and showing great promise for the $CuInSe_2/CdS$ device.

Discussions with Battelle were then made for the purpose of initiating life testing of our cells in their laboratories. The plan was to provide Battelle with approximately 12 existing, $1cm^2$ high efficiency cells (greater than 8% without AR coating).

The twelve cells were selected which had been fabricated by the standard process methods and device structure. One cell (no. 699B) had, however, been prepared with a mixed ZnCdS layer instead of the pure CdS. The basic photovoltaic properties of these cells as measured under simulated AMI illumination (ELH lamp) are listed in Table 3.6-1. In addition to these properties, the shunt resistance, series resistance, diode factor(A), reverse saturation current (J_o), quantum efficiency, and spectral response were measured for each cell.

Because our previous life-testing experience had shown the difficulty of making good electrical contact to both the Mo base and Al grid metallizations over a long period of time, it was believed that a more reliable contact area metallization would be highly desirable. Gold film metallizations seemed to be the best choice and processes for depositing gold pad contact areas were investigated.

A successful process was developed using straight thru-metal mask deposition. A Be-Cu, 5-mil thick mask was fabricated, an alignment technique developed, and the deposition process established. In this process, the cells were first vapor degreased in trichloroethylene for 10 minutes, placed in a substrate carrier and the stencil mask aligned to the proper position. This assembly was then installed in a high vacuum chamber for the electron gun evaporation of the pad layer consisting of 1000 Å of Al, 500Å of Mo, and 500 Å of Au. The Mo film was included to act as a diffusion barrier between the Al and Au films to prevent the formation of undesirable intermetallic compounds.

Table 3.6-1 Photovoltaic Properties of $CuInSe_2$ Thin-Film Cells To Be Used In Battelle Life-Test Studies

	Sample No.	V_{oc} (mV)	I_{sc} (mA)	F.F.	Eff. (%)
1	673A	417	32.52	0.630	8.55
2	682A	402	34.12	0.594	8.15
3	699B	415	33.07	0.606	8.32
4	750A	417	32.07	0.623	8.33
5	750B	420	32.34	0.627	8.51
6	750CB	416	32.70	0.633	8.60
7	751A	414	32.30	0.609	8.14
8	751B	416	31.36	0.629	8.19
9	751CA	409	32.38	0.650	8.58
10	751CB	408	32.80	0.643	8.61
11	772A	416	33.32	0.613	8.49
12	772B	418	32.46	0.605	8.21

After verifying that the above procedure was not detrimental to cell performance, all of the Battelle samples were then processed, characterized, and shipped to Battelle for their studies.

4.0 CONCLUSIONS AND RECOMMENDATIONS

Through a series of cell design and technology improvements, the conversion efficiency of the polycrystalline $CuInSe_2$ thin-film solar cell has been increased from 7.5% to 10.6% under simulated AM1 illumination. An increase in cell voltage resulting from the use of a mixed $Zn_xCd_{1-x}S$ layer instead of CdS has been a major factor in the cell improvement. The general cell fabrication technology and experience has been sufficiently advanced to make possible the repeatable preparation of cells with efficiencies of ~ 7.5% before AR-coating. A key feature of the high efficiency cells has been the development of a two-layer selenide film deposition process. The top or second selenide film has appeared to have undergone a semiconductor type conversion as the result of diffusion mechanisms. Preparation of the selenide film layers with a planetary apparatus has been shown feasible by the achievement of a 7.5% (without AR-coating) cell. Finally, the thin-film $CuInSe_2$ cells have been found to be remarkably stable when tested under accelerated aging conditions. After an accumulated 9300 hours of constant illumination, elevated temperature testing in an open environment of unpassivated or encapsulated cells, little cell degradation has been observed.

To continue the development of this highly promising thin-film cell, the following additional research studies are recommended:

1) Detailed cell analysis to clarify important cell mechanisms, determine performance limiting factors, and define approaches for cell improvement;
2) Basic properties of the deposited selenide film material and cell structures;
3) Detailed investigation of the back cell contact to determine its impact on cell performance and, if appropriate, development of a substitute for the Mo metallization;
4) Improved Cu/In vapor source structures for increased selenide film uniformity and reproducibility;
5) Selenide grain size effects on the cell characteristics;
6) Alternate N-type layer materials and ternary modifications, e.g., partial substitution of Ga and S;
7) Methods to reduce the high degree of compensation in the deposited selenide films;

8) In depth analysis and optimization of the cell grid structure, base metallization, and anti-reflection coating;
9) Continued optimization of the semiconductor film deposition processes with respect to cell performance;
10) Alternative selenide film deposition methods, e.g., sputtering, spraying, CVST, hot-wall evaporation, etc.; and
11) Single crystal cell fabrication and analysis.

5.0 REFERENCES

1. R. A. Mickelsen and W. S. Chen, "Improved Semiconductors for Solar Cells - CuInSe," Final Report, Contract E(49-18)-2459, August 1977.

2. R. A. Mickelsen, W. S. Chen, and B. Selikson, "Cadmium Sulfide/Copper Ternary Heterojunction Cell Research," Final Report, Contract EG-77-C-03-1458, October 1978.

3. S. Wagner, et al., Appl. Phys. Lett. 25, 434 (1974).

4. J. L. Shay, et al., Proc. Eleventh Photovoltaic Specialists Conf., Phoenix, Arizona, p. 503 (1975).

5. S. Wagner, et al., Appl. Phys. Lett. 26, 229 (1975).

6. L. L. Kazmerski, "Ternary Compound Thin Film Solar Cells," Final Report NSF/RANN/SE/AER 75-19676/PR/75/4, October 1976.

7. L. L. Kazmerski, et al., Appl. Phys. Lett. 29, 269 (1976).

8. L. L. Kazmerski, et al., J. Vac. Sci. Technol. 14, 65 (1977).

9. R. A. Mickelsen and W. S. Chen, "Cadmium Sulfide/Copper Ternary Heterojunction Cell Research," Final report, Contract XJ-9-8021-1, March 1980.

10. IEC, Univ. of Delaware, Abstracts, 4th Annual Photovoltaic Advanced Research and Development Conference, Colorado Spring, Nov. 18-20, 1980; p. 121, SERI/CP-611-956.

11. M. S. Tomar and F. J. Gacia, Preprint for the 1978 International Electron Devices Meeting, Washington, D.C., Dec. 4-6, 1978.

12. IEC, Univ. of Delaware, Final Report EG-77-C-03-1576-FR, May 1979.

13. R. Lesueur, et al., p. 15, Inst. Phys. Conf. Ser. No. 35 (1977).

14. L. L. Kazmerski, "Ternary Compound Thin Film Solar Cells," Final Report NSF/RANN/SE/AER 75-19576/PR/75/4, October 1976.

15. K. W. Mitchell, Evaluation of the CdS/CdTe Heterojunction Solar Cell, (Outstanding Dissertation on Energy), Garland Publishing Inc., 1979.

16. J. Shay, et al., IEEE Trans. Electron Devices, Vol. ED-24, p. 483 (1977).

17. K. W. Boer, Terrestrial Photovoltaic Measurement-II, ERDA/NASA-1022/76/10, p. 17 (1976).

18. P. E. Russell, et al., Appl. Phys. Lett. 40, 995 (1982).

19. H. Fischer, et al., p. 375, "Solar Cells," Proc. Int. Colloq., Toulouse, 6-10 July, (1970), Gordon and Breach, London (1971).

6.0 APPENDICES

6.1 Appendix A-Report

DISTRIBUTION LIST

Dr. Manjul Bushan
Institute of Energy Conversion
University of Delaware
One Pike Creek Center
Newark, DE 19711

Karl Boer
College of Engineering
University of Delaware
Newark, DE 19711

Dr. T. L. Chu
Southern Methodist University
Department of Electrical Engineering
Dallas, TX 75275

Dr. Richard H. Bube
Department of Materials
Science and Engineering
Stanford University
Stanford, CA 94305

Dr. Klaus Bachmann
Department of Chemistry
North Carolina State University
808 Dabney
Raleigh, NC 27650

Gordon B. Gaines
Battelle Columbus Laboratories
505 King Avenue
Columbus, OH 43201

Rodger W. Hardy
PV Program Officer, 17/1
Solar Energy Research Institute
1617 Cole Boulevard
Golden, CO 80401

Allen M. Hermann
PV Program Office, 17/1
Solar Energy Research Institute
1617 Cole Boulevard
Golden, CO 80401

Robert H. Lamoreaux
SRI International
333 Ravenswood Avenue
Menlo Park, CA 94025

Joseph J. Loferski
Division of Electrical Engineering
Brown University
Providence, RI 02912

John D. Meakin
Institute of Energy Conversion
University of Delaware
One Pike Creek Center
Newark, DE 19808

Kim Mitchell
PV Research, 16/3
Solar Energy Research Institute
1617 Cole Boulevard
Golden, CO 80401

Dr. Larry C. Olsen
Joint Center for Graduate Study
University of Washington
100 Sprout Road
Richland, WA 99352

Dr. John Mooney
SRI International
333 Ravenwood Avenue
Menlo Park, CA 94025

Gerald Noel
Battelle Columbus Laboratories
505 King Avenue
Columbus, OH 43201

Alan Postlethwaite
U.S. Department of Energy
Division of Photovoltaic Energy
Technology
Forrestal Building, (CE 313)
1000 Independence Avenue
Washington, D.C. 20545

Jim Sites
Colorado State University
CSU (Physics)
Ft. Collins, CO 80523

Allen Rothwarf
Electrical and Computer
Engineering Department
Drexel University
Philadelphia, PA 19104

John R. Szedon
Westinghouse Research
& Development Center
1310 Beulah Road
Pittsburgh, PA 15235

John A. Thornton
Telic Corporation
1631 Colorado Avenue
Santa Monica, CA 90404

Dr. S. Wagner
Department of E.E. & Comp. Science
Princeton University
Princeton, NJ 08544

Alex Zunger
PV Research, 16/3
Solar Energy Research Institute
1617 Cole Boulevard
Golden, CO 80401

Kenneth Zweibel
PV Program Office, 17/1
Solar Energy Research Institute
1617 Cole Boulevard
Golden, CO 80401

6.2 Appendix B - List of Research Participants

R. A. Mickelsen - Cell Fabrication and Material Analysis
Wen S. Chen - Cell Analysis and Modeling
R. Hsiao - Cell Measurement
J. M. Stewart - Cell Fabrication
V. Lowe - Material Analysis
G. Henderson - Engineering Aide
G. Wolff - Technician

6.3 Appendix C - List of Reports/Publications/Presentations

Reports

Quarterly Progress Reports

Sixth Quarterly Technical Progress Report, December 1980
Seventh Quarterly Technical Progress Report, March 1981
Eighth Quarterly Technical Progress Report, July 1981
Ninth Quarterly Technical Progress Report, September 1981
Tenth Quarterly Technical Progress Report, January 1982
Eleventh Quarterly Technical Progress Report, April 1982
Twelfth Quarterly Technical Progress Report, July 1982

Publications

1. "Thin-Film CdS/$CuInSe_2$ Heterojunction Solar Cell"; Role of Electro-Optics in Photovoltaic Energy Conversion, Ed. S.K. Deb, Proc. Soc. Photo-Opt. Instr. Eng. 248, p. 62 (1980). Wen S. Chen and Reid A. Mickelsen.

2. "Development of a 9.4% Efficient Thin-Film $CuInSe_2$/CdS Solar Cell", 15th IEEE Photovoltaic Specialists Conf. Record, p. 800, (1981). R. A. Mickelsen and W. S. Chen.

3. "Initial Oxidation of $CuInSe_2$", J. Vac. Sci. Technol., 19, 467 (1981). L.L. Kazmerski, O. Jamjoum, P.J. Ireland, S.K. Deb, R.A. Mickelsen, and W. Chen.

4. "Thin-Film Solar Cells", Design News, p. 38, July (1981). R.A. Mickelsen.

5. "Properties of the Mo-$CuInSe_2$ Interface", Appl. Phys. Lett. 40, 995 (1982). P.E. Russell, O. Jamjoum, R.K. Ahrenkiel, L.L. Kazmerski, R.A. Mickelsen, and W.S. Chen.

Presentations

1. CdS/Cu_2S and CdS/Cu-Ternary Photovoltaic Cells Sub-Contractors In-Depth Review Meeting, September 3-5, 1980. Washington, D.C.

2. Fourth Annual Photovoltaic Advanced Research and Development Conference, November 18-20, 1980. Colorado Springs, Colorado.

3. Workshop on Stability of Thin-Film Solar Cells Based on CdS, February 19-20, 1981. University of Delaware, Newark, Delaware.

4. CdS/Cu_2S and CdS/Cu-Ternary Photovoltaic Cells Sub-Contractors In-Depth Review Meeting, June 2-4, 1981. Golden, Colorado.

5. "Thin-Film Solar Cells" Society of Chinese Engineers of Seattle, November 18, 1981. Seattle, Washington.

6. Polycrystalline Thin-Film In-Depth Sub-Contractors Review Meeting, May 3-5, 1982. Golden, Colorado.

☆ U.S. GOVERNMENT PRINTING OFFICE: 1983-646-069/704