FACTORS AFFECTING THE USE OF CERAMIC CAPACITORS IN PULSE-DISCHARGE APPLICATIONS*

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Introduction

High-energy density, high-current, pulse-discharge capacitors have been utilized at Sandia National Laboratories for many years as the energy-storage medium in firing sets, trigger circuits and as laser power sources. To achieve the required high reliability under often extreme environmental conditions, these capacitors have typically utilized Mylar or mica-paper dielectrics for voltage applications in the 2-6 kV range with peak currents of a few kA having rise times around 100 nsec. or less.

The increased demands for higher-energy density (much lower volume) and lower-cost capacitors as energy storage devices have accelerated Sandia's research and development activities in the potential use of ceramic capacitors for these pulse-discharge applications. The major weakness in utilizing this type of capacitor was its unknown reliability, in this particular usage mode, compared to discrete film-foil capacitors. Continued improvements in fabrication processes, materials and designs have demonstrated that satisfactory pulse-discharge lifetimes can be achieved.

Sandia's progress in this field since C. A. Hall's original studies[1] will be presented showing that some ceramic capacitors from several commercial vendors have demonstrated pulse-discharge lifetimes greater than 100,000 cycles. Derating of the manufacture's rated voltage as a function of required discharge lifetime and operating voltage and changes in capacitance as a function of voltage stress and temperature are also presented for several ceramic capacitors with different dielectrics.

In determining if a capacitor is suitable for Sandia's pulse discharge applications, three probabilistic questions are addressed[2]. *1) Will the capacitor accept charge to rated voltage? 2) Will the capacitor accept charge at rated voltage for a time (t)? 3) Will the capacitor survive N pulse discharges at rated voltage?* These questions are answered experimentally by short-time breakdown (STB) tests, dc life (DCL) tests, and pulse discharge life (PDL) tests, respectively. Hall investigated 0.12 μF and 0.16 μF capacitors from four commercial venders. The composition from vender A exhibited a very linear dc hysteresis loop at 23°C, a negative temperature coefficient of capacitance, and a very low dissipation factor. The dielectric compositions from venders B and C were similar to typical X7R dielectrics which are modified, near-ferroelectric compositions. Their dc hysteresis loops at room temperature were slightly non-linear "S" shaped with very low remnant polarization. Five of the six lots utilized a single chip configuration and the other a 3-chip configuration. All were "rated" at 4 kV by the

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vendors. Hall utilized the STB and PDL tests in his evaluations.

Most of Hall's PDL data was taken at 23°C. The resistive load was adjusted to give a peak current reversal of about 40%, somewhat of an overtest compared to the 15-25% peak negative ringing resulting from most of Sandia's applications. Testing was done at a repetition rate of 12 charge/discharge cycles per minute. Four capacitors from each lot were tested at each condition, i.e. a selected charge voltage. The capacitors were charged/discharged until failure occurred or to a maximum of 10,000 cycles, or in the case from lot A1 and A3 to 15,000 cycles. Four units from lot A1 achieved 10,000 cycles at 23°C and 15,000 cycles at both -55°C and at 74°C, all at 3.4 kV. However, for the other three lots from vender A and the individual lots from venders, B, C & D, most of the other capacitors failed to achieve 10,000 cycles at even 3.0 kV. Nearly all of the capacitors did achieve 10,000 cycles at 2.0 kV, i.e. good results at 2.0 kV, but inconsistent results at the next test level of 2.5 kV.

All of the STB data was obtained at 23°C with average breakdown voltages between 5.3 kV and 6.0 kV. The associated standard deviations were between 0.3 kV and 0.7 kV. No DCL data was obtained for these units. Twelve capacitors from lot A3 were successfully cycled 1000 times, followed by 25 thermal shocks between -65°C and 125°C. They were then successively cycled another 1000 times. Ten of twelve capacitors then survived 10,000 cycles at 23°C, followed by 15,000 cycles at both 74°C and -55°C. The other two units failed much earlier at 23°C (about 1000 cycles) and -55°C (about 500 cycles).

Even though it appeared that these particular capacitors would have to be derated by about a factor of two, the PDL performance up to 10,000 to 15,000 cycles with peak current outputs between 2 and 4 kA (rise times on the order of 100 nsec.) was encouraging, as was the performance after the series of thermal shocks. These early results were sufficient to warrant additional research and development.

Our customers are interested in utilizing these high-energy density ceramic capacitors for two general application areas; the first requires approximately a 0.1 μF capacitor charged to 1.0 kV (single chip design) and the second application requires an identical capacitance charged to 3 kV (multi-chip design). Consequently, the decision was made to focus on separate capacitor designs that could operate reliably at these two voltage levels. The following table indicates the present design mix with respect to proposed operating voltage and dielectric composition. Most of the vender designations in this report are not related to Hall's report, and most of the ceramic configurations are different, even though there are two venders common to his and this study.

Table 1

Vendor	Dielectric Type	Voltage
A	X7R	1 kV
A	X7R	3 kV
B	NTC	3 kV
B	X7R	1 kV
B	X7R	3 kV
C	NTC	1 kV

Process Improvements

Commercial ceramic capacitors have not been designed specifically for pulse discharge applications, so one aspect of our current program is to focus on the identification of design and/or process defects which cause infant mortality during pulse discharge. Problems encountered include electrode-corner failures, surface-arcing failures and end termination-electrode tab interface problems.

The electrode-corner failures (for one vender) were solved by simply eliminating the relatively sharp electrode corners via radiusing. Surface-arcing failures (again for one vendor) between their closer-spaced end terminations were eliminated via painting the four major ceramic surfaces and the end terminations themselves with a dielectric coating. Gull-wing tabs were soldered to each end termination prior to painting on the dielectric coating.

The gull-wing electrode tab is attached to the end termination via two methods for the 3.0 kV capacitors (all rated at 4 kV by all of our venders). In one case, solder is utilized for the attachment and in the other silver conductive epoxy. Results to date indicate superior performance with the silver epoxy with respect to PDL results. The solder joint generally fails between 5000 and 20,000 pulse-discharge cycles. This particular vender is investigating how to improve the solder interface. The capacitors with the Ag-epoxy joints

fail between 50,000 and greater than 100,000 cycles.

To achieve the required fast rise times, 100 nsec. or less, requires a very-low total loop inductance. Initially, some ceramic capacitors had about 40 nH total circuit inductance, which is too high for our applications. This design had internal electrodes that were perpendicular to the discharge path. When the external tabs were rotated 90°, the internal electrodes were now parallel to the discharge path, and the total inductance was reduced to less than 8 nH.

Capacitance as a Function of Voltage and Temperature

For a ceramic capacitor to function reliably as the firing set energy source, two requirements must be met; 1) After "seeing" N cycles in various subassembly tests, it must survive the N + 1 cycle and 2) The capacitor must deliver a minimum threshold energy to the load based on $\frac{1}{2}CV^2$. While the voltage is the dominant factor in increasing energy density, and hence our interest in assuring reliable capacitor charge and discharge at a sufficiently high voltage level, the variation in capacitance with temperature, aging, and voltage is also very important. Hall's initial work[1] utilized the X7R and NTC dielectrics, and we have since continued to work with minor variations of these compositions (they vary from vender to vender). The variations in capacitance for these two dielectrics with temperature are familiar[1]. Low-signal capacitance as a function of time for several dielectrics is shown in Figure 1. This time variation is very important for Sandia's applications, as our capacitors may be utilized in systems that may be employed for 25-50 years.

Most ceramic capacitor manufacturers are only concerned about low-signal characterization of their product. However, an accurate, effective value of capacitance at 1 kV to 3 kV (or whatever is the actual bias voltage) is required to know the exact energy delivered to the load for our pulse-discharge applications. Sandia developed a simple, but effective, method of determining capacitance as a function of voltage. The measurement method is based on

$$I = C\, dV/dt \qquad (1)$$

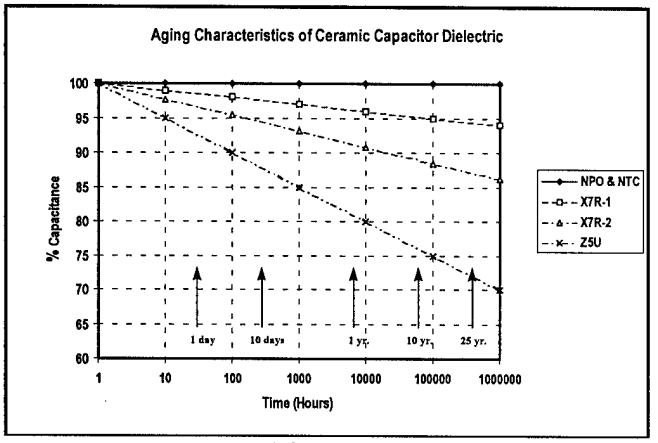

Figure 1

A constant, linear voltage ramp of 250 volts/sec. is applied to the ceramic capacitor under test, and a series ammeter is used to measure the displacement current as a function of the applied voltage. Since dV/dt is a constant, the current, I, is directly proportional to capacitance, and the capacitance vs. voltage function can be plotted as shown in Figures 2-4. (In Figures 2-5, 7-9 and 10-13, all capacitance values in the figure captions refer to the vender's low-signal, rated values). In these tests, the voltage

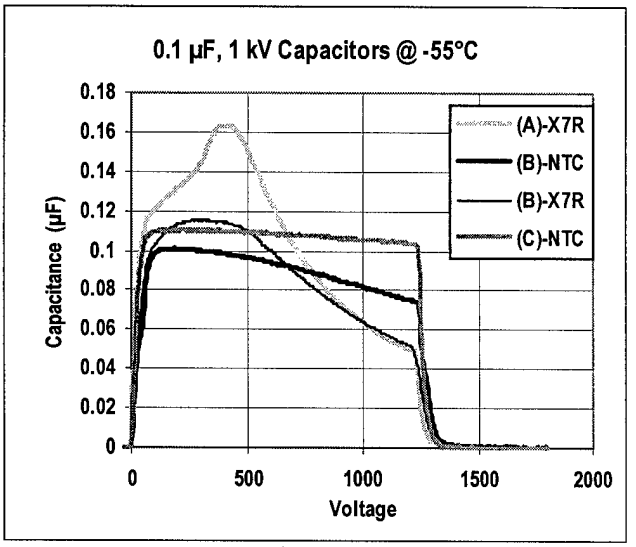

Figure 2

ramp was discontinued in the 1200 to 1300 volt range, as we were interested in these particular capacitors for 1.0 kV applications. Data is presented for capacitors from three venders designated as A, B and C at -55°C, 23°C and 74°C in the three figures respectively. Vendor A's material is X7R, vender B has samples of both X7R and NTC materials, and vender C's material is NTC.

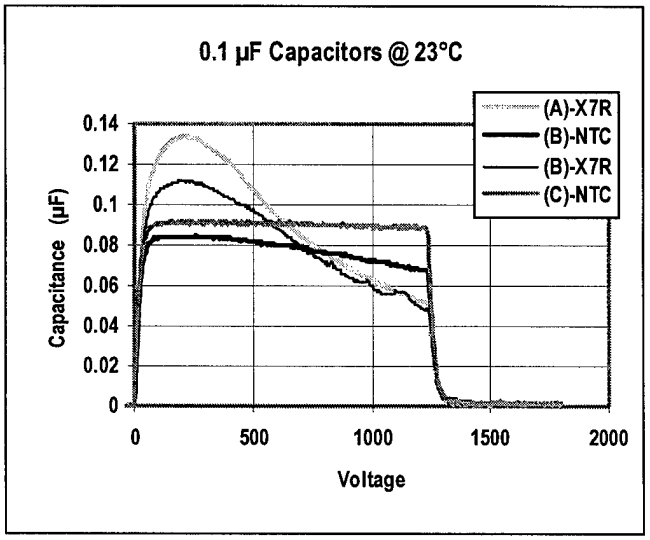

Figure 3

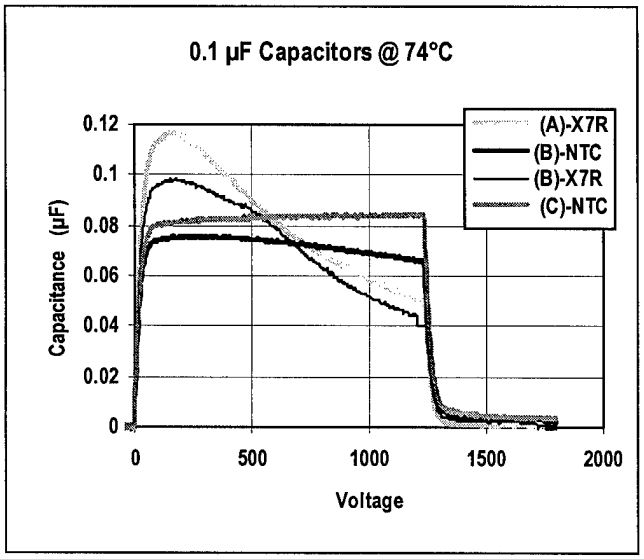

Figure 4

Note that the effective capacitance at 1.0 kV is much higher for the NTC dielectrics as compared with the X7R dielectrics. However, the NTC material from vender C is clearly superior to that from vender B. One can also, of course, see the expected continuous decrease in capacitance as temperature increases for the NTC material. Note that at 1.0 kV, the capacitance of the "X7R capacitors" is about 60% of the manufacturer's rated low-signal values.

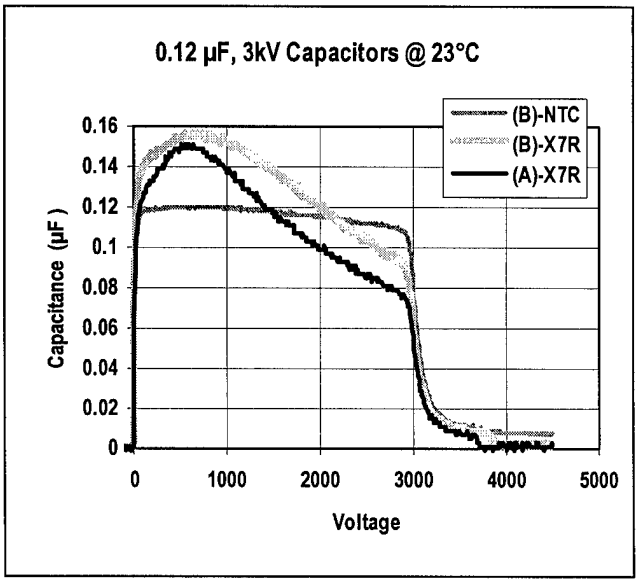

Figure 5

Similar data is presented in Figure 5 for different capacitors intended to operate at 3.0 kV. Only room temperature data is presented. Also note that no data is presented for vender C because this vendor has not yet provided any capacitors to operate near the 3.0 kV level. Again, one sees that the NTC material from Vender B indicates much less loss in capacitance than either of the X7R capacitors from Venders A or B. (In retrospect, the voltage ramp on this test should have been extended to about 3.3 kV so a more accurate capacitance at 3.0 kV could be determined. Remember the sudden drop in capacitance does not represent a voltage breakdown, but simply a discontinuation of the input ramp bias voltage).

1.0 kV PDL Data

Over the course of this development effort, our customers, due to system considerations, asked us to emphasize development of 1.0 kV capacitors compared to the "3.0 kV designs". Consequently, most of the remaining data presented in this report is for the lower-energy applications. All of our 1.0 kV test capacitors were rated at 1.5 kV by the venders. However, a small amount of corresponding data will be presented for ceramic capacitors specially designed for the higher, 3.0 kV operating voltage.

Data (percent sample remaining vs. cycles) is presented in Figure 6 for capacitors (1-chip design) utilizing vender C's NTC dielectric. By plotting the data in this way, the average slope is

the failure rate. L. R. Edwards has shown that the exponential distribution model[3] or constant

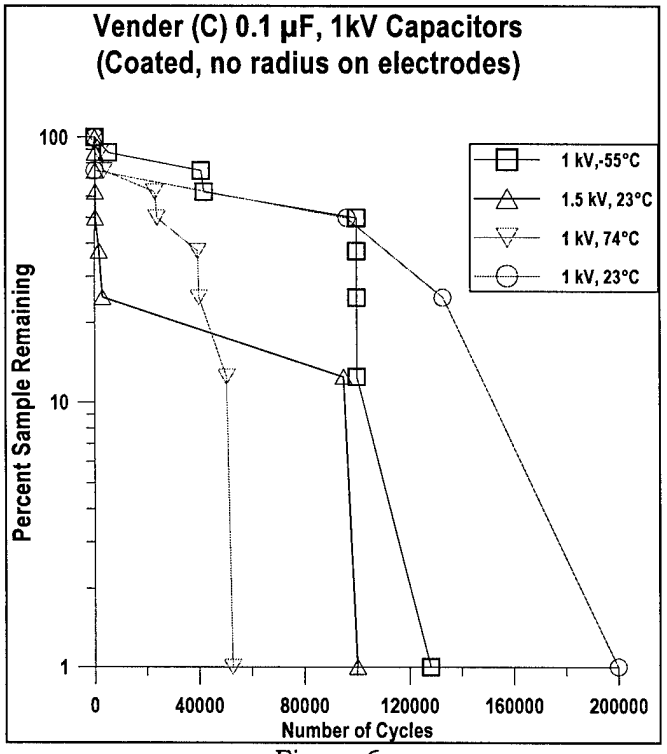

Figure 6

failure rate model is suitable for both dc life and pulse discharge life (PDL). For example, the probability (P) of surviving "c" cycles (equivalent to percent sample remaining) is given by:

$$P = e^{-Qc} \qquad (2)$$
$$\ln P = -Qc$$

where Q is the failure rate in number per cycle and c is the number of charge/discharge cycles. Of course an accurate slope cannot be obtained with only eight data points for each test condition. One is really interested in the early failure rates or the failure rate in the first several hundred cycles, but if we have "good" capacitors, we won't be able to obtain these data because failures won't occur until several hundred thousand cycles. Edwards also demonstrated that an accurate estimate of the "early failure rate" can be attained by plotting the log (1-P) vs. log c which effectively moves the data points to the right of the plot thus permitting a slope extrapolation back to lower values of c to obtain the "early failure rate".[3]

Arcing between end terminations occurred on uncoated capacitors from vender C as the spacing between end terminations was less than corresponding capacitors from the other venders. There were four uncoated test samples for each PDL test (this data is not shown) and eight coated samples for each test (as shown in Figure 6). Significant PDL performance improvement was obtained for each of the three test temperatures with the coated capacitors. We also see the substantial PDL performance degradation as the operating voltage is increased from 1.0 to 1.5 kV (data at 23°C for this single-chip design). Again, these capacitors are specifically designed for the 1.0 kV level. The data also indicates decreased performance at the high temperature test condition as compared to the room temperature results.

Data was also obtained on vender A's X7R parts at 1 kV (this data is not plotted). Three groups of four capacitors were also tested at -55°C, 23° and 74°C. All capacitors survived 100,000 cycles at the cold and hot extremes, but only two survived to 100,000 cycles at room temperature. One failed around 1000 cycles and the other at about 20,000 cycles. These data on the two dielectrics from two venders indicate significant performance improvements compared to Hall's early results, but still illustrate that more work is needed to understand and eliminate the "early" failures. We must next obtain similar data on a much larger sample base, so accurate predictions of failure rates can be obtained.

Representative output current wave-forms at 1 kV into a ¼ ohm load for vendor A's X7R capacitors and for vender C's NTC capacitors are shown for -55°C, 23°C, and 74°C in Figures 7-9 respectively. Note that the NTC material provides higher output current at every corresponding temperature than does the X7R material, the peak output current for the NTC material decreases as temperature increases, and that the peak current for the X7R material remains about constant or perhaps slightly increases as the temperature increases.

It can be easily shown that for a capacitor charged to voltage V and discharged into a series L-R-C circuit, the magnitude of the output current (for the under damped, ringing case) is proportional to the square root of C/L.[3] One can then see that the variation in the amplitudes of the output currents in Figures 7-9 follow fairly well the respective variations in capacitance at 1.0 kV from Figures 2, 3, and 4.

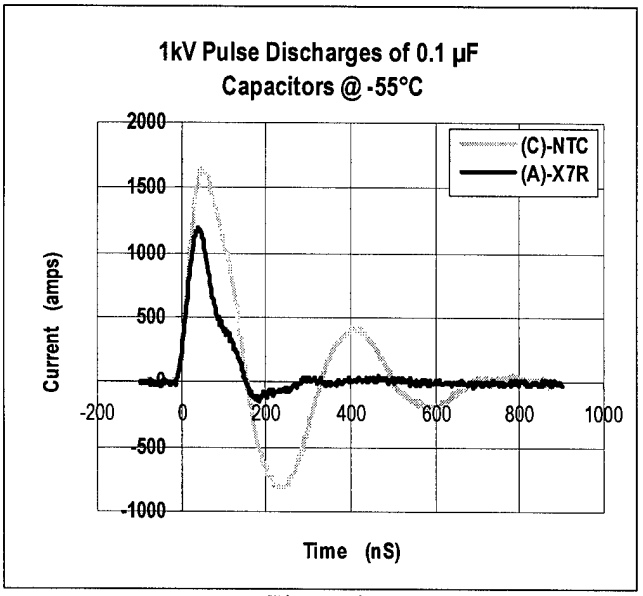

Figure 7

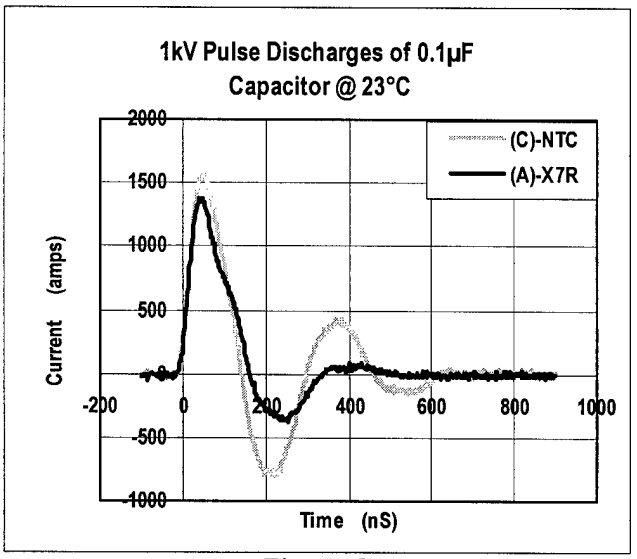

Figure 8

Of course, the NTC material's low-signal capacitance has greater variation with respect to temperature than the X7R. X7R's temperature variation depends on the vender, but it is typically about the same at -55°C and at 74°C with a relatively small peak between about 0°C and 30°C.[1] However, the combination of temperature variation and voltage sensitivity in the X7R dielectrics is more detrimental to pulse discharge output than the negative temperature variation of the NTC dielectrics.

3.0 kV PDL Data

Pulse discharge data is shown in Figure 10 for vender B's X7R material. Four separate samples were tested at each of our three temperatures. No failures were encountered at 74°C at the 100,000-cycle level, while some failures occurred before this level at the other two test temperatures. Figure 6 (for the 1.0 kV data).

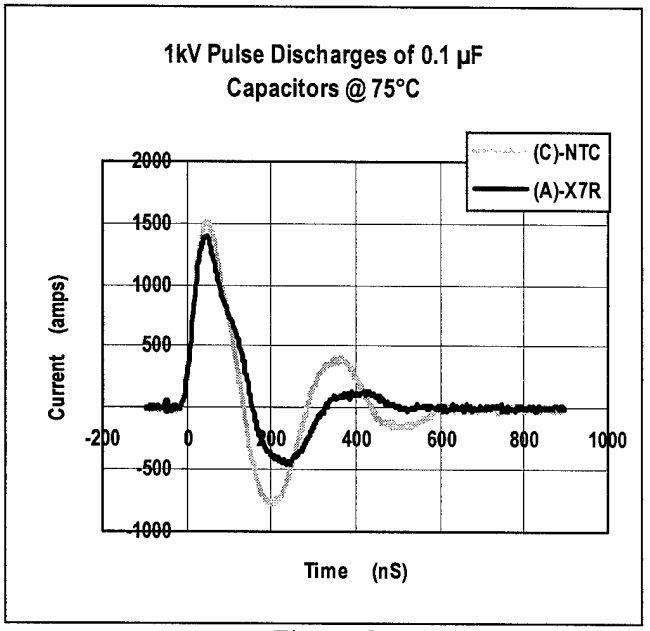

Figure 9

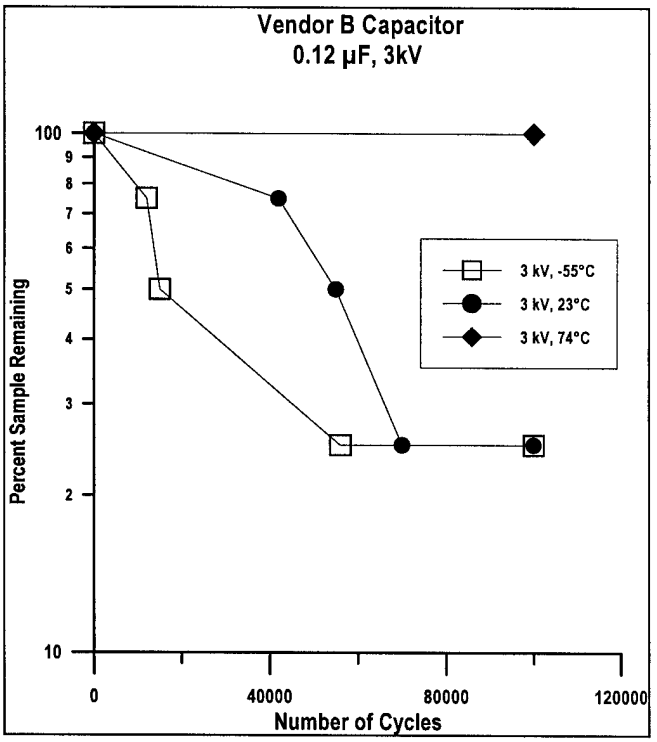

Figure 10

indicated superior performance at 23°C with the worst performance (highest slope) at 74°C.

Clearly, we do not yet have sufficient data to make an accurate determination on failure rates or lifetimes as a function of temperature. By utilizing larger samples, we can improve the accuracy of the failure rate estimates and provide statistical bounds.

Output waveforms for vender A's X7R material and vender B's NTC material (remember vender C has not yet provided us with a NTC capacitor that will operate at 3.0 kV) are shown in Figures 11, 12 and 13 for temperatures -55°C, 23°C and 74°C respectively.

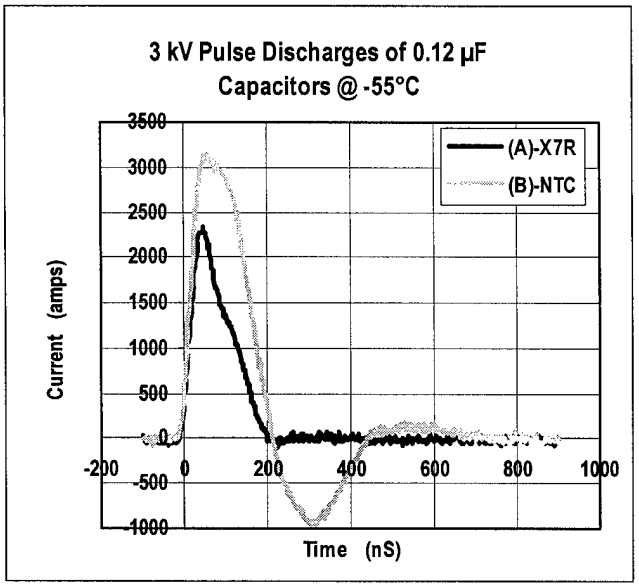

Figure 11

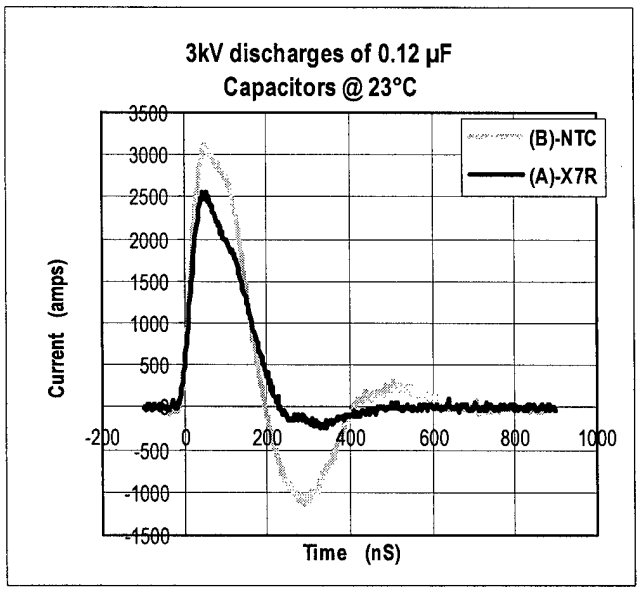

Figure 12

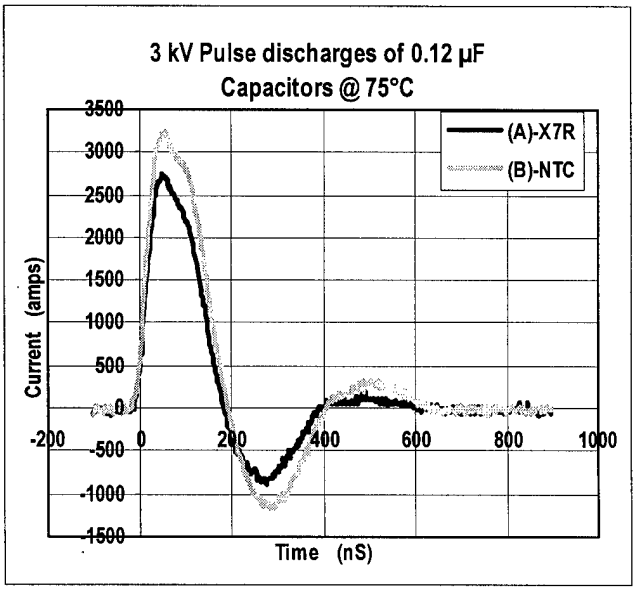

Figure 13

Unfortunately, we now only have C = f(V) data at 3.0 kV for 23°C (Figure 5). Again one notes that vender B's NTC material results in a higher peak output current than vender A's X7R dielectric. In fact, if one takes the square root of the ratio of the two capacitor values at 3.0 kV (from Figure 5), the result is about 1.20, which is almost the same ratio of the peak currents from Figure 13, i.e. about 1.24. Additional data from these two venders will be accumulated at 3.0 kV at all three temperatures of interest.

Summary

Improvements in processing and dielectrics, minor design changes, and expansion of our data bases via expanded testing and inclusion of candidate capacitors from additional vendors have demonstrated increases in pulse-discharge lifetimes from around 10,000 in 1993 to over 100,000 today. PDL tests utilizing much larger sample sizes on the capacitors of principle interest must be completed to obtain failure rate estimates and bounds, particularly after several hundred cycles. Accurate determinations of "large-signal" capacitance, or the value at the bias voltage, enables us to predict the energy and peak current delivered to the detonator load.

It still appears that the commercial venders' voltage ratings must be derated by approximately 25% to 33% for reliable pulse-discharge applications in the 1.0 kV to 3.0 kV operating range. Correspondingly, the capacitances at the actual bias voltages are some 15% to 40% lower than the venders' low signal capacitance values

(the capacitance "derating" is dependent, of course, on composition and operating temperature). Improved, demonstrated performance, higher energy density, and relatively lower costs, compared to discrete film/foil capacitors make these ceramic capacitors even more attractive for this type of application.

Acknowledgments

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[1] Hall, C. A. and Jacobs, E. L., "Characterization of Ceramic Capacitors for High-Voltage Pulse-Discharge Applications," CARTS'93, pp. 116-123, Costa Mesa, CA, March 8-11, 1993.

[2] Edwards, L. R., "Reliability Performance of Pulse Discharge Capacitors," CARTS'97, pp. 292-297, Jupiter, FL, March 24-27, 1997.

[3] Edwards, L. R., "A Potential CDU Capacitor Design for Conventional Weapons Applications," SAND96-1607 UC-706 (Export Controlled Information), July 1996.

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